國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

二位元分離式閘極氮化矽快閃式記憶體之
先進操作方法探討

The Investigation of a Novel Operating Method for
Two-Bit Split Gate SONOS Flash Memory

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研 究 生 ： 周承翰　　Student : Chen-Han Chou

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碩士論文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics College of Electrical and Computer Engineering

National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of Master of Science

in Electronics Engineering

July 2011

Hsinchu, Taiwan, Republic of China.

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摘要

此論文將提出在二位元分離式閘極氧化矽快閃式記憶體上先進的操作方法。在許多種不同的分離式閘極結構，源極注入(SSI)最常被使用在寫入以及帶對帶電洞入射(BTBHHI)則是用於抹除。有鑒於常見入射電荷的操作方法下，電子與電洞在底層氧化層的反應將會導致些可靠度上的議題，還有，底層氧化層的應力感應漏電流(SILC)現象已經在快閃記憶體中被視為主要的可靠度議題。在不同的抹除方法中,熱電洞入射引起的氧化層退化已被發現是蠻嚴重的情形，論文裡我們將提出新的抹除操作模式來抑制抹除對氧化層的破壞。

首先關於新的操作模式的電壓時間關係使用了多循環脈衝系列來加強寫入/抹除的效率,在寫入方法中-順向偏壓促進電子入射(FBEI)是由順向偏壓促進電子入射以及新的抹除方法-順向偏壓促進熱電洞入射(FBHHI)則是藉由合適的順向偏壓來產生電洞,FBEI可以達成低電壓以及高速度的操作目的，而抹除時使用FBHHI可以比BTBHHI用更少的時間產生更多的電洞。從實驗結果可得知新的操作模式比常見的操作更可靠。

最後，我們利用特殊的分離式閘極結構來分析不同的寫入方式造成的電荷分佈以及第二位元的影響(SBE)，並且在二位元的操作上使用多循環脈衝系列的操作方式，我們可以得到相對於常見的操作較好的性能及可靠性表現。

The Investigation of a Novel Operating Method for Two-Bit Split Gate SONOS Flash Memory

Student：Chen-Han Chou Advisor：Dr. Steve S. Chung

Department of Electronics Engineering & Institute of Electronics

National Chiao Tung University

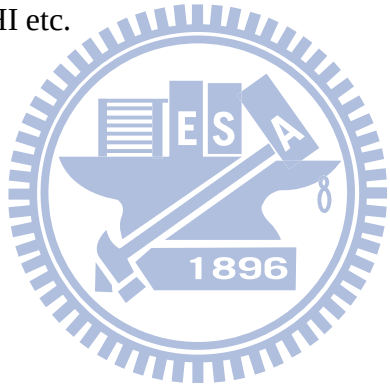
ABSTRACT

In this thesis, a novel operating scheme has been proposed for 2-bit/cell split gate SONOS. For a certain design of split gate structure, source-side injection (SSI) is usually used for programming and band-to-band hot hole injection (BTBHHI) is used for erase. By using the conventional operating method of charge injection, the interaction between the generated electron and hole pairs could cause the reliability issue for bottom oxide. Stress induced leakage current (SILC) at the bottom oxide has been discussed as a major reliability issue in flash memory. Among different erase method, hot hole injection induced oxide degradation has been found to be most serious condition. In thesis, we propose the new operating scheme to suppress the oxide damage during erase.

First, the new timing diagram for novel operating scheme used the multi-cycle pulse series to enhance the efficient of Program/Erase. For the programming method, Forward bias assisted Electron Injection (FBEI), achieved by forward-bias assisted electron injection, the new erase method, Forward Bias assisted Hot Hole Injection

(FBHHI), achieved by suitable forward-bias assisted hole generation were proposed. A lower voltage operation and high speed operation can then be implemented in FBEI program. For the erase, FBHHI can supply more holes and less time than BTBHHI in the same operation condition. The results showed that the new operation schemes are more reliable than conventional operation.

Finally, we used the specific split gate structure to analyze the charge profiling of various program methods and second bit effect (SBE). And then, a 2 bit/cell operation for split gate SONOS by using multi-cycle pulse series, in which better performance and reliability can be achieved in comparison to conventional operation scheme, e.g. SSI or BTBHHI etc.



Acknowledgements

碩士生活的兩年是短暫卻又充實的，交織著酸甜苦辣的實驗室日子。首先要感謝我的指導教授莊紹勳老師，莊老師不僅在研究上給予許多指導建議，教我應具有的研究精神跟態度，並在課業與生活上，也有許多的關懷，在此深表我對老師的感謝。

感謝何永涵學長在實驗研究上的細心教導，並且給予我許多的建議跟指導，感謝曾元宏、鄭世嵩、程政穎學長，給予學業跟實驗上的解答跟協助。還有感謝這兩年研究生涯的夥伴嘉偉、志宇，在日常的生活中，因為有你們，讓實驗研究生活變得更加有趣，相信數年後再聚，定倍感溫馨。也感謝汪老師研究群的邱榮標學長，雖然在不同的研究群中，但實驗室有你們，使得乏味的實驗室生活更多采多姿。此外，也感謝學弟蔡政達、黃英傑、蔡漢旻、蔡侑璉，感謝你們對實驗室的付出，使得學長們能專心於實驗研究上，真心的祝福你們明年可以順利畢業。總歸一句，感謝所有的夥伴，因為有你們，使我這兩年研究生活豐富且精彩，即使艱辛，仍充滿歡笑。

另外，在此也要感謝聯華電子在測試元件和儀器上的協助，讓本研究才得以順利完成。

最後要感謝我家人們，你們是我最大的精神支柱，有了你們的支持和鼓勵，讓我能堅持到現在。

謹將這份榮耀獻給培育我多年的父母親。

Contents

Table Caption

Table 4.1 The basic operation conditions of planar SONOS.

Figure Captions

Chapter 3

Chapter 4

Chapter 5

Fig. 5.14 Retention behaviors after 10k P/E of Bit-1 at Vth_{high} and Vth_{low} states with FBEI/FBHHI and SSI/FBHHI combinations.

Chapter 1

Introduction

1.1 The Motivation of This Work

In charge-trapping devices, such as SONOS memory, 2-bit per cell operation becomes the basic requirement of a flash memory, which is also a popular solution for the cell scaling. So far, many unique gate structure cells [1][2] have been proposed to improve the non-volatile memory (NVM) performance based on the operation scheme approach. For the specific split gate structure [3], in most cases, the cell is programmed by channel hot electron (CHE) or source-side injection (SSI) [1], while erase is achieved by band-to-band hot hole injection (BTBHHI) [4]. Based on a forward-bias assisted electron injection (FBEI) scheme that our group developed in [5], where a low voltage, high speed program, and excellent data retention could be achieved. From various erase mechanisms, a major reliability issue in flash memory is the hot hole injection induced oxide degradation [6]. The positive charge-assisted tunneling (PACT) was found to be a dominant stress induced leakage current (SILC) mechanism in HH stress [7]. An efficient erase method forward-bias assisted hot hole injection (FBHHI) was then developed to improve the BTBHHI erase scheme by using the suitable forward bias in drain/substrate p-n+ diode. As a consequence, the experimental result was demonstrated that FBHHI erase can suppress the oxide damage.

The charge distribution profiling in charge-trapping memory have been studied by various methods of charge-pumping [8][9]. They were used to investigate the

charge profiling of the dielectric layer with only program or erase condition. Nevertheless, it becomes more inaccurate after P/E cycles. In a fixed voltage base (FVb) charge pumping method, by further improving the method in [10], the hole-electron misalignment and oxide degradation of operation after P/E cycling can be further understood. Therefore, we can easily distinguish the residue charge of the dielectric layer under different program/erase combinations.

In this thesis, we used the specific split gate structure to study the charge distribution with various program methods and the second bit effect (SBE). And then, the new operation schemes for program/erase which are applicable for 2 bit/cell operation has been discussed. The degradation of bottom oxide can be suppressed in comparison to conventional operation scheme by using the multi-cycle pulse approach. Finally, we will draw a conclusion of the thesis.

1.2 Organization of the Thesis

The organization of this thesis consists of six chapters. After a brief introduction in Chapter 1, we will introduce the experimental devices and experimental setup in Chapter 2, which includes the operating schemes, program and erase, and the measuring method of charge pumping. In Chapter 3, we will introduce the mechanisms of FBEI and FBHHI and we will compare the performance and reliability with different program/erase schemes. In Chapter 4, we will explain the phenomenon of charge-pumping method in planar SONOS devices, which led to a development of a new monitor, defined as A. As a consequence, we will study the different operation combinations with this new parameter area A. In Chapter 5, we will focus on the second bit effect in split gate SONOS and the endurance and the retention of two bit

operation in different pulse series type will be discussed. Finally, the summary will be presented in Chapter 6.

Chapter 2
Device Fabrication and Equipment Setup

2.1 Introduction

This chapter is divided into four sections. First of all, both split-gate SONOS and the conventional SONOS cells used in this study will be described. Second, the instruments setup and the experimental techniques to accurately control these instruments are illustrated. Third, we will discuss the new programming and erasing schemes of these cells. Finally, charge pumping measurement technique setup used in this study will be demonstrated.

2.2 Device Fabrication

Figure 2.1 is the schematic diagram illustrating the fabrication of split-gate SONOS. As shown in Fig. 2.1(a), a substrate is provided, and a P well is formed in the substrate. Then, a plurality of control gate structure is formed on the P well. Each control-gate structure from bottom to top includes a gate insulating layer, a control gate oxide (65Å), and a cap nitride layer. As shown in Fig. 2.1(b), a silicon oxide layer (not shown), a nitride layer (not shown) is deposited on the substrate and control gate structure, and an etching back process is then performed to form a plurality of sacrificial spacers alongside each control gate structure. Meanwhile, a plurality of opening is formed between any two adjacent sacrificial spacers to expose the P well. Afterward, an implantation process is performed via each opening to form a plurality of N doped regions, serving as buried bit line, in the P well. As shown in Fig. 2.1(c), the sacrificial spacers alongside each control gate structure are removed. Then, a

composite dielectric layer is formed on the P well, the control-gate structure, and the N doped regions. In this embodiment, the composite dielectric layer is an ONO tri-layer dielectric including a bottom oxide layer (60Å), a nitride layer (90Å), and a top oxide layer (90Å). As shown in Fig. 2.1(d), a conductive layer is entirely deposited on the composite dielectric layer, and a photolithography and etching process is performed to define a plurality of parallel word line, which are perpendicular to the control-gate structure, as shown in Fig. 2.1(e) [11]. The SEM image and the 2D-TCAD simulation structure of dual-bit split-gate SONOS are shown in Fig. 2.2 (a) and Fig. 2.2 (b). The gate width is 0.2um, and the channel length is 0.18um under control-gate and three different word gate length (L_{WG}) splits (0.13um, 0.12um, 0.10um) under the word-gate.

The conventional SONOS cell used in this study is first grown by thermal oxidation with thicknesses of 50 Å. Next, a layer of 60 Å LPCVD nitride film is grown. Finally, the LPCVD blocking oxide is grown with thickness of 50 Å. (W/L=0.7/0.26 um)

2.3 Equipment Setup

The experimental setup for the I-V and transient characteristics measurement of SONOS is illustrated in Fig. 2.3. Based on the PC controlled instrument environment via HP-IB (GP-IB, IEEE-488 Standard) interface, the complicated and long-term characterization procedures during analyzing the intrinsic and degradation behaviors in SONOS cells can be easily achieved. As shown in Fig. 2.3, the characterization apparatus with semiconductor parameter analyzer (HP 4156C), dual channels pulse generator (HP 8110A), low leakage switch mainframe (HP E5250A), and a probe

station provides an adequate capability for measuring the device I-V characteristics and executing the SONOS cell program/erase operation.

Source-monitor units (SMU) and provided the high current resolution to 10^{-15}A range facilitates the gate current measurement, sub-threshold characteristics extraction, and the saturation drain current measurement. The HP E5250A equipped with a 10-input (6 SMU ports and 4 AUX ports) × 12-output switching matrix, switches the signals from the HP 4156C and the HP 8110A to device under test (DUT) in probe station, automatically. In addition, the HT-Basic are used as the program languages to achieve the personal computer (PC) control of these measurement instruments.

2.4 Programming and Erasing Setup

The general programming and erasing schemes for the conventional SONOS are Channel Hot Electron Injection (CHEI) and Band-to-Band Tunneling Hot Hole Injection (BBTHHI). For CHEI programming, source and substrate are grounded, while gate and drain are connected to the pulse generator as shown in Fig. 2.4 (a). The pulse timing diagram for both gate and drain are shown in Fig.2.4 (b). For BBTHHI erasing, substrate is grounded, and gate and drain are connected to the pulse generator just like CHEI, but keeps bulk floating this time as shown in Fig. 2.5 (a). The pulse timing diagram for both gate and drain are shown in Fig.2.5 (b). The novel programming scheme and erasing scheme for the split gate SONOS are Forward Bias assisted Electron Injection (FBEI) and Forward Bias assisted Hot Hole Injection (FBHHI). For FBEI programming, source is floating and substrate is ground, while gate and drain are connected to the pulse generator as shown in Fig. 2.6 (a) The pulse timing diagram for both gate and drain are shown in Fig. 2.6 (b). For FBHHI, source

is floating and gate is grounded, while gate and substrate are connected to the pulse generator as shown in Fig. 2.7 (a). The pulse timing diagram for both gate and drain are shown in Fig.2.7 (b). The operation mechanism and relevant measurement of FBHHI will be discussed after this chapter.

Dual-bit split-gate SONOS operates as conventional does, but adding a control-gate bias in the middle of the cell. The control-gate keeps a small constant bias for programming, while floating for erasing. And the other terminals are just the same as conventional operation.

2.5 Charge Pumping Measurement Technique Setup

The charge pumping measurement technique setup is shown in Fig. 2.6, which we called fixed based charge pumping, but with minor difference from the traditional one. The pulse generator is connected to the gate, and with the substrate and drain connecting to the HP4156C, while source is kept floating. Fig. 2.8 (a) shows the pulse series type sending out from the pulse generator used by this setup. By using this setup, we can measure the charge pumping current from drain. If one wants to measure the charge pumping from drain (/source), we should connect the HP4156C with them and open the source (/drain) to get the information of the charge pumping current. The second scheme for charge pumping measurement technique setup is shown in Fig. 2.8 once again. However, the pulse series type is different this time. As shown in Fig. 2.8 (b), we used likely the traditional fixed top charge pumping pulse series to do our measurement.

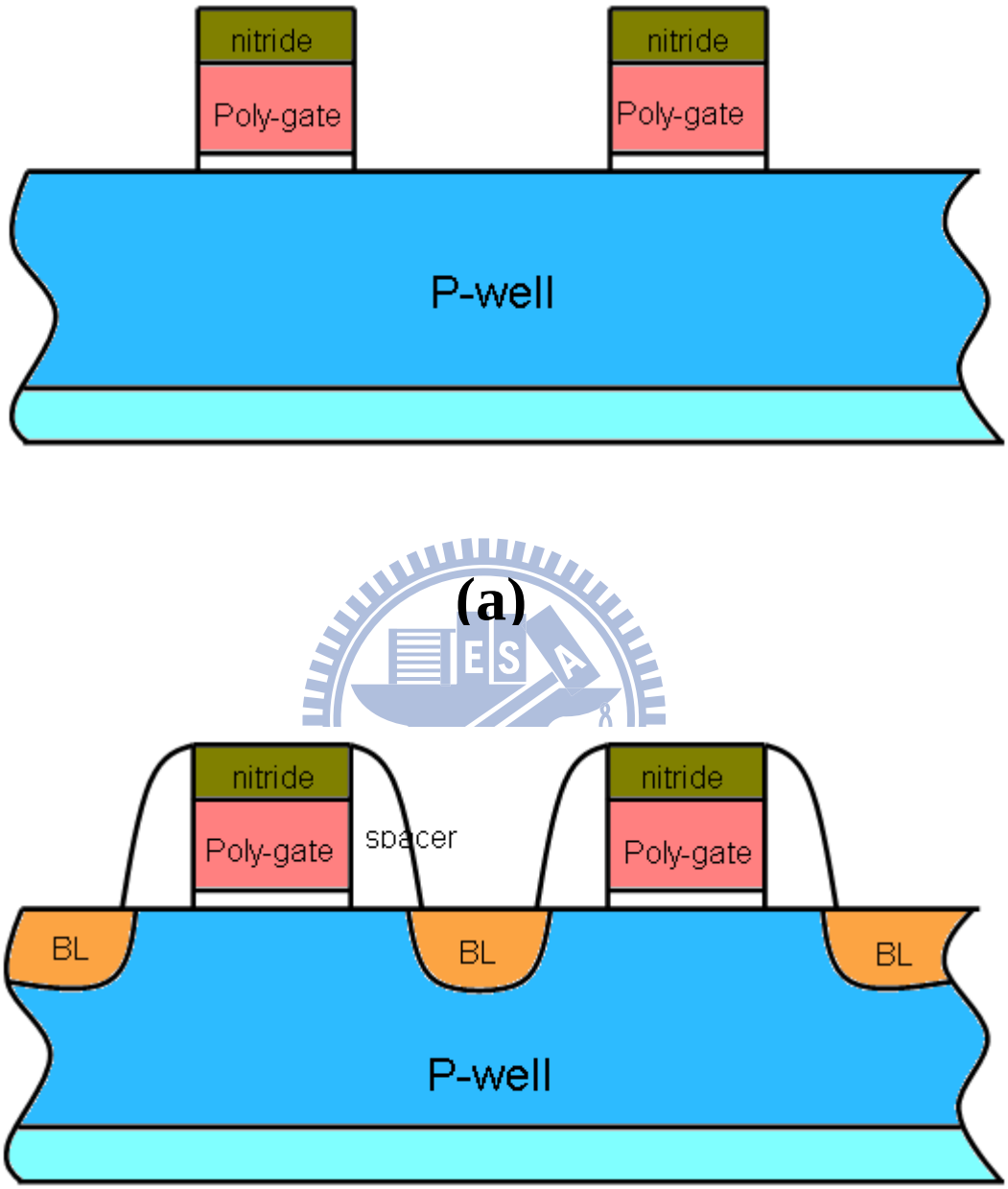


Fig. 2.1 The schematic diagram illustrating of forming the dual-bit split-gate SONOS.

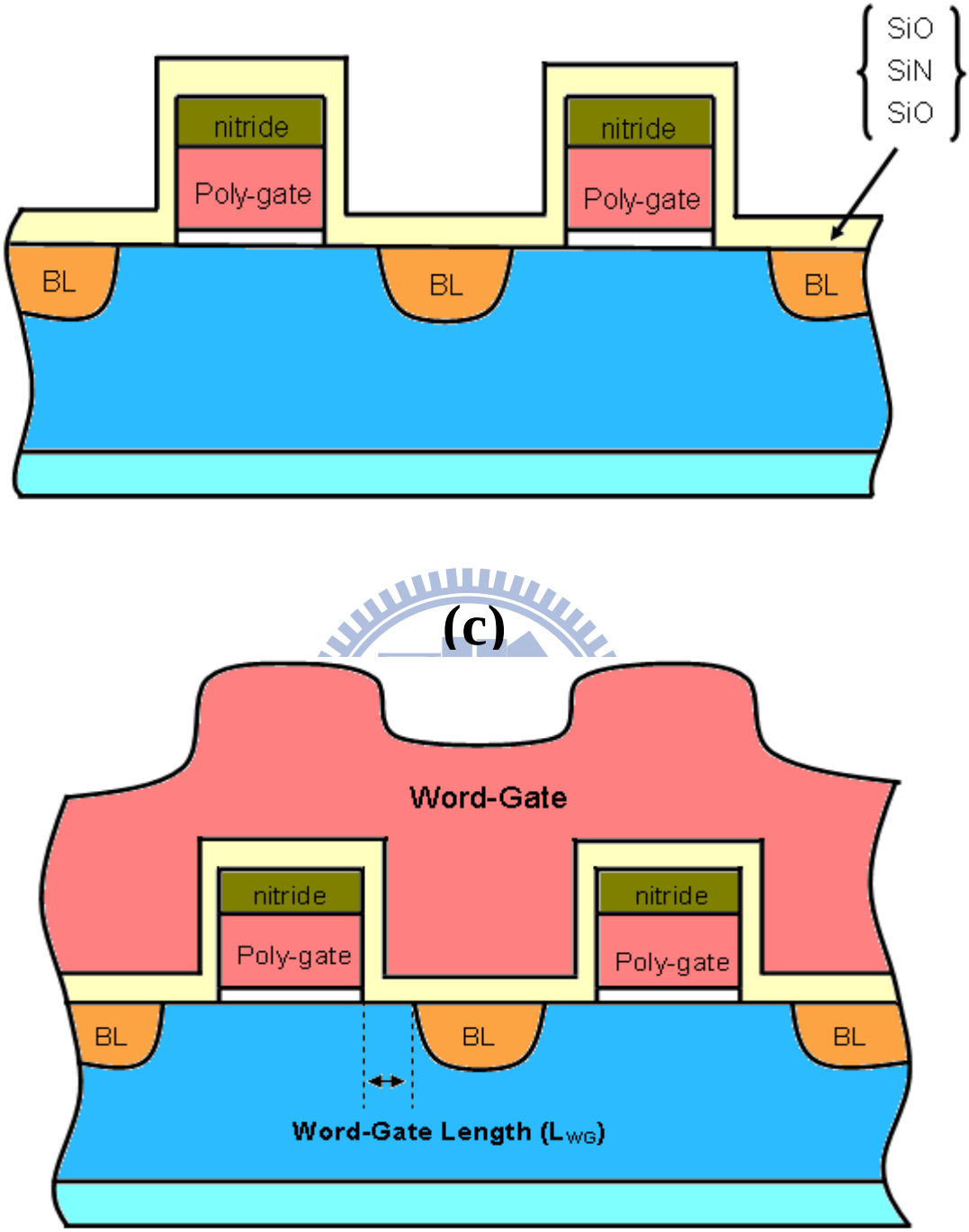
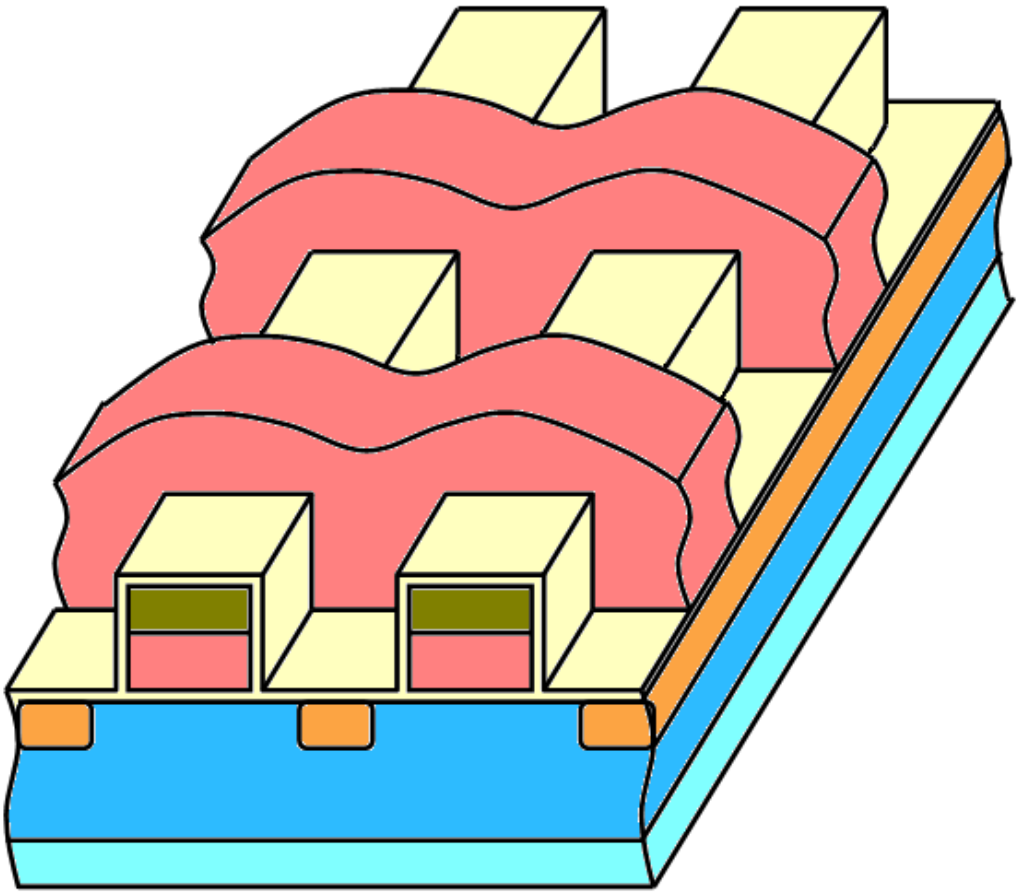
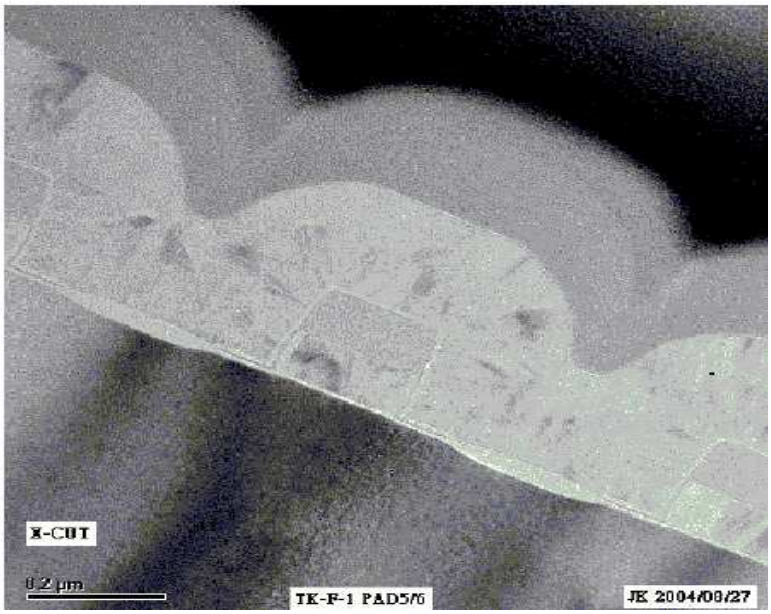


Fig. 2.1 The schematic diagram illustrating of forming the dual-bit split-gate SONOS.

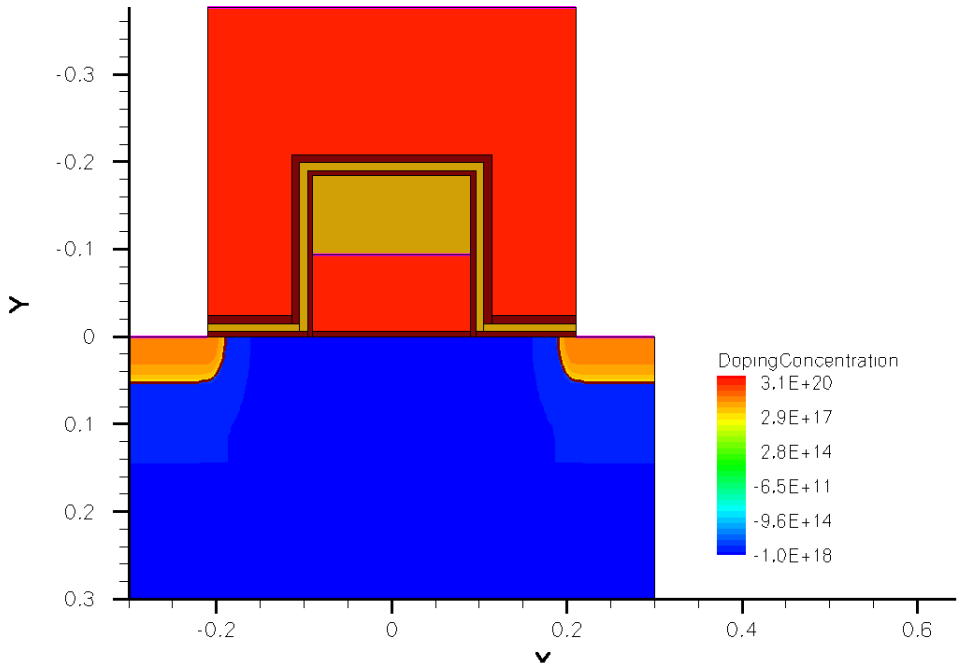


(e)

Fig. 2.1 The schematic diagram illustrating of forming the dual-bit split-gate SONOS.



(a)



(b)

Fig. 2.2 (a) The SEM image and (b) the simulation structure of the dual-bit split-gate SONOS.

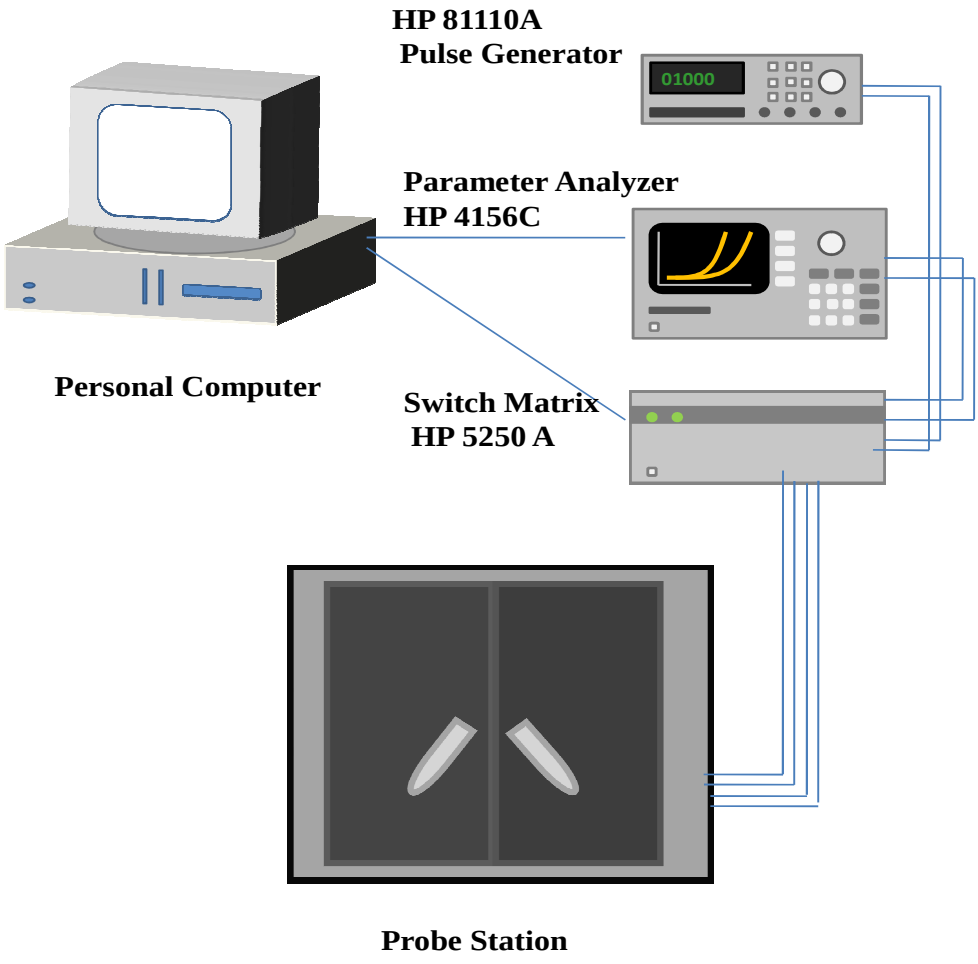
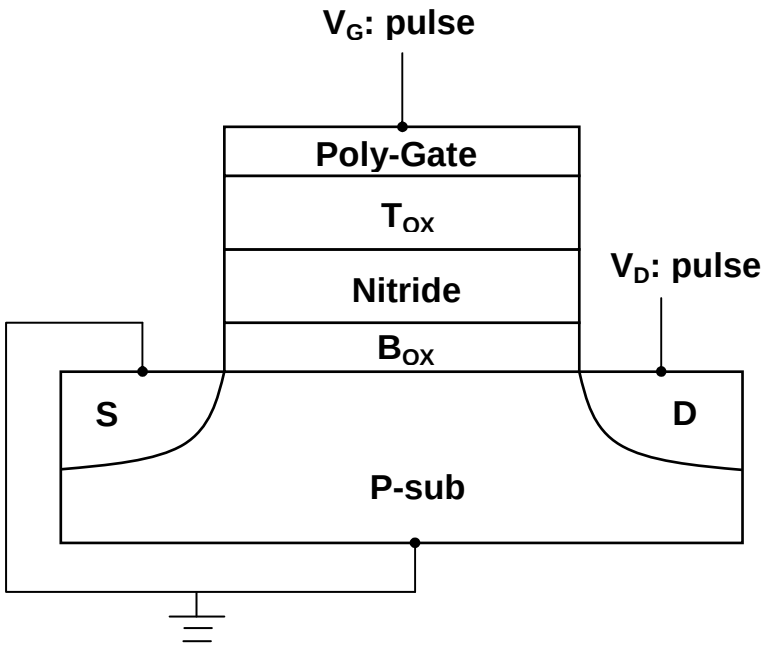
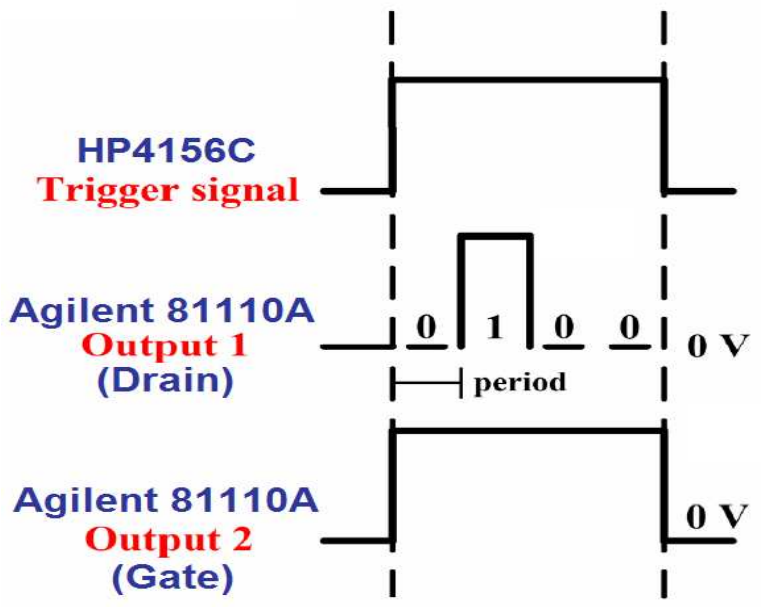


Fig. 2.3 The experimental setup of the current-voltage and the transient characteristics measurement. An automatic controlled characterization system is setup based on the PC controlled instrument environment.

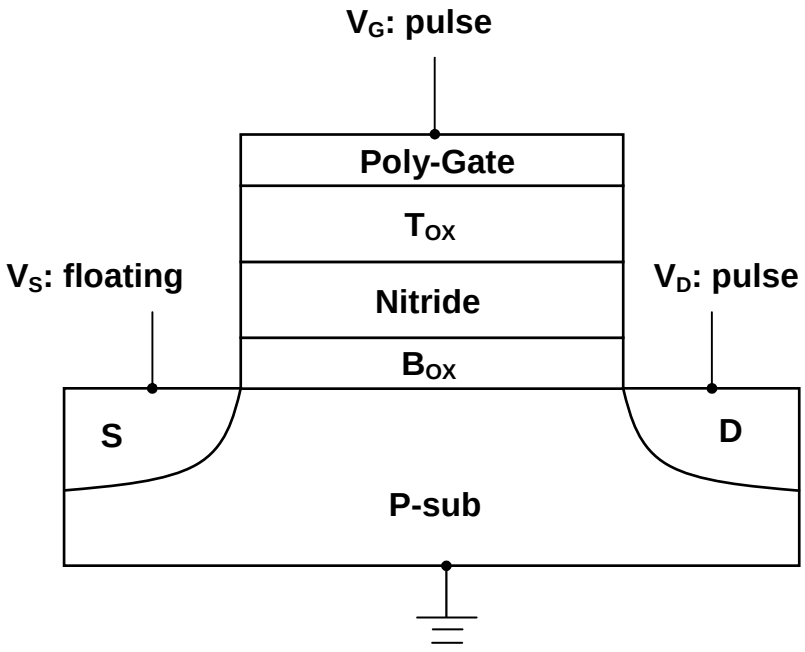


(a)

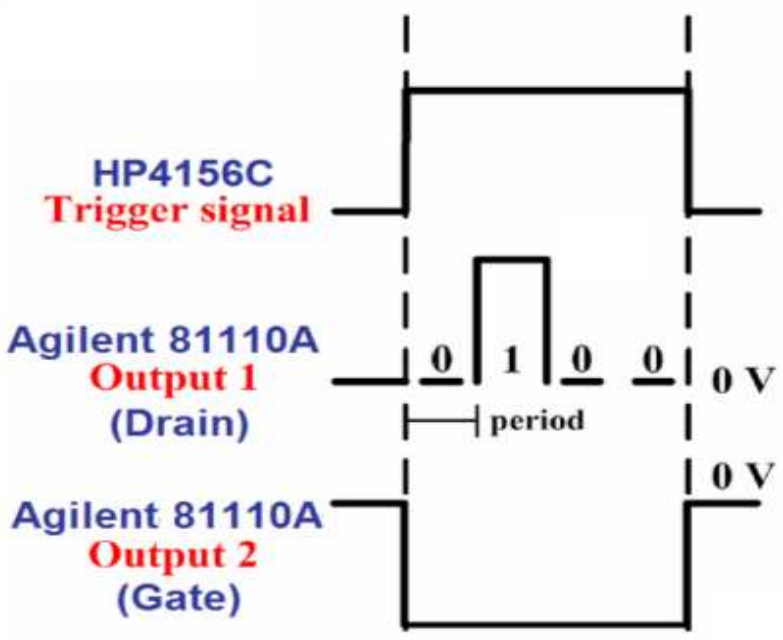


(b)

Fig. 2.4 (a) The operation scheme and (b) timing diagram for CHEI program.



(a)



(b)

Fig. 2.5 (a) The operation scheme and (b) timing diagram for BTBHHI erase.

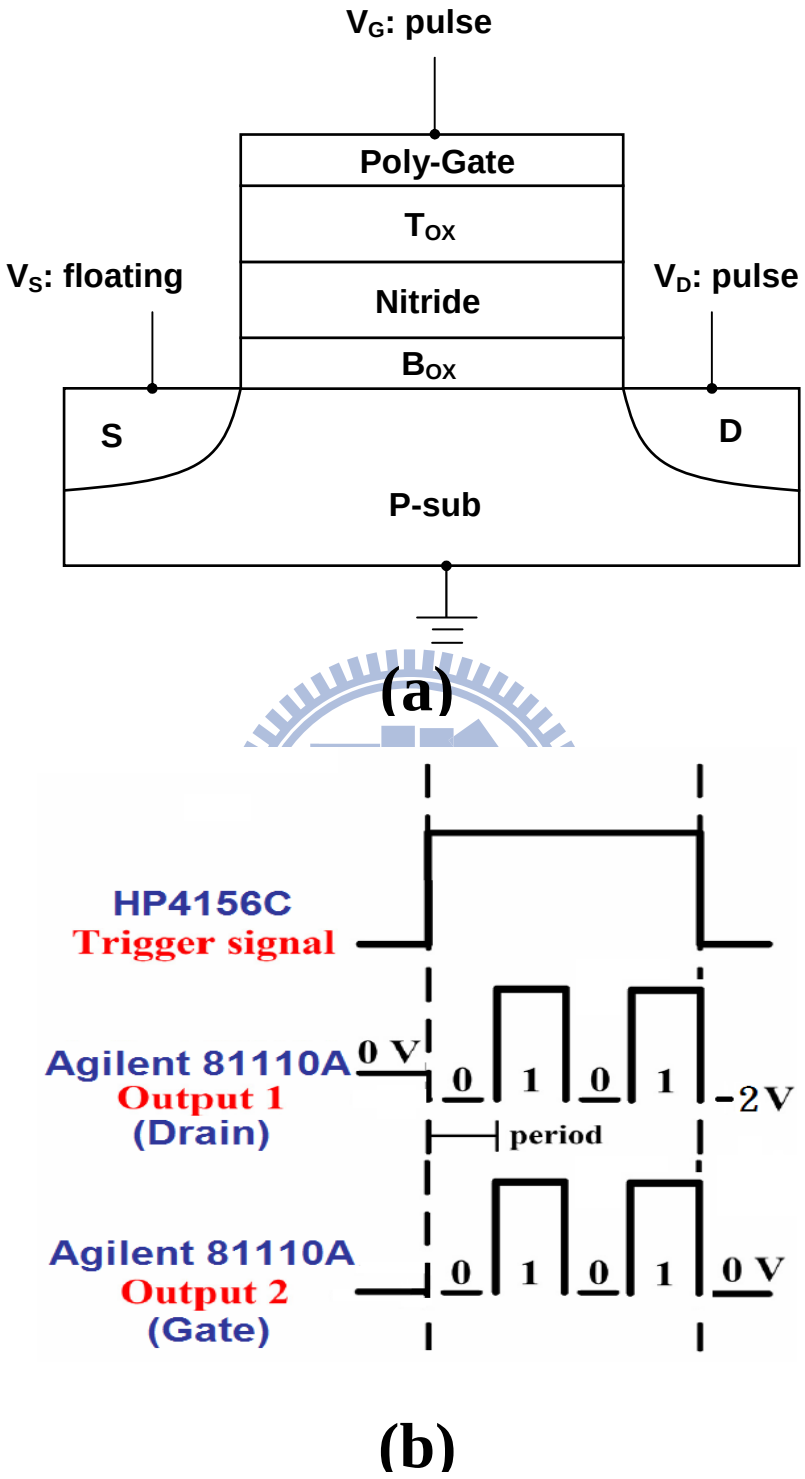


Fig. 2.6 (a) The operation scheme and (b) timing diagram for FBEI program.

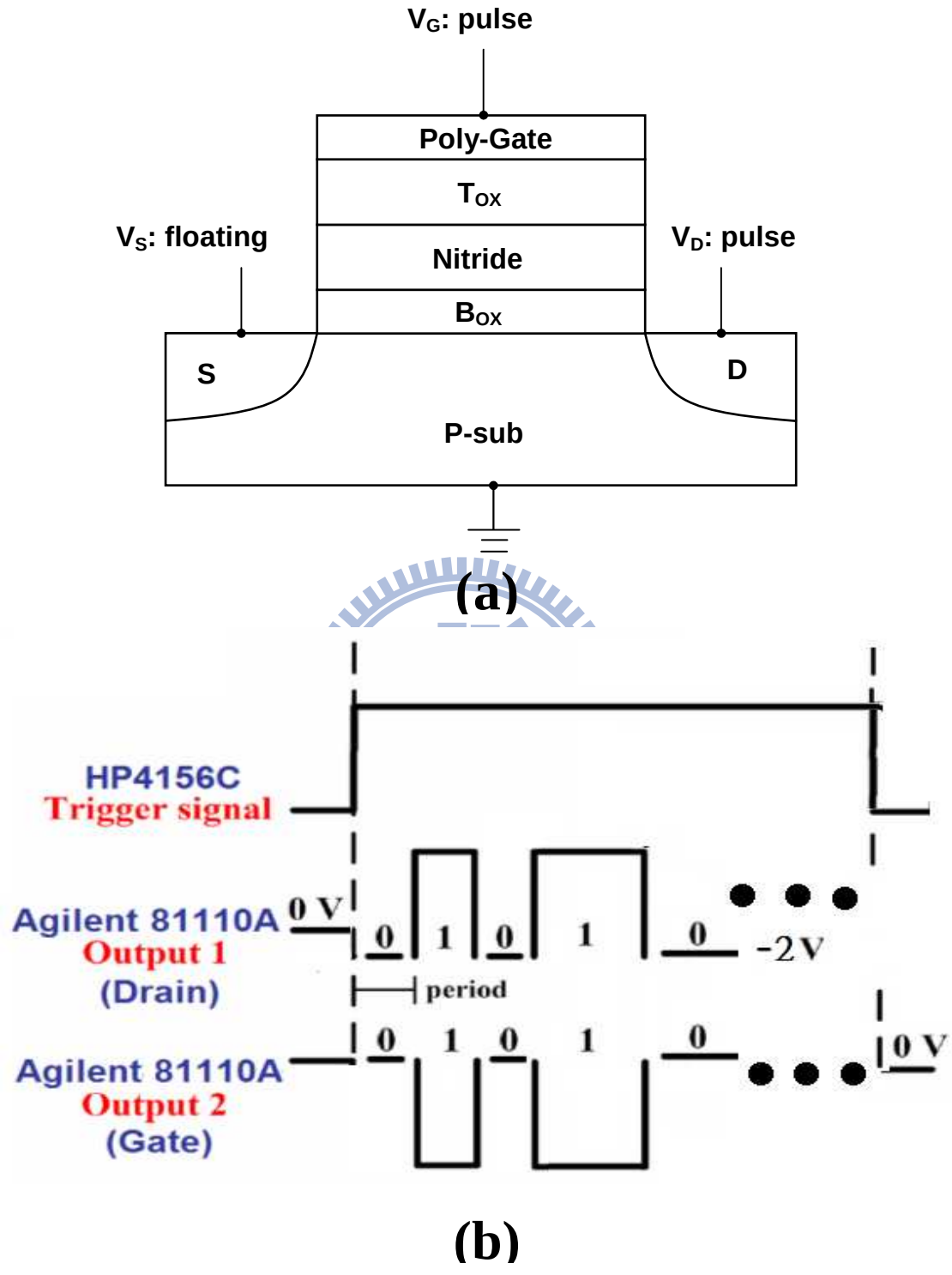


Fig. 2.7 (a) The operation scheme and (b) timing diagram for FBHHI erase.

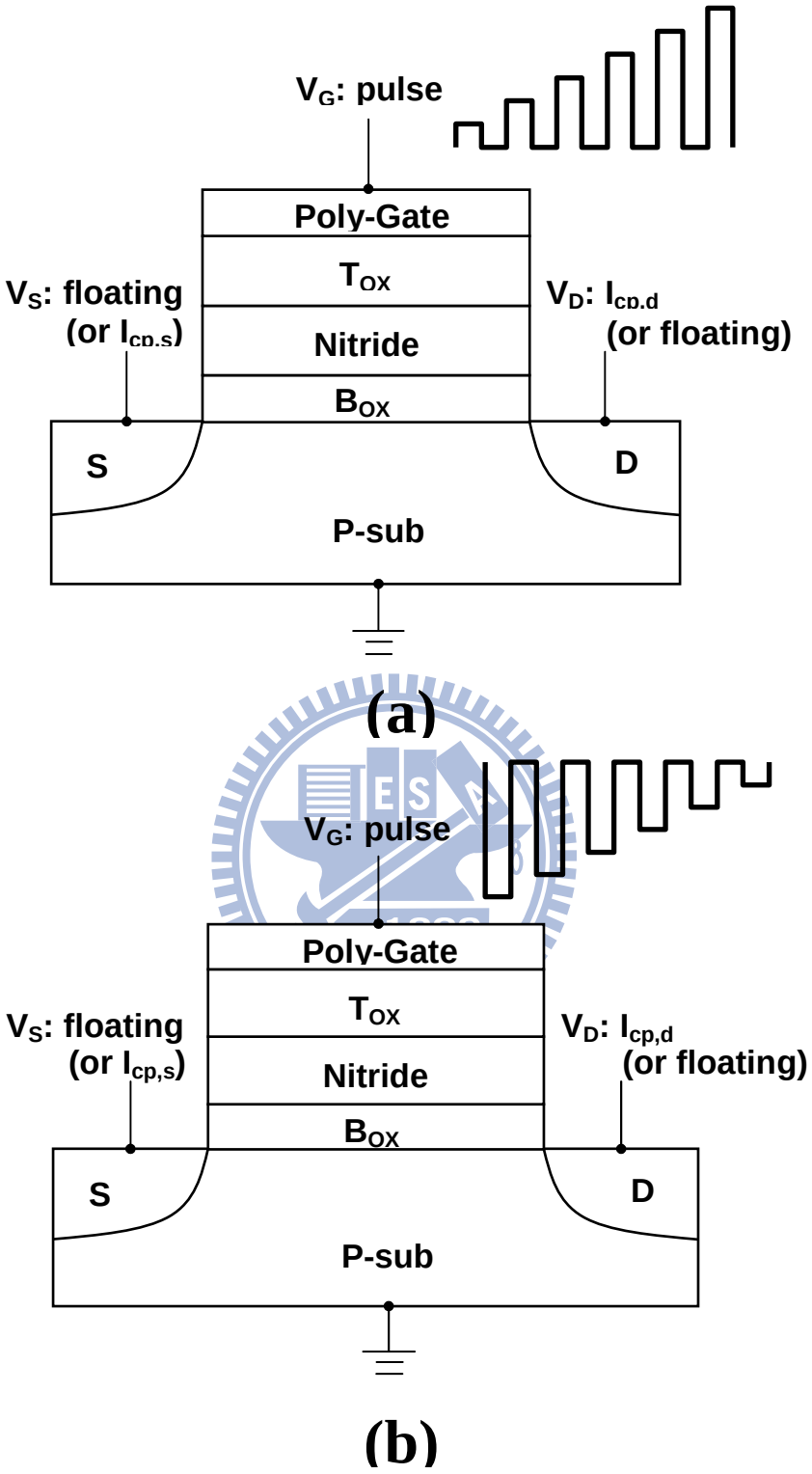


Fig. 2.8 The operation scheme for charge pumping with (a) fixed base pulse series measurement and (b) fixed top sketch.

Chapter 3

A Novel Operating Scheme and Properties of Split-Gate SONOS

3.1 Introduction

In chapter 3, we will propose a new mode of pulse operation to compete with the conventional operation scheme in split-gate SONOS. A novel operation concept used the multi-cycle pulse series and suitable forward-bias to enhance the efficiency of program/erase. Finally, several cell reliability issues by using the new operation scheme, such as forward-bias current disturbance, transient, endurance, and stress induced leakage current will be discuss in this chapter.

3.2 Basic Mechanism and Optimized Bias Condition of the Novel Operation Scheme

3.2.1 The Operating Mechanisms of FBEI and FBHHI

First, two modes of pulse operation are shown in Fig. 3.1, in which Fig. 3.1(a) shows the typical unit-pulse for conventional operation scheme, e.g., SSI or BTBHHI etc., and Fig. 3.1(b) shows a multi-cycle pulse series for new operation scheme, e.g., FBEI or FBHHI. In Fig. 3.1(b), the drain voltage was negative in 0 state, in which p-n+ diode was forward-biased to generate lots of carriers for increasing operating speed. Based on this idea, Fig. 3.2(a) is used for the FBEI program, source was

floating, during emitting phase T_1, the drain/bulk was forward biased and electrons were injected into the bulk. Subsequently, at T_2, the junction was reverse biased which will cause the previously injected electrons in the bulk to be accelerated across the depletion region and injected into the gate oxide.

FBHHI erase is shown in Fig. 3.2(b), substrate was grounded, while gate and drain bias used multi-cycle pulse series. Erase speed decays, for the pulse structure in Fig. 3.2(a), due to the trapping holes at the bottom oxide which leads to a decreasing FN field. The different emitting time T_2 can compensate the degradation of erase speed. During T_1, a large number of holes were injected into the drain side. Above all, we will get higher density of holes to enhance erase speed and keep the better quality of bottom oxide than that of BTBHHI erase (will be discussed in the next chapter).

3.2.2 Optimized V_{high} and V_{low} of FBEI Program

Figure 3.3 shows the characteristics of FBEI as a function of $V_{D,low}$ for a V_G=6.5V. We found that the ΔVth have a peak value at $V_{D,low}$= -2V and it will not be increased even if it is less than -2V. A suitable forward-bias is used to generate programming electron rather than to accelerate electron speed. Fig. 3.4(a) shows that a $V_{D,high}$ of over 5.5V is required for optimized injection voltage, due to the fact that hot electrons must surmount the ΔEc of the Si/SiO_2 interface (~3.1eV). The threshold voltage shift decreases when the voltage is over 5.5V, since the lateral electric field is larger than the vertical electric field. In Fig. 3.4(b), the ΔVth was increased with raising V_G. By using these optimized voltages, we can achieve an efficient operation condition. The other variables for FBEI program were reported in [5].

3.2.3 Optimized $V_{D,low}$ of FBHHI Erase

Figure 3.5 shows the characteristics of FBHHI as a function of $V_{D,low}$. The shift in the threshold voltage was saturated against increases in the forward-bias. Because the holes accumulated in the n+ drain will be recombined with electrons. Therefore, it is no useful by adding too large forward-bias at p-n+ diode and larger forward current will cause lots of reliability issues [12].

3.2.4 Program/Erase Transient for Different Modes of Operation

The programming speed of SSI and FBEI are compared in Fig. 3.6, which reveals that the new scheme, FBEI, achieving a faster programming speed and low voltage. In Fig. 3.7, it shows the most noticeable result in that the erase speed was greatly increased when V_{high} of drain voltage are 4V and 5V, respectively, and the low voltage of V_D was set at -2V. We understood that the larger V_{high} of drain voltage made more serious band bending to generate lots of band-to-band tunneling hot holes [4]. From the result of erase transient, we can estimate that the number of erasing hole by using forward-bias -2V at p-n+ diode is larger than that by using reverse-bias drain voltage 4V and 5V and are comparable when the drain diode is reverse-biased at 6V. Generally, it induces lots of hot holes by using a slight forward-bias, even if the V_{high} is too low. We know the large reverse-bias will stress the PN junction and a huge current also made the problem of circuit design and junction breakdown [13]. In the next section, we will discuss the reliability issue of FBHHI and BTBHHI erase.

3.3 Reliability for Non-Cycled Split-Gate SONOS

3.3.1 Operating Mode of P-N+ Diode

Figure 3.8 shows two different modes of measurement scale. On the left hand side of Fig. 3.8, the drain current as a function of the negative drain voltage for the V_G= 0V and V_D was varied from 0V to -3V. This bias condition was be used to realize the current of T_1 phase in FBHHI erase and we got I_D= 3.15 uA, while the forward-bias is -2V. In contrast, the right hand side of Fig. 3.8 shows the drain current of T_2 phase which is a function of the positive drain current and V_D was swept from 0V to 6V, the bias condition is equal to BTBHHI erase. The I_D is only near 10 nA even if V_D= 6V, so we can compare the currents from different operating modes to feel the benefits of FBHHI.

3.3.2 The Comparison with FBHHI and BTBHHI Erase

We have known that FBHHI has a better erase speed and enough erasing holes even if at low drain bias. By using multi-cycle pulse series, it only used a half of erase time (Fig. 3.9) to stress high voltage on the cell and remaining time is be used to generate the operating carriers. As a consequence, multi-cycle pulse series can enhance the operating speed and reduce the stress time because the mechanism of generated carriers in Fig. 3.10 are far away from the SiO_2/Si interface while we forward-bias the current at p-n+ diode. At T_2 phase of FBHHI, we set the drain and gate voltages equal to BTBHHI erase, then it is easy to compare the results with two kinds of pulse series. Above all, we have successfully achieved that hole stress time be decreased while keeping a better erase efficiency. Therefore, we will discuss the forward-bias condition correspond with some reliability issue.

3.3.3 Reliability for FBHHI

A large drain current will induce some problems about junction leakage or breakdown, but Fig. 3.11 will solve the concern about forward-bias current. We attempted to stress device under a long-term forward mode on the p-n+ diode. The result in Fig. 3.11 exhibits the stable value of leakage current and threshold voltage at V_D= -2V, even if it is until a thousand seconds. Generally, a suitable diode current will not destroy the implant p-n+ junction and will not cause an increase of the leakage current through the diode. In other words, threshold voltage was not disturbed while the drain voltage is negative and the storage node was not be erased at T_1 phase.

In chapter 4, we will discuss the oxide degradation and interface traps under different erase conditions. It shows that FBHHHI erase can reduce the oxide decay. In [14], the positive oxide charge assisted tunneling was dominated to be a serious SILC in a hot hole stressed cell. We estimated the negative bias at T_2 phase can annihilate the positive oxide charge at the bottom oxide and reduce the SILC.[15]

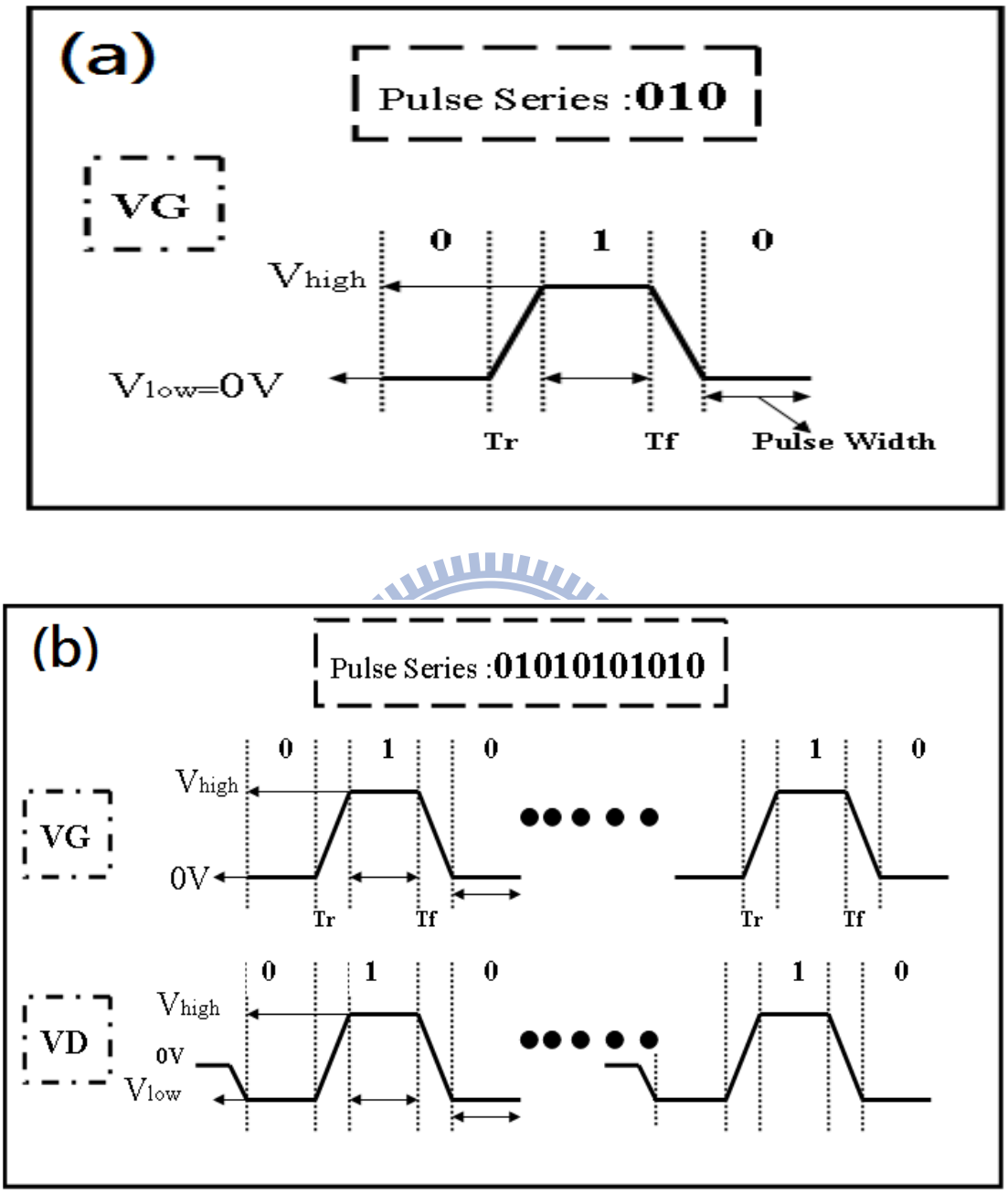


Fig. 3.1 (a) The conventional unit-cycle pulse series for CHEI or BTBHHI.

(b) The multi-cycle pulse series for FBEI or FBHHI.

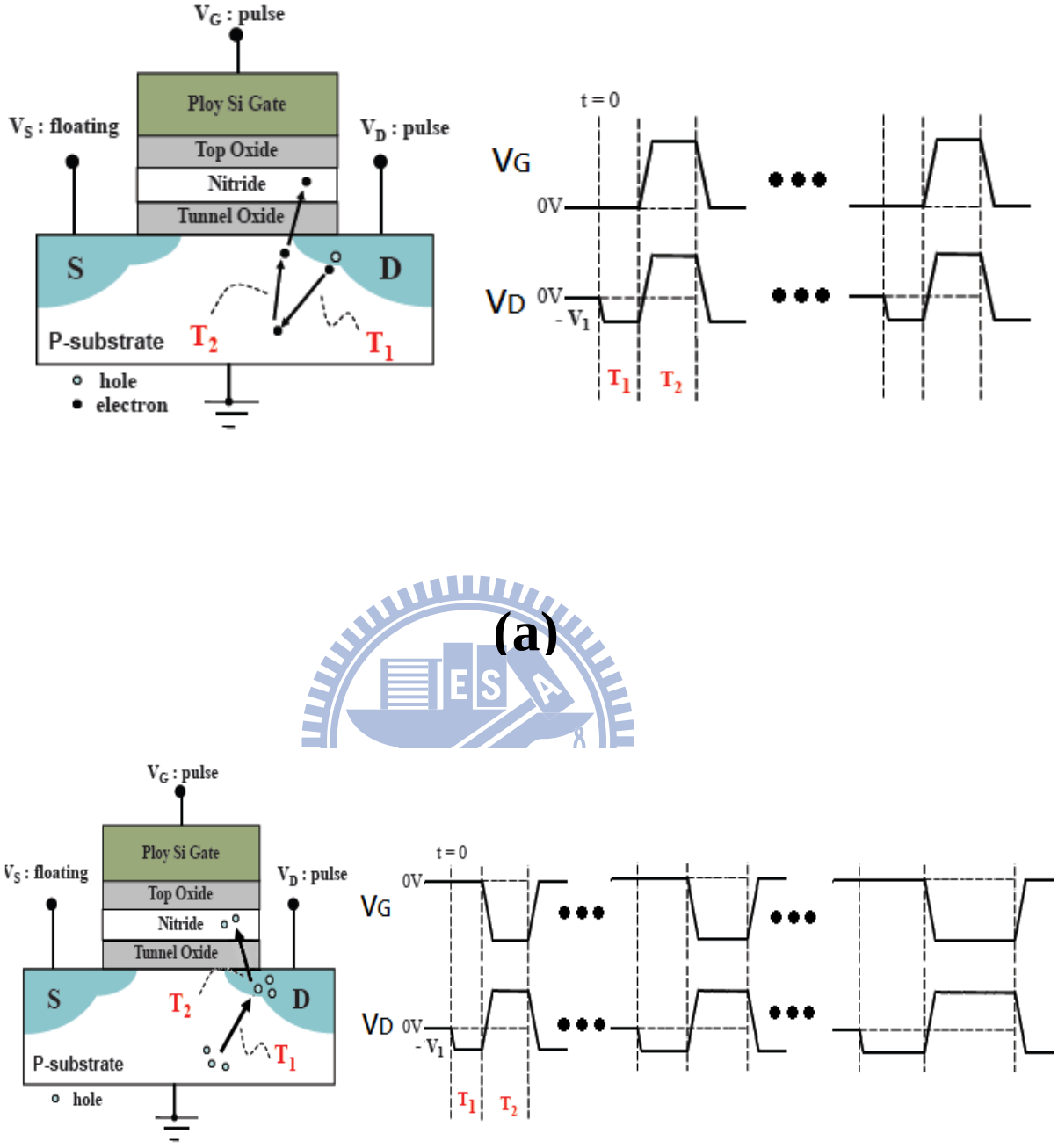


Fig. 3.2 The operation scheme and timing diagram for (a) FBEI program and (b) FBHHI erase. The FBEI pulse series were combined with the same pulse width, but the FBHHI series used a varying pulse width.

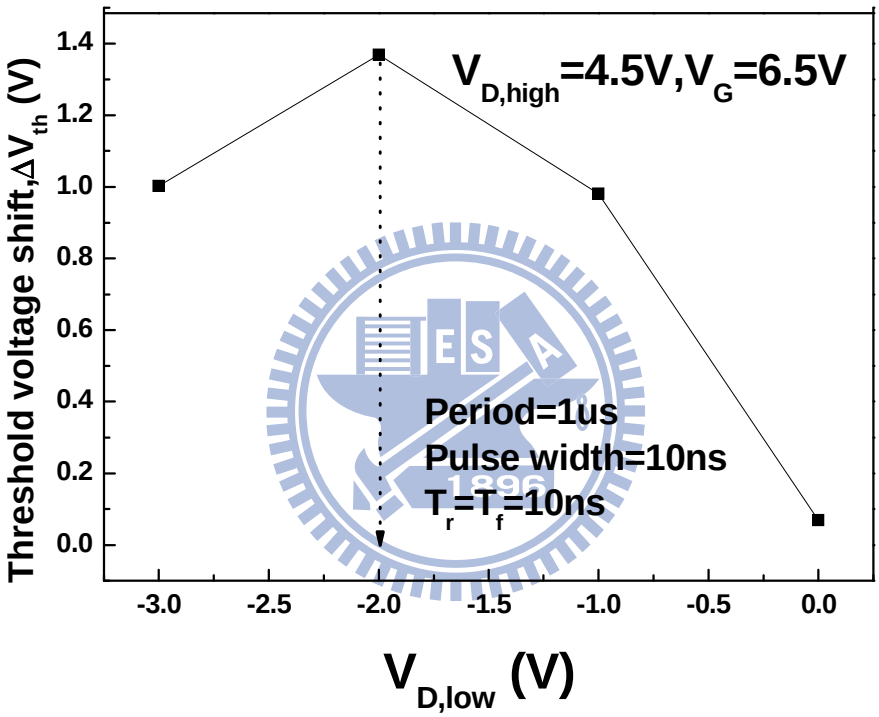
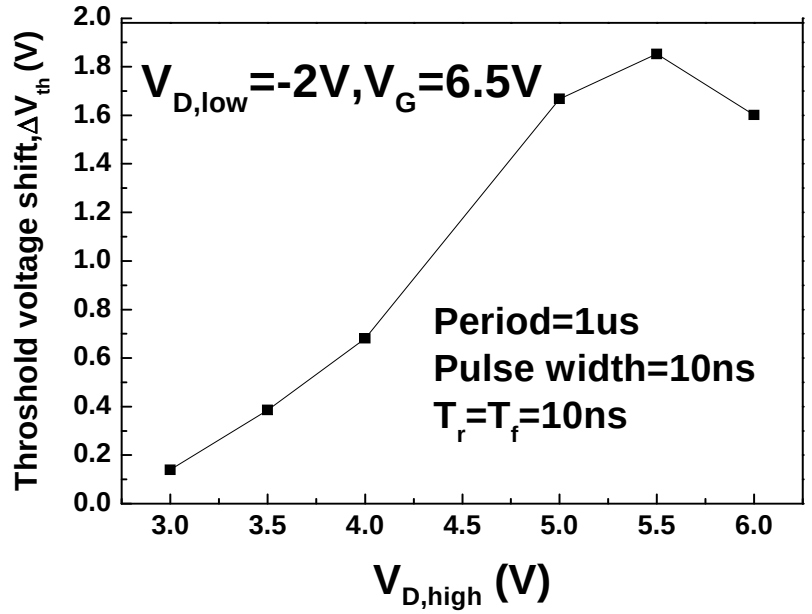
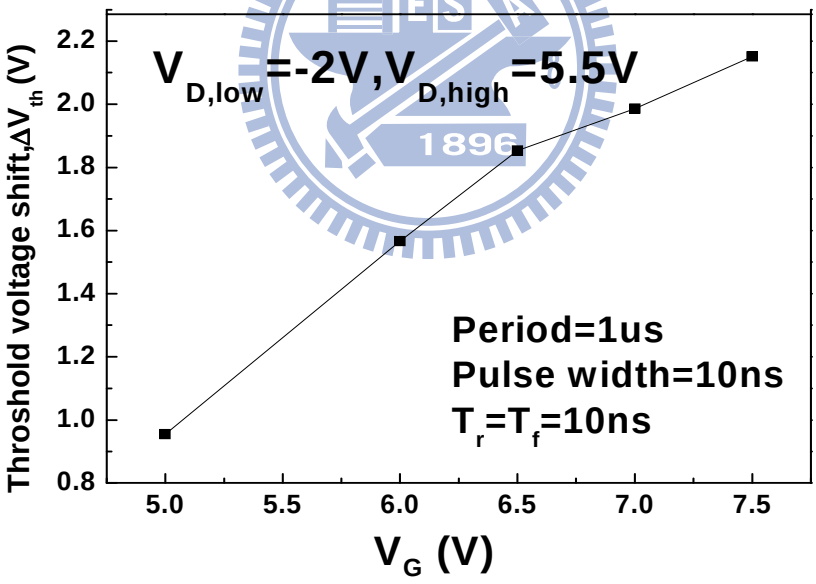


Fig. 3.3 The characteristics of FBEI as a function of $V_{D,low}$



(a)



(b)

Fig. 3.4 (a) The characteristics of FBEI as a function of $V_{D,high}$

(b) The characteristics of FBEI as a function of V_G

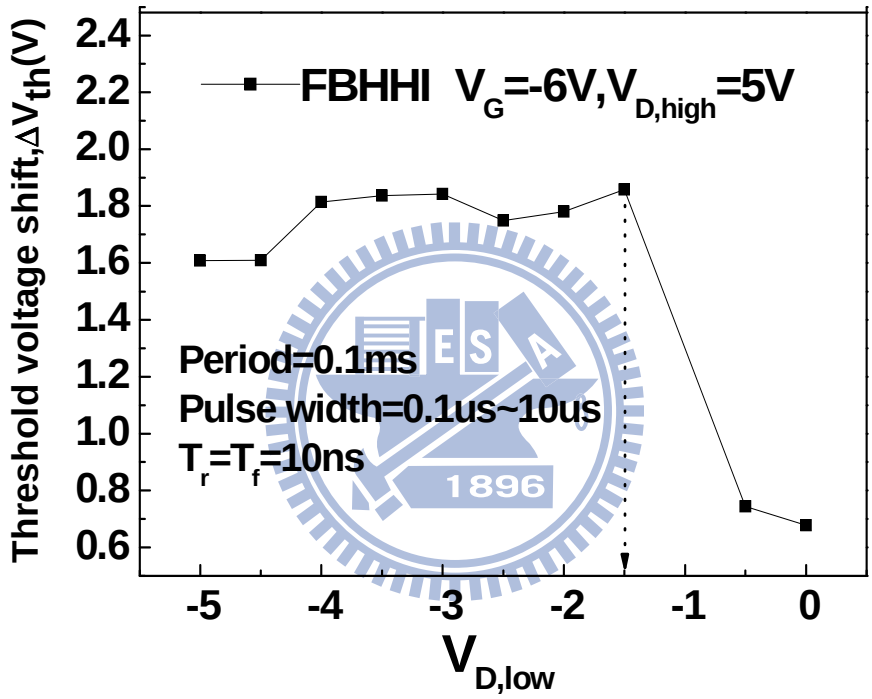


Fig. 3.5 The characteristics of FBHHI as a function of $V_{D,low}$

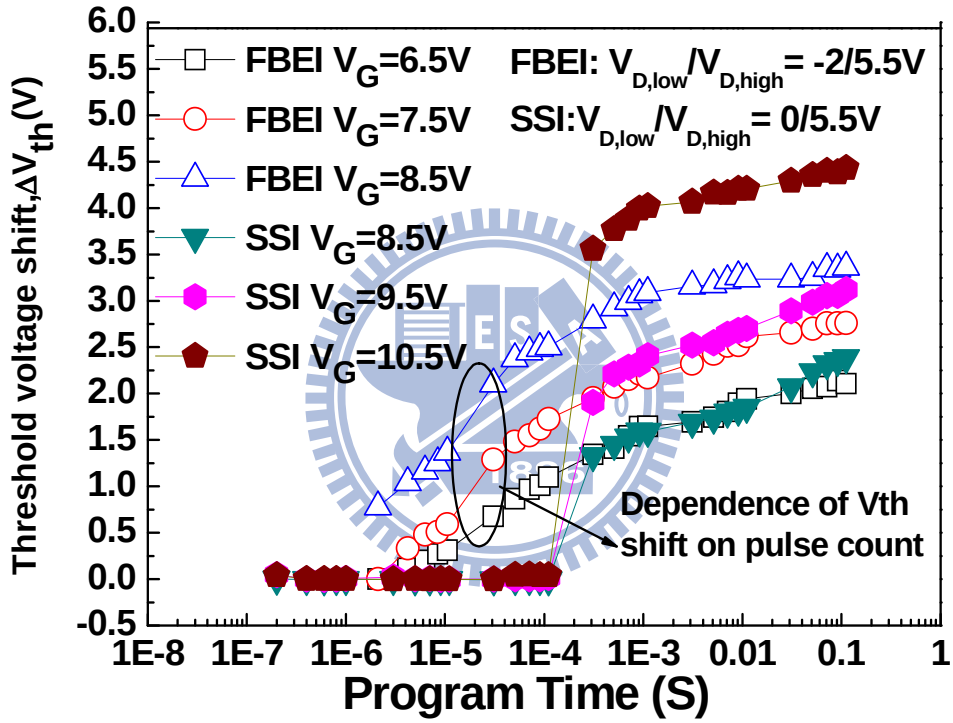


Fig. 3.6 The programming transient of SSI and FBEI programs for split-gate SONOS with multi-level cell application.

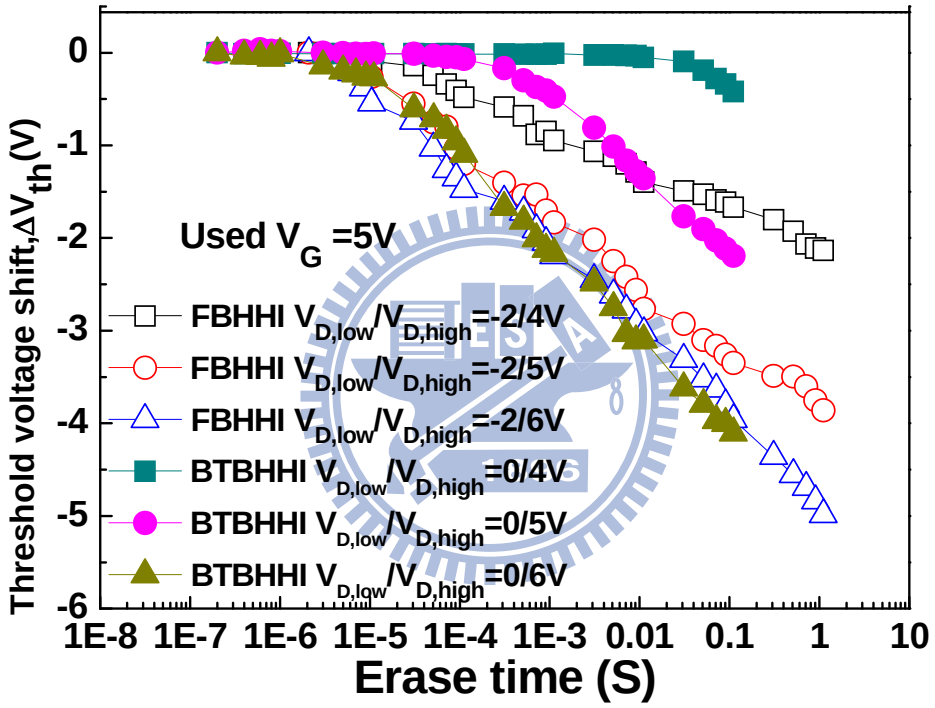


Fig. 3.7 The erasing transient of BTBHHI and FBHHI erases for split-gate SONOS with multi-level application.

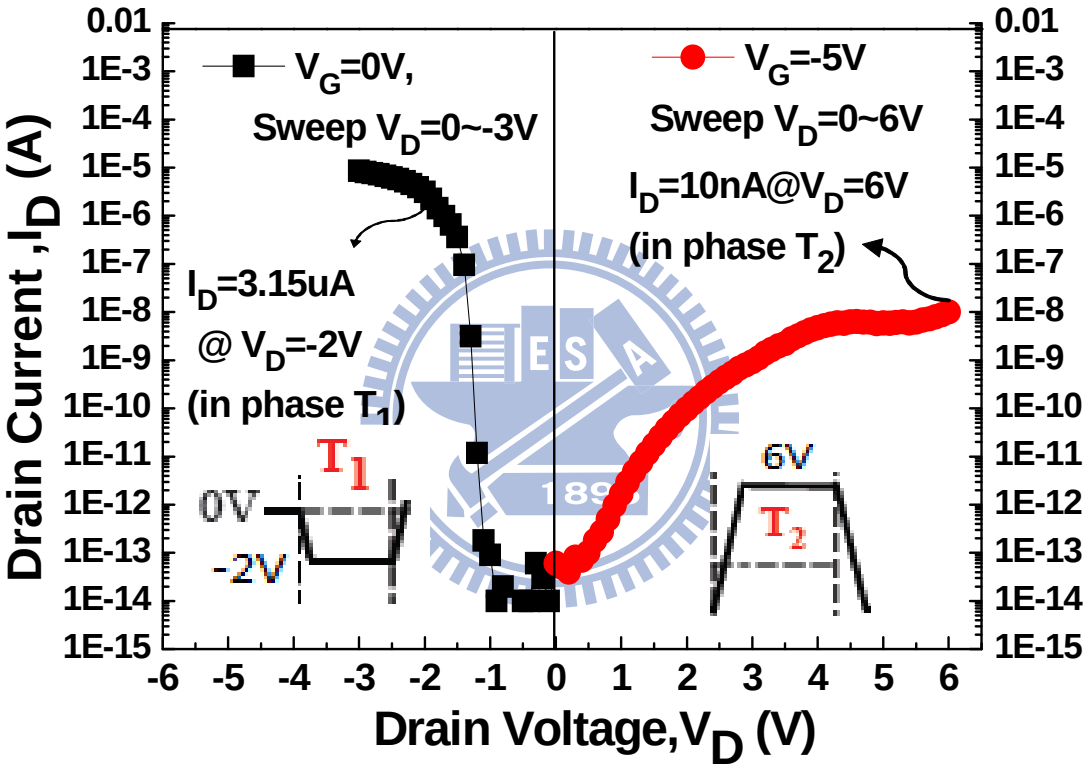


Fig. 3.8 Two different modes of measurement for split-gate SONOS.

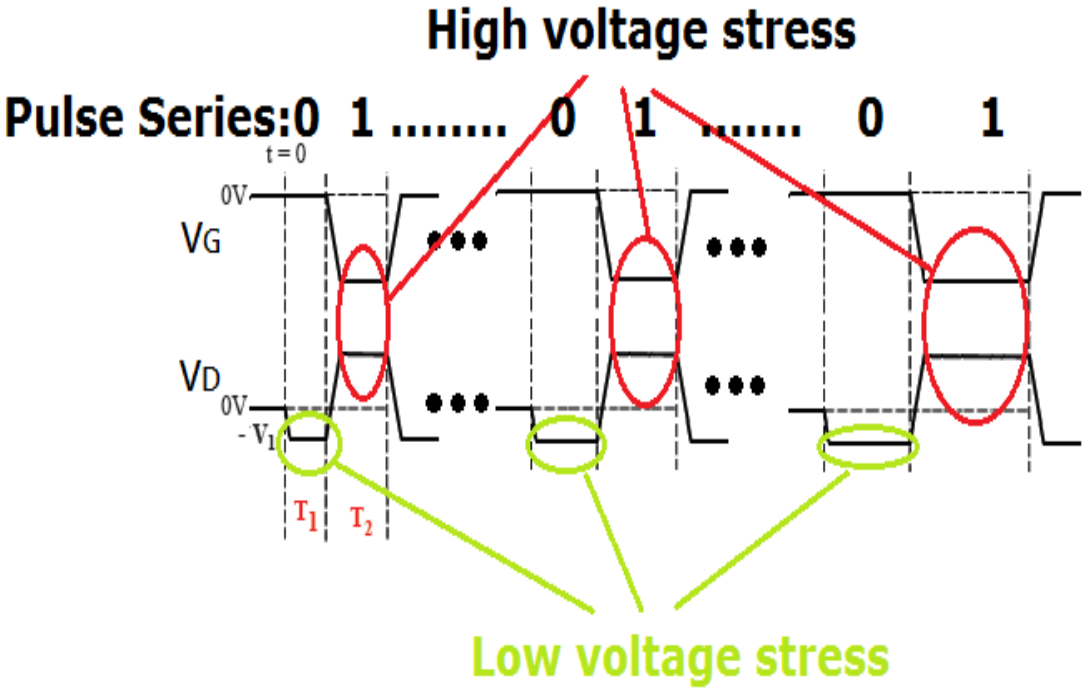


Fig. 3.9 By using multi-cycle pulse series, it only used a half of operating time to be stressed at high voltage and remaining time be stressed at low voltage.

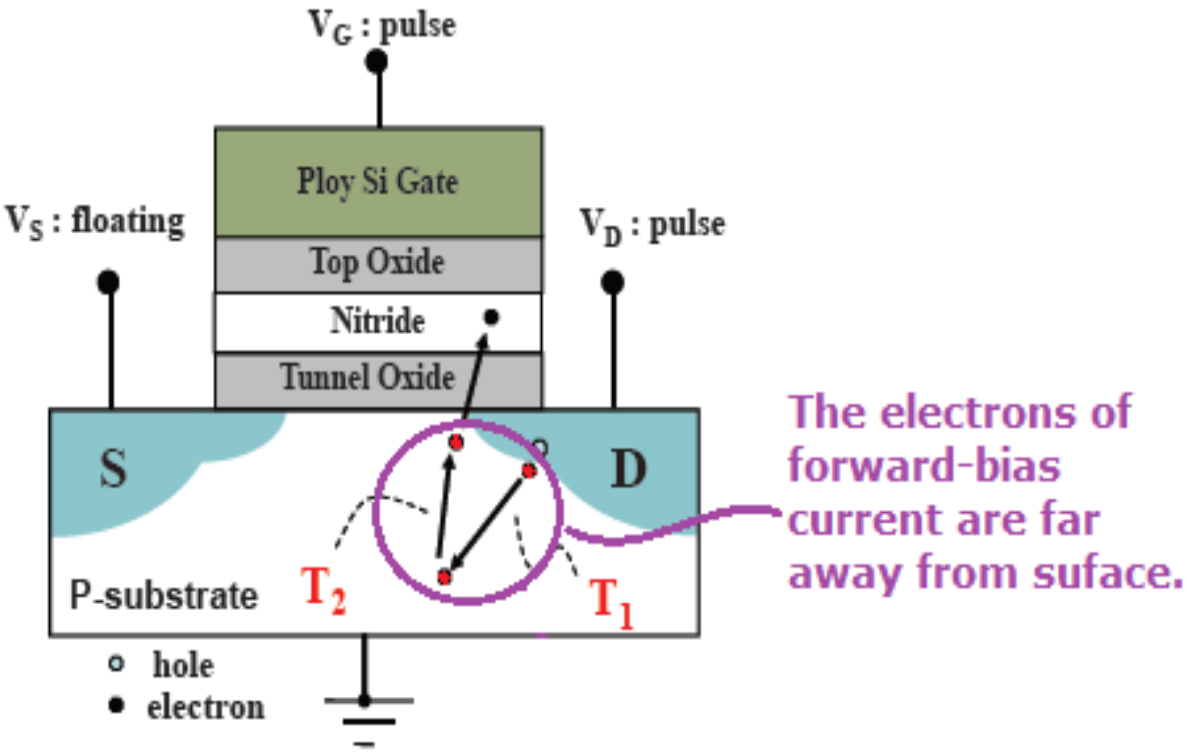


Fig. 3.10 The mechanism of multi-cycle pulse series operation. The generation of carrier is far away from the channel and reduces the oxide degradation.

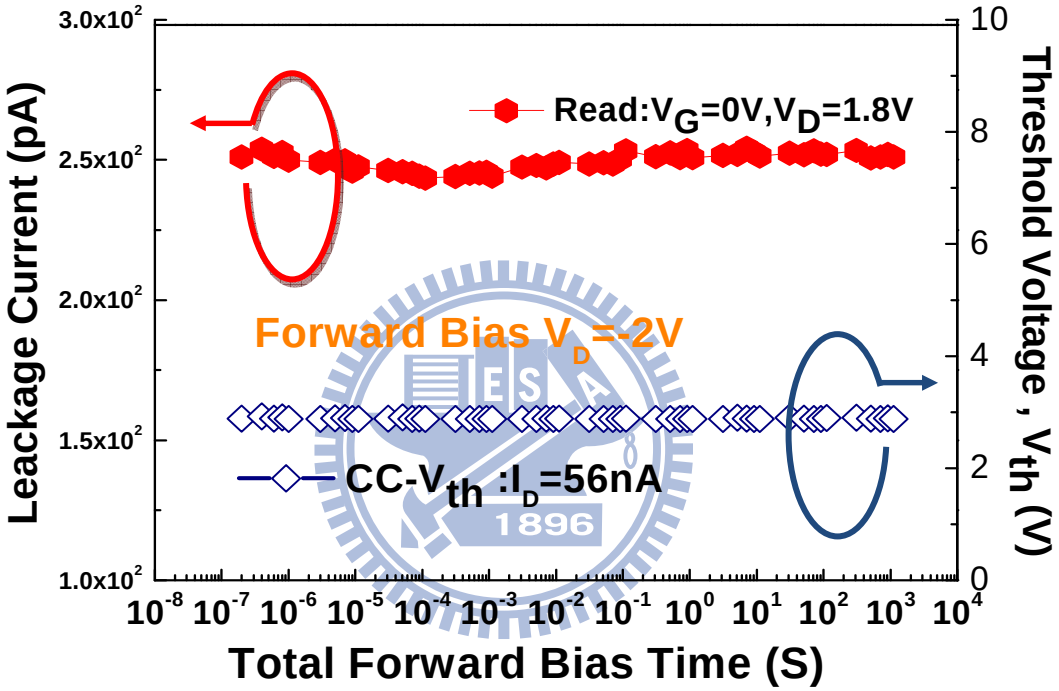


Fig. 3.11 The value of leakage current and threshold voltage at V_D=-2V, even if it is until a thousand seconds.

Chapter 4
The Monitoring of Stored Charges and Oxide Traps in a Planar SONOS

4.1 Introduction

In this chapter, we will discuss the different operation combinations in a planar SONOS and analyze the reliability issue for a P/E cycling device using different operating schemes. We will use the charge-pumping techniques to detect the misalignment between the distribution of electrons and holes. The charge distribution profiling in charge-trapping memory have been studied by various methods of charge-pumping [8][9], but it became more inaccurate after P/E cycles. We will propose a monitor to understand the hole-electron misalignment and degradation of operation. [10]

4.2 Principle of Charge Profile by Charge Pumping Method

4.2.1 Principle of Charge Pumping Method

The charge pumping method has been widely used for hot-carrier-related reliability characterization in MOSFETs. During a typical charge pumping measurement, a pulse string is applied to the gate terminal of a MOSFET while the substrate current (commonly called the “charge pumping current”) is monitored. Since this current is a result of the recombination of majority carriers (coming from

the substrate when the gate is biased between flat-band and accumulation) with the trapped minority carriers at the interface (coming from the source/drain when the gate is biased to inversion), to first order the charge pumping current (I_{cp}) is nonzero only if the high level (V_h) and the base level (V_b) of the gate pulses cover both the threshold voltage (V_t) and the flat-band voltage (V_{fb}) [8][16].

Unlike the conventional charge pumping (CP) method, the other two basic ways of charge pumping test to obtain the profile are demonstrated. First one is the fixed base CP (fixed base level and varying the top level) method with one side of drain (or source) floating and the other one is the fixed top CP (fixed top level and varying the base level) method with also one side of drain (or source) floating, which are defined as FV_b and FV_t, respectively.

In FV_b CP method, the setup is shown in Fig. 2.8 (a) in chapter 2, the gate is applied with a pulse string, as shown in Fig. 2.8 (a), and the I_{cp} can be measured from drain or source side with source or drain floating respectively. When measuring the charge pumping current $I_{cp,d}$ from the drain side, the minority carrier only contributed from the drain side and vice versa with $I_{cp,s}$. Therefore, we can obtain more precise information about the drain and source side from $I_{cp,d}$ and $I_{cp,s}$. By combining these two currents, we can profile the asymmetrical V_t along the channel for both virgin and programmed cells [9][18]. In FV_t CP method, the setup and gate pulse are shown in Fig. 2.8(b). The equipment setup is similar to FV_b CP method instead of the gate pulse string which is fixed on a constant level upon the threshold voltage.

4.2.2 Fixed Base Charge Pumping Method

Figure 4.1 (a) illustrates the V_t profile of a programmed nitride storage memory cell, which contains a narrow V_t peak near the drain side. Four regions are marked in this figure, and they are consistent with the I_{cp} curve tested from FV_b CP method in Fig. 4.1 (b). Fig. 4.1 (b) corresponds to the drain or source junction area in Fig. 4.1 (a). After the programming, localized trapped charges enhance the threshold voltage near drain side, which forms the asymmetrical V_t profile in Fig. 4.1 (a). Therefore, the $I_{cp,d}$ and $I_{cp,s}$ curves can be shifted toward the right, which corresponds to the regions B and C in Fig. 4.1 (b). The difference between curves B and C indicates the location and profile of the injected charges. As Fig. 4.1 (b) shows, the injection is closer to the drain side. It needs to be pointed out that I_{cp} keeps shifting rightward in region D, indicating a V_t peak here. Moreover, $I_{cp,d}$ and $I_{cp,s}$ overlap in this region, which means the minority carrier coming from drain or source is passing through the peak region under the channel. For this reason, the equivalent interface traps are sensed and contribute the same $I_{cp,d}$ and $I_{cp,s}$. Thus, in FV_b CP method, data obtained in region D cannot be used to extract the exact profile of V_t in large current region. We can, however, extract the accurate location using this method.

4.2.3 Fixed Top Charge Pumping Method

On the other hand, the equipment setup is similar to FV_b CP method instead of the gate pulse string which is fixed on a constant level upon the threshold voltage. In contrast, the I_{cp} curve shift caused by the V_t peak, takes place in the low current region and has higher precision in FV_t CP method. Fig. 4.2 (a) illustrates I_{cp} test with FV_t CP method in logarithmic scale. Correspondently, region B, C and D in Fig. 4.2 (a)

and Fig. 4.1 (b) also can be seen herein. I_{cp} in region D can be used to extract the accurate profile of narrow V_t peak due to its low testing current. However, V_h is set larger than the highest V_t along the whole channel, and I_{cp} current tested from drain and source are identical. FV_t CP method can only extract the width and value of narrow V_t peak but cannot be used to identify the location.

4.3 The Monitoring of Stored Charges for a Cycled Cell

4.3.1 The Correlation Between Stored Charges and I_{CP} in FV_b CP Method

Figure 4.3 shows the charge-pumping current measurement to identify the trapping charges and oxide traps with the source side floating in a planar SONOS. The curve in I_{CP} plot (Fig. 4.3) shows the existence of injected holes ($\Delta I_{CP,h}$), injected electrons($\Delta I_{CP,e}$), and oxide traps ($\Delta I_{CP,Nit}$) in dielectric layer after P/E cycles. The charge distribution profiling can be found by calculating the correlation between the injected charges and I_{CP} curve deviation [19][20]. These profiling methods can not be used to investigate the residue charges in P/E cycling device while they used the other measurement methods, e.g. GIDL, I_D-V_G etc., in [21][22].

We will propose a new concept to investigate the complex stored charges condition. In FV_b CP method, the cycling I_{CP} curve apparently deviates from fresh I_{CP} curve as a result of the injected charges. The curve shift presented the amount of the charge in the nitride or oxide. Finally, we used a new area parameter A to discuss the total charges of dielectric layer and compared the different operation combinations.

4.3.2 Derivation of the Area Parameter

Figure 4.4 shows the difference of $I_{CP,d}$ curve at fresh state and one time program state in a planar SONOS. The area A_o in the shaded region represents the total stored electrons in the nitride while the device was only programmed once. The area Ao was compared with the fresh state I_{CP}(fresh) and one time program state I_{CP}(1@pro).

$$A_o = \int_0^{V_h(I_{CP,MAX})} [I_{CP}(fresh) - I_{CP}(1@pro)]dV_h \quad (1)$$

In [10], equations used in FV_b to calculate the $N_{N,e}(x)$ versus x curve are as follows:

$$x = LI_{CP}(V_h)/I_{CPo,MAX} \quad (2)$$

$$N_{N,e} = \frac{1}{qfW}\frac{d\Delta I_{CP}}{dV_h}\frac{dV_h}{dx} \quad (3)$$

where q is electron charge, f is the frequency of the pulse, W is the effective channel width, L is channel length, and $N_{N,e}(x)$ is the trapping electrons density in the nitride. From these equations, we can derive the total charges Q_{total} in nitride by integrating the $N_{N,e}(x)$ from 0 to L. Comparing (2) and (3), we can derive

$$Q_{total} = \int_0^L N_{N,e}(x)dx = \frac{L}{I_{CPo,MAX}}\int_0^{I_{CP,MAX}} N_{N,e}(I_{CP})dI_{CP} \quad (4)$$

The trapped electron density $N_{N,e}(x)$ is then calculated using the V_h shift $\Delta V_h(I_{CP})$ [10] ; that is

$$N_{N,e} = \frac{C_{OX} C_N \Delta V_h(I_{CP})}{(C_{OX} + C_N) q} \tag{5}$$

This means that the trapping charges were stored near the SiO_2/Si_3N_4 interface. Then, the total charge can be given by:

$$Q_{\text{Pro},total} = \frac{L}{I_{CPo,MAX}} \int_0^{I_{CP,MAX}} \frac{C_{OX} C_N \Delta V_h(I_{CP})}{(C_{OX} + C_N) q} dI_{CP}$$

$$= \frac{L}{I_{CPo,MAX}} \int_0^{Vh(I_{CP,MAX})} \frac{C_{OX} C_N}{(C_{OX} + C_N) q} \bullet \Delta I_{CP}(V_h) dV_h \tag{6}$$

Then, we have the total charges in the nitride:

$$Q_{total} \approx \int_0^{Vh(I_{CP,MAX})} \Delta I_{CP}(V_h) dV_h \tag{7}$$

Finally, we can use the equation (7) to estimate the number of stored charges in the nitride with an area parameter A while the cell is at the one time programming state or any P/E cycled state.

$$Q_{\text{Pro@1}time} \approx A_o = \int_0^{V_h(I_{CP,MAX})} [I_{CP}(fresh) - I_{CP}(1@pro)] dV_h \tag{8}$$

$$Q_{N,e^- + h^+} \approx A(cycles) = \int_0^{V_h(I_{CP,MAX})} [I_{CP}(fresh) - I_{CP}(cycles)] dV_h \tag{9}$$

4.3.3 The Correlation Between Stored Charges and Area Parameter

First, it was known that the area parameter is related to the stored charges during any cycled state. The A_o was a basic parameter to compare the A(cycles) at any P/E cycled state. Fig. 4.3 shows that the injected holes ($N_{N,h}$) raise up the I_{CP} curve and decrease the value of A(cycles) in equation (9) while the I_{CP}(cycle) increased. On the other hand, the injected electrons will suppress the I_{CP} curve and increase the value of A(cycles). In Fig. 4.3, $\Delta N_{OX,it}$ presents the increase of the oxide traps in term of P/E cycles and it will increase the value of $I_{CP,MAX}$ when the oxide was degraded. Generally, we may draw a relationship. i.e.,

$$\frac{\Delta A = A(cycles) - A_O}{A_O} \propto N_{N,e} \propto 1/N_{N,h} \propto 1/\Delta N_{OX,it} \qquad (10)$$

From which we can utilize the $\Delta A/A_o$ to analyze the condition of hole-electron misalignment under different operating schemes and the erasing efficiency of BTBHHI and FBHHI schemes.

4.4 Experimental Results and Discussion

4.4.1 The Basic Operation Conditions of Different Operating Schemes

Table 4.1 is a combination of different program/erase schemes and the applied biases in a planar SONOS. For program, we used the same V_G and $V_{D,high}$ and programming time to emphasize the different pulse series mode in operating scheme.

For erase, we keep the same window margin of 2V while BTBHHI or FBHHI are used. The endurance of various operation combinations is shown in Fig. 4.5 and we found the window margin was closed and $V_{th,low}$ was raised by accumulated electrons while using the BTBHHI erase in Fig. 4.5 (a). Nevertheless, FBHHI can keep the stable window margin, even if it is until one thousand cycle times in Fig. 4.5 (b).

4.4.2 The Experiment Results of FV_b CP Method

Figures 4.6 (a) and (b) show the fix base charge-pumping method for CHEI/BTBHHI cycle and FBEI/BTBHHI cycle, with different cycling time on programming state to do the test. We can get the A_o from fresh $I_{CP,d}$ and 1@Pro $I_{CP,d}$ to know the total injected electrons after first program. The stored charges in the nitride with P/E cycling were complicated, and we estimated that the non-recombined electrons at erase state were accumulated, and the holes accumulated above the overlapping region between the gate and drain. The A(cycles) was reduced while more holes accumulated at the programmed state.

Generally, we already know the number of total injected electrons by A_o parameter and then we calculated the $\Delta A/A_o$ in different cycling times to investigate the hole-electron misalignment and operating scheme. In Fig. 4.6, at first, we found the $I_{CP,MAX}$ increased rapidly by using CHEI program, it means that CHEI program made more interface traps in bottom oxide than FBEI program. For FBHHI erase in Fig. 4.7, we detected that the value of $\Delta I_{CP,MAX}$ was suppressed, in comparison with the BTBHHI erase. Besides, we found the raising current at low current state as a result of the accumulation of holes at the drain side.

Next, we show the variation of $\Delta A/A_o$ with increasing P/E cycles in four operating conditions, as show in Fig. 4.8. Mainly, FBHHI can inject more holes to the nitride, leading to the excess holes accumulated even at the programed state. Comparing the electron-hole misalignment in Fig. 4.8, FBEI can reduce more accumulated holes than CHEI because its injected electrons are near the drain side by using FBEI program [5]. Fig. 4.9 was used to know which operating scheme will make even more oxide degradation, and it shows that FBEI/FBHHI be the best P/E operation as a result of a slope of the increasing $\Delta I_{CP,MAX}/I_{CPo,MAX}$ was suppressed.

Basically, the misalignment makes the electrons accumulation in the channel, which can not be recombined by the injected holes. Both electrons and holes accumulated in the channel will change the drain current flowing path and the electric field in the channel, resulting in the impact ionization position move toward into the channel, making the mismatch more serious[23][24][25][26]. From the experimental results, FBEI and FBHHI can suppress the oxide degradation in comparison to conventional operating scheme and FBEI/FBHHI also reduced the misalignment in the trapping memory.

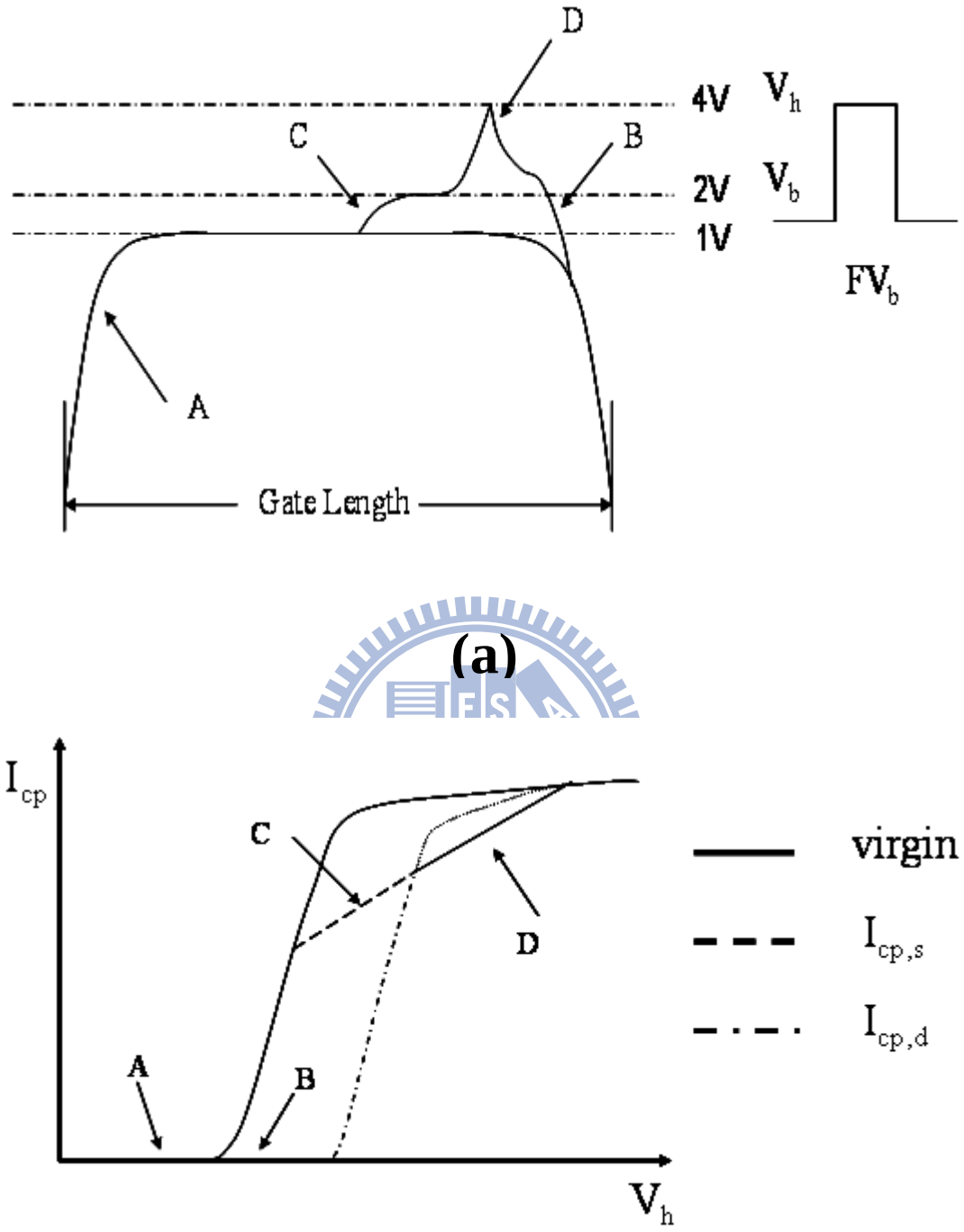


Fig. 4.1 (a) The V_T profile in a programmed nitride storage memory cell.

(b) Illustration of I_{cp} curves versus V_h before and after programming.

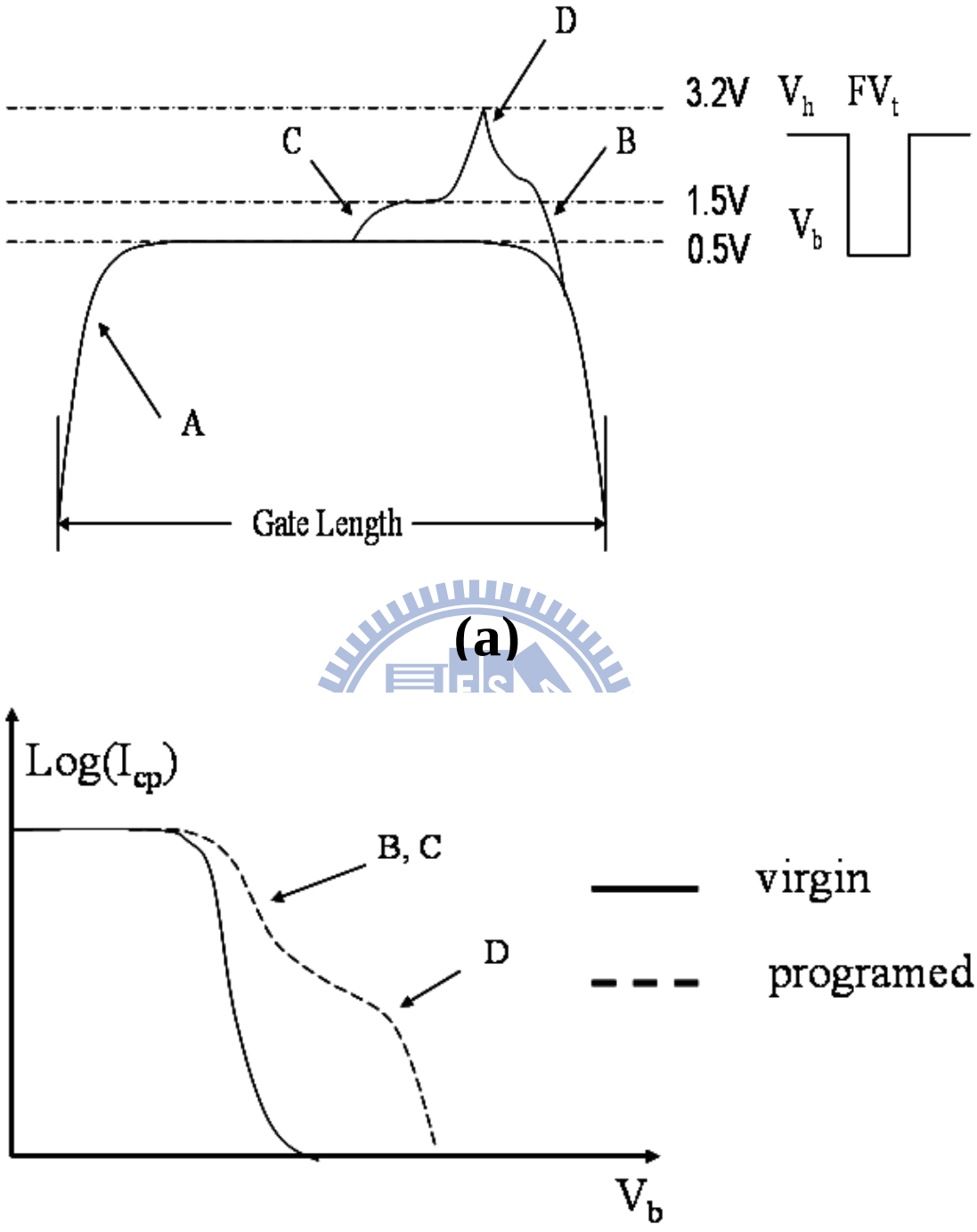


Fig. 4.2 (a) The V_T profile in a programmed nitride storage memory cell.

(b) Illustration of I_{cp} curves versus V_b before and after programming.

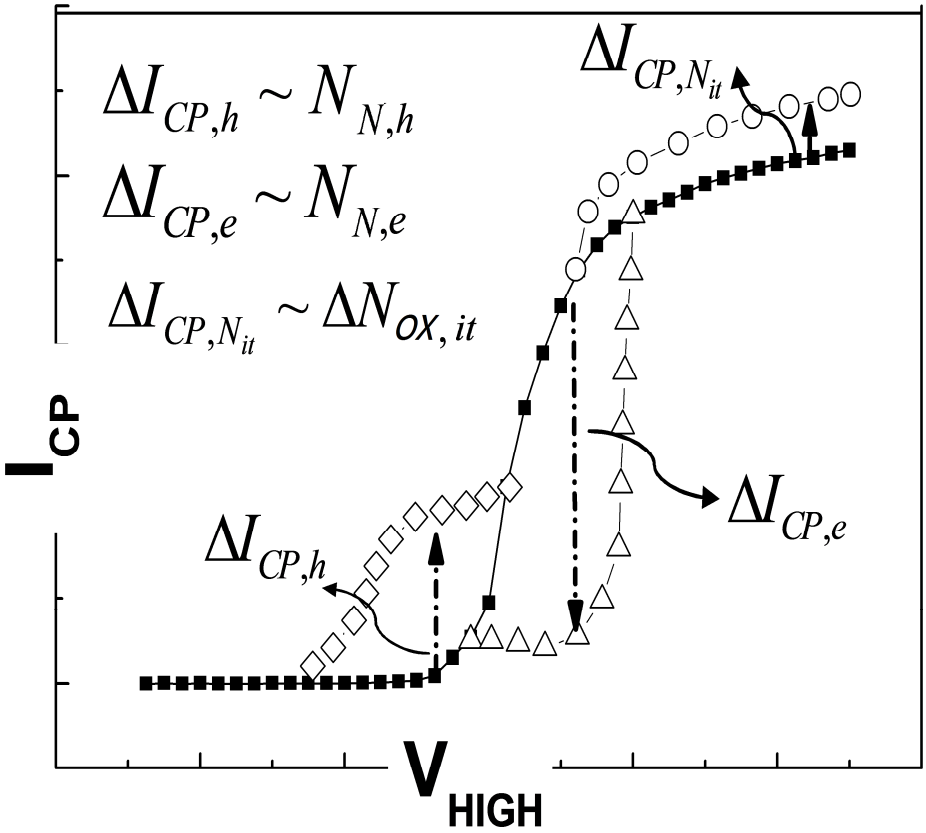


Fig. 4.3 The schematic FVb charge-pumping current curves related to the trapping charges and interface traps for a planar SONOS.

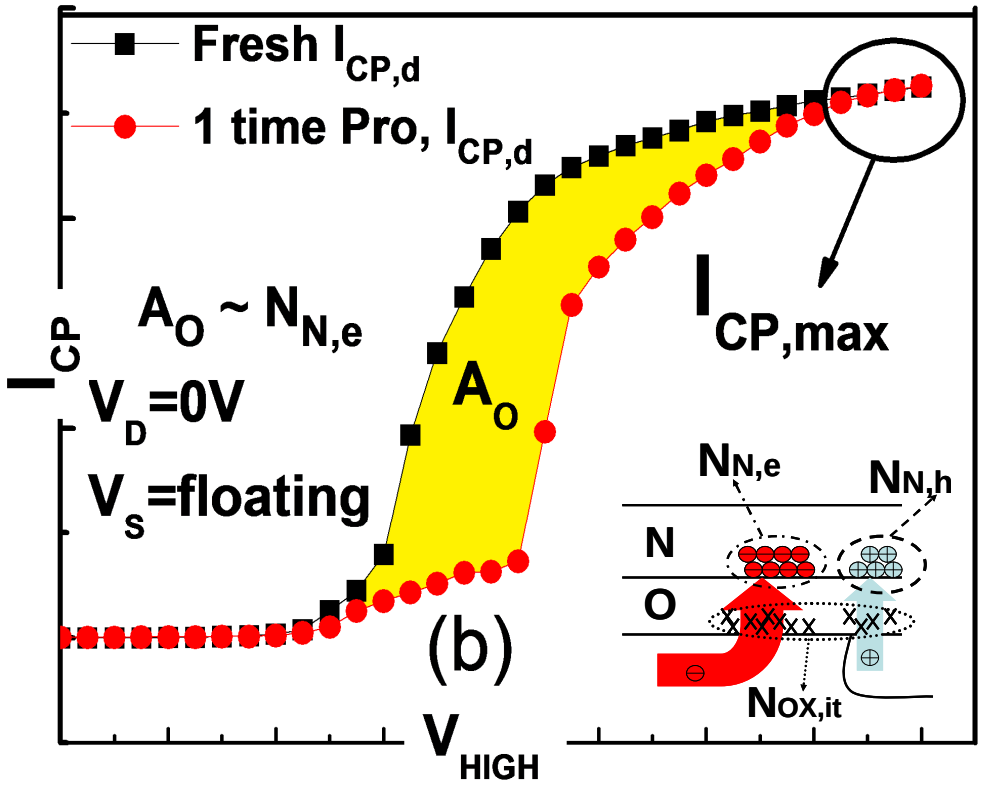
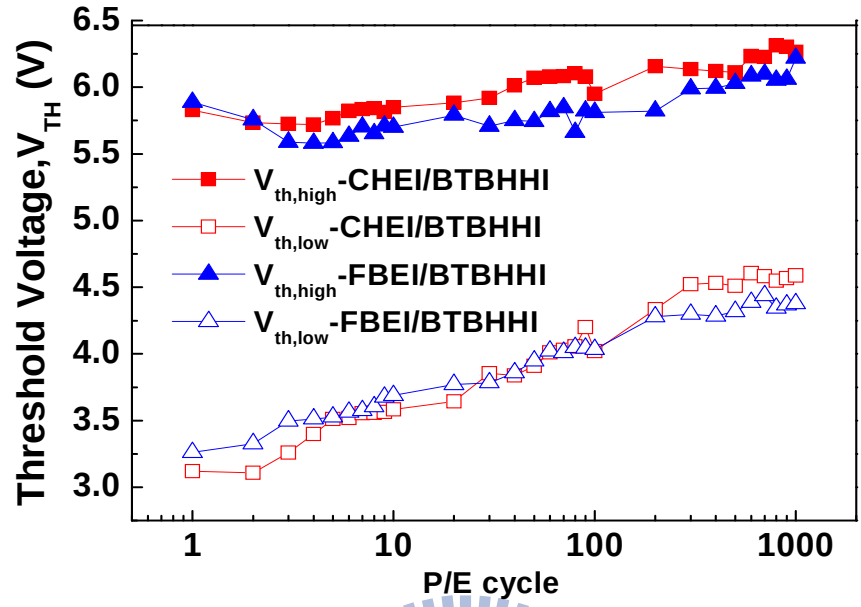


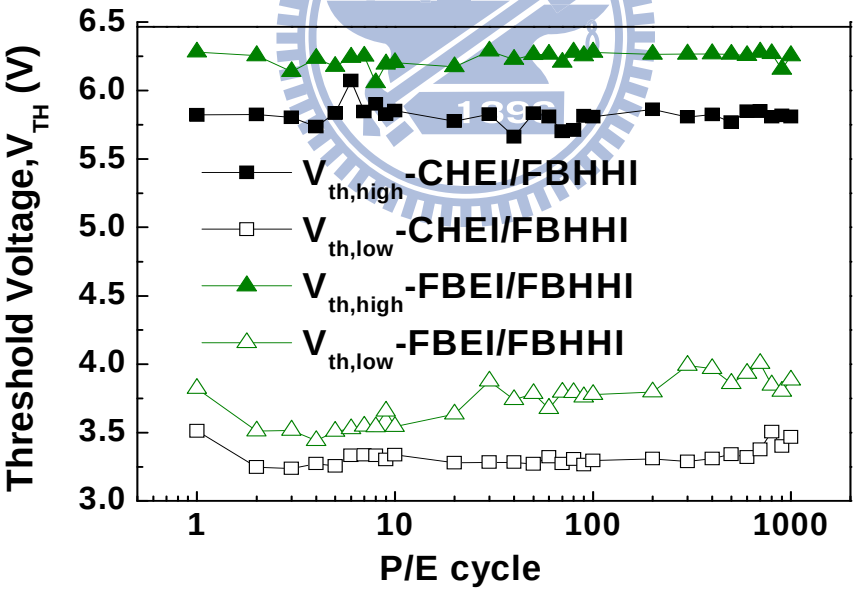
Fig. 4.4 The difference of $I_{CP,d}$ curves for fresh state and one time program state in a planar SONOS. The area A_o in the shade region represents the total stored electrons in the nitride after the first time programming.

	CHEI	FBEI	BTBHHI	FBHHI
V_G	7	7	-6	-6
V_D	5	-2/5	5	-2/5
V_S	0	floating	floating	floating
Time	1ms	1ms	2ms	1ms
Pulse type	unit-cycle	multi-cycle	unit-cycle	multi-cycle

Table 4.1 The basic operation conditions of planar SONOS.



(a)



(b)

Fig. 4.5 The endurance for planar SONOS with different operation combinations.

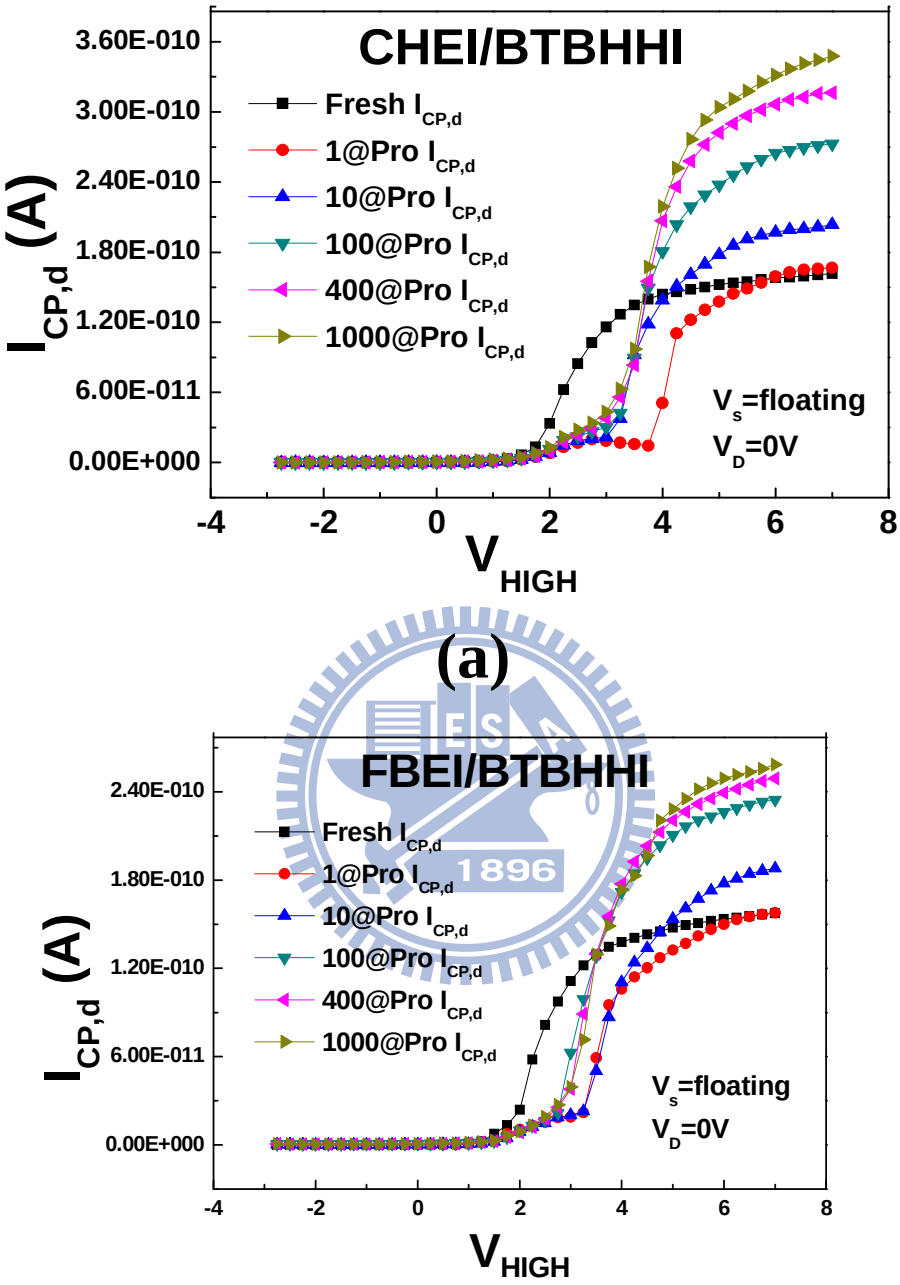


Fig. 4.6 The $I_{CP,d}$ versus V_{HIGH} for a planar SONOS with (a) CHEI/BTBHHI cycle and (b) FBEI/BTBHHI cycle during different cycling times by using fix base charge-pumping method.

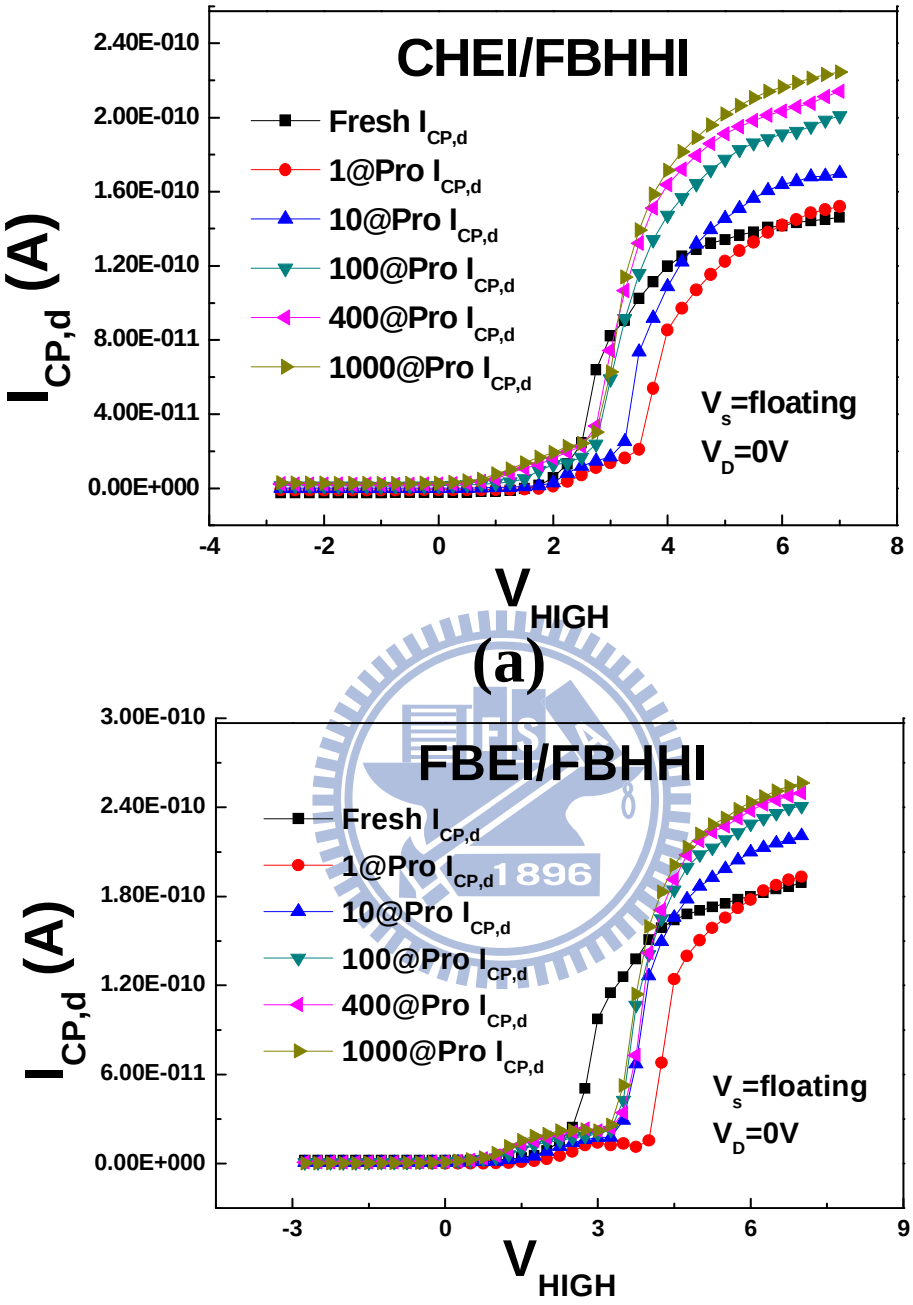


Fig. 4.7 The $I_{CP,d}$ versus V_{HIGH} for a planar SONOS with (a) CHEI/FBHHI cycle and (b) FBEI/FBHHI cycle during different cycling times by using fix base charge-pumping method.

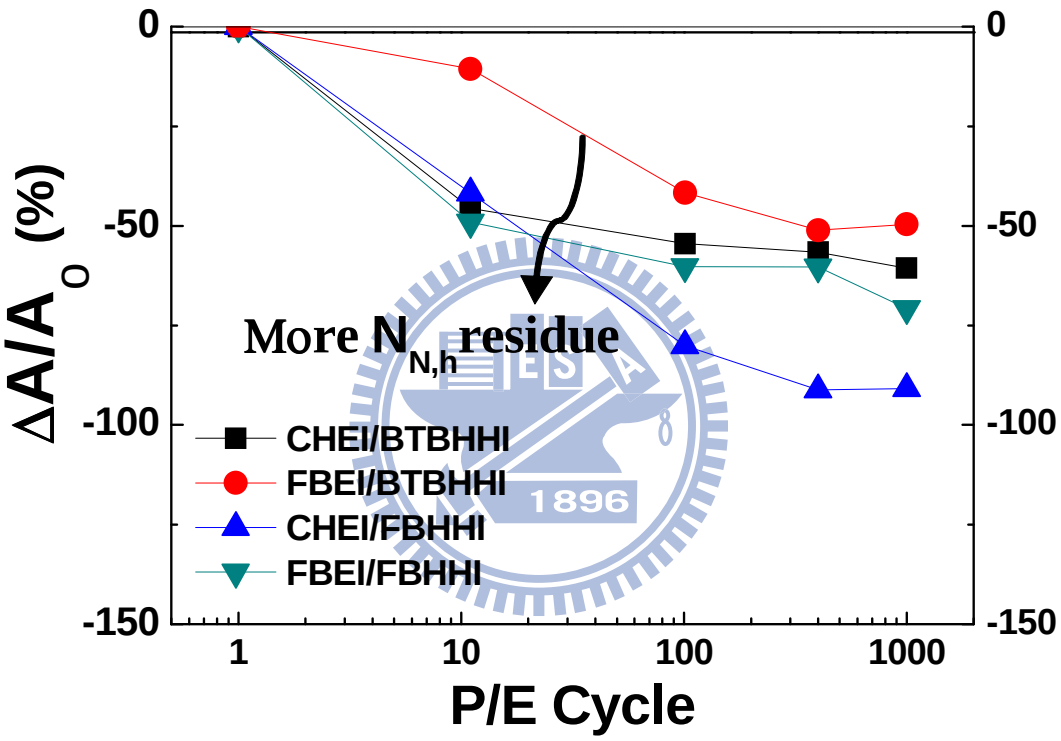


Fig. 4.8 The ΔA/Ao versus P/E cycle with four operating combinations.

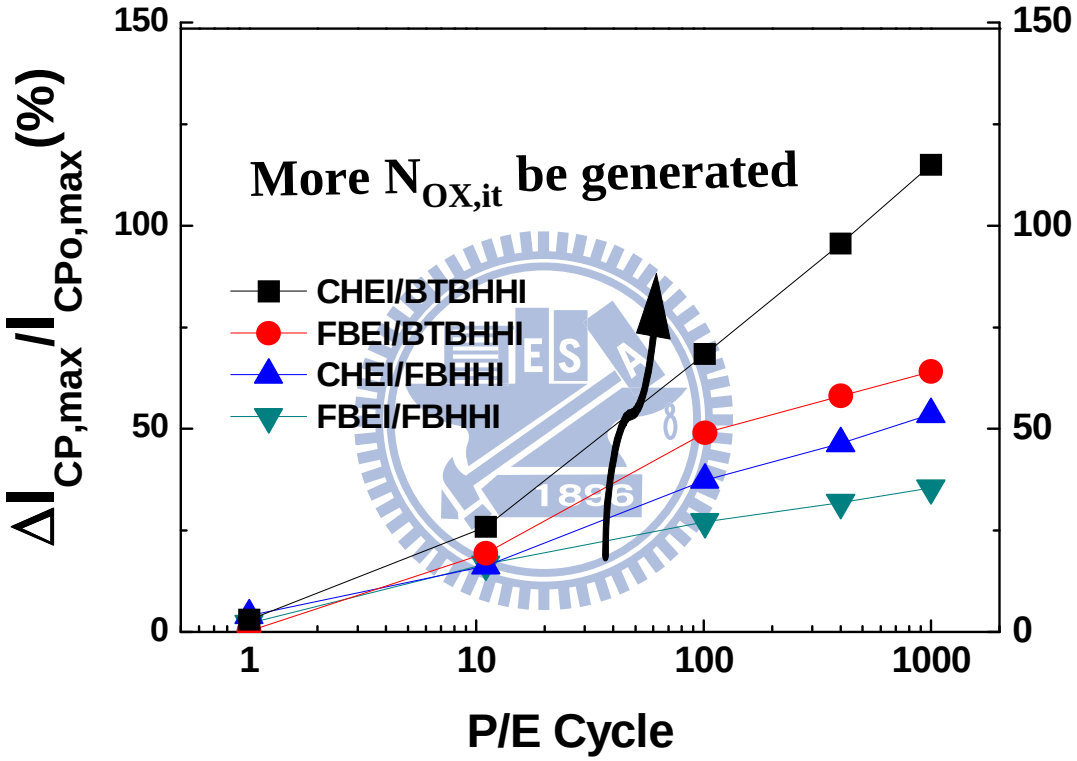


Fig. 4.9 The $\Delta I_{CP,max}/I_{CPo,max}$ versus P/E cycle with four operating combinations.

Chapter 5
Reliability Analysis of Two Bit per Cell Operation Split-Gate SONOS

5.1 Introduction

Recently, the charge-trapping devices, such as SONOS memory, are a promising solution for flash memory scaling. Moreover, many unique gate structure cells have been propose to improve the non-volatile memory (NVM) performance by corresponding operation scheme. To achieve the high density non-volatile memory, two bits per cell operation and multi-level logic state are necessary tendency. In [3], storing different amount of charges in the trapping layer distinguished different threshold voltages and can be treated as different combination of bits, the multi-level operation can be successfully implemented in split-gate SONOS (Fig. 5.1).

In this chapter, we will focus on the basic characteristics of reading methods in the unique split-gate structure. Furthermore, the fundamental two-bit operations were shown in the next section. The second-bit-effect-free in our split-gate can also be achieved, such that we can study the two-bit program/erase cycle with using different programming methods. Finally, we will provide some conclusions on the optimized operation combinations with better reliability.

5.2 The Basic Electrical Characteristic in Split-Gate SONOS

Figure 5.2 shows the drain current versus gate voltage under forward read (V_D= 1.8V) and reverse read (V_S= 1.8V) while the control gate was biased at 0.9V in a split-gate SONOS. As shown in Fig. 5.3(a), we observed the shift of threshold voltage with varying control gate voltages V_{CG} from 0.6V to 1V. The I_D-V_G curve with varying V_{CG} in Fig. 5.3(b) shows the uniform shift and the same value of sub-threshold swing when V_{CG} was increased. This phenomenon can explain the V_{CG} determined the peak of channel potential and then we simulated the channel potential with V_{CG} from 0.6 V to 1V when constant current I_D= 56nA in Fig. 5.4. The potential peak increased uniformly when V_{CG} is from 0.6V to 0.8V, but the large V_{CG} will decrease the potential peak seriously for the same constant current state when V_{CG} over 0.9V (not shown). We used a positive voltage at the control gate, can be regarded as the hole stored in control gate, just like as floating gate. Fig. 5.5(a) shows the threshold voltage for various drain voltages and a same control gate voltage and Fig. 5.5(b) exhibits the simulated channel potential for drain voltages from 0.2V to 1.8V, respectively.

In this section, we discussed the basic electrical characteristic with different control gate and drain bias conditions. Then, we will study the location of stored charge with different programming methods by changing the voltage condition when we read the threshold voltage.

5.3 Basic Characteristics on the Programming Cells

5.3.1 Results on the One-Bit Programming Cells

Figure 5.6 shows the diagram for the forward read and reverse read modes. First, for one-bit operation, we used SSI and FBEI program in split-gate SONOS. Here, only bit-1 was programmed and bit-2 was fresh state. The two physical logic states were demonstrated from the threshold voltage difference of the bit-1 and bit-2 during forward read and reverse read. Fig. 5.7 shows the window ($V_{TH,RR}$-$V_{TH,FR}$) versus Vth shift of bit-1 with the word gate length L_{WG}= 0.1um and 0.13um for split-gate SONOS. The second bit effect (SBE) can be suppressed when V_D= 1.8V during reading in our split gate structure, even if the ΔVth= 3V on bit-1 with L_{WG}= 0.1um, nevertheless, the window closed slightly (~0.5V) in the high ΔVth region, due to the stored electrons were for away from drain side, as show in [27]. This result will lead the mismatch phenomenon during cycling and induce the leakage mechanism during retention measurement.

To detect the location of programming charges with SSI and CHEI program, we changed the bias conditions of V_D and V_{CG} during reading the constant current voltage CC-Vth of 56nA. Fig. 5.8 (a) and (b) show the window ($V_{TH,RR}$-$V_{TH,FR}$) for various read voltages with different ΔVth shift of bit-1 in SSI and FBEI program, respectively. In Fig. 5.8, the window increased with the raising read voltage because the screening effect which comes from the local potential barrier lowering induced by the read voltage [24]. By increasing the ΔVth in bit-1, we need more read voltage to reduce the second bit effect and open the value of window. The result in Fig. 5.8(b) means the local increasing potential barrier by stored electrons can be lessened efficiently in FBEI program, comparing with the Fig. 5.8 (a), the second bit effect should be suppressed in SSI program by using larger read voltage. Generally, we

conclude that the injected electrons by FBEI program were more close to the drain than by the SSI program.

Figures 5.9 (a) and (b) show the window for various control gate voltages V_{CG} with different ΔVth shift of bit-1 in SSI and FBEI program. The slope in Fig. 5.9(a) exhibits the stable variation however the slope in the Fig. 5.9(b) was steep. It means the injected electrons by FBEI program can be affected while varying V_{CG}, but it is not obvious in SSI program. The experience result shows the possibility of the distribution of stored electrons by using FBEI program is wider than using SSI program. From the result of Fig. 5.9, the raising V_{CG} can enhance the window ($V_{TH,RR}$-$V_{TH,FR}$) and reduce the second bit effect during forward read. Apparently, the equivalent holes can reduce the raising channel potential by programming electrons in read and achieve the second-bit-effect-free. Fig. 5.10 represents the operating mechanism of SSI and FEBI program and explains the stored electrons distribution. We understood the mechanism of SSI program needing a high electric field to accelerate the programming electrons along the channel, leading to the distribution location correspond to the high electric field region. For FBEI program, the result shows the wider distribution of stored electrons, however, we can enhance the lateral electric field by raising $V_{D,HIGH}$ at T_2 phase, leading to the stored electrons were near to drain side. Nevertheless, for a large threshold voltage shift, the distribution of stored electrons became boarder, so we should increase the read voltage to keep the same window with different ΔVth cases.

5.3.2 Applications to Two-Bit Programming Cells

Base on the basic reliability operation, we will show the program transient, the

characteristic of endurance, and the retention for two-bit operation. First, Fig. 5.11 shows the programming speed for first bit and second bit by SSI and FEBI program. We found the second bit transient was decelerated on using SSI, because the electron of bit-1 increased the channel potential and reduced the electric field along the channel. So far, we understood the advantage of using multi-cycle pulse series, e.g., FBEI is the two-bit operation is mutual containment during programming by superiority of one-side operating.

In chapters 3 and 4, it has been realized that the FBHHI can reduce the oxide degradation. In order to decrease the erasing breakdown, we tried two operating combinations, FBEI/FBHHI and SSI/FBHHI, for endurance measurement. The cycle sequence is program bit-1 => program bit-2 => erase bit-2 => erase bit-1, which is the worst operating sequence [28]. Fig. 5.12 shows endurance characteristics of two-bit per cell application, using SSI program and FBHHI erase. The window of SSI/FBHHI closed gradually by second bit transient slowing down. Fig. 5.13 shows the endurance characteristics of two-bit per cell, by using FBEI program and FBHHI erase. The FBEI/FBHHI kept the window of 2V and the same ΔVth shift on bit-1 sand bit-2. Next, Fig. 5.14 shows retention behaviors after 10k P/E cycles of bit-1 and bit-2 in different states, respectively for split-gate SONOS with SSI and FBEI program. As we can see, FBEI has 1.6V window after ten years in Fig. 5.14 and is larger than the window (~1.4V) of SSI retention.

More importantly, the retention behavior shows the reliability of the bottom oxide, which leads to with using by multi-cycle mode, e.g. FBEI, FBHHI, less damage can be achieved. In short, for the 2-bit per cell operation, the new scheme exhibits much better retention and endurance characteristics.

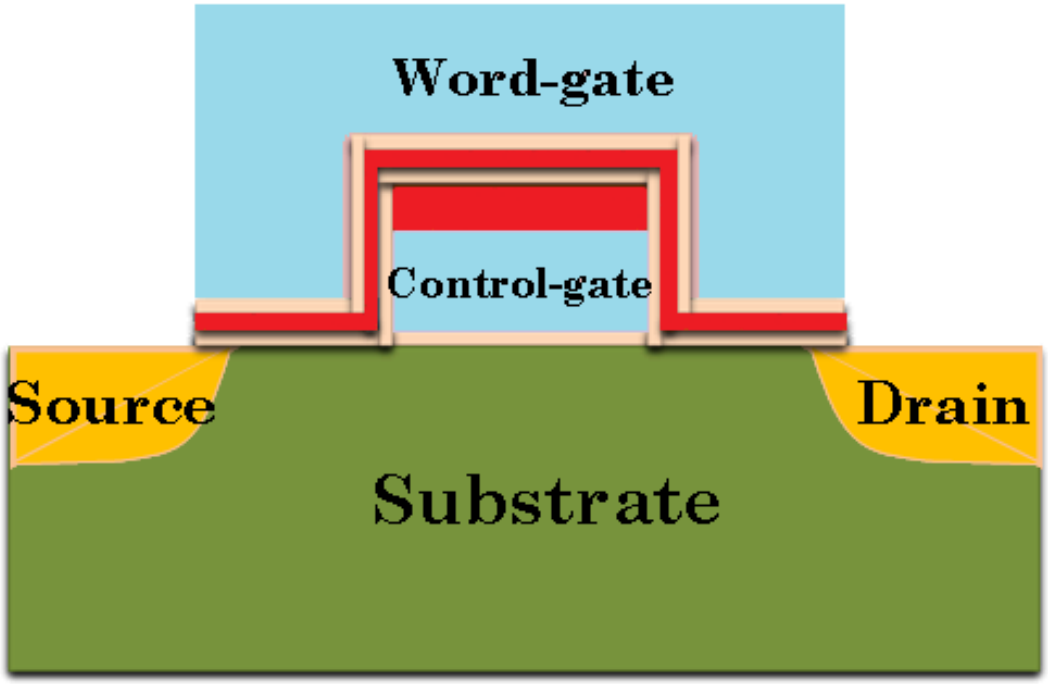


Fig. 5.1 The schematic structure of the split-gate SONOS.

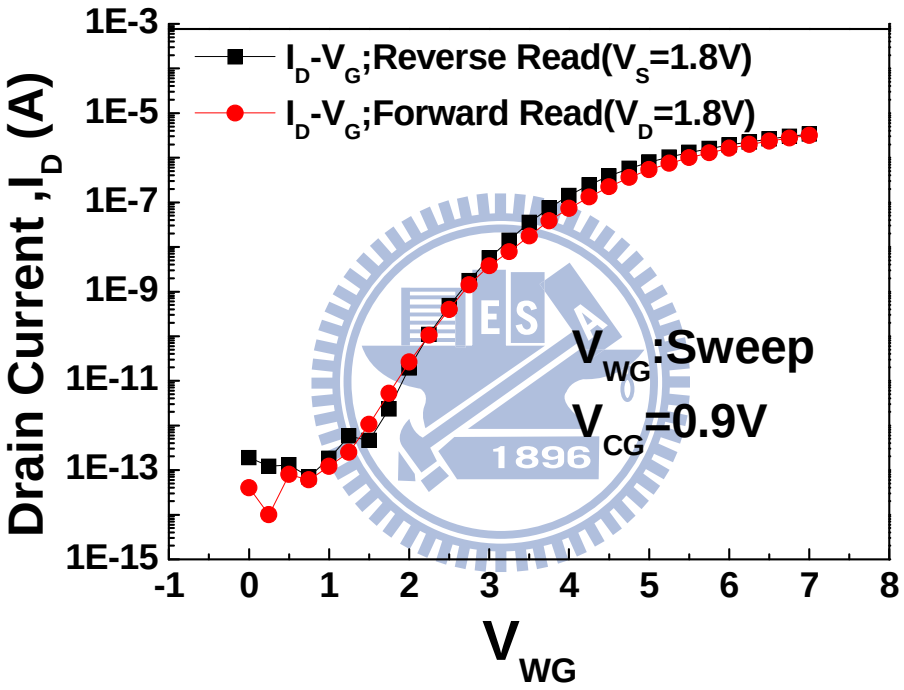


Fig. 5.2 The drain current versus gate voltage under forward read and reverse read when the V_{CG} was biased at 0.9V in a split-gate SONOS.

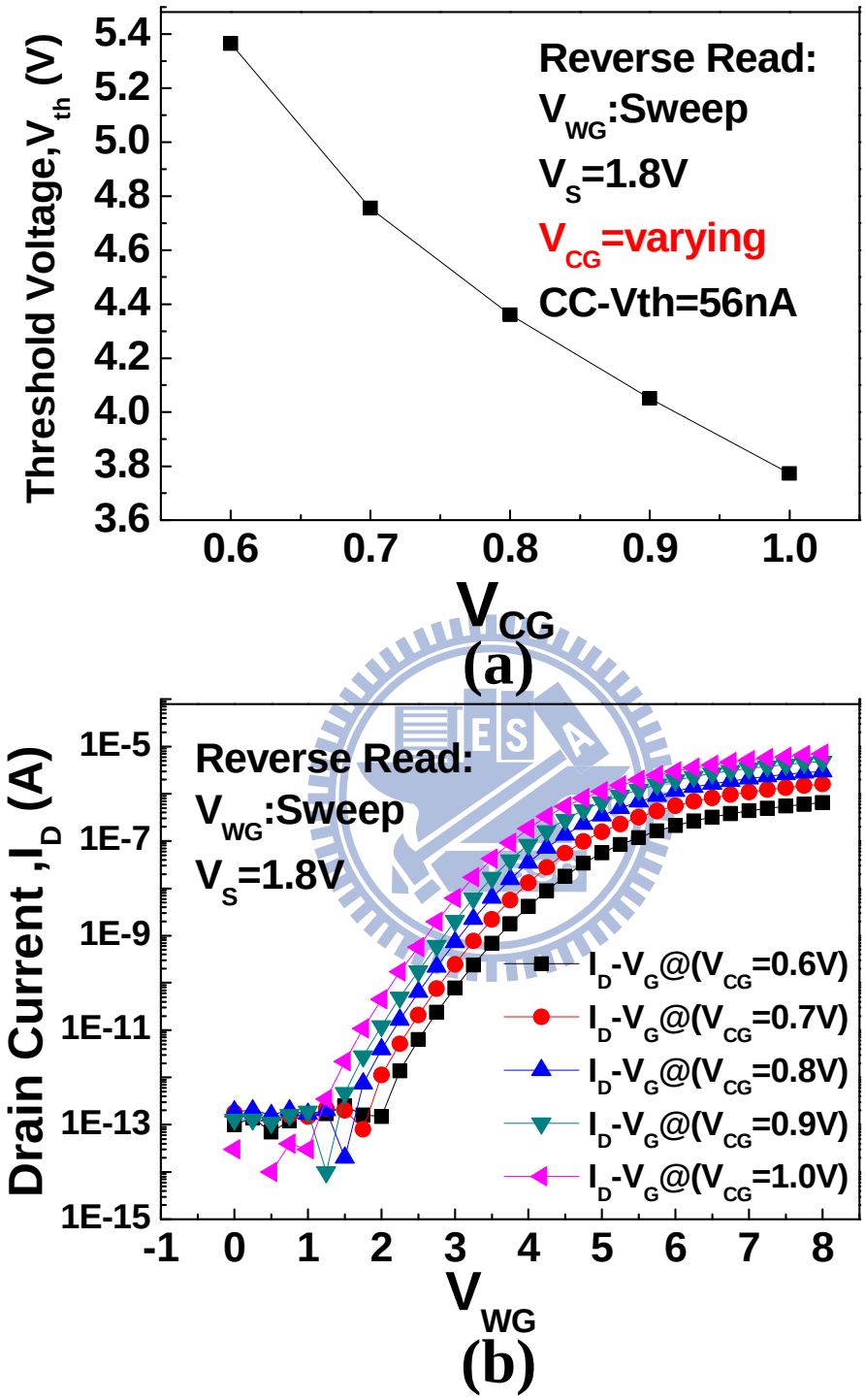


Fig. 5.3 (a) The threshold voltage shift with varying V_{CG} .

(b) The I_D-V_G curves with different V_{CG} conditions.

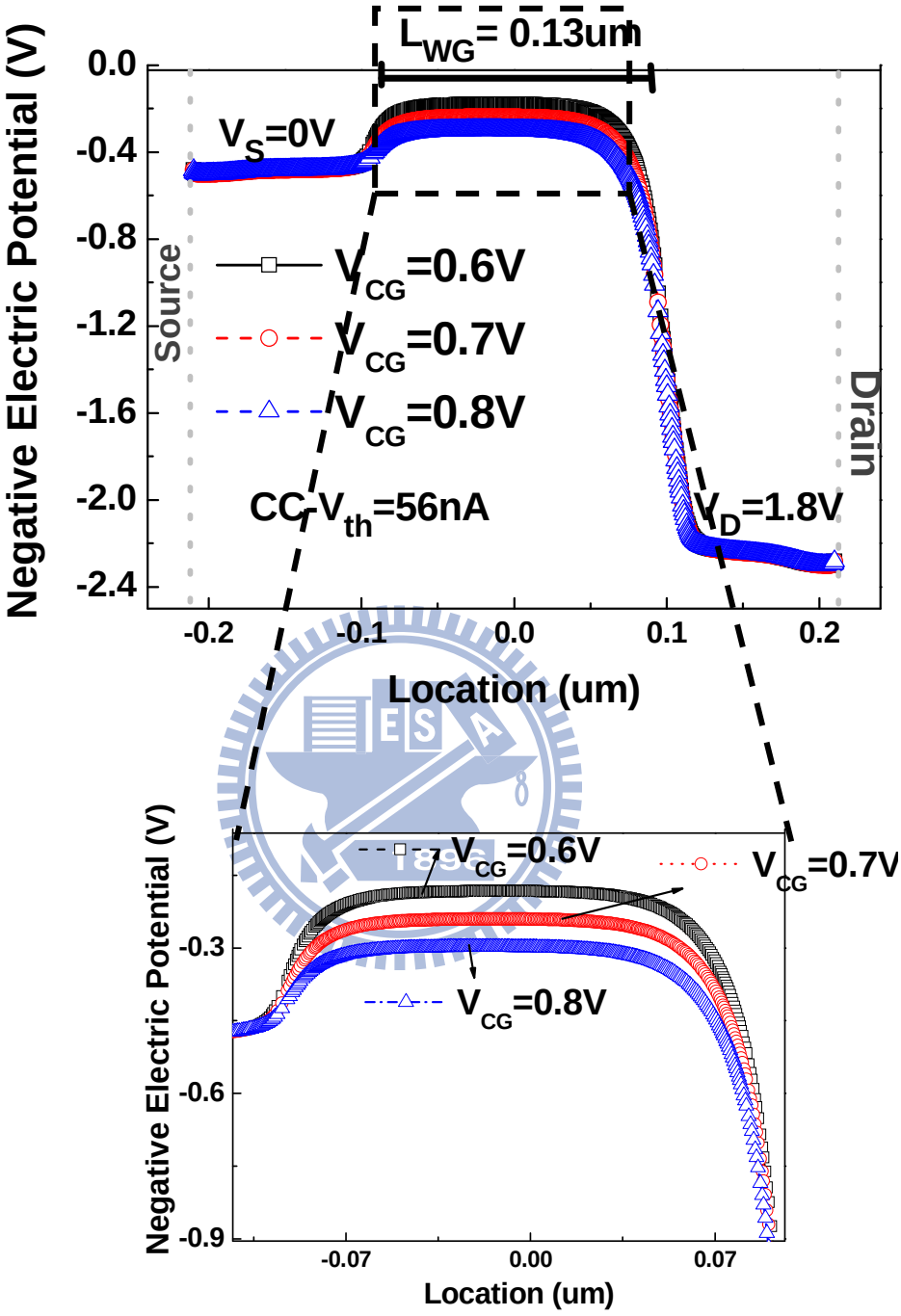


Fig. 5.4 The negative channel potential along lateral location with different V_{CG}=0.6V, 0.7V and 0.8V conditions at CC-Vth=56nA.

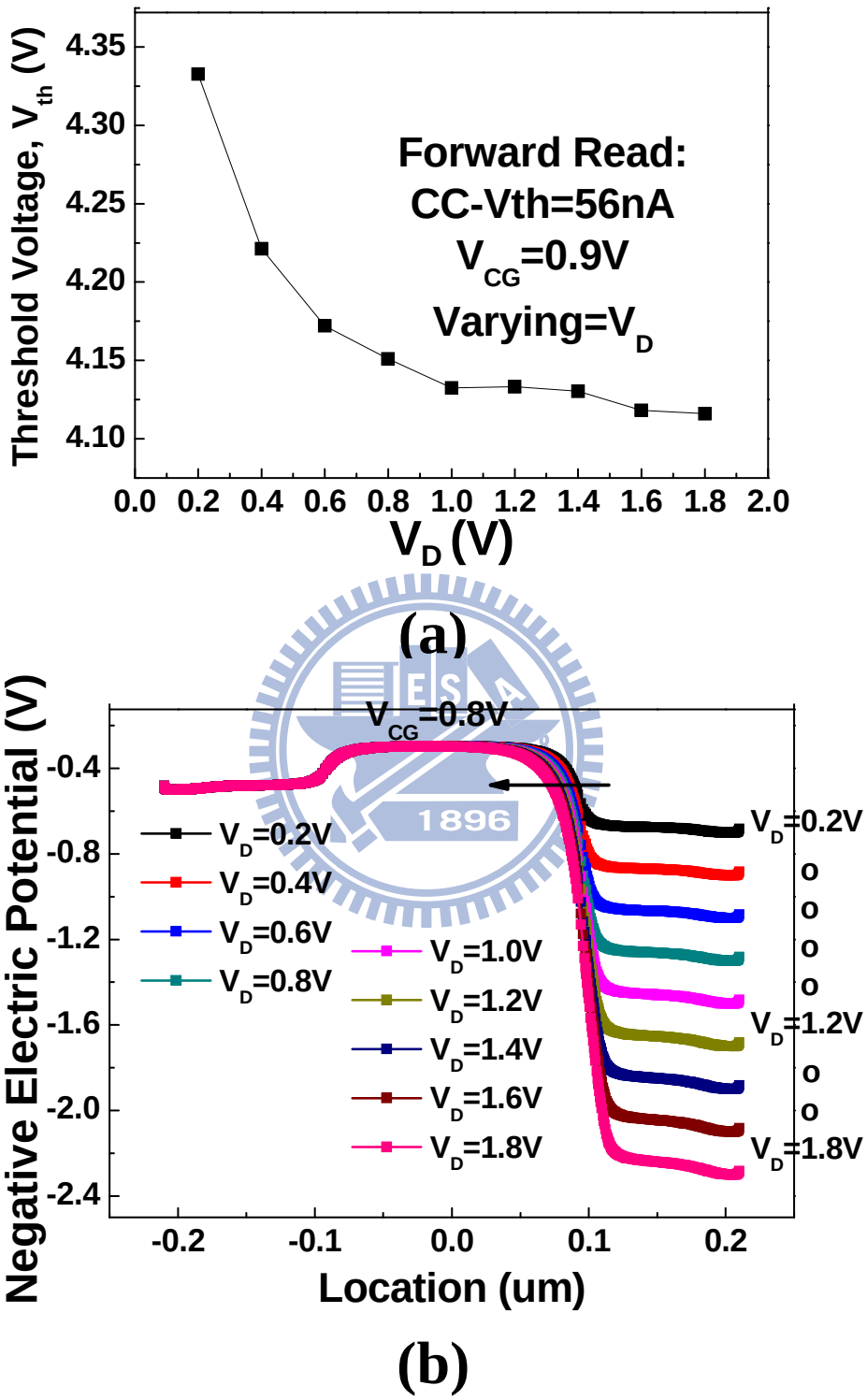


Fig. 5.5 (a) The threshold voltage shift with varying $V_{D.}$

(b) The negative channel potential along lateral location with different V_D =0.2 ~ 1.8V conditions.

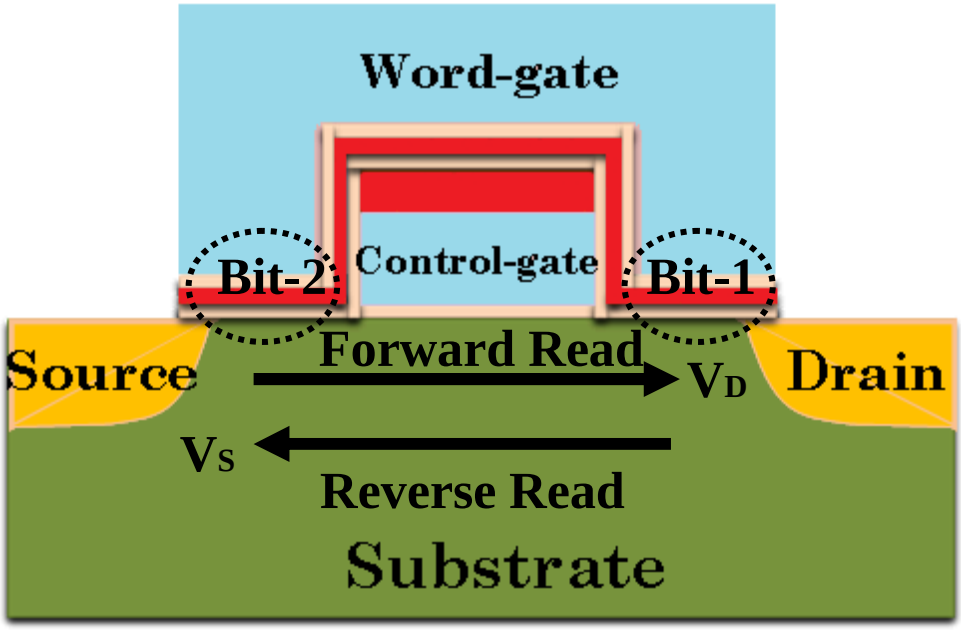


Fig. 5.6 The diagram for the forward read and reverse read modes.

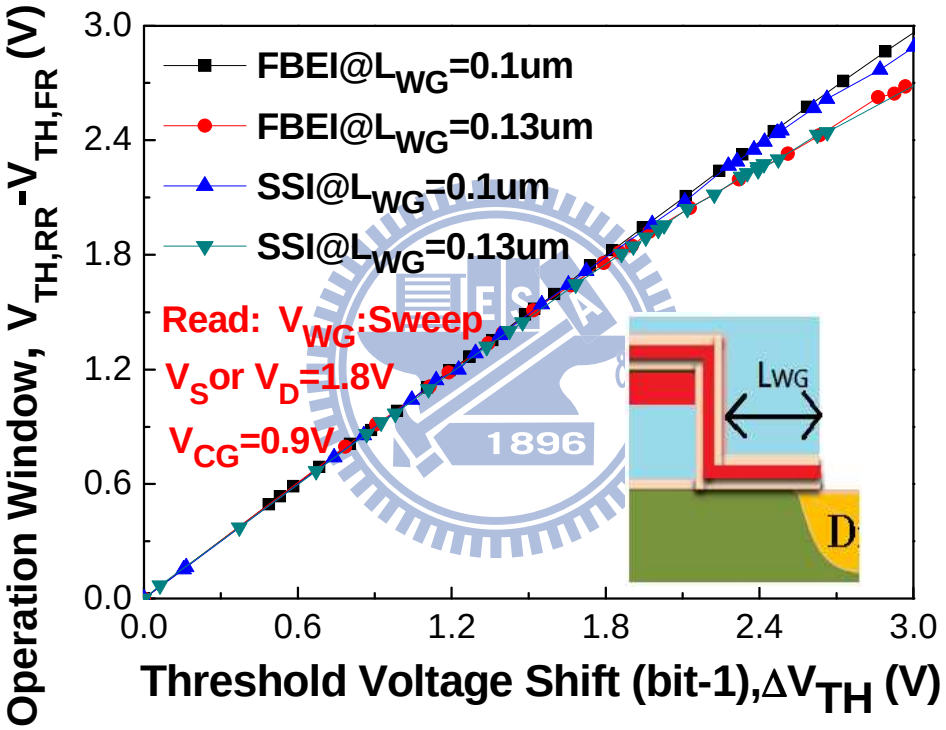
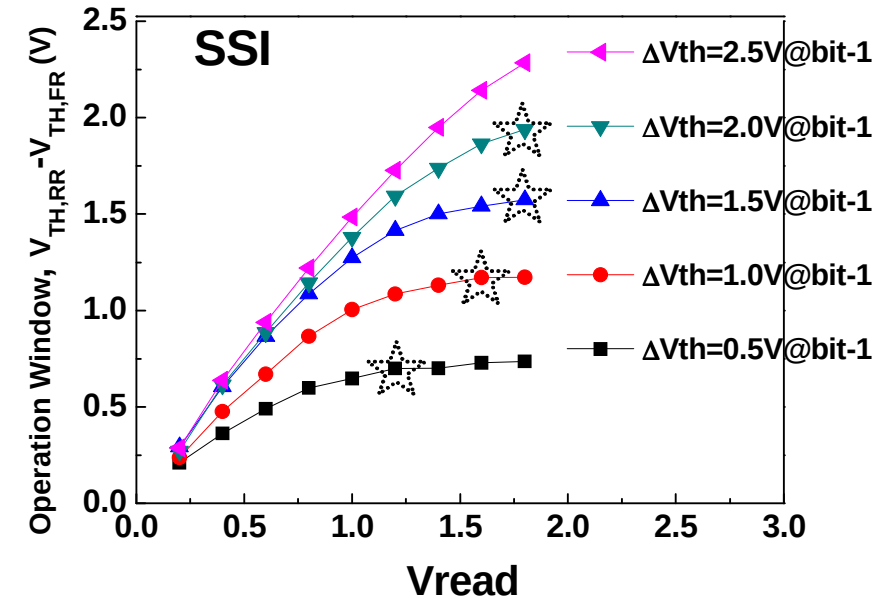
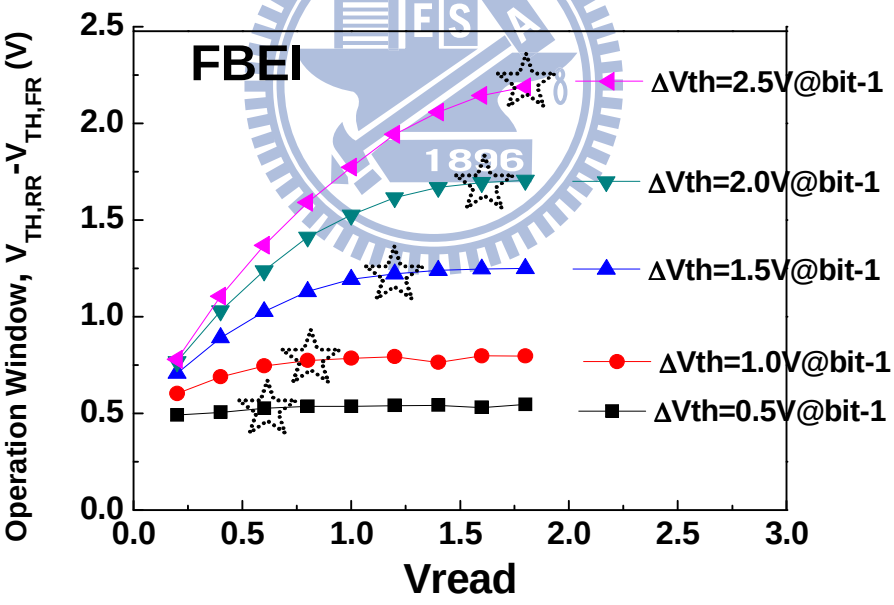


Fig. 5.7 The window versus Vth shift of bit-1 for split-gate SONOS with L_{WG}=0.1 and 0.13 um.



(a)



(b)

Fig. 5.8 The window for various read voltage with different ΔVth (bit-1), using (a) SSI program and (b) FBEI program. The star symbol indicated the saturation point.

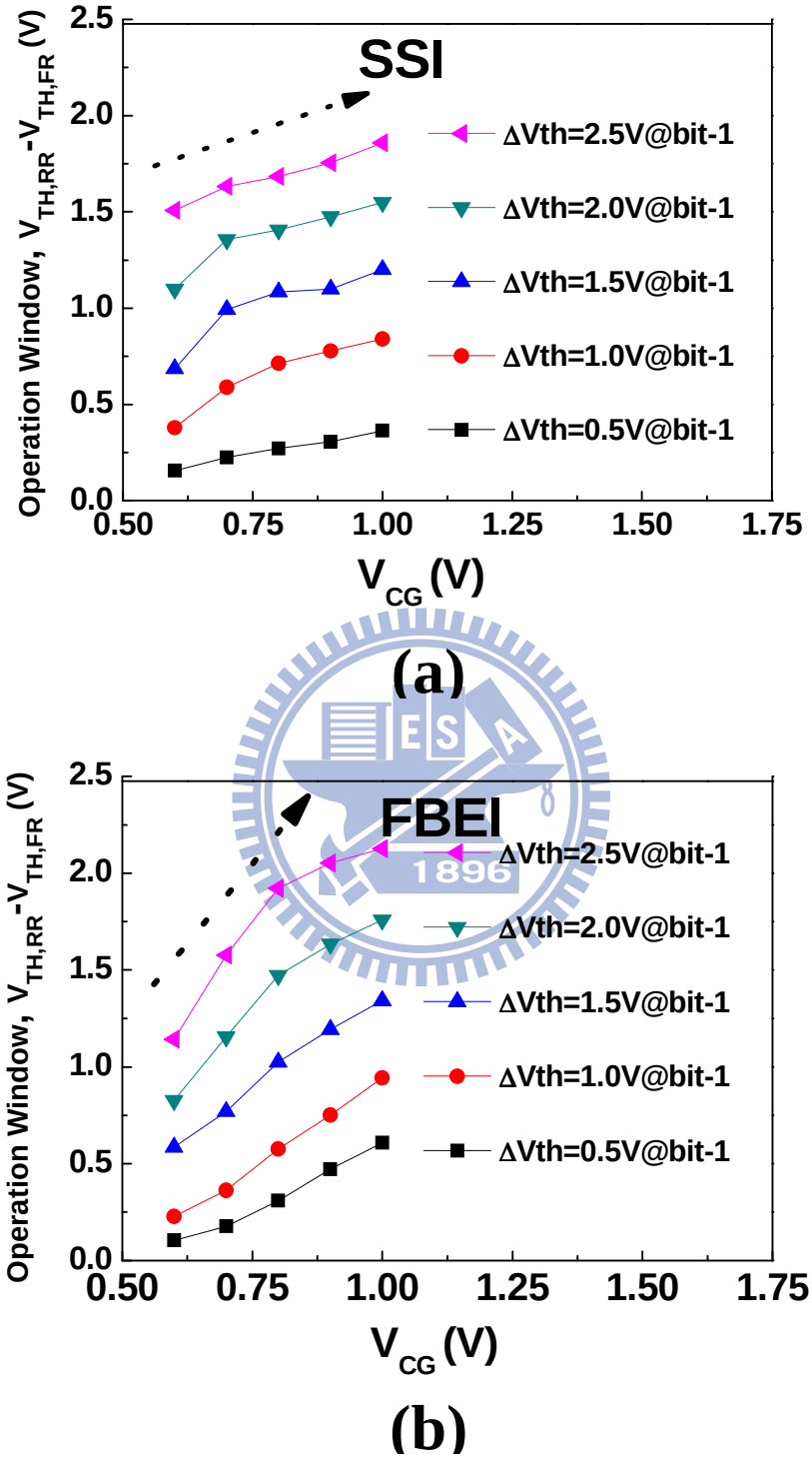


Fig. 5.9 The window for various V_{CG} with different ΔVth of bit-1 by (a) SSI program and (b) FBEI program.

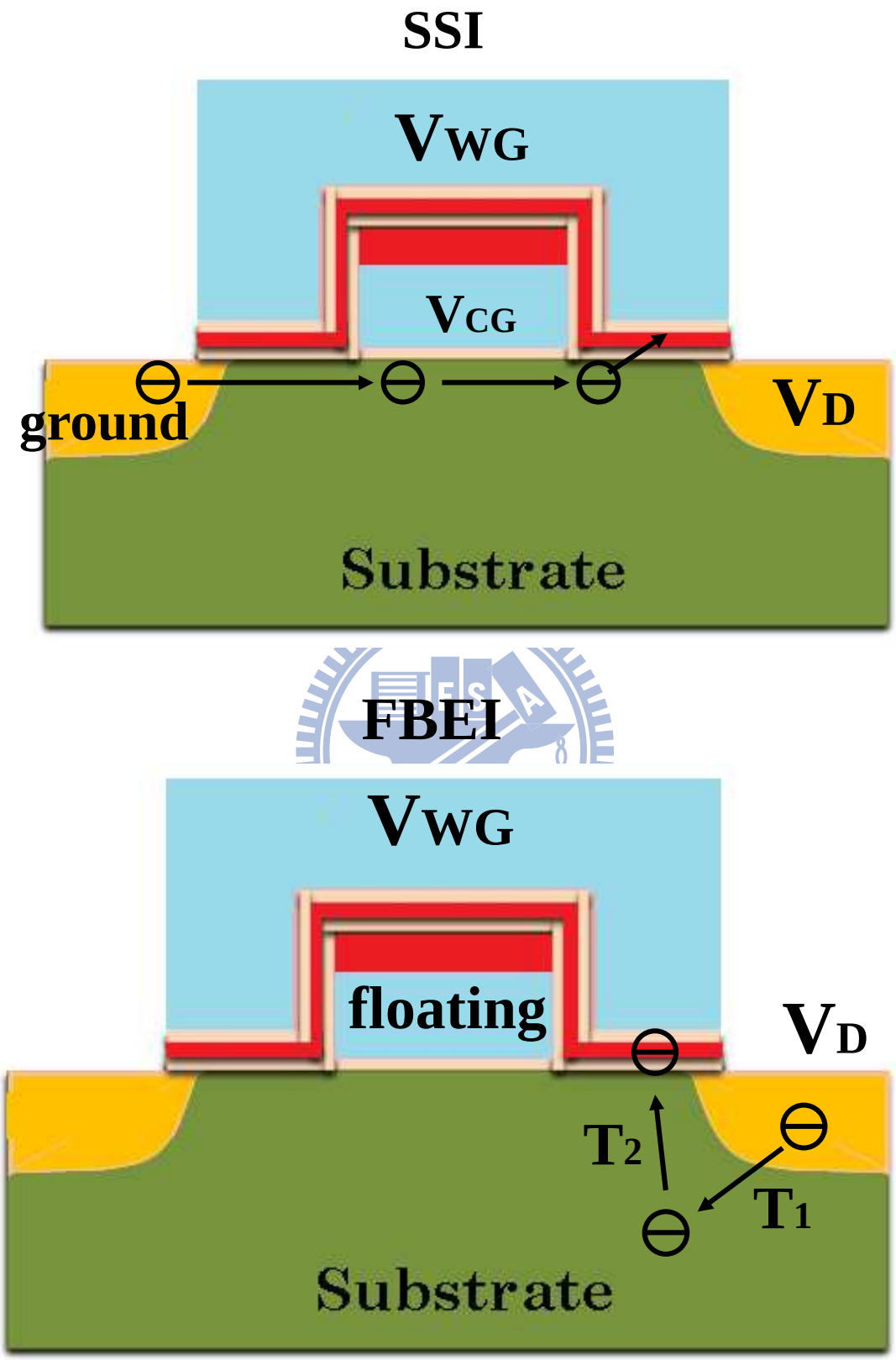


Fig. 5.10 The operating mechanism of SSI and FBEI programs.

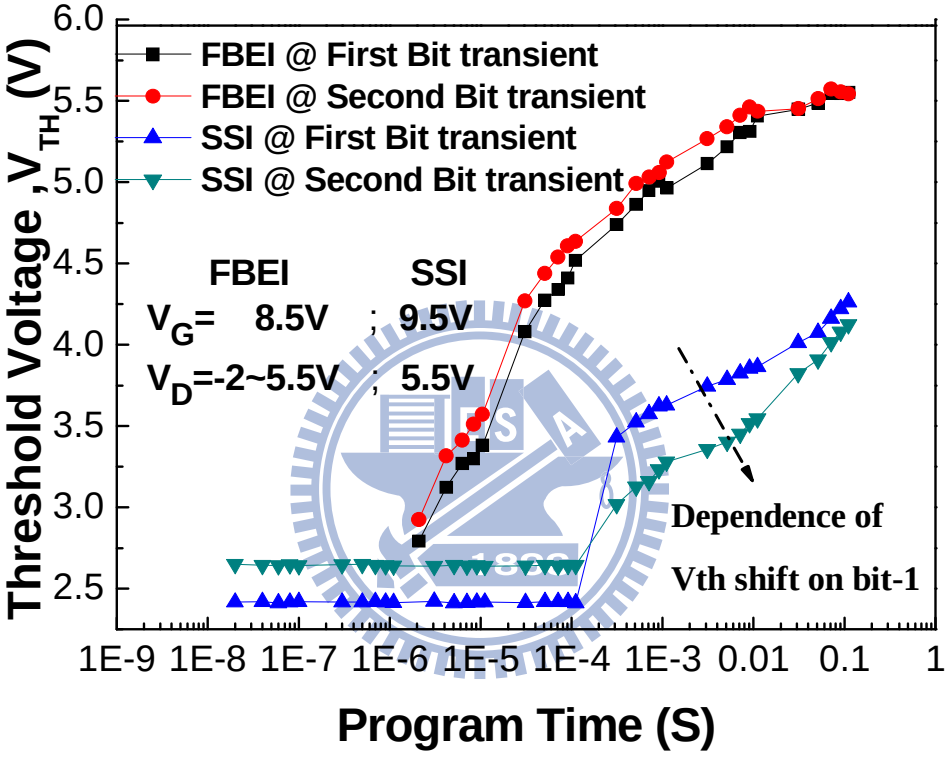


Fig. 5.11 The programming speed for first bit and second bit by FBEI and SSI programs.

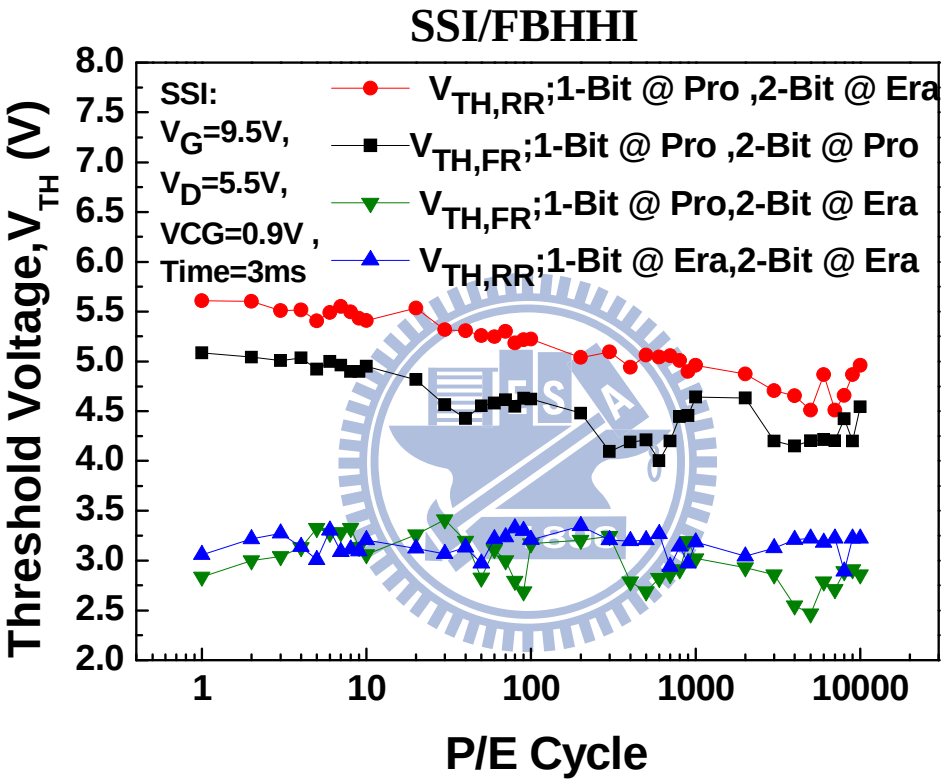


Fig. 5.12 Endurance characteristics of two-bit per cell application, using SSI program and FBHHI erase.

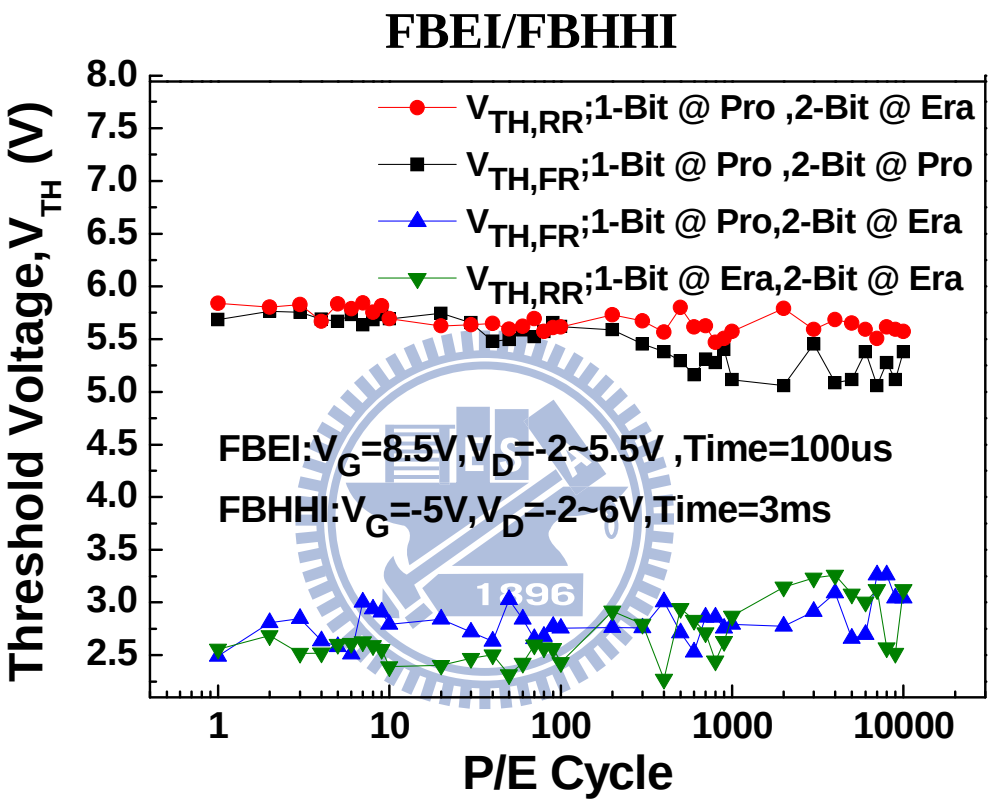


Fig. 5.13 Endurance characteristics of two-bit per cell application, using FBEI program and FBHHI erase.

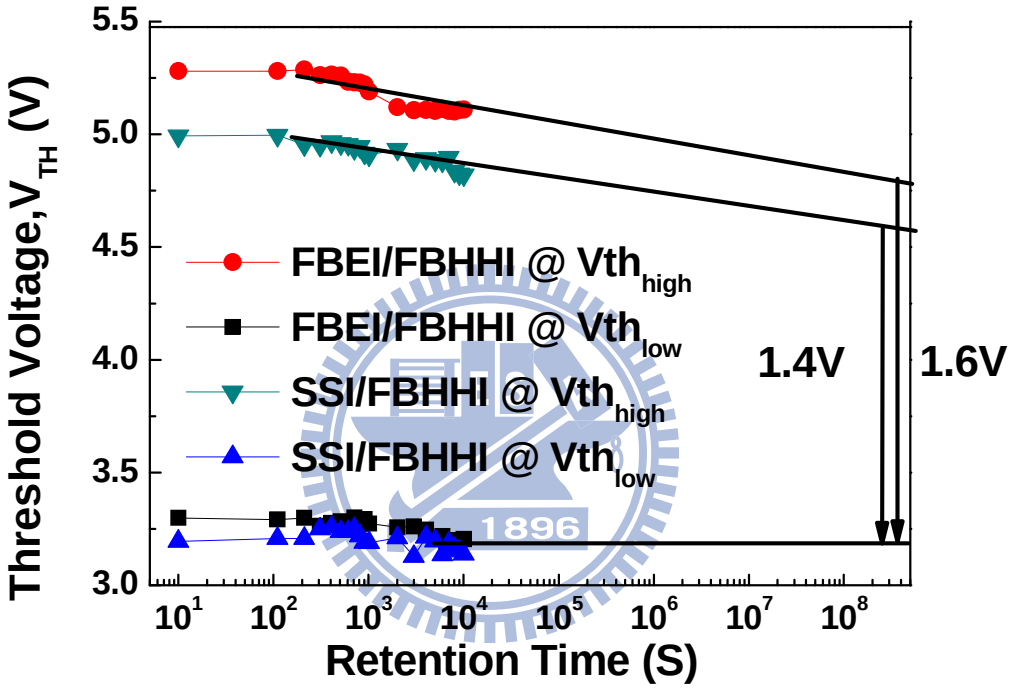


Fig. 5.14 Retention behaviors after 10k P/E of Bit-1 at Vth $_{high}$ and Vth $_{low}$ states with FBEI/FBHHI and SSI/FBHHI combinations.

Chapter 6

Summary and Conclusion

In this thesis, a novel operating scheme has been propose for 2-bit/cell split-gate SONOS. We proposed a new mode of pulse operation to compare it with the conventional operation scheme in split-gate SONOS. A novel operation concept used the multi-cycle pulse series and suitable forward-bias to enhance the efficiency of program/erase. The multi-cycle pulse type can achieve a superior operation efficiency, even it only needs half of time for the charge injection. The reliability for junction leakage was dominated by forward-bias stress, while it exhibits a stable value of the leakage current in the new operating scheme. Above all, threshold voltage was not disturbed with a suitable forward-bias current.

Next, we discussed the different operation combinations in planar SONOS and analyzed the reliabilities for a P/E cycling device using different operating schemes. By calculating a new parameter $\Delta A/A_o$, we found the multi-cycle pulse series, e.g., FBEI and FBHHI, can reduce the misalignment in the trapping memory, and by calculating $\Delta I_{CP,MAX}/I_{CPo,MAX}$, FBHHI can suppress efficiently the oxide degradation in comparison to BTBHHI.

On the other hand, we did the test about the multi-cycle pulse type for two-bit per cell operation reliability in split-gate SONOS. We used the unique double-gate structures to discuss the second-bit-effect and different programming scheme induced charge distribution in the dielectric layer. FBEI could inject the electrons near the drain side, although it had wider distribution location than SSI in the nitride, but it can

keep a stable endurance window by using the FBHHI erase. More importantly, for the two-bit per cell operation, the new operating scheme exhibited much better program speed, endurance, and retention characteristics in split-gate SONOS and achieved a better alignment between the two bits.

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