國 立 交 通 大 學

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碩 士 論 文

22 奈米高介電係數金屬閘極電晶體之正向偏壓溫度不穩定性分析及模擬

Positive Bias Temperature Instability(PBTI) Analysis and Simulation in 22 nm High-k Metal Gate nMOSFETs

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摘要

在本篇論文中，我們提出了一個新的方法來模擬高介電係數CMOS在經過高溫偏壓操作後截止電壓的分佈。在量測上我們使用快速暫態的量測技術來減少量測的延遲時間，我們發現在經過高溫偏壓操作後由於電子被捕捉使得電流發生階梯狀衰減的現象。

為了了解在高溫偏壓操作時的單電子捕捉的現象，我們首先萃取由於電子被捕捉時電流的衰減量的機率分佈，接著我們也建立了在施壓(stress)及回復(recovery)時的時間模型。由以上實驗所得到的參數進行蒙地卡羅模擬來預測經過高溫偏壓操作後截止電壓的分佈。

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Abstract

In this dissertation a new method to predict the post-stress threshold voltage distribution is introduced. We proposed the fast transient measurement, which minimizes the switching delay between stress and measurement. Consequently, a staircase-like post-positive bias temperature (PBT) current instability caused by single electron trapping is investigated.

To analyze the characteristic of PBTI stress induced threshold voltage degradation. First, we extract the probability distribution of the single electron trapping induced drain current degradation. Second, the time model is developed in stress and recovery phase. According to the characterization of the single charge

phenomenon, we proposed a Monte Carlo simulation to simulate the post-stress threshold voltage distribution.

Acknowledgement

首先，我要感謝我的指導教授汪大暉老師，能夠提供一個設備完善的實驗資源，老師謝心與耐心的教導使我們能夠學習到正確的研究態度與方法。另外，博士班的邱榮標、馬煥淇學長也是從我剛進實驗室到要畢業的現在一直在各方面都給了我很大的幫助,使我獲益良多,實驗室同學王明緯、周承翰還有學弟們不管在研究上以及日常生活中都帶給了我許多支持與樂趣。

最後我要感謝我的父母以及女友，在這段期間給我的支持鼓勵。謝謝！

Contents

Figure Captions

Chapter 1
Introduction

Metal oxide semiconductor field effect transistors (MOSFETs) have been continuously scaled down since it was developed. Thickness of gate dielectric is required to be smaller in the progressive technology node, as the device scaled down, it reached the physical limit of conventional silicon dioxide (SiO_2) MOSFETs, SiO_2 is no longer an appropriate material of gate dielectric, because of the quantum mechanical direct tunneling leakage current increase in MOSFETs with ultra-thin gate oxide [1.1], which induced standby power consumption. In order to maintain the scaling roadmap, MOSFETs with high permittivity (high-k) material and metal gate is proposed. Recently, HfO_2 has been successfully integrated into CMOS as gate dielectric. The MOSFETs with high-k/metal gate have good reliability, comparable mobility (as SiO_2), and the gate leakage is greatly reduced at the same equivalent oxide thicknesses (EOT) [1.2-1.4].

Although the technique of high-k/metal gate is regarded as a good solution of the device scaling problem, it also produced other reliability issues. Positive bias temperature instability (PBTI) is one of the serious reliability concerns [1.5]. Threshold voltage (V_T) of a MOSFET is observed to shift under a positive bias with stressing time, this phenomenon which caused by single charge trapping is called PBTI [1.6-1.8]. From Fig.1.1 compare with SiO_2, PBTI induced V_T shift increased in the Hafnium based high-k gate dielectric devices. It shows that the Hf plays the role of creating traps in the high-k gate dielectric stack [1.5].

In Chapter 2, we showed how to set an experiment with a novel transient measurement to characterizing single electron trapping in the PBTI stress phase, and the single electron emission in the PBTI recovery phase. In the stress phase the single electron trapping caused staircase-like drain current degradation, on the other hand the post-stress recovery transient of drain current in recovery phase can be measured [1.7-1.9]. Finally, the probability distribution of drain current fluctuation has been developed [1.7], also we set up the time model in the stress and recovery phase, and a comparison of different condition PBTI stress will be shown. Because of the random telegraph noise (RTN) and PBTI are both single charge effect, the difference of ΔI_d probability distribution of these two mechanism is investigated. At last we showed the dimensional dependence of device in PBTI stress.

In Chapter 3, based on the probability distribution of ΔI_d and the time model of PBTI stress and recovery phase in the previous chapter, we developed a new method to simulate the PBTI stress induced V_T shift by a Monte Carlo simulation. Using this method we can simulate the post-stress V_T distribution and the V_T distribution after recovery, based on the simulation result the device lifetime can be well estimated. Finally, we give a conclusion in Chapter 4.

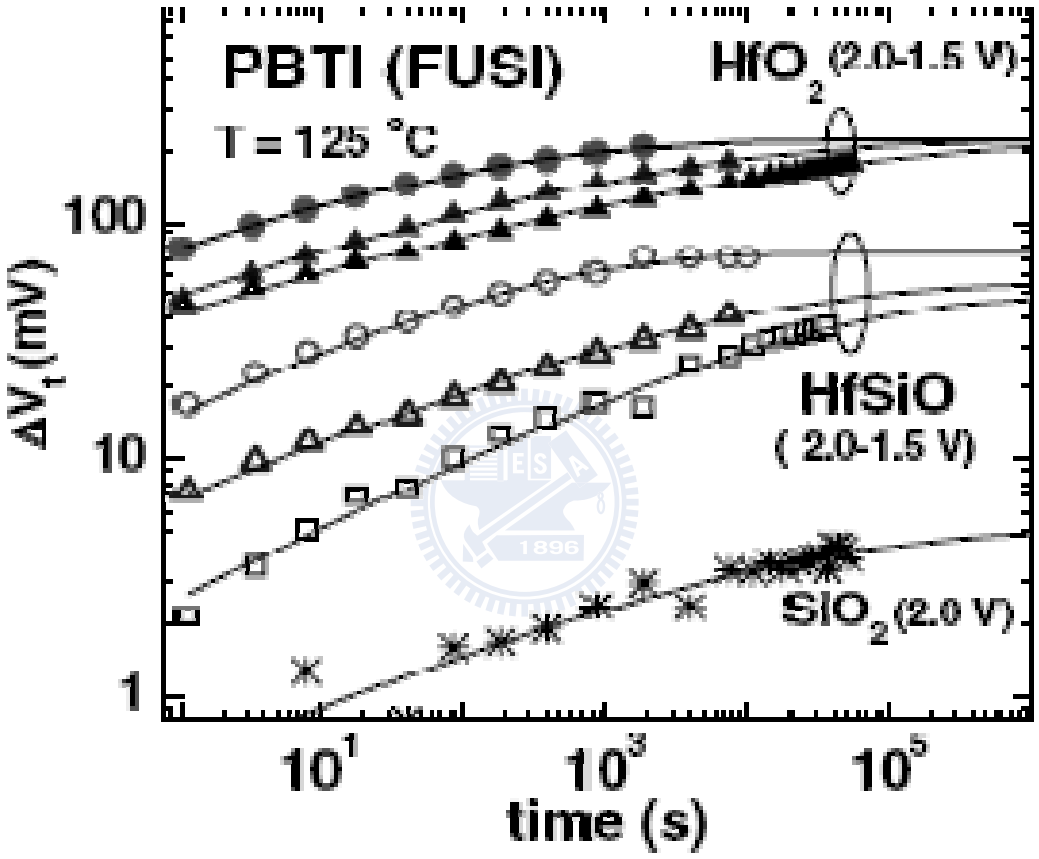

Fig. 1.1 PBTI becomes worse in the Hf based high-k device.

Chapter 2
Single Electron Phenomena in PBTI

2.1 Introduction

The cause of PBTI is believed to be essentially related to charge trapping in high-k layer [2.1]. PBTI induced V_T shift is traditionally characterized by stressing transistors at a high temperature and electric field, periodically interrupting the stress to monitor threshold voltage or drain current, but these methods wasted lots of devices. We proposed a new method to simulate the post-stress V_T distribution from the single electron process.

First, to identify the charge trapping mechanism a novel method for characterizing high-k gate dielectric is demonstrated [2.2-2.4], in which direct measurement of ingle electron trapping manifested by discontinuous step-like drain current is measured. Similarly, the charge de-trapping mechanism in recovery phase can be observed by the drain current recovery. The ΔId distribution is found by analyzed the drain current fluctuation caused by electron trapping. We compare the distribution in stress and recovery phase, and in different stress voltage. Because RTN and PBTI are both related to single charge effect, we also showed the difference of the ΔId distribution in these two mechanism.

Second, with the record of the electron trapped time, the time model in PBTI stress is developed, based on the model we can predict electron trapped time. On the other hand, the recovery time model is found in the same way. At last we investigated the device width dependence in the recovery phase.

2.2 Measurement setup

BTI induced V_T shift is traditionally characterized by stressing transistors at a high temperature and electric field, periodically interrupting the stress to monitor threshold voltage or drain current as shown in Fig. 2.1. Although the fast transient method solved the problem of the delay time between switching from stress and threshold voltage measurement, still, these method should waste lots of devices and measurement time to complete the V_T distribution. Due to these disadvantages of the traditional method, we proposed a new method to simulate post-stress V_T distribution which showed in Fig. 2.2. In our method, the step-like drain current induced by single electron trapping is measured. According to ΔI_d probability distribution and the time model, we can simulate the process of every single electron trapping. Finally the post-stress V_T distribution is found.

Fig. 2.3 showed the device structure in the following experiment, and the instrument setting is shown in Fig. 2.4. A two channel Agilent 8110 pulse generator connected to drain and gate electrode to simultaneously change the bias of each electrode, and the source electrode connected Agilent 4156 to measure the current. The trapped charge behavior in high-k dielectric is studied by “stress phase” and “recovery phase”, Fig. 2.5(a) and (b) illustrates a typical measurement result in stress phase, and the pulse pattern applied the gate and drain, respectively. A step-like drain current caused by single electron trapping is measured [2.2]. Similarly, the measurement result in recovery phase, and the pulse pattern applied are shown in Fig. 2.6(a) and (b). During the recovery phase, the phenomenon of trapped electrons discharge is observed [2.3-2.4]. The fast transient measure technique is proposed to minimize the switching delay time between stress and measurement, reduced the

amount of charge de-trapping in the delay time.

2.3 ΔI_d Distribution of PBTI

2.3.1 The Probability Function of ΔI_d in Recovery Phase

After a PBTI stress (1.8V 1sec), the recovery I_d exhibits a step-like evolution in a small device (W/L=0.08μm /0.03μm), and the ΔI_d amplitude is extracted as shown in Fig. 2.7, we defined the ΔI_d amplitude as following Eq. (2.1):

$$\Delta Id\ amplitude(\%) = {\Delta I_d}/{I_d(fresh)} \times 100\% \qquad \text{Eq. (2.1)}$$

In order to have an equitable standard of the statistic, the current fluctuation ΔI_d is normalized with I_d (Fresh) which measured before the device being stress.

According to the result illustrated in Fig. 2.8, the probability distribution exhibited an exponential function, which showed that the amplitude of the drain current recovery induced by single electron de-trapping obeyed percolation theory. An empirical formula had been studied as following [2.5]:

$$f(\Delta I_d) = \frac{1}{\sigma}\exp\left(-\frac{\Delta I_d}{\sigma}\right) \qquad \text{Eq. (2.2a)}$$

For convenience to observe the characteristic of the probability distribution, Fig. 2.8 is plotted in cumulative. In this case, Eq. (2.2a) should be integrated, Eq. (2.2b) showed the cumulative probability Function:

$$f(\Delta I_d) = \exp\left(-\frac{\Delta I_d}{\sigma}\right) \qquad \text{Eq. (2.2b)}$$

As the result of Eq. (2.2b), the slope of distribution showed in Fig.2.8 is -1/σ, a larger σ denoted the average ΔI_d induced by single electron is larger. From Fig. 2.7, we compared the devices with two different dimensions (W0.08μm/0.16μm L0.03μm), a dimensional dependence of σ is investigated, which a larger device demonstrated a smaller σ [2.5], this phenomenon also followed the percolation theory.

When the device area is large the dopant can regard as uniform distributed in the substrate, as the device scaled down, the random dopant induced surface potential non-uniformity caused a current-path percolation, which called the percolation theory [2.6]. Compared the two figures of Fig. 2.9(a) and (b), an occupied interface trap is located on a critical path in Fig. 2.9(a), which induced larger current fluctuation than the Fig. 2.9(b) one.

2.3.2 Comparison of the ΔI_d Distribution in Different Condition

Based on the same method in recovery phase, we extracted the ΔI_d amplitude in stress phase (stress1.3V 100sec), which illustrated in Fig. 2.10(a). Consequently, as the result showed in Fig. 2.10(b), ΔI_d distribution is consistent in stress and recovery phase, which implied it followed the same mechanism in these two phase.

In this section, we compared the ΔI_d distribution in different stress voltage, Fig. 2.11(a) and (b) displayed the comparison of different stress voltage in stress and recovery phase respectively. ΔI_d distribution exhibited independent with stress voltage neither in the stress and recovery phase.

2.3.4 The Difference of ΔI_d Distribution between Initial Trap and Stress Induced Trap

In previous section, we discussed the ΔI_d distribution with different stress voltage in stress and recovery phase. Currently, we compared the difference between initial trap and trap induced by PBTI stress. First, the ΔI_d distribution of RTN in a fresh device and the PBTI ΔI_d distribution are illustrated in Fig. 2.12(a), from Table. 2.1 the σ of PBTI is two times bigger than RTN in fresh device. Due to this phenomenon, we proposed an assumption. According to Fig. 2.12(b), on the random dopant region the surface potential is lower, which means the electron density is lower in this region. On the other hand, the electron density of the critical current path region is higher, it caused a higher probability of trap generation on the critical current path region. Hence, most of the stress induced trap located on the critical current path, it makes the σ of PBTI larger.

In Fig. 2.12(a), we also showed an evidence to support our assumption, the ΔI_d distribution of post-stress RTN is similar to the PBTI one, and demonstrated a larger σ compared with the fresh one. As the result, the reliability problem of the stress induced trap is more serious than the initial trap.

2.4 The Time Model in Stress and Recovery Phase

2.4.1 The Time Model in Stress Phase

V_T degradation can be measured in stress phase by the fast transient measurement. Average each step-like data, as shown in Fig. 2.13 the threshold voltage shift versus stress time follows a perfect time-power law of the form [2.7-2.9]:

$$\Delta V_T(t) \propto t^n \qquad \text{Eq. (2.3a)}$$

$$\log(\Delta V_T) \propto n\log(t) \qquad \text{Eq. (2.3b)}$$

Fig. 2.14 showed that parameter n~0.232 in Eq. (2.3b) is consistent in different stress voltage.

Since the trap density has a power-law relationship with time, and the number of electron trapped should be proportional to trap density, we record the time of each electron trapped as illustrated in Fig. 2.15(a). We found that the number of electron trapped followed the same roles with time as in Eq. (2.4):

$$\log(N) \propto n\log(t) \qquad \text{Eq. (2.4)}$$

Fig. 2.15(b) showed that the time dependence with number of electron trapped can be well explained by Eq. (2.4).

2.4.2 The Time Model in Recovery Phase

There are three possible paths for electron de-trapping as illustrated in the energy band diagram in Fig. 2.16, i.e. Frenkel-Poole (F-P) emission, thermally assisted tunneling (TAT) to gate electrode, and TAT to substrate [2.4]. Using the Arrhenius equation in Eq. (2.5):

$$E_a = R\frac{d\ln(\tau)}{d\left(1/T\right)} \qquad \text{Eq. (2.5)}$$

The extracted activation energy (E_a) is only 0.52eV as the result showed in Fig. 2.17. The tunneling path is ruled out, since the activation energy for F-P tunneling should

be equal to the trap energy (E_T), which is over 1eV. According to the electron emission time is proportional to the gate voltage, the tunneling path of TAT to gate can be excluded. TAT to substrate is the only reasonable explanation of the electron emission mechanism. Consequently, an analytical model of SRH-like thermally assisted tunneling is developed [2.4].

The analytical model of the tunneling mechanism can be displayed by the energy band diagram and trap distance in Fig. 2.18 [2.3-2.4]:

$$\tau^{-1} = \upsilon \exp\left(-\alpha_{ox} T_{ox}\right) \exp\left(-\alpha_k x\right) \qquad \text{Eq. (2.6)}$$

where

$$\upsilon = N_c \left(1 - f_c\right) \upsilon_{th} \sigma_0 \exp\left(-\frac{E_a}{kT}\right) \qquad \text{Eq. (2.6a)}$$

$$\alpha_{ox} = \frac{2\sqrt{2m_{ox}^{*} q\left(E_t + \Phi_B\right)}}{\hbar} \qquad \alpha_k = \frac{2\sqrt{2m_k^{*} q E_t}}{\hbar} \qquad \text{Eq. (2.6b)}$$

Eq. (2.6) reveals the nature of tunneling for trapped electron emission time, τ_i. The pre-factor υ, a lumped parameter referred to as the ”attempt-to-escape frequency” can be written as Eq. (2.6a), where N_C is the effective density-of-state in the Si conduction ban, $N_C(1-f_c)$ is the amount of available states in substrate for out-tunneling electrons from high-k traps, σ_0 and E_a are the cross-section and the activation energy.

According to the traps in the high-k layer can be recognized as a uniform distribution, the emission number increased with logarithmic time dependence as shown in Fig. 2.19.

2.5 Width Dependence in PBTI Recovery

In the previous result, the larger device exhibited a smaller σ, but as a result of Eq. (2.6), it showed that as the cross section of the device increased, the more electrons had de-trapping in the same recovery time, which showed in Table. 2.2. According to Fig. 2.20, the analytical model of electron de-trapping is available in different dimension of device.

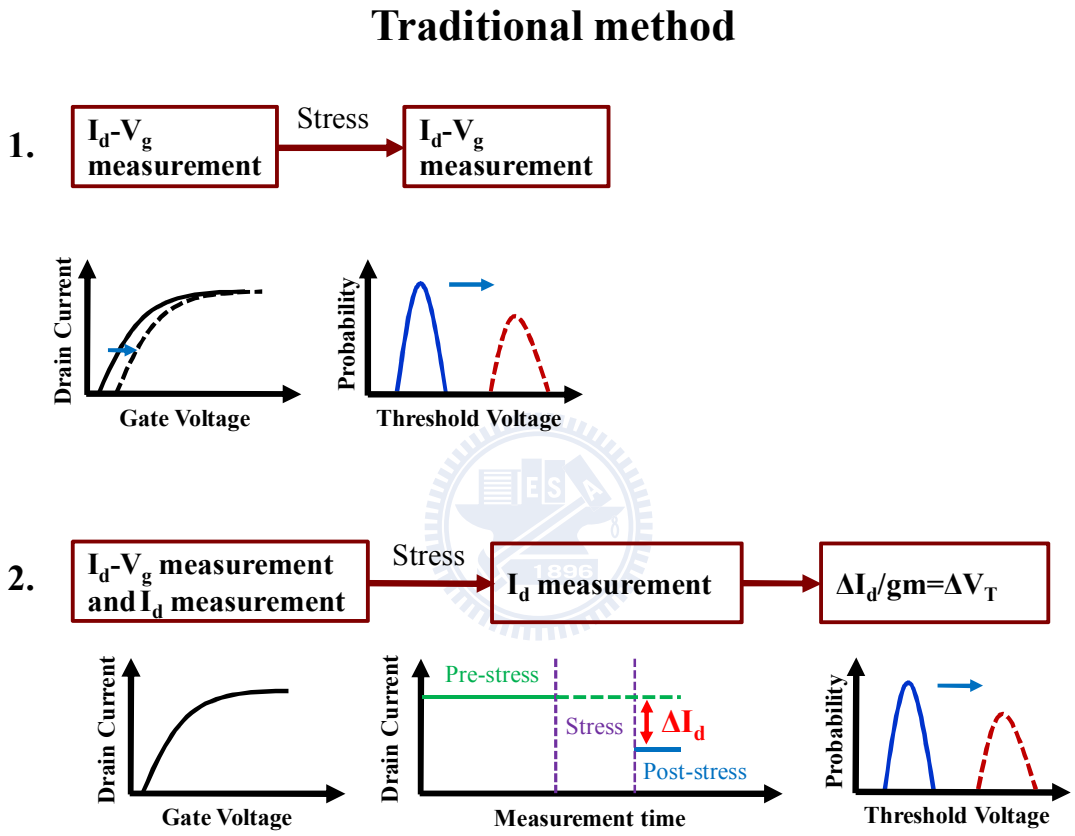

Fig. 2.1 Traditional method needs long measurement time and wastes lots of devices.

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Our method

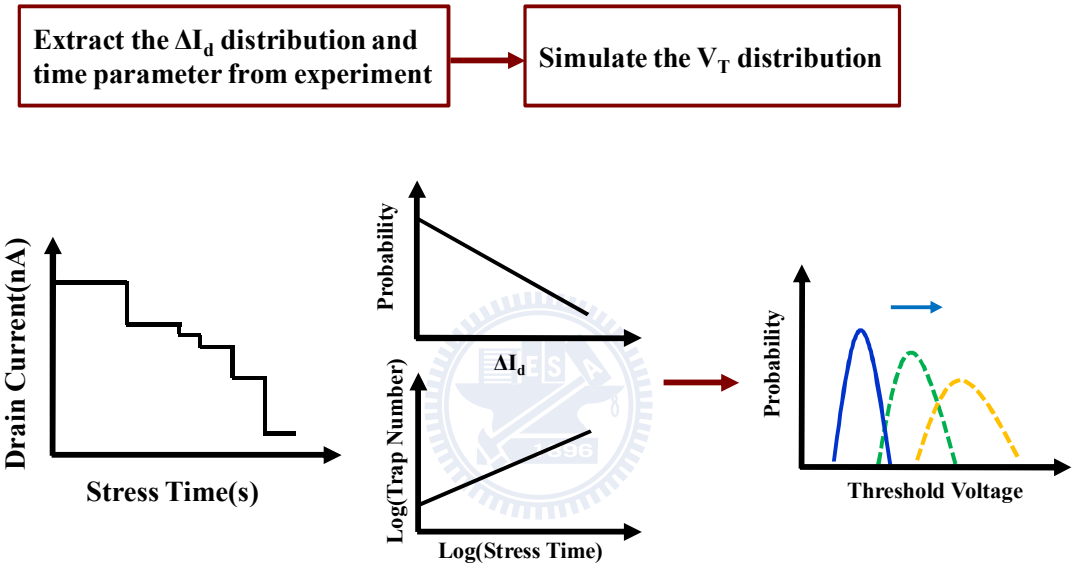


Fig. 2.2 Our method is based on characterizing the single charge phenomena, in order to simulate single electron trapped in PBTI.

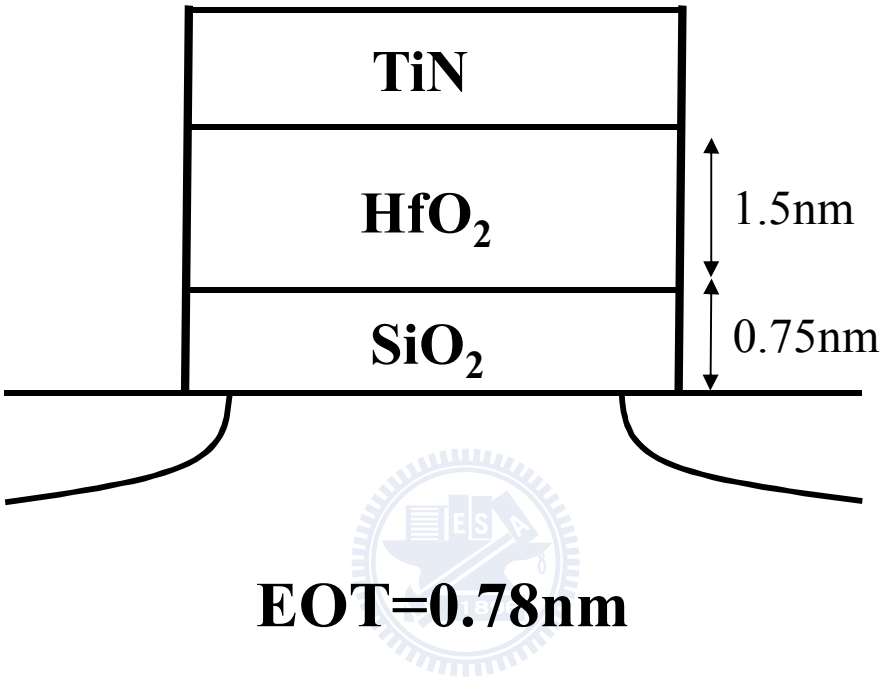


Fig. 2.3 The high-k/metal gate device structure used in the following experiment.

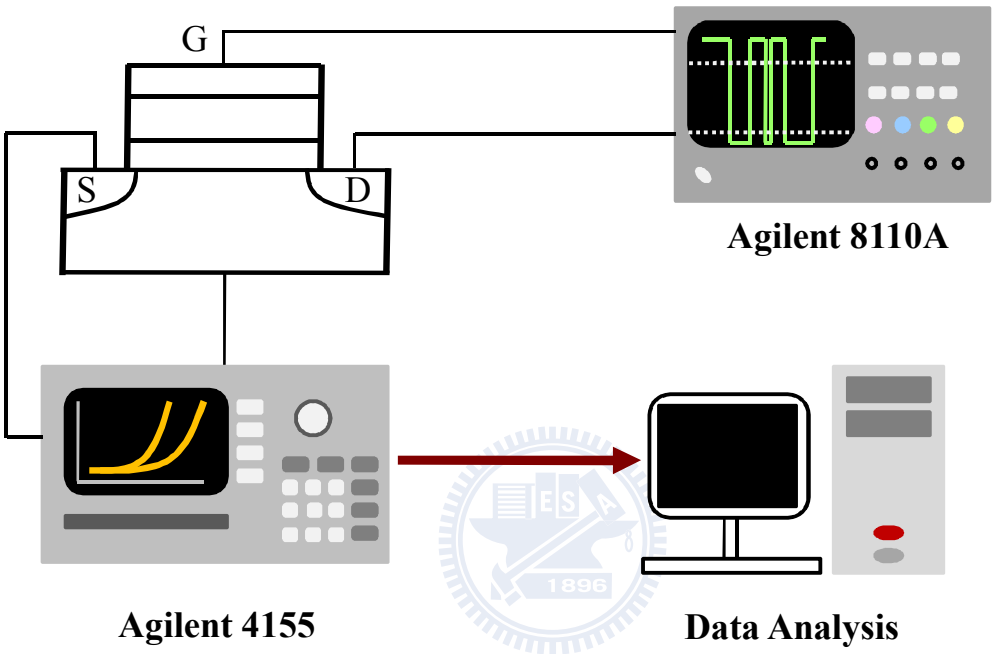


Fig. 2.4 The instrument setting in order to achieve the fast transient measurement.

Fig. 2.5(a)

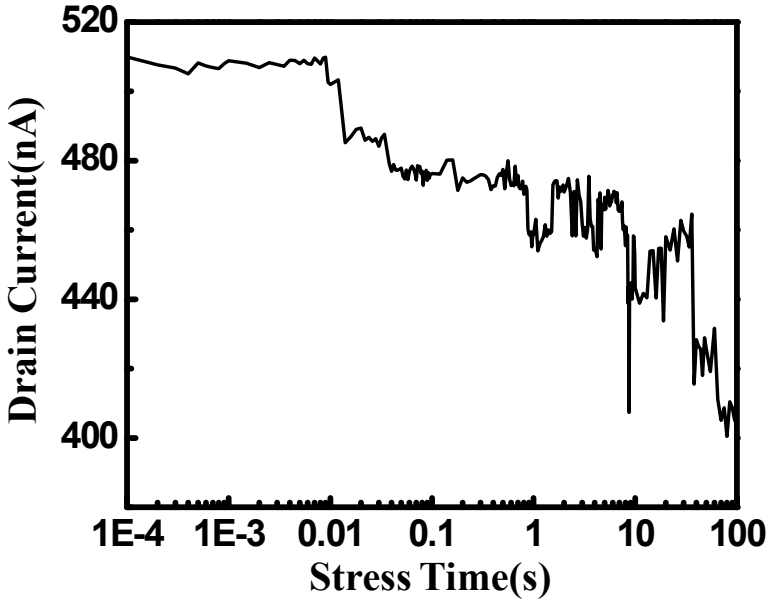


Fig. 2.5(b)

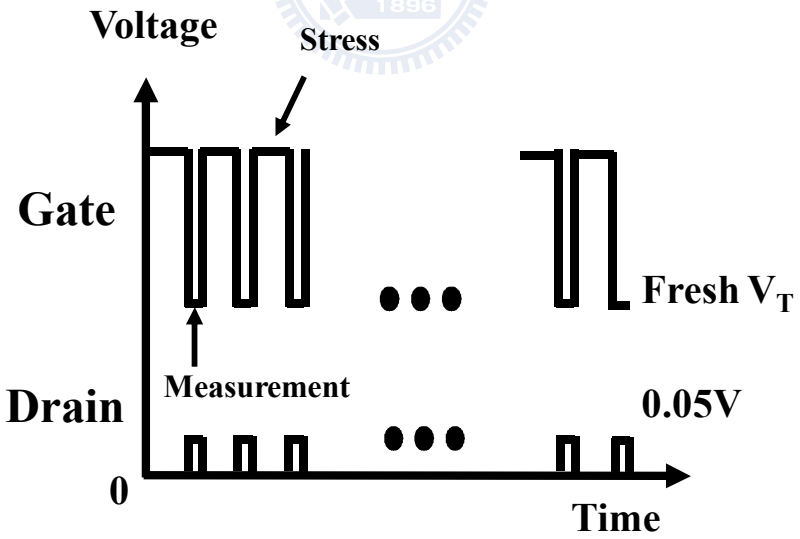


Fig. 2.5 (a) A typical pattern of I_d degrade in PBTI stress phase, which cause by single electron trapping.(b)Schematic of the constant voltage stress procedures.

Fig. 2.6(a)

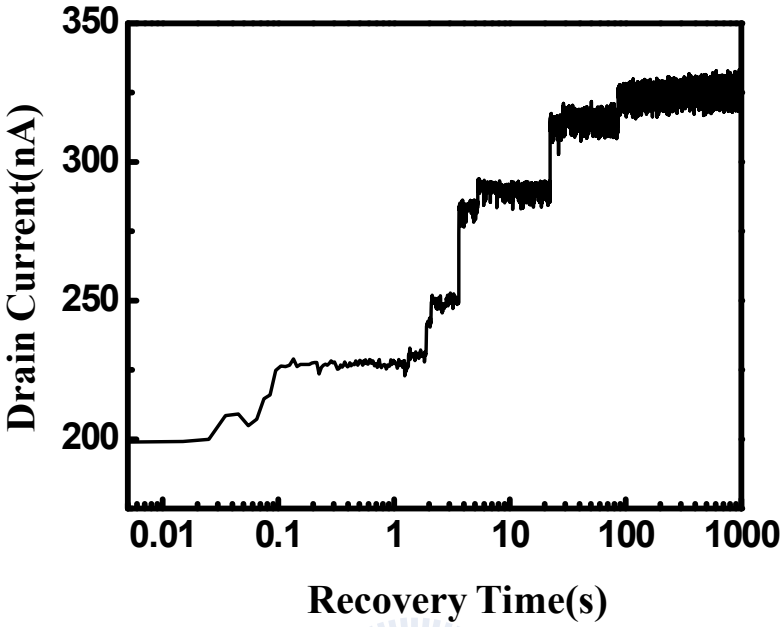


Fig. 2.6(b)

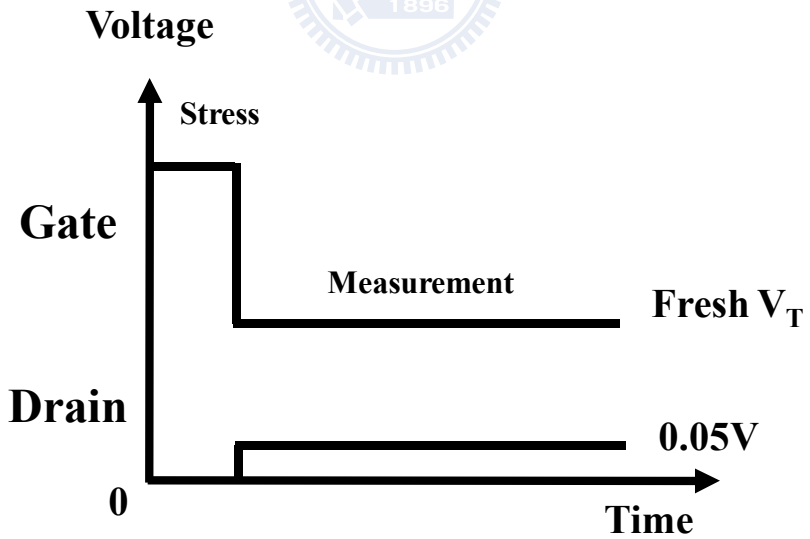


Fig. 2.6 (a) A typical pattern of I_d recovery in PBTI recovery phase, which cause by single electron de-trapping.(b)Waveforms applied to gate and drain during stress and measurement.

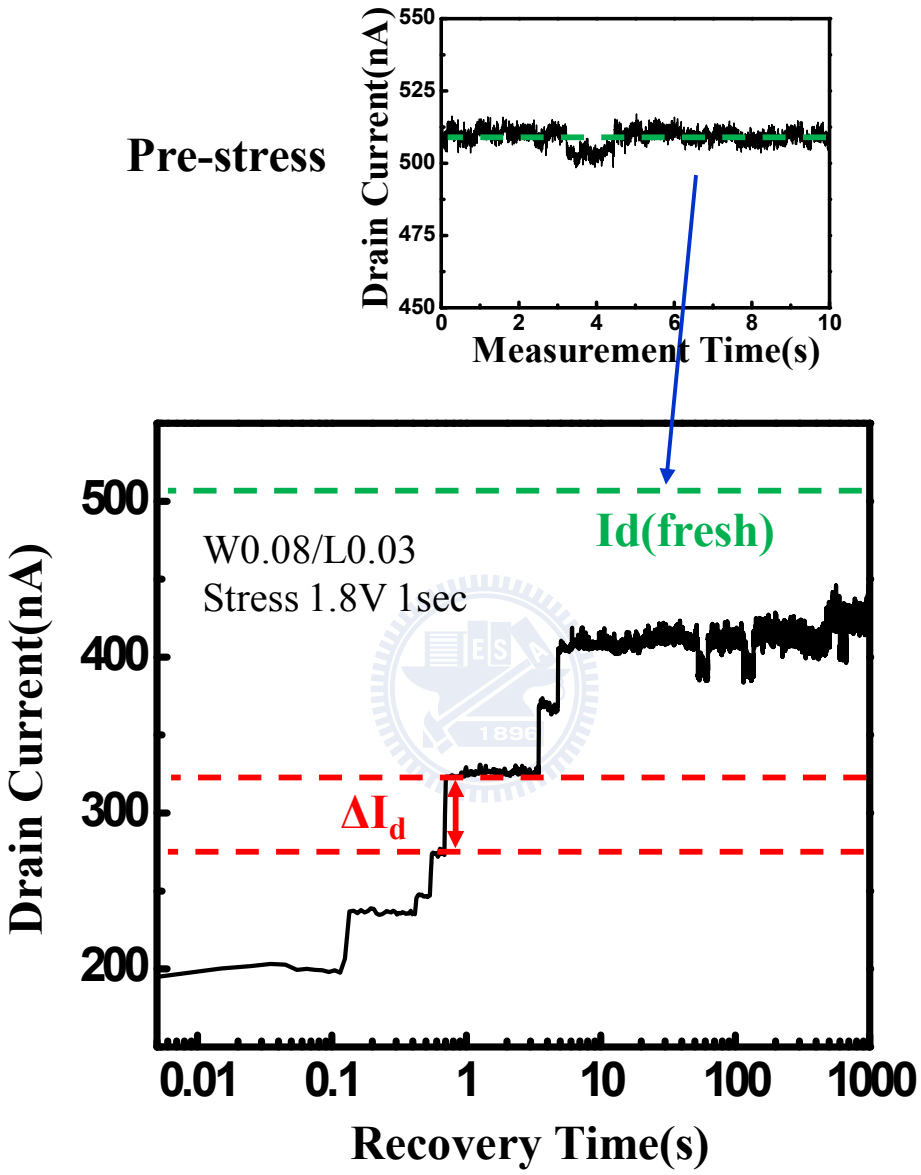


Fig. 2.7 To extract ΔI_d amplitude, we normalized ΔI_d with I_d(fresh) for the same criterion.

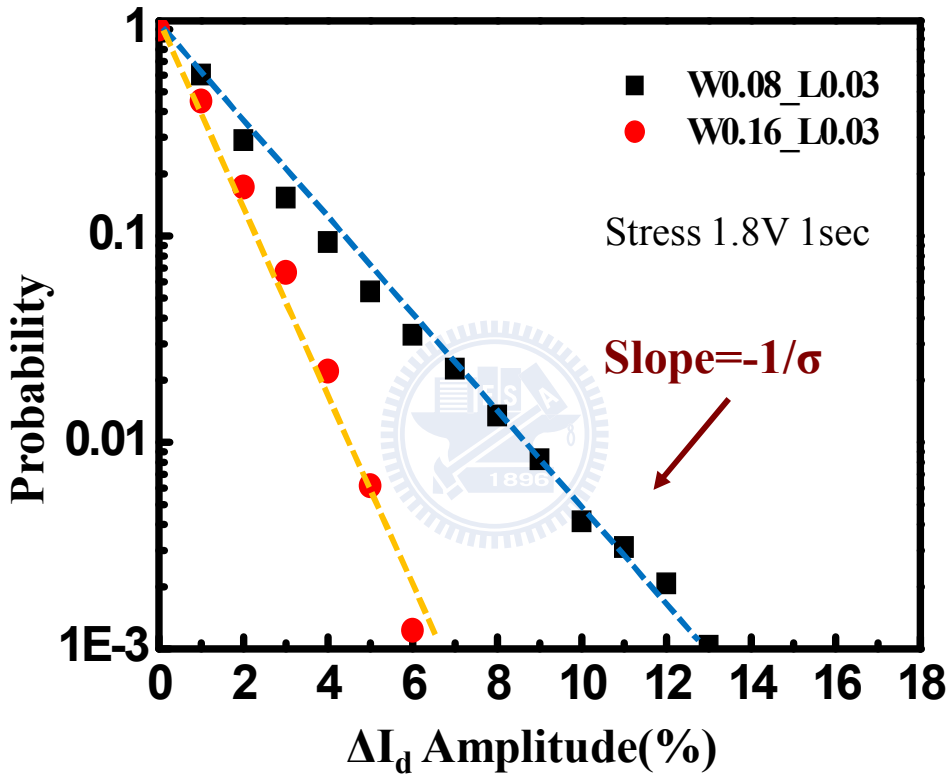


Fig. 2.8 The ΔI_d amplitude follows exponential distribution caused by percolation effect.

Fig. 2.9(a)

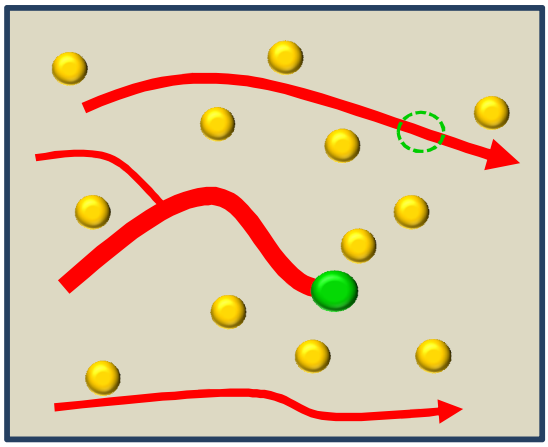
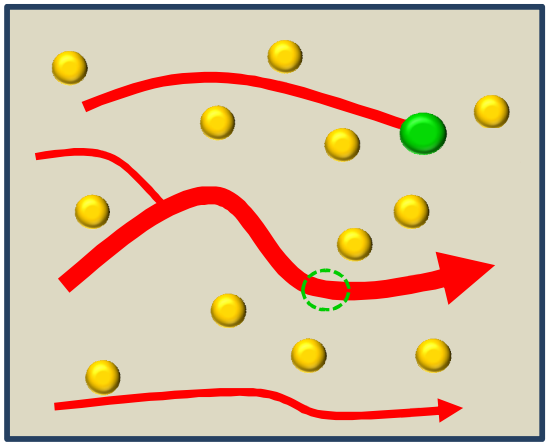


Fig. 2.9(b)



Random Dopant **Current Path**

Interface Trap Occupied by Electron **Empty Interface Trap**

Fig. 2.9(a) A interface trap located at critical path would make ΔI_d larger.(b) A interface trap located at a insignificant point make smaller ΔI_d.

Fig 2.10(a)

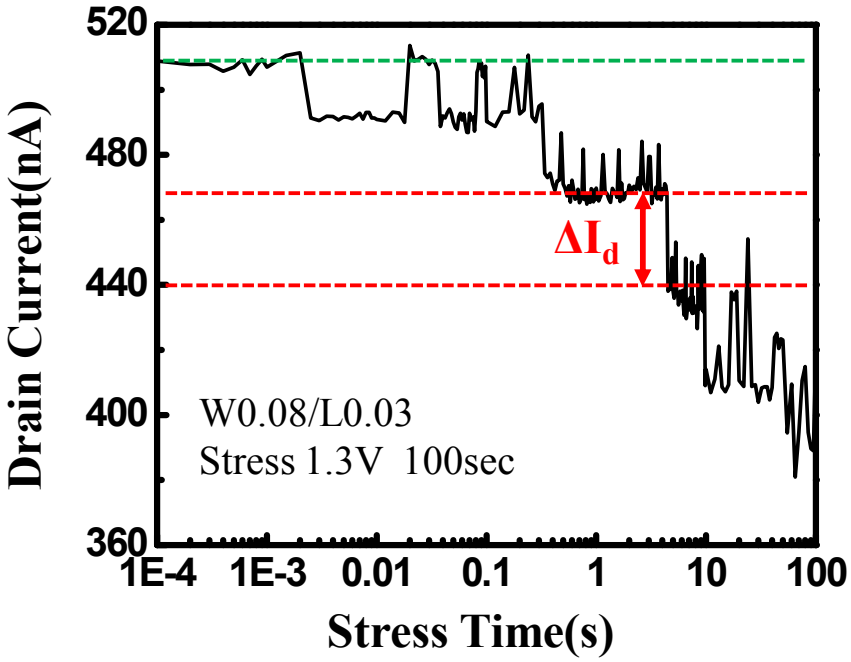


Fig 2.10(b)

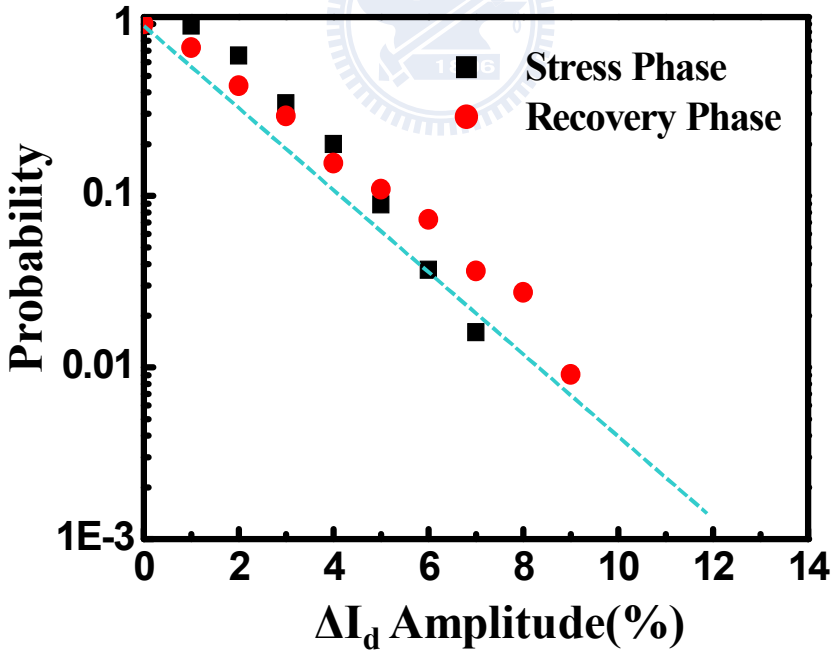


Fig. 2.10 (a) Similarly, ΔI_d amplitude in stress phase is extracted.(b) The ΔI_d distribution followed the same mechanism in stress and recovery phase.

Fig. 2.11(a)

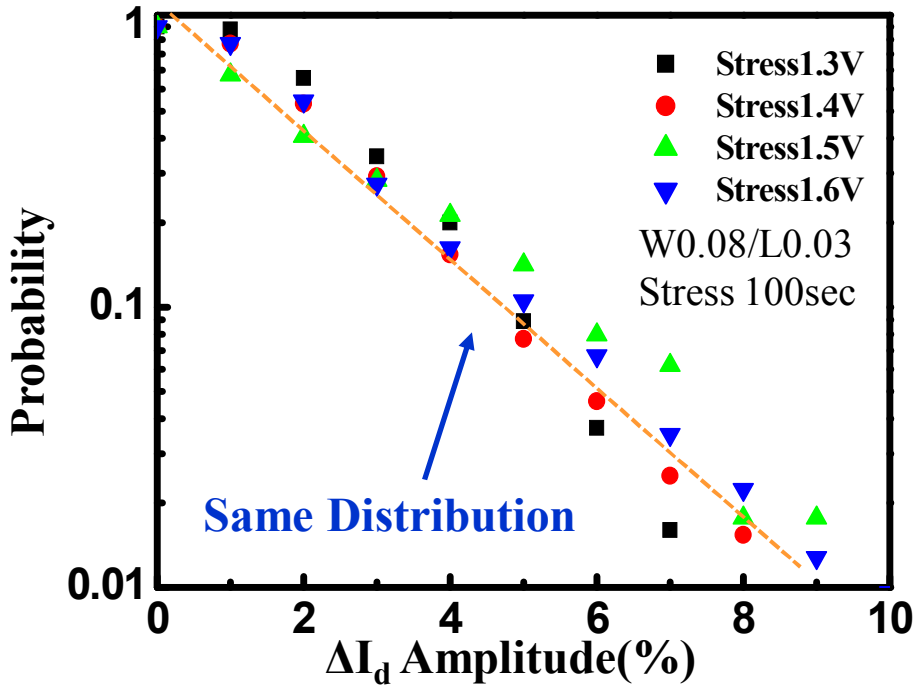


Fig. 2.11(b)

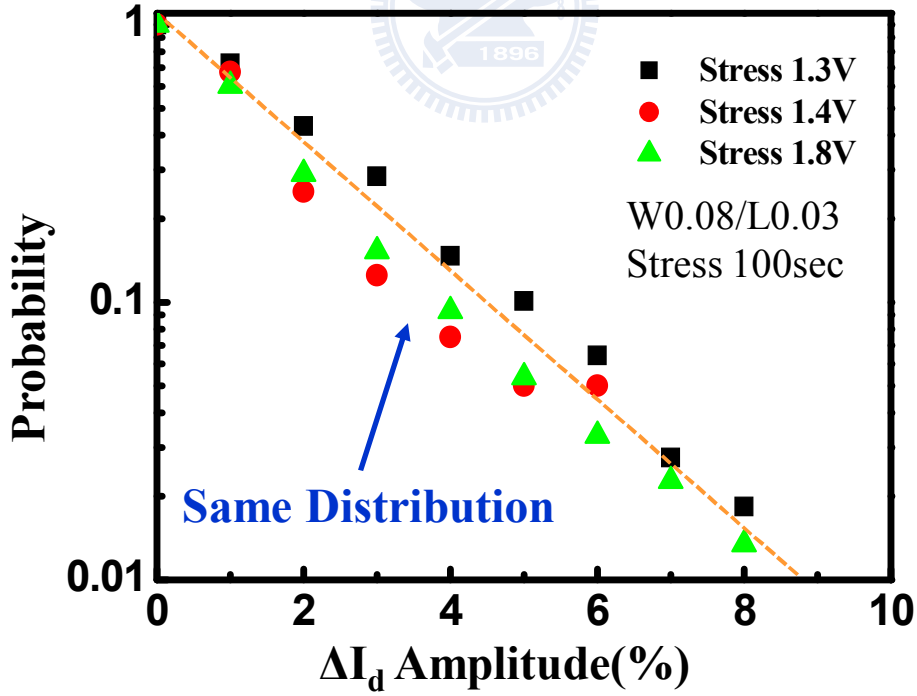


Fig. 2.11 The ΔI_d distribution had no stress voltage dependence in (a) stress and (b) recovery phase.

	σ
PBTI	1.846
RTN	0.724
Post stress RTN	1.479

Table. 2.1 The stress induced trap exhibited a larger σ.

Fig. 2.12(a)

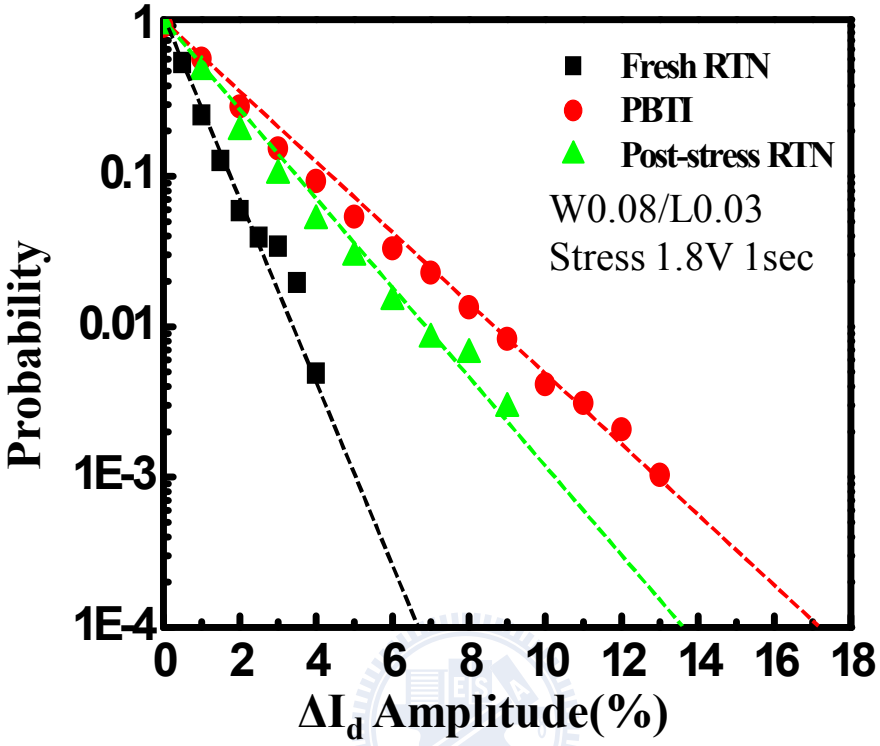


Fig. 2.12(b)

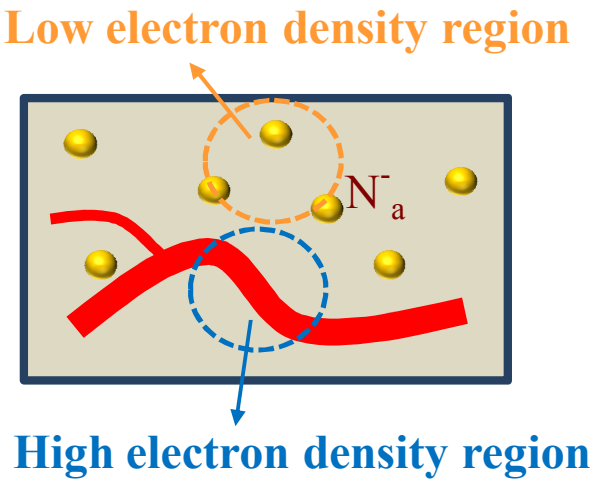


Fig. 2.12(a) The ΔI_d distribution of PBTI and post-stress RTN exhibited larger σ, which means the stress induced traps located on the critical current path.
(b) The higher probability of trap generation on the high electron density region.

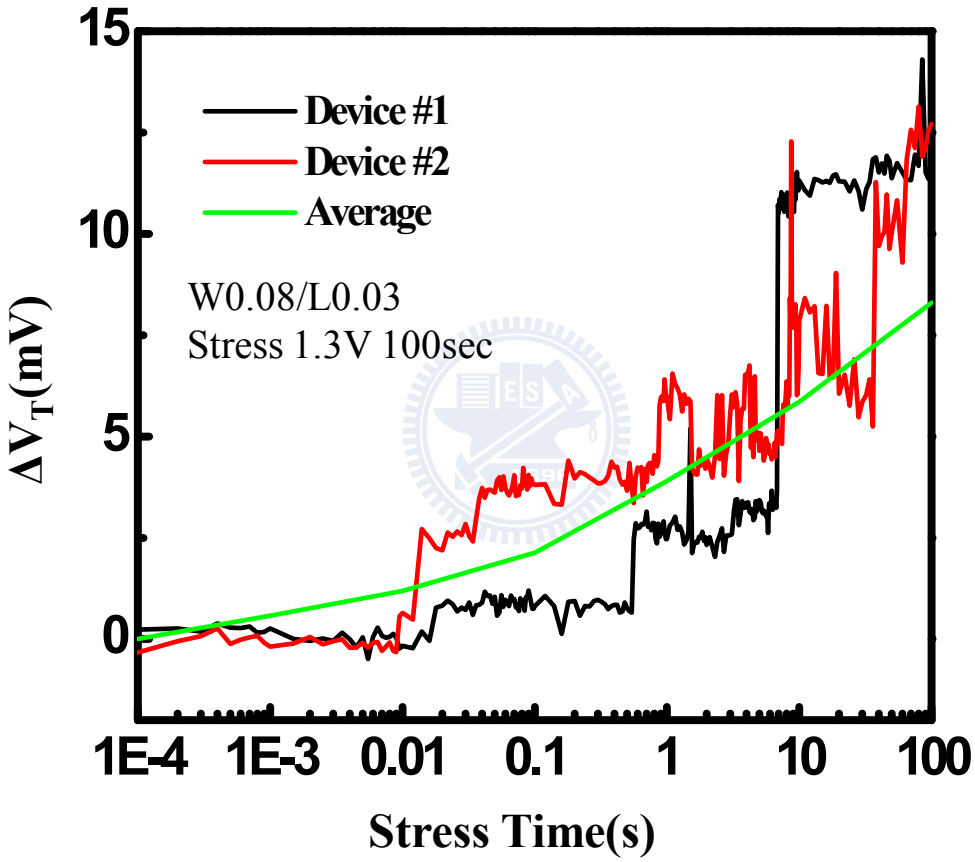


Fig. 2.13 Threshold voltage shift versus stress time followed power-law of a device stressed under high gate voltage.

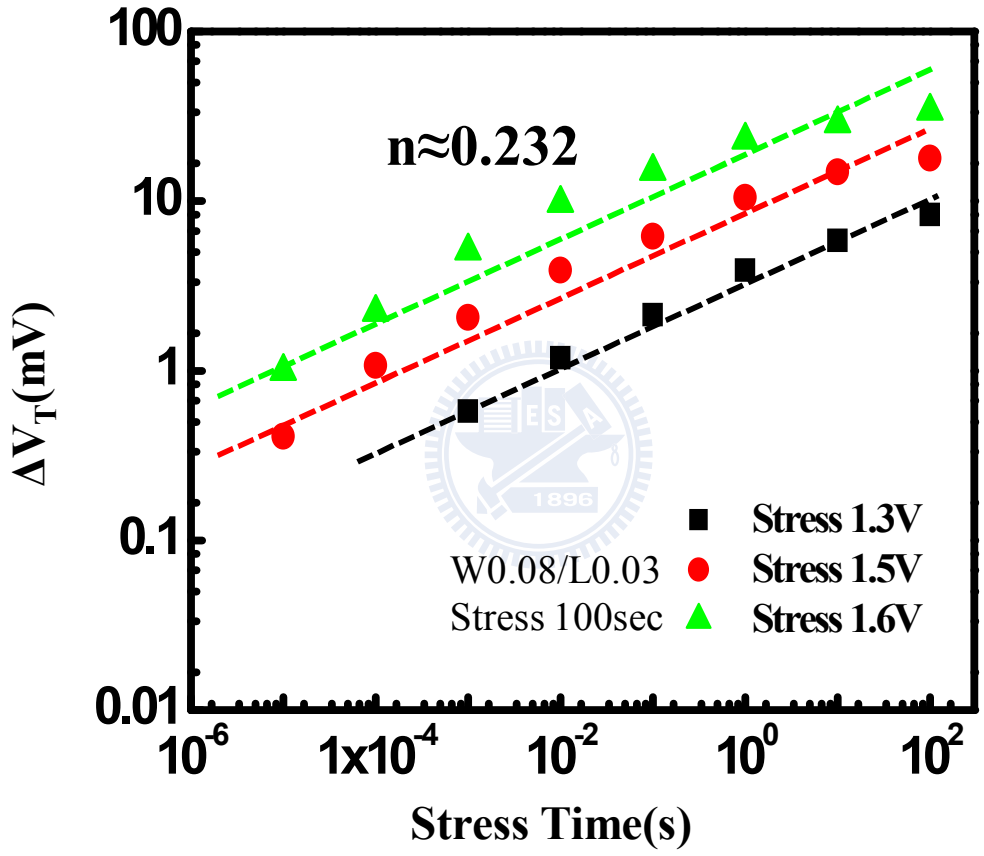


Fig. 2.14 The ΔV_T versus stress time characteristics under three different stress voltage.

Fig. 2.15(a)

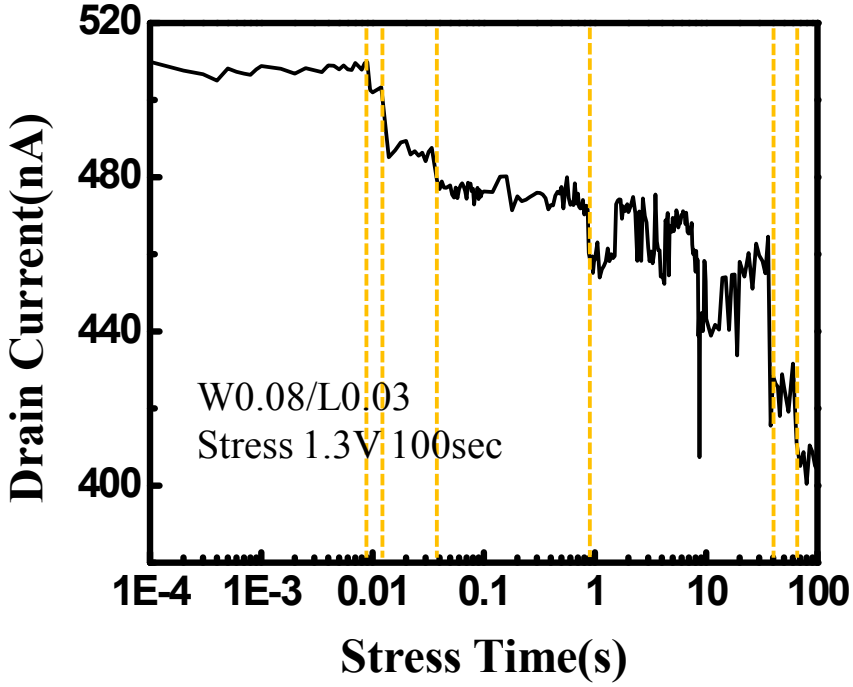


Fig. 2.15(b)

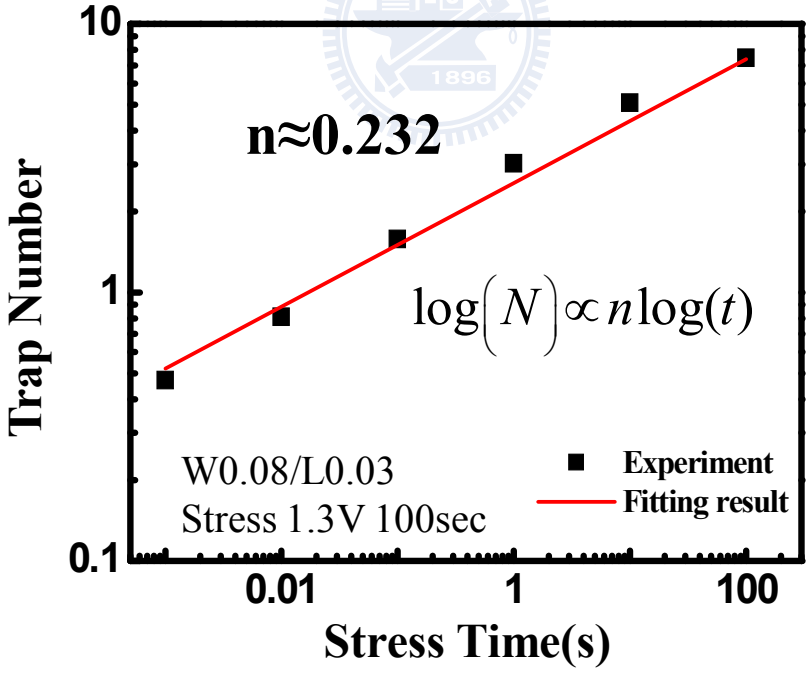


Fig. 2.15(a) We record the time of each electron trapped in the stress phase.
(b) The number of electron trapped versus stress time followed the same power-law.

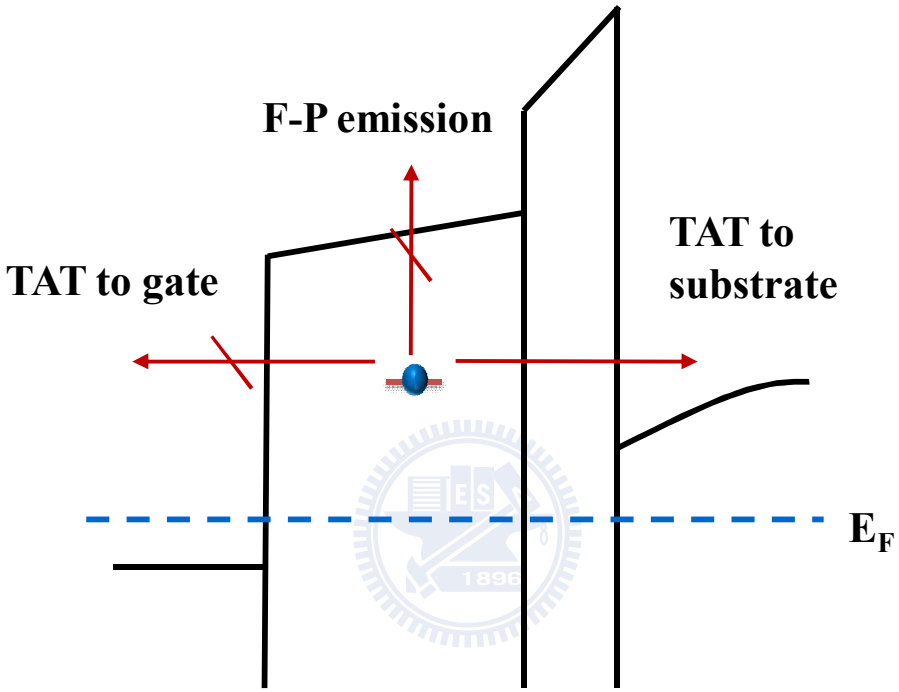


Fig. 2.16 Energy band diagram illustrating possible paths for trapped charge emission.

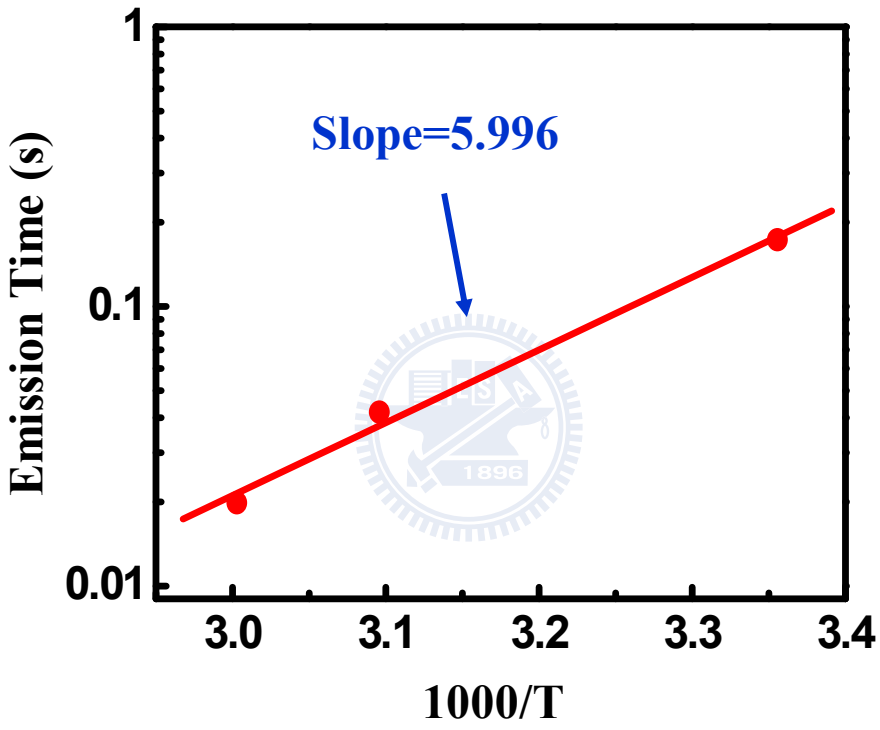


Fig. 2.17 Temperature dependence of emission time.

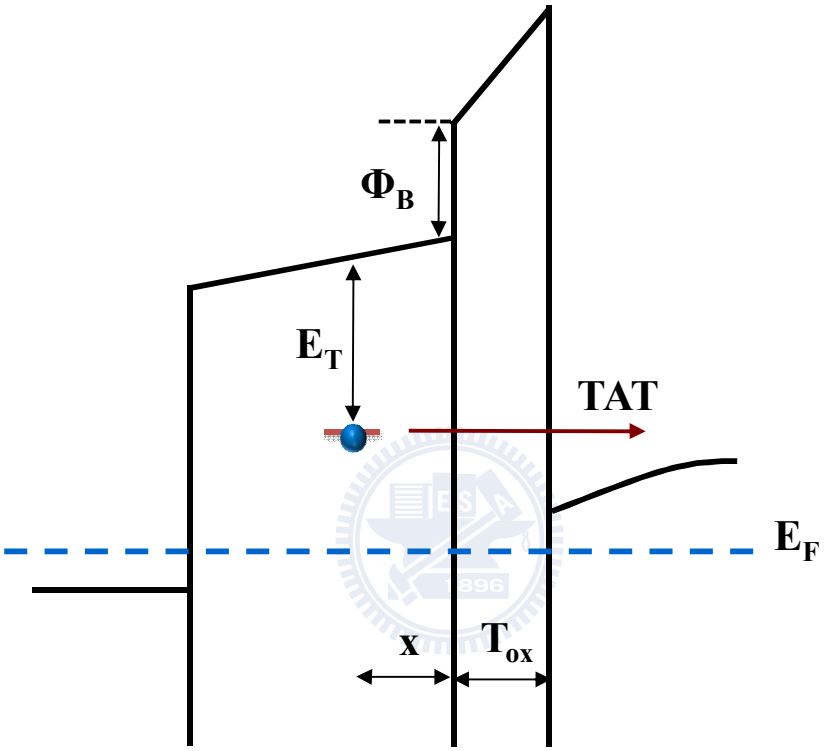


Fig. 2.18 Schematic representation of gate dielectric band diagram in recovery phase and trap positions, and the proposed model is described in detail in the text.

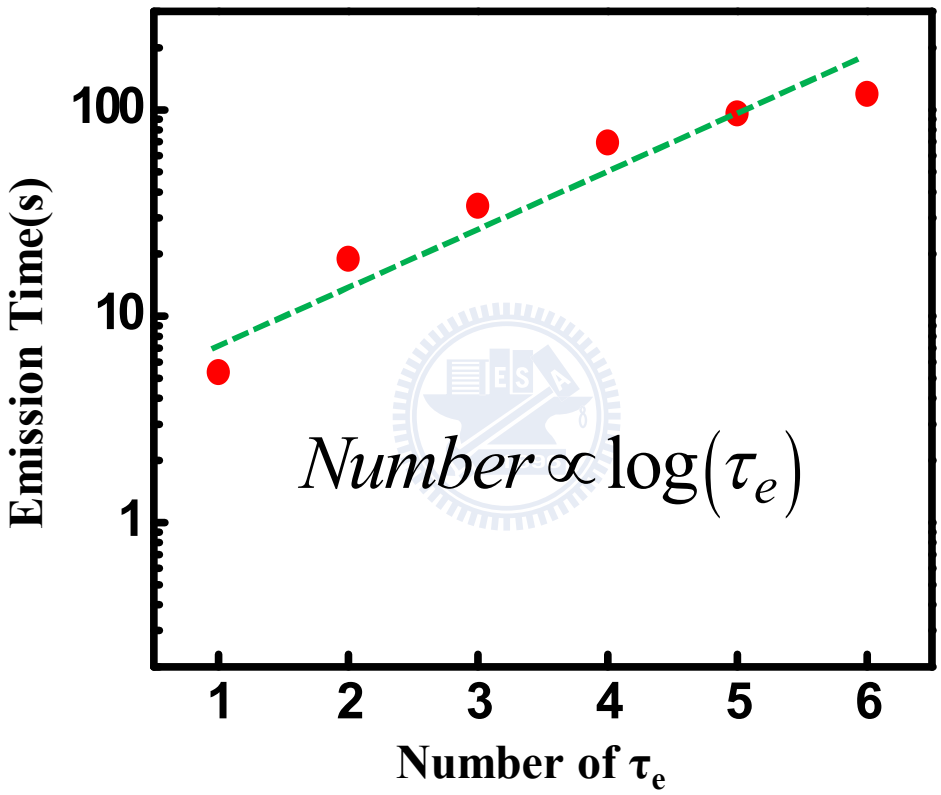


Fig. 2.19 The emission number with a logarithmic time dependence during recovery.

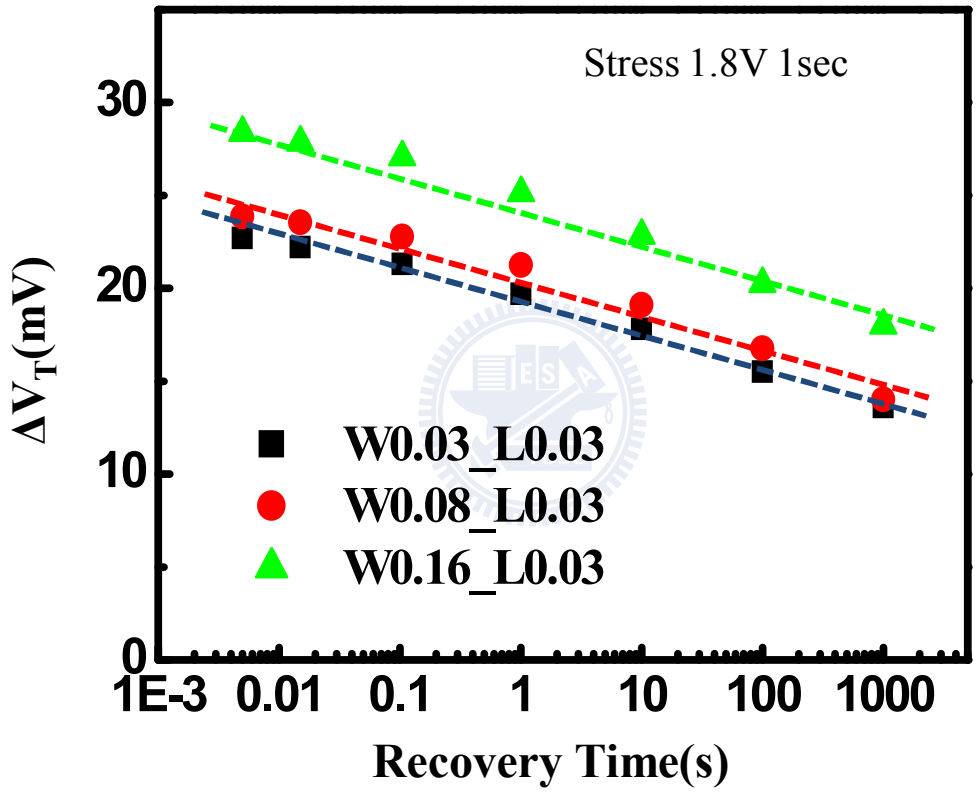


Fig. 2.20 NMOS recovery ΔV_T traces in different dimensional device.

Width	σ	Number of electron detrapping
0.03μm	1.963	10
0.08μm	1.846	12
0.16μm	1.411	17

Table. 2.2 A smaller device exhibited a larger σ, but when the cross-section increased more electrons are trapped in the same stress time.

Chapter 3
Monte Carlo Simulation of V_T Distribution in PBTI Stress

3.1 Introduction

Using the result of the ΔI_d distribution and the time model respectively in stress and recovery phase, we can simulate the V_T shift after each electron trapped or emission. Furthermore, the post-stress V_T distribution can also be predicted by our method, which is we can't obtain from the traditional method. Finally, the divination of device lifetime is displayed, moreover, the V_T distribution at lifetime is investigated.

3.2 Simulation Flow

The model of single electron trapping/de-trapping is constructed in chapter 2. In this section, the procedure of Monte Carlo is introduced. Fig. 3.1 displayed the flow chart of the simulation.

First, as the result showed in Fig. 3.2, the fresh threshold voltage distribution can be finely approach with a Gaussian distribution Eq. (3.1):

$$f(x;\mu,\sigma)=\frac{1}{\sigma\sqrt{2\pi}}\exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right) \qquad \text{Eq. (3.1)}$$

Second, from the ΔI_d distribution extracted in the experiment, we applied a random number y into the probability function to obtain the ΔI_d for each sample, moreover, integrated with the time model, the V_T degradation behavior in PBTI stress can be

simulated, as shown in Fig. 3.3(a) and (b) [3.1], respectively. Third, as the result in the last step, every sample had the correspondent ΔV_T. Repeat the second and third step, we can obtain the post-stress V_T distribution, and the V_T distribution after recovery is simulated in a similar way. Fig. 3.4 illustrated the final result of the V_T distribution of the devices (W/L=0.08μm/0.03μm) under a PBTI stress (1.8V 1sec), and after 1000sec recovery.

3.3 Simulation of Width Dependence in PBTI Stress

Since the ΔI_d distribution is extracted in previous chapter, as the result in Table. 3.1, the smallest device (W/L=0.03μm/0.03μm) exhibited a largest σ in these three different dimension devices, which means a single electron trapped in these devices induced more V_T shift. On the other hand, the σ of the largest device (W/L=0.016μm/0.03μm) is smallest, but there are more electrons trapped in the same stress time due to the larger cross-section of the device. Fig. 3.5 demonstrated the simulation result of these three different dimension devices under the 1.8V 1sec PBTI stress. According to the result showed in Table. 3.1, V_T shift is larger in the largest device, which means not only the σ but also the number of trapped electrons effected the amount V_T shift.

3.4 Simulation of Device Lifetime in PBTI Stress

Generally, we defined the device lifetime as the stress time that made the average V_T shifted 0.1V, Fig. 3.6 illustrated how do we estimated the device lifetime in the traditional method. Since the V_T distribution after each electron trapped can be

simulated, we proposed a new method to evaluate the device lifetime under a PBTI stress.

As shown in Fig.3.7 we can simulated the number of electron trapped that made the average threshold voltage shifted 0.1V. Consequently, the lifetime is calculated from the time model in the previous chapter. According to the experiment result, the ΔI_d distribution is consistent in the different PBTI stress voltage, we can derive the conclusion that the post-stress V_T distribution is the same at the device lifetime. Fig. 3.8 showed the corresponding V_T distribution with an average threshold voltage shifted 0.1V. Finally, we can predict the stress time which made the device reached a respective V_T variation from the time model of each stress voltage Eq. (3.2).

$$N = At^n \qquad \text{Eq. (3.2)}$$

As the result of Fig. 3.9, our method can perfectly estimate the device lifetime.

In the previous simulation we figure out the average device lifetime, although the average device lifetime exceed the 10 years line, there still have some devices couldn't bare with the stress condition, the following theme discussed about the lifetime distribution of every devices. First, we simulate how many electrons should be filled that makes each sample across the deadline (post stress V_T=0.464) as shown in Fig. 3.10, and Fig. 3.11(a) demonstrated the probability distribution of the number

of jumps needed in every samples, as the previous result the ΔI_d distribution is the same in different stress voltage, which means the probability distribution showed in Fig. 3.11(a) must be consistent in different stress voltage. Second, the number of jumps can be transformed to the device lifetime from the time model Eq. 3.2, the device lifetime distribution in stress voltage is shown in Fig. 3.11(b). Finally, the failure rate of the device in PBTI stress can be estimated, Fig. 3.12 demonstrated that in the stress voltage 1V condition, although the average device lifetime exceed the 10 years line, but there still have 9% devices failed.

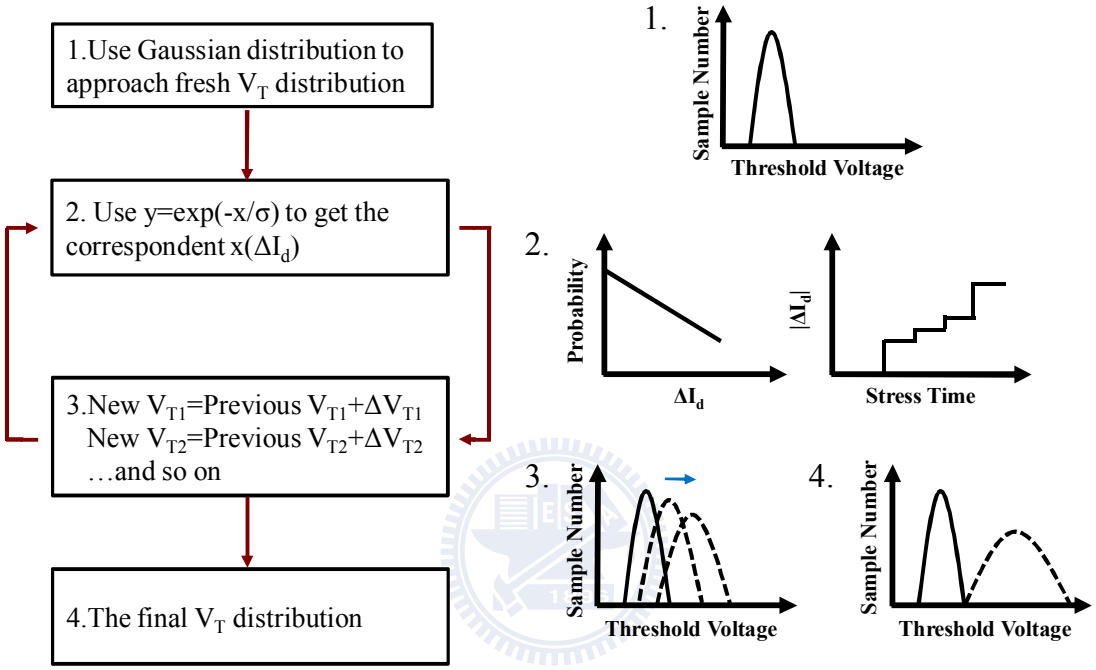


Fig. 3.1 Flow chart of Monte Carlo simulation for post-stress V_T distribution.

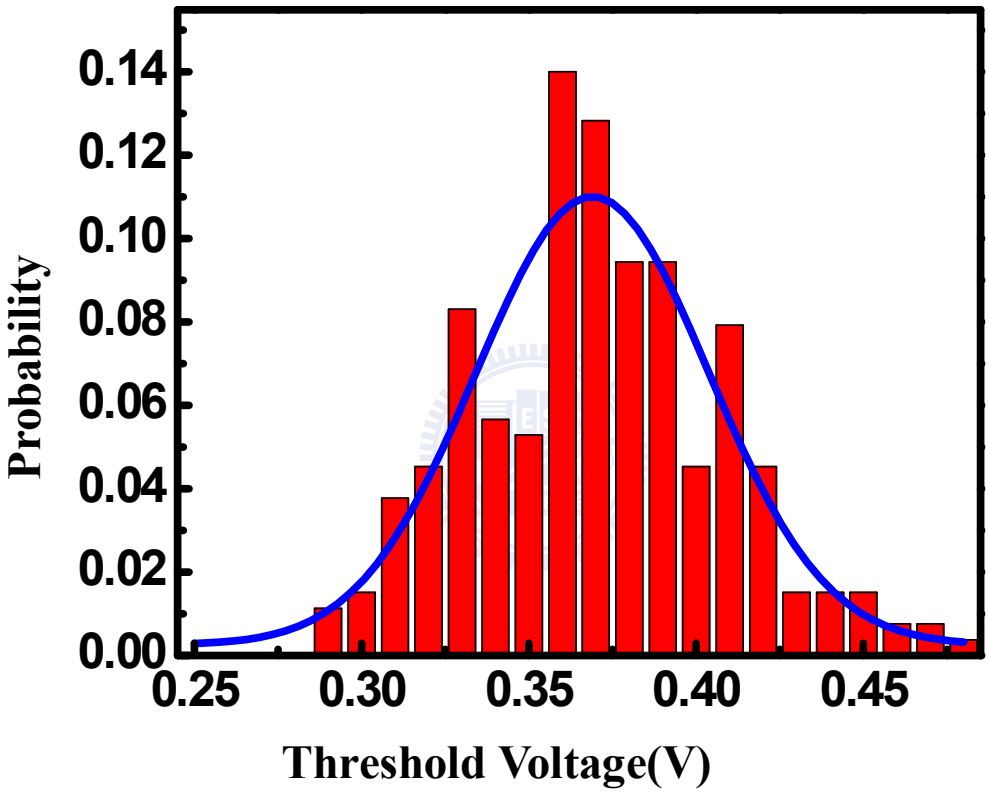


Fig. 3.2 Gaussian distribution approach is appropriate in this simulation.

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Fig. 3.3(a)

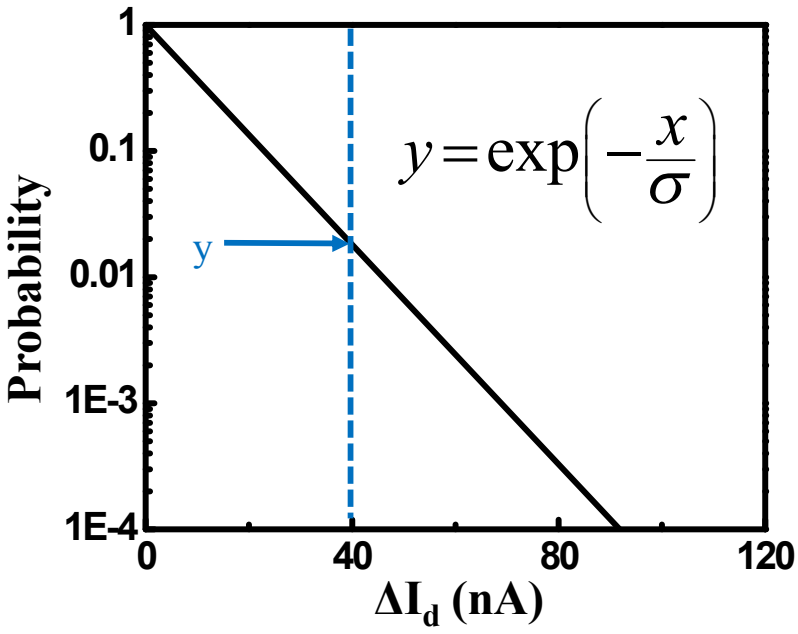

Fig. 3.3(b)

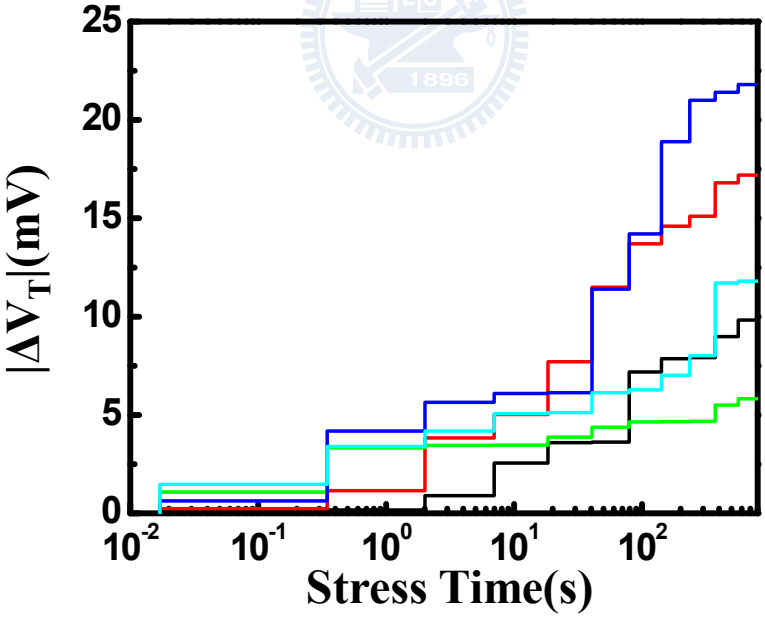

Fig. 3.3 (a) A random number y is applied to obtain the corresponding ΔI_d according to the ΔI_d distribution.(b) Using σ and the time model extract from experiment, we can simulate the step-like V_T variation.

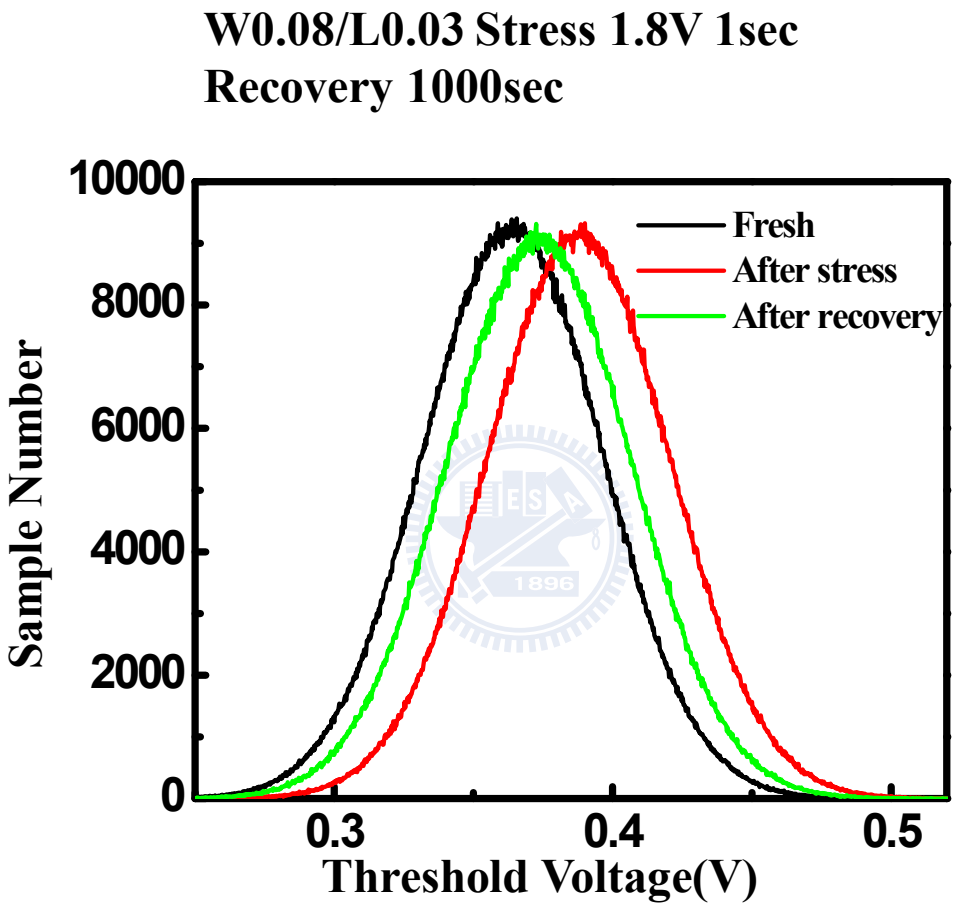

Fig. 3.4 The simulation of V_T distribution under a PBTI stress (1.8V 1sec) and after 1000sec recovery.

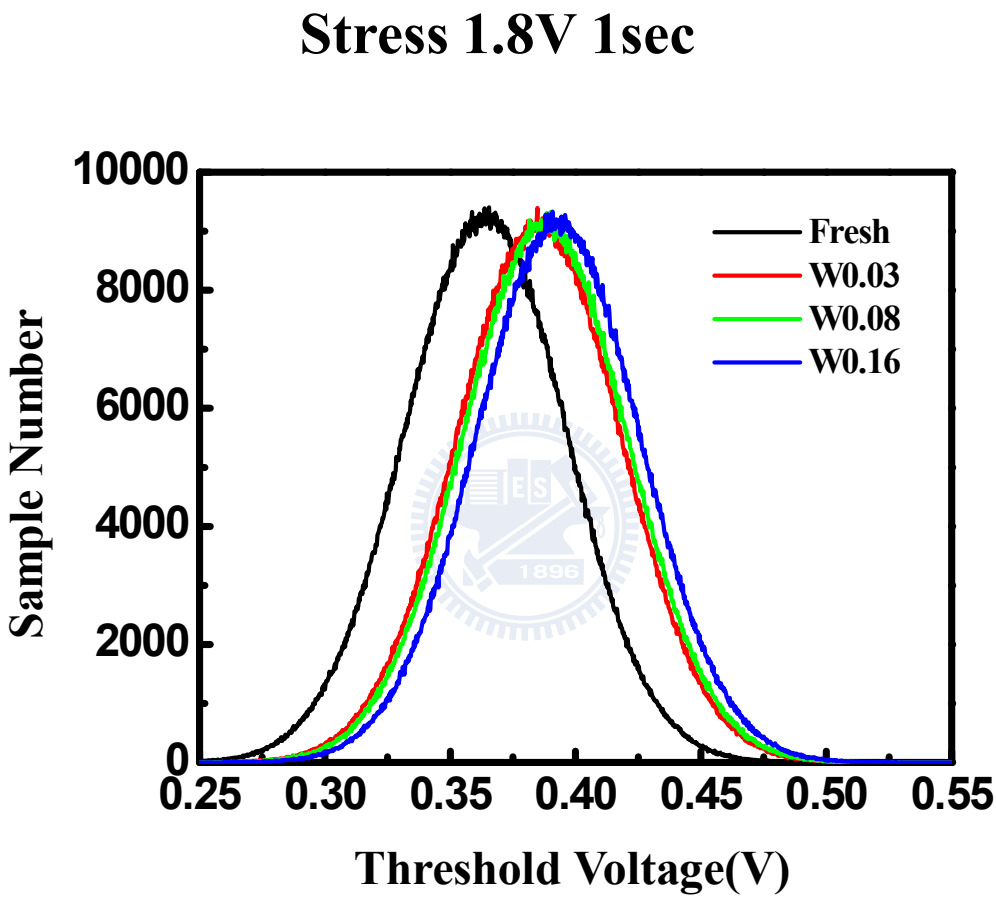

Fig. 3.5 Due to the result, larger device exhibits more threshold shift under the same stress condition, which because more electrons trapped.

Width	Average V_T (V)	σ	Number of trapped electron
0.03μm	0.38537	1.963	16
0.08μm	0.38765	1.846	20
0.16μm	0.39292	1.411	33

Table. 3.1 As the result, the variation of threshold voltage is concerned not only the σ but also the number of trapped electron.

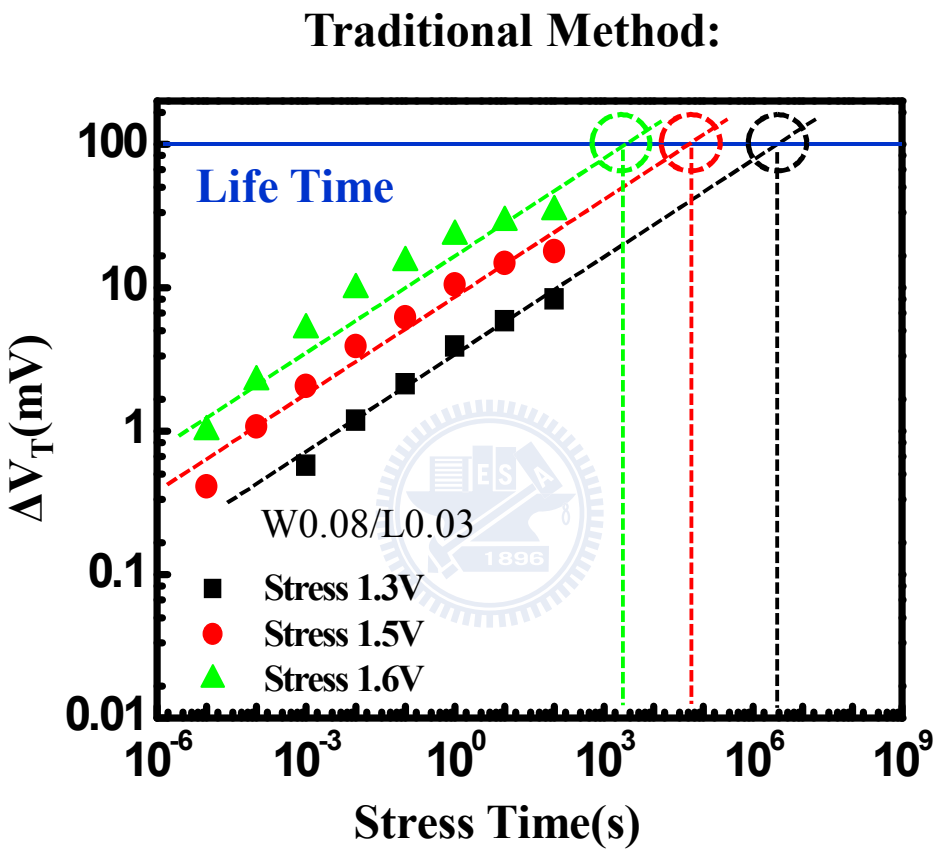

Fig. 3.6 The traditional method to estimate the device lifetime.

Our Method:

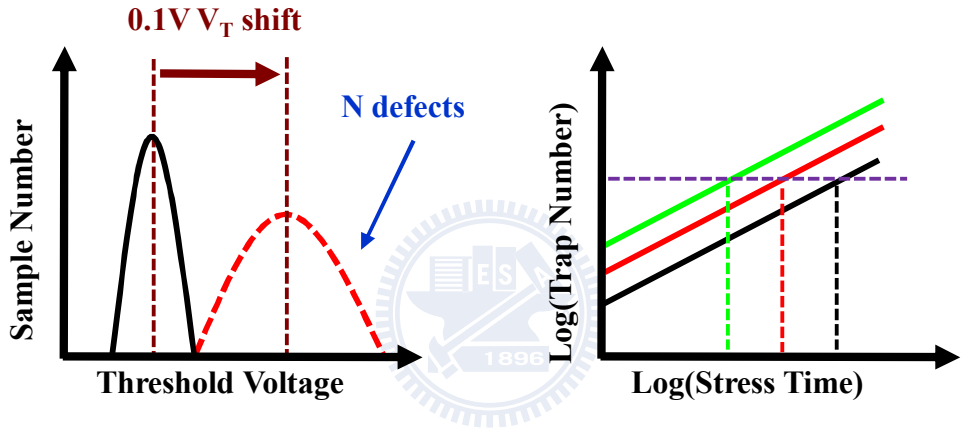

Fig. 3.7 Evaluate the device lifetime due to the simulation of post-stress threshold voltage distribution.

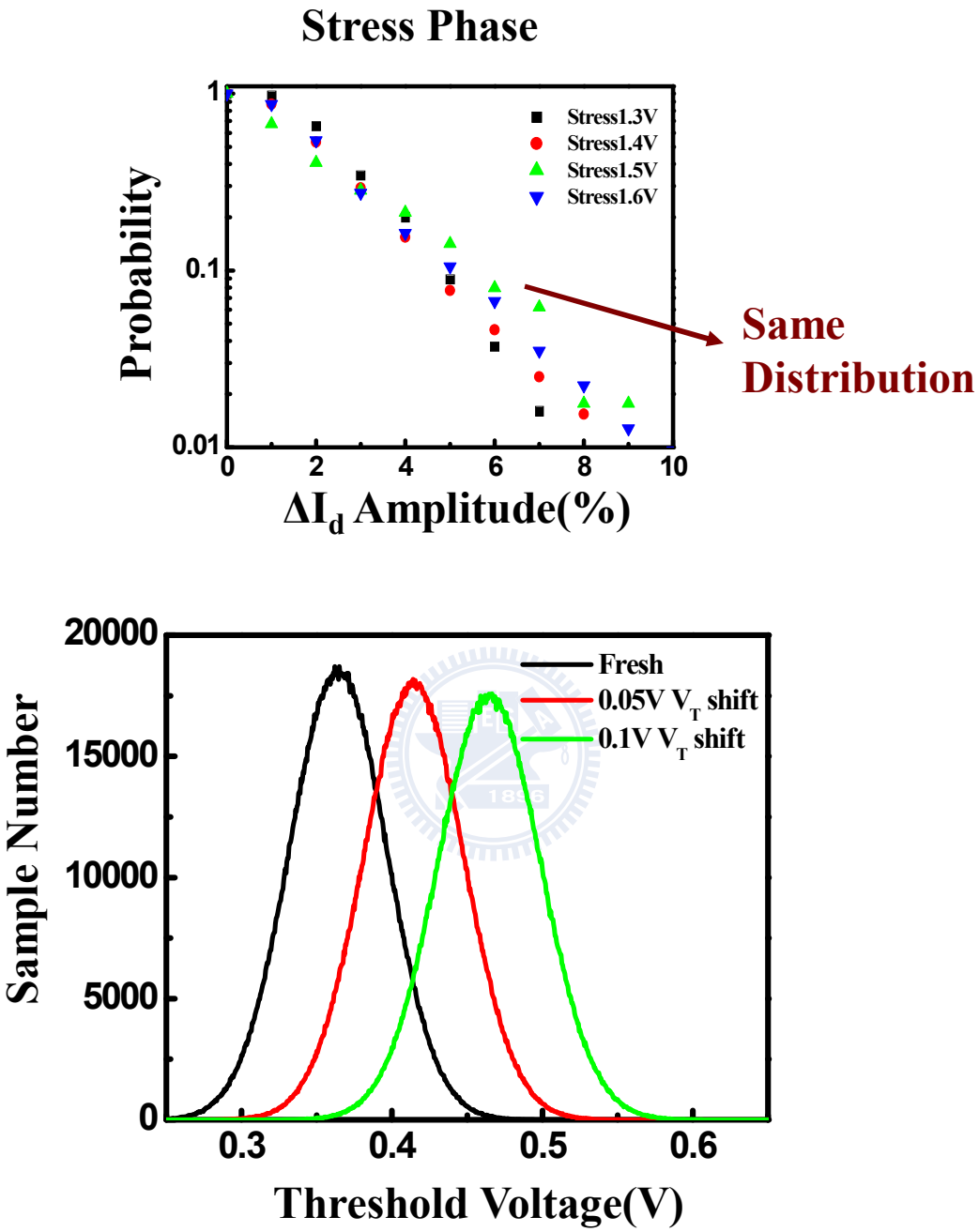

Fig. 3.8 According to the ΔI_d distribution is irrelevant to stress voltage, the post-stress VT distribution is consistent due to the same V_T variation.

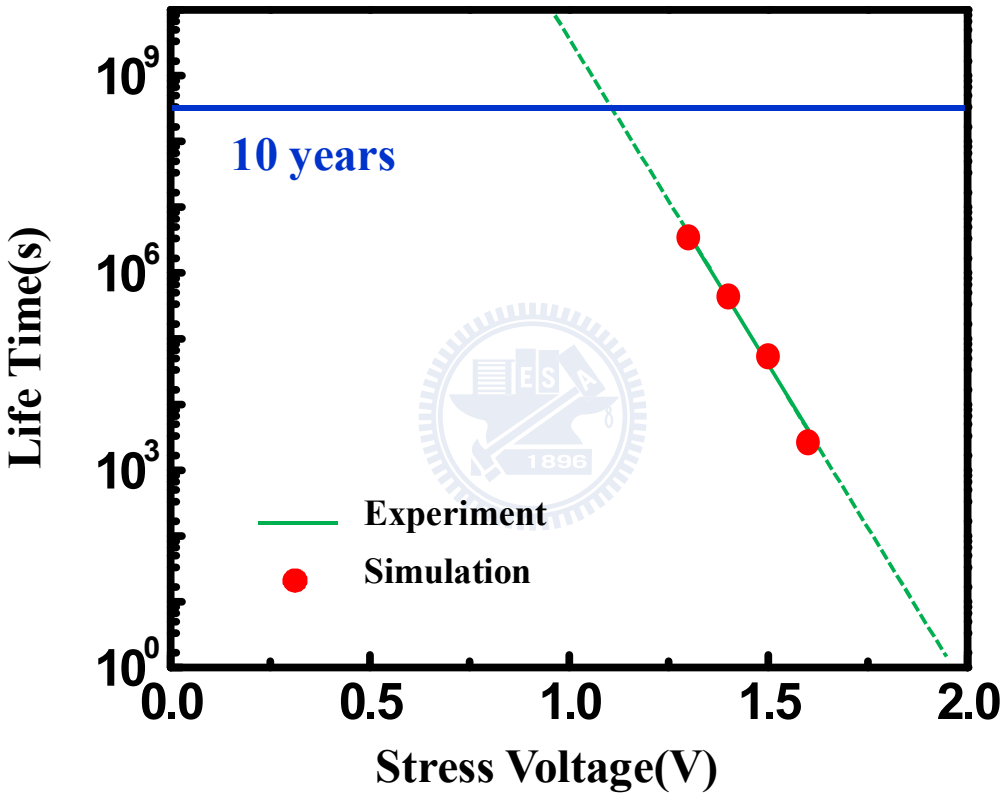

Fig. 3.9 As the result the device lifetime can perfectly estimate.

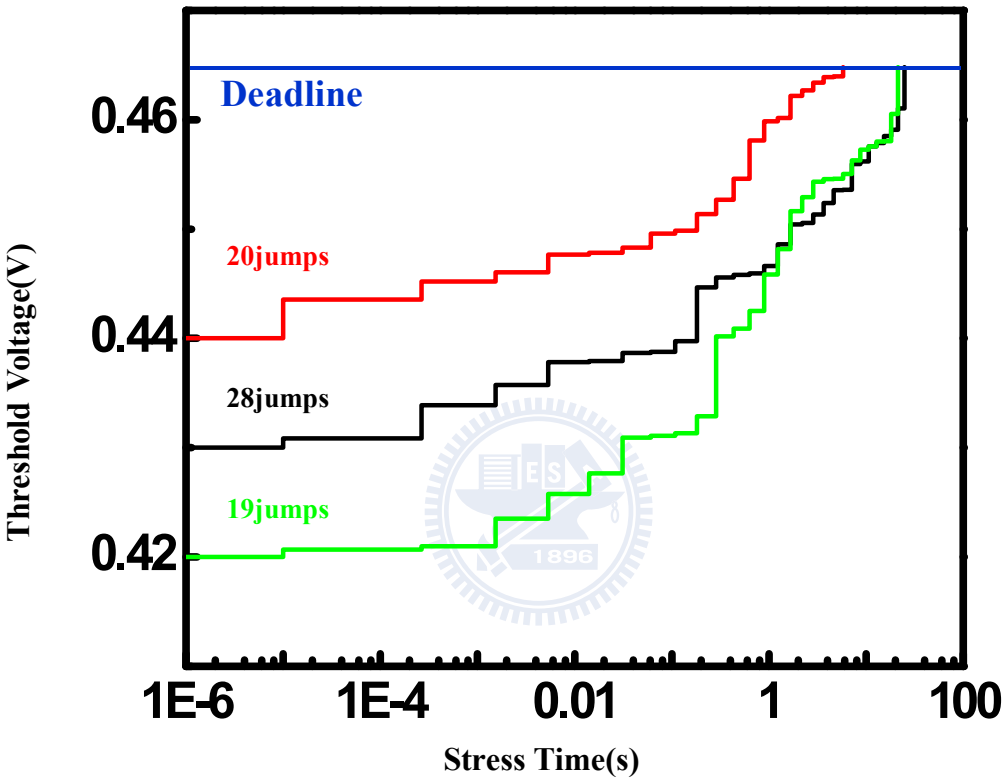

Fig. 3.10 The number of filled electron to make VT across deadline (0.464V) is different.

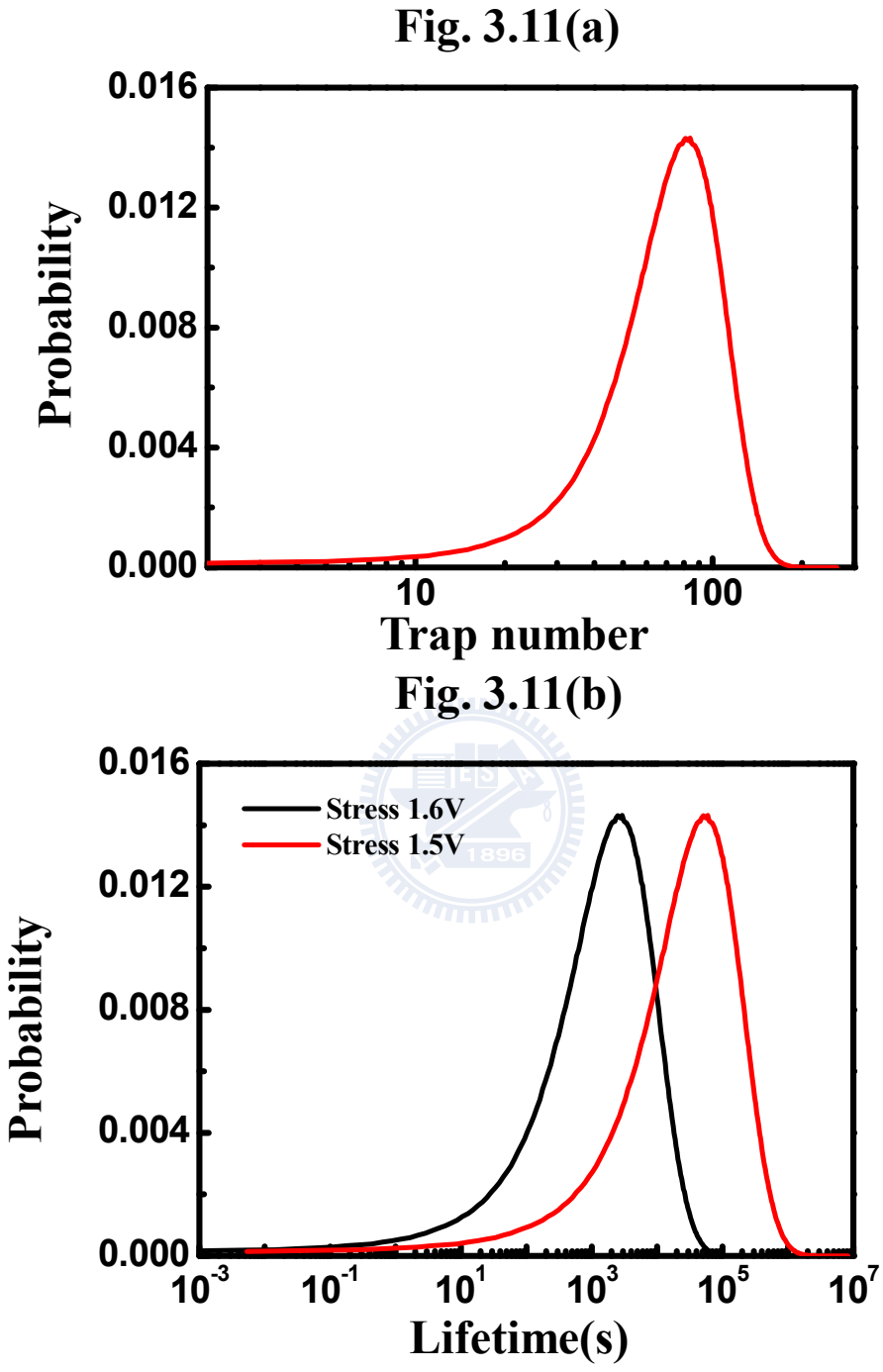

Fig. 3.11(a) The probability distribution of the trap number. (b) The lifetime distribution transformed from (a).

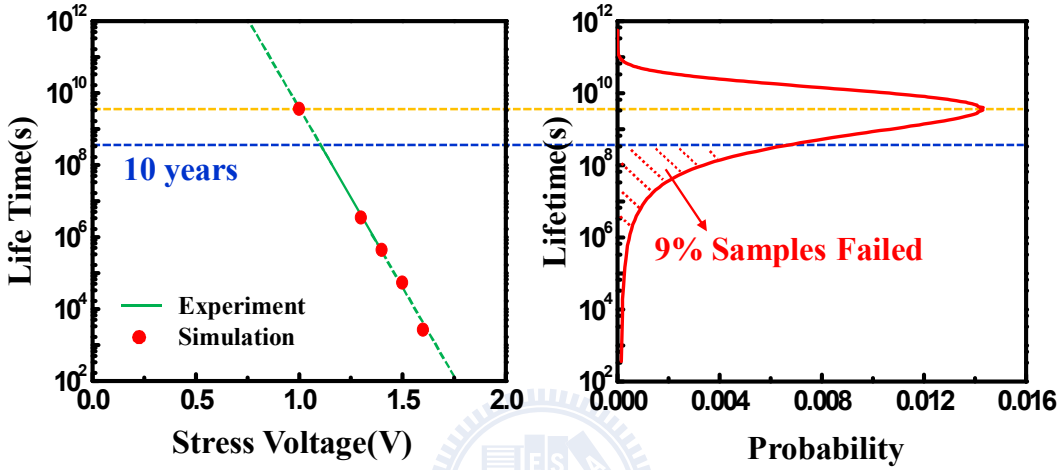

Fig. 3.12 From the lifetime distribution we can estimate the failure rate of the samples under the PBTI stress.

Chapter 4
Conclusion

Single Electron Phenomena in PBTI is characterizing in this work. We investigated the ΔI_d amplitude distribution followed the same mechanism in stress and recovery phase, which is irrelevant to the stress voltage. Consequently, the ΔI_d distribution of initial trap and stress induced trap is compared, as the result the stress induced trap caused more current fluctuation. On the other hand, based on the characterization in the stress and recovery phase, we derived the time model of PBTI. Also we observed that when device scales down, σ becomes larger but I_d degradation cause by PBTI stress is reduced, which because less traps.

According to the ΔI_d amplitude distribution and the time model obtained from the experiment, a Monte Carlo simulation of V_T distribution in PBTI is developed. Due to the simulation we obtained the post-stress V_T distribution, moreover, the device lifetime can be estimated. Since the ΔI_d distribution is independent with the stress voltage, V_T distribution is the same at device lifetime in different stress condition. The proposed method of simulate the post-stress V_T distribution is a powerful tool according to the PBTI induced reliability.

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Chapter 3

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碩士論文題目:

22 奈米高介電係數金屬閘極電晶體之正向偏壓溫度不穩定性分析及模擬

Positive Bias Temperature Instability(PBTI) Analysis and Simulation in 22 nm High-k Metal Gate nMOSFETs