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ScienceDirect
Microelectronic Engineering 84 (2007) 1801–1805
MICROELECTRONIC ENGINEERING
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Effects of capping layers on the electrical characteristics of nickel silicided junctions

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Available online 8 February 2007

Abstract

In this paper, effects of capping layers on formation and electrical properties of Ni-silicided junctions have been investigated. Nickel silicide films using the Ti or TiN-capped layer process are used to compare to those by the uncapped process. The uncapped (Ni single layer) and TiN-capped samples are shown to exhibit better thermal stability than the Ti-capped samples. For the silicided junctions, samples using Ti capping layer processes exhibit larger leakage current densities. A high-resistivity $Ni_xTi_ySi_z$ compound layer is formed on the surface during silicidation for the Ti-capped sample, while the uncapped and TiN-capped samples are not. In addition, it is found that the thickness of NiSi layer, as well as the $Ni_xTi_ySi_z$ layer, increases with increasing the Ti capping layer thickness. The formation of $Ni_xTi_ySi_z$ layer not only increases the contact resistance, but also deepens the silicide thickness.

Keywords: Nickel silicide; Capping layer; Junction diode

1. Introduction

The self-aligned silicidation (SALICIDE) process is one of the critical techniques for ultra large scale integrated (ULSI) circuits, and is more emphasized as the device dimensions become small towards sub-100 nm. By using this technology, the contact resistance of silicide-Si interface at poly-Si gate and source/drain regions will be decreased, thereby increasing the driving current and the transconductance (Gm) of the MOS device [1].

$TiSi_2$ is widely used as the silicide material for several years [2]. However, it has been found that the transformation of $TiSi_2$ from high-resistivity C49 phase to low-resistivity C54 phase is restricted by the linewidth, causing higher sheet resistance for lines narrower than 0.35 μm [3]. Neither $CoSi_2$ nor NiSi has such linewidth dependence effects as observed in $TiSi_2$ [4]. On the other hand, with the continuously decreasing junction depth, the silicide thickness is being shrunk to decrease silicon consumption at the expense of a higher sheet resistance [5,6]. For this reason, NiSi is being considered as a potential candidate for deep sub-100 nm devices because the same sheet resistance can be obtained with less Si consumption as compared to $CoSi_2$ [7–9].

Although NiSi have many merits, there are obstacles to be overcame such as large junction leakage current and thermal stability related degradation. In this work, the effects of the Ti or TiN-capped layers on formation of nickel silicide are demonstrated. The results of our study show that there is higher leakage current for NiSi sample with the Ti-capped layer than that of the uncapped sample. Further studies identified that the excess junction leakage current is due to the Ti–Ni–Si compound layer formed on the nickel silicide surface.

2. Experimental

The n^+–p junctions were formed by As^+ implantation at an energy of 20 keV with a dose of 5×10^{15} cm^{-2} followed

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doi:10.1016/j.mee.2007.01.198

by the rapid thermal annealing (RTA) process. After wafers were cleaned, they were introduced to a cluster sputtering system to deposit the metal films. Prior to the film deposition, Ar presputter cleaning was further carried out to remove the thin native oxide layer. Ni films of 20 nm and Ti or TiN films were sputtered, respectively. The thickness of Ti thin film was 10 or 30 nm, and the TiN thin film was 30 nm.

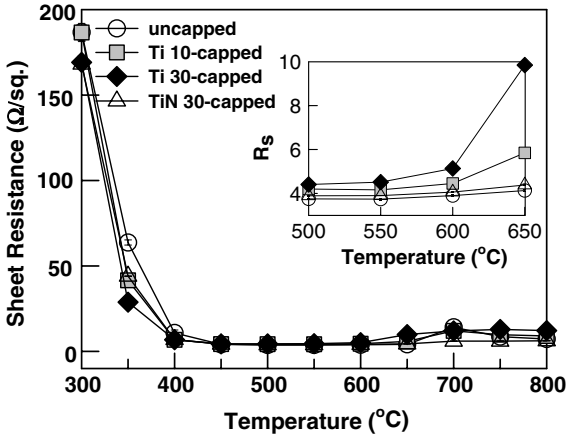

Fig. 1. Sheet resistance of NiSi using different capping layer processes as a function of annealing temperature.

After deposition of metal films, nickel silicidation was done in a RTA (AG 610) system, followed by a $H_2SO_4 + H_2O_2$ mixture to selectively remove the unreacted metal. Finally, TiN/AlSiCu/TiN was deposited and patterned as the metal pad. For easy identification, the uncapped silicide sample, Ti 10 nm-capped silicide sample, Ti 30 nm-capped silicide sample, and TiN 30 nm-capped silicide sample are denoted herein as uncapped, Ti 10-capped, Ti 30-capped, and TiN 30-capped, respectively.

The leakage currents of junction diodes were determined at a reverse bias of 5 V by a HP4156 semiconductor parameter analyzer. For the unpatterned sample, sheet resistance of the silicide film was measured by a four-point probe. Microstructures of the silicide films and interfaces were examined using transmission electron microscopy (TEM). The compositions and the phase identification of silicide films were carried out by energy dispersive spectroscopy (EDS) and X-ray diffraction (XRD) analysis, respectively. Compositional depth profiles were characterized by secondary ion mass spectroscopy (SIMS).

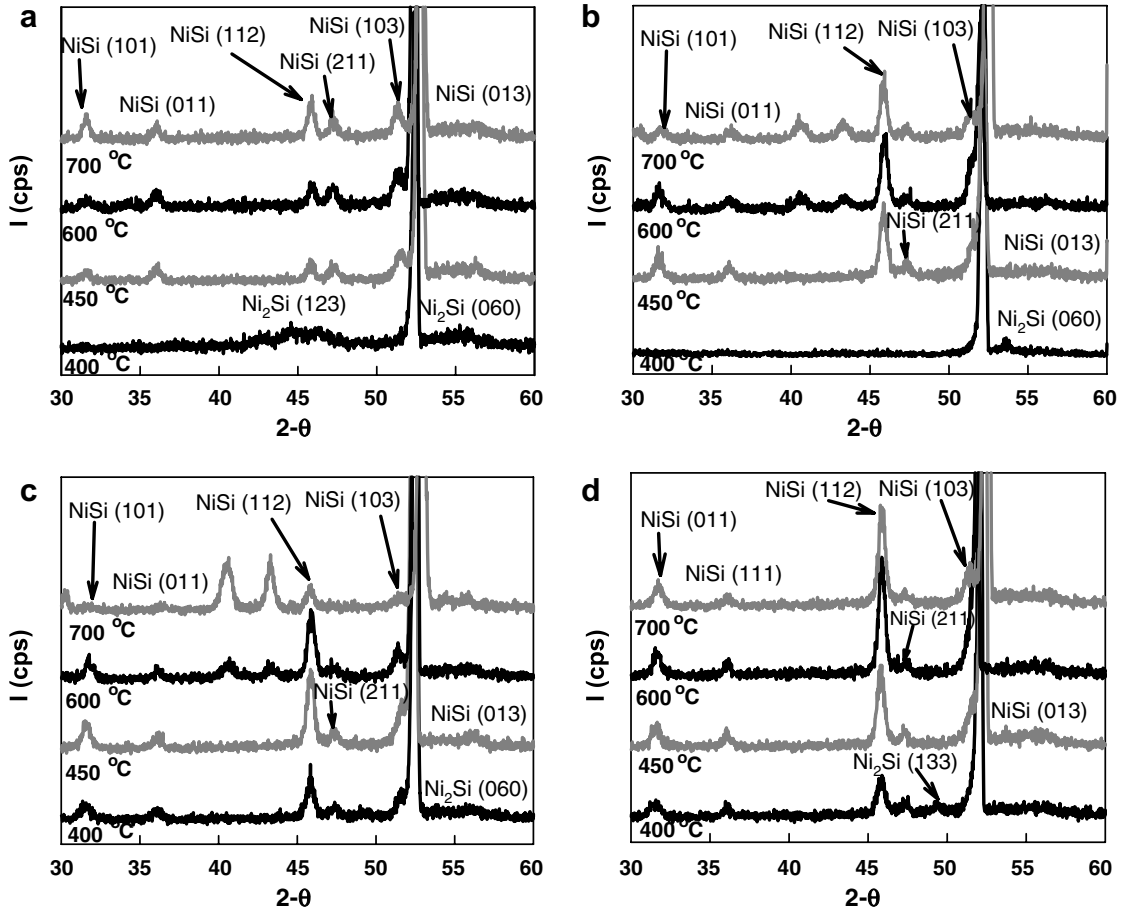

Fig. 2. XRD spectra of (a) uncapped, (b) Ti 10-capped, (c) Ti 30-capped, and (d) TiN 30-capped samples after annealing at 400–700 °C for 30 s.

3. Results

Fig. 1 compares the sheet resistance of Ni-silicide using different capping layer processes after annealing at 300–800 °C for 30 s in an N_2 ambient. At temperatures below 450 °C, all samples exhibit large sheet resistance and it is attributed to the formation of nickel-rich Ni_2Si phase, as analyzed in XRD spectra of Fig. 2. NiSi with low sheet resistance (about 4–5 Ω/sq.) are shown for temperatures ranging from 450 up to 600 °C. At higher than 600 °C, the silicide thin films start to degrade with slight increase in sheet resistance, especially for the Ti-capped samples, as shown in the inset of Fig. 1. The degradation for nickel silicide film annealed at higher temperature is attributed to either the phase transformation from low-resistivity NiSi to high-resistivity $NiSi_2$ or the agglomeration of the silicide film caused by local energy equilibrium at the intersection of grain boundaries [10].

So far as the result of sheet resistance is concerned, the uncapped and TiN 30-capped samples exhibit better thermal stability than the Ti 10-capped and Ti 30-capped samples. Obviously, it does not conduce to relevant shift of the Ni-silicided transformation temperature by using either Ti or TiN capping layer on Ni-silicidation process. This result is distinct from the phenomenon of Co-silicidation process. It has been demonstrated that the transformation point of Co_2Si to CoSi was shifted towards lower temperature by a Ti capping layer, which is arose from that the Ti capping layer lowers the activation energy for CoSi formation by eliminating the formation of SiO_2 between the growing CoSi and the Co [11]. The fact that Ti capping layer does not play an active role for Ni-silicidation process is ascribed to the lower reaction temperatures for Ni and Si.

The XRD spectra for samples annealed at 400, 450, 600 and 700 °C are shown in Figs. 2a–d. All samples annealed at 400 °C exhibit nickel-rich Ni_2Si preferred orientation. After 450 °C annealing, the NiSi phase predominated, and no $NiSi_2$ phase was detected even the annealing temperature is up to 800 °C (not shown here). This finding is consistent with the sheet resistance result that Ti-capped sample does not lead to a significant shift of the nickel silicide transformation temperature. It is more noteworthy that there are two peaks (about 40.6° and 43.3°) detected from the Ti 30-capped and Ti 10-capped samples (peaks from Ti 10-capped sample are unapparent, but still visible), while the uncapped and TiN 30-capped samples are not. The intensity of the two peaks that were detected from the Ti 10-capped and Ti 30-capped samples increase with increasing either the annealing temperature or the Ti thick-

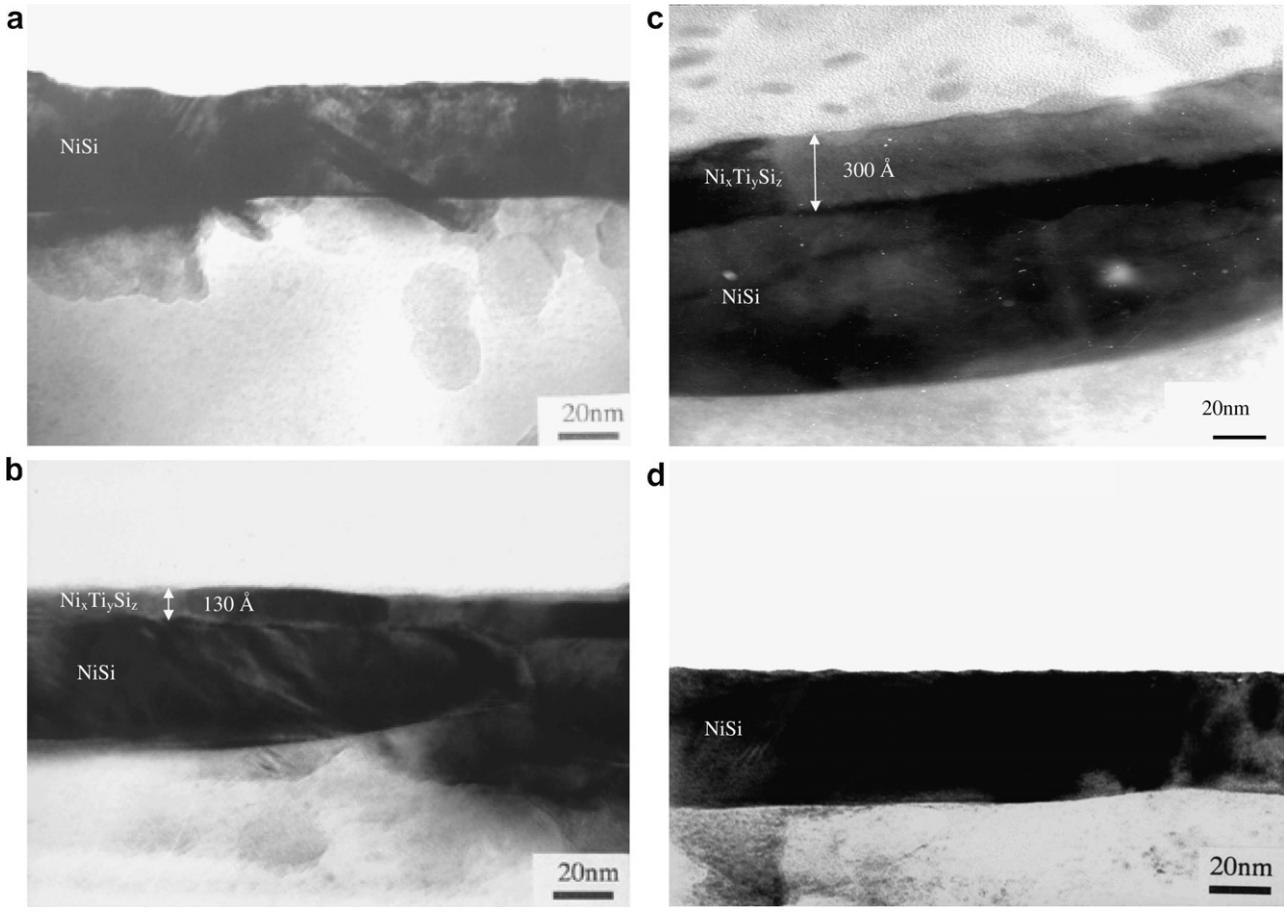

Fig. 3. Cross-sectional TEM images of (a) uncapped, (b) Ti 10-capped, (c) Ti 30-capped, and (d) TiN 30-capped samples after annealing at 650 °C for 30 s.

ness, which indicate that there may be a Ti-compound layer formed on silicide thin film.

To verify the composition of the Ti-compound layer, samples were further analyzed by TEM. Figs. 3a–d show the cross-sectional TEM images of the uncapped, Ti 10-capped, Ti 30-capped, and TiN 30-capped samples annealed at 650 °C for 30 s, respectively. As shown in the figures, there are two layers formed on the Ti 10-capped and Ti 30-capped sample, while only a single layer are found on the uncapped and TiN 30-capped samples. The two layers formed on the Ti 30-capped sample were also analyzed by EDS to confirm their compositions. Figs. 4a and b show the EDS analyses of the upper layer and the lower layer formed on the Ti 30-capped sample, respectively. It is clearly seen that the upper layer is composed of a high-resistivity $Ni_xTi_ySi_z$ compound and could not be removed by etchant, while the lower layer is a relatively low-resistivity Ni–Si compound. Oxygen signal was not detected at either upper layer or lower layer in TEM and EDS results, which is distinct from the result of the previous report about $CoSi_2$ study. It was reported that a Ti cap or alloying layer is capable of gettering oxygen that is incorporated into the deposited Co, and reducing interfacial oxide in the silicidation process by forming a TiO_2 layer in the silicide surface [12]. The similar results are also found in the NiSi studies [13,14]. No detectable oxygen in this study is possibly due to the pre-etching process so that native oxide was completely removed and a clean surface was showed up to form silicide. Furthermore, it is found from Figs. 3b and c that the overall thickness of the silicide layers, as well as the $Ni_xTi_ySi_z$ layer, increase with increasing the Ti capping layer thickness. This result is harmful to the electrical properties of the Ni-silicided device because both thinner silicide layer and lower sheet resistance are the main demand for the ULSI technology. The thicker silicide layer will cause excessive leakage current of the source/drain region, and result in degradation in properties of the devices.

Fig. 5 illustrates the cumulative distributions of reverse-biased leakage current densities (J_R) for the Ni-silicided n^+–p junction diodes annealed at 500 °C for 30 s. Twenty five randomly chosen diodes of area 0.1×0.1 cm^2 was measured at room temperature. As shown in Fig. 5, the uncapped and TiN 30-capped samples exhibit smaller leakage current densities than that of the Ti 10-capped and Ti 30-capped samples. As mentioned above, the thickness of NiSi and $Ni_xTi_ySi_z$ layers increase with increasing the Ti capping layer thickness, as shown in the TEM images of Fig. 3. This means that increasing the Ti capping layer thickness result in the more seriously consumed junction depth, and hence, caused larger junction leakage current.

Fig. 6 reveals the SIMS depth profiles of As^+ for samples annealed at 500 °C for 30 s. There are almost the same junction depth for the uncapped, Ti 10-capped, and TiN 30-capped samples (about 0.076 μm at 10^{19} atoms/cm^3). However, the As profile of the Ti 30-capped sample is shifted toward deeper side (about 0.091 μm at 10^{19} atoms/cm^3). This finding explains why the leakage current of the Ti 30-capped sample is slightly smaller than that

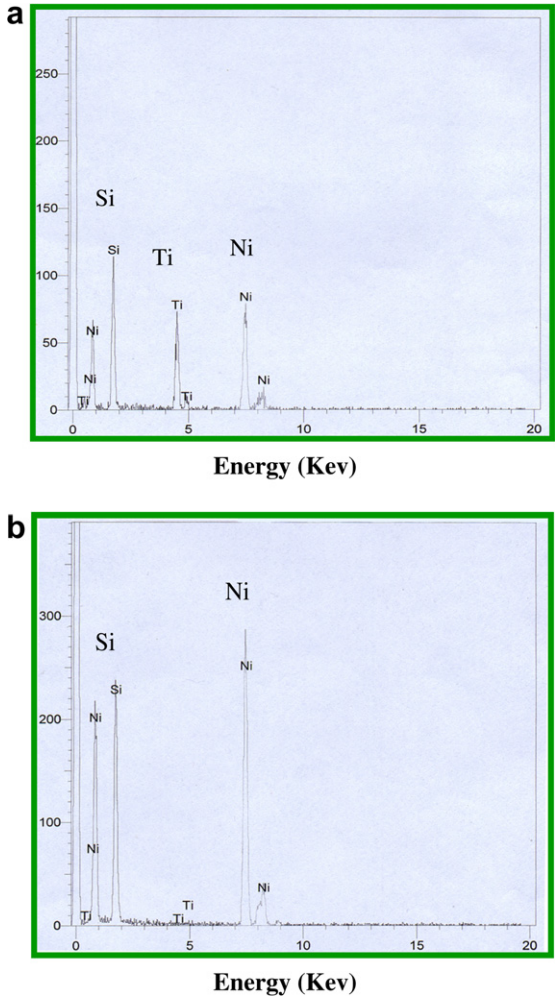

Fig. 4. EDX spectra of (a) the upper layer and (b) the lower layer formed on the Ti 30-capped sample.

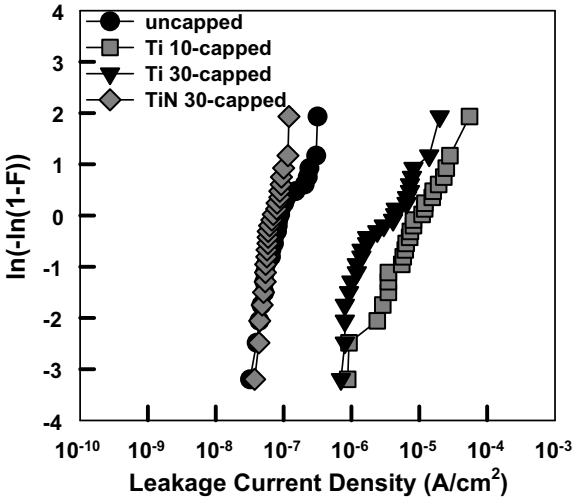

Fig. 5. Cumulative distribution of reverse-biased leakage current densities for the Ni-silicided n^+–p junction diodes annealed at 500 °C for 30 s.

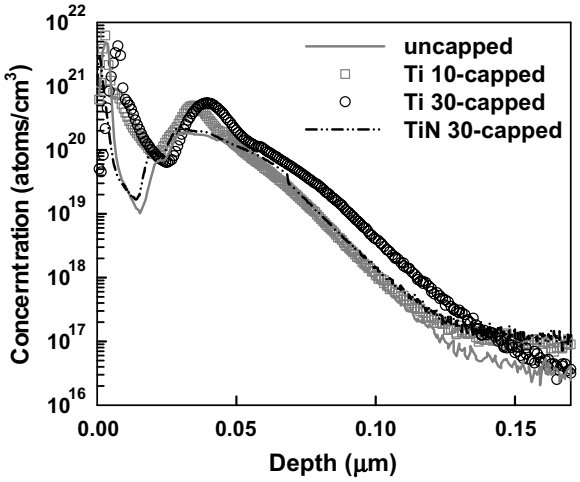

Fig. 6. SIMS depth profiles of As^+ for samples annealed at 500 °C for 30 s.

of the Ti 10-capped sample shown in Fig. 5. It has been demonstrated that As is depleted in the $TiSi_2$ layer and thus diffuses significantly into Si underneath [15]. Therefore, the Ti 30-capped sample with a thicker $Ni_xTi_ySi_z$ compound layer, caused the impurity redistribution to induce a deeper junction depth. In addition, the "snowplough" effect that As accumulates at the silicide/Si interface, especially for the Ti 10-capped and Ti 30-capped samples, is found. This observation indicates that the Ti capping layer leads to the snowplough effect enhancement during the NiSi formation. Moreover, the accumulation of As is deeper for the Ti-capped sample, which is due to the formation of the thicker silicide layers, as shown in Fig. 3.

4. Conclusion

Effects of capping layers on formation of Ni-silicided junction were investigated. With a Ti-capped layer on Ni-silicided sample, it is shown to exhibit inferior thermal stability than the uncapped and TiN-capped samples. For the silicided junctions, samples with a Ti capping layer are shown to have larger leakage current density. A high-resistivity $Ni_xTi_ySi_z$ compound layer formed on the NiSi surface for the Ti-capped sample, resulted in the overall silicide thickness and the junction leakage current increased. In addition, we find that the Ti capping layer enhance the snowplough effect during the NiSi formation.

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