Chapter 1
Introduction

1-1 General Background

Three-dimensional integrated circuit (3D IC) is a new approach for IC fabrication and system integration. It is very important for semiconductor industry because it has many advantages including heterogeneous integration, high performance, and low power consumption. In addition, it is viewed as the extension of Moore’s law [1].

Actually, chip functions can be improved by scaling down the volumes of the transistors and enhancing abilities of computing since 1960. Basically the progression of IC follows the Moore’s law. The roadmap by Intel is shown at Fig. 1-1. But in the future, Because of lithography and physical limitation, the development of scaling down will meet its bottleneck [2]. Not only the transistor itself gets the limitation but also the number of transistors keeps increasing on the single chip. The key to dominate IC performance is not the single transistor anymore. The global interconnect RC delay plays an important role [3]. Although it can reduce the transmission distance of some important areas by IC design, the total conduct distances are still the same. If the chip function needs to keep making progressing, efficiently reducing the total transmission distance of conduce lines is the essential factor. Therefore, 3D IC is needed for semiconductor development.

Moreover, semiconductor industries always increase some unique processes and materials with requests of boosting IC function. So the heterogeneous integration is more important than usual, this concept is described at Fig. 1-2. This kind of heterogeneous integration involves using different heterogeneous substrate materials and fabricating chips at different process temperatures. For integration of heterogeneous substrate materials, it is apparently to use new approaches to integrate them together. And for fabricating chips at different process temperatures, the latter process temperature needs to lower than the former one. If it exceeds the thermal budget, many transistors applications like the waveguide transistors and the integration of traditional CMOS will be restricted [4].

For the purpose of resolving the challenges and requirement above, the concepts of 3D integration and 3D IC appear. The general idea of 3D IC technique is to change the traditional method placing IC at X and Y two dimensions. It enhances Z dimensions. The space of vertical stacking can be created. According to this concept, utilizing 3D technique can avoid the problems of traditional 2D IC keeping scaling down like the too long total conduct lines and the volume of chips is too large to get the frivolous requirements in Fig. 1-3 [5].

3D IC technique always uses two methods which are wafer bonding and chip stacking. And it use through–silicon via (TSV) to connect the thinning wafers and chips. It can convert the traditional 2D IC to 3D IC, and the development is shown in Fig. 1-4.

Due to 3D IC can efficiently put the space to use and shorten the transmission distance of current signals, resistance-capacitance delay and total resistance can be reduced. Besides, owing to using these unique concepts of wafer bonding and chip stacking, fabrications of heterogeneous substrate materials can be separated at the beginning and stack together in the end. As mentioned above, the process temperatures and other circumstance requirements will restrict different ICs. But now these problems can be resolved by the method of stacking. Through optimized design of the chip stacking, the heterogeneous integration of 3D-IC can achieve future demand. So 3D IC can provide a lot of advantages like multi-functions heterogeneous integration, high performance and low power dissipation under the requirements of frivolous demands and cost down.

Due to this characteristic concept of 3D IC, this technology will subvert traditional 2D IC. And it is closely linked to IC design, process techniques, instruments, packaging, testing methods, terminal product application and performance. These fields will dominate the maturity of 3D IC and its terminal products. In other words, 3D IC is a novel technology to integrate all fields. In all these fields, the process of 3D IC is the most essential factor [6].

3D IC brings many new process techniques such as wafer bonding, chip stacking, TSV fabrication and wafer thinning in Table 1-1. Directions of stacking are face-to-face and face-to-back. And stacking approaches are die-to-die, die-to-wafer and wafer-to-wafer. In addition, 3D IC involves using different substrate materials, bonding materials and stuffing materials. So many derivative phenomena of material and physics need to be resolved. Under so many kinds of process selections, developing 3D IC with low cost, high yield and high performance is the most key point.

1-2 Motivation – Why do we need adhesion strength test and hetero-bonding approach?

Hybrid bonding is one of most core technologies for 3D integration [7-13]. It has abilities to combine metal to metal bonding with oxide dielectric or organic adhesives (ex. polymer dielectric material) or inorganic other dielectrics material (ex. silicon nitride), which able to achieve native metal interconnection with adhesive interlayer bring reinforcement of the mechanical strength between stacked ICs as shown in Fig 1-5. Because of the adhesives or dielectrics is use to play simultaneously the roles of bonding material and under-fill filling, they effectively improve the bonding strength and raise the device reliability. Furthermore, the electrical interconnect and inner-gap filling can be fabricated at the same time, the process flow can be simplified and avoids the micro-gap filling challenge, and therefore increases the throughput and yield.

In this thesis, we focus on two topics: one is the investigation of adhesion strength test between metal and polymer, and the other one is hetero-bonding approach using oxide-polymer and different metals. These investigation results provide useful information for hybrid bonding development in three-dimensional integrated circuit (3D IC) applications. However, there have many critical topics in this thesis as shown in Fig. 1-6.

About material selection for this research, Cu metal and benzocyclobutene (BCB) polymer dielectric were studied as the main materials in adhesion strength test. In addition, silicon oxide-BCB, Al-Cu, and Sn-Cu were fabricated for hetero-bonding investigation. In the adhesion strength test, the effects of layer thickness, layer stacking order, and usage of titanium or tantalum nitride layer between Cu and BCB polymer were investigated. Quantity analysis data was achieved to define the optimized staking structure, and the results of this research can provide important guidelines of hybrid bonding and under-fill for 3D integration applications. In hetero-bonding study, the bonding condition and corresponding mechanism of each bonding scheme were explored. Finally, Four-terminal Kelvin test structure was fabricated to investigate the electrical characteristics and reliability of Al-Cu bonding, including AC current stressing test, DC current stressing test, and humidity test. However, Cu bonded interconnect with Al bonded interconnect as major bonding and conduction layer, it can be regarded as a new approach of integrated circuit fabrication such like integration of 65 nm Cu process and 0.11 μm Al special process on 3D IC applications. Therefore, in order to verify the capability of Cu-Al bonded interconnect for commercial usage and mass production, reliability test is strongly required.

1-3 Organization of the Thesis

In Chapter 2, the major characteristics of all instruments which are used in this thesis will be literally introduced.

In Chapter 3, we measure the adhesion strength between different layers including: Cu-BCB, Cu-Ti-BCB, Cu-TaN-BCB, Cu-Parylene, Cu-Ti-Parylene, and Cu-TaN-Parylene by 4-point bending test. In addition, the effects of layer thickness, layer stacking order, and usage of titanium or tantalum nitride layer between Cu and polymer were investigated.

In Chapter 4, we investigate the different material to do hetero-bonding including: chip level PECVD oxide-BCB bonding and thermal oxide-BCB bonding, chip and wafer level Al-Cu bonding, electrical measurement of chip level patterned Al-Cu bonding, and chip level patterned Sn-Cu bump bonding. And the bonding condition and corresponding mechanism of each bonding scheme were explored.

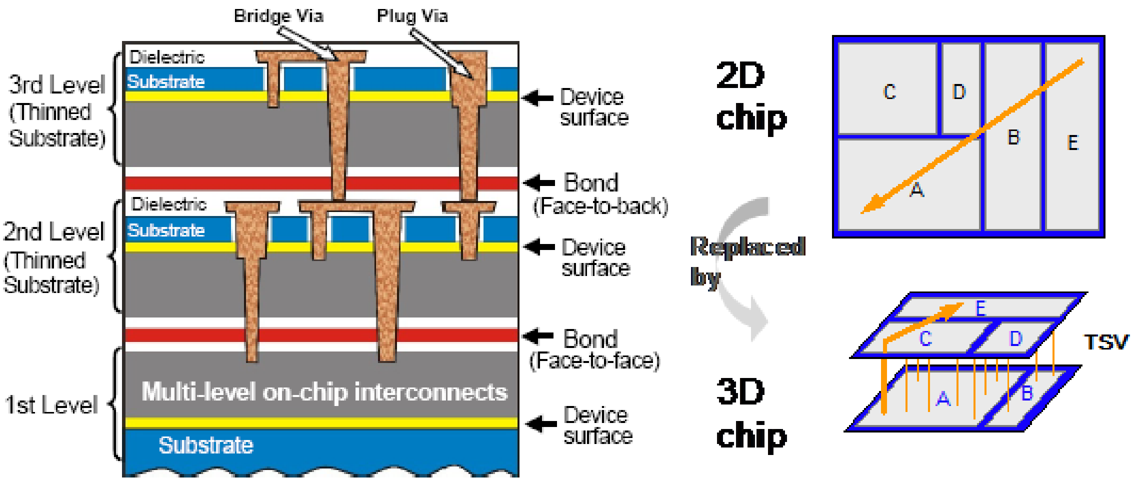
In Chapter 5, it will jump to conclusion for this thesis and make some suggestions. Also the future work for this study will be told.

(Intel)

Fig. 1-1 Intel demonstrates roadmap

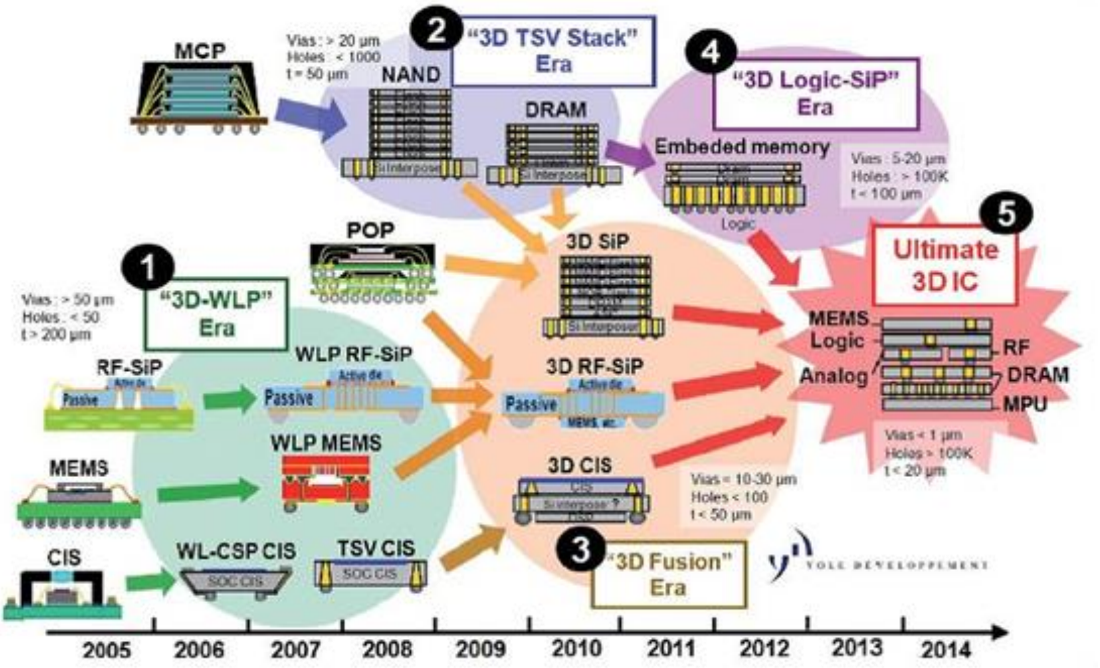
(Zycube, MNCN)

Fig. 1-2 3D IC technology integrate different function chips by heterogeneous stack



(LETI, EMC 2007)

Fig. 1-3 3D integration can improve performance compare with nowadays 2D circuit



(Yole development)

Fig. 1-4 Development of 3D-IC scheme

Category	Detail terms
Stacking approach	a. Die-to-Die (D2D) b. Die-to-Wafer (D2W) c. Wafer-to-Wafer (W2W)
Substrate selection	a. Bulk (Si, Ge, GaAs……) b. SOI
Bonding method	a. Metal-to-Metal b. Oxide-to-Oxide c. Polymer-to-Polymer d. Hetero-bonding
Direction of stacking	a. Face-to-Face b. Face-to-Back
Fabrication of TSV	a. Via-First b. Via-Last

Table 1-1 Classification of 3D IC processes and integration techniques

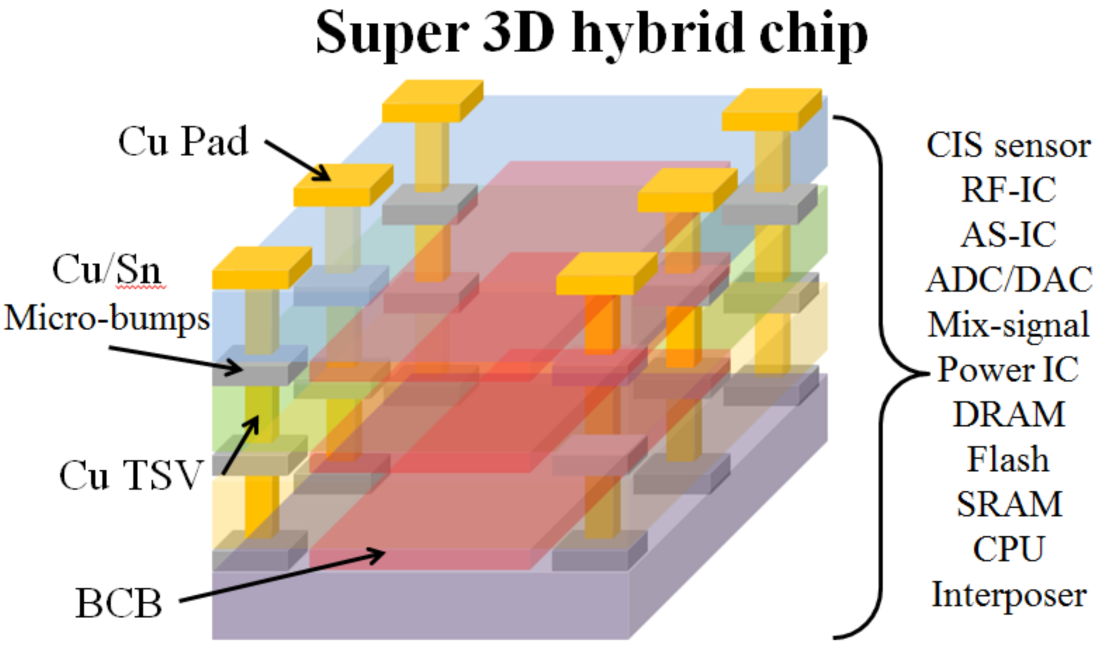


Fig. 1-5 Hybrid chip

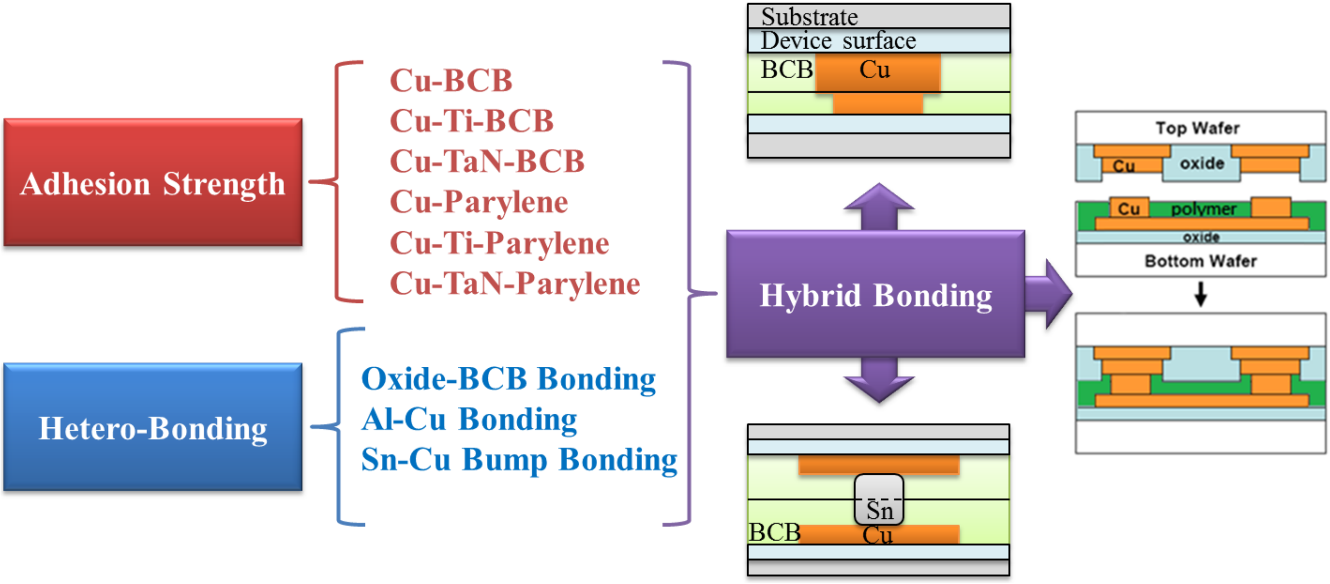


Fig. 1-6 The critical topics for hybrid bonding development

Chapter 2
Experimental Instruments

2-1 Introduction

In this chapter, some of the equipment instruments are been described. They play an important role in our research. It is divided into two parts to do introduction: process instruments and material analysis instruments. All the samples studied in this work are prepared in Nano Facility Center (NFC), Center for Nanotechnology, Materials Science, and Microsystems (CNMSM), National Nano Device Laboratories (NDL), Instrument Technology Research Center (ITRC), and MA-Tek. The condition of the instrument described in the thesis is based on the instruments provided in these places.

2-2 Process Instruments

I. Oxford Plasma Enhanced Chemical Vapor Deposition system

Plasma enhanced chemical vapor deposition (PECVD) is usually used for the thin film deposition, and let material source change from gas state into plasma state to accelerate chemical reactions, the outlook of

PECVD shows at Fig. 2-1. The plasma is filled by process gases and generated by two electrodes which is bias with RF signal or DC signal. Processing plasmas are usually operated at the pressures of a few mTorr to a few Torr so the atoms and ions can reach enough meant free path. Ionized atoms or molecules are accelerated towards or leave the neighboring surface in sheath region (depends on their charges); therefore, all surfaces exposed to the plasma receive energetic ion bombardment. The potential across the sheath layer is typically only 10–20 V, the sheath layer is naturally generated because those electrons move faster than atoms or molecules, and can produce much higher sheath potential by modified reactor geometry. Ion bombardment is not only leaded to increases in density of the film but also remove contaminants that cover the sample surface to improving film quality. Ion bombardment density can be high enough to do planarization of thin film. Silicon dioxide can be deposited by using different silicon precursor gasses like dichlorosilane or silane and oxygen precursors. Silicon nitride can be formed by using silane and nitrogen or ammonia. Silicon Dioxide can also be deposited from a tetra-ethyl-ortho-silicate (TEOS) silicon precursor in oxygen or oxygen-argon plasma. Silicon dioxide deposited by High-density plasma can create a nearly hydrogen-free film with good conformality.

II. Thermal Evaporation Coater ULVAC EBX-6D

In PVD system as show in Fig. 2-2, thermal evaporation is popular and widely used. By using high temperature to melt metal of target into vapor state, because high temperature let atom and molecule shaking, and through a vacuum space, atom and molecule of vapor is condensed on substrate surfaces to forming thin film. In the vacuum chamber, molecules are able to evaporate freely, and then condense on substrate. In this method, high temperature is play important role. By using a big current passing through the resistance to produce high temperature, and the temperature can reach the melting point, so that it can melt metal of target. Because the resistance need to tolerate high temperature, it is manufactured by W(mT=3380℃), Ta(mT=2980℃), or Mo(mT=2630℃) on usually. The melting temperature of target should be lower than the melting point of resistance; therefore, thermal evaporation coater is often used to deposit Al, Ag, Au, and Cr. This method have some advantage such as simple and cheap of equipment, but also have disadvantage such as bad quality of thin film, low depositing speed, poor hardness, and uniformity problem.

III. Sputter

Ion Tech Microvac 450CB showed in Fig. 2-3, was used for depositing all of our metal materials. The sputtering system is composed of the following: (1) Sputtering chamber (2) vacuum pumps, consisting of one cryo pump and mechanical pump (3) DC power (4) 4-inch magnetron gun (5) gas flow meter (6) pressure gauges (7) film thickness monitor. The 4-inch or 6-inch Si substrates are placed in the spin holder driven by a motor. The targets (metals such as Cu, Ti, Fe, etc.) are 4-inch. The DC source can provide up to 200 W powers. Normally the base pressure is around 3.0 × 10-6 torr and the working pressure is around 7.6 mtorr. The flow rate of Ar is around 24 sccm. The sputtering DC source is kept at 150W for our experiment.

Its basic principle is physical vapor deposition. PVD is driven by momentum exchange between the ions and atoms in the materials, due to collisions. The incident ions set off collision cascades in the target. When such cascades recoil and reach the target surface with energy above the surface binding energy, an atom can be ejected.

IV. Flip Chip Bonder

This multipurpose bonding platform FINEPLACER Pico MA for advanced assembly can process bonding step where 5 μm accuracy shows at Fig. 2-4. And it has high magnification to do alignment procedure. Advanced device packaging like assembly of MEMS, sensors, RFID, embedded components and surface mount photonics can be completed at this bonder. Also, it can execute precise die attach, flip chip bonding, LED bonding and chip to wafer (6”) bonding. Some high technologies have been adopted on this instrument such as thermo compression, thermo sonic, ultrasonic bonding, soldering (AuSn, C4, Indium), face-up/face-down assembly, flip chip on flex, chip on glass (CoG) and adhesive technologies (ACF/ACP/NCP). Some features are spotlighted like vision alignment system ensures placement accuracy 5μm, larger field of view and working area (6”), shifting module for bigger chip sizes, quick and easy setup of new applications, manual & motorized configuration available, hands-off operation in motorized configuration, high resolution video optics with fiber optic lighting, process observation and monitoring and independent substrate handling without tool change. Its software “WinFlipChip” can advanced process recording and reporting functions, control of all connected process modules, advanced force control, drag & drop function to adjust profiles, options to capture pictures and movies and graphical user interface. The outlook of FINEPLACER Pico MA is shown in Fig. 2-4.

V. Wafer Bonder

The EVG520HE is a thermo-compress bonding tool as shown in Fig. 2-5; the theory of thermo-compress bonding is using pressure and heat to make the contact area between these two wafers distortion slightly to increase contact area. At a certain temperature that is high enough at the wafer surface, these wafers will going diffuse between each other to make the bonding process complete, but this method doesn`t require strict surface cleaning and high vacuum condition.

Because thermo-compress bonding process is simpler and cost less, it`s more attractive to industry and academic circle, more effort, investigation and development are put in. The most important parameter in this method is temperature cause wafer level bonding is used at 3D-IC electron device and application, so the bonding temperature should compatible with BEOL (back-end-of-line) to avoid influencing device performance and reliability.

EVG520HE is a single chamber tool that the maximum size of procedure wafer is 4 inch, besides it can handle 2 × 2 cm^2 chip. It is a semi-automatic tool that can heat or cool upper and bottom wafer at the same time. And EVG520HE has individual ramp system to provide different process temperature to upper and bottom wafer, the maximum process temperature is 400 ℃, besides, it can provide compress force up to 10000 Nt for 4 inch wafer to enhance bonding, this tool does not require vacuum environment to achieve bonding successful.

2-3 Material Analysis Instruments

I. Optical Microscope (OM)

Light incident from the object will be enlarged by at least two optical systems such as objective lens and eyepiece, First objective lens to produce a zoom in real image, and the human eye observe real image that enlarge by objective lens through the eyepiece. The optical microscope can replace the lens, so that the observer can replaced magnification.

These objectives are generally placed on a rotating nosepiece, rotation of nosepiece can let different lens enter into the optical path reached the eyepiece. 1600 times became a light microscope magnification, the maximum limit, making the morphology of the application to be greatly restricted in many areas. If you want to observe smaller objects, you will require other methods such as electron microscopy.

II. Scanning Electron Microscopy (SEM)

SEM provide an express way to inspect the surface morphology and the cross section inspect image of the critical layer and the resistive switching thin films, are characterized by the scanning electron microscopy (SEM, Hitachi S-4700) with a resolution of 1.5 nm operated at 15 kV, the outlook of SEM shows at Fig. 2-6. We need to coat a thin Pt layer on the samples before sent them into the chamber of SEM to enhance conductivity and get a high quality image. The accelerated electron beam, emitted from a cold-cathode electron gun with the extract voltage in the range from 0.5 kV to 30 kV, collides with DUT, and the secondary electrons originated within a few nanometers from the surface of the DTU are detected and rendered into a bright SEM image.

III. Focused Ion Beam

Focused ion beam (FIB), is a technique used particularly in the semiconductor and materials science fields for site-specific analysis, deposition, and ablation of materials. FIB systems have been produced commercially for approximately twenty years, primarily for large semiconductor manufacturers. Its setup is a scientific instrument that resembles SEM. However, while SEM uses a focused beam of electrons to image the sample in the chamber, FIB setup instead uses a focused beam of ions. It can also be incorporated in a system with both electron and ion beam columns, allowing the same feature to be investigated using either of the beams. It should not be confused with using a beam of focused ions for direct write lithography, where the material is modified by different mechanisms.

FIB systems use a finely focused beam of ions (ex. Ga) that can be operated at low beam currents for imaging or high beam currents for site specific sputtering or milling. Fig. 2-7 shows the gallium primary ion beam hits the sample surface and sputters a small amount of material, which leaves the surface as either secondary ions or neutral atoms. The primary beam also produces secondary electrons. As the primary beam rosters on the sample surface, the signal from the sputtered ions or secondary electrons is collected to form an image. At low primary beam currents, very little material is sputtered and modern FIB systems can easily achieve 5 nm imaging resolution. At higher primary currents, a great deal of material can be removed by sputtering, allowing precision milling of the specimen down to a sub micrometer scale. If the sample is non-conductive, a low energy electron flood gun can be used to provide charge neutralization. In this manner, by imaging with positive secondary ions using the positive primary ion beam, even highly insulating samples may be imaged and milled without a conducting surface coating, as would be required in a SEM.

At lower beam currents, FIB imaging resolution begins to rival the more familiar scanning electron microscope (SEM) in terms of imaging topography, however the FIB's two imaging modes, using secondary electrons and secondary ions, both produced by the primary ion beam, offer many advantages over SEM.

FIB secondary electron images show intense grain orientation contrast. As a result, grain morphology can be readily imaged without resorting to chemical etching. Grain boundary contrast can also be enhanced through careful selection of imaging parameters. FIB secondary ion images also reveal chemical differences, and are especially useful in corrosion studies, as secondary ion yields of metals can increase by three orders of magnitude in the presence of oxygen, clearly revealing the presence of corrosion.

IV. Transmission Electron Microscopy (TEM)

TEM is short for Transmission Electron Microscopy; it is a powerful tool for materials analysis. The outlook of TEM is shown at Fig. 2-8. From 1930, first TEM is applied into industry, now days the resolution of TEM can reach 2~3Å with high working voltage about 1000KV. This nano scale inspection is really important and necessary to semiconductor development. The working principle of TEM is that electrons have wave form brought out by Louis de Broglie. The atomic resolution capability offers an express way to enter nano-scale world. It is commonly used to materials investigation on morphological observation, crystallographic study, and elemental identification. The field applications may cover a wide span from semiconductor, ceramics, metals, alloy, polymer, and bio-medical materials.

V. Scanning Acoustic Tomography (SAT)

SAT is the short for Scanning Acoustic Tomography and it`s also called SAM (Scanning Acoustic Microscope) shown at Fig. 2-9. The working frequency of SAT is MHz level but not the ultrasonic cleaning that working at KHz frequency. The transmission depth depends on the raise of frequency to decrease, in normal condition, MHz level ultrasonic don`t bring cavitation effect so it can`t use at cleaning or agitate fragile device.

Because this characteristic that MHz ultrasonic don`t cause any damage to the sample and it can transmit a certain depth of solid or liquid material to inspect the structure, but ultrasonic is very sensitive to the air inside the test structure that air can interrupt the transmission of ultrasonic, so this can applied to check the completeness of chips.

Test structure are soaked in dielectric normally be water, by analyze the reflex of ultrasonic with software, we can check the line and layer inside the chip that can`t be seen by bare eye.

2-4 Electrical Measurement Instrument

Agilent 4156C precision semiconductor analyzer is used to measure the electrical properties of the bonded structure. The 4156C provides highly accurate laboratory bench top parameter analyzers for advanced device characterization. The superior low-current and low-voltage resolution and built-in quasi-static CV measurement capability of the 4156C provide a firm foundation for future expansion with other measurement instruments. A picture of 4156C is shown in Fig. 2-10.

(NDL)

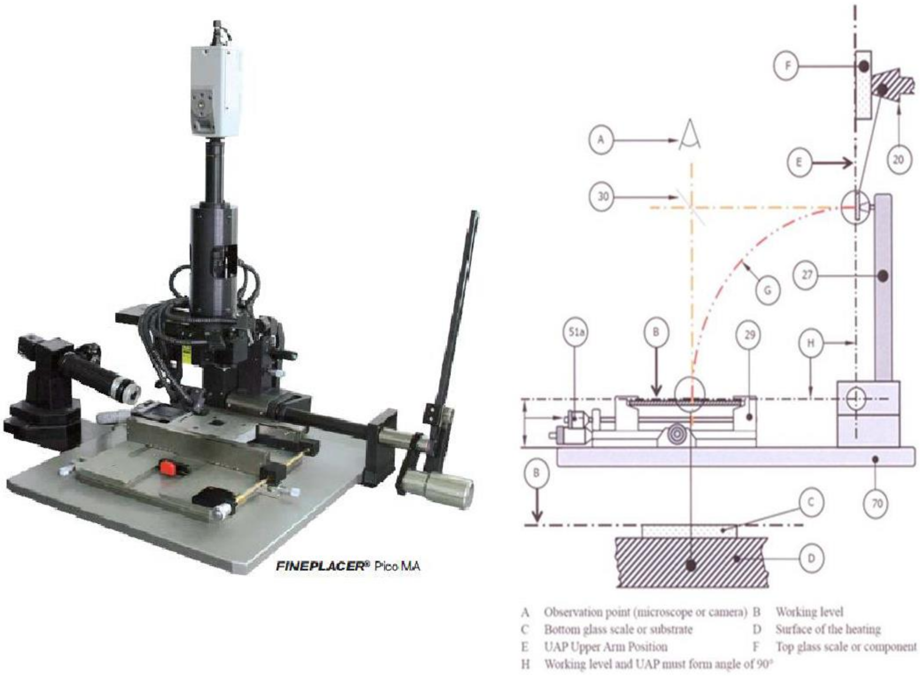
Fig. 2-1 Outlook of plasma enhanced chemical vapor deposition

(NFC)

Fig. 2-2 Outlook of thermal evaporation coater

(NFC)

Fig. 2-3 Photo of Ion Tech Microvac 450CB, Sputter A

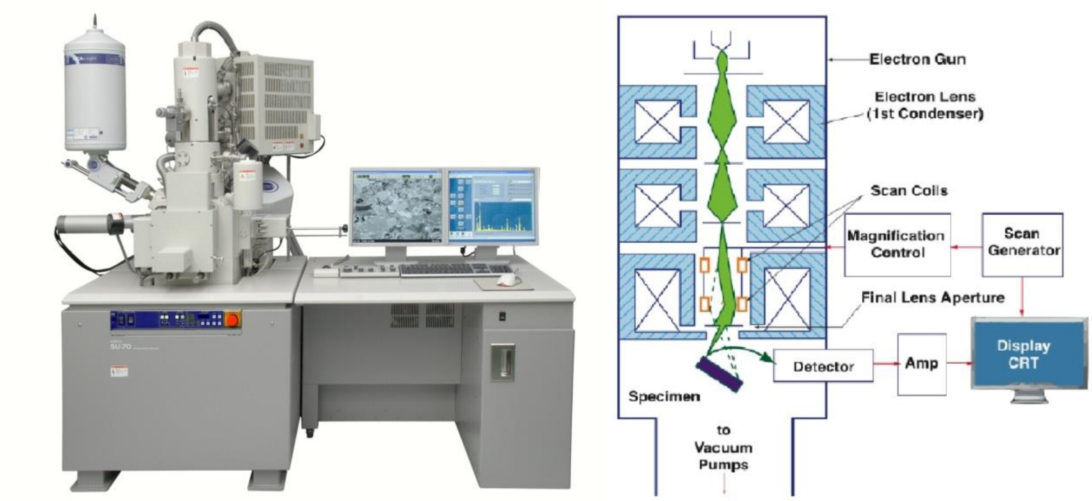


(NFC)

Fig. 2-4 Outlook of flip chip bonder

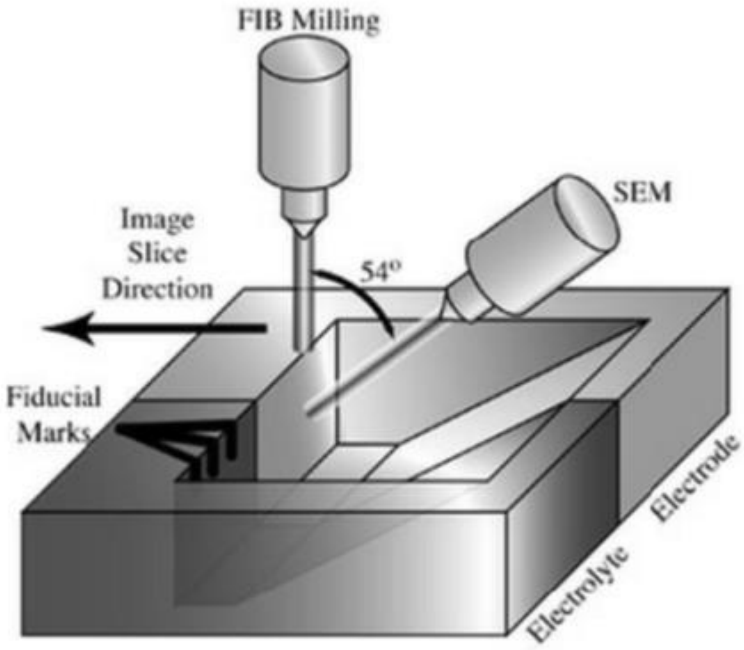
(CNMM)

Fig. 2-5 Outlook of EVG 520



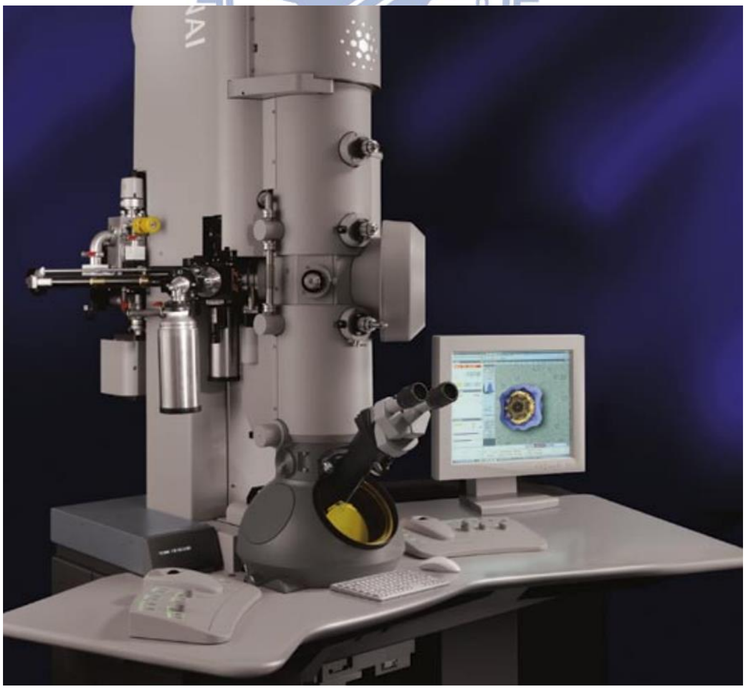
(Hitachi, University of California Riverside)

Fig. 2-6 Outlook of scanning electron microscopy



(Imperial college, London)

Fig. 2-7 Schematic of FIB



(FEI)

Fig. 2-8 Outlook of Transmission Electron Microscope

(HITACHI)

Fig. 2-9 Outlook of scanning acoustic tomography (SAT)

Fig. 2-10 Picture of Agilent 4156C

Chapter 3
Investigations of Adhesion Strength

3-1 Introduction

This chapter focuses on the investigation of adhesion strength between metal and polymer. The adhesion strength between copper (Cu) metal and benzocyclobutene (BCB) polymer dielectric was investigated. This investigation results provide useful information for hybrid bonding development in three-dimensional integrated circuit (3D IC) applications.

The effects of layer thickness, layer stacking order, and adding titanium layer between Cu and BCB polymer were studied using 4-point bending test. Surprisingly, the conventional titanium (Ti) adhesion layer commonly used in semiconductor industry weakened the adhesion between Cu and BCB. In addition, sum frequency generation vibrational (SFG) spectroscopy was used to gain a better understanding at molecular level. SFG is currently the only technique that can provide vibrational spectra at buried interfaces. It has been shown to provide monolayer surface sensitivity at polymer interfaces.

In this research, we investigate the adhesion between copper and BCB polymer dielectric to extract the guidelines for copper and BCB bonding. The adhesion between copper and BCB polymers are important in two schemes of 3D integration, one is the hybrid bonding scheme, and the other is BCB as under-fill situation, as shown in Fig. 3-1 [14,15].

Regarding the metal and polymer selection for bonding schemes, copper is a popular metal used for interconnection in semiconductor fabrication due to the excellent thermal and electrical properties. In addition, BCB polymer is commonly used in semiconductor and packaging industries because of its excellent physical properties such as low curing temperature, low level of ionic contaminants, low moisture absorption, low dielectric constant, good thermal stability, good compatibility, high optical clarity and high degree of planarization with metallization systems. With 3D integration becomes more and more popular for next generation IC application, the aforementioned bonding schemes will becomes common conditions. Therefore, it is significant to study the adhesion between copper and BCB [16,17].

3-2 Experimental Procedure

In this study, three groups of sample combination were prepared as shown in Fig. 3-2. In group 1, 3 μm thick BCB was formed on bare Si wafers first. Part of the wafers was then sputtered with 30 nm thick titanium layer. Finally, all wafers were sputtered with 0.2 μm thick copper layer. The group 2 wafers were prepared with the same steps as group 1, but the thickness of copper and titanium layers were changed to 1.2 μm and 100 nm, respectively. In group 3, the wafers were prepared by sputtering a 1.2 μm thick Cu layer first on bare Si wafers. Part of the wafers was then sputtered with a 100 nm Ti layer. Finally, a 3μm thick BCB layer was formed on all these wafers. In addition, we change a 100 nm Ti layer and a 3 μm BCB polymer into a 100 nm TaN layer and a 3 μm Parylene polymer for comparison of group 3 as shown in Fig. 3-3.

Prior to 4-point bending test, all wafers were first diced into 70 mm × 70 mm size square shape, cleaned, and then face to face bonded with bare silicon dies of same size by epoxy glue. The bonded samples were annealed at 150 ℃ for 1 hour for glue curing. Six types of bonded samples were subsequently diced into dies with 4 mm × 70 mm size. Finally, a notch was created in each bonded sample by dicing at middle position of either Cu/BCB die or bare Si die side.

3-3 Result and Conclusion

Fig. 3-2 shows six types of test sample structure. Through the evaluation by 4-point bending test, the fracture behavior at the interface can be analyzed, and the fracture energy of peeling layer can be measured to obtain the adhesion strength of each Cu/BCB test structure [18].

In this research, the interfacial quantitative fracture energy (G_C) can be obtained by the formula [19]:

$$G_C = \frac{21(1-v^2)P_C{}^2L^2}{16Eb^2h^3} \qquad (1)$$

where v, P_C, L, E, b, h denote the Poisson ratio of the substrate, the critical applied force, half the difference of outer to inner span with the loading points, Young’s modulus of the substrate, the sample width and the half thickness of the sandwich sample, respectively. And the setup for 4-point bending test is shown as Fig. 3-4.

The measurement results of adhesion strength for different types of sample structure are shown in Table 3-1. The results from group 1 and 2 indicate the thickness of metal layer is not a critical factor to affect adhesion strength. In addition, the extra titanium layer cannot enhance the adhesion strength between BCB and copper metal, but induce the strength degradation in all groups. On the other hand, the group 3 results indicate that changing the stacking order of copper and BCB layers can effectively increase the adhesion strength. Therefore, the group 3 structure without extra titanium layer has the best result in this research.

Generally, the interface stress between layers is dependent on the thickness of metal layer. However, the scale of copper layer thickness in this research is small and interface stress effect between thin films is not obvious [20]. Therefore, the adhesion strength of group 1 and 2 are low and about the same quantity.

From the experimental results, stacking order can affect the adhesion strength significantly, because the thermal expansion coefficients of different materials cause the stress mismatch between different layers. However a well-designed stacking order for multi-layer structure can minimize the extrinsic stress of mismatch, which can further increase the adhesion strength [21].

However, for all groups, the extra titanium layer could not enhance the adhesion strength between Cu and BCB and caused strength degradation. Therefore, we changed a 100 nm Ti layer and a 3 μm BCB polymer into a 100 nm TaN layer and a 3 μm Parylene polymer for comparison of group 3, and the results are shown in Table 3-2. We can discover that extra TaN layer has not bad adhesion between Cu/BCB and Cu/Parylene. But the same result of extra titanium layer, it could not enhance the adhesion strength between Cu and Parylene and caused strength degradation, too.

To gain a molecular-level understanding on why the adhesion strength of Ti/BCB is lower than that of Cu/BCB, SFG was used to study the BCB/metal interfaces after a cure process. SFG was carried out by mixing a picosecond 800 nm beam and a broad band femtosecond IR beam on a surface, and SFG from the surface is measured as a function of the input IR frequency. Fig. 3-5 (a) shows the SFG spectrum of an air/BCB interface (3 μm of BCB on Si). Two main peaks were observed in the CH region. The 2870 cm^{-1} and 2930 cm^{-1} peaks are consistent with to the methyl group symmetric C−H stretching mode and the Fermi resonance. The results indicated that the methyl groups are ordered at the air/BCB interface [22].

Fig. 3-5 (b) and 4c show the SFG spectra of Ti/BCB and Cu/BCB interfaces, respectively. The nonzero baselines presented in Fig. 3-5 (b) and 4c came from the SFG from the metal films. The 2870 cm^{-1} peak appear as a negative peak in Fig. 3-5 (b) because of the interference between the signal from BCB and Ti film. Comparing Fig. 3-5 (b) with Fig. 3-5 (c), it is clear that the 2870 cm-1 peak of BCB is observable at the Ti/BCB interface while it is undetectable at the Cu/BCB interface. It indicates that BCB maintains certain ordering at the Ti/BCB interface but becomes disordered at the Cu/BCB interface. The ordering change of BCB upon deposition of Cu film is an indication that there is a stronger interaction between Cu and BCB, which is consistent with the above 4-point bending test.

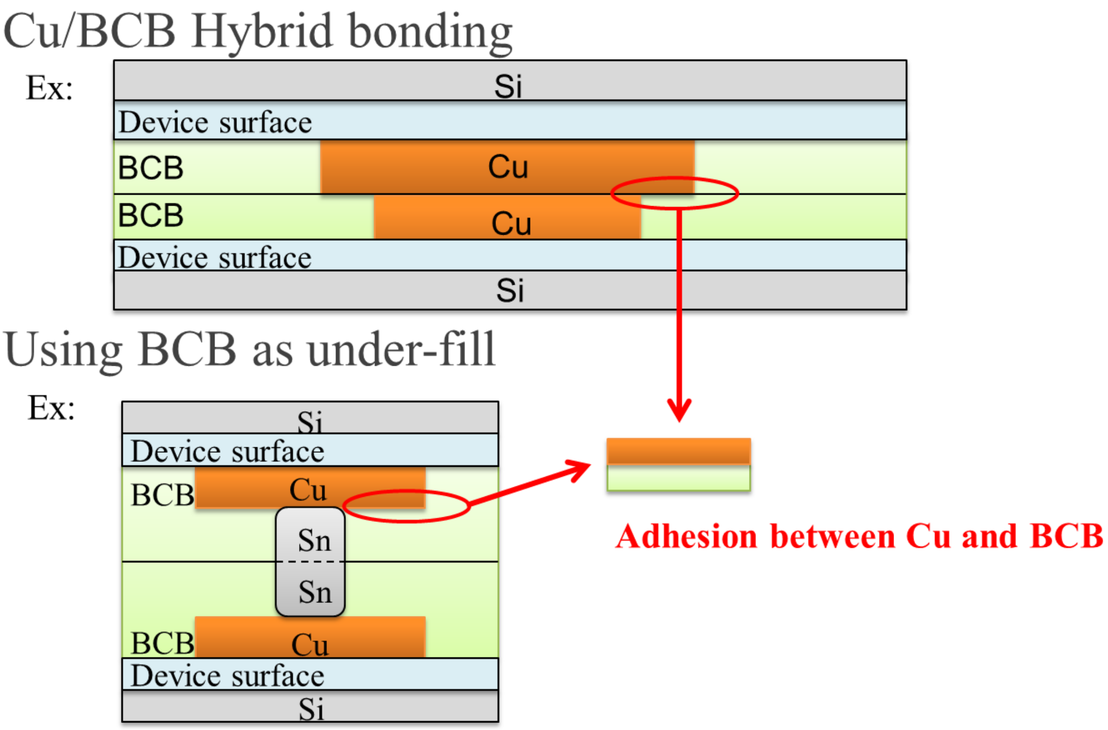


Fig. 3-1 The adhesion between copper and BCB in hybrid bonding and under-fill

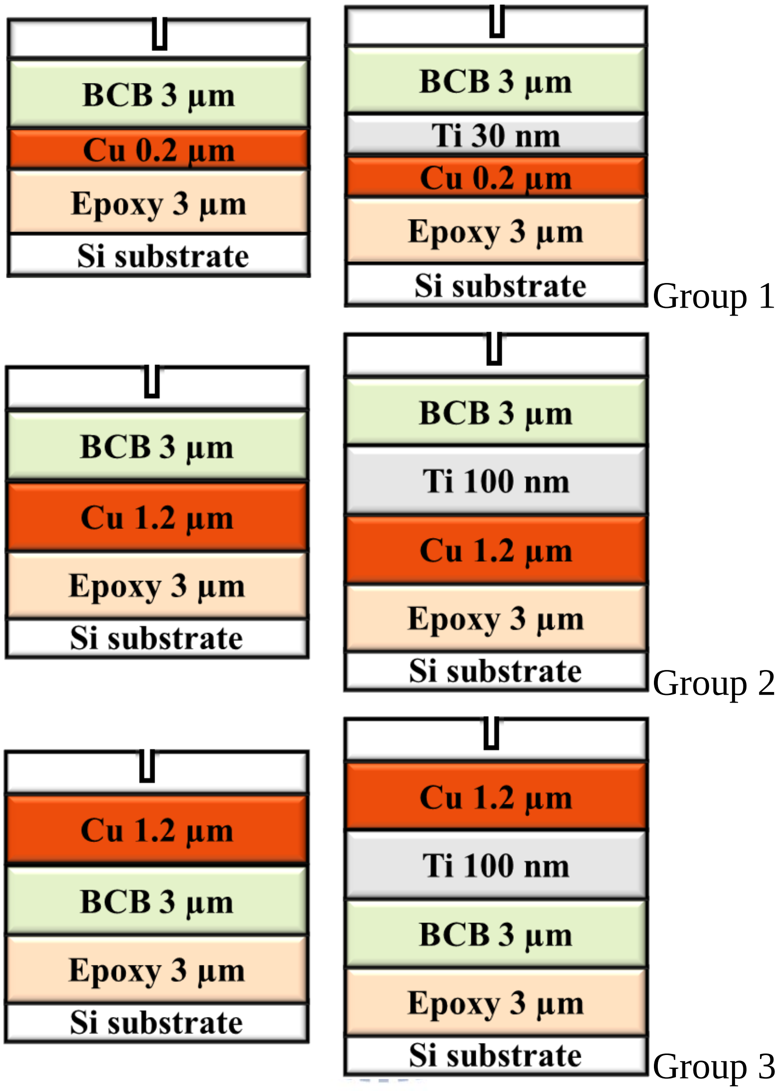


Fig. 3-2 The samples whit Group 1, Group 2, and Group 3

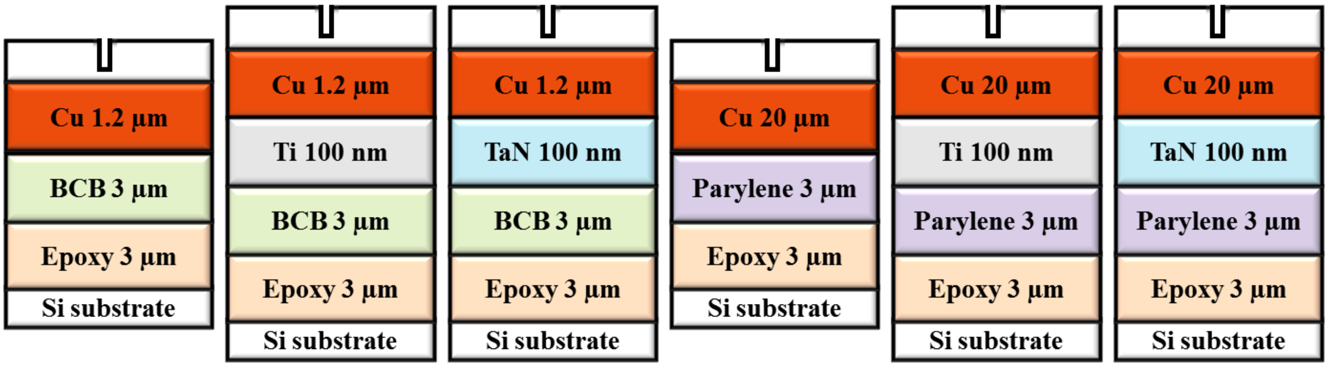


Fig. 3-3 Comparison of using TaN layer and Parylene polymer

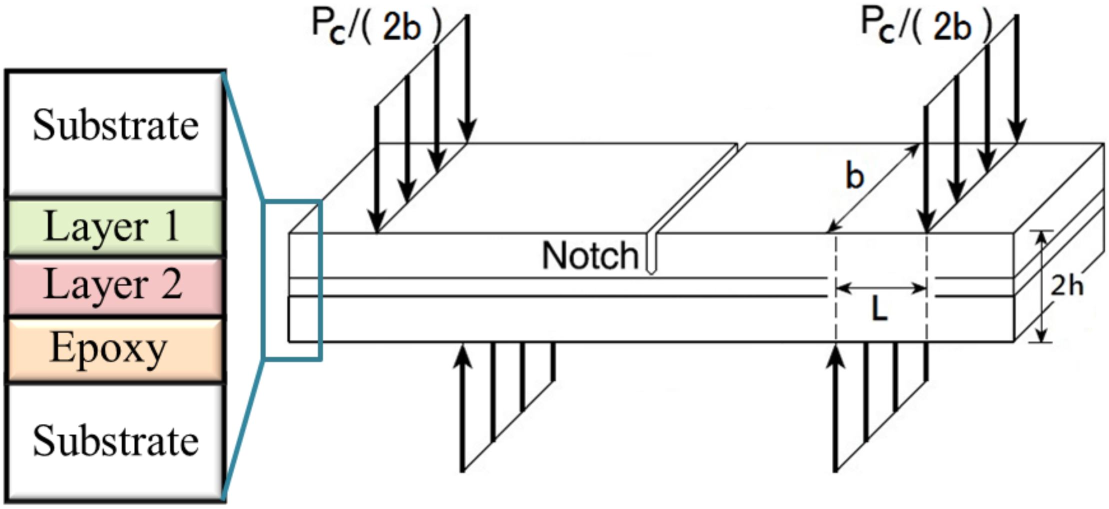


Fig. 3-4 4-point bending test setup

Group 1	*G_C (J/m^2)*
Si–BCB(3 μm)–Cu(0.2 μm)	3.39
Si–BCB(3 μm)–Ti(30 nm)–Cu(0.2 μm)	1.58
Group 2	*G_C (J/m^2)*
Si–BCB(3 μm)–Cu(1.2 μm)	2.15
Si–BCB(3 μm)–Ti(100 nm)–Cu(1.2 μm)	0.85
Group 3	*G_C (J/m^2)*
Si–Cu(1.2 μm)–BCB(3 μm)	11.2
Si–Cu(1.2 μm)–Ti(100 nm)–BCB(3 μm)	1.37

Table 3-1 Adhesion strength results of group 1, group 2, and group 3

BCB	G_C *(J/m²)*
Si–Cu (1.2 μm)–BCB (3 μm)	11.2
Si–Cu (1.2 μm)–Ti (100 nm)–BCB (3 μm)	1.37
Si–Cu (1.2 μm)–TaN (100 nm)–BCB (3 μm)	5.6
Parylene	G_C *(J/m²)*
Si–Cu (20 μm)–Parylene (3 μm)	12.75
Si–Cu (20 μm)–Ti (100 nm)–Parylene (3 μm)	0.45
Si–Cu (20 μm)–TaN (100 nm)–Parylene (3 μm)	11.21

Table 3-2 Comparison of using TaN layer and Parylene polymer

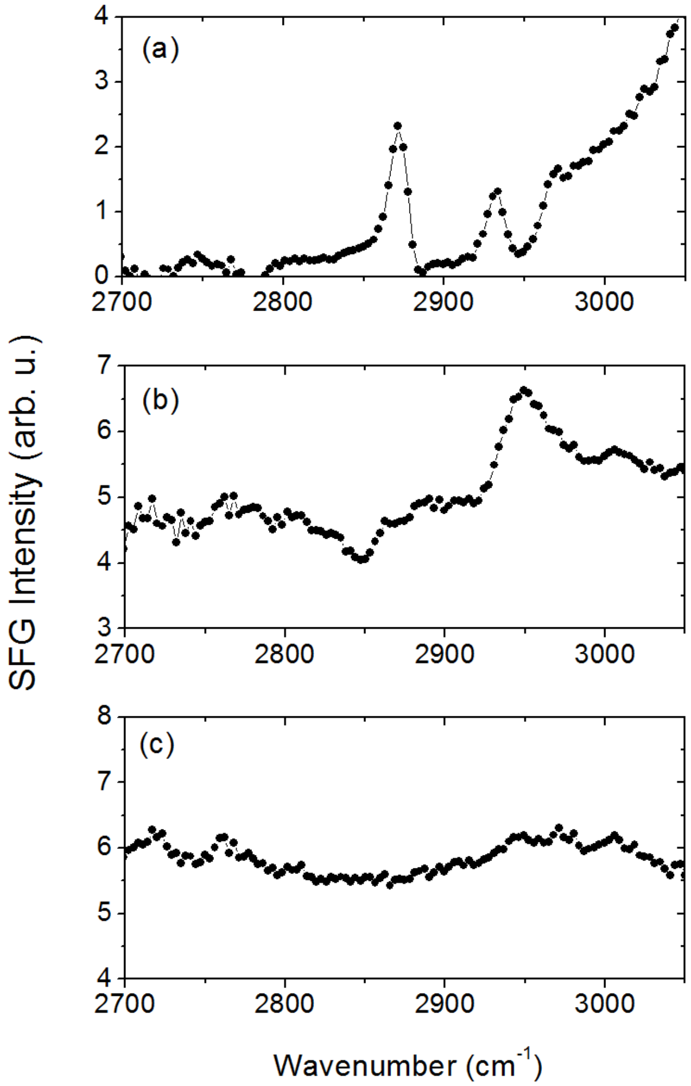


Fig. 3-5 SFG spectrum of (a) air/BCB, (b) Ti/BCB, and (c) Cu/BCB interfaces

Chapter 4
Investigations of Hetero-Bonding

4-1 Introduction

This chapter focuses on four topics: Oxide-BCB bonding, Al-Cu bonding, electrical measurement of Al-Cu Bonding, and Sn-Cu bump bonding respectively. This investigation results provide useful information for hybrid bonding development in three-dimensional integrated circuit (3D IC) applications. About material selection for this research, silicon oxide and benzocyclobutene (BCB) polymer dielectric were studied as the main materials in oxide-polymer hetero-bonding, and Al-Cu, and Sn-Cu were fabricated for different metal hetero-bonding investigation. In these hetero-bonding studies, the bonding condition and corresponding mechanism of each bonding scheme were explored. Finally, Four-terminal Kelvin test structure was fabricated to investigate the electrical characteristics and reliability of Al-Cu bonding, including AC current stressing test, DC current stressing test, and humidity test.

4-2 Oxide-BCB Bonding

4-2.1 Introduction

3D integration technology is a promising solution for enhancing chip performance, functionality, and device packing density. Hybrid bonding, one promising bonding technology in 3D IC, can provide a strong mechanical attachment and reduce the steps in the fabrication process. Among materials for hybrid bonding, oxide-polymer bonding is a new concept in 3D IC without detailed studies [23].

However, we use the polymer material BCB for this research because of its physical property and its monomer structure is shown in Fig.4-1. BCB has low dielectric constant, low moisture absorption, low cure temperature, high degree of planarization, low level of ionic contaminants, high optical clarity, good thermal stability, excellent chemical resistance, and good compatibility with various metallization systems, so it has been extensive activity in developing processing techniques. Therefore, BCB is a good candidate to be integrated with oxide in hybrid bonding. In this research, we studied the physical mechanism of oxide-polymer bonding and investigated the process flow optimization.

4-2.2 Experimental Procedure

In this research, three groups of Si wafers were deposited with 2 µm thermal oxide layer, 2 µm PECVD oxide layer, and coated 3 µm BCB polymer layer respectively. All wafers were diced into 1.0 cm × 0.7 cm chips. The principle of the bonding is that two flat, clean and smooth wafer surfaces are brought into contact and form a bonding force (Van der Waals bonds, Covalent bonds…etc.) to form Van der Waals bonds and Covalent bonds, the atoms of two opposing surfaces must be less than 0.3-0.5 nm apart. In order to bring two material surfaces in sufficient close contact to achieve bonding, at least one material surface must deform to fit the other. This deformation may be accomplished by wetting of a surface with a semi-liquid material (BCB) during the bonding. However, the surface contaminants may reduce the degree of the wetting of a surface with a liquid adhesive. Hence, surface preparations are the key element for bonding. So all wafers were cleaned for 30 minutes by DI water rinse and spin dried. Then the oxide chips (the first and second groups) were dipped in DHF for 10 seconds to remove the native oxide followed by another 30 minutes DI water rinse and spin dried.

Typically, deposition temperatures of CVD oxides are lower

(150 ℃~500 ℃) than thermal oxidation temperatures (>800 ℃). Therefore, the CVD oxide layers can be grown on surfaces that contain temperature sensitive devices. Hence, PECVD oxide is more suitable than thermal oxide in wafer bonding technology. In this research, we want to compare the bonding quality between PECVD oxide-BCB bonding and thermal oxide-BCB bonding. After surface preparation, PECVD oxide and thermal oxide samples were bonded directly to BCB samples face-to-face respectively, at 200 ℃, 250 ℃, 300 ℃, 350 ℃, and 400 ℃ for 30 and 50 min, with 1 Mpa, and in atmosphere ambient by flip chip bonder. The structural of two single side bonded samples depiction is shown in Fig. 4-2. After bonding, the bonding quality between BCB and PECVD/Thermal oxide was examined using the razor test. The bonding surface and interface were analyzed by OM and SEM [24].

Fig. 4-3–5 show the BCB surfaces after three bonding conditions: Fig. 4-3 thermal oxide-BCB bonding at 200 ℃/ 30 min; Fig. 4-4 PECVD oxide-BCB bonding at 200 ℃/ 30 min; and Fig. 4-5 PECVD oxide-BCB bonding at 400 ℃/ 30 min. BCB surfaces were investigated by breaking the bonded structure. In Fig. 4-3, the BCB surface after thermal oxide-BCB bonding at 200 ℃/ 30 min has no prominent changes. It means that the BCB surface does not interact with the thermal oxide surface.

In Fig. 4-4, the BCB surface after PECVD oxide-BCB bonding at 200 ℃/ 30 min, which failed the razor test, gathered into many of lumps. This phenomenon may represent the BCB surface beginning to bond with the oxide surface. From Fig. 4-3–4, it is apparently that the change of BCB surface after PECVD oxide-BCB bonding at 200 ℃/ 30 min is more prominent than that of BCB surface after thermal oxide-BCB bonding under same bonding conditions. As a result, PECVD oxide-BCB bonding is more easily bonded than thermal oxide-BCB bonding in same condition. Fig. 4-5 shows the BCB surface after PECVD oxide-BCB bonding at 400 ℃/ 30 min. The BCB surface also shows the similar lumps in Fig. 4-4. In addition, there is a peeling phenomenon occurring in the upper right corner of this figure. This peeling represents that the area has already been bonded together. In addition, the change in BCB surface color (brown and brittle) means the BCB chemical structure has been changed at 400 ℃ and shows a highly irregular structure with practically no links between adjacent molecules. Dark brown color and a less robust structure were the main phenomenon that the bonding would fail under this condition (400 ℃/ 30 min). Fig. 4-6 shows a well-bonded cross-section SEM image of PECVD oxide-BCB bonding interface (350 ℃/ 50 min). It is clear that the BCB chip bonded at 350 ℃ shows well-bonded results and there is no prominent bonding interface. In fact, similar bonded results can be found for oxide-BCB chips bonding between 300 ℃ and 350 ℃. To find the temperature and time optimization, all the bonded chips were analyzed by razor test.

4-2.3 Result and Conclusion

The results of razor test in Table 4-1 and 4-2 show that the quality of oxide-BCB bonding improves as the increase of bonding temperature and time until 400 ℃. Because of BCB is a thermosetting polymer, it undergoes cross-linking to form a three–dimensional network. When the bonding temperature and time increased, the cross-linked thermosetting polymer cannot flow but continue to soften until degradation occurs. This semi-liquid phase achieves sufficiently close contact with the surface to be bonded. After heating, the hardening of polymers transforms adhesive from a liquid phase into a solid material and form a force to hold two chips together. The Table 4-1 and 4-2 also show that PECVD oxide to BCB bonding is possible for 200 ℃/ 50 min and for 250 ℃/ 30 min, but for these conditions, the thermal oxide to BCB bonding fails. It is suggested that PECVD oxide to BCB bonding is superior than thermal oxide to BCB bonding under the same bonding condition. The main reason for this phenomenon is that PECVD oxide film has many more pores than thermal oxide. These pores can provide sites for the gases, trapped after bonding process, escape from the bonding interface. Therefore, the bonding strength is enhanced with the decrease of the number of bonding voids on the bonding interface. In addition, porous oxide can help water molecules generated during bonding diffuse into the silicon. In general, silicon oxide layer is terminated by Si-OH on the surface. For silicon oxide to silicon oxide bonding at high temperature, the chemical reaction can be written as [25]:

$$Si-OH+OH-Si \rightarrow Si-O-Si+H_2O \qquad (2)$$

Since the pores provide sites for water molecules continue moving from bonding interface, the chemical reaction can further continue. It means that the Si-OH group can continue interacting and producing the new stronger Si-O-Si bonds. Therefore, it not only suggests that the formation of Si-O-Si bonds is easier for porous PECVD oxide to BCB bonding than for thermal oxide to BCB bonding but also give a hint that the Si-O-Si is the main bond to connect two surfaces.

In the end, BCB chips were annealed between 325 ℃ and 450 ℃ with spacing of 25 ℃, and then analyzed by FTIR that we want to explain the reason why oxide -BCB bonding always fails at 400 ℃.

In the FTIR analysis, we have studied below 2000 cm^{-1} wavenumber regions, the so-called fingerprint of the whole molecule. Due to relatively large BCB molecule, the fingerprint region contains numerous partially overlapping peaks. Fig. 4-7 shows the FTIR analysis of BCB samples in annealing procedure. As the temperature increased from 325 ℃ to 450 ℃, the two critical peaks located at wavenumbers of 805 and 1263 cm^{-1}, which correspond to epoxy rings decreased sharply. As the temperature reached 400 ℃, the epoxy ring in BCB almost dissociated. This indicates that the cross-linking between two adjacent monomers in BCB had almost disappeared at 400 ℃, which may affect the bonding quality at this temperature [26], and this result is consistent with the razor test of oxide-BCB bonding. According to the mechanism of silicon oxide bonding [27], when BCB surface and silicon surface contact together, the water molecules form a bridge between the surfaces. During annealing these water molecules gain more surface mobility and diffuse out from the interface. During further annealing, weak silanol bonds (Si–OH) was replaced with strong siloxane-covalent bonds (Si–O–Si) by the condensation reaction, which is the proposed mechanism that BCB surface connect to the silicon oxide surface, as shown in Fig. 4-8.

In summary, FTIR analysis of BCB reveals the suitable temperature range for oxide-BCB bonding. In addition, we propose the mechanism of silicon oxide to BCB polymer surface bonding. Finally, PECVD oxide-BCB bonding is found to have better quality than that of thermal oxide-BCB bonding.

4-3 Al-Cu Bonding

4-3.1 Introduction

In this section, we try to find a good stacking approach and bonding conditions for doing the next topic – electrical measurement of Al-Cu bonding. Therefore, there have two stacking approach of Al-Cu Bonding: one is die-to-die bonding, and the other one is wafer-to-wafer bonding. In addition, we investigated Al-Cu bonding with various conditions including: bonding time, bonding temperature and with or without metal oxide cleaning before bonding. And these investigation results provide useful information for integration of Cu process and Al process applications.

4-3.2 Al-Cu Chip Bonding

4-3.2.1 Experimental Procedure

Standard RCA cleaning was applied to the wafers before 300 nm Si thermal oxide deposition. In next, Ti adhesion layer of 20 nm was deposited first, and then deposited Cu layer of 400 nm and Al layer of 400 nm by sputter and thermal coater respectively. And then, the parts of the wafers were diced into 1.0 cm × 1.0 cm chips to do chip level bonding for Al-Cu bonding conditions demo. The structural of two single side bonded samples depiction is shown in Fig. 4-9.

However, when the prepared sample is exposed in atmosphere, a considerable amount of native copper oxide will be formed on the surface. According to previous studies, copper oxide on the bonding interface would greatly affected bonding quality and bonding strength. Therefore, prior to bonding, a dilute hydrochloric acid ($HCl:H_2O=1:1$) cleaning was applied to the Cu surface for 30 sec and a 20 sec BOE ($HF:NH_4F=1:6$) cleaning was applied to the Al surface. Finally, samples were bonded face-to-face at 250 ℃, 300 ℃, 350 ℃, and 400 ℃ for 50 and 100 min, with 1 Mpa, and in atmosphere ambient by flip chip bonder. After bonding, the bonding quality between Al and Cu was examined using the razor test.

4-3.2.2 Result and Conclusion

The results of razor test in Table 4-3 shows that the quality of Al-Cu bonding improves as the increase of bonding temperature and time. By this useful information, we can modify the variable of time and temperature for Al-Cu wafer level bonding again. And the metal oxide cleaning process that a dilute hydrochloric acid ($HCl:H_2O=1:1$) cleaning was applied to the Cu surface for 30 sec and a 20 sec BOE ($HF:NH_4F=1:6$) cleaning was applied to the Al surface before bonding is good for Al-Cu chip bonding, because of the samples under the same conditions were all fail without this cleaning process.

4-3.3 Al-Cu Wafer Bonding

4-3.3.1 Experimental Procedure

All wafers are 4 inch. Just similar Al-Cu chip bonding, first standard RCA cleaning was applied to the wafer before 300 nm Si thermal oxide deposition. In next, Ti adhesion layer of 20 nm was deposited first, and then deposited Cu layer of 400 nm and Al layer of 400 nm by sputter and thermal coater respectively. The same structural with Al-Cu chip bonding of two single side bonded samples bonding depiction is shown in Fig. 4-9.

And then there were divided into two groups, the first group was doing direct wafer bonding after depositing metal layers without the metal oxide cleaning process. The second group 2 was doing the metal oxide cleaning process that a dilute hydrochloric acid ($HCl:H_2O=1:1$) cleaning was applied to the Cu surface for 30 sec and a 20 sec BOE ($HF:NH_4F=1:6$) cleaning was applied to the Al surface before wafer bonding.

The first group were bonded face-to-face at 350 ℃, and 400 ℃ for 50 min, with 1.25 Mpa, and in atmosphere ambient by EVG 520. After bonding, the well-bonded samples were analyzed by SEM, SAT, TEM, and EDX. And we modified the variable of time and temperature for Al-Cu wafer level bonding again. the second group were bonded face-to-face at 400 ℃ for 150 and 250 min, with 1.25 Mpa, and in atmosphere ambient by EVG 520. After bonding, the well-bonded samples were analyzed by SEM and SAT and compared with the first group.

4-3.3.2 Result and Conclusion

In the first group under the same bonding time 50 min, we can discover that the bonding area of 400 ℃ is bigger than 350 ℃ as shown in the SAT images of two wafer bonding samples Fig 4-10 and 11. This result also conforms to the conclusion of Al-Cu chip bonding that we investigated. Although the Al-Cu bonding interface is very well as shown in SEM image Fig. 4-12, it is not forming intermetallic compounds (IMC) between Al and Cu. As shown in Fig. 4-13–15, we can observe there has an oxide layer between Al and Cu, and we discovered that oxide is a metal oxide by EDX line scan as shown Fig. 4-16. Because of the metal oxide, Al/Cu atoms diffusing and forming IMC were prevented. Therefore, we added the metal oxide cleaning process such like chip bonding for the second group. In addition, we modified the bonding conditions again that the new conditions were extending bonding time to 150 and 250 min at 400 ℃.

In the second group, we can discover that the bonding area of 250 min is good but the 150 min one is almost fail as shown in the SAT images of two wafer bonding samples Fig 4-17–18. Although this result also conforms to the conclusion of Al-Cu chip bonding that extending bonding time can enhance the bonding quality, it is not good in the bonding interface as shown in Fig. 4-19. The possible reason is the samples uniformity becomes bad after the metal oxide cleaning, and wafers have bigger area than chips so that a poor uniformity has a great effect on wafers. Therefore, the metal oxide cleaning process is good for metal oxide removal, and chip level bonding, but it is not suitable for wafer level bonding. And in next section, we selected die-to-die stacking approach, and bonding at 400 ℃ for 50 min, with the metal oxide cleaning process.

4-4 Electrical Measurement of Al-Cu Bonding

4-4.1 Introduction

In this section, we investigated Al-Cu bonded interconnect with various electrical reliability tests including: contact resistance measurement, AC current stressing test, DC current stressing test, and humidity test.

Cu bonded interconnect with Al bonded interconnect as major bonding and conduction layer, it can be regarded as a new approach of integrated circuit fabrication such like integration of 65 nm Cu process and 0.11 μm Al special process on 3D IC applications. Therefore, in order to verify the capability of Cu-Al bonded interconnect for commercial usage and mass production, reliability test is strongly required.

4-4.2 Experimental Procedure

Standard RCA cleaning was applied to the wafers before 300 nm Si thermal oxide deposition. A thin film of HMDS was deposited, and a layer of photo-resistance of designed pattern for Kelvin structure measurement shown in Fig. 4-20 or Fig. 4-21 is developed. Ti layer of 20 nm and Pt layer of 30 nm were deposited by E-Gun Evaporation, and then deposited Cu layer of 400 nm and Al layer of 400 nm by sputter and thermal coater respectively. At last, the metal line pattern was revealed using lift-off in a micro sonic tank, and immerse in acetone. The structural of two single side bonded samples depiction is given in Fig. 4-22.

The test structure of the upper sample is in Fig. 4-20 and the lower sample is Fig 4-21. The patterned was designed for the lower layer to have a longer metal line than the upper layer, such that the metal lines of the lower layer were exposed and can served as probing pads for further measurement. The structure after bonding is shown in Fig. 4-23, and the purple area represents the bonded area. The square area of 62500 μm^2 was the test structure in the following tests. This test structure was designed according to reference which has a large tolerance of miss alignment along the y-axis (parallel to the metal lines) [18].

Because of when the prepared sample was exposed in atmosphere, a considerable amount of native copper oxide will be formed on the surface. So the metal oxide cleaning is needed prior to bonding, a dilute hydrochloric acid ($HCl:H_2O=1:1$) cleaning was applied to the Cu surface for 30 sec and a 20 sec BOE ($HF:NH_4F=1:6$) cleaning was applied to the

Al surface. Finally, samples were bonded face-to-face at 400 ℃ for 50 min, with 1 Mpa, and in atmosphere ambient by flip chip bonder.

4-4.3 Reliability Tests of Al-Cu Bonded Interconnect

4-4.3.1 Contact Resistance Measurements

The contact resistance of Al-Cu bonded interconnect was evaluated by fabricating and measuring a Kelvin structure of a bonding area subjected to 62500 μm^2. However, if we calculate the specific contact resistance of the bonded structure with the following equation:

$$\boldsymbol{\rho_C = R_C \times A_C} \qquad (3)$$

where $\boldsymbol{\rho_C}$ is specific contact resistance, $\mathbf{R_C}$ is contact resistance, and $\mathbf{A_C}$ is contact area , the value of some samples are a few orders larger than the other samples are shown in Fig. 4-24. The reasons of this great discrepancy are possible oxide formation or degradation between bonding interface and poor uniformity of our present method, which is believed to be caused by uneven bonding pressure of our bonder, and used in Eq. 3 we can observe the actual bonded area is smaller than the purposed 62500 μm^2. In addition, a typical SAT image of a well-bonded contact area is given in Fig. 4-25, with the dark area as the bonded area and vice versa.

However, we select the samples which have the lowest contact resistance to measure AC and DC current stressing test, because of it have the most sensitive various.

4-4.3.2 AC Current Stressing Test

The stability of the bond structure is significant for 3D integration applications, especially its electrical performance after multiple operations. Therefore, the Al-Cu bonded structures were evaluated for stability against current stressing, with each cycling consists of a sweeping of current from -10 mA to 10 mA. The average contact resistance after multiple loops of current stressing were measured and shown in Fig. 4-26. It is shown that the deviation of resistance is small within the entire range of 1000 current stressing loops. This result implies that the bonded contact is stable and could also endure a long term of electrical current.

4-4.3.3 DC Current Stressing Test

A DC current stressing test for 24, 48, 72, 96, and 120 hours were applied to the bonded interconnects, with stressing current density of

3.2×10^2 A/cm^2. The contact resistance had been recorded after each period of time, and the resistance changes are shown in Fig. 4-27. We can discover that the resistance deviations in Fig. 4-27 are very small. The result suggests that the structure was stable under large current density and could stand for long operating time. This is an important indicator for structure reliability, since most interconnect is concerned for its electro-migration resistance. Same as the AC current stressing case, the stability of the bond structure is significant for 3D integration applications, especially its electrical performance after multiple operations. However, the endurance under DC current stressing is a more major concern. In the AC current stressing case, the structure is likely to recover the defects with the alternation applied current. DC current stressing, on the other hand, can be more truthful of showing the reliability of the structure. In our case, the results of DC and AC current stressing test both prove that the structure is stable and has a high resistance toward electro-migration.

4-4.3.4 Humidity Test

Humidity test is subjected to evaluate the effect of moist to the test subject. Depending on the absorbing rate of moist of the material, and the interaction of the material to moist, the resistance of material against moist can be analyzed. Humidity test is done by placing a sample in an environment of high humid and temperature, in order to simulate an accelerated aging condition to the sample.

A humidity test of 50 ℃ and 100% RH was performed on the Al-Cu structure for 24, 72, 120, and 168 hours, and the two results of different initial contact resistances are shown in Fig. 4-28–29. One was using the sample which has a lower contact resistance for this test, and the other one was using a bigger contact resistance sample to compare each other. According to the results, the contact resistances of both samples were not stable within the whole test. The samples may be deterioration and oxidation in the bond interface. Therefore, it is implied that the bonding quality becomes bad. So these samples do not have a good resistance to moisture and heat ability.

4-5 Sn-Cu Bump Bonding

4-5.1 Introduction

3D IC of using TSV technology has several advantages. For instance, we can achieve reducing the delay time, heterogeneous integration, and increasing I/O port number. Yield enhancement will be done in future and has benefits of reducing cost. Development of TSV technology has been a trend in the semiconductor industry. We have experienced a difficult years of size miniaturization, three-dimensional integrated circuits can be said that one of the solution. Therefore, we must develop TSV technology.

This section focuses on sealing bump bottom-up plating method that belongs to via last process. However, the sealing Sn-Cu bump bottom-up plating scheme has been demonstrated including Sn-Cu bump bonding process. These studies provide useful information for package process development in 3D IC applications. In additional, TSV diameter can achieve 50 µm with 200 µm thick.

4-5.2 Experimental Procedure

Detail of sealing bump-up plating process is demonstrated in Fig. 4-30. We select thick photoresist as hard mask. The lithography process is using to 50 μm TSV opening. The wafer is sent to do photoresist coating by spin coater as shown in Fig. 4-30 (a) and do soft baking to remove out of the excess solvent to increase the adhesion of photoresist on the wafer after coating and then use double side mask aligner do exposure as shown in Fig. 4-30 (b), and then to do developing, fixing, and hard baking. In Fig. 4-30 (c), TSV holes are etched by ICP etching process. After using lift-off in a micro sonic tank, and immerse in acetone to remove thick photoresist, we send wafer to do thinning process down to 200 μm as shown in Fig. 4-30 (d) and (e). In Fig. 4-30 (f), TEOS with thickness of 1.5 μm is deposited on front side and sidewall to as insulation layer. In older to completely fabricate TSV have perfect insulation, back side of wafer also need to deposit TEOS with thickness of 1.5 μm as shown in Fig. 4-30 (g). In next, a Ti adhesion layer with thickness of 20 nm and a Cu seed layer with thickness of 300 nm are sputtered onto the front side of the wafer as shown in Fig. 4-30 (h). Then, all wafers were diced into 1.0 cm × 1.0 cm chips along the edge of patterns. And next step, we put the chips into plating bath and electroplate sealing cap to do bottom-up plating that forms Cu TSVs and Cu bumps with DC power which have faster sealing ability as shown in Fig. 4-30 (i) and (j). In addition, parts of the samples continue to electroplate Sn as shown in Fig. 4-30 (k). Finally, the chip which contains TSVs with Sn-Cu micro-bumps is bonding with another chip which contains TSVs with Cu micro-bumps by flip chip bonder as shown in Fig. 4-30 (l).

4-5.3 Result and Conclusion

In order to make sure there has no defect in this sealing bump bottom-up process, we used SEM and EDX to analyze. The SEM image of top view that is etched TSVs with diameter of 50 μm as shown in Fig. 4-31, and the SEM images of cross-section that has deposited TEOS with thickness of 1.5 μm as shown in Fig. 4-32–34 before Cu-filling. We can discover the TSV has smooth sidewall and TEOS was fully deposited on the edge of TSV, so we can make sure there has no leakage current from Si substrate when we do the electroplated process.

After the thin film process that TEOS was deposited in the front side and back side, we begin to prepare the plating process, Before seal electroplating, the wafers has been deposited 20 nm titanium adhesion layer and 300 nm copper seed layer on front side by sputter and been diced into 1.0 cm × 1.0 cm chips. Then, we can put the chips into plating bath and electroplate sealing cap as shown in Fig. 4-35. And then the bottom-up plating process begins forming Cu TSV and Cu bump with a stable DC power supply soon. The parts of the samples continue to electroplate Sn, and the cross-section images of a complete TSV module that is fabricated by sealing Sn-Cu bump bottom-up plating are shown in Fig. 4-36–39. From these SEM images, we can clearly observe there has no defect in this sealing bump and TSV, and good insulation layer in TSV sidewall. In addition, the SEM images of the Sn-Cu bumps and Cu bumps 45° tilt view are shown in Fig. 4-40–41. Because of the uniformity of these bumps is pretty good, so we can begin the Sn-Cu bonding process. After checking the above process were defects-free, the chip which contains TSVs with Sn-Cu micro-bumps is bonding with another chip which contains TSVs with Cu micro-bumps by flip chip bonder, bonding at 350 ℃ for 50 min, with 1 Mpa, and in atmosphere ambient. The bonding result is shown in Fig. 4-42. We can observe the good bonding quality of Sn-Cu bump bonding from Fig. 4-42, and make double check the Sn-Cu-Sn structure was well-bonded by EDX as shown in Fig. 4-43.

Although this experiment is just a demo of sealing Sn-Cu bump bottom-up, it is really useful in 3D IC applications. This process had several advantages, for some examples: it is only using general PCB electroplating machine to achieve fast and void-free bottom-up filling, and did not need additive like accelerator, leveler, and suppressor, so that it can be cost down. Because of all front side and back side had deposited same thickness and material film, so it has less stress and warpage in the chip, and use copper and tin bump to achieve low temperature bonding application.

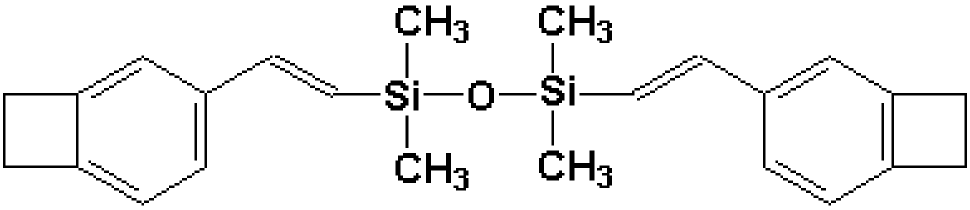


Fig. 4-1 BCB monomer chemical structure

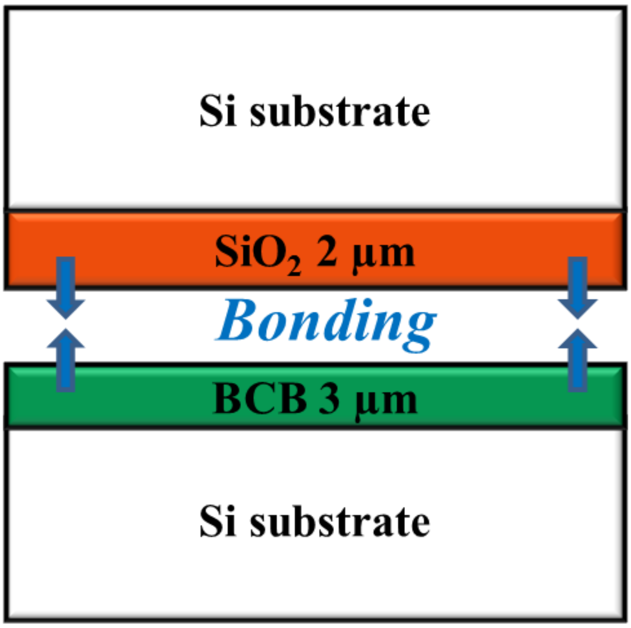


Fig. 4-2 Oxide-BCB bonding structure of two single side bonded samples

Fig. 4-3 OM image of BCB polymer surface after BCB to thermal oxide bonding at 200 ℃/ 30 min

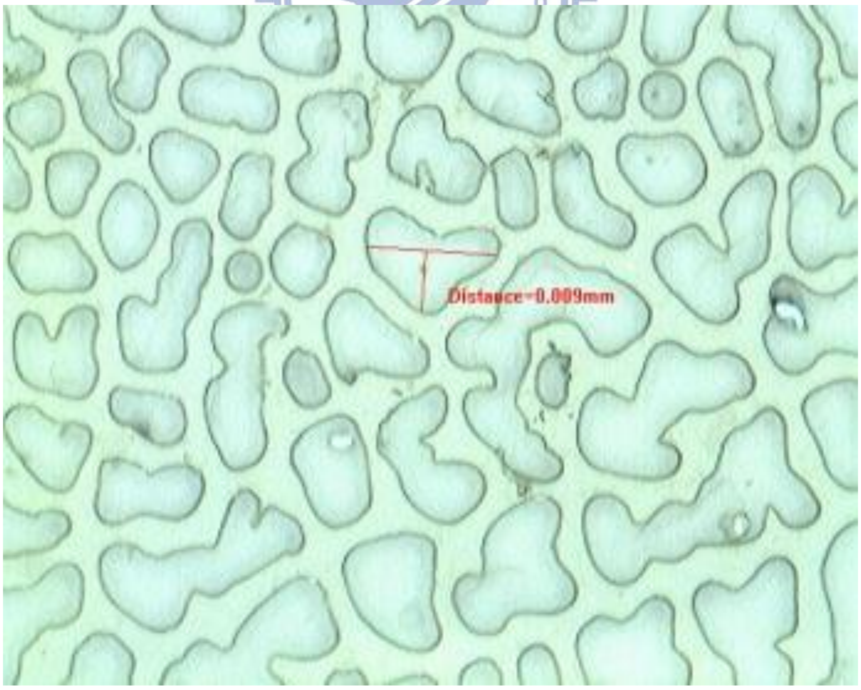


Fig. 4-4 OM image of BCB polymer surface after BCB to PECVD oxide bonding at 200 ℃/ 30 min

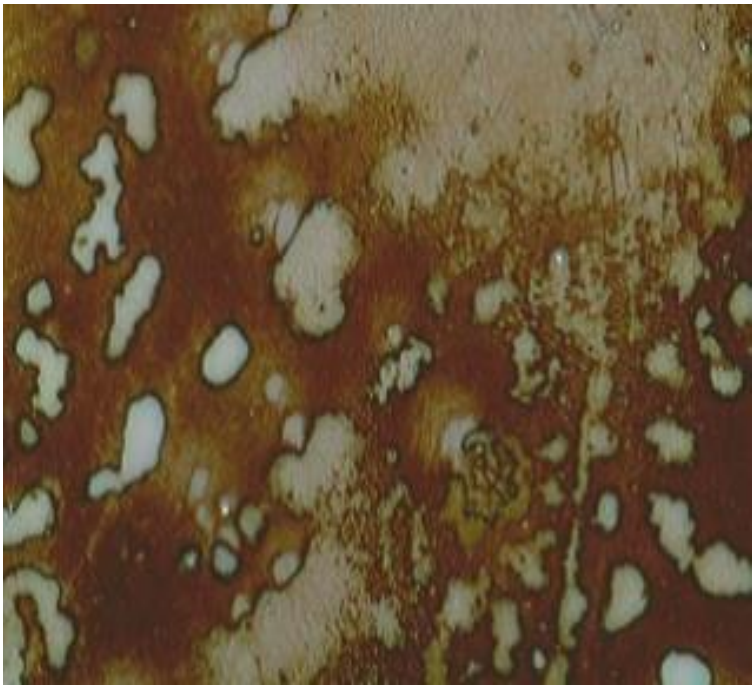


Fig. 4-5 OM image of BCB polymer surface after BCB to PECVD oxide bonding at 400 ℃/ 30 min

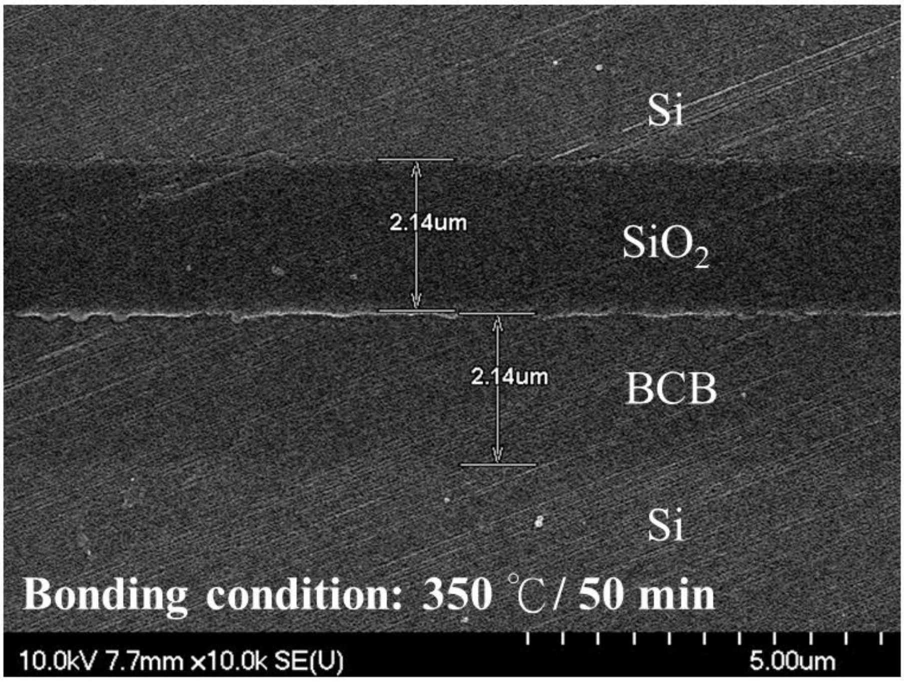


Fig. 4-6 SEM image of BCB to PECVD oxide bonding interface

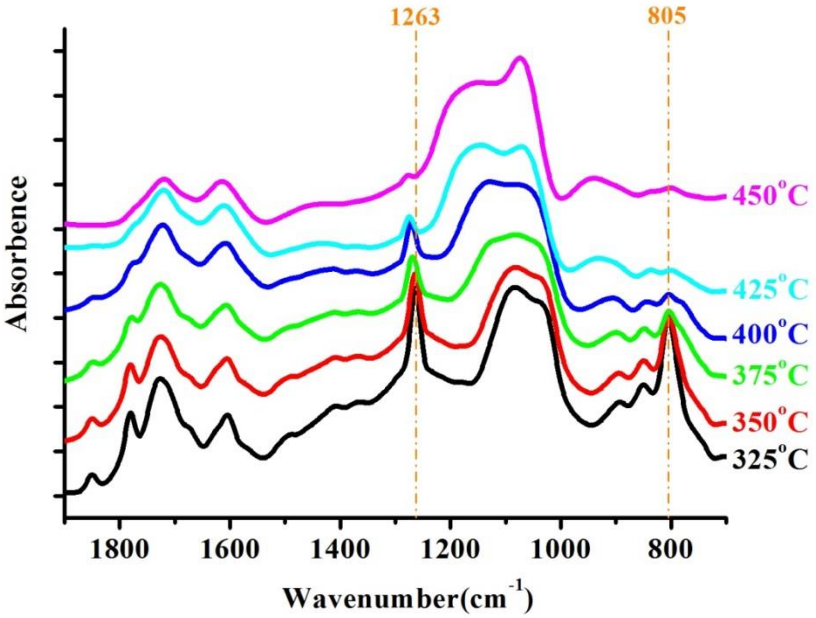


Fig. 4-7 FTIR diagram of annealing BCB polymer surface structure for

325 ℃, 350 ℃, 375 ℃, 400 ℃, 425 ℃, and 450 ℃

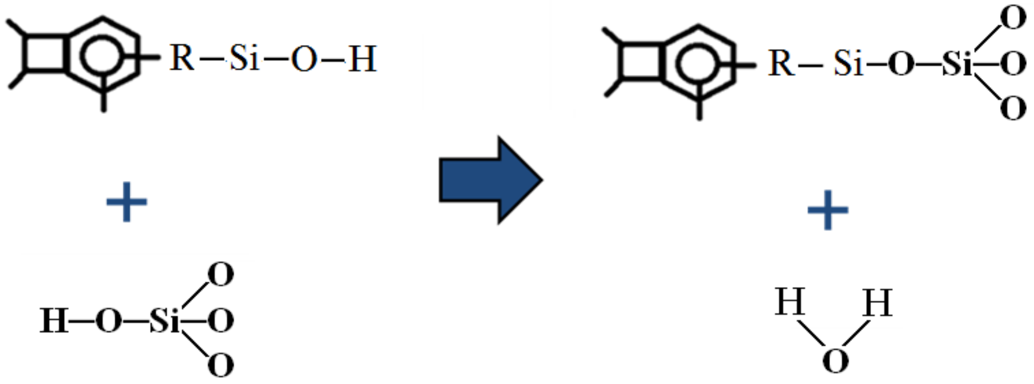


Fig. 4-8 The proposed mechanism of silicon oxide surface-BCB polymer surface bonding

Temp. Time	200 ℃	250 ℃	300 ℃	350 ℃	400 ℃
30 min	X	O	O	O	X
50 min	O	O	O	O	

Table 4-1 Results of PECVD oxide-BCB bonding razor test

Temp. Time	200 ℃	250 ℃	300 ℃	350 ℃	400 ℃
30 min	X	X	O	O	X
50 min	X	O	O	O	

Table 4-2 Results of thermal oxide- BCB bonding razor test

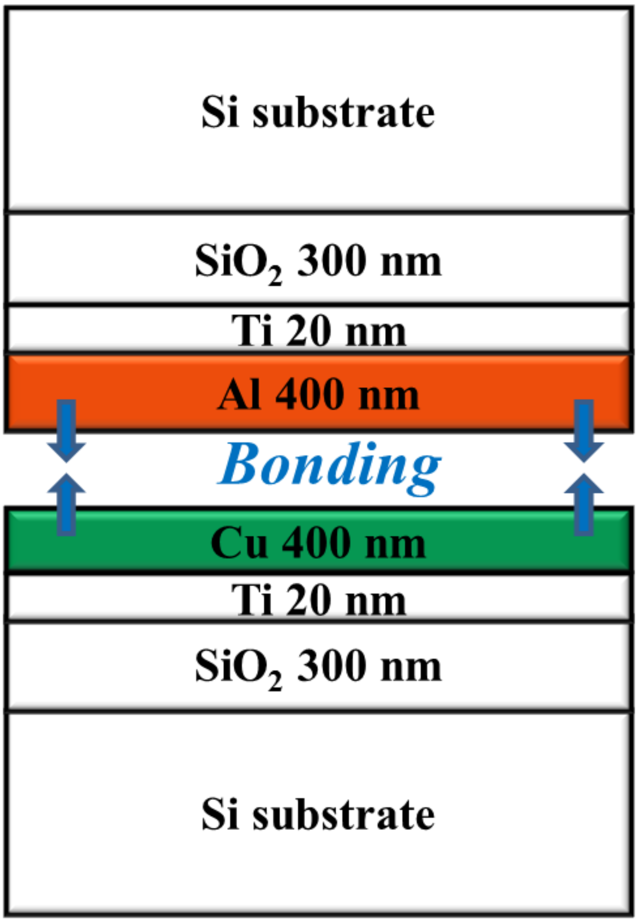


Fig. 4-9 Al-Cu Bonding structure of two single side bonded samples

Temp. Time	250 ℃	300 ℃	350 ℃	400 ℃
50 min	O	X	O	O
50 min	X	O	X	O
100 min	O	O	O	O

Table 4-3 Results of Al-Cu bonding razor test

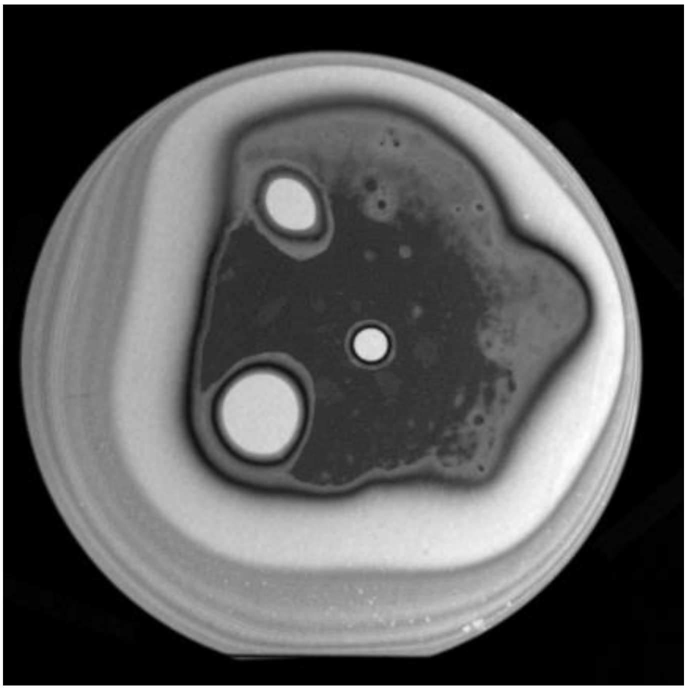


Fig. 4-10 SAT image of Al-Cu bonding at 350 ℃ for 50 min,

with 1.25 Mpa by EVG 520

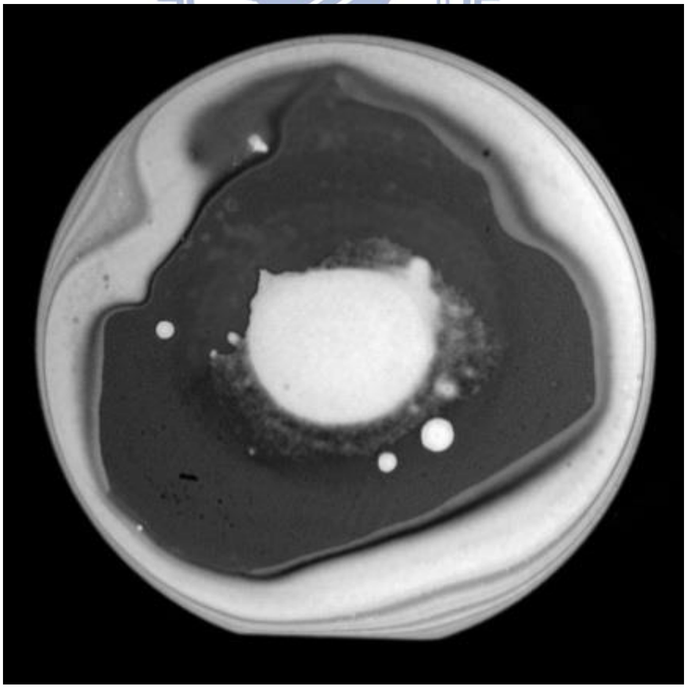


Fig. 4-11 SAT image of Al-Cu bonding at 400 ℃ for 50 min,

with 1.25 Mpa by EVG 520

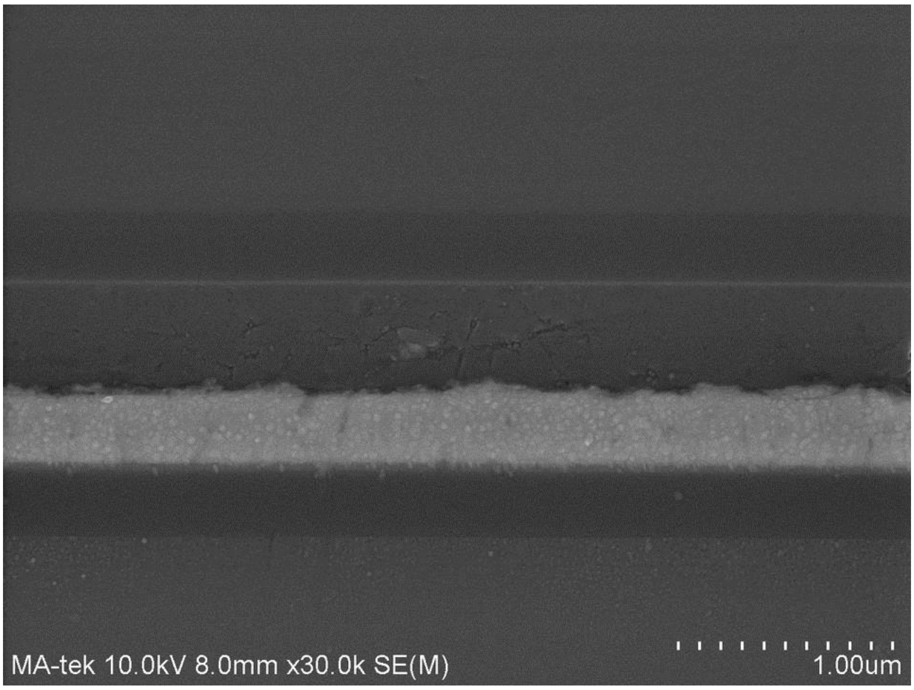


Fig. 4-12 SEM image of Al-Cu bonding cross-section at 400 ℃ for 50 min, without metal oxide cleaning

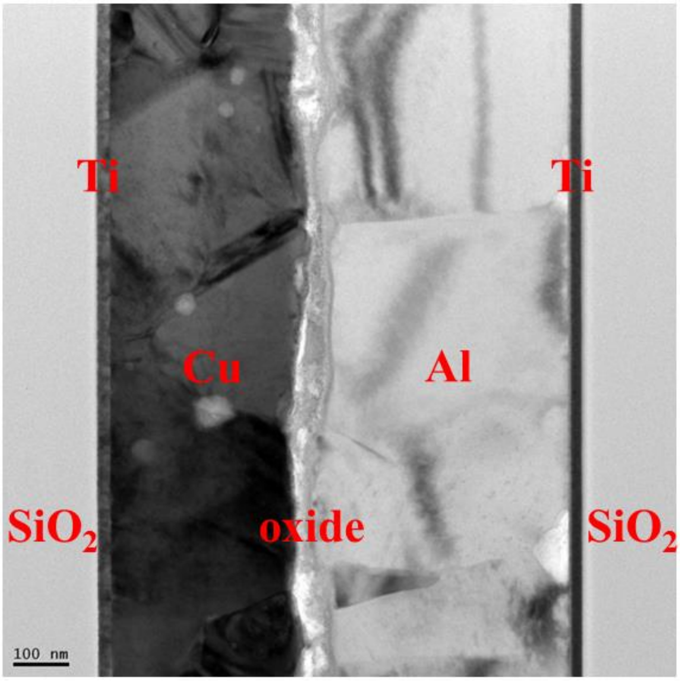


Fig. 4-13 TEM image of Al-Cu bonding cross-section at 400 ℃ for 50 min, without metal oxide cleaning

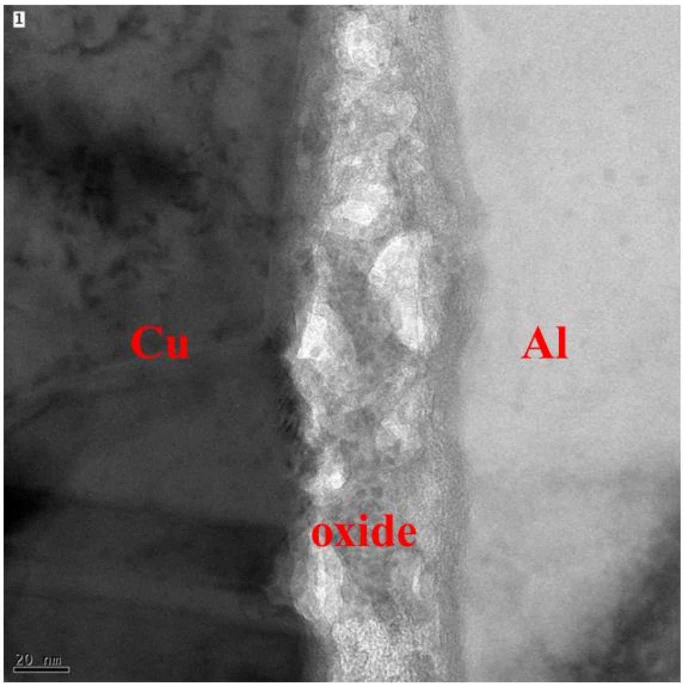


Fig. 4-14 TEM image of Al-Cu bonding cross-section at 400 ℃ for 50 min, without metal oxide cleaning (Zoom in)

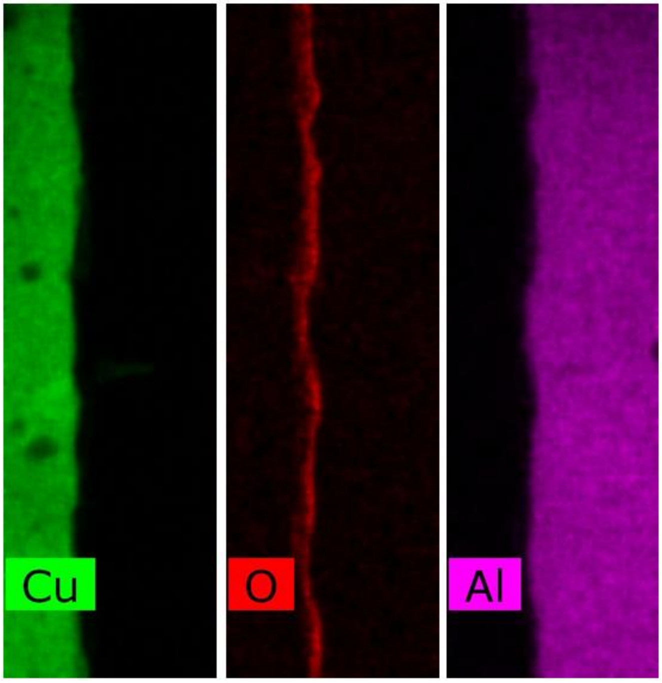


Fig. 4-15 EDX mapping of Al-Cu bonding cross-section at 400 ℃ for 50 min, without metal oxide cleaning

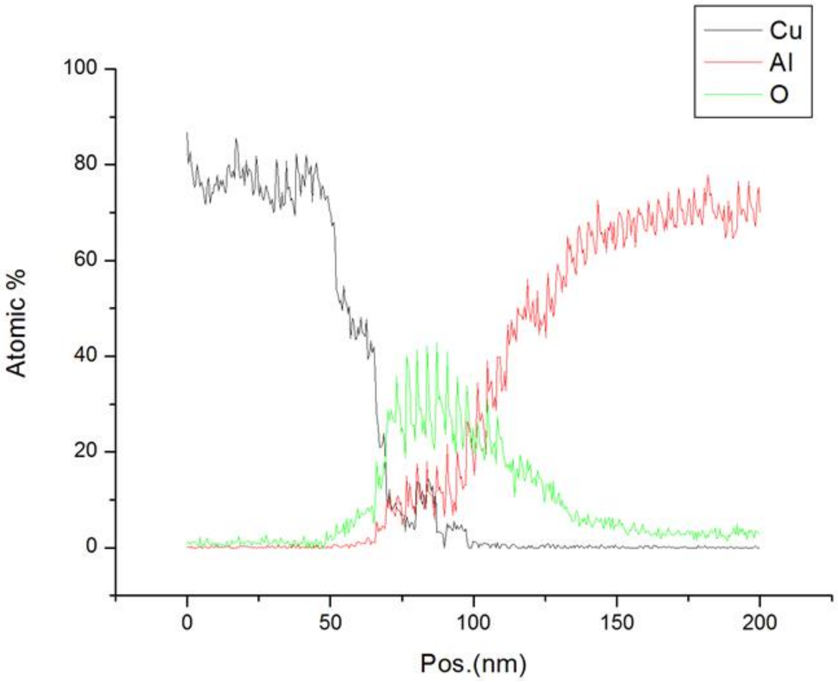


Fig. 4-16 EDX line scan of Al-Cu bonding cross-section at 400 ℃ for 50 min, without metal oxide cleaning

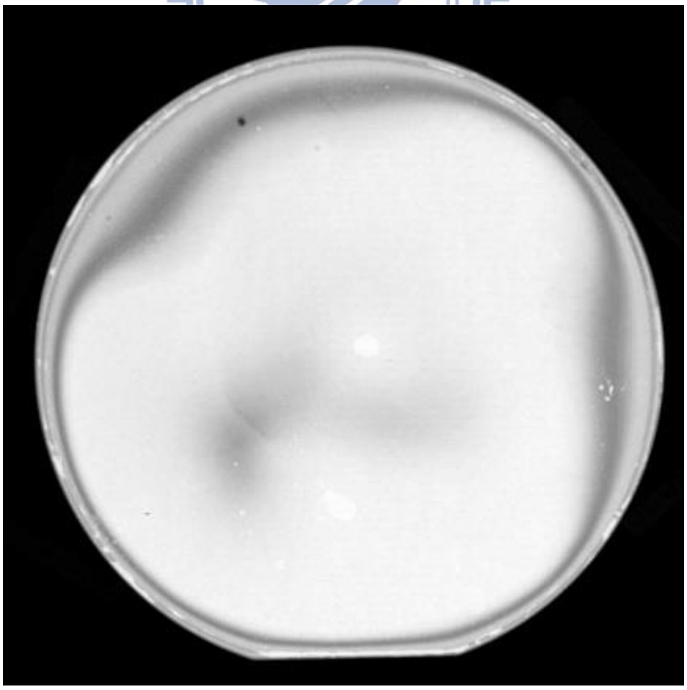


Fig. 4-17 SAT image of Al-Cu bonding at 400 ℃ for 150 min, with 1.25 Mpa by EVG 520

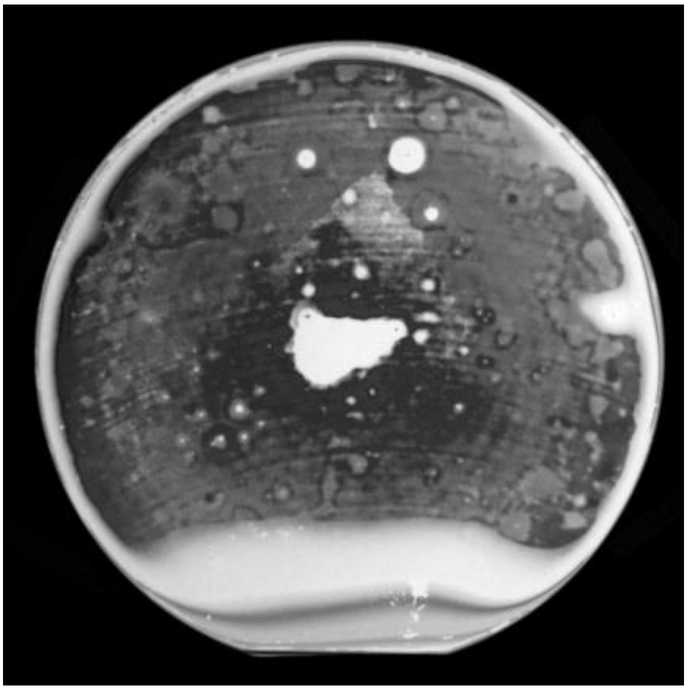


Fig. 4-18 SAT image of Al-Cu bonding at 400 ℃ for 250 min, with 1.25 Mpa by EVG 520

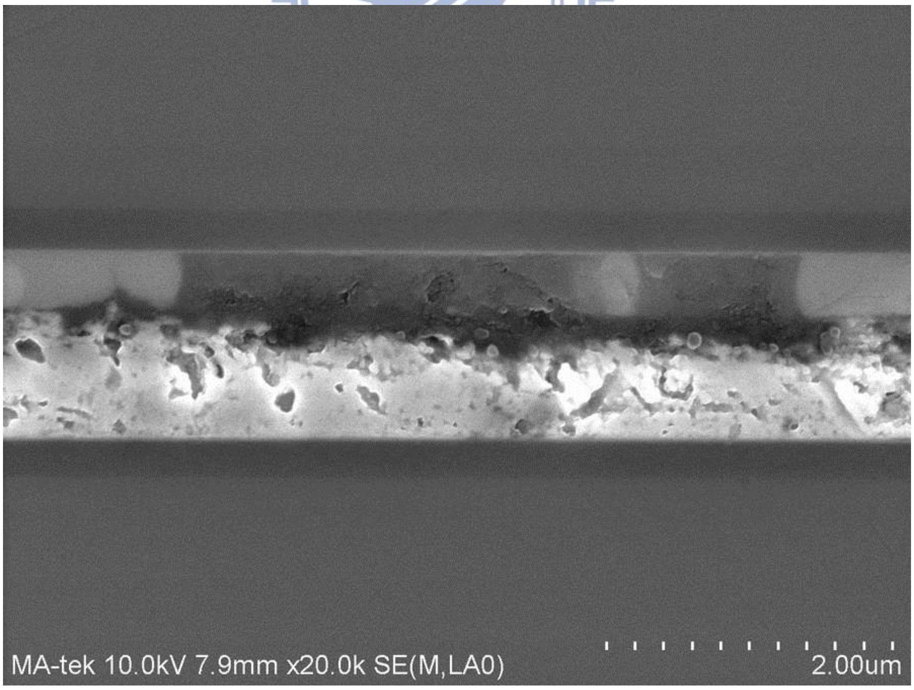


Fig. 4-19 SEM image of Al-Cu bonding cross-section at 400 ℃ for 250 min, with metal oxide cleaning

Fig. 4-20 Mask for the top bonding sample

Fig. 4-21 Mask for the bottom bonding sample

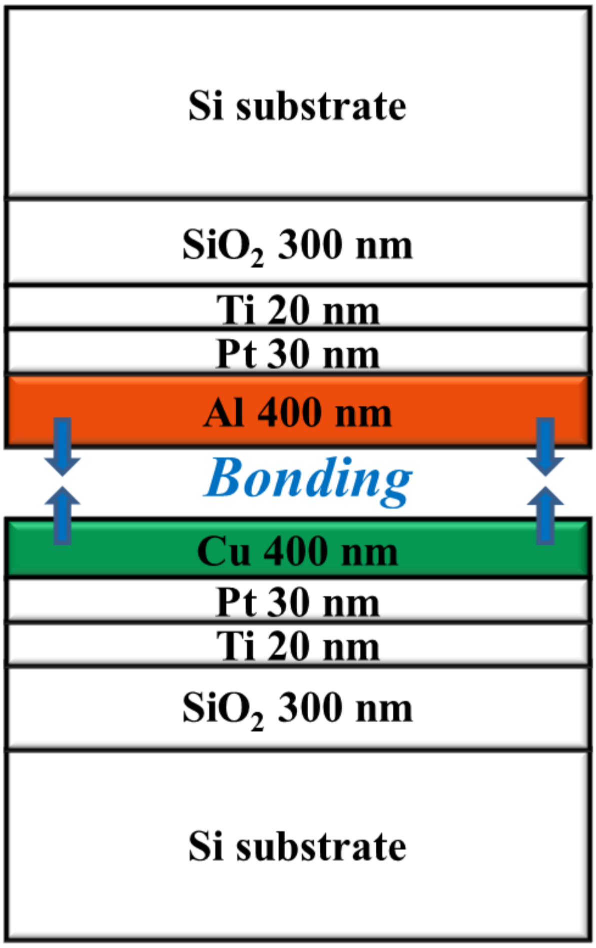


Fig. 4-22 Electrical measurement of Al-Cu Bonding structure of two single side bonded samples

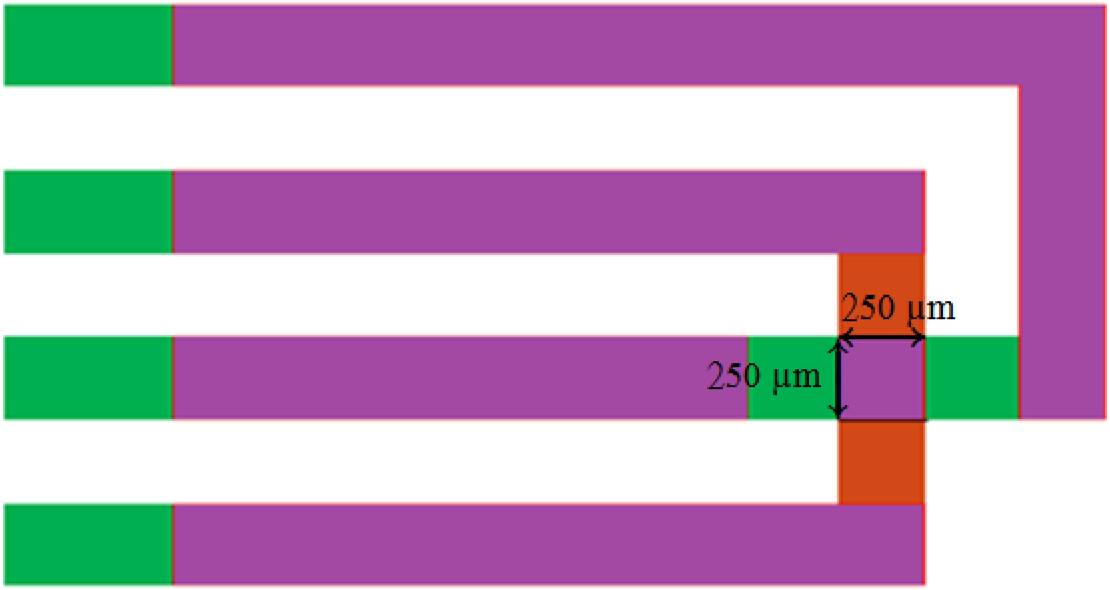


Fig. 4-23 Schematics for the bonded sample

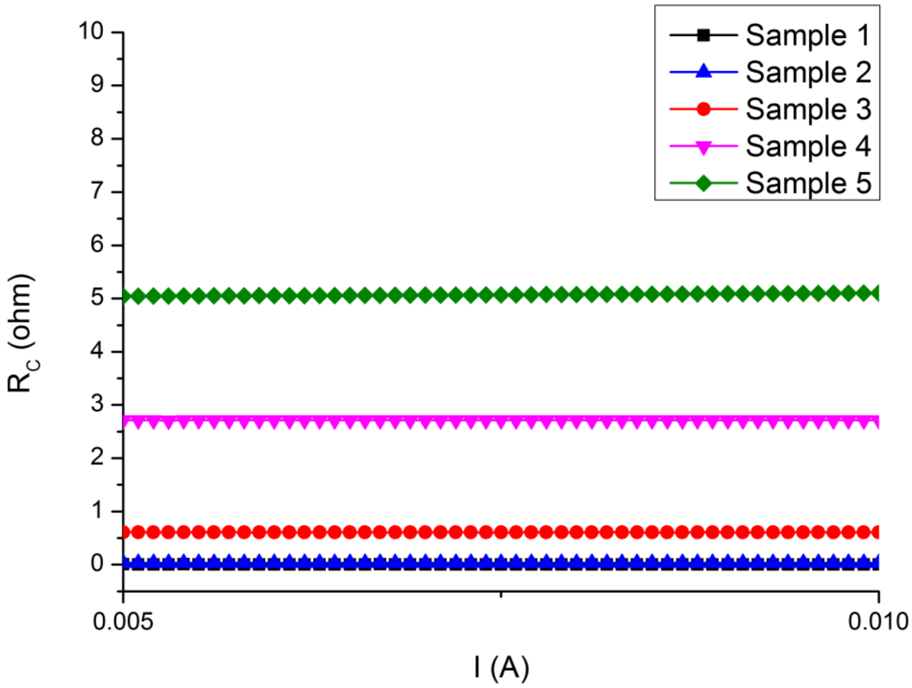


Fig. 4-24 Samples selection for experiment

Fig. 4-25 A SAT image of a well-bonded sample

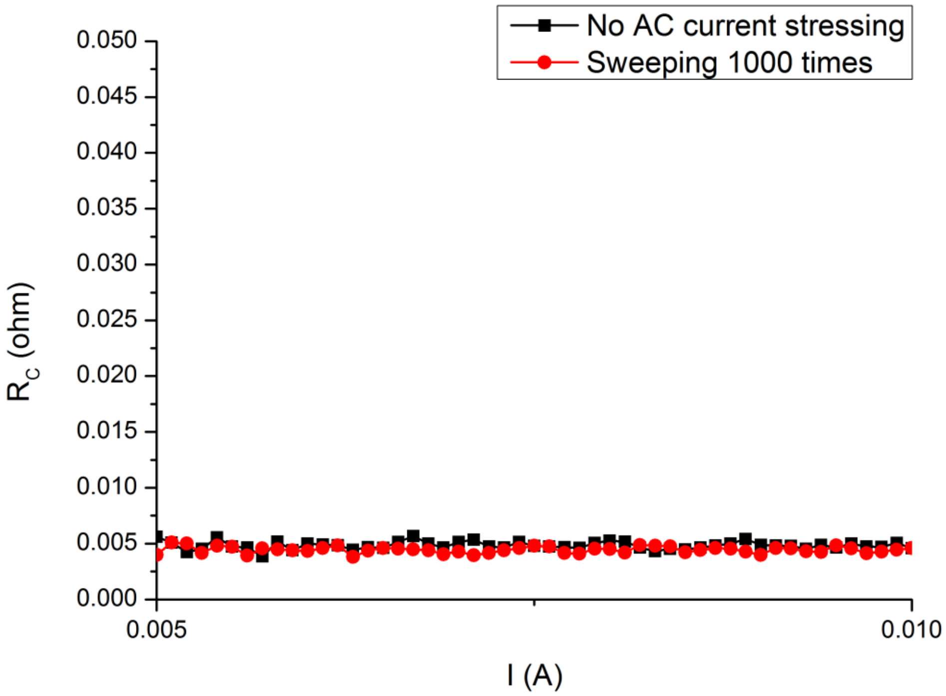


Fig. 4-26 AC current stressing (-10 mA to 10 mA)

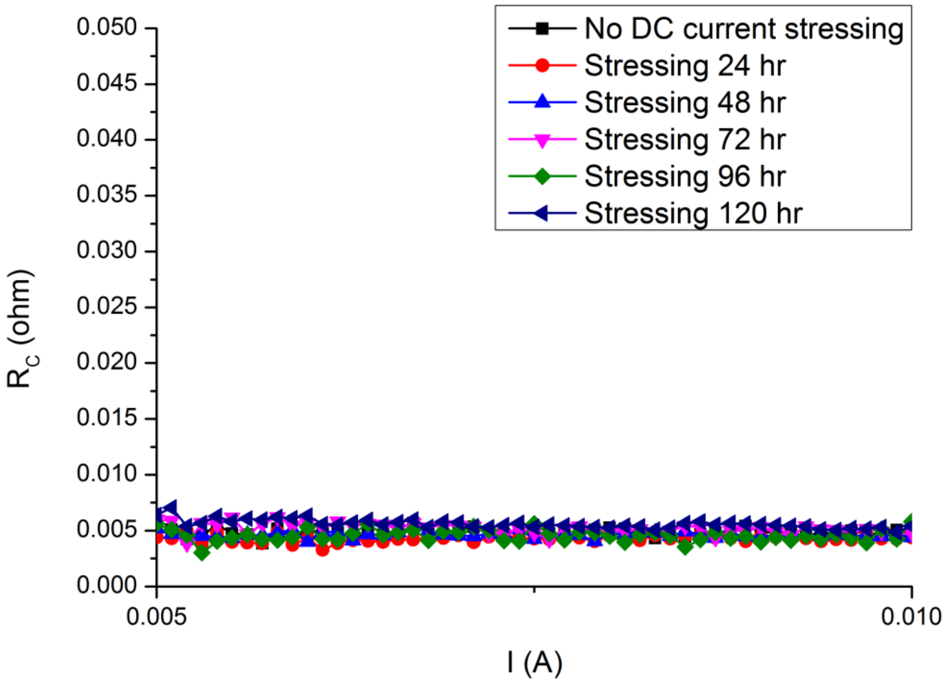


Fig. 4-27 DC current stressing (3.2×10^2 A/cm^2)

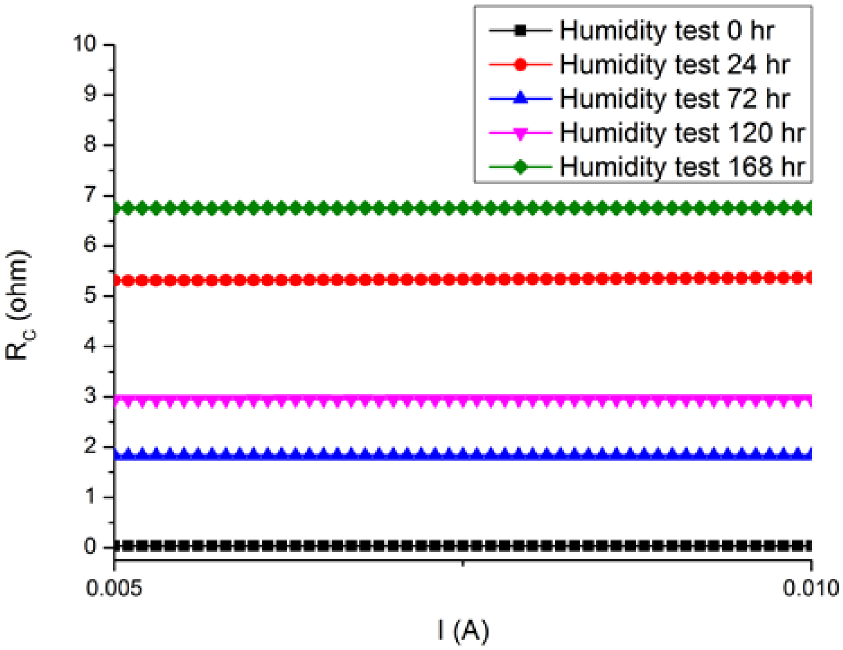


Fig. 4-28 Humidity test (Initial contact resistance: 0.035 Ohm)

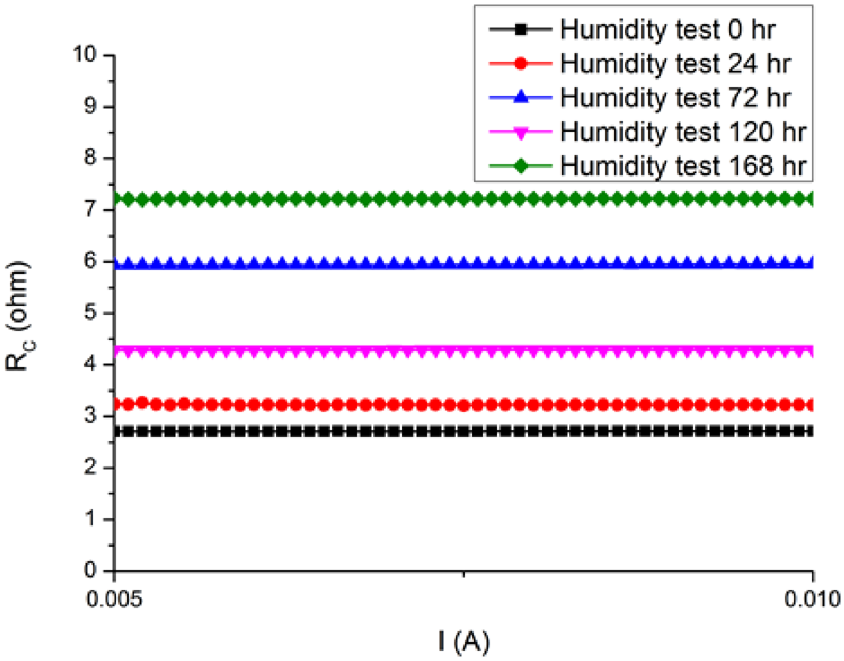


Fig. 4-29 Humidity test (Initial contact resistance: 2.7 Ohm)

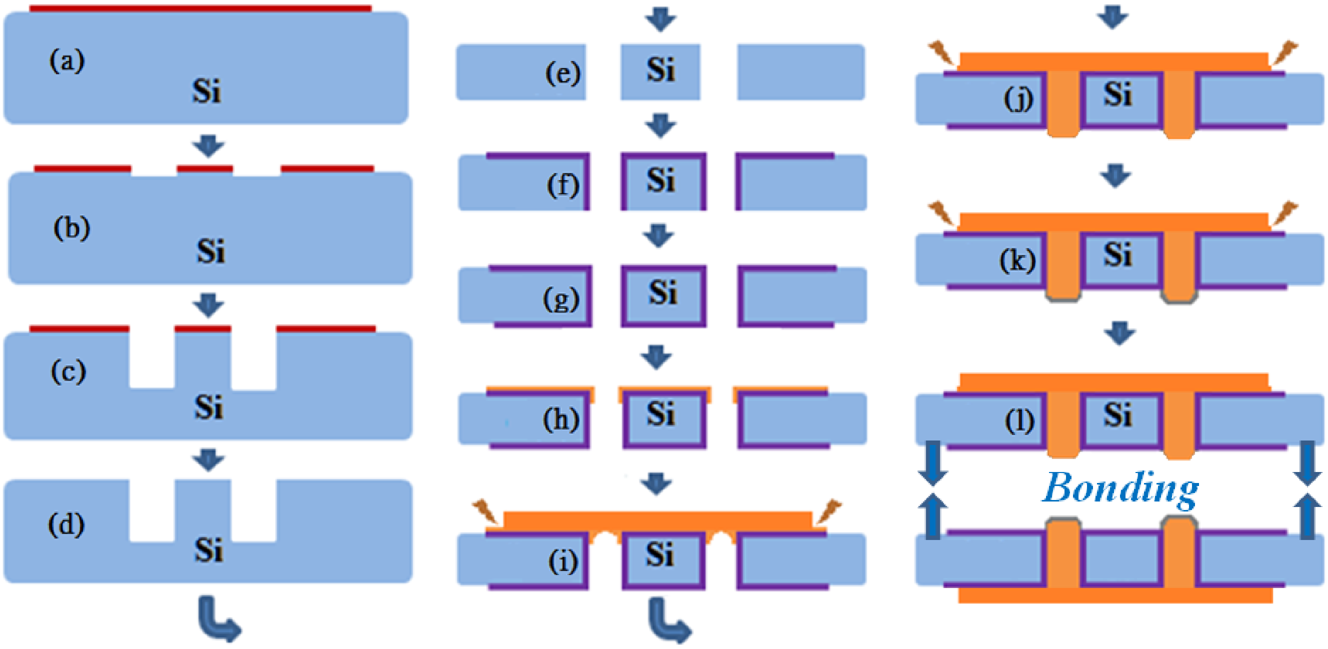


Fig. 4-30 Process flow of sealing bump bottom-up plating method including Sn-Cu bump bonding

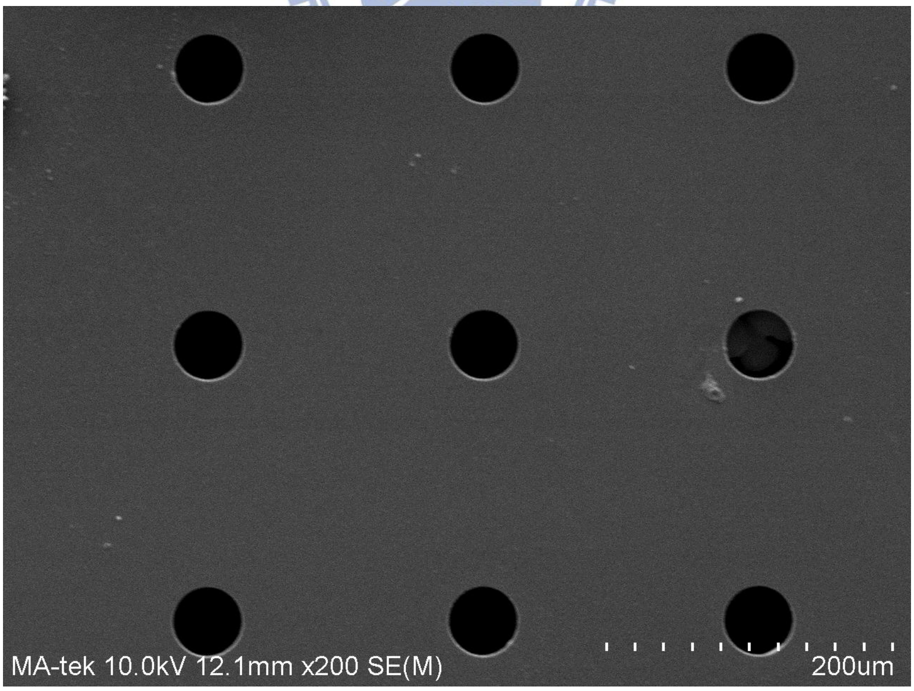


Fig. 4-31 SEM images of TSVs top view

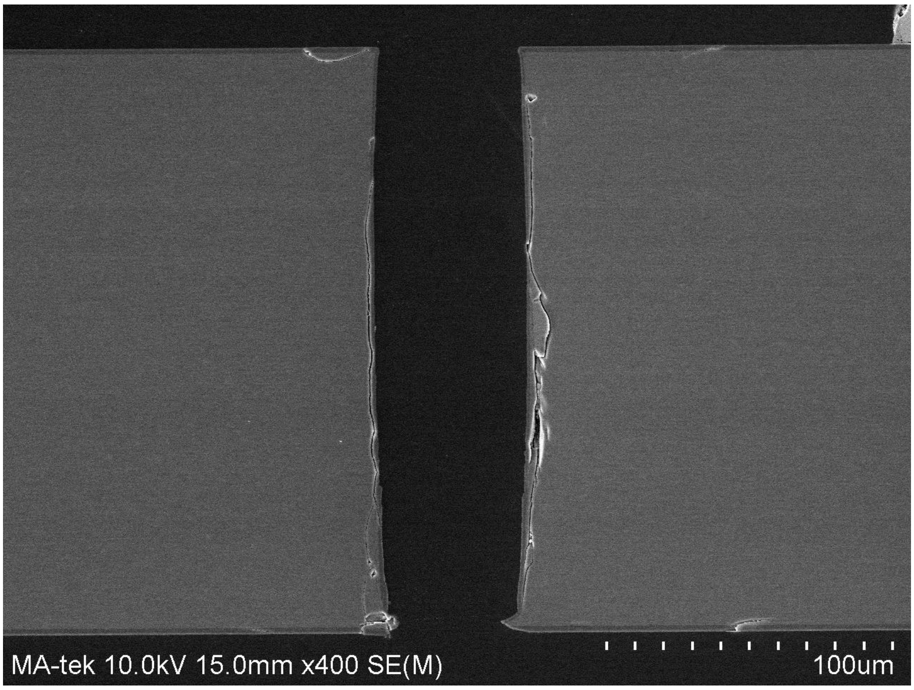


Fig. 4-32 SEM images of cross-section that has deposited TEOS on TSV sidewall

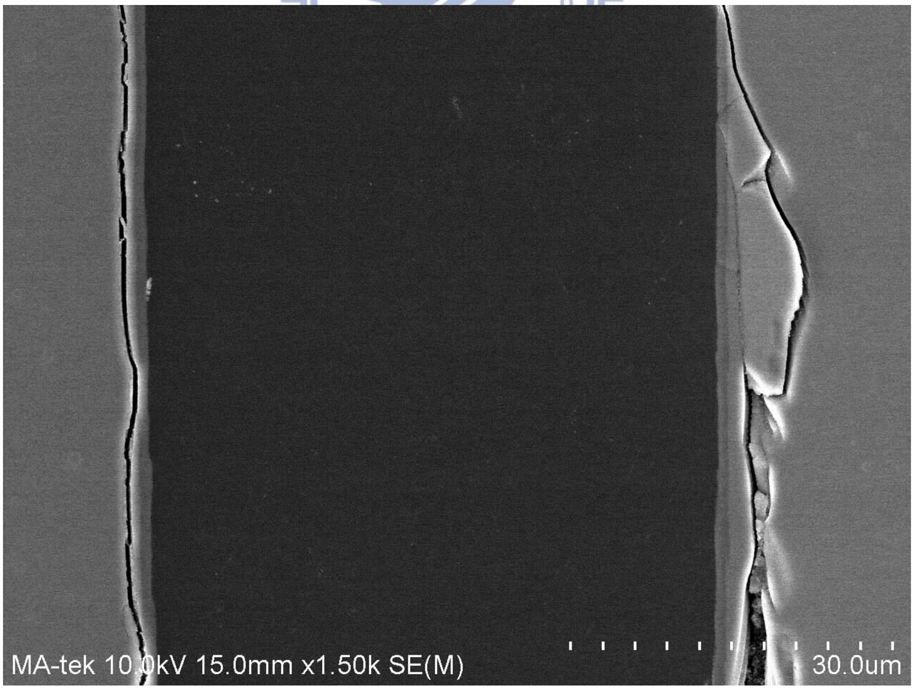


Fig. 4-33 SEM image of cross-section that has deposited TEOS on TSV sidewall (Zoom in)

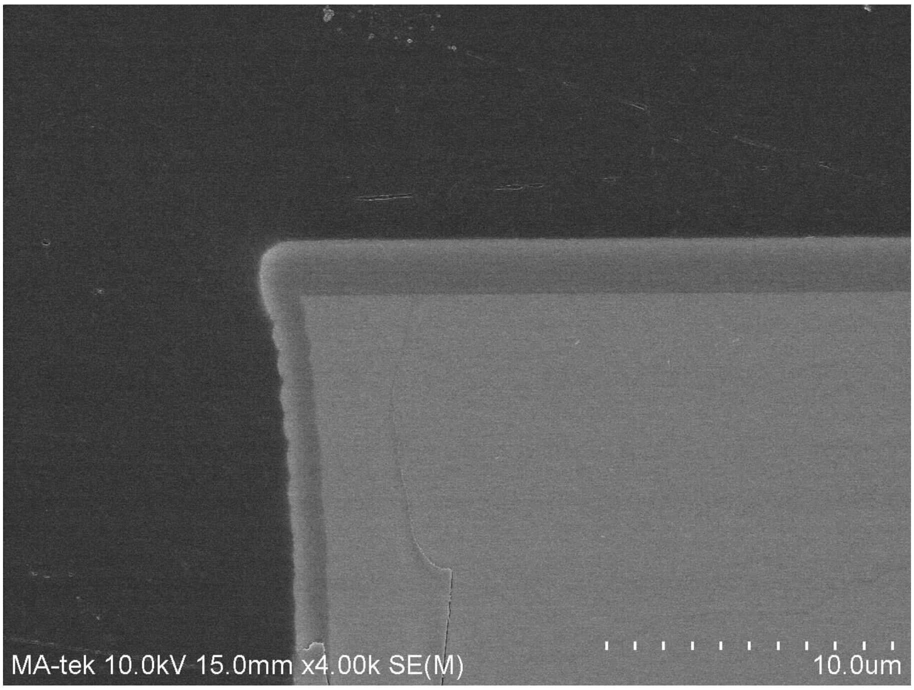


Fig. 4-34 SEM image of cross-section that has deposited TEOS on TSV sidewall and front side

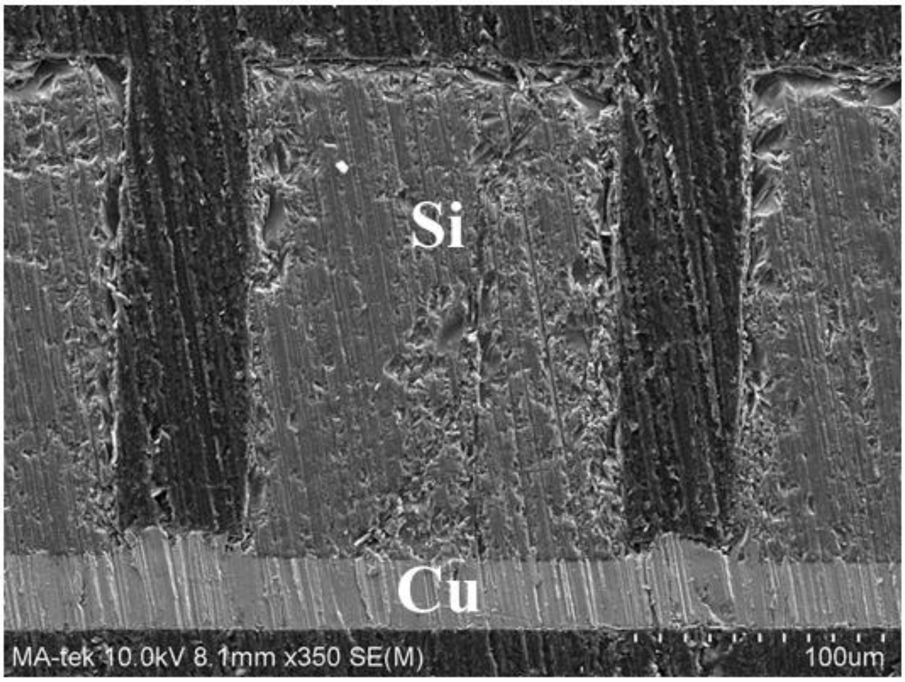


Fig. 4-35 SEM image of cross-section that is shown the electroplating sealing caps for forming Cu TSVs

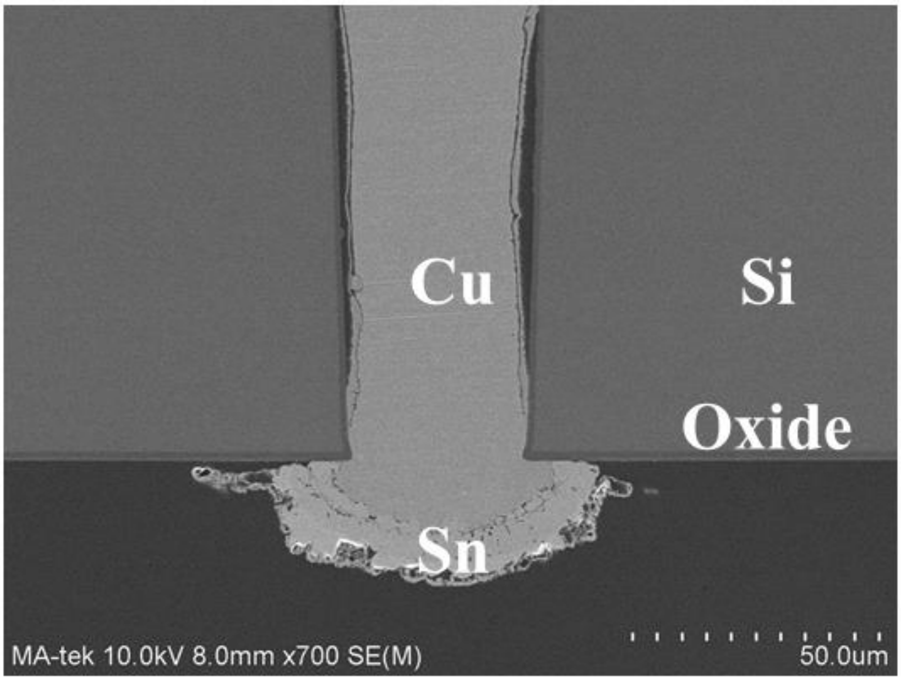


Fig. 4-36 A cross-section image of a complete TSV module which has sealing Sn-Cu bump bottom-up

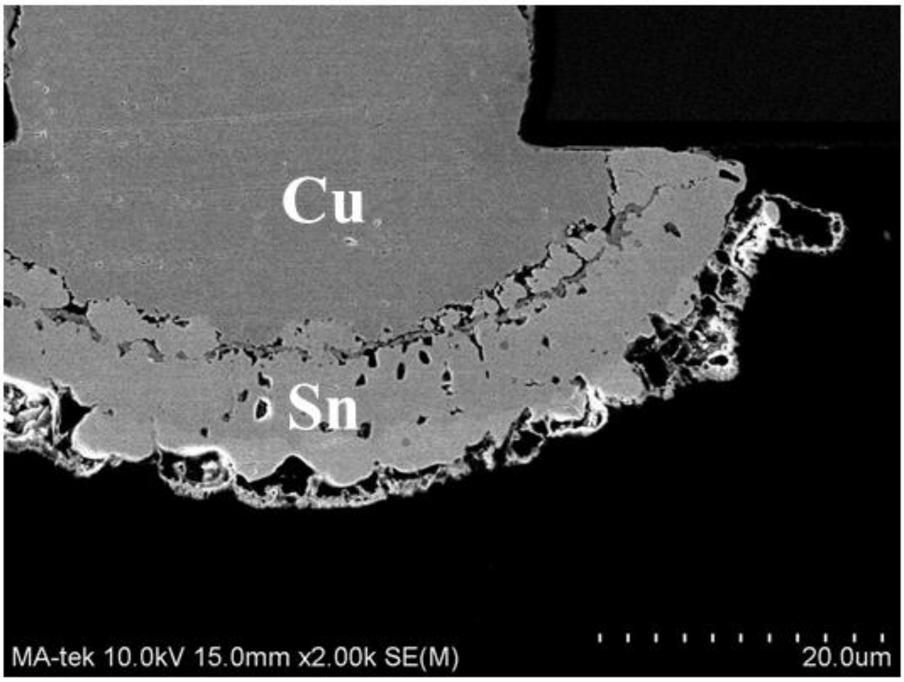


Fig. 4-37 A cross-section image of a complete TSV module which has sealing Sn-Cu bump bottom-up (Zoom in)

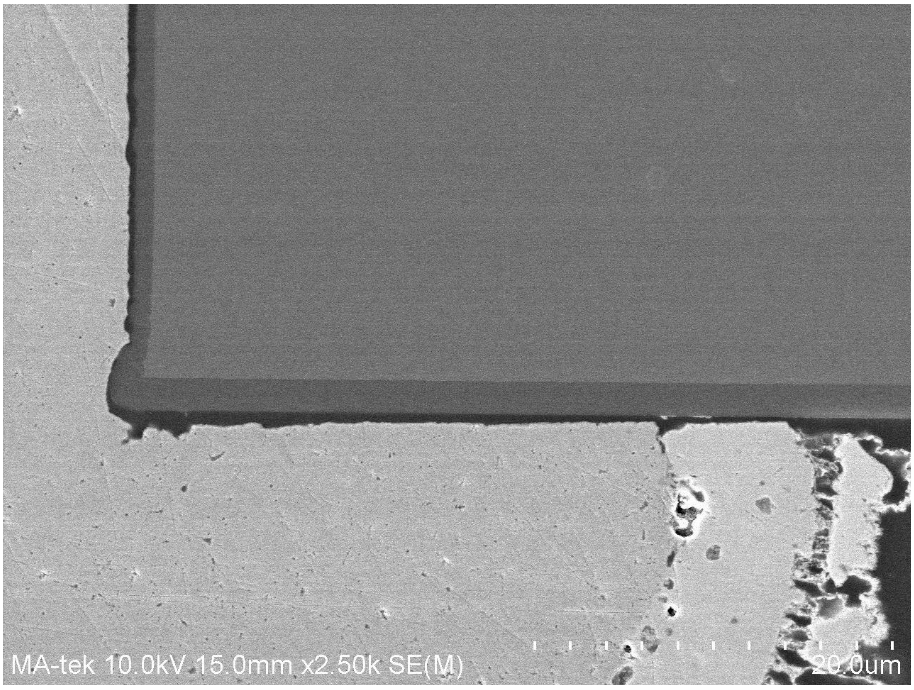


Fig. 4-38 A cross-section image of TEOS between Si and metal

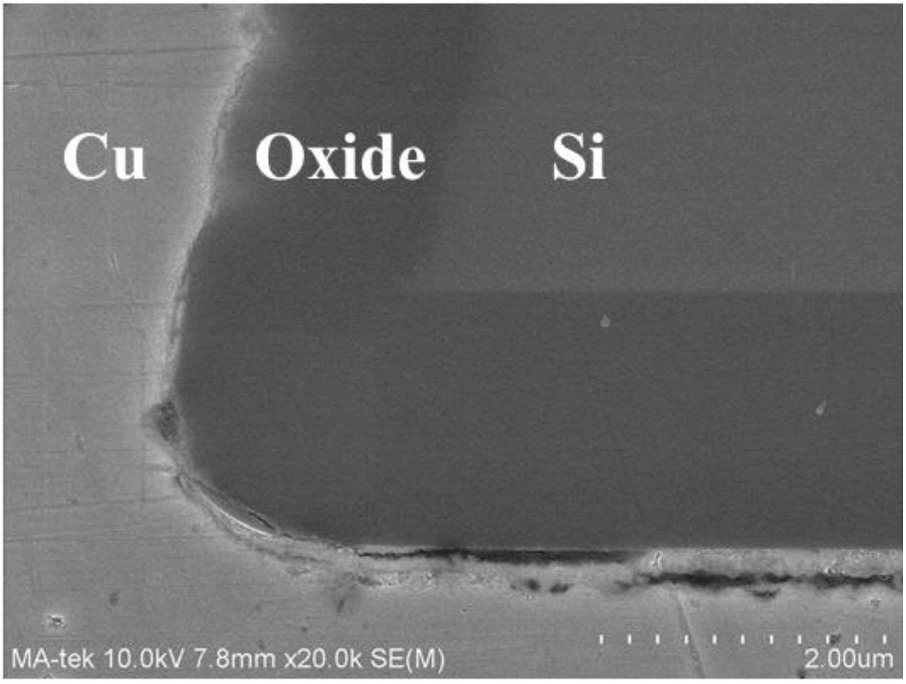


Fig. 4-39 A cross-section image of TEOS between Si and metal

(Zoom in)

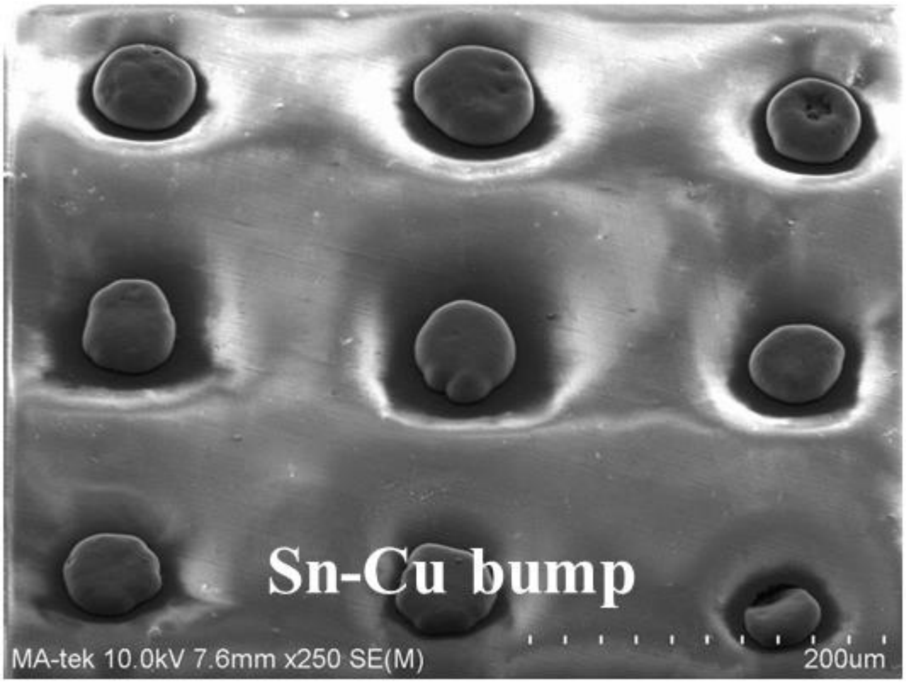


Fig. 4-40 A 45˚tilt view of Sn-Cu bumps

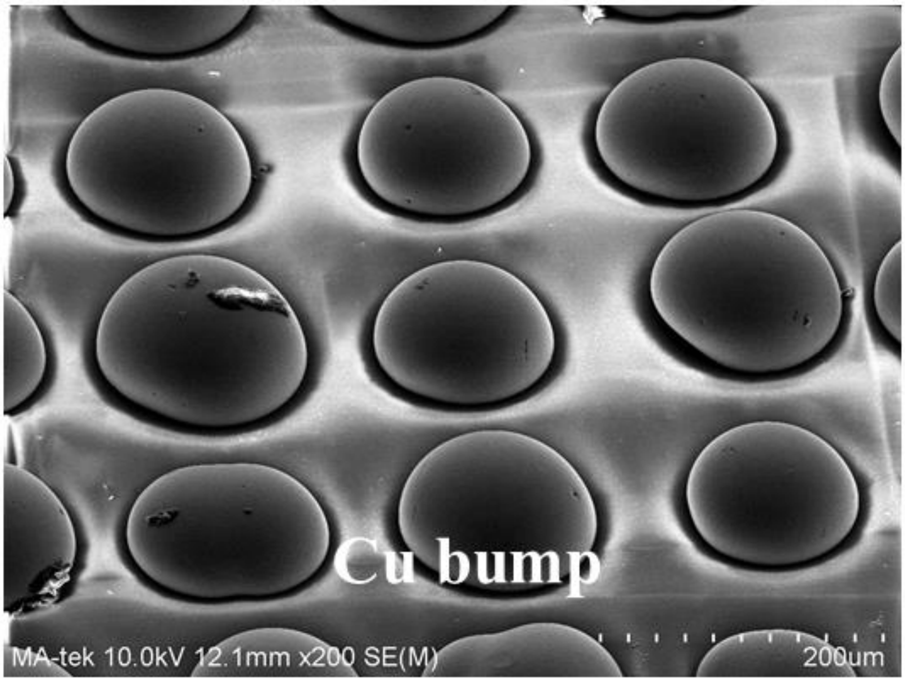


Fig. 4-41 A 45˚tilt view of Cu bumps

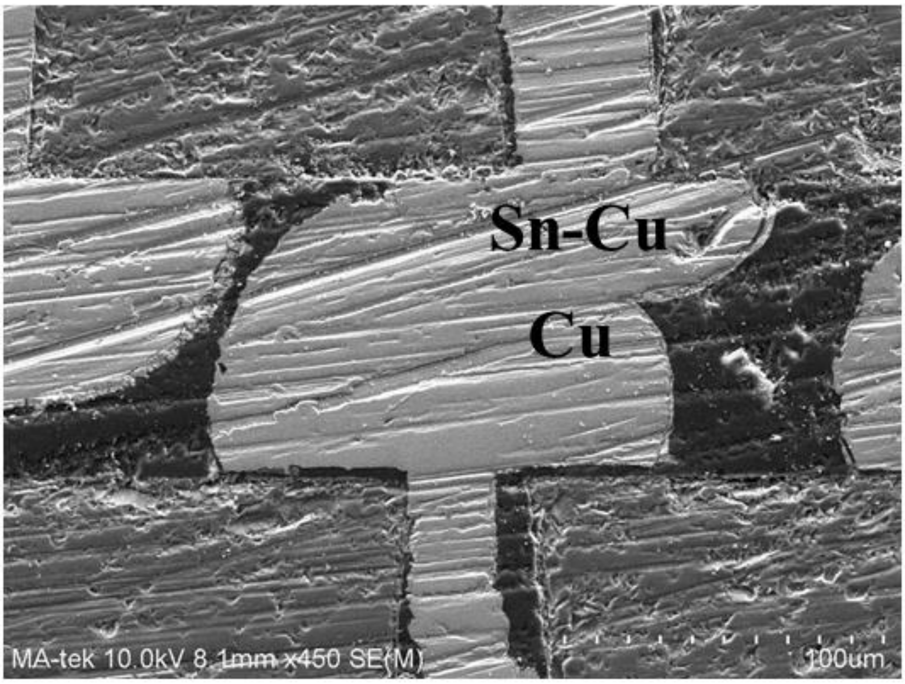


Fig. 4-42 A cross-section image of Sn-Cu bump bonding

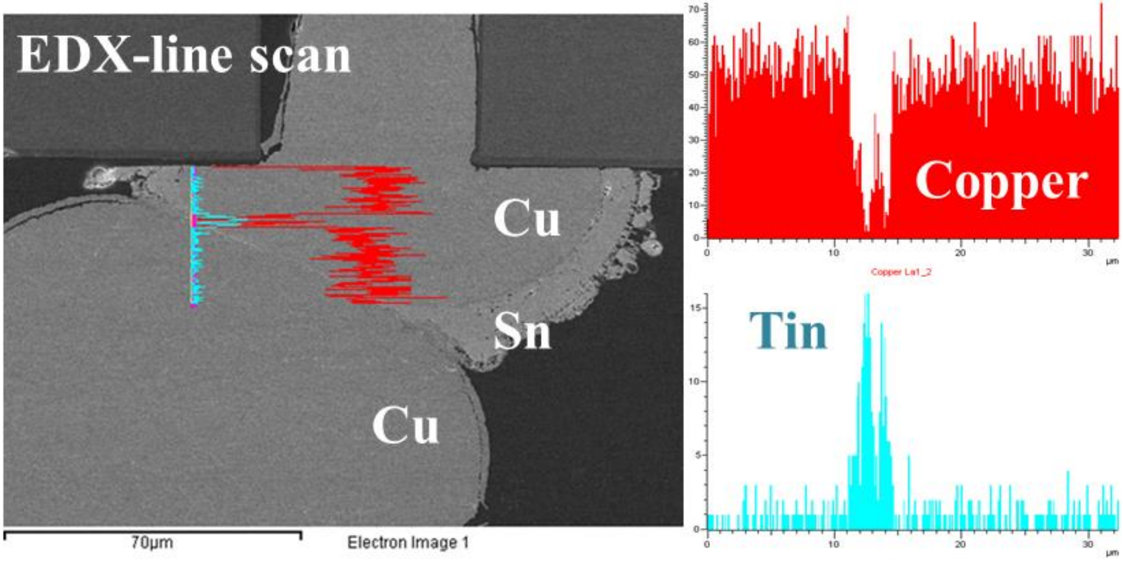


Fig. 4-43 A EDX analysis of Sn-Cu bump bonding

Chapter 5
Conclusions and Future Work

5-1 Conclusions

In this thesis, the research of adhesion strength between Cu and BCB, and hetero-bonding using oxide-BCB, Al-Cu, and Sn-Cu are investigated well. These investigation results provide useful information for hybrid bonding development in three-dimensional integrated circuit (3D IC) applications. In adhesion strength part, Si-Cu-BCB stacking order without Ti or TaN layer for fabrication has the best adhesion strength. And an extra Ti layer between Cu and BCB cannot achieve good adhesion strength because of weak interaction between Ti and BCB. In oxide-BCB bonding part, the suitable temperature range for oxide-BCB bonding is around 350 ℃. And compared with the BCB-thermal oxide bonding, BCB-PECVD oxide bonding can bring a better quality. In Al-Cu bonding part, the suitable temperature range for Al-Cu bonding is around 400℃. In direct wafer bonding, an oxide layer between Al and Cu was observed. And the cleaning process is good for metal oxide removal, and chip level bonding, but it is not suitable for wafer level bonding. In electrical measurement of Al-Cu bonding part, electrical results at AC and DC current stressing are good. But after humidity test, the bonding quality becomes bad because of possible oxide formation or degradation between bonding interface. Finally, in Sn-Cu bump bonding part, the suitable temperature range for Sn-Cu bump bonding is around 350℃. And the sealing Sn-Cu bump bottom-up plating scheme has been demonstrated.

5-2 Future Work

In adhesion strength part, we will measure adhesion strength between metal layers of different lattice structure with BCB polymer and confirm the results by SFG. In oxide-BCB bonding part, we will try to do hybrid bonding such like oxide/Cu-BCB/Cu bonding and in Al-Cu bonding part, we will find a good method for metal oxide removal and suitable for wafer level bonding. In electrical measurement of Al-Cu bonding part, we will do the temperature cycle test (CTC) for Al-Cu interconnect reliability. Finally, in Sn-Cu bump bonding part, we will try to fabricate bump scaling down and enhance TSV density.

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碩士論文題目：

附著力強度與異質接合於三維積體電路應用之研究

Investigation of Adhesion Strength and Hetero-Bonding for 3D IC Applications