國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

超薄高介電常數金屬閘極層之互補式金屬氧化物半導體元件對於隨機電報雜訊的分析

The Random Telegraph Noise (RTN) Analysis in Ultra Thin High-κ Metal Gate CMOS Device

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摘要

當CMOS 元件製程不斷進步，在通道中之電子亦隨之越來越少，單電子效應如Random Telegraph Noise(RTN)對元件造成之臨界電壓擾動亦越來越嚴重，近年更成為可靠度研究之主流題目。本次報告利用RTN 其物理特性，發展出一套對其缺陷位置的分析及萃取方法，更進一步對其位置分佈加以研究。最後，我們對其缺陷能階在無電場情況下(E_{T0})上去做萃取及分析方法，有了前述的方法，我們可以得到RTN的缺陷在位置以及能帶中的分佈情況。有助於未來對於此可靠性議題之研究。

Abstract

As the scaling of the CMOS technology advances aggressively, the Random Telegraph Noise (RTN) becomes an important reliability issue.[1] Since RTN is a stochastic fluctuation between two levels of either the device drain current (I_D) or threshold voltage (V_t) induced by trapping/de-trapping of a single charge in a gate trap.

In this work, we demonstrate a method to extract RTN trap position both in vertical direction (channel surface to gate electrode) and lateral direction (source to drain). Therefore, the traps in gate dielectric can be profiled.

Finally, we extract RTN trap energy at zero electric field condition (E_{T0}) in vertical direction.

謝誌

首先我要感謝指導老師汪大暉教授，如果沒有汪老師兩年的悉心指導以及提供完善的實驗環境，就不會有今天這本論文的完成，更不會有今天的成就，再次感謝汪老師的幫忙。

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除了實驗室的夥伴，我要特別感謝我研究所的室友曾至均，當我在研究上的碰到不順遂的時候，他總是能夠幫我分擔我憂慮並幫我打氣，至均對於他研究的熱忱與細膩，是我的目標以及榜樣，並祝他能夠在未來的生涯發展能夠順利。

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Chapter 1

Introduction

Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFETs) has been widely utilized in the past few decades. When device geometry scale down to nanotechnology, the random telegraph noise (RTN) becomes an important reliability issue. It will reduce the device performance in both analog and digital circuit.[2] RTN has been proposed in recent years. Fig.1.1 is an illustration of our MOSFETs cell structure and typical Two level RTN pattern, where (i) $<\tau_c>$ means not only capture time but average of empty trap state time, (ii) $<\tau_e>$ means either emission time or average of empty trap state time, and (iii) ΔI_d is the current fluctuation between two levels. Fig.1.2 shows RTN is observable when trap of energy level E_T is a few kT differences to the Fermi level E_F, where k is the Boltzmann's constant, T is equilibrium temperature. The trap of energy level can be extracted from RTN according to the following equation [3]:

$$\frac{<\tau_c>}{<\tau_e>} = g\exp(\frac{E_T - E_F}{kT}) \propto \exp(\frac{E_T - E_F}{kT}) \qquad \text{Eq.1.1}$$

where g is degeneracy factor, $<\tau_c>$ and $<\tau_e>$ are average of capture and emission times, k is the Boltzmann's constant and T is temperature. If we can obtain the time constant ratio $<\tau_c>/<\tau_e>$, the trap of energy E_T can be extracted. Fig.1.3 shows a typical single level RTN and obtains the time constant ratio $<\tau_c>/<\tau_e>$. Fig.1.4 shows example of multi-level RTN. However, the RTN amplitudes are different from the same device caused by percolation effect. The percolation effect will be introduced in the chapter 3.

There are five chapters in this thesis. Chapter 1 is a brief introduction to RTN and its most important three parameters $<\tau_c>$, $<\tau_e>$ and ΔI_d. In Chapter 2, we will extract trap position both in lateral direction (source to drain) and vertical direction (channel surface to gate electrode). In Chapter 3, demonstrate the measurement process flow chart and its result discussions. The extraction of trap energy at zero electric field condition E_{T0} will be characterized in Chapter 4. Finally, we make conclusions in the last chapter.

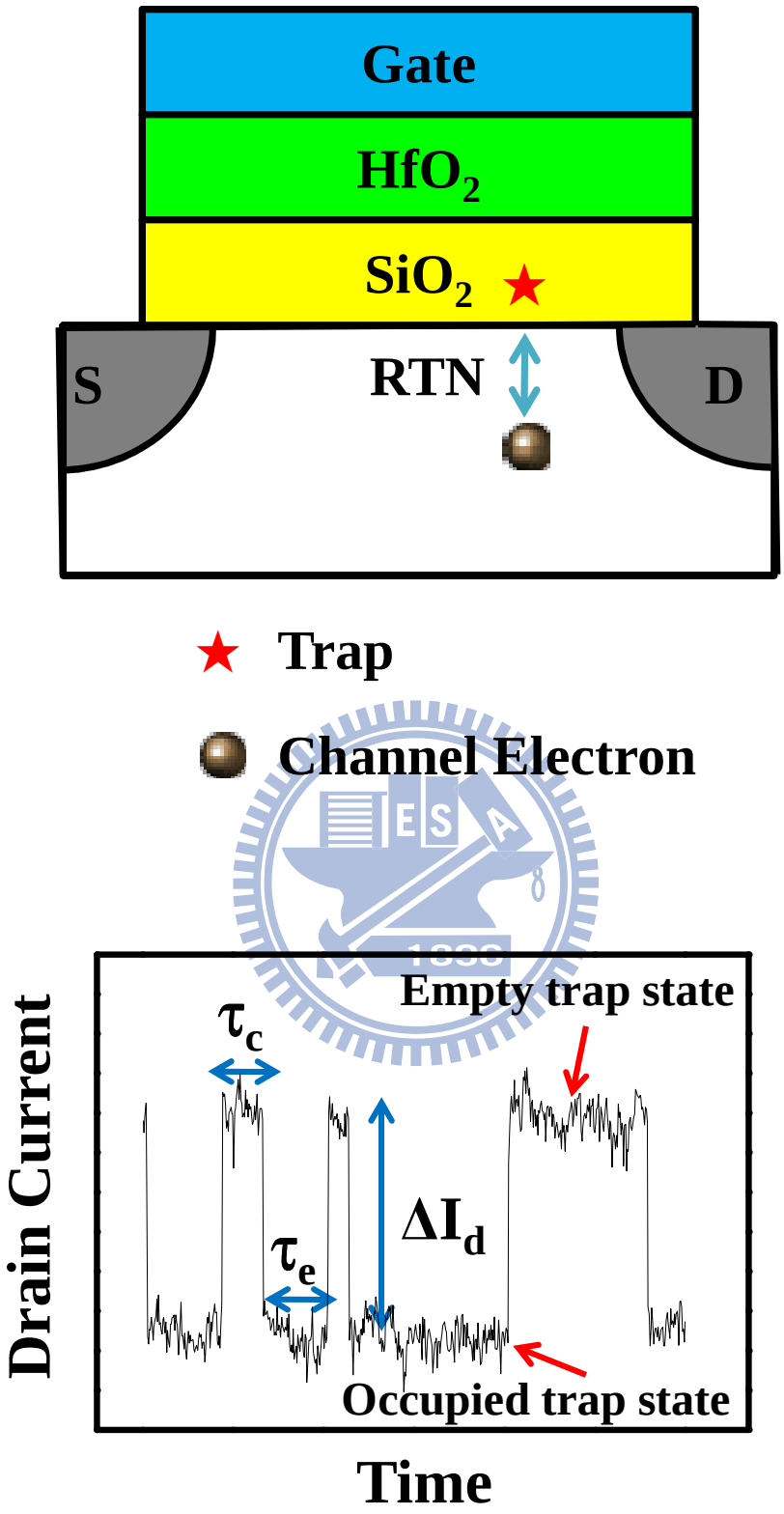


Fig.1.1 Illustration of a channel electron capture and emission by an interface trap in our high-κ metal-gate MOSFET. And drain current waveform resulting from electron emission and capture at an interface trap.

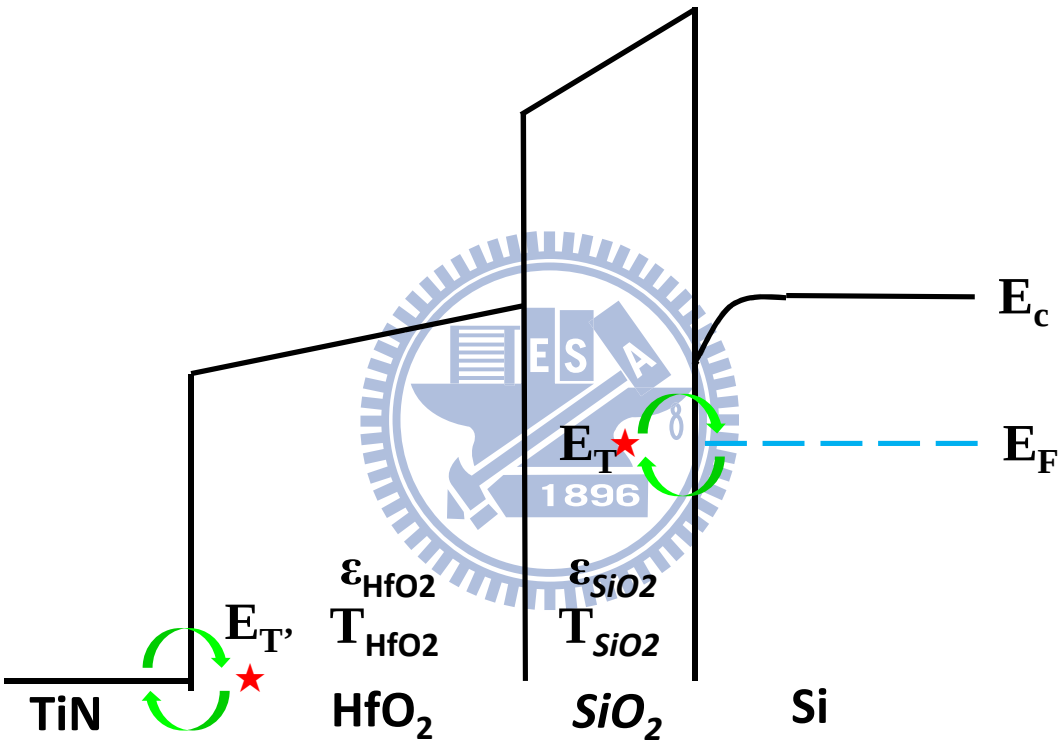


Fig.1.2 RTN is observable when trap of energy level E_T is a few kT different from the Fermi level E_F.

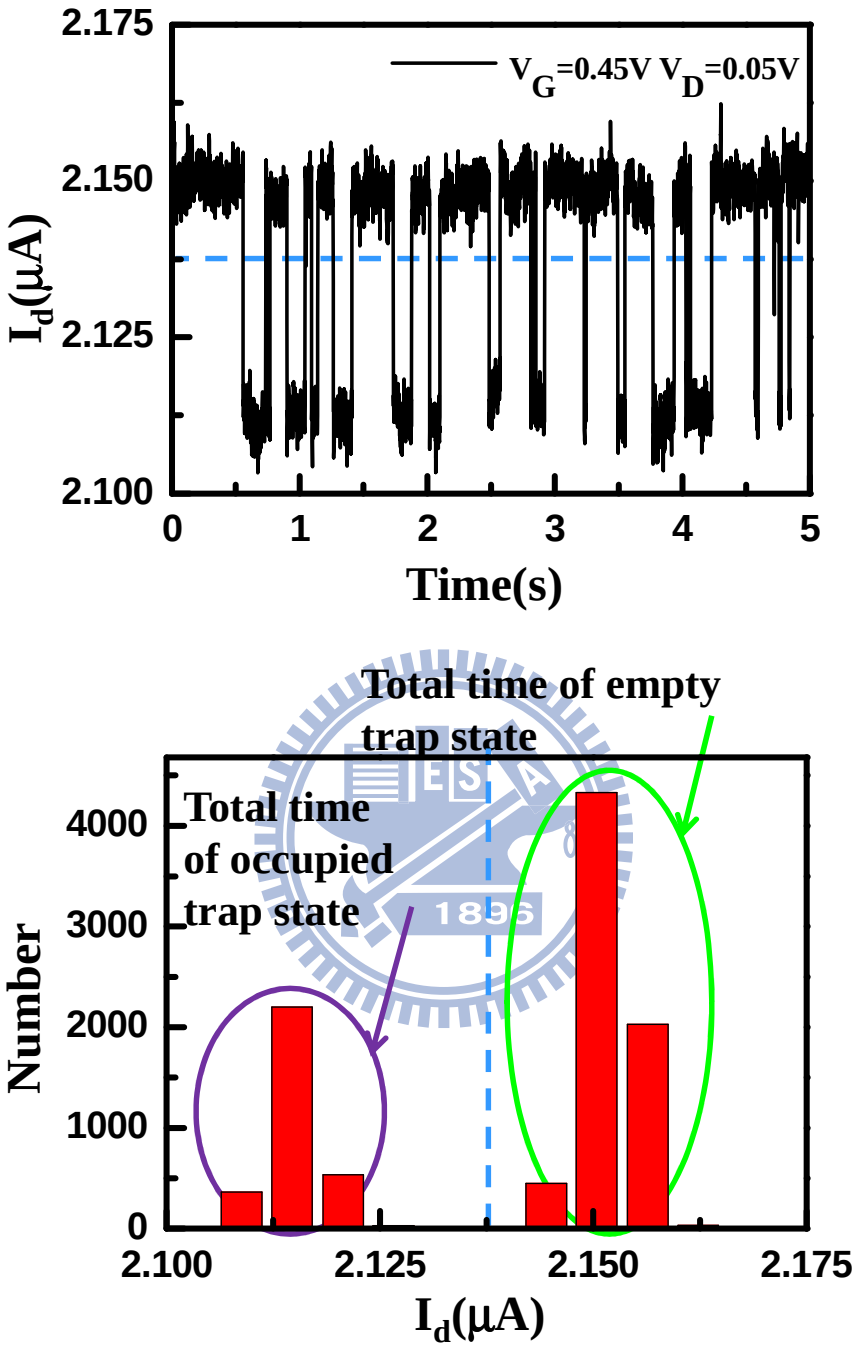


Fig.1.3 A typical drain current waveform of single level RTN induced current fluctuation @(V_G=0.45V V_D=0.05V).

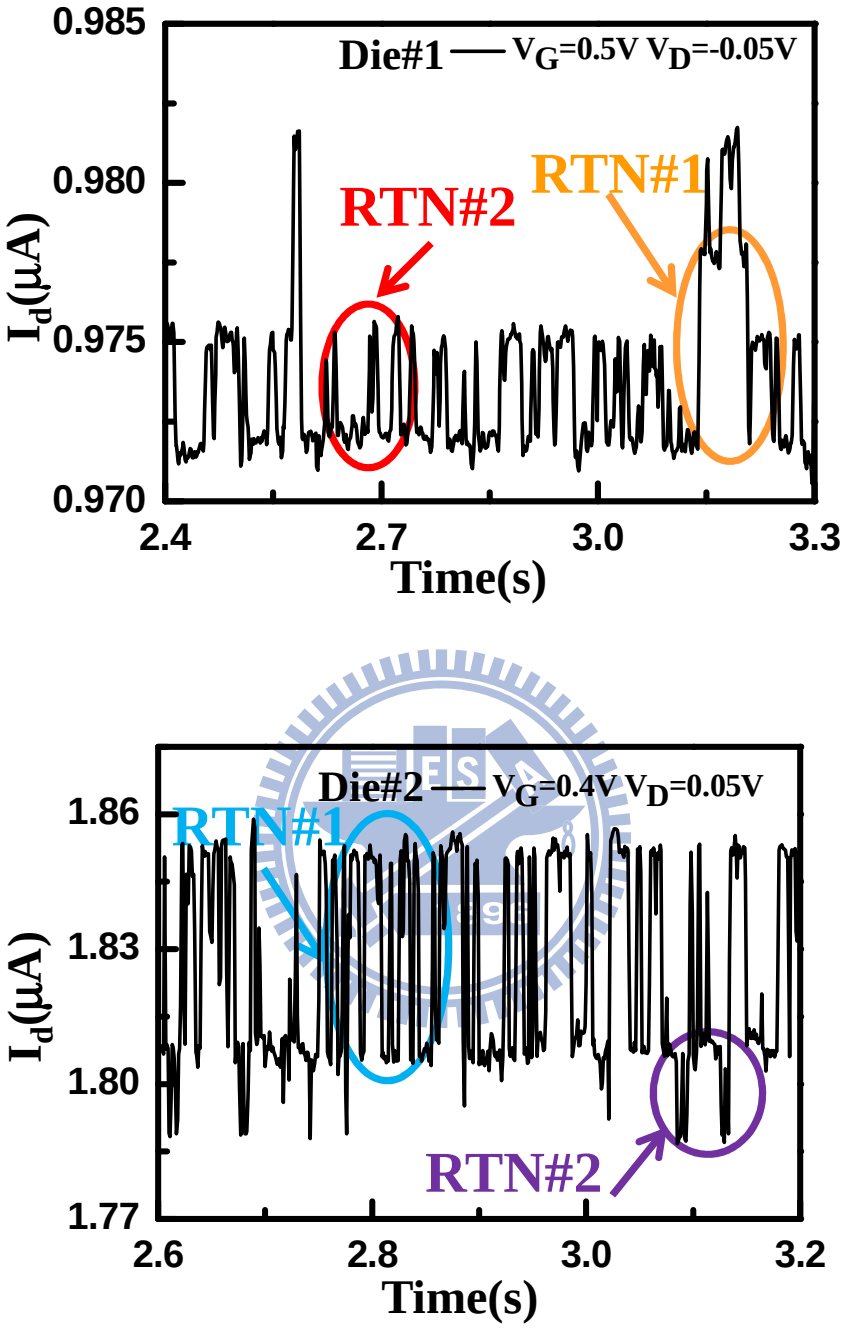


Fig.1.4 Drain current waveform of Multi-level RTN. RTN amplitudes are different from the same device caused by percolation effect.

Chapter 2
Trap Position Extraction

2.1 Introduction

From Chapter 1, we obtained the relationship between the time constant ratio $<\tau_c>/<\tau_e>$ and trap energy E_T. In this chapter, we will derive trap position equations in both lateral direction (source to drain) and vertical direction (channel surface to gate electrode). In order to investigate the reference point of HK/IL interface, a 1D Poisson simulation is used to evaluate $d\ln(\tau_c/\tau_e)/dV_G$ in the end of this chatper.

2.2 RTN Trap Lateral Position Extraction

From the above discussions, we know the time constant ratio $<\tau_c>/<\tau_e>$ has relationship to E_T-E_F according to Eq.2.1. Therefore we can manipulate different of bias conditions to reach the same time constant ratio.

Fig.2.1 illustrates the trap lateral position extraction. Since MOSFETs operate in linear region, the voltage inside channel is proportion to length direction. Thus we can extract the trap position in lateral direction Y_{TS} according to the following equation:

$$Y_{TS} = \frac{\Delta V_{TS}}{\Delta V_{DS}} \times L_{DS} \qquad \text{Eq.2.1}$$

where L_{DS} is the distance from source to drain, ΔV_{TS} is the voltage difference under same time constant ratio and ΔV_{DS} is drain bias difference. All we have to do is to extract the ΔV_{TS} from measurement data analysis, and then Y_{TS} is extracted.

2.3 RTN Trap Vertical Position Extraction

Fig.2.2 illustrates the band diagram where a trap with trap energy E_T in SiO_2 layer. From the Eq.1.1, assume degeneracy factor g=1 [4][5], we get:

$$\ln(\frac{\tau_c}{\tau_e}) = -\frac{1}{kT}\left[\begin{array}{l}(E_{C_{SiO_2}} - E_T) - (E_C - E_F) - \Phi_0 + \\ q\Psi_s + q\frac{X_T}{T_{SiO_2}}(V_G - V_{FB} - \Psi_s - \Psi_p)\end{array}\right] \quad \text{Eq. 2.2}$$

where E_{CSiO2} is the conduction band edge of SiO_2, E_T is trap energy level, E_C is the conduction band edge of silicon, E_F is Fermi level, Φ_0 is the difference between the electron affinities of Si and SiO_2 , Ψ_s is the surface potential band bending, X_T is the vertical position from channel surface, T_{SiO2} is the thickness of SiO_2, V_G is gate to source voltage, V_{FB} is the flat band voltage, Ψ_p is the poly gate band-bending, q is elementary electronic charge. The right hand side in brackets is the difference between trap energy level E_T and Fermi level E_F. By differentiating Eq.2.2 with V_G, Eq.2.2 becomes the following equation:

$$\frac{d\ln(\tau_c/\tau_e)}{dV_G} = -\frac{q}{kT}\left[\frac{\Psi_s}{dV_G} + \frac{X_T}{T_{SiO_2}}(1 - \frac{\Psi_p}{dV_G} - \frac{d\Psi_s}{dV_G})\right] \quad \text{Eq.2.3}$$

Finally, the trap in vertical position from channel is obtained by the following equation:

$$X_T = T_{SiO_2}[\frac{kT}{q}\frac{d\ln(\tau_c/\tau_e)}{dV_G} + \frac{d\Psi_s}{dV_G}] \Big/ (\frac{d\Psi_p}{dV_G} + \frac{d\Psi_s}{dV_G} - 1) \quad \text{Eq. 2.4}$$

But our device is shown high-κ and metal gate stack MOSFETs. Thus the equation he poly gate energy variation rate is zero and EOT substitute to SiO_2. Finally, Eq.2.4 becomes:

$$X_T = \left(T_{SiO_2} + \frac{\varepsilon_{SiO_2}}{\varepsilon_{high\text{-}\kappa}} T_{high\text{-}\kappa} \right) \left(\frac{kT}{q} \frac{d \ln(\tau_c / \tau_e)}{dV_G} + \frac{d\Psi_s}{dV_G} \right) \Big/ \left(\frac{d\Psi_s}{dV_G} - 1 \right) \quad \text{Eq.2.5}$$

In addition, similar procedure can be made as the charge exchanges with gate. A positive slope is observed in gate-exchanging case. All condition is listed in Table.1.[6]

In order to investigate the reference point of HK/IL interface, a 1D Poisson simulation is used to evaluate $d\ln(\tau_c/\tau_e)/dV_G$ in both negative and positive slope case.[6] Fig.2.3 shows the reference value in both negative and positive conditions. For our device, the negative reference point value is about $-27V^{-1}$ and is about $12V^{-1}$. If the experimental value $d\ln(\tau_c/\tau_e)/dV_G$, for example, is over $-27V^{-1}$, the trap is located in HfO_2 layer, otherwise, is located in SiO_2 layer.

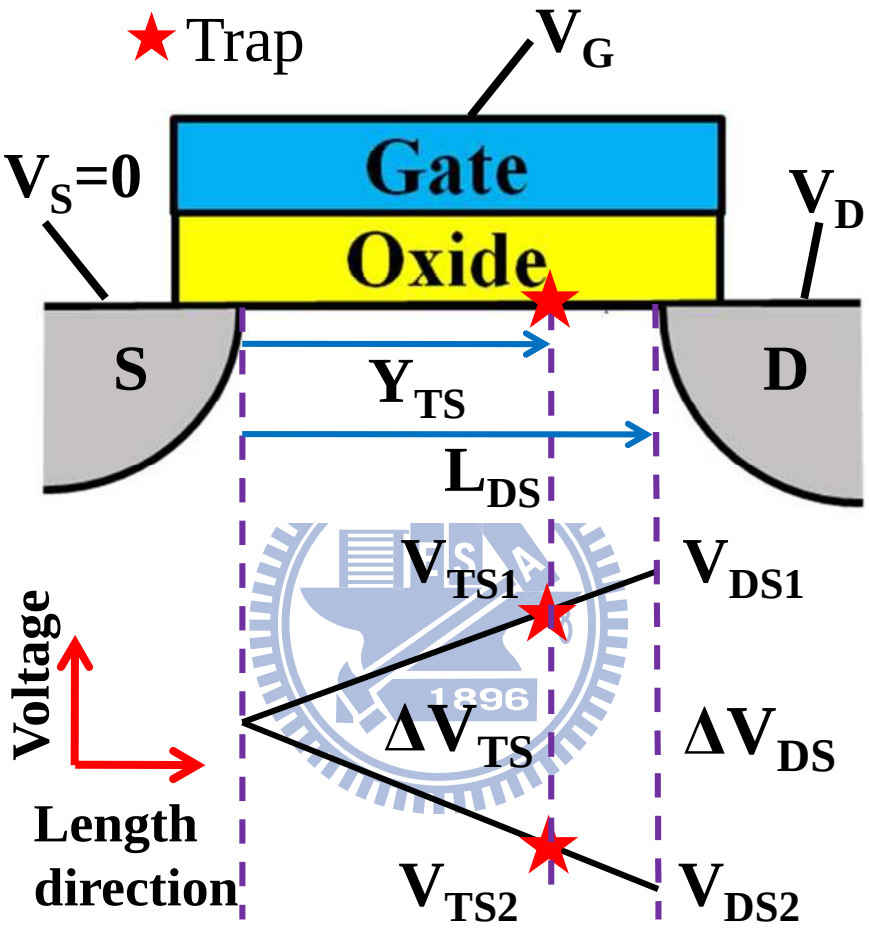


Fig.2.1 Illustration of lateral position extraction of RTN trap. The voltage in channel is proportion to lateral position.

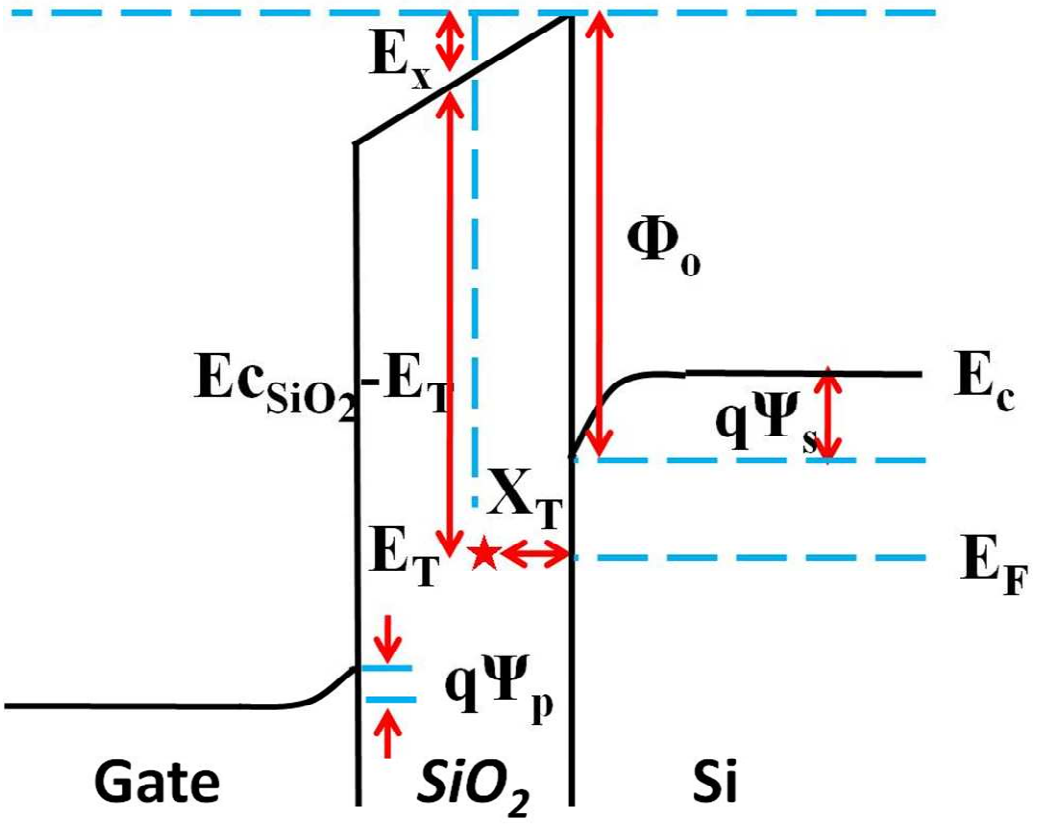
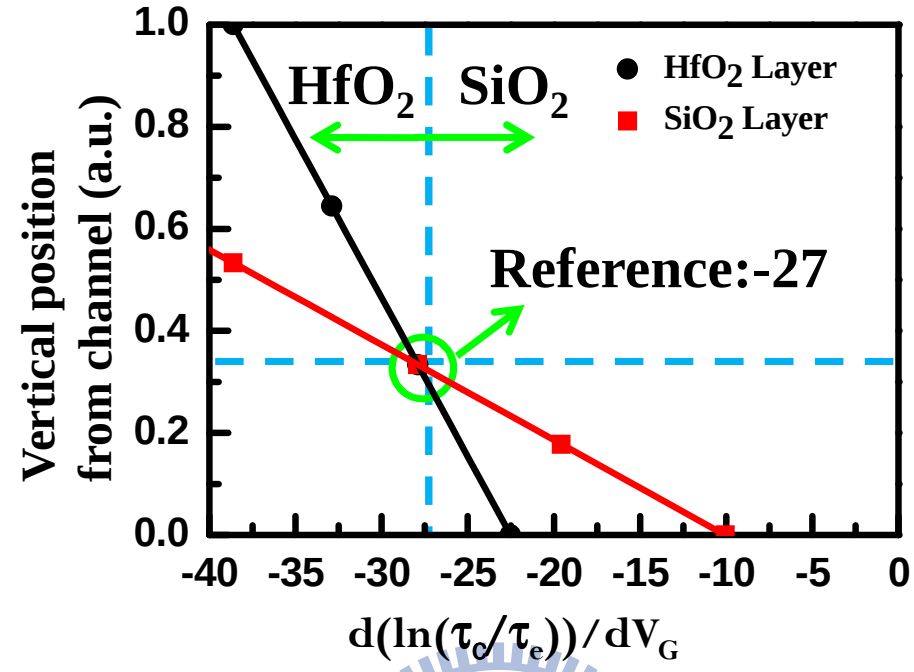
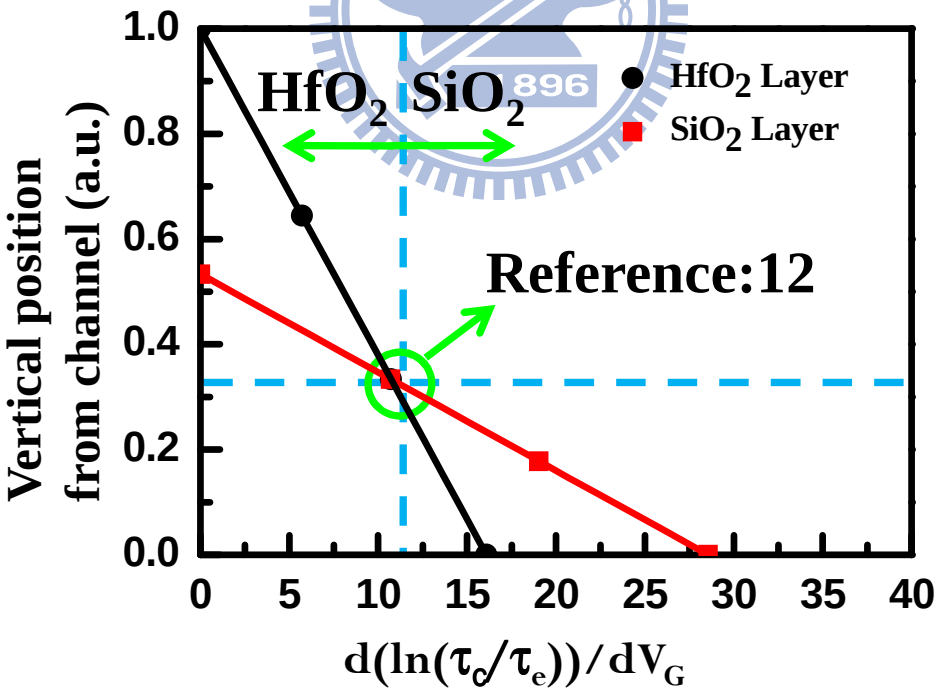


Fig.2.2 Band diagram of a trap with a vertical position (X_T) and a trap energy (E_T) in SiO_2 layer.



(a)



(b)

Fig.2.3 Reference values of negative (a) and positive (b) slopes using 1D Poisson equation simulation.

Table.1 is a trap vertical position extraction in different gate dielectric layers.

A trap in Oxide interact with channel

$$X_T = \left(T_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{high\text{-}\kappa}} T_{high\text{-}\kappa} \right) \left(\frac{kT}{q} \frac{d \ln(\tau_c / \tau_e)}{dV_G} + \frac{d\Psi_s}{dV_G} \right) \Big/ \left(\frac{d\Psi_s}{dV_G} - 1 \right)$$

A trap in High-κ interact with channel

$$X_T = \left[\left(T_{high\text{-}\kappa} + \frac{\varepsilon_{high\text{-}\kappa}}{\varepsilon_{ox}} T_{ox} \right) \left(\frac{kT}{q} \frac{d \ln(\tau_c / \tau_e)}{dV_G} + \frac{d\Psi_s}{dV_G} \right) \Big/ \left(\frac{d\Psi_s}{dV_G} - 1 \right) \right] + \left(1 - \frac{\varepsilon_{high\text{-}\kappa}}{\varepsilon_{ox}} \right) T_{ox}$$

A Trap in Oxide interact with gate electrode

$$X_T = \left[1 - \frac{kT}{q} \frac{d \ln(\tau_c / \tau_e)}{dV_G} \Big/ \left(1 - \frac{d\Psi_s}{dV_G} \right) \right] \left(T_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{high\text{-}\kappa}} T_{high\text{-}\kappa} \right)$$

A trap in High-κ interact with gate electrode

$$X_T = \left[1 - \frac{kT}{q} \frac{d \ln(\tau_c / \tau_e)}{dV_G} \left(1 + \frac{\varepsilon_{high\text{-}\kappa} T_{ox}}{\varepsilon_{ox} T_{high\text{-}\kappa}} \right) \Big/ \left(1 - \frac{d\Psi_s}{dV_G} \right) \right] T_{high\text{-}\kappa} + T_{ox}$$

Chapter 3

Measurement Data Analysis and Discussions

3.1 Introduction

Firstly, we extract the parameters from measurement data. Then we can obtain trap position both in lateral direction and vertical direction. Secondly, we make result discussions. Finally, we introduce percolation effect.

3.2 Measurement Setup and Analysis Method

We use Agilent 4155C to measure the high-κ and metal gate stack CMOS devices with gate length of 30 nm, width of 0.03~0.16 μm and two different EOT 7.8, 12.89Å under an appropriate sampling rate as shown in Fig.3.1.

Fig.3.2 is the flow chart of our analysis process. Fig.3.3 shows a two level RTN pattern with varies gate voltage, $\ln(\tau_c/\tau_e)$ becomes smaller as gate voltage increases, that is, a negative slope can be observed. We measured nMOS with V_G=0.4V, V_D=0.1V and $V_{G,step}$=25mV. As V_G increase, the capture time $<\tau_c>$ decreases and emission time $<\tau_e>$ increases. In other words, the time constant ratio $<\tau_c>/<\tau_e>$ become smaller when V_G increases. We can obtain the slope value, $d\ln(\tau_c/\tau_e)/dV_G$, is about -13.426V^{-1}. Since the slope value was smaller than the reference value -27V^{-1}, the vertical trap position can be calculated by Eq.2.5 is 5.79Å in the SiO_2 layer and lateral trap position can be calculated by Eq.2.1 is about 0.4422L_{DS} from source. The other one is shown in Fig.3.4. On the contrary, As V_G increase, the capture time constant $<\tau_c>$ increases and emission time constant $<\tau_e>$ decreases. Therefore the time constant ratio $<\tau_c>/<\tau_e>$ become larger when V_G increases. Similarly, the slope value,

$d\ln(\tau_c/\tau_e)/dV_G$, is about $3.2161V^{-1}$. It's smaller than reference value $12V^{-1}$. The trap positions in vertical and lateral direction are 19.8Å in the HfO_2 layer and $0.1462L_{DS}$ from source. Finally, we measured 124 nMOS RTN samples and the trap distribution along vertical and lateral direction is shown in Fig.3.5. Most of RTN trap position in vertical direction locates in HfO_2 layer. And RTN trap position has a uniform distribution.

3.3 Percolation Effect

While device technology node scaling down, the number fluctuation can't explain that RTN amplitudes are different. Therefore, the atomistic random dopant induced percolation effect is proposed. RTN amplitudes in current generation are dominated by percolation effect. Fig.3.6 is the illustration channel surface potential and current pattern at channel surface.[7] The current will percolates through valleys from source to drain. When interface trap trapping a channel carrier, it will generate local potential barrier to disturb the current percolation path. Fig.3.7 shows the current fluctuation result from an interface trap charge at varies positions. If the interface trap charge position locates on the critical current path, then RTN amplitude ΔI_D is relatively large. On the contrary, interface trap charge position locates on the minor percolation path will induce small current fluctuation ΔI_D.

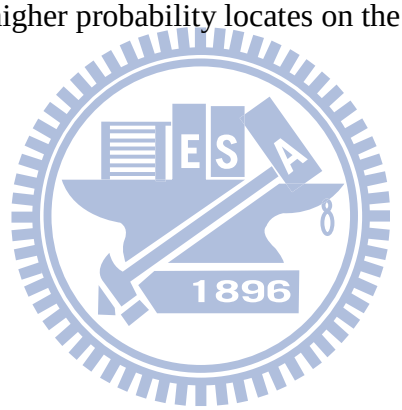
Moreover, RTN amplitudes obey exponential distribution and have the following equation [1] [8]:

$$f(\Delta I_d) = \frac{1}{\sigma}\exp(-\frac{\Delta I_d}{\sigma}) \qquad \text{Eq.3.1}$$

where σ is distribution standard variation and is a function of doping concentration, cell length, width and oxide thickness**.** Integrating Eq.3.1, we obtain:

$$f(\Delta I_d) = \exp(-\frac{\Delta I_d}{\sigma}) \qquad \text{Eq. 3.2}$$

We measured devices with same cell length and controlled different cell width. Fig.3.8 is the RTN amplitude distribution. The distribution standard variation, σ, is increase while cell width is decrease. In other words, cell width is decrease, the interface trap position has higher probability locates on the main percolation path.



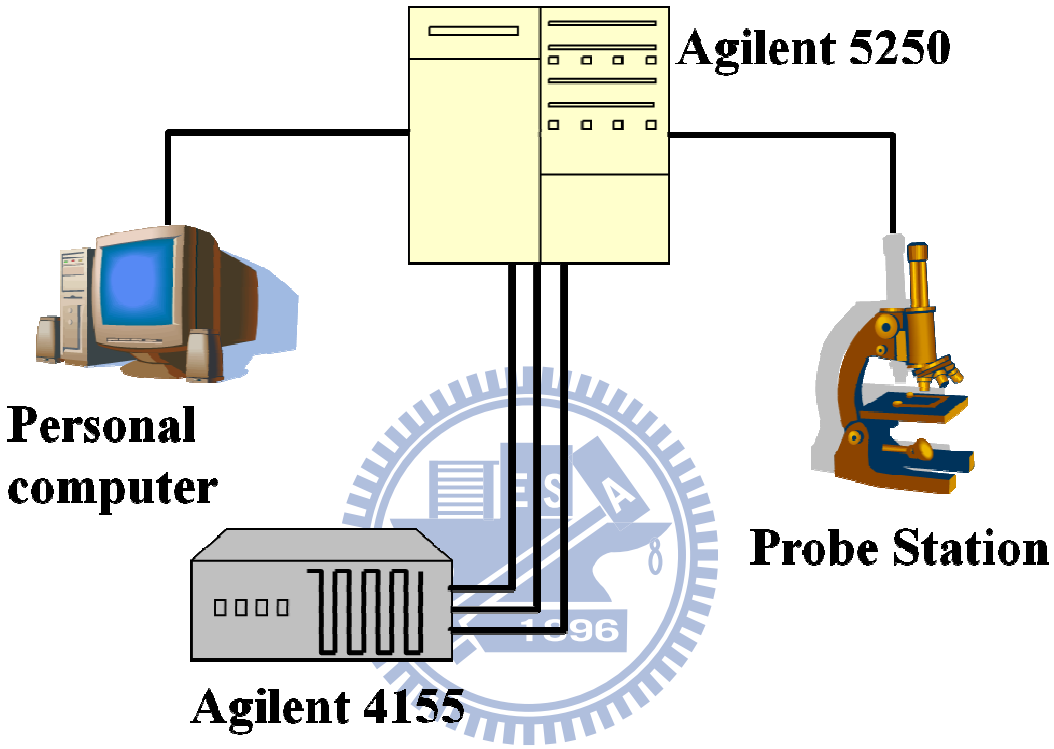


Fig.3.1 Illustration of measurement setup and we use Agilent 4155 to measure the high-κ and metal gate stack CMOS devices.

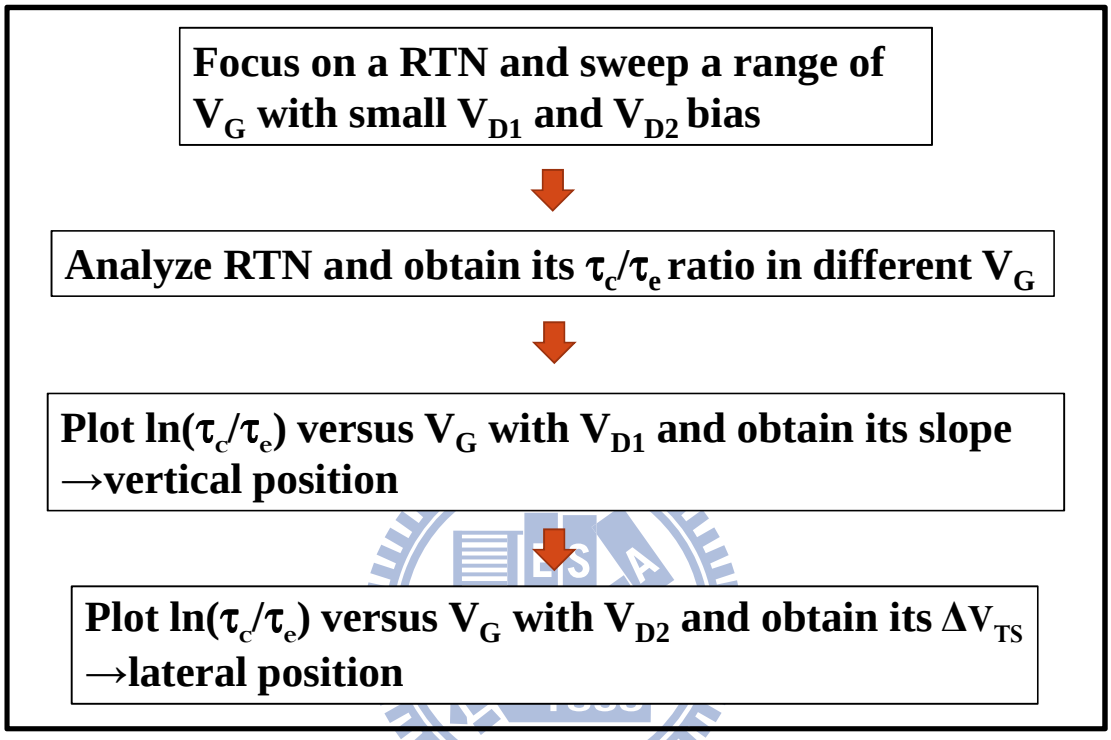


Fig.3.2 First, focus on a RTN and sweep a wide range of V_G with two drain bias V_{D1} and V_{D2}. Second, obtain the time constant ratio $<\tau_c>/<\tau_e>$ in different V_G with V_{D1}. Third, plot $\ln(\tau_c/\tau_e)$ versus V_G with V_{D1}, obtain its slope and compare with our reference points which indicates the trap locates in either HK or IL. Therefore, we can extract the trap vertical position from Table.1. Finally, repeat the steps before with V_{D2}. Then obtain ΔV_{TS} and the trap lateral position can be extracted by Eq.2.1.

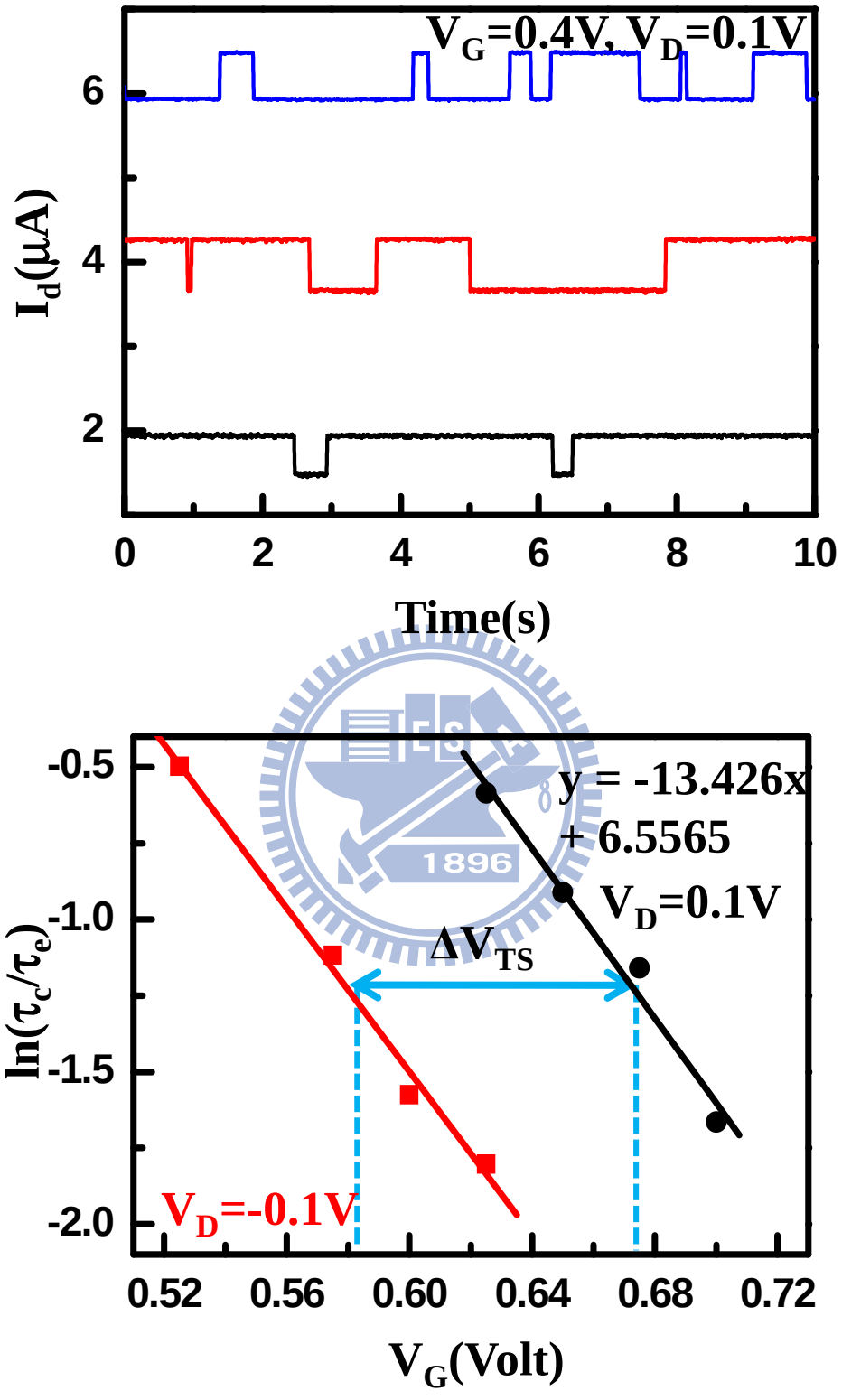


Fig.3.3 A two level RTN pattern with varies gate voltage, τ_c becomes smaller as gate voltage V_G increases. ΔV_{TS} is the voltage difference at same time constant ratio.

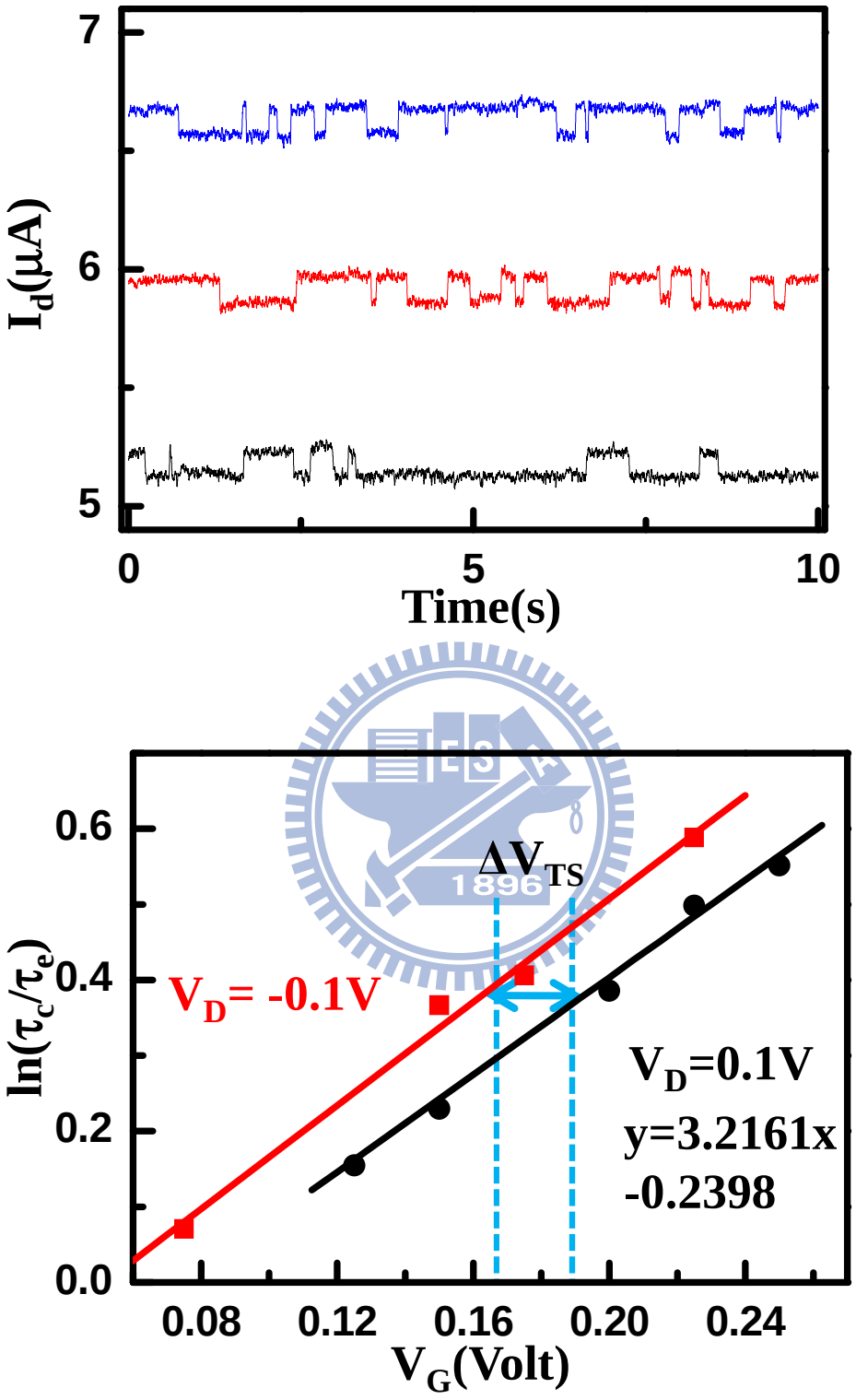
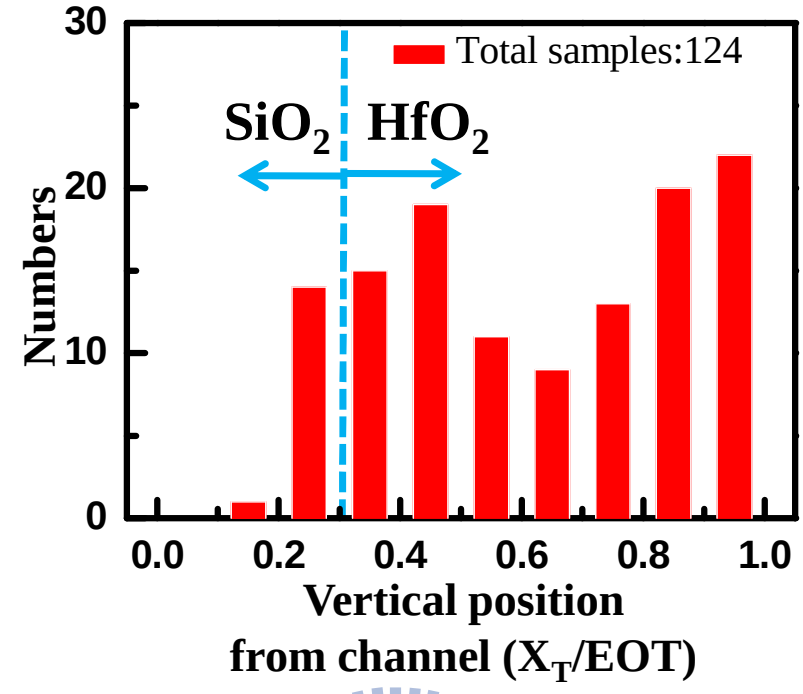
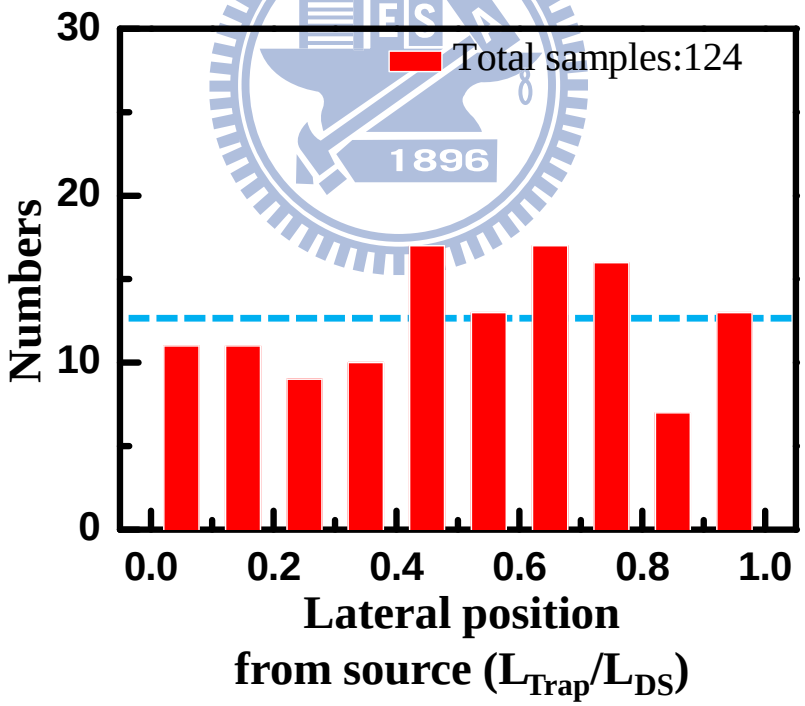


Fig.3.4 A two level RTN pattern with varies gate voltage. Capture time constant τ_c becomes larger as gate voltage V_G increases.



(a)



(b)

Fig.3.5 (a) is trap distribution along vertical direction. Most of traps locate in HfO_2 layer. (b) is trap distribution along lateral direction, which exhibits an uniform distribution.

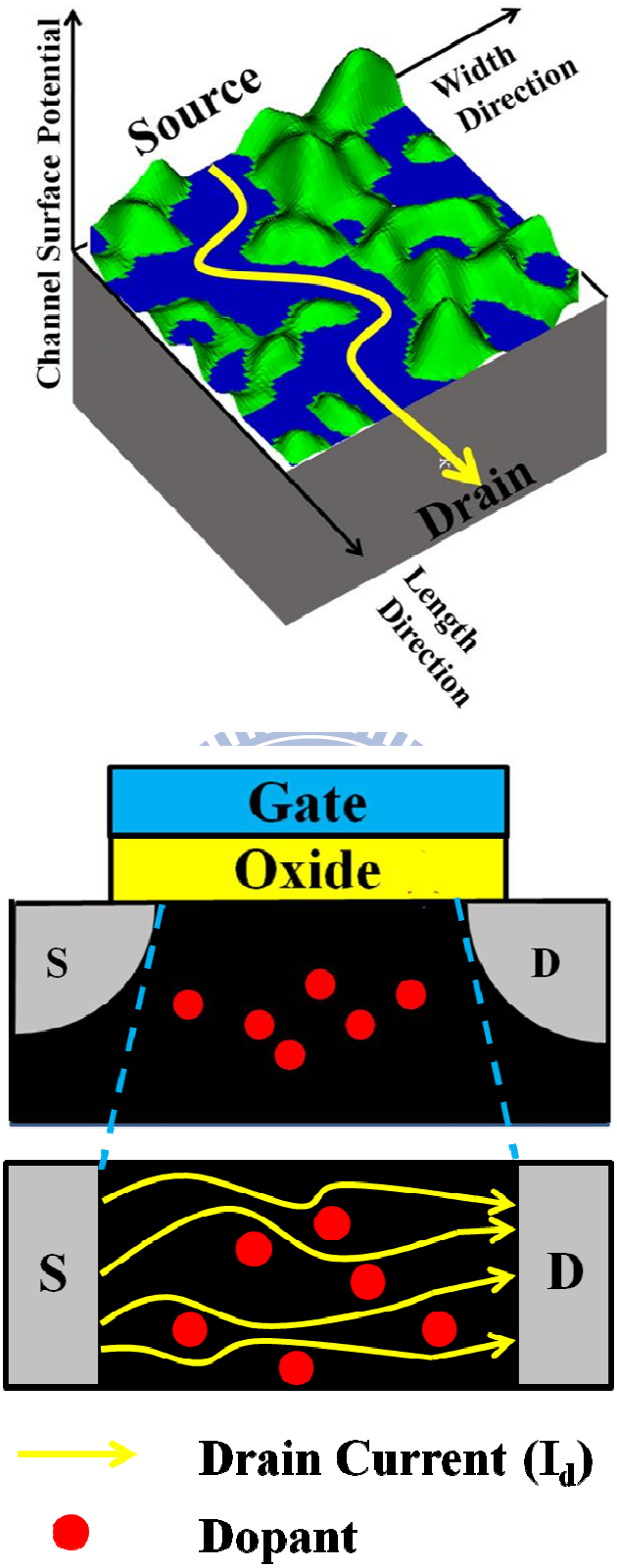


Fig.3.6 Illustration of channel surface potential and current pattern.

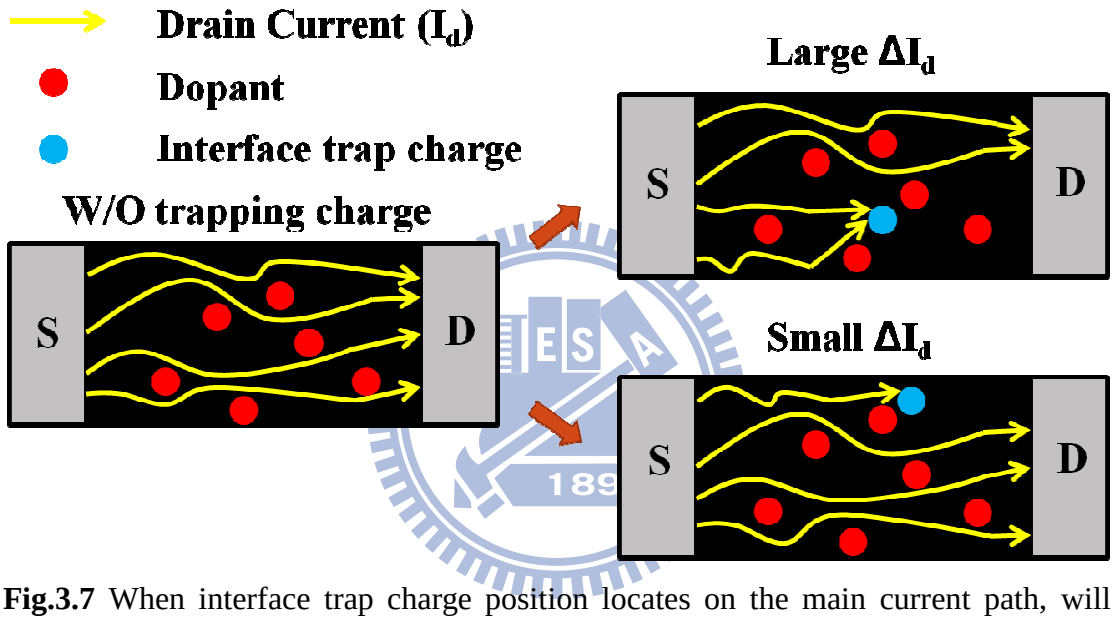
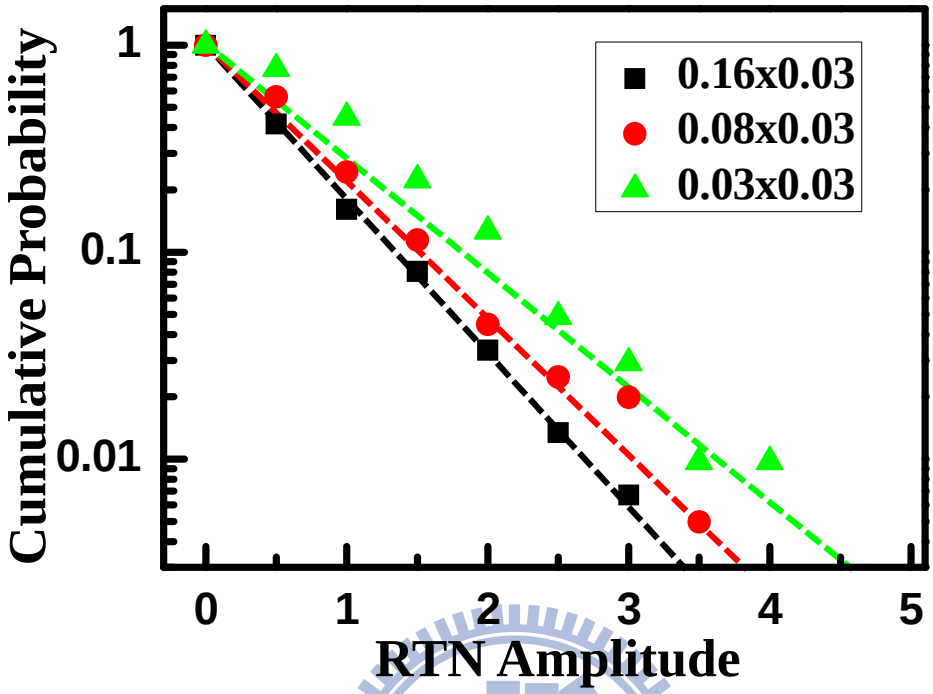


Fig.3.7 When interface trap charge position locates on the main current path, will induce large drain current fluctuation ΔI_d.



W / L	0.16 / 0.03	0.08 / 0.03	0.03 / 0.03
σ	0.58	0.68	0.94

$$f(\Delta I_d) = \exp(-\frac{\Delta I_d}{\sigma})$$

Fig.3.8 RTN amplitude distribution with different cell width. σ becomes large as cell width is decrease.

Chapter 4

Analysis of Trap Energy

4.1 Introduction

In this chapter, we demonstrate the extraction of trap energy at zero electric field condition E_{T0}. First of all, we explain that $d\ln(\tau_c/\tau_e)/dV_G$ has different dependences as V_G increases. Second, we derive the trap energy at zero electric field condition E_{T0}; in other words, extraction of trap energy at flat band condition. Finally, result discussions.

4.2 Cause of V_G Dependent Difference

From chapter 3, we know that $d\ln(\tau_c/\tau_e)/dV_G$ has different V_G dependences. To simplify the explanations, we define two types of trap as shown in Fig.4.1. We regard negative and positive V_G dependences as Type A trap and Type B trap. Fig.4.2 shows the band diagram on different V_G conditions. From the Fig.4.2, Type A trap exchanges carriers with channel. Type B trap exchanges carriers with gate electrode.

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4.3 RTN Trap Energy in Flat Band Extraction

Fig.4.3 illustrates nMOS band diagram with a Type A trap in IL layer at different V_G biases V_{FB} and V_{G0}.[9] Where X_T is trap vertical position from channel, E_T is trap energy, E_{T0} is E_T at zero electric field, E_c is bottom of conduction band, E_v is bottom of valance band, E_F is Fermi level of channel, Ψ_s is surface potential band-bending,

ε_{SiO2} is dielectric constant of IL layer, ε_{HfO2} is dielectric constant of high-κ layer, T_{SiO2} is IL layer thickness, T_{HfO2} is high-κ layer thickness.V_{G0} is defined as the value of $d\ln(\tau_c/\tau_e)/dV_G$ is zero. It means that the condition where the trap energy aligns with Fermi level. To simplify the equations, V_{SiO2} and V_{HfO2} are voltage crossed on IL and high-κ layer respectively and have following equations:

$$V_{SiO_2} = (V_{G0} - V_{FB} - \Psi_s) \times \frac{T_{SiO_2}/\varepsilon_{SiO_2}}{T_{SiO_2}/\varepsilon_{SiO_2} + T_{HfO_2}/\varepsilon_{HfO_2}}$$
$$V_{HfO_2} = (V_{G0} - V_{FB} - \Psi_s) \times \frac{T_{HfO_2}/\varepsilon_{HfO_2}}{T_{SiO_2}/\varepsilon_{SiO_2} + T_{HfO_2}/\varepsilon_{HfO_2}} \quad \text{Eq.4.1}$$

Thus the trap energy at zero electric field E_{T0} can be extracted according to Eq.1.1 and equation becomes:

$$\ln\left(\frac{\tau_c}{\tau_e}\right) = \frac{1}{kT}\left(E_{T0} - E_F - q\frac{X_T}{T_{SiO_2}}V_{SiO_2} - q\Psi_s\right) \quad \text{Eq.4.2}$$

where k is the Boltzmann's constant and T is temperature. When V_G is equal to V_{G0}, the Eq.4.2 becomes:

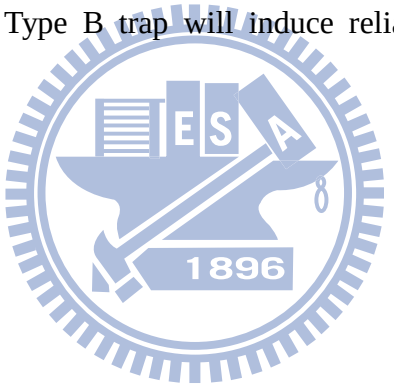
$$E_{T0} - E_F = q\frac{X_T}{T_{SiO_2}}(V_{G0} - V_{FB} - \Psi_s) \times \frac{T_{SiO_2}/\varepsilon_{SiO_2}}{T_{SiO_2}/\varepsilon_{SiO_2} + T_{HfO_2}/\varepsilon_{HfO_2}} + q\Psi_s \quad \text{Eq.4.3}$$

Finally, the extraction of trap energy at zero electric field in other conditions listed in Table.2.

Moreover, traps in the triangular area in the E_{T0} over X_T plane can be extracted by RTN measurement as shown in Fig.4.4.[10] The equipotential line sweeps within this window by varying the applied gate voltage. Fig.4.5 shows the trap energy distribution in common case and our case. The former is measured in strong inversion

condition and surface potential variation rate is zero. But the latter was our measurement condition. Most of Type A trap locates within high-κ layer. And Type B trap located within high-κ metal gate interface surface.

It is found that Type B trap is observable when dielectric EOT scaling down as shown in Fig.4.6. Fig.4.7 demonstrates trap energy distribution in two different EOT devices. Type B trap concentrates in a defect band [10]. Thus the traps can be characterized by RTN measurement. It is found that Type B trap is observable due to $|V_{FB}|$ decreases. $|V_{FB}|$ decreases as device dielectric EOT is decrease.[11][12] When the defect band overlaps the triangle window, the trap can be characterized by RTN measurement. Average of nMOS RTN amplitudes in different types trap as shown in Fig.4.8. The amplitude of Type B trap will induce reliability problem in modern device.



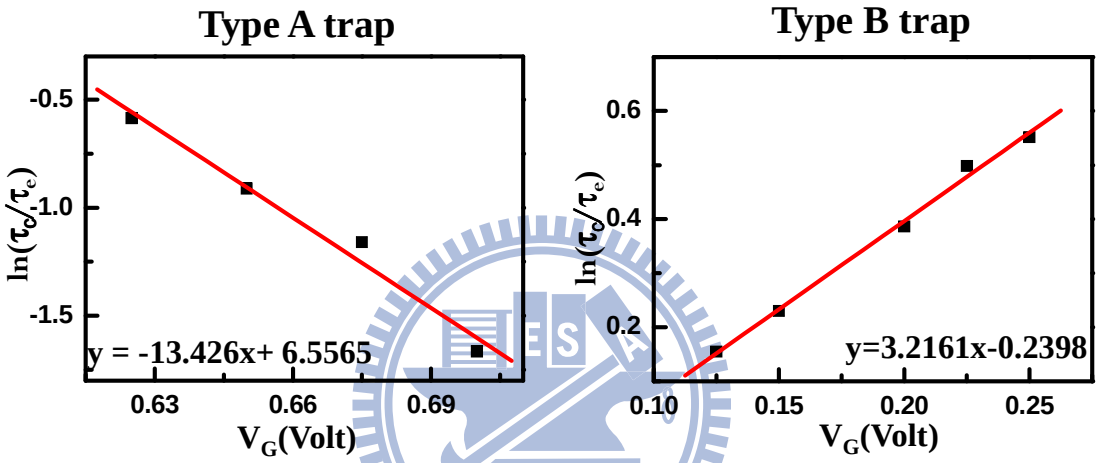


Fig.4.1 Definitions of two different types trap. We regard negative and positive V_G dependence as Type A trap and Type B trap.

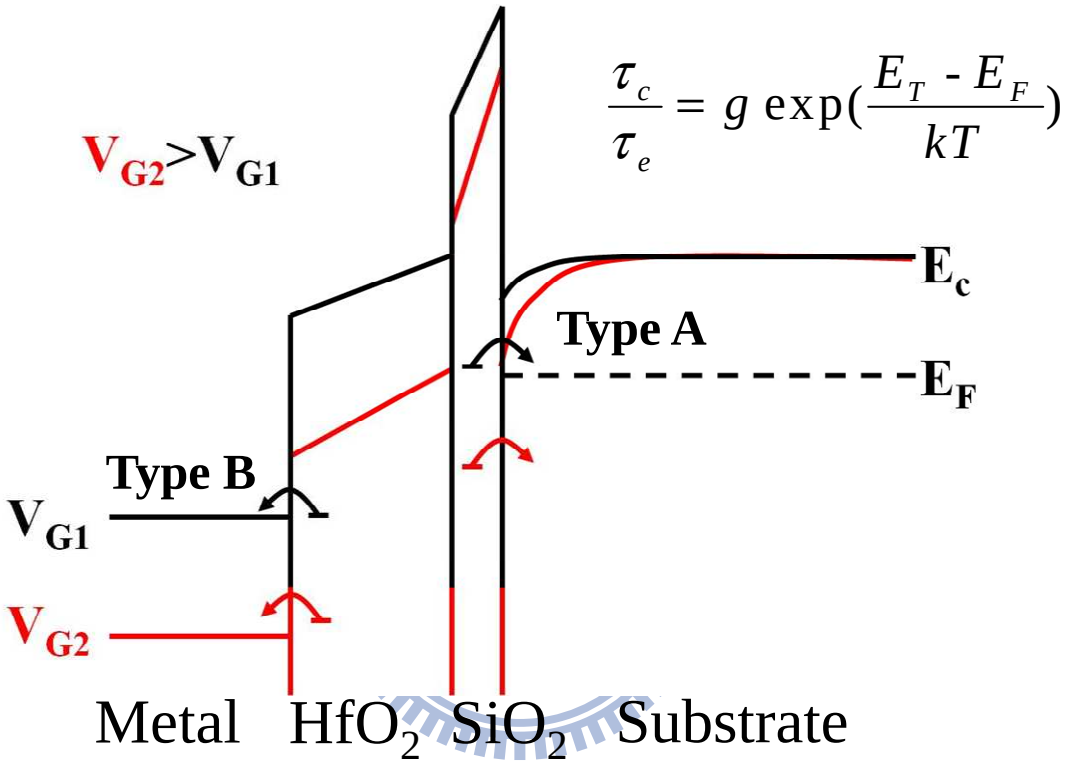


Fig.4.2 Cause of V_G dependent difference. Type A traps and Type B traps are interact with channel and gate electrode respectively.

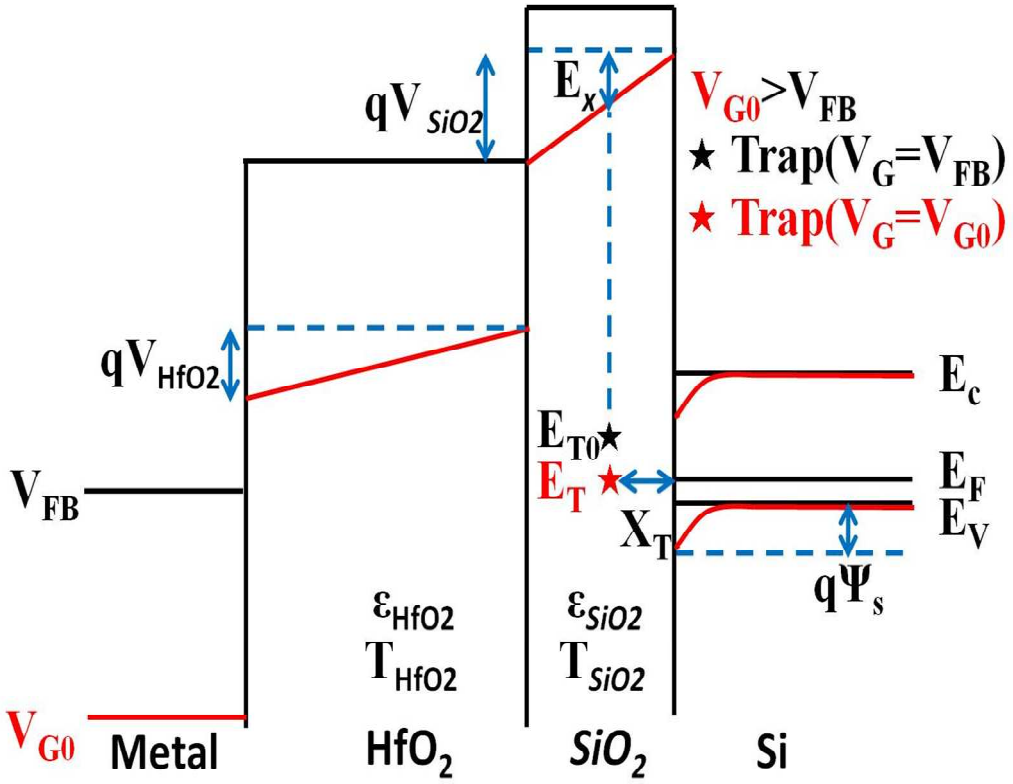


Fig.4.3 Illustrates band diagram about extraction of trap energy at zero electric field condition E_{T0}. The gate voltage varies from flat band voltage V_{FB} to V_{G0}. When $V_G=V_{G0}$, the trap energy E_T aligns to Fermi level E_F.

Table.2 is trap energy at zero electric field E_{T0} in different condition.

Trap in Oxide interact with channel

$$E_{T0}-E_F=q\frac{X_T}{T_{SiO2}}\left(V_{g0}-V_{FB}-\Psi_s\right)\times\frac{T_{SiO2}/\varepsilon_{SiO2}}{T_{SiO2}/\varepsilon_{SiO2}+T_{HfO2}/\varepsilon_{HfO2}}+q\Psi_s$$

Trap in High-k interact with channel

$$E_{T0}-E_F=q\left[\begin{array}{l}\left(V_{g0}-V_{FB}-\Psi_s\right)\dfrac{T_{SiO2}/\varepsilon_{SiO2}}{T_{SiO2}/\varepsilon_{SiO2}+T_{HfO2}/\varepsilon_{HfO2}}+\\ \left(V_{g0}-V_{FB}-\Psi_s\right)\dfrac{T_{HfO2}/\varepsilon_{HfO2}}{T_{SiO2}/\varepsilon_{SiO2}+T_{HfO2}/\varepsilon_{HfO2}}\dfrac{X_T-T_{SiO2}}{T_{HfO2}}\end{array}\right]+q\Psi_s$$

Trap in Oxide interact with gate electrode

$$E_{T0}-E_F=-q\left[\begin{array}{l}\left(V_{g0}-V_{FB}-\Psi_s\right)\dfrac{T_{HfO2}/\varepsilon_{HfO2}}{T_{SiO2}/\varepsilon_{SiO2}+T_{HfO2}/\varepsilon_{HfO2}}+\\ \left(V_{g0}-V_{FB}-\Psi_s\right)\dfrac{T_{SiO2}/\varepsilon_{SiO2}}{T_{SiO2}/\varepsilon_{SiO2}+T_{HfO2}/\varepsilon_{HfO2}}\left(1-\dfrac{X_T}{T_{SiO2}}\right)\end{array}\right]+q\Psi_s$$

Trap in High-k interact with gate electrode

$$E_{T0}-E_F=q\left[\begin{array}{l}\left(V_{g0}-V_{FB}-\Psi_s\right)\dfrac{T_{SiO2}/\varepsilon_{SiO2}}{T_{SiO2}/\varepsilon_{SiO2}+T_{HfO2}/\varepsilon_{HfO2}}-\\ \left(V_{g0}-V_{FB}-\Psi_s\right)\dfrac{T_{HfO2}/\varepsilon_{HfO2}}{T_{SiO2}/\varepsilon_{SiO2}+T_{HfO2}/\varepsilon_{HfO2}}\left(1-\dfrac{X_T-T_{SiO2}}{T_{HfO2}}\right)\end{array}\right]+q\Psi_s$$

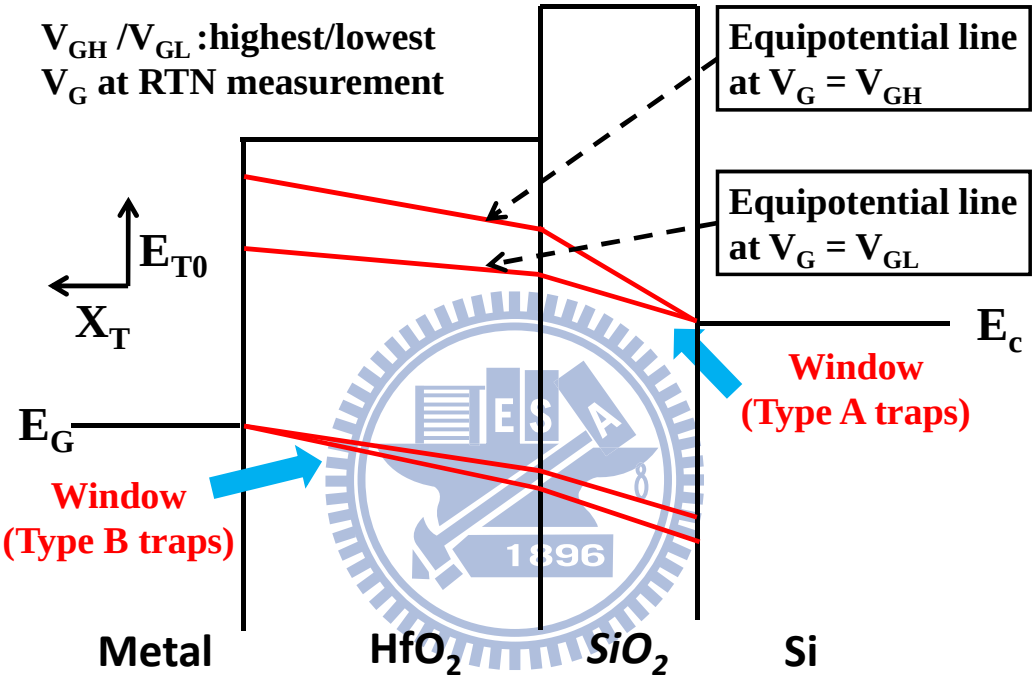


Fig.4.4 Window on E_{T0} over X_T plane where the trap locates within the window can be characterized.

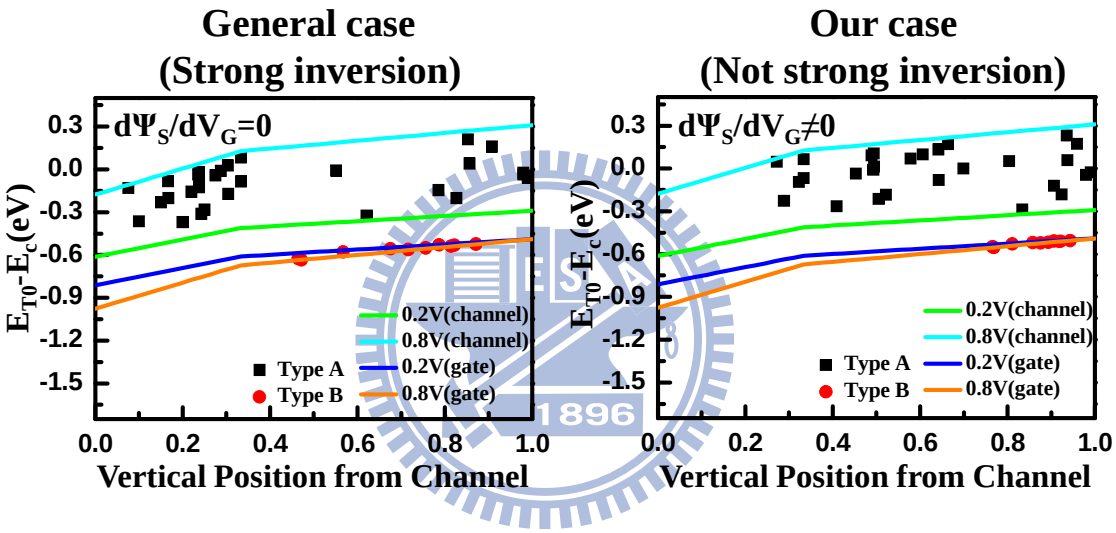


Fig.4.5 Shows the traps energy distribution in common case and our case. For our devices, we consider surface potential variation rate.

Type of RTN traps	Type A (trap interact with channel)	Type B (trap interact with gate)
EOT=7.8Å	28	10
EOT=12.89Å	37	0

Fig.4.6 Shows the number of traps in different EOT devices. Type B traps is observable when EOT scaling down to 7.8Å.

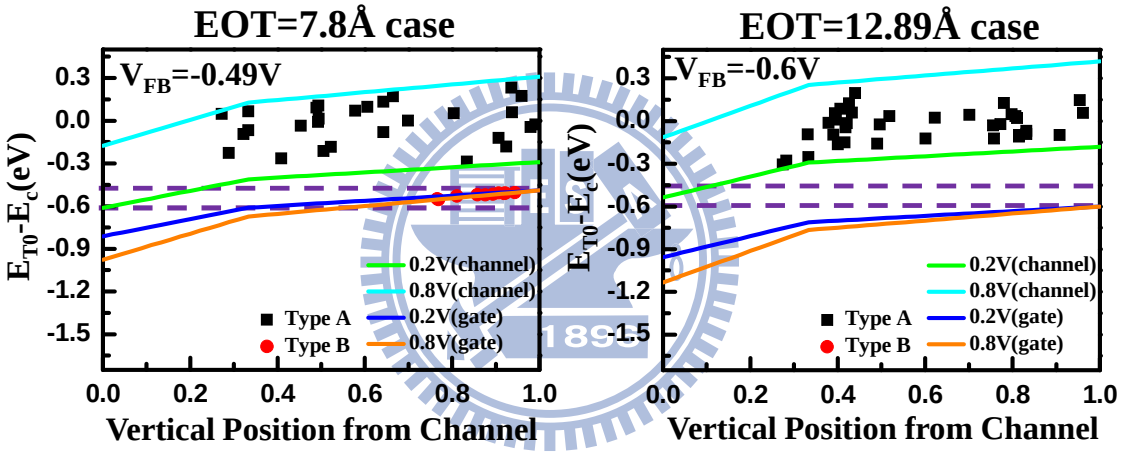


Fig.4.7 Type B trap is observable due to $|V_{FB}|$ decreases. Therefore the defect band overlap the triangle window, Type B trap can be characterized.

Type of RTN traps	Type A (trap interact with channel)	Type B (trap interact with gate)
Average of RTN amplitude	2.28%	2.064%

Fig.4.8 The average of RTN amplitude of Type B trap is nearly equal to that of Type A. Type B trap will induce reliability problems in modern devices.

Chapter 5

Conclusion

A method demonstrated in this thesis to extract trap of position along vertical direction (channel surface to gate electrode) and lateral direction (source to drain). This method can help us to extract the trap profile to device. Moreover, RTN amplitude is dominant by percolation effect. When device EOT becomes thinner, the Type B trap is observable due to $|V_{FB}|$ decreases. Type B trap will induce severe reliability problem in the modern device.

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