國 立 交 通 大 學

電 信 工 程 學 系 碩 士 班

碩 士 論 文

單晶片溫度感測器中的三角積分調變器之設計與製作

The Design and Implementation of Sigma-Delta Modulator for CMOS Monolithic Temperature Sensors

研 究 生：吳 書 豪

指導教授：闕 河 鳴 博士

西元二００四年七月

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研 究 生：吳書豪　　Student：Su-How Wu

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中文摘要

本研究目的是設計出一個低功率、高準確性的類比數位轉換器，並必須具有較大且較高的工作溫度區間。其功能是實現介於晶片型溫度感測器和內嵌控溫單元的介面電路，因此對於使用在晶片系統上的溫度管理系統而言是相當重要的。包括功率消耗、溫度範圍、製程相容性、、等挑戰，都使得這個類比數位轉換器的設計變的相當困難。本論文提出一個採用台積電 0.25 微米互補式金氧半標準製程的過取樣三角積分調變器原型晶片，其量測結果能達到八位元準位和極低功率消耗的表現，這樣的研究成果符合溫度管理系統所需的規格。除此之外，因為設計流程中已考慮到製程縮小的趨勢，因此對於採用更先進製程的溫管理系統也得以實現，這使得超大型積體電路或是高集線密度的電路得以免去過熱的問題。

The Design and Implementation of Sigma-Delta Modulator for CMOS Monolithic Temperature Sensors

Student: Su-How Wu Advisor: Dr. Herming Chiueh

Department of Communication Engineering

National Chiao Tung University

Hsinchu, Taiwan

Abstract

In this research, a low power high accuracy analog to digital converters (ADCs) with higher and wider temperature rang is designed. The proposed design plays an important role in modern system-on-chip thermal management system, which acts as an interface circuitry between monolithic temperature sensors and thermal management unit. Several challenges exists, including temperature range, power dissipation requirements and processing technology compatibility, which cause the design of such an ADC become a difficult work. This thesis examines a practical design of oversampling ADC based on sigma-delta modulation with thermal considerations. The prototype is fabricated in a TSMC 0.25μm standard CMOS process. The experimental result achieves eight bits resolutions and dissipates only a few mw which fulfill the system requirements of targeting thermal management design. Besides these requirements, the processing scaling of proposed ADC is considered in order to be compatible with targeting SoC fabrication technology. The integration of monolithic temperature sensor, proposed ADC and thermal management unit keep the progressing trend of modern VLSI and high-density circuits without thermal problems.

Acknowledgments

本篇論文得以順利完成，首先要感謝的是我的指導教授闕河鳴博士。闕老師總在研究遇到瓶頸的時候給予寶貴的建議，使我得以突破與進步。除此之外，老師在平日培養學生獨立思考與分析問題的能力，更使我在研究領域建立正確的態度。

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最後，我要感謝父母的栽培與弟妹的鼓勵，以及所有關心我的家人與朋友，唯有藉著大家的愛護和幫忙，才能造就今日的我。

我誠心感謝上述提攜或幫助過我的你們，謝謝大家並祝福大家。

吳書豪

July, 19, 2004

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List of Abbreviations and Symbols

AC	Alternative Current
ADC	Analog to Digital Converter
Av	Open loop gain
BW	Bandwidth
CAD	Computer-Aided Design
CDS	Correlated Double Sampling
CMFB	Common Mode Feedback
CMOS	Complementary Metal-Oxide Semiconductor
CMRR	Common Mode rejection ratio
DAC	Digital to Analog Converter
DC	Direct current
DFT	Discrete Fourier Transform
DNL	Differential Nonlinearity
DR	Dynamic Range
DSP	Discrete-Time Signal Processing
DUT	Device Under Test
ENOB	Effective Number Of Bits
FFT	Fast Fourier Transform
fc	Input Cutoff Frequency
fs	Sampling Frequency
Fu	Unit-gain Frequency
gm	Transconductance
ICMR	Input Common Mode Range
I_D	Drain Current
INL	Integral Nonlinearity
k	Boltzmann's constant
LSB	The Least Significant bit
M	Oversampling Ratio
m	m-order Sigma-Delta Modulator
N_{TF}	Noise transfer function
OPAMP	Operational Amplifier
OSR	Oversampling Ratio
PCB	Printed Circuit Board
PSD	Power Spectral Density
PSRR	Power Supply rejection ratio

Px	Power of quantity x, i.e. *Pin, Pe*
R	Capacitor Ratio
rds	CMOS output resistance
RMS	Root Means Square
Ron	turn-on resistance of switches
S	Device Ratio, namely *W/L*
SC	Switched-Capacitor
SCI	Switched-Capacitor Integrator
SDM	Sigma-Delta Modulator
SFDR	Spurious-Free Dynamic Range
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SoC	System On Chip
SR	Slew Rate
S_{TF}	Signal transfer function
T	Absolute temperature
THD	Total Harmonic Distortion
Vds	Drain to Source Voltage
Vgs	Gate to Source Voltage
VLSI	Very Large Scale Integrated
Vov	CMOS Overdrive Voltage
Vth	CMOS Threshold Voltage
ZTC	Zero-Temperature-Coefficient

Chapter1

Introduction

1.1 Motivation

Increases in circuit density and clock speed in modern VLSI design brought thermal issues into the spotlight of high-speed VLSI design [1]. Previous research has indicated that the thermal problem in modern integrated circuits can cause a significant performance decay [2] as well as reducing of circuitry reliability [3-6]. Local overheating in even one spot of high-density circuits, such as CPUs and high-speed mixed-signal circuits [7, 8] can cause the whole system crashed. The reasons include clock synchronization problems, parameter mismatches or other coefficient changes due to the uneven heat-up on a single chip [2]. In order to avoid thermal damages, early detection of overheating and properly handling such events are necessary.

Recent research has proposed the utilization of a thermal management system [9, 10] for large scale integrated circuits. In such design, adapting cooling and temperature monitoring mechanisms are widely used. However, implementation of on–chip thermal management systems, as shown in Figure 1.1, consist several challenges: embedded sensors, accurate ADCs, low power circuitry, and small physical area. In order to overcome such challenges, this thesis focuses on the design and the analysis of suitable ADC for thermal manager systems. The characteristics of this ADC includes following requirements [5]:

- Compatibility with the target process without any additional fabrication step;
- Low power consumption;
- A reasonably wide temperature range;
- Small active area;
- Accuracy and long term stability;

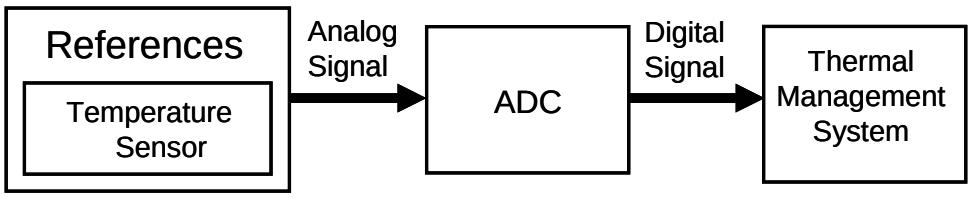

Figure 1.1 Building blocks of thermal management system

The implementation of thermal-aware ADCs in modern deep-sub-micron CMOS technology implies servile difficulties [1, 5].The most important design aspect of ADC is accuracy. The specification for conventional applications is 2 ^{o}C in a limited temperature range from -20 ^{o}C to 100 ^{o}C. Since thermal sensors has maximum inaccuracy of approximately 1 ^{o}C can be met at room temperature. Assuming that errors introduced by ADCs can be neglected, that indicates the resolution of such ADCs are higher than seven bits [11]. Nyquist rate ADCs can effectively produce digital codes without followed processing, but hard to achieve high resolution due to mismatching in CMOS process at elevated temperature, furthermore such architecture are difficult to maintain long term stability over wide temperature range. By contrast, the oversampling ADCs based on sigma-delta-modulator (SDM) structure are generally robust to several expected impairments, such as decreased amplifier open-loop gain and increased comparator offset [12]. As well as, the SDM enables nearly unlimited high resolution data conversion without precise matching due to inherent linearity one bit ADC and feedback DAC [13]. Additionally, some great benefits to accomplish SDMs in CMOS technology, for instant, circuitry are complicated by low power and a sample-and-hold circuit is not required at the input. The drawback of SDM is its low speed operation. But the thermal disturbance rate is reckoned into millisecond and the worse case of temperature sensor is specified to hundreds of samples, giving a required bandwidth of few kilo-hertz scale [11].It should be concluded that according to the trade-off between accuracy, simplicity and power consumption, the best candidate of ADC at high temperature is the SDM architecture, which consist of an analog filter and a coarse (often single-bit) quantizer connected together in a feedback loop operated in oversampling and noise shaping.

In practice, the imperfections of circuits, namely leakage integrators and several noise sources must be considered in system architecture. System level design used MATLAB determines the sensitivity to analog sub-circuits, and the circuit level specifications are decided. In addition to this architecture constraint, approaches to minimize high temperature disfigurement are taken into account in transistor level design for operation correct from ambient to elevated temperature.

This thesis describes the flow and results of the design and implementation of SDM for CMOS monolithic temperature sensors. The experimental SDM present herein have been fabricated in a standard 0.25μm CMOS technology, and provides 8 bits resolution at 25^{o}C and 7 bits resolution at 125^{o}C as well as dissipation only a few milliwatts.

1.2 Organization

In Chapter 2, the beginning is the overview of analog-to digital converters (ADC) consists of basic characteristics and classification. After them, quantization issues, wherein the principles of oversampling and noise shaping technology are introduced mathematically. Then diverse structures of sigma-delta modulators (SDM) and performance metrics end this chapter.

Chapter 3 represents system level design considerations, including the analysis of error mechanisms, high temperature issue, design trade-offs. All of limitations can construct a behavioral modeling of SDM to determine system characteristics.

Chapter 4 discusses the topics of sub-circuits that will be used to realize an actual integrated circuit, which covers an operational amplifier (OPAMP), a comparator, switches and capacitors, and the feedback path. The simulation results and device ratios are given at each section. The circuit level, transistor level, and layout level design will be described in sequence.

In chapter 5, the testing environment is present, including the instruments and external testing circuits on printed circuit board (PCB). Experimental results for a SDM, which is fabricated in a 0.25μm 1P5M 3.3V standard CMOS with MIM process, will be plotted and summarized.

Chapter2

Fundamentals of SDM

This chapter begins with a brief overview of analog-digital converters (ADC) in the aspects of speed and architecture. Following by the classification of ADC, a quantization error is considered and defined mathematically. A subclass of oversampling ADC based on noise shaping topologies is then examined, which referred to various architectures of sigma-delta modulators (SDM). The performance metrics of targeting ADC is then described in the end of this chapter.

2.1 A brief introduction of ADCs

ADCs, or equivalently quantizers, are fed a continuous-time analog signal to convert discrete-levels and play the most important role in signal processing. A pre-filter called an antialiasing filter is necessary to avoid off high frequency signals back into the baseband of the ADC, is usually followed by a sample-and-hold circuit that maintain the input signal constant during the time this signal is converted to an equivalent output code. This time is called the conversion time of the ADC. Depending on its speed and accuracy, ADCs are used in signal-processing applications, for instance, video, radio, radar, and telecommunications.

According to input bandwidth, there are three categories of ADCs, and are listed in Table 2.1 below. All of them are Nyquist-rate ADCs except oversampling structure, and the carefully definitions will be examined in the following section.

Table 2.1 Various kinds of ADCs

Category	***Structure***
Low-to-Medium Speed High Accuracy	Integrating Oversampling
Medium Speed Medium Accuracy	Successive approximation Algorithmic
High Speed Low-to-Medium Accuracy	Flash, Two-step, Interpolating, Folding, Pipelined, Time-interleaved

In the viewpoint of system architecture shown in Figure 2.1, the Nyquist-rate ADC can cover signal directly, the relationship between digital output and analog input is one-on-one. On the contrast, non-Nyquist-rate ADCs (oversampling ADCs) need a register to store a sequence of digital output for one analog input. Another key point of non-Nyquist-rate ADCs is that, the operational frequency of the modulators and digital filters is above Nyquist-rate that is why they are called "oversampling".

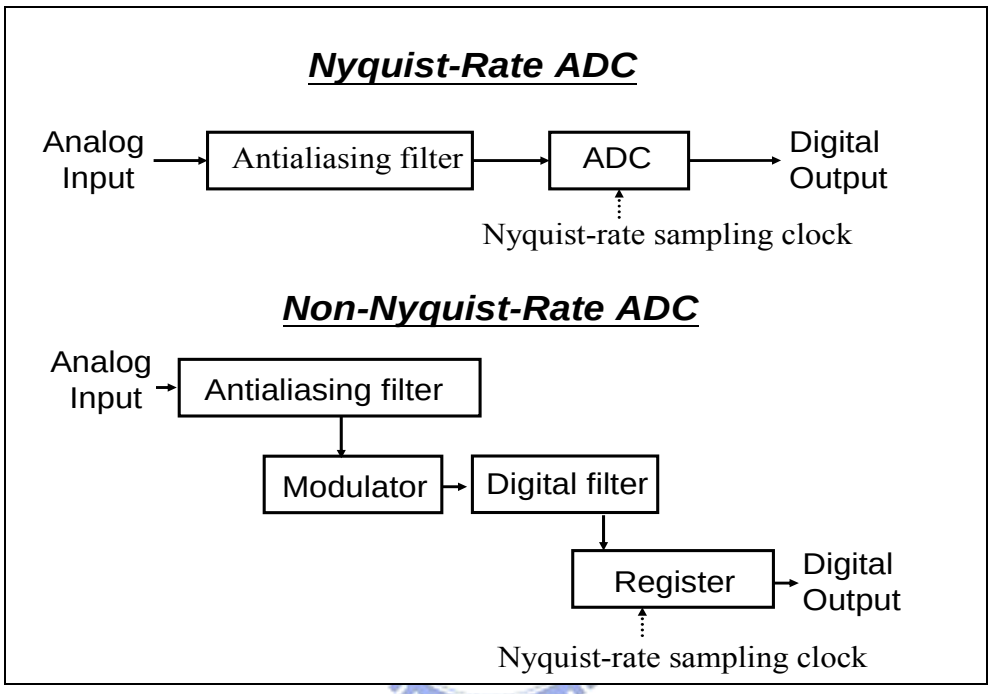

Figure 2.1 System architectures of ADCs

Assume discrete-level of a quantizer outputs are transferred to specific states by references, which has the same voltage level with input signal. It is easy to plot transfer curve, like Figure 2.2(a) next page, and this diagram helps to define several basic properties of ADCs.

1. The number of output states can be estimated by binary and referred as *N* bits resolutions. Thus *N* bits ADCs can map input signals into 2^N output levels.
2. The full scale input range which a quantizer can handle is called *A*. If the input signal exceed *A*, the quantizer is overload.
3. The separation of output level is the least significant bit (LSB). Generally speaking, the linear gain of ADCs is one, so the relationship between *A*, *N* and LSB, can be written as:

$$A = LSB \times (2^N - 1) \cong LSB \times 2^N \qquad (2.1)$$

4. The quantization noise (quantization error) is the diversity between the input and

output of the quantizer and can be plotted versus input signal, as Figure 2.2(b). If the magnitude of input is less than *A*, its noise error is less than a half of LSB. On the contrast, the noise error greatly grows when the quantizer is overload.

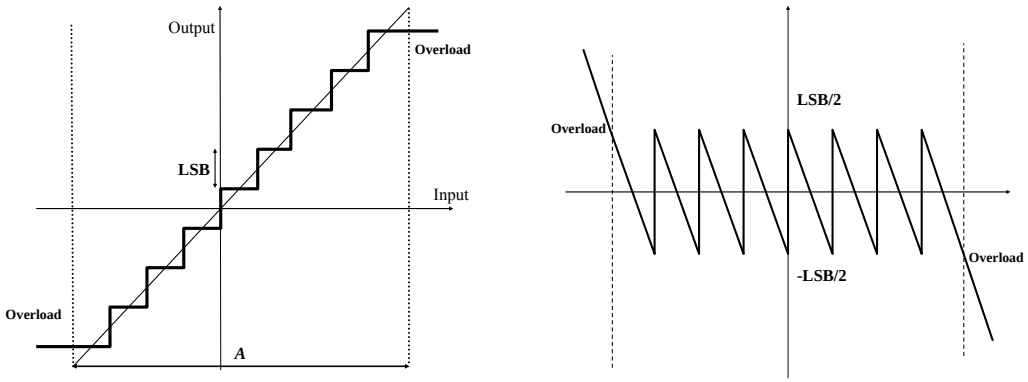

Figure 2.2 (a) Transfer curve of ADCs (b) Quantization noise

The present trend of ADCs is focused on (a) high resolution, more than 14 bits (b) high speed, more than 100MHz (c) low power. A conflict, however, is likely to exist between each of them when design a real quantizer.

2.2 Quantization Noise

Previous study is focused on static characteristic of ADCs. Next we will focus on its dynamic characteristic. Before that, it is appropriate to use the "white noise approximation" when followed conditions are satisfied [14]:

1. The noise sequence is a sample sequence of a stationary random process.
2. The noise sequence is uncorrelated with the input.
3. The random variables of the noise process are uncorrelated.
4. The probability distribution of the noise process is uniform over the range of quantization noise.

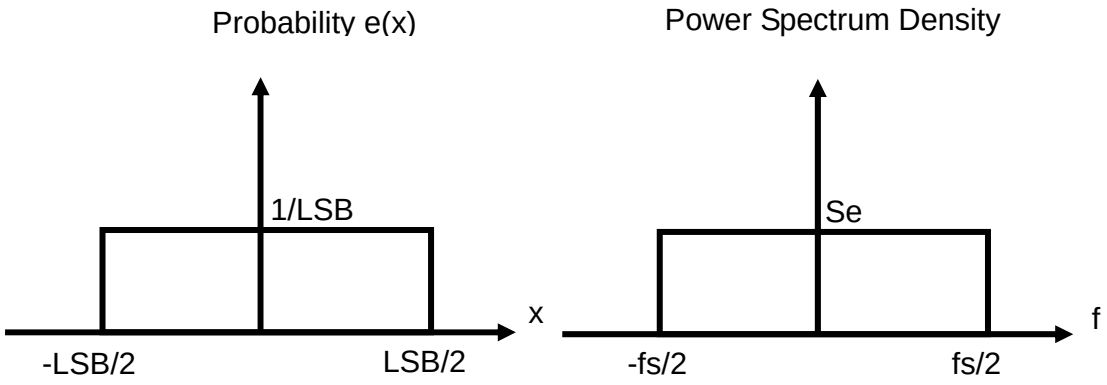

Figure 2.3 Probability and power spectral density function of quantization noise

Therefore the probability density function and the power spectral density function of quantization noise can be sketch in Figure 2.3. Above left figure shows the double side band frequency and leads into frequency domain analysis. On the other words, it is intended as an investigation of dynamic characteristic of ADCs. From Figure 2.3, the total noise power can be estimated by:

$$Pe = \int_{-fs/2}^{fs/2} Se^2(f)df = Se^2 \times fs = \int_{-LSB/2}^{LSB/2} \frac{1}{LSB} x^2 dx = \frac{LSB^2}{12} \tag{2.2}$$

$$\Rightarrow Se = \sqrt{\frac{LSB^2}{12\,fs}} \tag{2.3}$$

Where the *fs* is the sampling rate and *Se* is the power spectral density. By the way, owing to an antialiasing filter, input signal of a quantizer is band limited, the bandwidth is referred as *fc*, the *fs* must more than double of *fc*. Because the transfer curve, like Figure 2.2(a), can not be found in frequency domain, we need to define the resolution of ADCs by signal to noise ration (SNR), which is expressed as:

$$SNR = 10 \times Log\left(\frac{Input\ signal\ power}{Output\ noise\ power}\right) = 6.02\,ENOB + 1.76 \tag{2.4}$$

ENOB is the effective number of bits for ADCs. For a given *fc*, the quantizer can be classified into two groups according to sampling rate, Nyquist-rate and oversampling. Further speaking, oversampling ADCs can be divided into white noise and noise shaping. Three kinds of ADCs mentioned overhead are illustrated in Figure 2.4 and are explained below:

1. Nyquist-rate: the sampling rate is close to double of *fc*.
2. Oversampling: the sampling rate is more than double of *fc*.
3. Noise shaping: belong to oversampling group. The probability distribution of the noise process is various over the range of quantization noise.

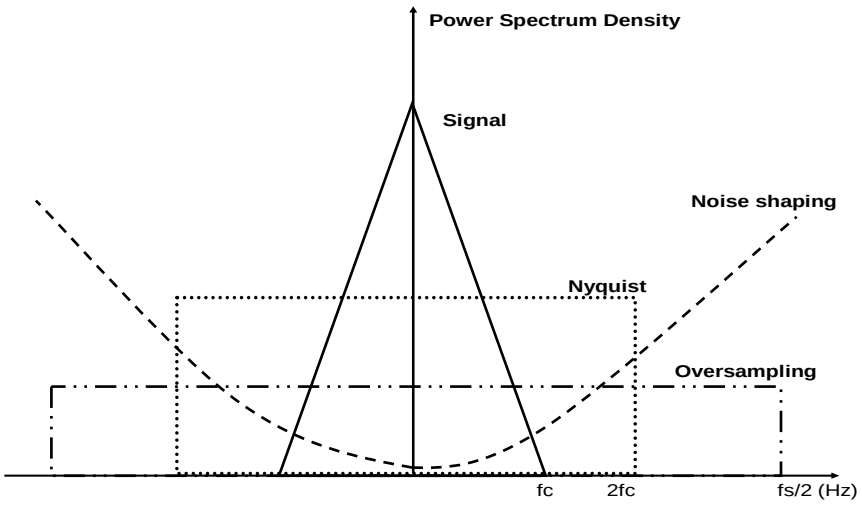

Figure 2.4 Three categories of ADCs

The power spectrum density of white noise is altered from uniform to noise shaping by a noise transform function, N_{TF}. Suppose N_{TF} can be expressed as $(1-z^{-1})^m$, then we call it m-order sigma-delta modulator (SDM) and the noise shaping can be illustrated in Figure 2.5. It is clear that most of quantization noises are restrained in low frequency and shaped out of band to sharp increase signal to noise ration (SNR) in Nyquist frequency for higher resolution. In order to evaluate its resolution, we estimate the noise power again:

$$\left|N_{TF}(e^{jwTs})\right| = \left|2\sin(\frac{wTs}{2})\right|^m = \left|2\sin(\frac{\pi f}{fs})\right|^m \cong \left|\frac{2\pi f}{fs}\right|^m \quad when\ f \ll fs$$

$$P_e' = \int_{-fc}^{fc} Se^2 \left|N_{TF}(f)\right|^2 df\ ,\ Pe'\ is\ shaped\ noise\ power$$

$$= Se^2 \times \frac{\pi^{2m}}{2^m+1} \times \frac{2^{2m+1} fc^{2m+1}}{fs^{2m+1}}\ ,\ substitue\ Se^2\ by\ equation\ (2.2-2)$$

$$= \frac{LSB^2}{12} \times \frac{\pi^{2m}}{2^m+1} \times M^{-(2m+1)}\ ,\ M\ is\ oversampling\ ratio = \frac{fs}{2\,fc} \qquad (2.5)$$

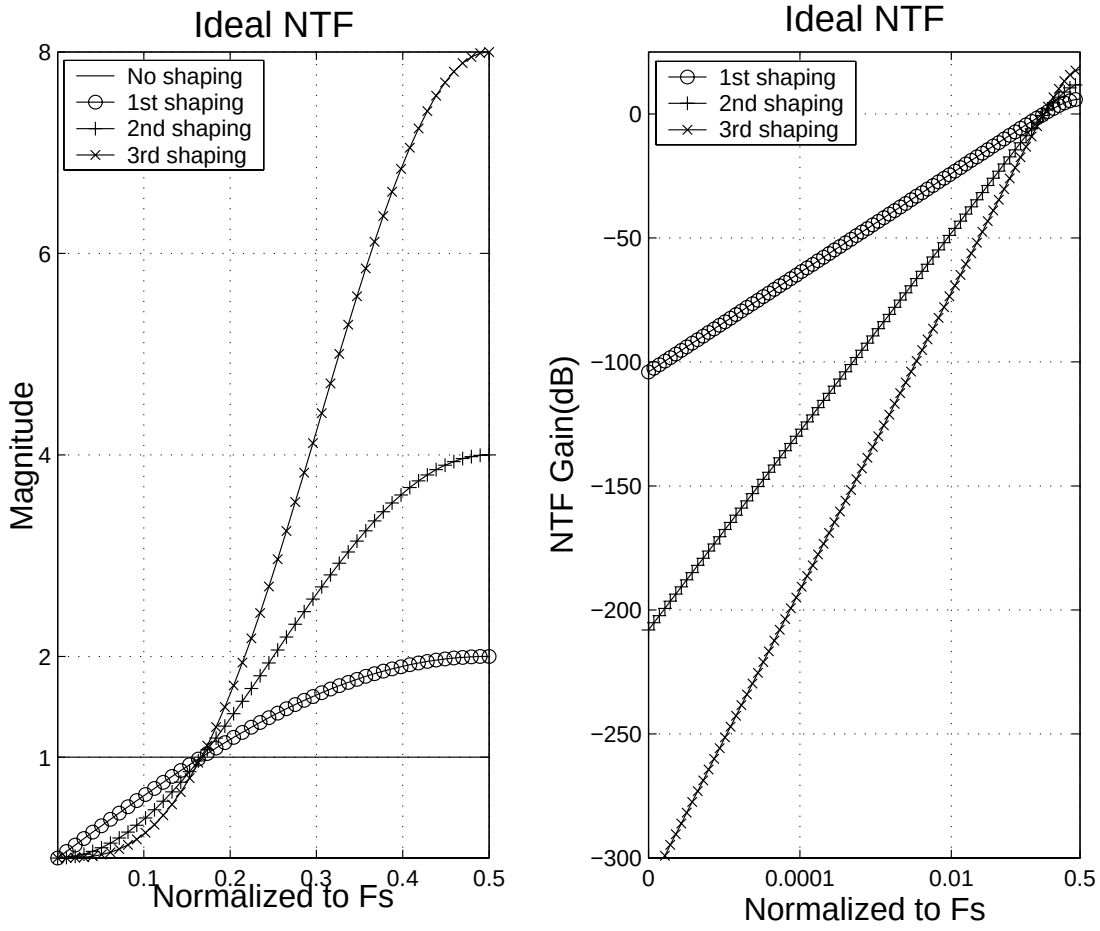

Figure 2.5 The magnitude and gain of N_{TF}

For a sinusoidal signal has full scale input, the input signal power is:

$$Pin = \frac{(A/2)^2}{2} = \frac{(LSB \times 2^{N-1})^2}{2} = \frac{4^N}{8} \times LSB^2 \tag{2.6}$$

Therefore, the SNR inside the Nyquist bandwidth is derived:

$$\begin{aligned} SNR &= 10Log(\frac{Pin}{P_e^{'}}) = 6.02ENOB + 1.76 \\ &= 10Log[\frac{4^N \times 12 \times (2m+1)}{8 \times \pi^{2m}} \times M^{2m+1}] \\ &= 6.02N + 1.76 + (2m+1)10LogM - 10Log\ \frac{\pi^{2m}}{2m+1} \end{aligned} \tag{2.7}$$

From above equation, it is clear that:

1. Without oversampling, without SDM structure, thus M=m=0

$$SNR = 6.02ENOB + 1.76 = 6.02N + 1.76 \tag{2.8}$$

2. With oversampling, without SDM structure, thus m=0

$$SNR = 6.02ENOB + 1.76 = 6.02N + 1.76 + 10LogM \tag{2.9}$$

3. With oversampling, with SDM structure

$$SNR = 6.02ENOB + 1.76 = 6.02N + 1.76 + (2m+1)10LogM - 10Log\ \frac{\pi^{2m}}{2m+1} \tag{2.10}$$

Where N is the initial bits of ADCs without oversampling or SDM structure, and ENOB is the effective one. We can conclude that, (a) a Nyquist-rate ADC can be express by equation (2.8) and the ENOB is N bits, (b) the higher sampling rate makes the higher resolution, (c) the higher order of SDM makes the higher resolution. Finally, let us devote a table, Table 2.2 and Figure 2.6, to examine the SDM structure.

Table 2.2 Summarize the SNR of SDM

Structure	SNR	Description
First-order	6.02N+1.76- 5.17+30LogM	doubling M , increase 9dB
Second-order	6.02N+1.76-12.90+50LogM	doubling M , increase 15dB
Third-order	6.02N+1.76-21.38+70LogM	doubling M , increase 21dB
m-order	Equation (2.1-10)	doubling M , increase (6m+3)dB

We may note, in passing, there are a lot of structures to implement noise shaping topology, SDM is just one of them but is also most feasible one. The reason is that recent CMOS VLSI technology focused on realizing high speed density packed

digital circuits, SDM used only one bit ADC and related analog signal processing circuits are usually have less precision requirements than others.

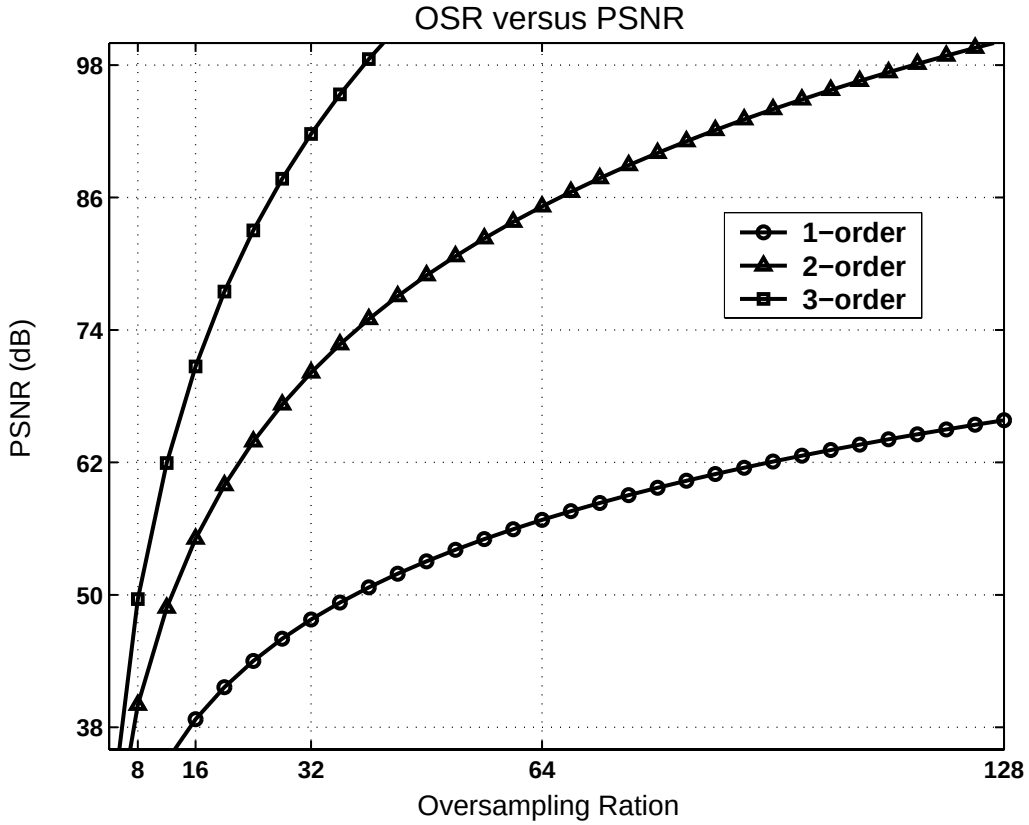

Figure 2.6 The SNR of SDM

2.3 SDM Architecture

We shall now look more carefully into the principles of SDM. In practice, recalling Figure 2.1, SDM just one of building blocks of oversampling ADCs. A digital filter and a register are needed to complete fully architecture. From the viewpoint of signal processing, SDM converts continuous analog signals to a sequence digital code, it is like an ADC. The sequence of digital code, however, consists of original signals and shaped quantization noise, a digital filter must remove unnecessary noise to return to original signals. Capitalize Figure 2.7 to realize the correlation between the time domain and the frequency domain of SDM [15]. By contrast, a Nyquist-rate ADC directly maps an analog input into a digital output without further processing. In viewpoint of system level, the latter can effectively generate digital codes, but rarely practical to achieve better than 12 bits resolution without error correction due to mismatching in CMOS process. In order to accomplish high resolution, SDM are widely adopted, for example, DVD-ROM, audio codec, ADSL, cell phone and so on. Briefly speaking, SDM exchange resolution in time for

that in amplitude by combining sampling at well above Nyquist rate with coarse quantizer embedded in order to suppress quantization noise appearing in signal band [16].

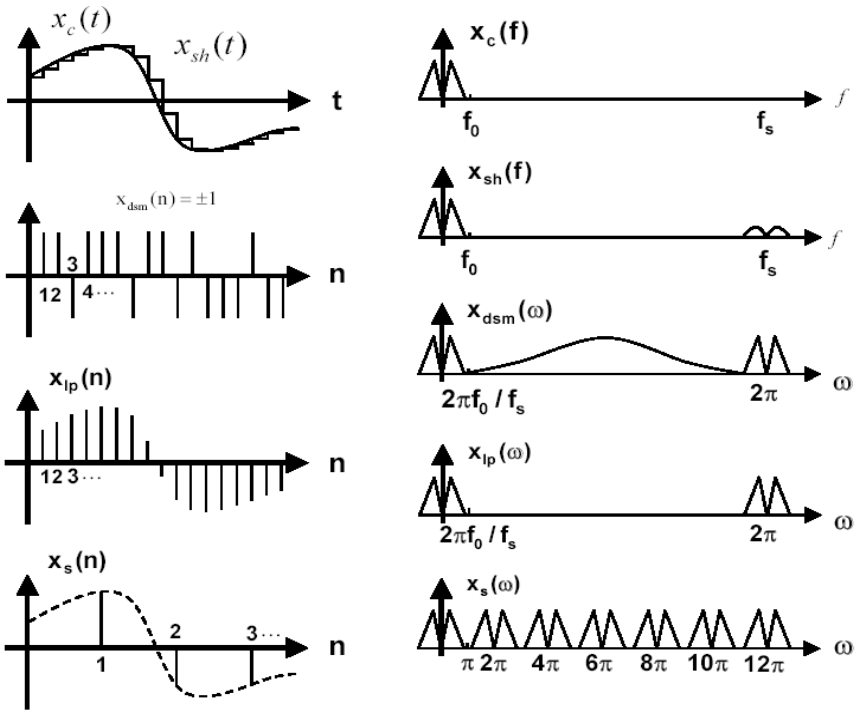

Figure 2.7 Analysis of time domain and frequency domain of SDM

We have defined the noise transfer function, N_{TF}, of SDM as $(1-z^{-1})^m$ in previous section. The use of feedback illustrated in Figure 2.8 next page to realize NTF of SDM is a familiar structure and has several advantages in CMOS technology, for instant:

- Relax the requirements placed on the analog circuitry at the expense of more complicated digital circuitry.
- High-resolution analog circuitry is complicated by low power and poor output impedance
- Reduced requirements on matching tolerances and amplifier gain.
- Simplify the requirements of anti-aliasing filter.
- A sample-and-hold is usually not required at the input.

Judging from above, SDM provide a robust structure to implement for (a) high resolution ADCs (b) low power system (c) disappointing environment. We need not elaborate on the points of the decimation filter, which are treated much more adequately in references. From the present, we shall confine our attention on various SDM architectures.

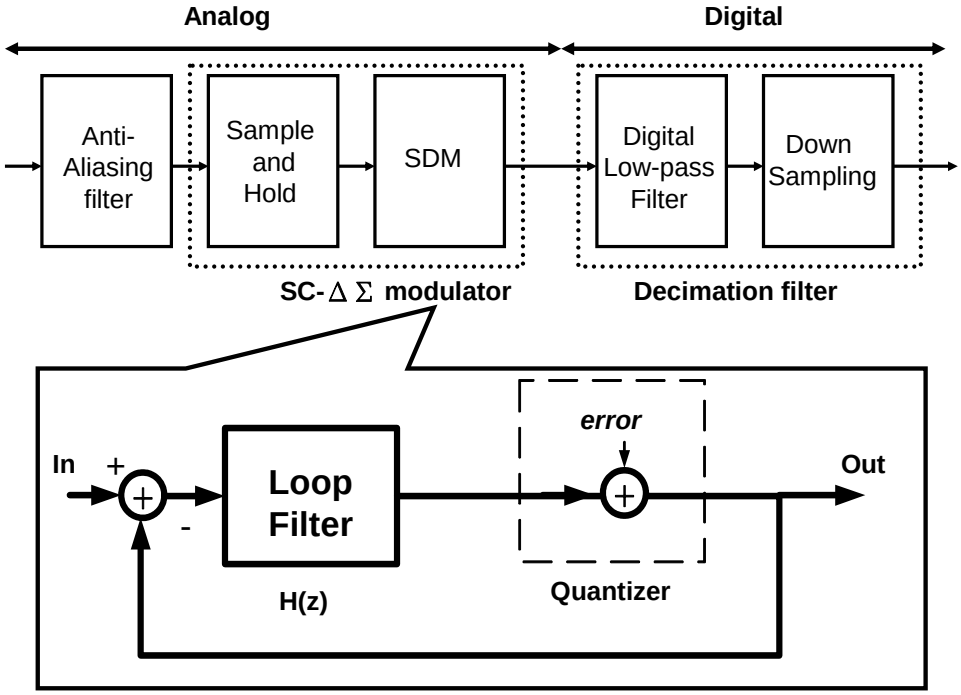

Figure 2.8 Building blocks of oversampling ADCs used SDM

2.3.1 First Order SDM

The first order SDM has a noise transfer function, $(1-z^{-1})$. In order to achieve high resolution, the oversampling ration (OSR), M, can be estimated by Table 2.2. Then it is clear that OSR more than 38 for 8 bits resolution, even more than 96 for 10bits resolution, therefore, the application is narrowed for ultra-low input bandwidth or unfavorable operational status.

Refer to Figure 2.8, the loop filter has transfer function, H(z). The output can be written in term of input and quantization error as:

$$\because Out(z) = E(z) + H(z)\left[In(z) - Out(z)\right]$$

$$\therefore Out(z) = S_{TF}(z)In(z) + N_{TF}(z)E(z)$$

$$H(z) = \frac{A(z)}{B(z)}$$

$$S_{TF}(z) = \frac{H(z)}{1+H(z)} = \frac{A(z)}{A(z)+B(z)} \tag{2.11}$$

$$N_{TF}(z) = \frac{1}{1+H(z)} = \frac{B(z)}{A(z)+B(z)} \tag{2.12}$$

Where N_{TF} and S_{TF} is noise and signal transfer function, respectively. We can observe that, the zeros of the N_{TF} are equal to the poles of the H(z). Therefore, in order to curtail noise power, maintain the H(z) is large and NTF(z) is small in the frequency band of interest. For instance, we can choose H(z) is a low-pass filter and $N_{TF}(z)$ is a high-pass filter to construct a low-pass sigma-delta modulator (LP-SDM)**.** Toward that, the simplest case of H(z) is $(z\text{-}1)^{-1}$, which is a discrete-time integrator, so the resulting output is :

$$Out(z) = z^{-1} In(z) + (1 - z^{-1}) E(z) \tag{2.13}$$

This shows that the output is delayed by one sample period. Ideally, a quantizer does not introduce amplitude distortion and has a linear phase characteristics [17].

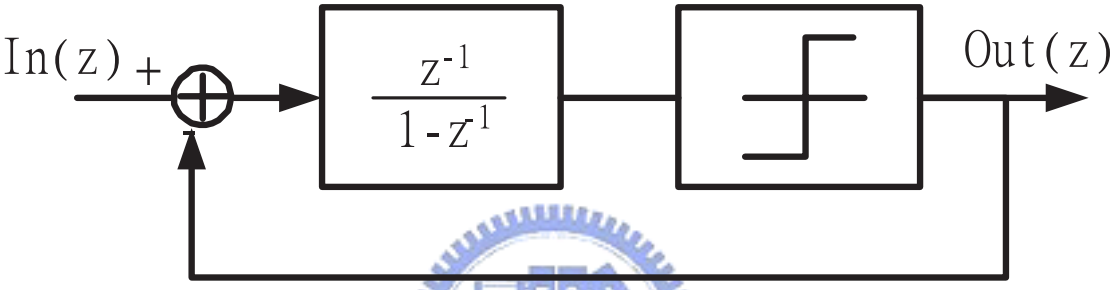

Figure 2.9 A first order SDM

2.3.2 Second Order SDM

The second order SDM is widely used, and Figure 2.10 shows the building blocks, and the output is:

$$Out(z) = z^{-1} In(z) + (1 - z^{-1})^2 E(z) \tag{2.14}$$

Note that, compared with first order SDM, the second order SDM provides more quantization noise suppression over the low frequency band, thus more noise power outside the input bandwidth [18]. Suppose OSR is 64, this structure can be a 12 bit ADC due to equation (2.10).

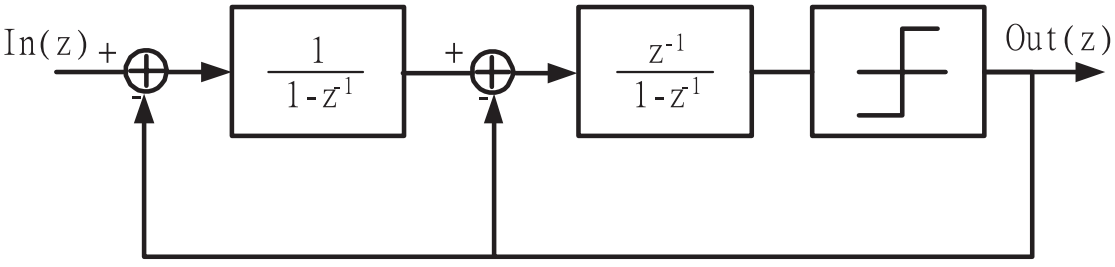

Figure 2.10 A second order SDM

2.3.3 Higher Order SDM

A high order SDM is often defined as a SDM with the number of order higher than three. It is obvious that higher order SDM requires lower OSR to achieve the same SNR, for instance, it can be a 13 bit ADC when OSR is 32. The order, however, is less than six is compatible in CMOS technology because of instability and mismatching problems. Stability of SDM is defined that as one in which the input to the quantizer remains bounded such that the quantization does not become overloaded. In fact, the stability of higher-order modulator is not well understood as they include a highly nonlinear element, especially embedded low-bit quantizers. A rule of thumb for a stable SDM is expressed in equation (2.15), but it has little rigorous justification. A useful stable criterion is proposed by [19].

$$\left|N_{TF}(e^{j\omega T})\right| \le 1.5 \; for \quad 0 \le \omega \le \pi \tag{2.15}$$

High order SDM is divided into signal-stage and multi-stage structures [20]. Single-stage structure contains Feed-forward (FF) modulator, Multiple-feedback (MF) modulator and others. Figure 2.11(a) and Figure 2.11(b) gives an example of them diagrammatically. Multi-stage structure (MASH) uses several stages instead of a single loop to reduce the quantization noise of the coarse quantizer. A second stage followed by a first order SDM shown in Figure 2.11(c) is used usually because it is insensitive to circuit performance.

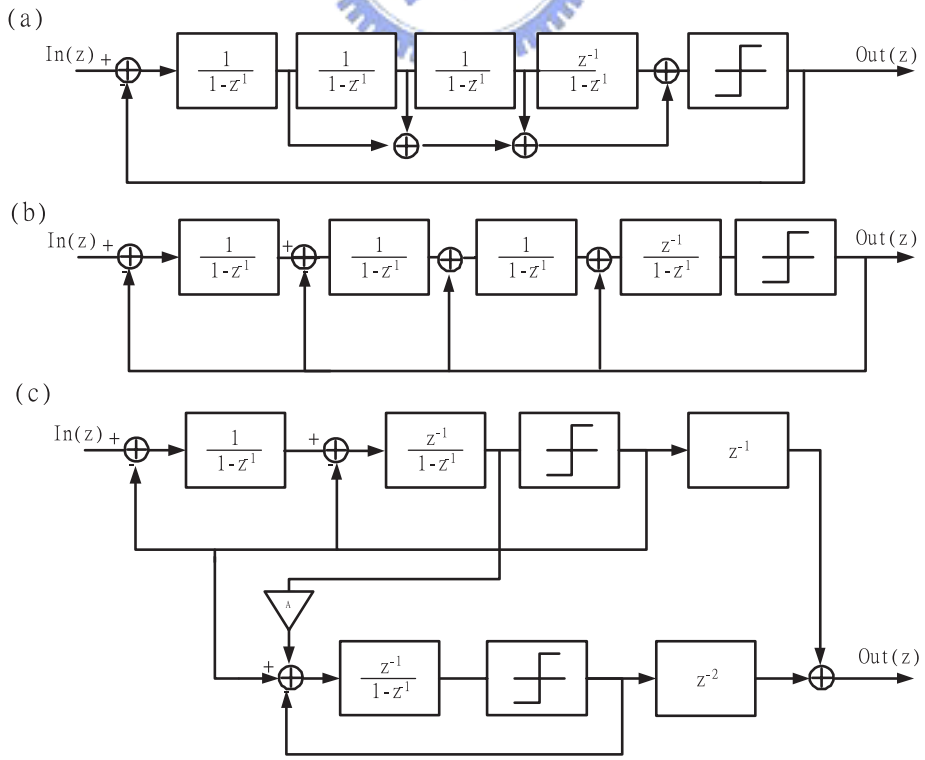

Figure 2.11 Higher order SDM

2.4 Performance Metrics

In practice, transfer characteristics are different from Figure 2.2 and Figure 2.4 because imperfections in a practical implementation. Performance metrics are used to describe the deviation are fall into static and dynamic categories which are main subject here.

Static performance metrics:

1. Offset: transfer curve shift, like Figure 2.12(a)
2. Gain error: conversion point shift, like Figure 2.12(b)
3. Non-monotonic: vertical jump is negative, like Figure 2.12(c)
4. Differential nonlinearity (DNL): shown in Figure 2.12(d)

$$DNL=\frac{S-LSB}{LSB} \quad (unit: LSB) \tag{2.16}$$

5. Integral nonlinearity (INL): shown in Figure 2.12(d)

$$INL = \frac{T}{LSB} \quad (unit : LSB) \tag{2.17}$$

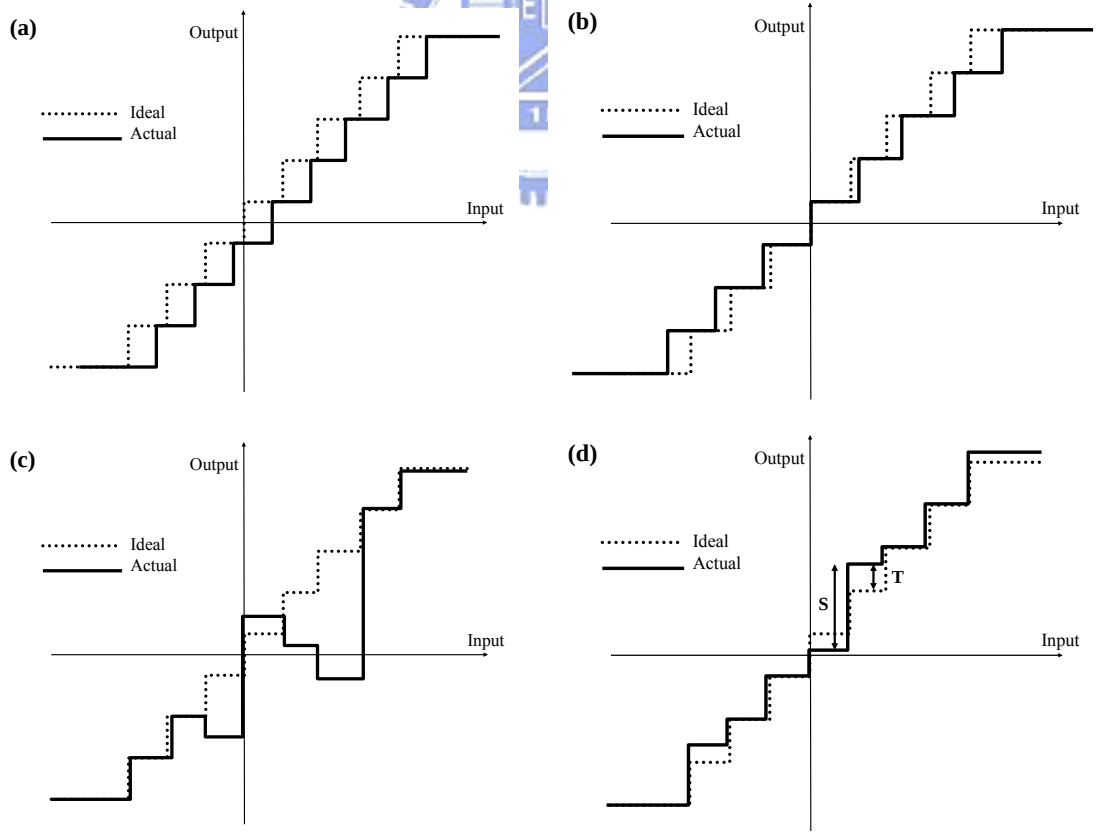

Figure 2.12 Static performance metrics

Dynamic performance metrics is measured with a low-noise full scale sine wave to the ADC, performed continuous conversions on the input signal, collect the conversion results, performed a Discrete Fourier Transform (DFT) to map into Fast Fourier Transform (FFT) spectrum. Some of these are listed below and the unit is "dB".

1. SNR: the abbreviation of "signal to noise ratio". Fundamental power divided by the power of the bins in the FFT other than DC, fundamental, and first N harmonic bins.
2. SNDR: the abbreviation of "signal to noise and distortion ratio", it is also called SINAD. Fundamental power divided by the power of the bins in the FFT other than DC, and fundamental bins.
3. SFDR: the abbreviation of "spurious free dynamic range". Difference between fundamental bin and the highest bin.
4. DR: the abbreviation of "dynamic range". Effective input range when SNR is one.
5. THD: the abbreviation of "total harmonic distortion". Power of first N harmonic bins divided by the power of fundamental bin.
6. ENOB: the abbreviation of "effective number of bits".

$$ENOB = \frac{SNR - 1.76}{6.02} \quad (unit : dB) \tag{2.18}$$

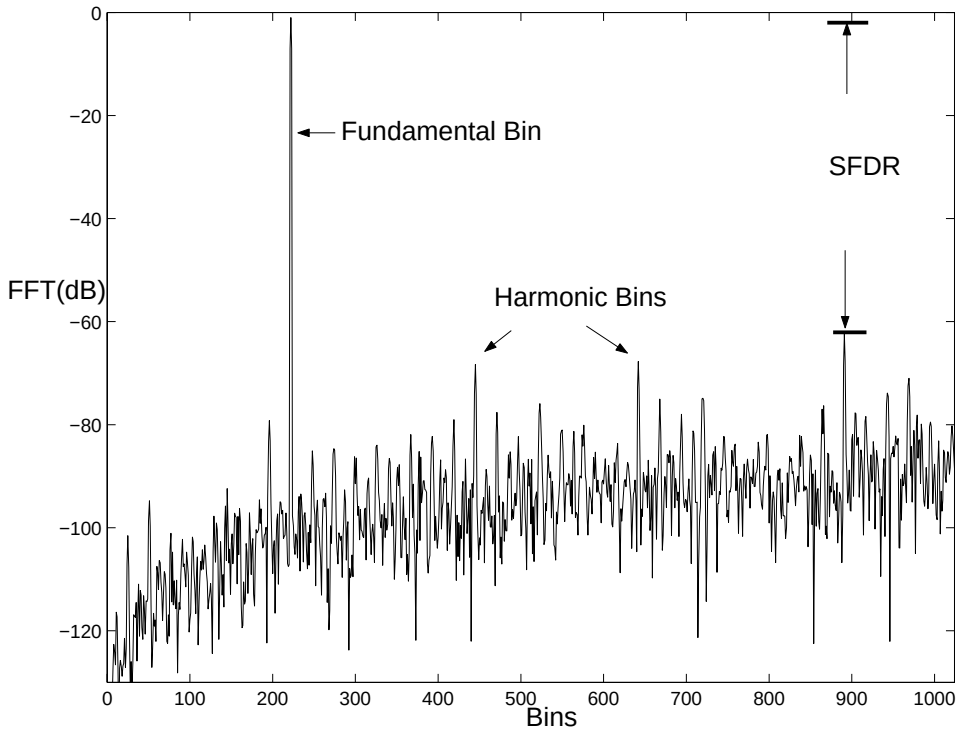

Figure 2.13 Dynamic performance metrics

Chapter3

System Level Design Considerations

This chapter discusses defects of actual SDM caused by thermal noise, OPAMP finite gain, clock jitter, and so on. Several mathematical methods are proposes to estimate the curtailed Peak SNR of SDM. In addition to this, design issues to overcome high temperature impact and leakage current are discussed in section 3.2. Both of them are major problems for proposed SDM design. In the end of this chapter, several approaches to overcome above limitation are proposed and the detail mechanisms of such improvement are discussed.

3.1 Limitations

A SDM used noise shaping topology gives rise to an increase of in-band SNR, and the Peak SNR can be obtained by equation (2.7), and the Figure 2.5 shows the quantization noise is suppressed in low frequency and increased in high frequency. However, the N_{TF} accomplished by switched-capacitor technology with OPAMP have two fundamental limitations, namely non-zero turn-on resistances of switches and non-ideal amplifier. The former generate the thermal noise, the latter contains finite gain, finite bandwidth, and slew rate.

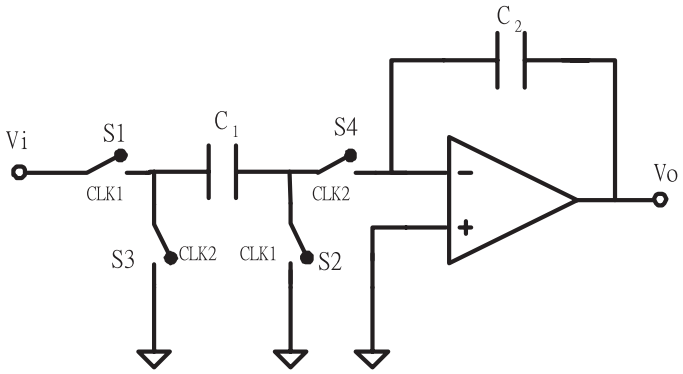

Figure 3.1 A SC integrator

A switched-capacitor integrator (SCI) is popularly adopted to accomplish N_{TF} in SDM structures. Figure 3.1 shows a SC integrator which has transfer function:

$$H(z) = \frac{C_1}{C_2} \times \frac{z^{-1}}{1-z^{-1}} = Ratio \times \frac{z^{-1}}{1-z^{-1}} \qquad (3.1)$$

Above equation is satisfied when DC gain is infinite, but the finite gain of this amplifier is considered now, then equation 3.1 is altered as:

$$H(z) = R \times \frac{z^{-1}}{\alpha - \beta z^{-1}} \tag{3.2}$$

$$\alpha = 1 + \frac{1}{Av}(1 + R) \qquad \beta = 1 + \frac{1}{Av}$$

Where *Av* is open loop gain and *R* is the capacitor ratio of SCI. So the first order SDM has:

$$S_{TF} = \frac{Rz^{-1}}{\alpha - (\beta - R)z^{-1}} \;\&\; N_{TF} = \frac{\alpha - \beta z^{-1}}{\alpha - (\beta - R)z^{-1}} \tag{3-3}$$

Then, N_{TF} can be calculated as equation below and illustrated in Figure 3.2:

$$N_{TF}(0.5\,fs) = \frac{2 + \frac{1}{Av}(2+R)}{(2-R) + \frac{1}{Av}(2+R)} = 1 + \frac{R}{(2-R) + \frac{1}{Av}(2+R)} \tag{3.4}$$

$$N_{TF}(dc) = \frac{1}{Av+1} \;\&\; N_{TF}(3dB) \cong \frac{1}{2\pi}\frac{R}{Av+1} \tag{3-5}$$

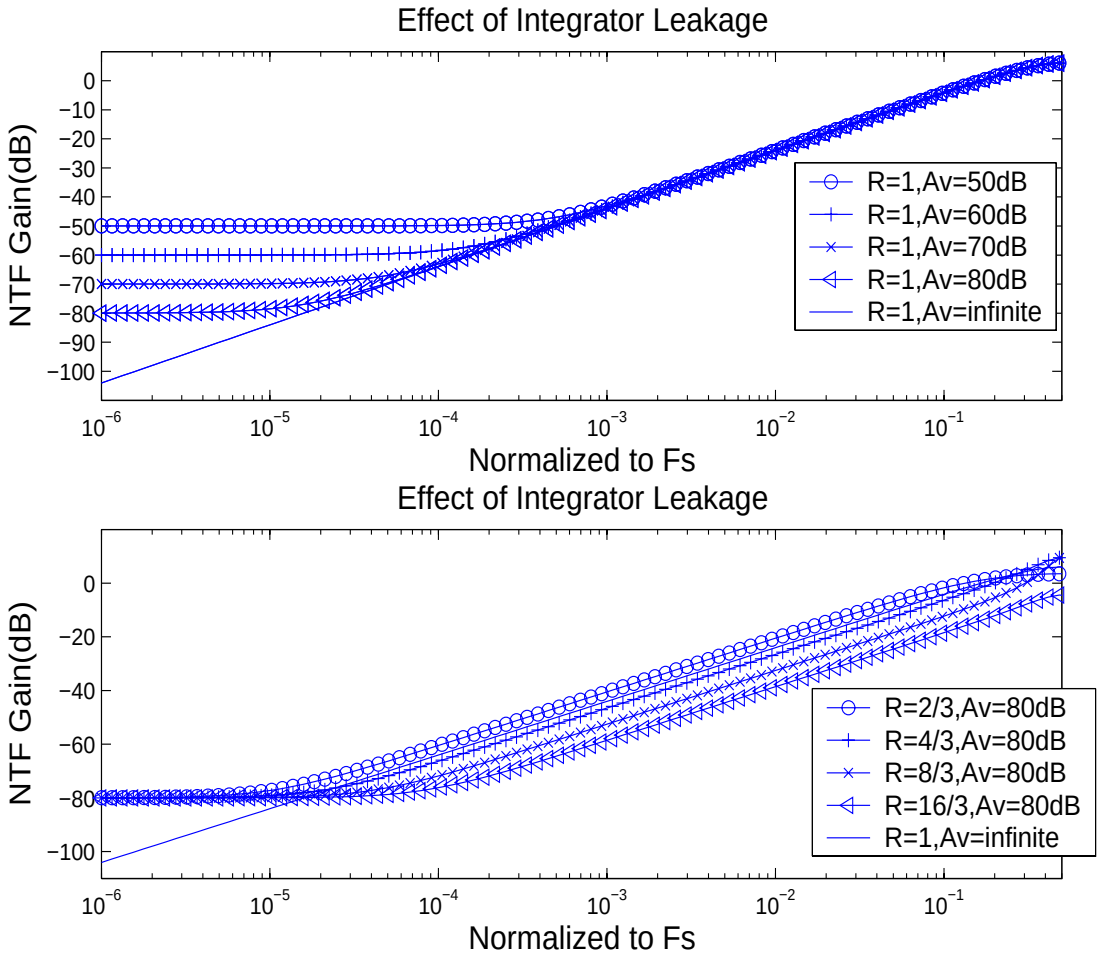

Figure 3.2 Effects of leakage in the SCI

If the order of SDM and OSR are simultaneously invoked into integrator leakage, equation (2.5) can be expressed [21]:

$$P_e^{'} \cong \frac{LSB^2}{12} \times \left\{ \frac{\mu^2 \pi^{2m-2} m}{(2m-1)M^{2m-1}} + \frac{\pi^{2m}}{(2m+1)M^{2m+1}} \right\}$$
$$\mu = R / Av \tag{3.6}$$

This error degrades the SNR and contributes the noise floor in-band. Figure 3.2 indicates us that the higher OPAMP gain and the higher capacitor ratio, the more quantization noise are repressed at low frequency. Nevertheless, the feedback factor has its ceiling to avoid two effects:

(1) Overload of quantizers: Because limited input range of quantizers. Figure 3.3 shows the probability distortion of the integrators outputs, it implies that dynamic range is required more times of full scale input for larger ratio to ensure quantization noise is less than a half of LSB. This requirement restricts the input range of modulators when input range of quantizers is confined.

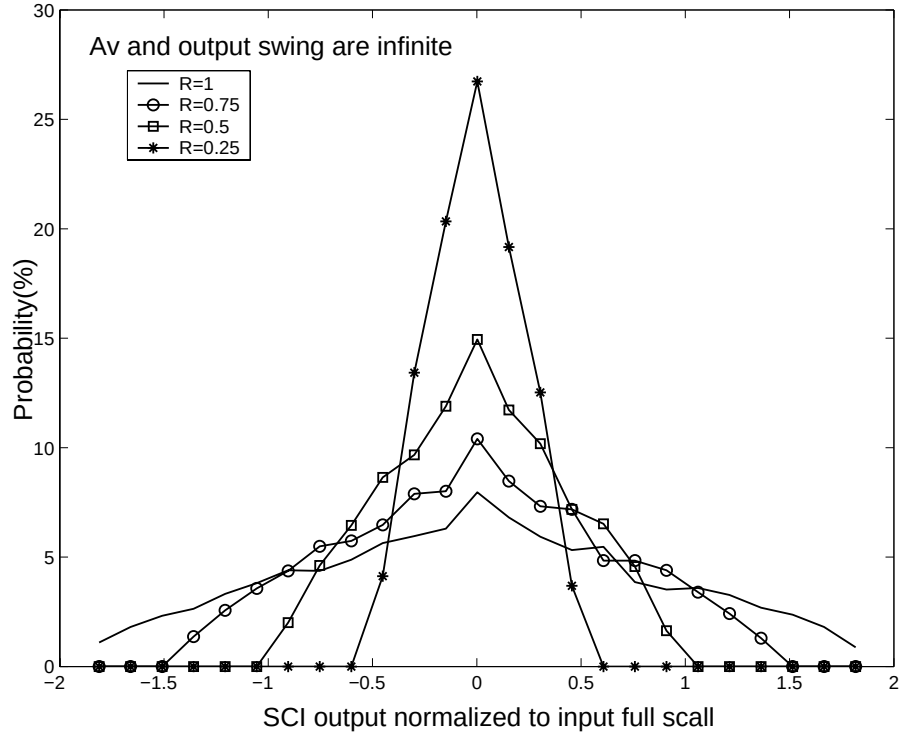

Figure 3.3 Comparison of SCI output probability densities for different feedback factor

(2) SCI distortion: This distortion is caused by the limited output range of OPAMP, as sketched in Figure 3.4, warps SCI output waveform which reflects the sum of input signal and feedback signal and will bring about inaccurate bit-steam produced by quantizers. The higher resolution of quantizers, the worse SNR exists

when SCI distortion happened.

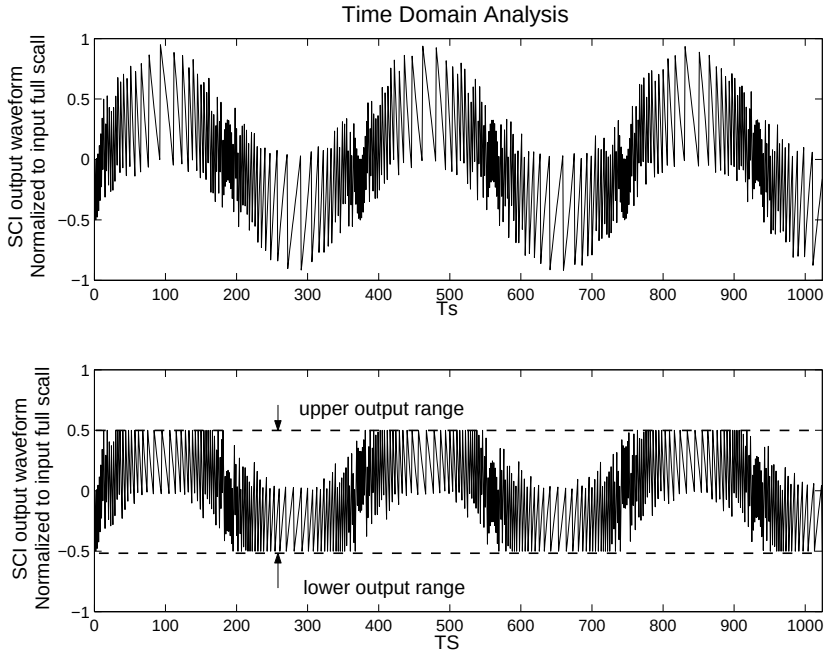

Figure 3.4 Simulated integrator distortions

The Z transform is good to describe SC integrator efficiently, the transform function indicates the stable states as well as low clock rate. Unfortunately, the final sample and setting voltage have deviation between the ideal cases calculated by equation (3.1) due to limited period and RC time constant, this error is called as "incomplete setting noise". A transient model needs to be established for an accurately designed SDM. For simplicity, we assume a single-pole and limited output current model for OPAMP in the SC integrator.

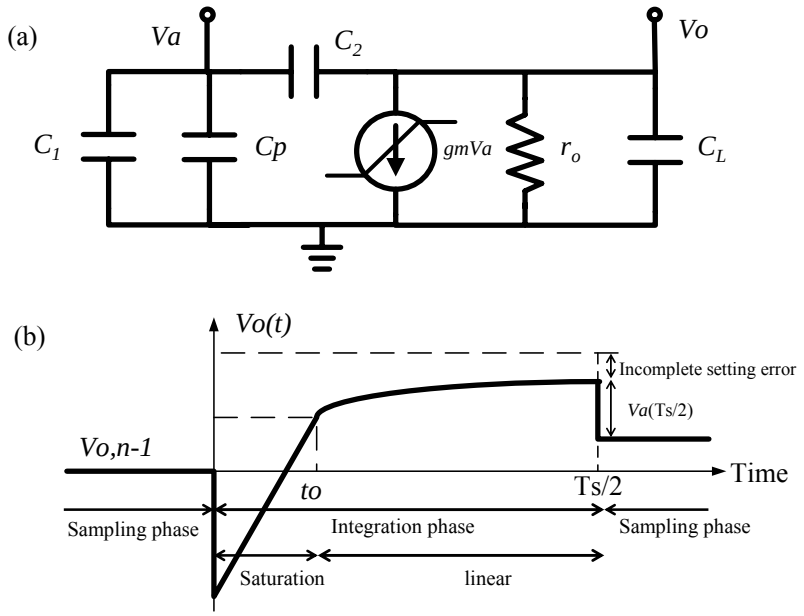

Figure 3.5 (a) Equivalent model for integration mode (b) Time evolution of v_o

An equivalent circuit during the integration phase is shown in Figure 3.5(a). Owing to the fact that C_1 samples the input voltage and a feedback path provided by C_2 and OPAMP, the v_o jump in the opposite direction to the final increase, and a similar evolution occurs in the input node whose v_a experiences a jump in the instant in which switches S1 and S2 are just closed [21]. Depending on the value of v_a, we will distinguish two operational modes, (a) Linear: if $|gmv_a| < Io$, (b) Saturation: if $|gmv_a| > Io$, where Io is the maximum output current of OPAMP. Suppose t=0 at the end of sample phase, and $t=t_o$ at the end of saturation mode, like illustrated in Figure 3.5(b). The output voltage is a function of time and we will discuss it in detail at next page and study the effect of this kind of voltage error by some equations. The initial value of $v_a(t=0)$ and $v_o(t=0)$ can be obtained by charge conservation:

$$v_a(t=0) = v_{ai} = \frac{-C_1}{C_1+Cp+\frac{C_2C_L}{C_2+C_L}} vi \tag{3.7}$$

$$v_o(t=0) = v_{oi} = v_o[(n-1)Ts] + \frac{C_2}{C_2+C_L} v_{ai} \tag{3.8}$$

Capitalize the RC time constant to derive $v_o(t)$, when linear mode:

$$v_o(t) = v_o(t=\infty) + \left[v_{oi} - v_o(t=\infty)\right] e^{\frac{-t}{R_{eq}C_{eq}}} \tag{3.9}$$

$$v_o(t=\infty) = \frac{v[(n-1)Ts] + \frac{C_1}{C_2}vi}{1+\frac{1}{Av}(1+\frac{C_1+Cp}{C_2})}, \quad Av = gmr_o$$

$$R_{eq} = (g_o + gm \times \frac{C_2}{C_1+C_2+Cp})^{-1} \quad \& \quad C_{eq} = C_L + \frac{(C_1+Cp)C_2}{C_1+Cp+C_2}$$

At saturation mode, for g_o is much smaller than one, the $v_a(t)$ is expressed by equation (3.7) and t_o can be calculated when this equation is equal to Io/gm, so:

$$v_a(t) = \frac{-C_1}{C_1+Cp+\frac{C_2C_L}{C_2+C_L}} vi + \frac{Io \times \mathrm{sgn}(vi)}{Ceq} \times \frac{C_2}{C_1+C_p+C_2} t \tag{3.10}$$

$$t_0 = \frac{-C}{gm} + \frac{C_1}{Io}(1+\frac{C_L}{C_2})|vi| \quad \& \quad C = C_1 + Cp + C_L(1+\frac{C_1+Cp}{C_2}) \tag{3.11}$$

For $t > t_o$, the SC integrator is operating at linear mode, we can get:

$$v_o(t) = v_o(t=\infty) + \left[v_o(t=t_o) - v_o(t=\infty)\right] e^{\frac{-(t-t_o)}{R_{eq}C_{eq}}} \tag{3.12}$$

$$vo(t=t_o) = vo[(n-1)Ts] + \frac{-C_1}{C_1+Cp+\frac{C_2C_L}{C_2+C_L}} vi + \frac{Io \times \mathrm{sgn}(vi)}{C_{eq}} \times to$$

$$v_a(t) = \frac{v_o(t=\infty)}{-Av} + \left[v_a(t=to) - \frac{v_o(t=\infty)}{-Av}\right] e^{\frac{-(t-t_o)}{R_{eq}C_{eq}}} \tag{3.13}$$

The time constant in equation (3.12) is the same with equation (3.9). Combing equation (3.9) and (3.12), we can obtain the value in the end of integration phase. Output voltage happen to another drop because v_a tend to analog ground during next sampling phase and the voltage stored in C_2 keeps constant, as shown in Figure 3.5(b). General speaking, C_L (Cp) is much smaller than C_2 (C_1), therefore:

$$\frac{C_1}{C_2} = R \quad \& \quad Av >> 1$$

$$v_{ai} = -vi \ , \ v_{oi} = v_o[(n-1)Ts] - vi \ , \ v_o(t=\infty) = v_o[(n-1)Ts] + R \times vi$$

$$R_{eq} C_{eq} = C_1 / gm = \tau$$

$$t_o = \frac{C_1}{Io} vi - \tau = \frac{C_1 / C_{eq}}{Io / C_{eq}} vi - \tau = \frac{1+R}{SR} vi - \tau$$

When linear mode:

$$v_o(t) = v_o[(n-1)Ts] + R \times vi - (1+R)vi \times e^{\frac{-t}{\tau}} \tag{3.14}$$

When saturation mode:

$$\begin{cases} v_o(t) = v_o[(n-1)Ts] - vi + SR \times t & t \le t_o \\ v_o(t) = v_o[(n-1)Ts] + R \times vi - [(1+R)vi - SR \times t_o] e^{\frac{-(t-t_o)}{\tau}} & t \ge t_o \end{cases} \tag{3.15}$$

Above equations imply that, some error introduced in integrator output can be seen as the error term of SC integrator. This will make up distortion and harmonics at the modulator output, and this error exits a dependency between the leakage of the integrator, slew rate and its input voltage.

Another noise source is thermal noise, which contribute principally to the overall thermal noise power are the non-zero turn-on resistance of switches, both sampling and integration phase, and the input-referred OPAMP. The total power of thermal noises is proposed by [21].

$$Pth \cong \frac{kT}{4MC_1} + \frac{kT}{2M(C_1+Cp)} \left(\frac{1}{3} + gmR_{on}\right) \tag{3.16}$$

Where k is the Boltzman's constant and its value is 1.38×10^{-23}, T is absolute temperature and *Ron* is the turn-on resistance of switches. Note that equation (3.16) should be multiplied by two when referred to fully-differential structures. For time domain simulation, thermal noise can be modeled as a noise source with n(t) denotes a Gaussian random process with unit standard deviation [22], which is:

$$Vth = \sqrt{\frac{kT}{4MC_1} + \frac{kT}{2M(C_1+Cp)} \left(\frac{1}{3} + gmR_{on}\right)} \times n(t) \tag{3.17}$$

Clock jitter refers to the temporal variation of the clock period at a given point on the chip, thus the clock period can reduce or expand on a cycle-by-cycle basis. Jitter is a zero-men random variable [23]. Once the analog signal has been sampled, the SC circuit is a sampled-data system where variations of the clock period have no effect on the circuit performance. This also means that effect of clock jitter on a SDM is independent of the stricture and the order of the modulator. As a result, a non-uniform sampling time sequence produces an error which increases total error at the quantizer output.

$$\frac{x(t+D)-x(t)}{D} \cong \frac{d}{dt}x(t)$$

$$if \ \ x(t)=Ain\times\sin(2\pi\ fin\times t)$$

$$\Rightarrow\frac{d}{dt}x(t)=2\pi\ fin\left[Ain\times\cos(2\pi\ fin\times t)\right]$$

$$\therefore x(t+D)=x(t)+D\times 2\pi\ fin\left[Ain\times\cos(2\pi\ fin\times t)\right]$$

$$=input\ \ signal\ \ +\ error\ \ sorce(V_{jitter})$$

$$\Rightarrow P_{jitter}=\frac{Ain^2}{2}(2\pi\ fin)^2 \tag{3.18}$$

$$\Rightarrow Vjitter=\frac{Ain}{2}2\pi\ fin\times d(t) \tag{3-19}$$

Here, we suppose D is a Gaussian random process with standard deviation d [22].

A behavior model established in MATLAB with a sub-circuit, shown in Figure 3.6 and Figure 3.7, can be used to determine the sensitivity to analog sub-circuits, and the circuit level specifications are decided. The set of blocks takes in account of imperfection previous study.

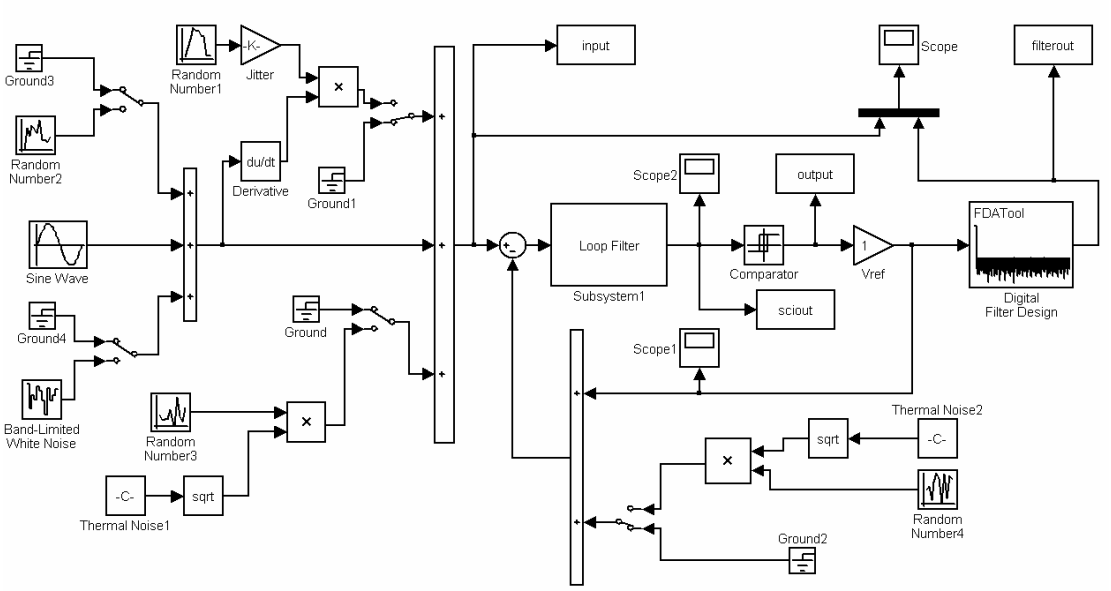

Figure 3.6 A behavior model implemented in MATLAB

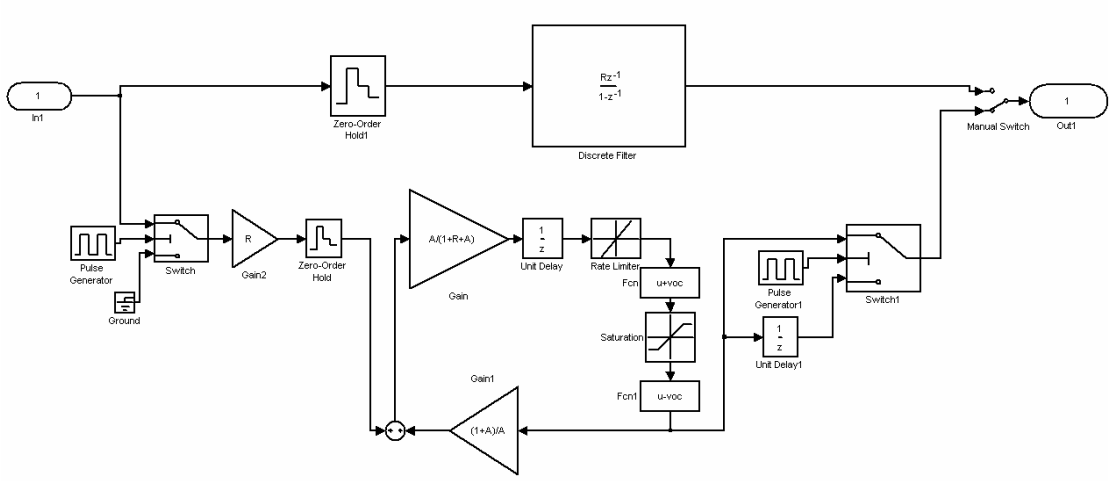

Figure 3.7 The sub-circuit of loop filter

It should be concluded, from what has been said above, the Peak SNR is reduced by:

- OPAMP open loop gain, equation (3.6).
- OPAMP slew rate and BW, equation (3.15).
- Thermal noise of switches and OPAMP, equation (3.16).
- Clock jitter, equation (3.18).
- Others: OPAMP saturation voltages, Capacitors ratio.

3.2 Higher Temperature Issues

Current commercial CMOS technologies can be used without any process modifications to design circuits useful up to 250^{o}C [24]. However, thermal effects on small signal parameters of CMOS are studied necessarily to figure out the design tradeoffs and considerations limitation for analog circuits.

Table 3.1 lists some parameters with level 2 model [25], it is evident that the drain current have strong dependency on temperature, furthermore all of small signal models as transconductance and output resistance, are based on the amount of drain current. We may, therefore, reasonably conclude that the relationship between these parameters and temperature is quite close. Direct deriving correlations, however, bring about complex results and inefficiency on circuit design. Fortunately, some effectives equations proposed in [24] are present along with the temperature dependencies of key design parameters and represent sufficient information for first-order hand analysis prior to CAD design.

Table 3.1 Some parameters of NMOS with level 2 model

Parameter	Equation
Drain current	$I_D=\frac{\mu C_{ox}}{2}\frac{W}{L}\times(V_{GS}-V_T)^2\times(1+\lambda V_{DS})$
Threshold voltage	$V_T=V_{FB}+\phi+K_1(\phi-V_{BS})^{0.5}\leftarrow\phi=\frac{2kT}{q}\ln\frac{N_{sub}}{ni}$
Intrinsic carrier concentration	$ni = 7.785\times10^{15}\times T^{\frac{3}{2}}\times e^{\frac{-Eg}{2kT}}$
Band gap of silicon	$Eg=1.17-\frac{4.73\times10^{-4}}{T+636}T^2$
μ *is effective mobility*, φ *is surface potential*, $K1$ *is substrate effect coefficient*	

The effects of temperature on large signal parameters of the MOSFET are discussed first. Recalling the drain current, wherein threshold voltage and effective mobility are critical points. Whether both of them are analytical quantity, two good approximations can describe the temperature dependency, thus:

$$Vth(T) = \alpha T + \beta \tag{3.20}$$

$$\mu(T) = \mu(T_o)\times(\frac{T}{T_o})^{\gamma} \tag{3.21}$$

Where T is absolute temperature, (α, β, γ) are parameters depend on processing. Then we can estimate the Zero-Temperature-Coefficient (ZTC) bias points for saturation region, at which the drain current exhibits minimum temperature sensitivity, it is possible to write:

$$\frac{\partial I_D}{\partial T} = \frac{\partial I_D}{\partial Vth}\frac{\partial Vth}{\partial T} + \frac{\partial I_D}{\partial \mu}\frac{\partial \mu}{\partial T}$$

$$=\frac{\partial I_D}{\partial Vth}\times\alpha+\frac{\partial I_D}{\partial \mu}\times\frac{\gamma\mu}{T}$$

$$=I_D\times\left(\frac{-2\alpha}{Vgs-Vth}+\frac{\gamma}{T}\right)$$

$$if\ \ \frac{\partial I_D}{\partial T}=0\ \Rightarrow\ Vgs_{sat}=Vth+\frac{2\alpha}{\gamma}T \tag{3.22}$$

Another ZTC bias point over the range $[T_1, T_2]$ is addressed in [24], that is:

$$Vgs_{sat} = \beta - \frac{(T_1+T_2)}{6}\alpha \tag{3.23}$$

In 0.25 μm CMOS technology, (α, β, γ) = (-0.9m, 800m, -1.5) and (+0.88m, -1124m, -1.5) for NMOS and PMOS respectively. Using equation (3.20), (3.22) and (3.23), the ZTC bias point for a NMOS during temperature [300k, 500k] is about 920mv. If we use HSPICE to fide out this ZTC bias point, shown in Figure 3.8, its value is 897mv.

A similar result is exhibits in triode region can be expressed as:

$$Vgs_{triode} = \beta + \frac{(T_1+T_2)}{6}\alpha \tag{3.24}$$

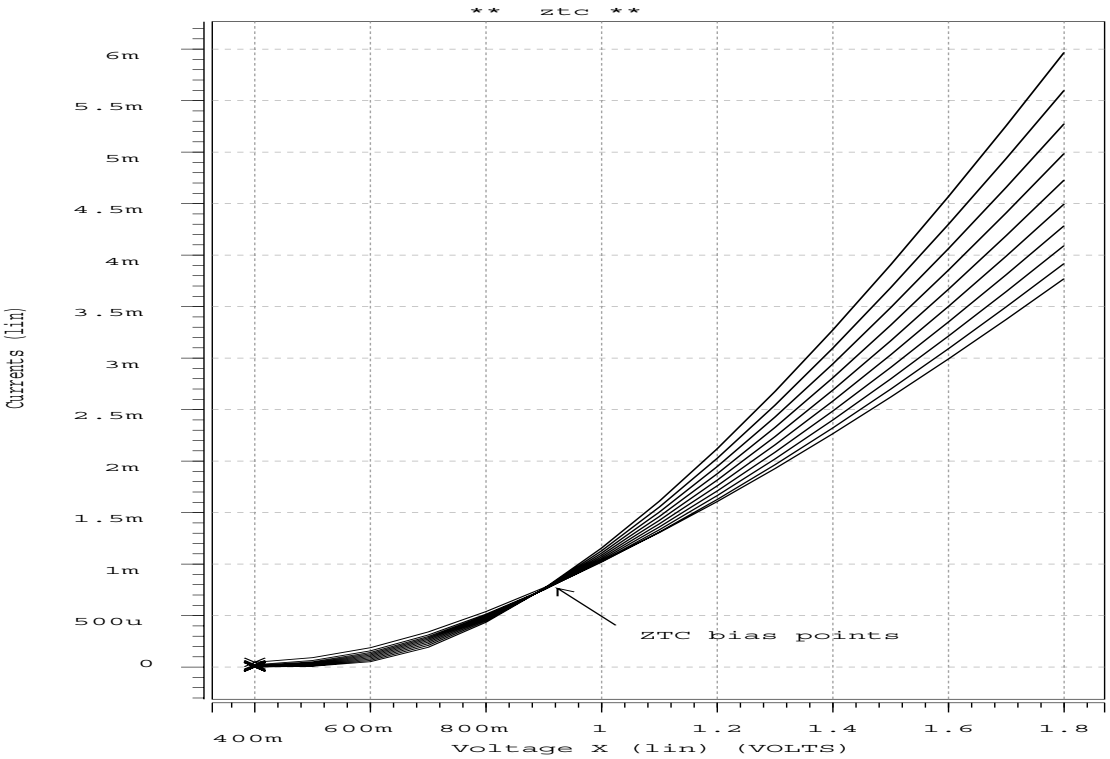

Figure 3.8 ZTC bias points for NMOS (14 μ m/0.7 μ m) in 0.25 μ m process

By the way, retuning to equations (3.20) and (3.21), the threshold voltage decreases with down scaling, the mobility have no effect with down scaling, and the ration of n to p inversion layer mobility $\mu_n(T)/\mu_p(T)$ remains approximately constant between 25°C and 250°C [26].

Let us consider small signal models right now. Most important two parameters are transconductance and output resistance, which determine the gain and bandwidth of many circuits. It is easy to write that:

$$gm = \frac{2I_D(T)}{Vgs-Vth(T)}$$

$$\frac{\partial gm}{\partial T} = \frac{gm}{2}\left(\frac{\gamma}{T} + \frac{\partial I_D}{\partial T}\times\frac{1}{I_D}\right) \tag{3.25}$$

$$rds = \frac{1}{\lambda I_D}$$

$$\frac{\partial r_{ds}}{\partial T} = \frac{\partial I_D}{\partial T}\times\frac{-r_{ds}}{I_D} \tag{3.26}$$

Previous equations imply that the minimum variation of transconductance and output resistance occur at ZTC bias point. So, in order to maintain the same characteristic during temperature rise, bias at ZTC is the best choice, below are simulation results:

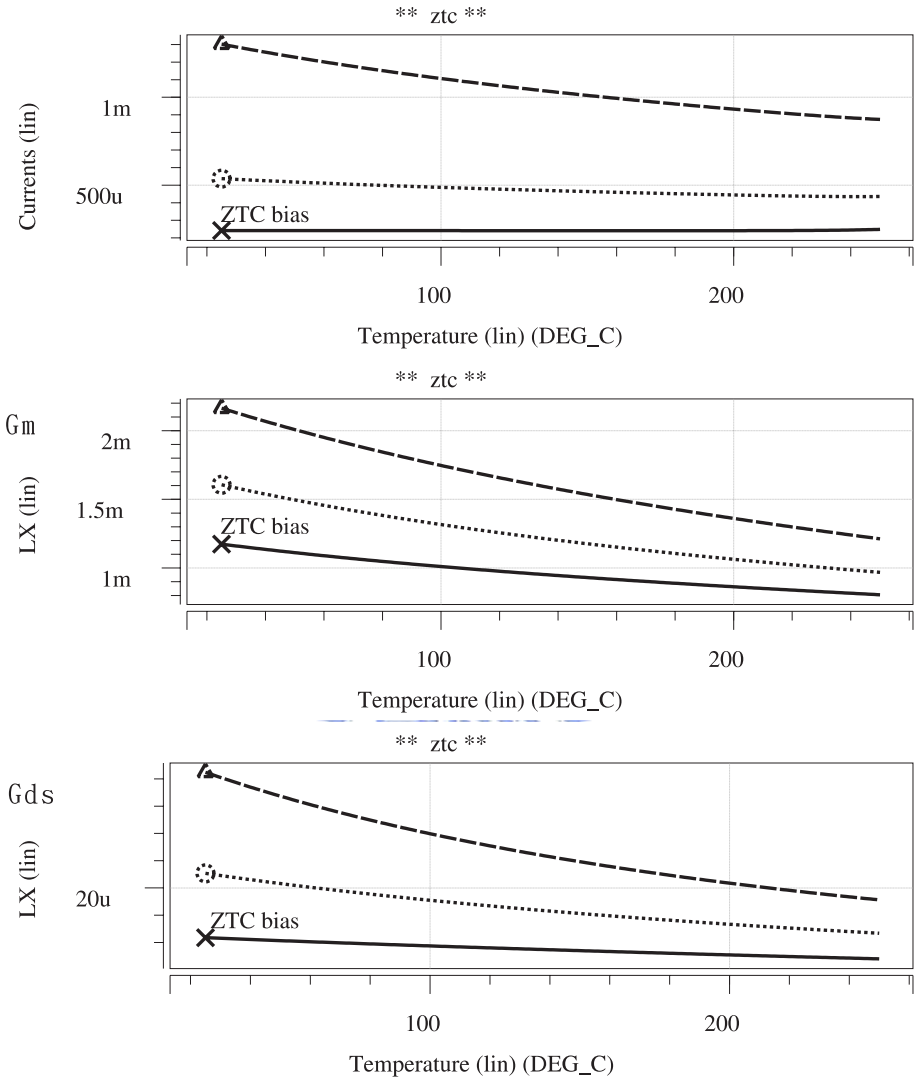

Figure 3.9 Id, gm, gds characteristics for ZTC, ZTC+0.2v, ZTC+0.6v

If the temperature is higher than 250^{o}C, sharp increases in the output conductance and body effect transconductance have consistently been observed [27], it has been determined that diffusion leakage current. The various leakage currents comprise the following:

1. The drain and source to body junctions' bottom wall component, Ib(T), which is proportion to W and D, shown in Figure 3.10.
2. The drain and source to body junctions' sidewall wall component, Isw(T), which is proportion to W and X, shown in Figure 3.10.
3. The inversion layer to body junctions component, Ich(T), which is proportion to the W and L, shown in Figure 3.10.

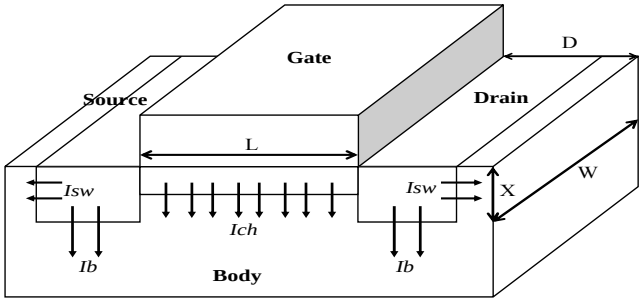

Figure 3.10 Leakage current components

Leakage current, in particular, can be a significant source of impairment and is worthy of a more detail review. The ideal P-N diode current is described by:

$$I_{Diode} = Aqn_i^2 K_D (e^{\frac{qVF}{kT}} - 1)$$

A is the area of leaky diodes. If this diode is operated under strong reverse, it can be reduced as:

$$I_{Diode} = -Aqn_i^2 K_D$$

In addition to this, there is reverse bias current due to generation-recombination events within the depleted region, which is:

$$I_{GR} = -Aqn_i K_{GR}$$

So, the total leakage current in the reverse bias as shown [12]:

$$I_L = -Aqn_i^2 K_D - Aqn_i K_{GR} \tag{3.27}$$

Figure 3.11 indicates that, the leaky diodes are sinks and sours at the drain or source node of NMOS and PMOS respectively. Although, we can use equation (3.27) to calculate leakage current, but the exactly amount is difficult to predict and hard to avoid. Design a compensation circuit is more effective to restrain thermal problems.

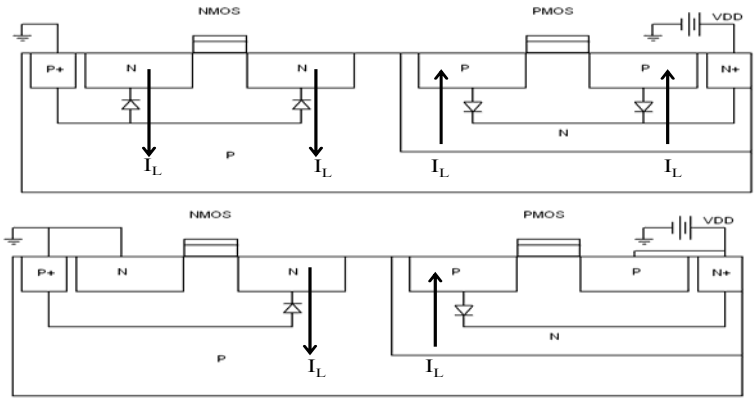

Figure 3.11 The leaky junction diodes are explicitly shown in CMOS

The principle of compensation circuits is algebraic sum of all leakage current be zero at any given node. If one was not this case, net leakage current would flow into or out of this node, thus forcing an increase or decrease in drain current of adjacent transistors, which result in voltage shift from bias points and performance degrade. To this point, adding diodes or complementary structure are approaches to reduce leakage current, as sketches below.

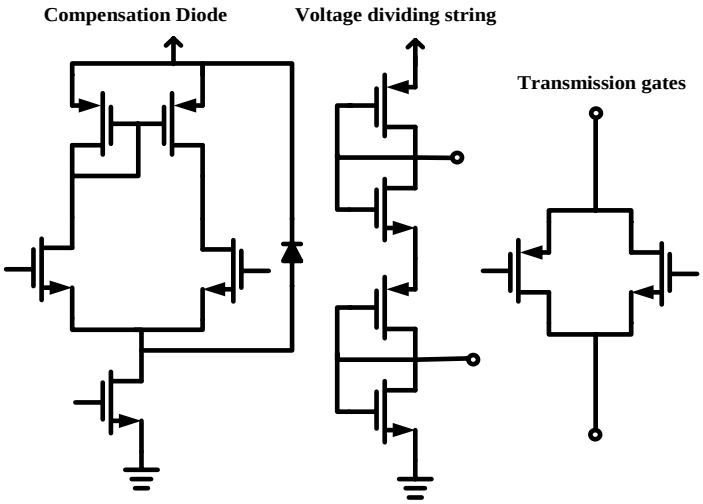

Figure 3.12 Compensation circuits for leakage current

We should note that transmission gates, show in Figure 3.12, this structure is popular in the switches-capacitor system to be a switch. The leakage current is not matched all the time and keeps almost constant for any given node, thereby charging or discharging loading capacitors, so that setting or holding error as a result. Increasing clock rate, which can decrease the charging or discharging time, is one way to solve this problem.

From previous study, we can make a conclusion below to minimize leakage current in high temperature environment:

- Small diffusion area
- Low leakage switches
- Compensation devices, like diodes
- Matching leakage area
- Bias at ZTC points
- External capacitors to increase the time constant
- High clock rate

Chapter4

Implementation of Proposed Sigma Delta Modulator

A prototype of proposed sigma delta modulation has been fabricated in TSMC 0.25 μm single-ploy five-metal CMOS process. The circuitry is operating at a supply voltage of 3.3 volt. The design issues for this prototype in circuitry, transistors and physical levels are thoroughly discussed in this chapter. The whole circuitry blocks are described in Section 4.1. In Section 4.2 the sub-circuitry of each component is presented, which includes OPAMP, comparator, switch capacitors, integrator, feedback DAC, and output buffers. In Section 4.3, the final physical design of proposed SDM prototype is then described.

4.1 Circuit Level Design

The detail schematic design and system considerations have been present in earlier this thesis. Implementation of these principles to an actually monolithic chip is our objective here. Let us recall all of building blocks of SDM, they are a loop filter, a quantizer, the feedback path and an adder. We should notice that a loop filter and an adder can be carried out by a differential SC integrator, and another advantage of this is a sample and hold circuit call be omitted. In addition to this, a one-bit ADC is used be to be a quantizer for SDM. Therefore the SDM can be divided into three parts, which consist of sub-circuits, and we can summarize them in Table 4.1 below.

Table 4.1 Organization of SDM

Schematic	Building Block	Sub-circuit	Section
Adder	Differentia	OPAMP	4.2.1
Loop Filter	SC Integrator	Switches & Capacitors	4.2.3
Quantizer	1 bit ADC	Comparator	4..2.2
Feedback Path	1 bit DAC	Feedback DAC	4.2.5
		Output buffer	4.2.6

A fully experimental SDM circuit is shown in Figure 4.1 at next page, input and output signal are illustrated simultaneously. The key point I wish to emphasize is that, output buffers are required due to parasitic package capacitors.

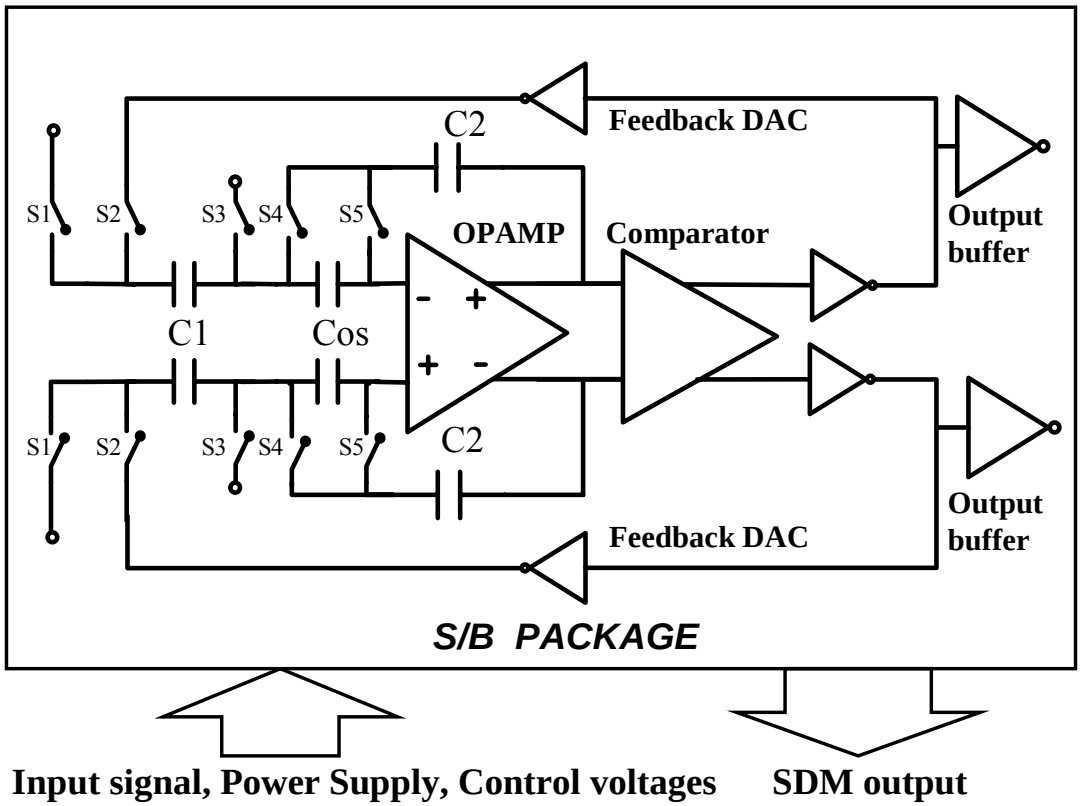

Figure 4.1 Circuit level of SDM

Two topologies, switched-capacitor (SC) and correlated double sampling (CDS), are invoked, so there are ten switches and six capacitors are employed. We list device ration of switches and capacitors sizes in Table 4.2 first, the detail design considerations of them will be discussed at section 4.2.3 and 4.2.4 later.

Table 4.2 Switches and comparators information

Component	Size	Type	During
S1	20 μ m/0.36 μ m	NMOS	Φ1d
S1	20 μ m/0.36 μ m	PMOS	Φ2d
S2	4 μ m/0.36 μ m	NMOS	Φ2d
S3	4 μ m/0.36 μ m	NMOS	Φ1
S4	20 μ m/0.36 μ m	NMOS	Φ2
S5	20 μ m/0.36 μ m	NMOS	Φ1
C1	0.4pF	MIM	Always
C2	0.5pF	MIM	Always
Cos	0.5pF	MIM	Always

Above table also lists operational period of switches in order to (a) sample input and add feedback signal (b) use CDS technology (c) avoid charge injection. In other words, Figure 4.1 is controlled by two phase, non-overlapping clocks, $\Phi 1$ and $\Phi 2$, a delayed clock phase $\Phi 1d$ and $\Phi 2d$. A timing diagram illustrating these clock signals are shown in Figure 4.2.In practice, these clocks are generated by external circuit and will be described in Chapter 5. By the way, all of circuit level design and transistors level design are using the CAD simulation tool, HSPICE.

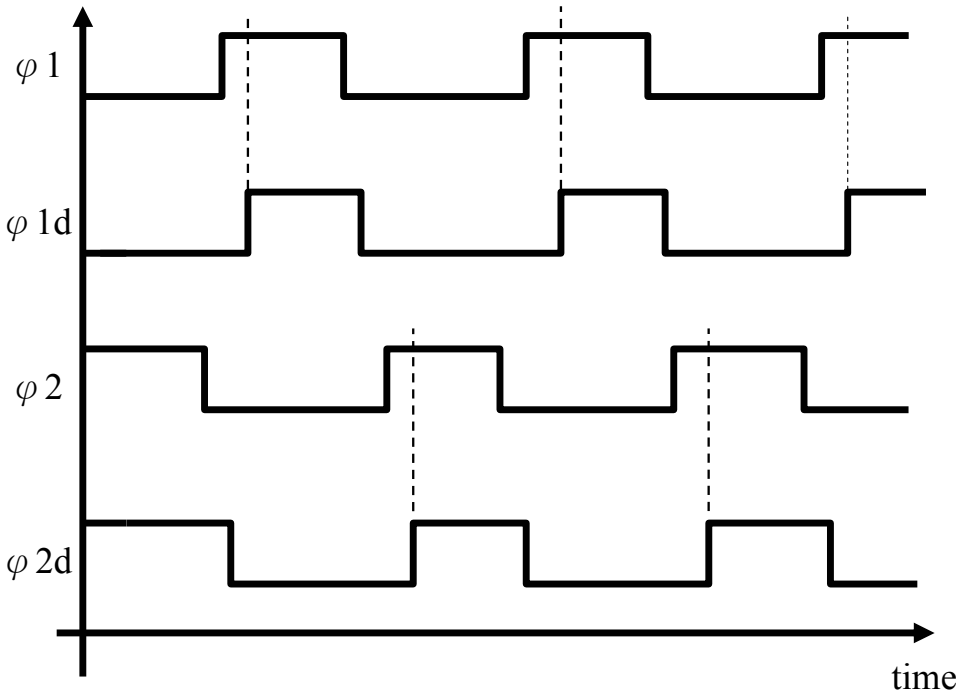

Figure 4.2 A timing diagram illustrating clock signals

4.2 Transistors Level Design

This section described the elaboration of sub-circuits that will be used to realize an actual integrated circuit, which covers an operational amplifier (OPAMP), a comparator, switches and capacitors, and feedback path. The simulation results and device ratios are given at each section.

4.2.1 Differential OPAMP

Utilizing switched-capacitor technology and an operational amplifier (OPAMP) to realize a loop filter in a SDM is a common circuitry for high speed and low power

applications. It is clearly that, however, the performance of this loop filter dominates dynamic specifications of a SDM. Designing a high performance OPAMP is the main purpose in this section. In addition to a main circuit, a bias circuit and a common mode feedback circuit (CMFB) will be discussed.

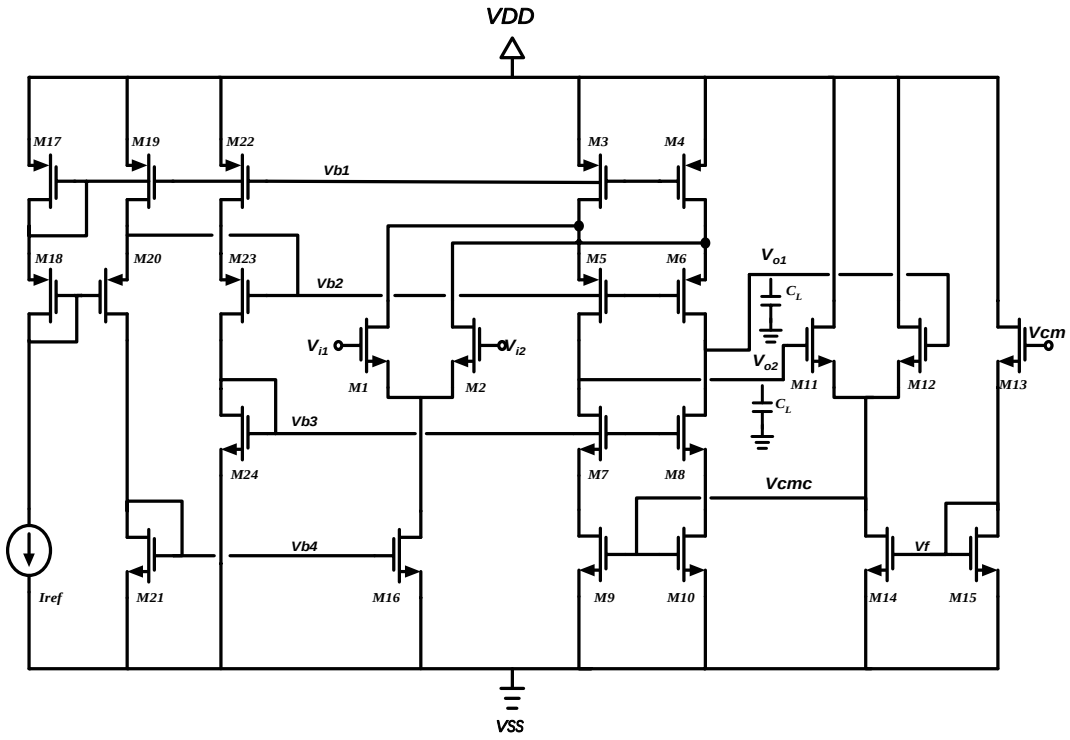

Figure 4.3 Fully differential OPAMP

Figure 4.3 shows the fully differential OPAMP including its bias circuit and CMFB. The OPAMP, which is a folded cascade amplifier, was chosen for its large dc gain and ability to drive capacitive loads [12]. The bias circuit supplies several internal bias voltages except Vcm. The CMFB determine the output common mode voltage and control it to be a specified voltage [15].

The OPAMP circuit consists of eleven transistors, from M1 to M10 and M16. The first stage including M1, M2, and M16; the remainders are second stage. It must be noted that the drain current of M16 determines the slew rate of this amplifier. Added to this, the drain current of M3 (or M4) should be more than M16 to avoid operating failed during slewing. By Naming the drain current of M3 and M16 is "*Iss*" and "*Ir*" respectively, the drain currents of M7 to M10, which are active loads, can be represented as *Ir* minus *Iss*. This shows that the device ratios of active loads don't affect the quantity of current, but affect the voltage gain sufficiently. Briefly speaking, high output resistance is the critical issue to design these four transistors. And then

higher output resistance, higher DC gain. From above discussions, we obtain the following results:

$$\text{If } \left(\frac{W}{L}\right)_i = S_i$$

$$\text{If } V_{gs} - V_{th} = V_{ov}$$

$$S_{16} = \frac{2 \times Iss}{\mu nCoxVov^2} \tag{4.1}$$

$$S_{3,4,5,6} = \frac{2 \times Ir}{\mu nCoxVov^2} \tag{4.2}$$

$$S_{7,8,9,10} = \frac{2 \times (Ir - 0.5\,Iss)}{\mu nCoxVov^2} \tag{4.3}$$

The device ratio of M1 and M2 are another critical issue for high DC gain. By the way, the unit-gain frequency (Fu) is also dependent on their sizes. It can be found that:

$$Fu \cong \frac{gm_{1,2}}{2\pi \times CL} \Rightarrow gm_{1,2} = 2\pi FuCL$$

$$S_{1,2} = \frac{gm_{1,2}^2}{\mu nCoxIss} \tag{4.4}$$

The overall gain of this amplifier can be derived from Figure 4.4, and the detail procedure is given:

$$R = r_{o7} + (1 + gm_7 r_{o7}) r_{o9} \cong gm_7 r_{o7} r_{o9}$$

$$RB = \frac{r_{o5}}{1 + gm_5 r_{o5}}$$

$$RA = r_{o3} // r_{o1}$$

$$i1 = \frac{gm_1}{2} \times Vid$$

$$i = i1 \times \frac{RA}{RA + RB}$$

$$\frac{-Vo}{2} = -i \times R_{out}$$

$$R_{out} = R // gm_5 r_{o5} RA$$

$$\therefore Gain = \frac{gm_1 (gm_7 r_{o7} r_{o9} // gm_5 r_{o5} RA)}{1 + (g_{o1} + g_{o3})\left(\frac{r_{o5}}{1 + gm_5 r_{o5}}\right)} \tag{4.5}$$

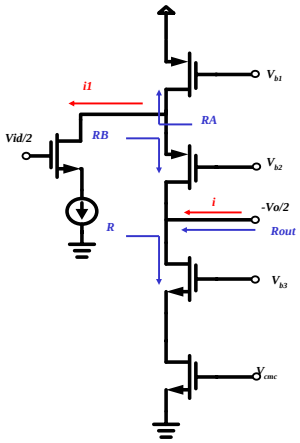

Figure 4.4 Small signal equivalent circuit of OPAMP

The bias circuit contains eight transistors, from M17 to M24. Its outputs are four independent voltage sources to drive OPAMP operating at active mode. Strictly speaking, M22 and M3 is a current mirror pair. Compared with the drain current of M3, the quantity of Vb1 is not the key point in design. In other words, the amount of current and minimum output voltage should be considered prior to Vb1 when design the size of M22 in order to ensure it could be a current mirror source. A similar result could be found in M21.On the other hand, using two skills for higher output swing [28]. First is minimizing the size of M18, second is connecting the gates of M23 and the source of M20. Figure 4.5 shows the results diagrammatically.

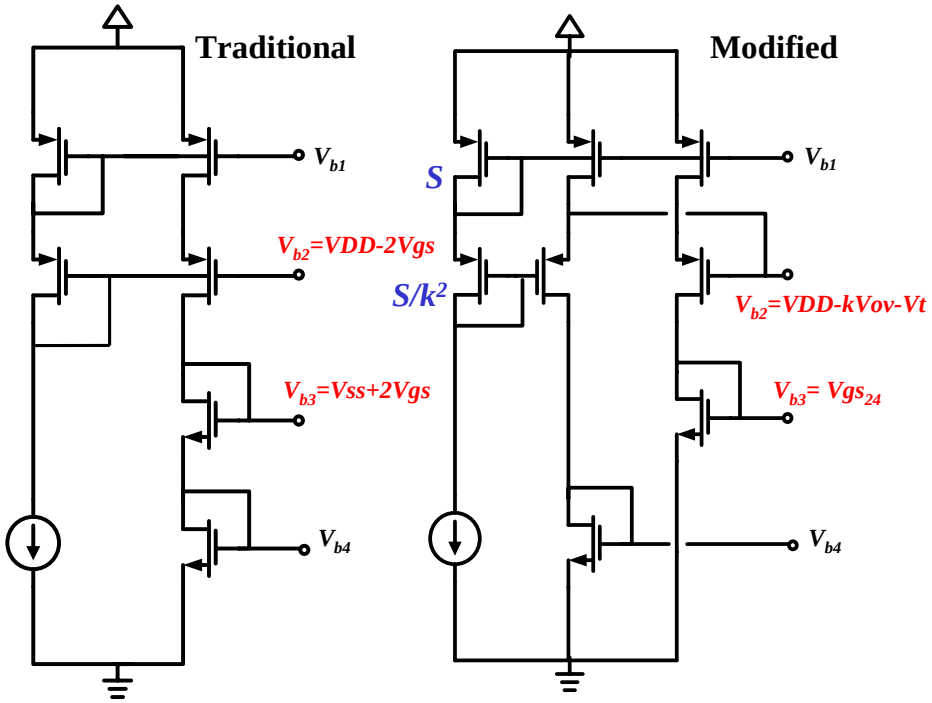

Figure 4.5 Two types of the bias circuit

Thus if VDD is 3.3V, Vov is 0.2V, and k is 3, the Vb1, Vb2, Vb3, and Vb4 is 2.4V, 2.0V, 1.0V, and 0.8V respectively. Equations for these device rations can easily be written as:

$$S_{17,19,20,22,23} = \frac{2\times Iref}{\mu pCoxVov^2} = k^2 S_{18} \tag{4.6}$$

$$S_{21} = \frac{2\times Iref}{\mu nCoxVov^2} \tag{4.7}$$

$$S_{22} = \frac{2\times Iref}{\mu nCox(Vb3-Vt)^2} \tag{4.8}$$

From M11 to M15, there are five transistors comprise the CMFB. In order to simplify the description of operating, we recall that Voc= (Vo1+Vo2)/2, Vg_{15}= Vf, Vg_{13}=Vcm, and Vg_{10}=Vcmc, as illustrated in Figure 4.3.If Voc raises (drops) slightly greater (less) than specified quantity, the drain currents flow through M11 and M12 will raise (drop) at the same time and then Vcmc will increase. After that Voc will drop (raise) cause of output resistance. This implies that there is a negative feedback loop to "latch" Voc at an immobile position if Vcmc is fixed. Figure 4.6 seeks to capture the fact.

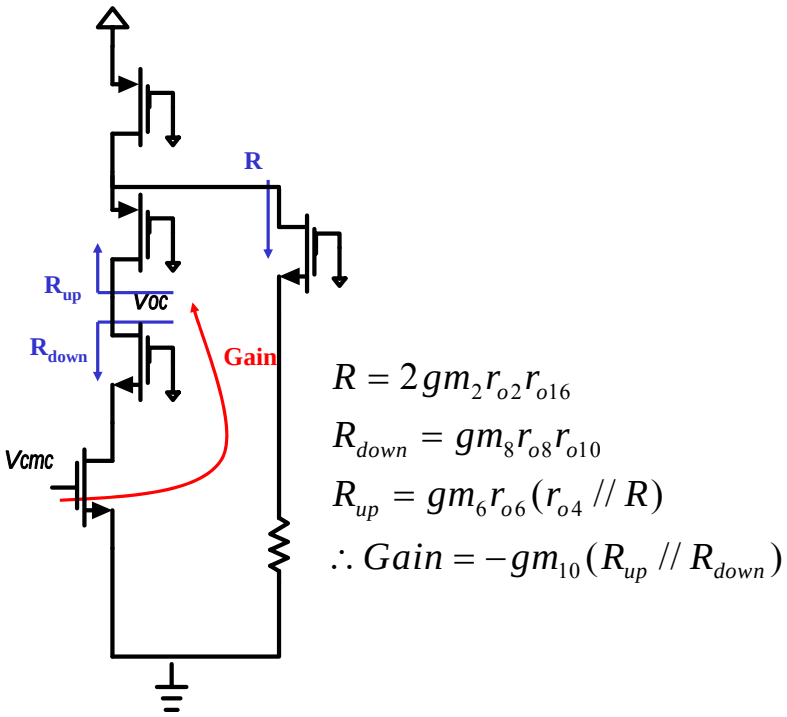

Figure 4.6 Latch Voc by negative feedback

On the other hands, the source follower, which is made up of M13 and M15, senses the Vcm and adjusts Vf to drive Vcmc at a designated voltage. Precisely speaking, Vcmc is a shift form Vcm and output voltage characteristics are controlled

by it, such as common mode (4.9), maximum (4.10).

$$V_{oc} = V_{cmc} + \sqrt{\frac{S_{14}}{2 \times S_{11}}} \times (V_{g15} - V_{th}) \tag{4.9}$$

$$V_{o\_peak} = V_{cmc} + \sqrt{\frac{S_{14}}{S_{11}}} \times (V_{g15} - V_{th}) \tag{4.10}$$

The relationship between Vcm and Voc can be proved by CAD simulation. The results can be schematized as follows:

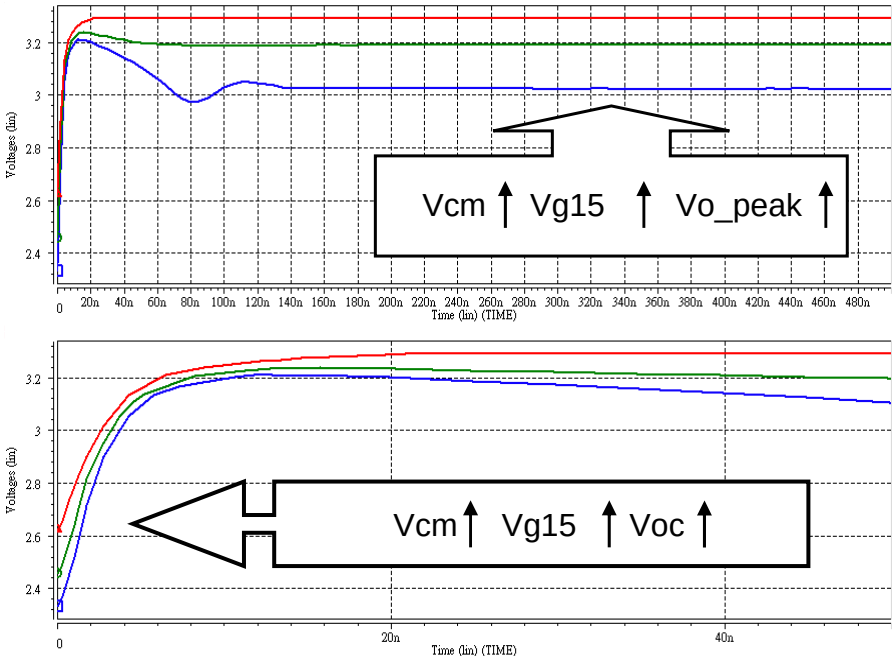

Figure 4.7 Relationship between Vcm and Voc

Capitalizing the foregoing equations, the aspect ratio of this OPAMP can be estimated except CMFB. These constrain represent sufficient information for first-order hand analysis before CAD simulation, however, the results of CAD simulation exhibits a large difference form desired specifications. This is because of the model for CAD is more complex than level 2 model used hand analysis. In order to solve this problem, several methods are proposed here:

(1)Tune the value of S3 and S4 until the drain current is equal to Ir.
(2)Tune the value of S16 until the drain current is equal to Iss.
(3)Tune the value of S7~S10 to improve DC gain.
(4)Tune the value of S1 and S2 to improve DC gain and Fu.
(5)Tune the value of S11~S15 to meet output characteristics.
(6)Using multiple fingers instead of inadequately wide device

Finally, the transistors sizes and the simulated results, when ambient temperature is 25°C, C_L is 1.4 pF, are summarized in Table 4.3 and Table 4.4, respectively. The frequency response of this fully differential OPAMP is revealed in Figure 4.8.

Table 4.3 OPAMP device ratios summary

Transistors	**Ratio**	**Transistors**	**Ratio**
$M_{1,2,7,8,9,10}$	40	$M_{13,16}$	25
$M_{3,4,5,6}$	128.57	$M_{11,12,18}$	5
$M_{14,15}$	15.71	$M_{17,19,20,22,23}$	20
M_{24}	1	M_{21}	2.86

Table 4.4 OPAMP simulated specifications summary

DC Gain	74.867dB	Fu	152MHz
PSRR+	98dB	Phase Margin	53.78°
PSRR-	109dB	Slew rate	158V/us
CMRR	96dB	ICMR	2.1V
Output swing	2.17V	Power	2.53mW

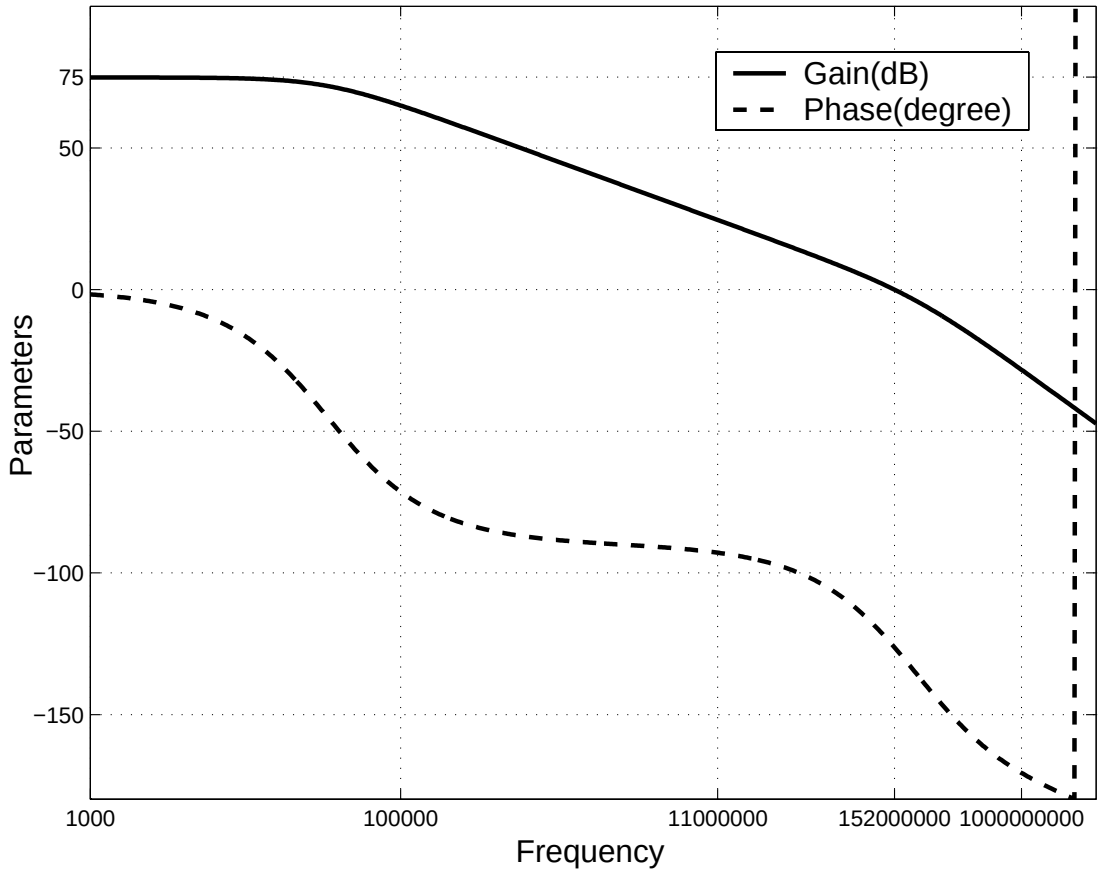

Figure 4.8 Frequency response of this fully differential OPAMP

4.2.2 Comparator

Generally speaking, the comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on comparison. Binary signal means one of two given point exhibits anytime, but this concept is too ideal fore real world situation, where there is a transition region between the two binary states [20]. Therefore, the cores of designing a comparator are speed, dynamic rang, accuracy, and so on.

From the circuitry point of view, comparators can be divided into open-loop and regenerative comparators. The open-loop comparators are based on OPAMP and the regenerative comparators are based on positive feedback. From operation point of view, they can be classified into continuous-time and discrete-time comparators. The continuous-time means comparators generate digital level outputs all the time and the discrete-time means comparators only functions over a portion of a time period [20].In this thesis, we decide to adopt the discrete time comparators founded on regenerative structure for high speed and low power dissipation.

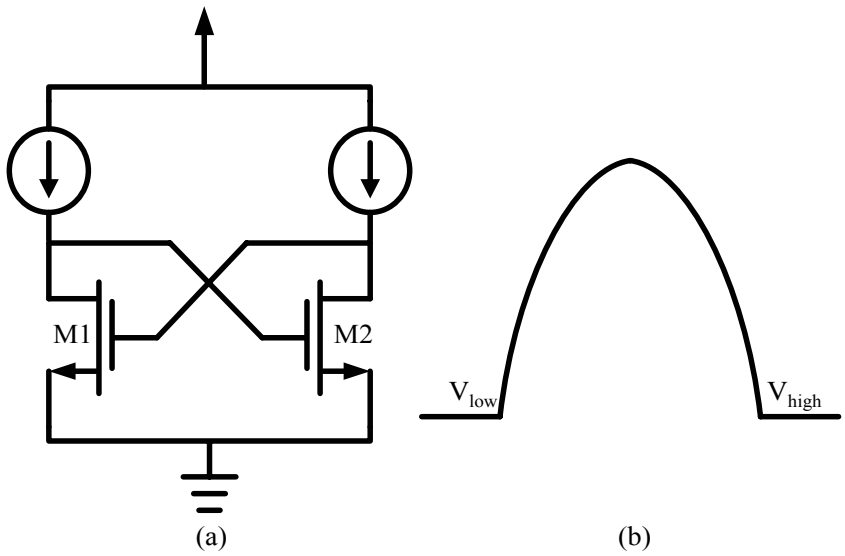

Figure 4.9 (a) A NMOS latch (b) An analogy

Before tuning to realize a whole comparator, the principle of regenerative comparators must be clarified. A simple model is shown in Figure 4.9(a) and it is also called a NMOS latch. If their drain voltage is different from each other, one of them will be push up to a high position (VDD) and the other will be pull down to a low position (ground), Figure 4.9(b) is an analogy. In other words, the latch output binary signal caused by practically dissimilar drain voltage or unavoidable noise.

We can analyze a latch more detail by plotting I-V curves illustrated in Figure 4.10. Suppose the drain voltage of M1 raises a little voltage, vds, and approaches to Vgs+vds, the gate voltage of M2 immediately raises to this identical level. The drain voltage of M2 drops vds' on account of fixed current as shown in Figure 4.10(a), this lead to the gate voltage of M1 drops to Vgs-vds' at the same time. Then the drain voltage of M1 raises vds'' because of fixed current as shown in Figure 4.10(b). Obviously vds'' is bigger than vds, and this implies that there is a positive feedback loop. The result of this effect is binary outputs we read on the front page.

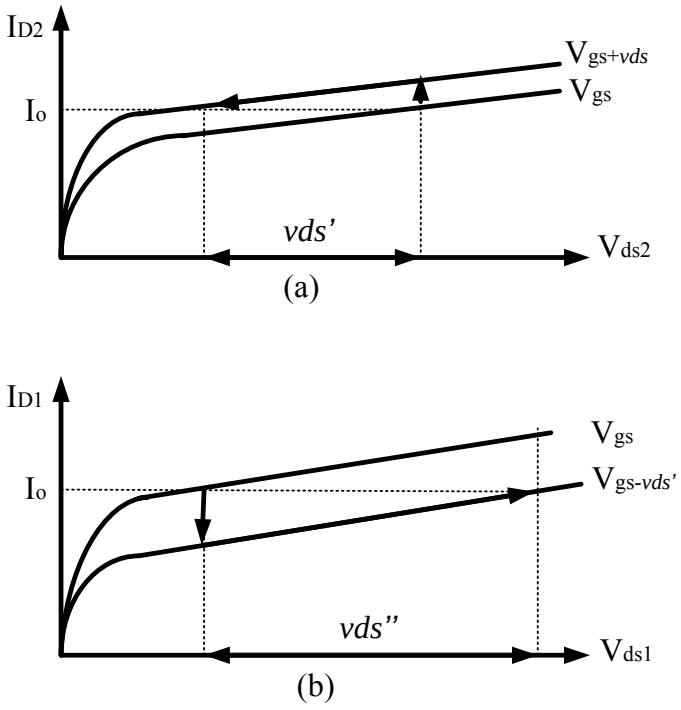

Figure 4.10 DC analysis of a NMOS latch

The first important parameter of a latch is its equivalent output resistance. If adding a testing voltage, like Figure 4.11(a), the output resistance can be derived below. The second is the time it takes for a latch goes from its initial value to the final value [20] developed the equations (4.12) by Figure 4.11(b).

$$Ix = gdsVo1 + gmVo2$$

$$-Ix = gdsVo2 + gmVo1$$

$$\Rightarrow 2Ix = (Vo1 - Vo2)(gds - gm)$$

$$\therefore ro = \frac{Vo1 - Vo2}{Ix} = \frac{2}{gds - gm} \cong \frac{-2}{gm} \tag{4.11}$$

$$\Delta Vo \approx e^{\frac{gm}{C}t} \Delta Vi$$

$$\therefore \tau = \frac{C}{gm} \tag{4.12}$$

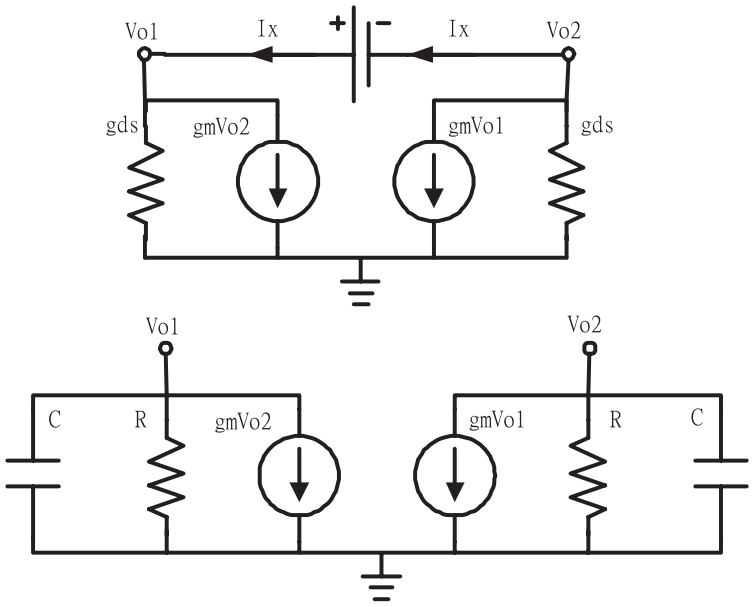

Figure 4.11 Equivalent models for (a) output resistance (b) time constant

Let us now return to realization of an entire comparator. Figure 4.12 is a discrete-time comparator bases on regenerative structure which is used a clock input to alter its operation modes. Assume clock is high, M7~M10 becomes two pair of active loads for M5 and M6, this make input signal can be amplified and called "preamplifier" or "track mode". Assume clock is low, one active load becomes invalid and the latch built up by M7 and M8 push or pull the output signal, this is called "latch mode".

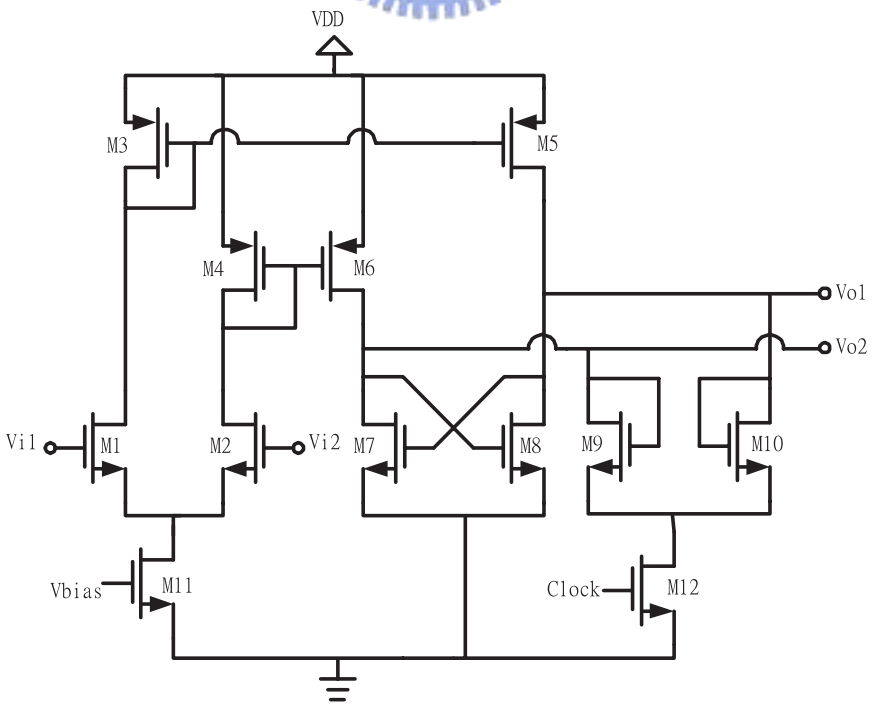

Figure 4.12 A regenerative comparator

The gain of this preamplifier can be confirmed by equation (4.11), and the result is equation (4.13). We should notice that the denominator have to be positive to ensure correct output polarity, in addition to this, the denominator must as small as possible to amplify input signal tremendously. In order to, precisely speaking, remove outputs from the highest or lowest state to the common mode voltage and track inputs, gm9 a little more than gm6 is the best choice.

$$\frac{\Delta Vo}{\Delta Vi}=\frac{gm1}{gm9-gm7}\times\frac{S_6}{S_4} \tag{4.13}$$

The dc analysis of this preamplifier is shown in Figure 4.13, it reveals the gain is approximately fifteen decibel and output range is 1.5 volt. Although performance of this preamplifier is worse than an amplifier like an OPAMP, but it is enough to trigger the latch and compare input signal by quite low power. Table 4.5 summarizes device rations of the entire comparator.

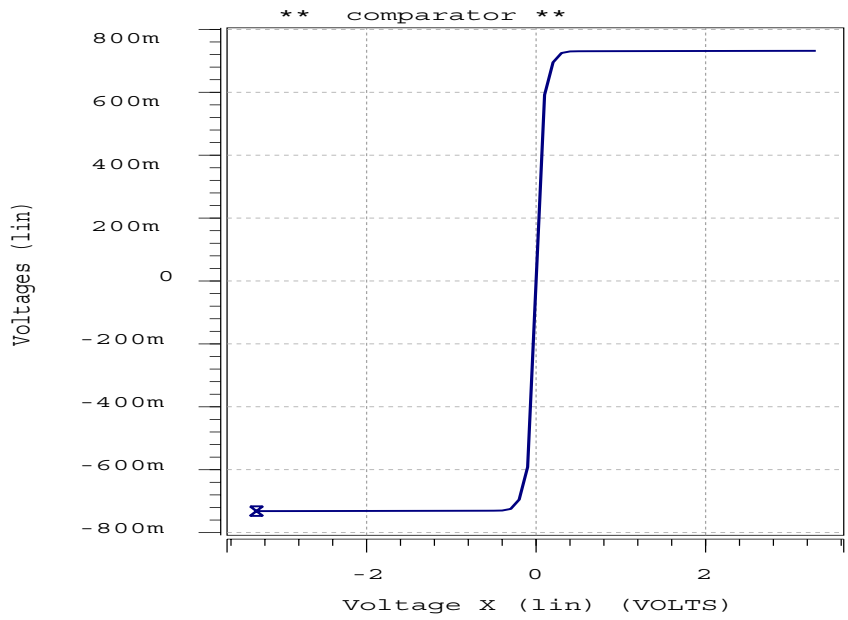

Figure 4.13 DC analysis of the preamplifier

Table 4.5 Comparator device ratios summary

Transistors	Ratio	Transistors	Ratio
M1,2	5	M3,4	18
M5,6	18	M7,8	5
M9,10	10	M11	20
M12	20	Power dissipation is 238 μW	

The outcomes of the transient analysis are illustrated in Figure 4.14.From high to low, the input frequency is 0.2MHz, 2.5MHz, and 5MHz respectively; the clock rate is 2MHz, 25MHz, and 50MHz respectively. It is evident that higher input has longer settling time. Finally, another thing we need to note is that, a comparator can be considered as a one bit ADC, so the inputs must lower than half of clock rate to meet the Nyquist rate theory.

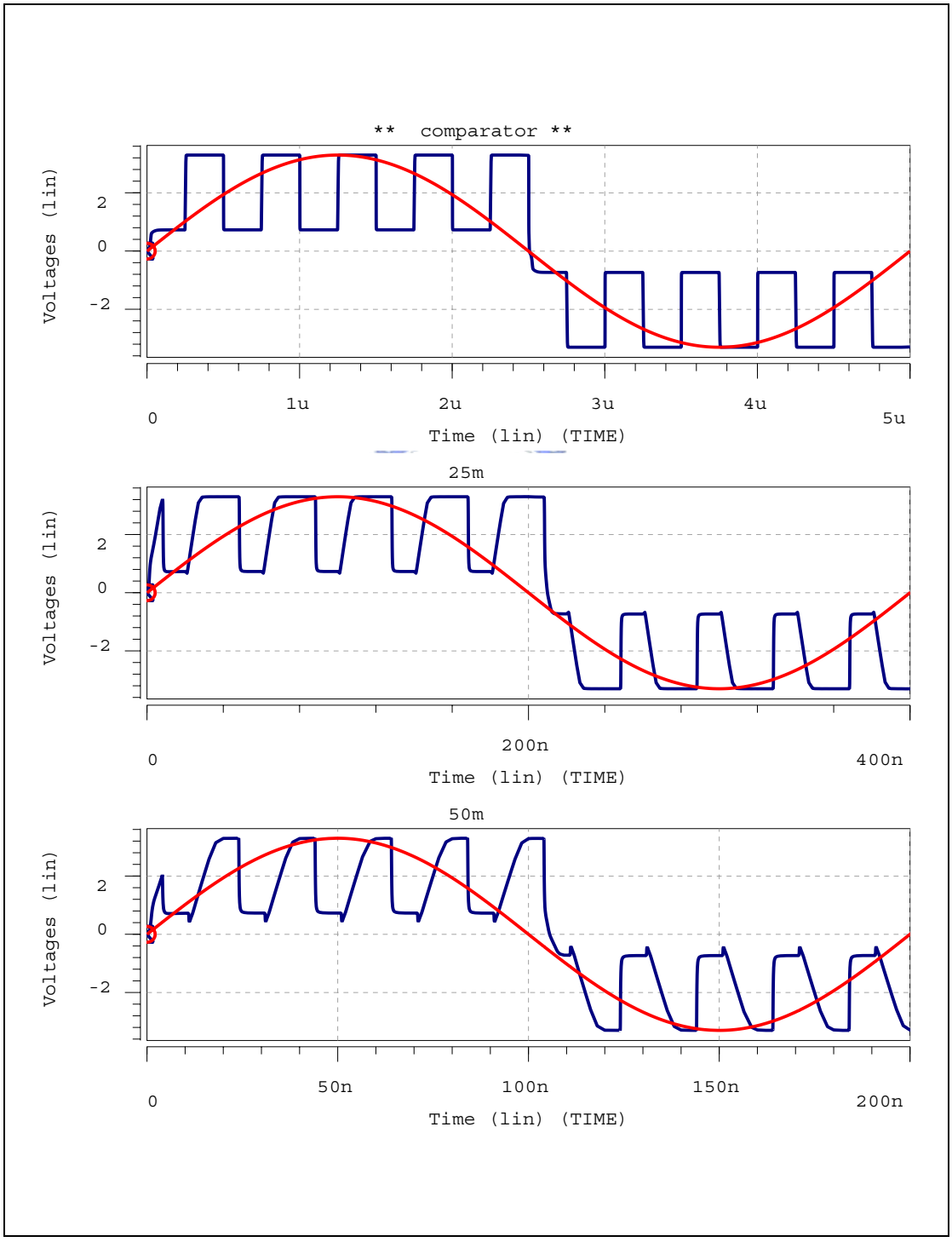

Figure 4.14 Transient analysis of the preamplifier

4.2.3 Switches and Capacitors

The switches and capacitors are frequently used in integrated circuit design, for example, sample and hold circuits. No mater each of them can be built up by transistors. Special process of capacitors, however, is good for implementation of larger size and lower variation. Different fabricator provides different capacitor for designers to use, but this is irrelevant to the main subject here, we will only discussed some key points about them. On the contrary, switches are only made up by transistors without special process and need to be discussed more detail.

A MOS transistor can serve as a switch because (a) it can be on while carrying zero current and (b) its source and drain voltage need not follow that variation [29]. Figure 4.15(a) show three structures of CMOS switches. The first point to note is how to turn on them? As we know, for NMOS, Vgs must bigger than Vthn, for PMOS, Vsg must bigger than |Vthp|. Suppose the gate voltage of NMOS and PMOS is VDD and ground respectively, and then the output ranges of different switches can be estimated, the results are shown in Figure 4.15(b). It is important that transmission gates which are made up by a PMOS and a NMOS can pass full voltage level. The second point to note is the speed consideration. Simply speaking, a switch circuits can be seen as a R-C circuit because of turn on resistance. Smaller turn on resistance has smaller time constant and can approach to input level sooner. So, we focus on the evaluation of turn on resistances.

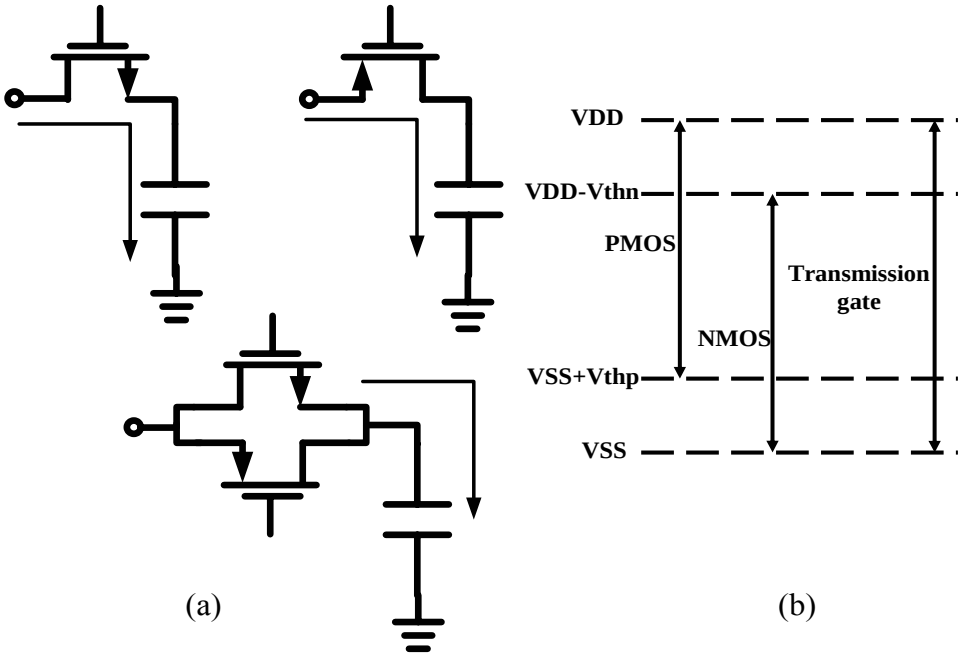

Figure 4.15 (a) MOS switches (b) Output level for different switches

As illustrated in front of page, if NMOS switches on, the output is approximately equal to input and the transistor is operated at triode region. Thus we can obtain the current flowing the switch is:

$$I_D = \mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{ds})V_{ds}$$

So we can express turn on resistance of a NMOS switch as:

$$R_{on\_NMOS} = \frac{V_{ds}}{I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{ds})} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{thn} - V_{in})} \quad (4.14)$$

Similarly, turn on resistance of a PMOS switch and a transmission gate is:

$$R_{on\_PMOS} = \frac{V_{ds}}{I_D} = \frac{1}{\mu_p C_{ox} \frac{W}{L}(V_{in} - Vss - V_{thp})} \quad (4.15)$$

$$R_{on\_transmission} = \frac{1}{\mu_p C_{ox} \frac{W}{L}(V_{in} - Vss - V_{thp})} // \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{thp} - V_{in})} \quad (4.16)$$

It is clearly that:

(a) Bigger device ratios have smaller turn on resistance, but larger area is needed.

(b) Turn on resistance is a function of input level.

(c) For a transmission gate, NMOS dominates the turn on resistance when input is low. PMOS dominates the turn on resistance when input is high.

Despite equations written above, accuracy is not enough for high speed applications. The CAD simulation is necessary and results are indicated in Figure 4.16. The first curve is turn on resistance of NMOS, the second is turn on resistance of PMOS, and the last is turn on resistance of transmission gates. These curves are based on that, device ration of NMOS and PMOS is 20/0.36 (or 4/0.36) and 20/0.36 respectively. All of them are agreed with principles we proposed before. There is another important thing we need to know, transmission gates allow full swing and constant resistance all the time, but requires complementary clocks and larger area. If input level is confined in some region, NMOS or PMOS is satisfied for adoption.

This work is implemented in single-poly five-metal 0.25um CMOS process provides metal-insulator-metal (MIM) process to implement capacitors. The structure and equivalent circuit is shown in Figure 4.17 next page. By the way, the parasitic capacitor of the bottom plate is always larger than top plate, so we should avoid the input nodes of OPAMP connecting to the bottom plate s of capacitors.

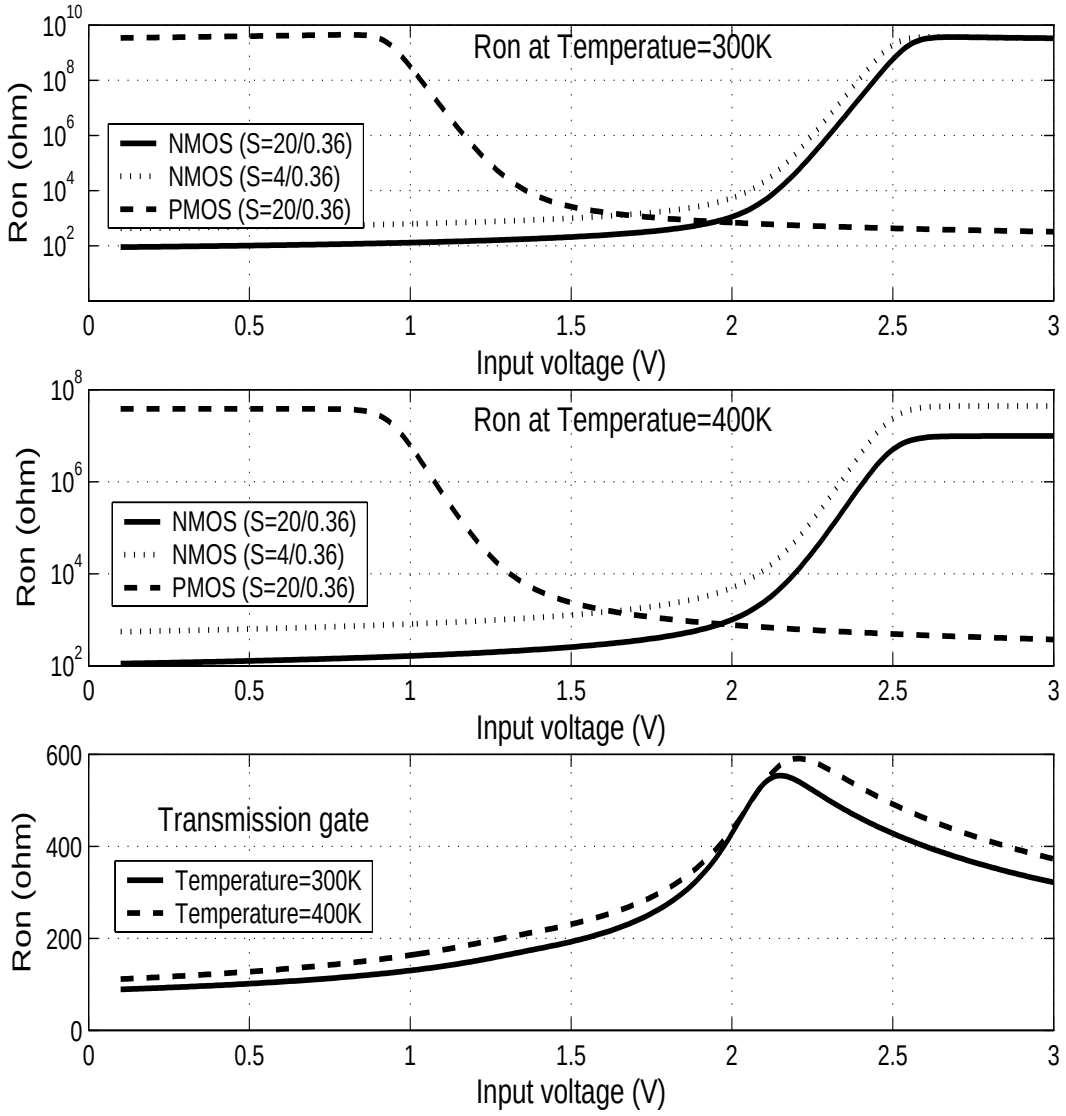

Figure 4.16 Turn on resistance of NMOS, PMOS, and a transmission gate

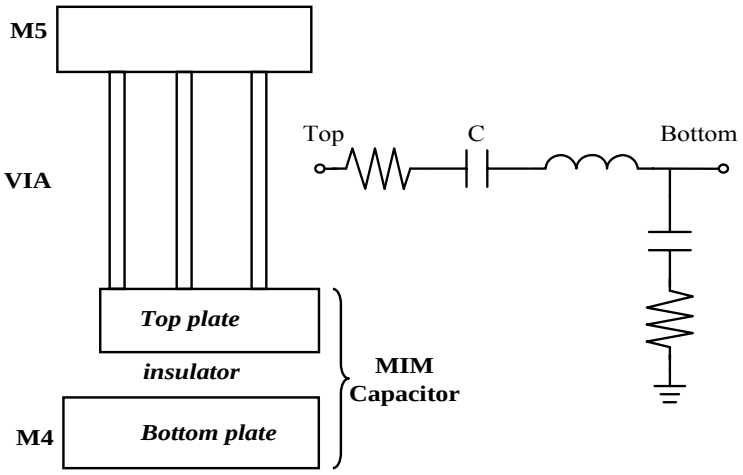

Figure 4.17 MIM capacitor structure and its equivalent circuit

4.2.4 Integrator

An integrator is a main building block of SDM. It plays a loop filter to eliminate quantization error of the ADC, so the overall performance of the modulator is determined by it. We shall now confine our attention to realize an integrator by OPAMP, comparator, switches and capacitors which we have discussed in detail at early sections.

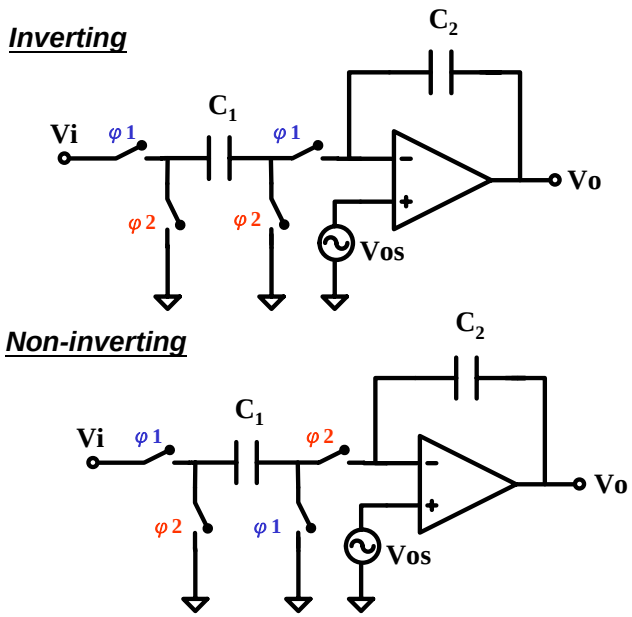

Figure 4.18 A pair of complementary SC integrators

Our objective is a discrete-time integrator based on switched-capacitor (SC) technology. Toward that we show a pair of complementary SC integrator in Figure 4.18, one is called inverting and another is called non-inverting. Both of them are completely insensitive to stray capacitances between any node and ground [15]. For infinite amplifier gain and bandwidth, Figure 4.18 has the ideal transform functions below:

$$Inverting\ :\ H(z) = \frac{-C_1}{C_2} \times \frac{1}{1-z^{-1}} \tag{4.17}$$

$$Non-inverting\ :\ H(z) = \frac{C_1}{C_2} \times \frac{z^{-1}}{1-z^{-1}} \tag{4.18}$$

Assume there is an offset voltage at the OPAMP input node, these equations are:

$$Inverting\ :\ Vo(z) = \frac{-C_1}{C_2} \times \frac{1}{1-z^{-1}} Vi(z) + \frac{C_1}{C_2} \times \frac{1}{1-z^{-1}} Vos + Vos \tag{4.19}$$

$$Non-inverting\ :\ Vo(z) = \frac{-C_1}{C_2} \times \frac{z^{-1}}{1-z^{-1}} Vi(z) + \frac{C_1}{C_2} \times \frac{1}{1-z^{-1}} Vos - Vos \tag{4.20}$$

Figure 4.19 shows several structures to complete differential input, all operational procedures of them are similar to the complementary SC integrators.

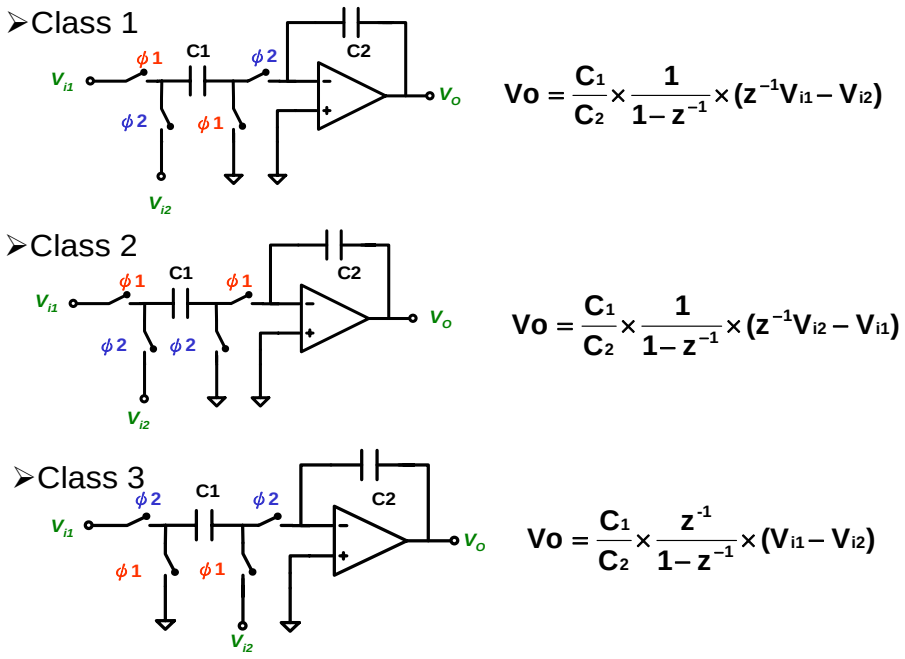

Figure 4.19 Differential SC integrators

Owing to limitations of OPAMP, however, the deviation of ideal ones and SC integrators can not be ignored. However, SC filters are much tolerant of OPAMP limitations when encountered in active-RC filters. Fuller discussion has been present in section 3.1, we only plot the gain and phase versus frequency at Figure 4.20 for SCI with OPAMP described in section 4.2.1 and switches described in section 4.2.3.

From the equations (4.19) and (4.20), the offset voltage affects output signal seriously, in order to attenuate this effect, a popular schematic called correlated double sampling (CDS) is employed [30], Figure 4.21 at next page is a simple diagram of it. An offset capacitor is the key feature of CDS, and then the offset voltage is double sampled, as its name, by this capacitor. During $\varphi 1$, the input signal and offset voltage is stored at C1 and Cos respectively, during $\varphi 2$, the charges on the C1 are transferred to C2 and offset voltage is still sampled on Cos, then output level is unaffected by it.

According to previous discussions, we adopt a differential SC integrator, like Figure 4.19 class one, and add CDS technology to complete the loop filter in SDM, fully Figure is shown in 4.1-1. Table 4.1 summarizes sizes of the SC integrator and operational period. We don't repeat these data again, readers can refer to section 4.1

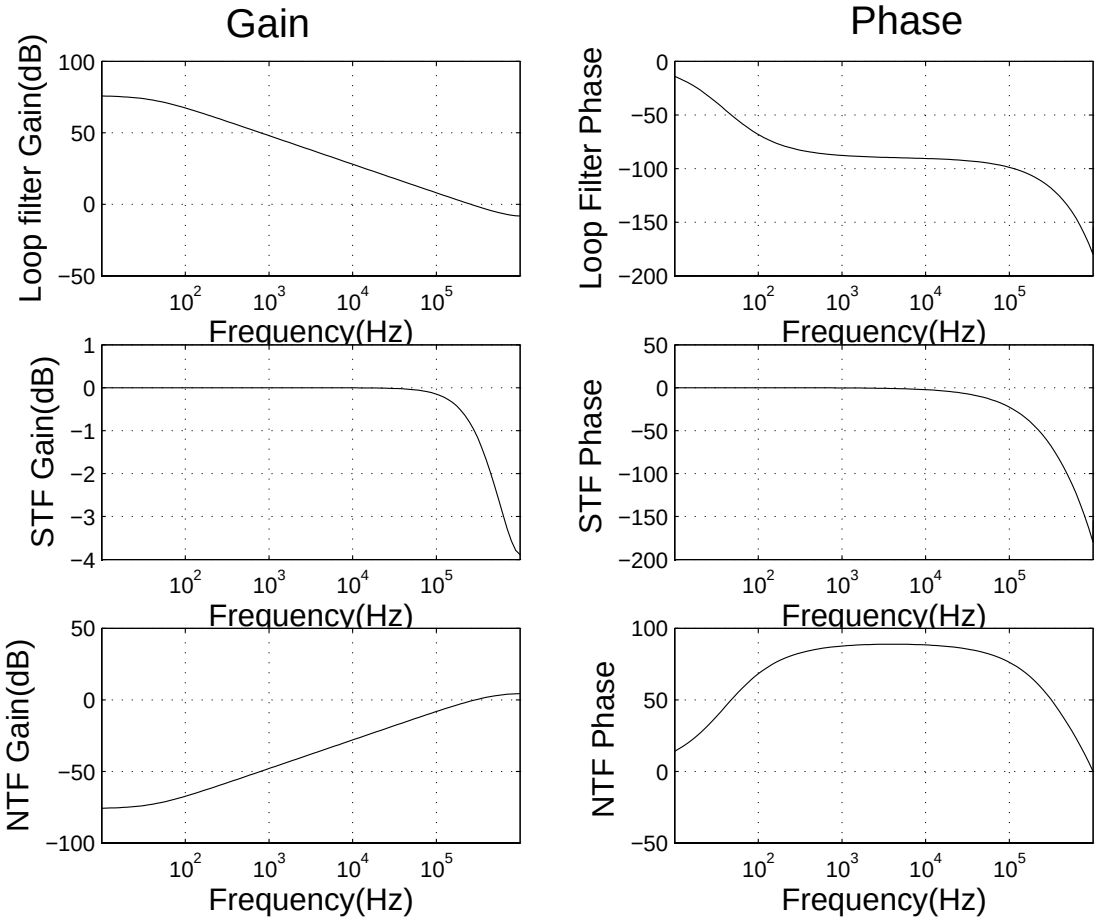

Figure 4.20 The Bode plot of SCI with present OPAMP, C1/C2=0.8, and 2Mhz clock

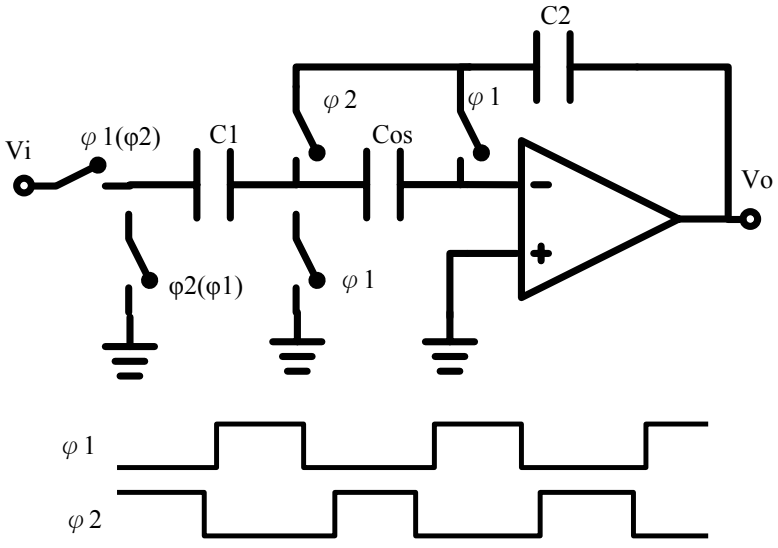

Figure 4.21 A CDS SC integrator

4.2.5 Feedback DAC

From the viewpoint of system level design, the function of the feedback DAC is generating an analog output to feedback into the SC integrator when sensing a digital signal input comes from the quantizer. In view of circuit level design, this feedback DAC has to output a pair of signals when fed a complementary input. For tracking input signal, these output signals are generally reference voltages. The feedback DAC circuit is shown in Figure 4.22 below [12].

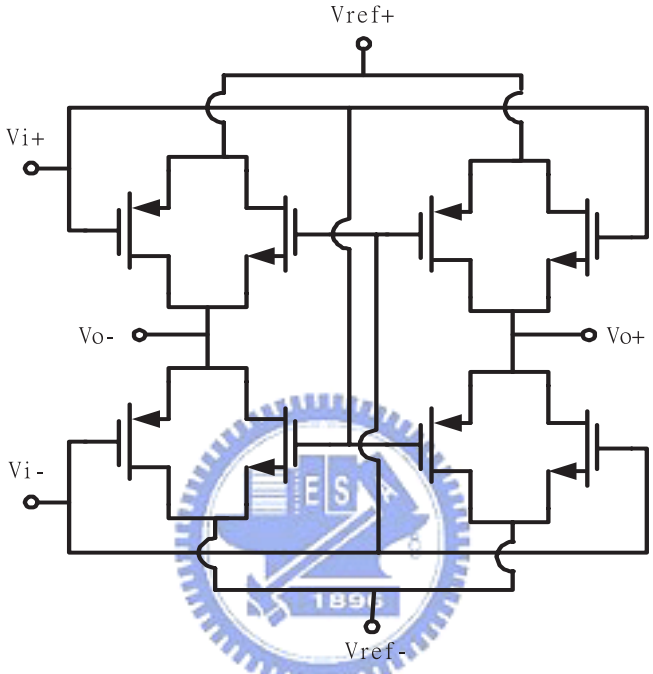

Figure 4.22 Feedback DAC circuit

Because of using discrete-time comparator mentioned previously, the outputs of it are binary signals in partial of time, and then can not be feedback into SC integrator directly. Employing an inverter behind the discrete time can solve most of problems, but the speed consideration is another issue. Decreasing the output swing of an inverter undoubtedly decreases settling time. On the other hand, the capability of driving next stage should not be omitted. It is clear that there are four transmission gates in Figure 4.22, and only two of them will be turn on anytime, which are controlled by a comparator with an inverter buffer. Using CAD simulation tool, HSPICE, all of these transistor sizes are 1 μm/0.36 μm, and the threshold voltage is 0.6 volt when Vref+ is 2.0 volt and Vref- is ground. This point deserves explicit emphasis that the turn on resistances of transmission gates must be considered with input capacitance of SC integrator when determine device ratio, in order to sample correct polarity feedback voltage.

4.2.6 Output Buffer

Owing to inescapable parasitic capacitance caused by package and next input stage, we need an output buffer to pass modulated output signals outside, so this output buffer is connected afterward to SDM, as Figure 4.1. These modulated output signals, in fact, are binary signals produced by the comparator. Therefore the question now arise is propagation delays, including high-to-low and low-to-high. Very often, we adopt an inverter chain to reduce delays attributed capacitance loading, shown in Figure 4.23(a), then there are tow issues (a) how many stage are needed to minimize the delay (b) how to size the inverters.

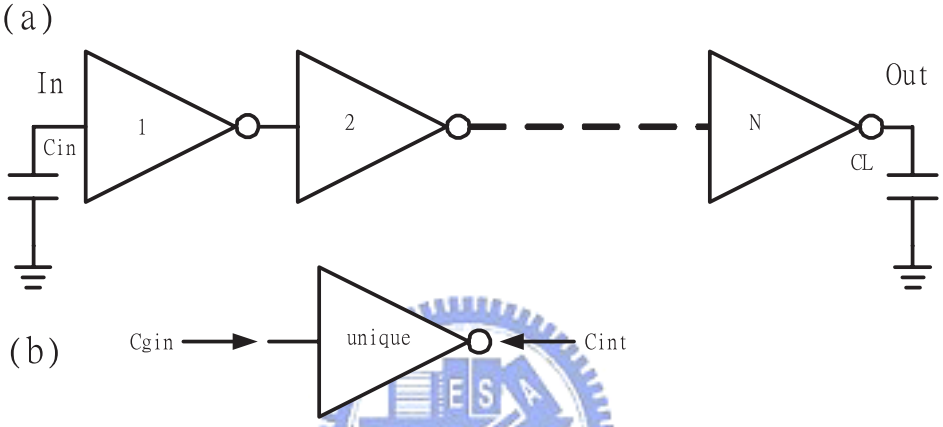

Figure 4.23 A chain of N inverters with output capacitance.

The optimize size of each inverter is that, each inverter is sized up the same factor *f*, the factor *f* and the minimum delay through the chain can be derived as [23]:

$$\gamma = C_{\text{int}} / C_{gin}\,;\; F = CL / Cin$$

$$\gamma + \sqrt[N]{F} - \frac{\sqrt[N]{F}\ln F}{N} = 0 \qquad (4.21)$$

$$f = \sqrt[N]{F} = \sqrt[N]{CL/Cin} \qquad (4.22)$$

$$t_p = Nt_{po}(1 + f/\gamma)$$

Where *F* is the overall effective fan-out, t_{po} is unloaded delay, γ is depicted in Figure 4.23(b) and is a proportionality factor dependent on processes. When, CL and Cin are given, we can obtain the right stage, N, by equation (4.21), and the sizing-up factor, *f*, by equations (4.22).In our work, N is 4 and f is 3.67, then Table 4.6 summarize all device sizes of the output buffer.

Table 4.6 Output buffer device ratios summary

	Stage 1	Stage 2	Stage 3	Stage 4
CMOS	1 μm/0.36 μm	3.7 μm/0.36 μm	13.6 μm/0.36 μm	25 μm*2/0.36 μm

4.3 Layout Level Design

A physical design, in the context of integrated circuit, is referred to as layout [20]. Effects of parasitic components and mismatching will damage the performance of the actual chip, so layouts must be considered heavily in design process. Several principles of layout needed to obey in order to minimize crosstalk, mismatches, noise and so on [29]. This layout of experimental SDM chip is introduced by (a) design considerations for higher temperature (b) multi-finger transistors (c) symmetry (d) dummy cell (e) common centroid. Beside the elevated temperature issues which has mentioned in section 3.2, it is not necessary for the purpose of this thesis to enter into detailed discussion of others tricks, reader can refer to bibliographies.

In order to meet layout considerations, the OPAMP shown in Figure 4.1 and the comparator shown in Figure 4.12 have to be redrawn, and are depicted in Figure 4.24.

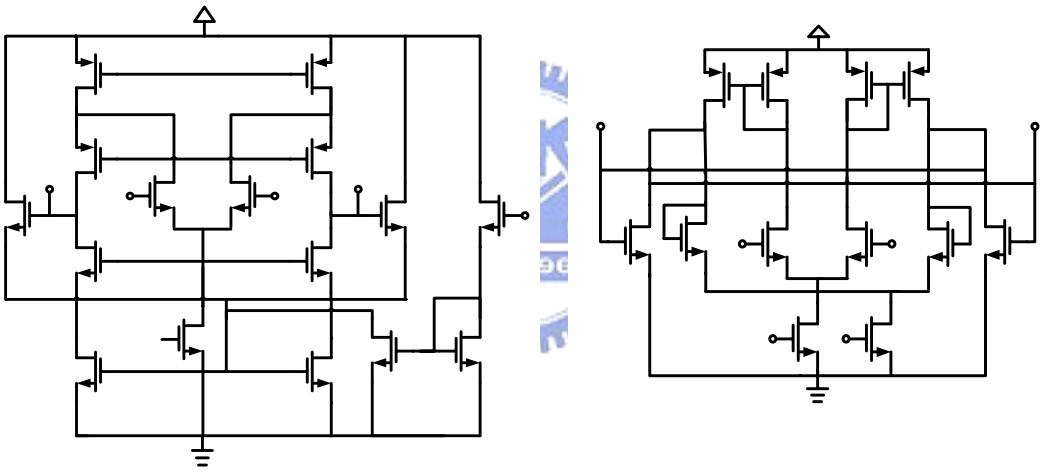

Figure 4.24 Redraw (a) OPAMP (b) Comparator

There are eight I/O ports, including a pair of differential inputs, a pair of modulated outputs, and four different phase clocks. All of these signals are generated by an external circuit which will be discussed in chapter five. This work is fabricated in a 0.25 μm 1P5M 3.3V standard CMOS with MIM process. The layout diagram is shown in Figure 4.25. Active area was 0.04 mm^2 excluding output buffers.

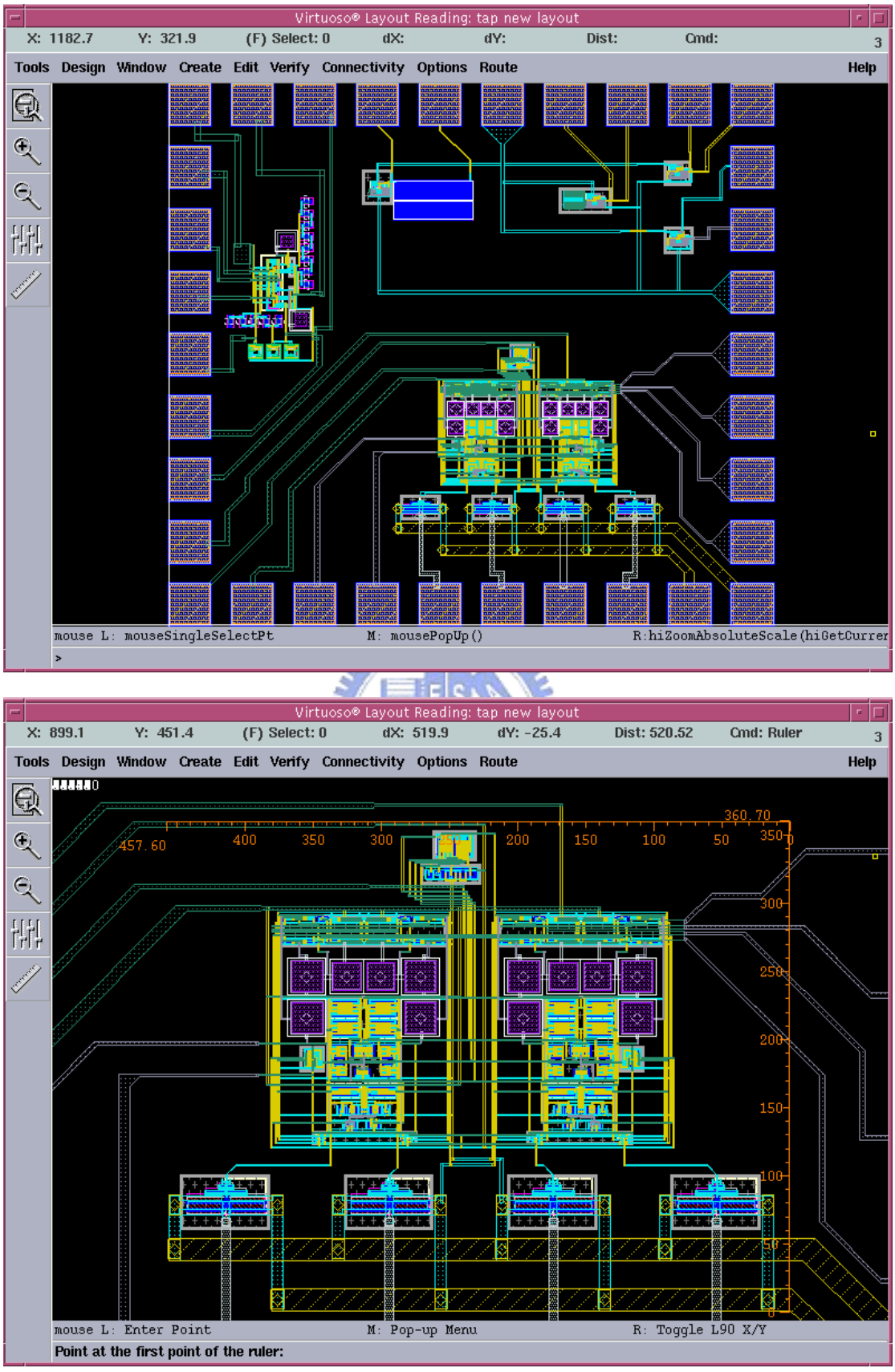

Figure 4.25 Diagram of SDM layouts

4.4 Simulation Results

Figure 4.26 plots the time domain simulation results in which digital filter is fulfilled by program MATLAB. As well as Figure 4.27 plots the frequency domain simulation results, the SNDR is 50.9dB and SFDR is 42dB with 2MHz clock rate, OSR=64 for a -1dB full scale, 5kHz sinusoidal input. It is evident that quantization noises are shaped and the slope is about 20dB/dec for this first order SDM. The SNDR and the power spectral density (PSD) is calculated by 4096 points Fourier transformed data sets (FFT) with Hanning window [14].

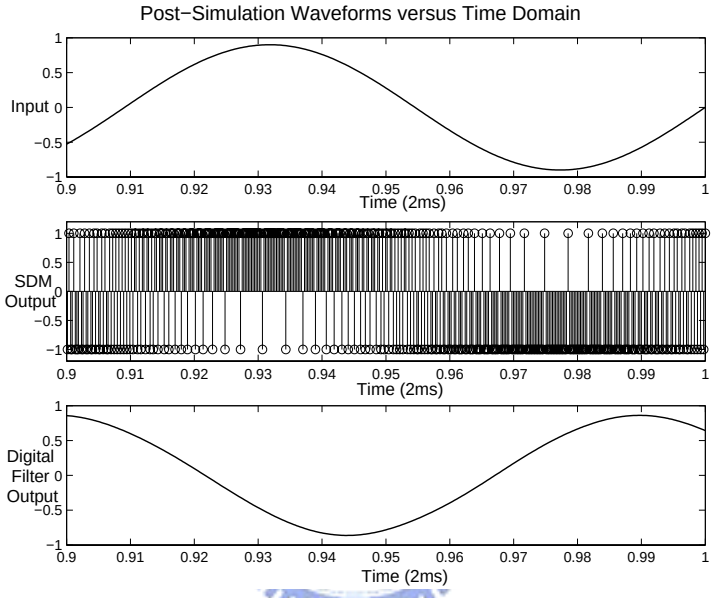

Figure 4.26 Transient Analysis of proposed SDM

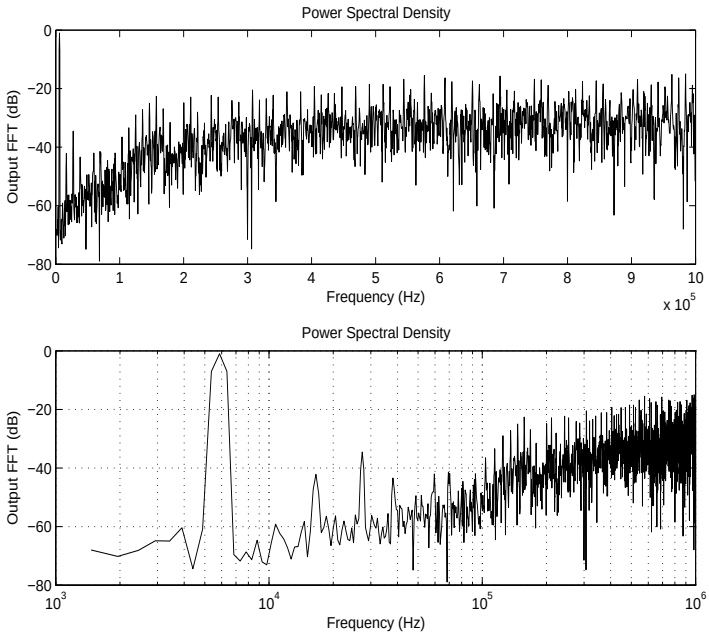

Figure 4.27 Power spectrum of proposed SDM (a)log scale (b)linear scale

In order to detect frequency response within 16kHz bandwidth, calculated PDF by 65536 FFT with the same input signal and operating conditions, then the results is shown in Figure 4.28. And then is a series of three diagrams illustrating the performance of proposed SDM: Figure 4.29 indicates the input mismatch degrades seriously SNDR. Figure 4.30 is the Dynamic range simulation which implies DR=39dB. Figure 4.31 shows SNDR versus temperature which reveals 8 bits resolution at 25°C and 7 bits resolution at 125°C.

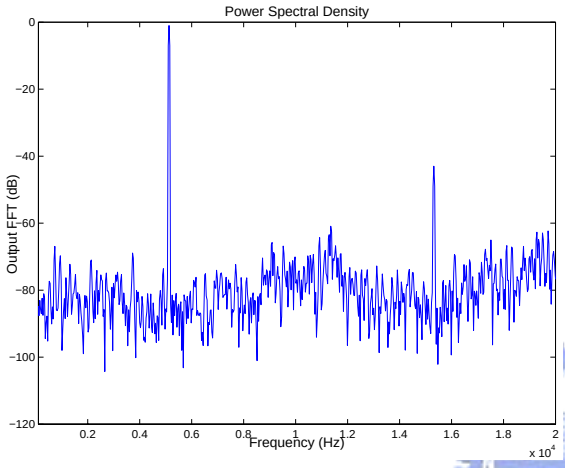

Figure 4.28 Baseband output spectrum

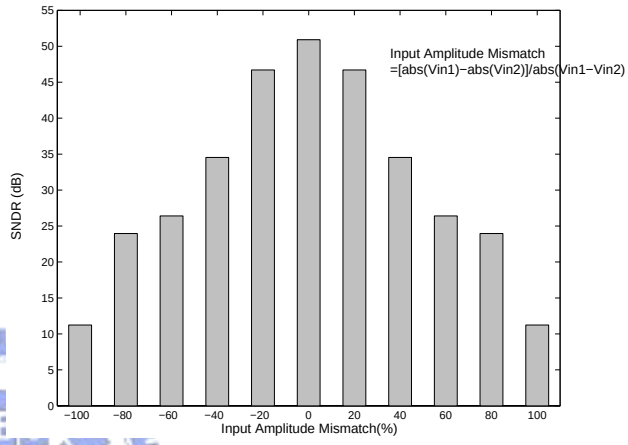

Figure 4.29 SNDR versus input mismatch

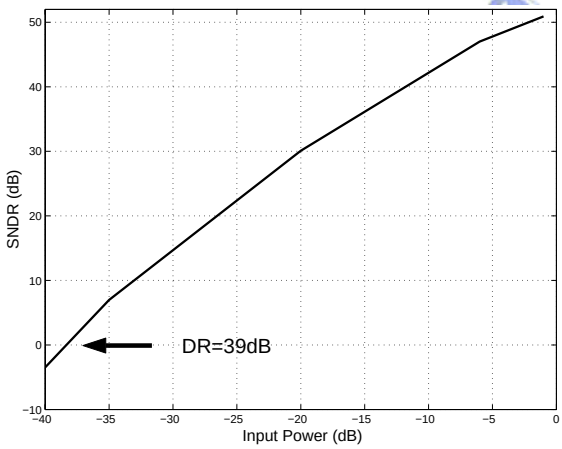

Figure 4.30 Dynamic range simulation

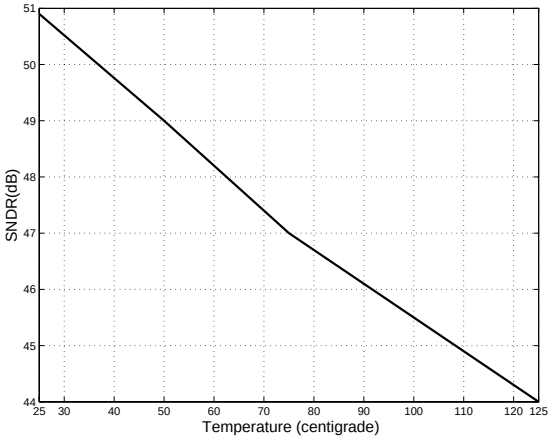

Figure 4.31 SNDR versus temperature

Chapter5

Testing Setup and Experimental Results

A testing setup for fabricated prototype chip is presented in this chapter. Several accessory circuitries such as clock generation circuitry, biasing circuitry and differential signal generator are designed and verified. And a costumed designed printed circuit board (PCB) is designed and fabricated to integrate the accessory circuitries and targeting prototype chips in order to measure the performance metrics of proposed design. This chapter also described the instrumental setup and signal processing mechanism to measure and analysis the output for proposed design. Following by above information, the experimental results of above environment is presented and discussed. And the measured performance metrics is summarized in the end of this chapter.

5.1 Testing Environment

Figure 5.1 shows the whole measurement process, including a device under test (DUT) board, a logic analyzer and personal computer (PC). A PCB combines voltage regulators, clock generators, input terminal and DUT to measure various operations of experimental chip. The regulators are provided by 9 V batteries and the clocks are driven by a crystal oscillator. The input signal is generated by audio signal generator, and digit output is fed to the logic analyzer, then load to PC for MATLAB simulation.

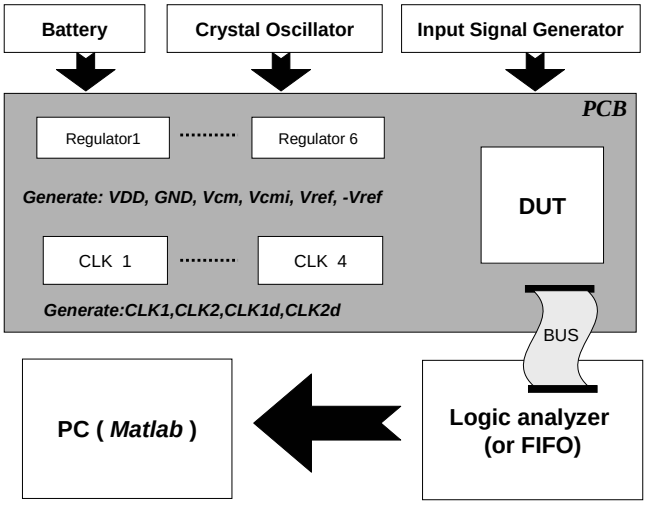

Figure 5.1 Experimental test setup

We adopt HP16500B, Agilent 54641D to measure mixed signal, including every input/output (I/O) port of DUT and auxiliary circuits on PCB. Figure 5.2 shows the measurement situation.

Figure 5.2 The measurement situation

5.2 PCB circuits

Details of the various components of this test system will be described at this section, we consider this subject under three heads: (a) clock generator; (b) voltage regulator; (c) input terminal. The photograph and description of this PCB are shown at next page.

Because the CDS technology discussed in Chapter 4.2 are used, there are four different phase clock are necessarily input DUT to control switches accurately. The schematic of non-overlap clock are depicted in Figure 5.3 [23]. The number of the inverter chain can be altered by external switches, the longer inverter chain cause the longer delay time and smaller duty cycle. More noteworthy are:

- The smaller duty cycle introduces the incomplete setting error which generates harmonic distortion and then diminishes the peak SNR.
- The longer duty cycle may result in the operation abort of switches due to clock jitter and clock overlap.

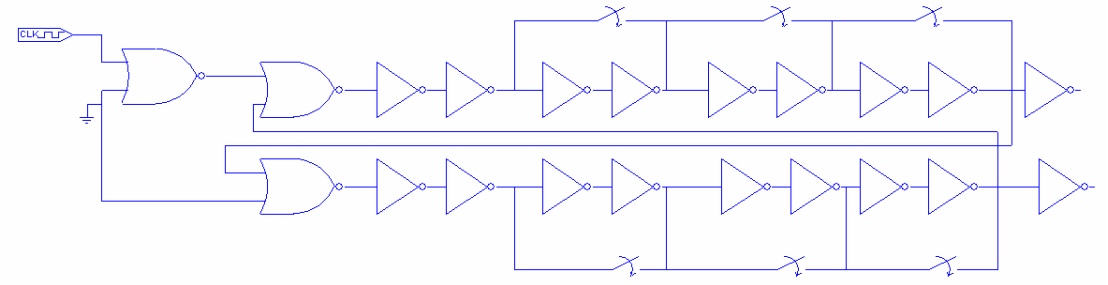

Figure 5.3 The schematic of the clock generator

The analog and digital voltages are generated by LM317 adjustable regulator as shown in Figure 5.4. We use 9V batteries instead of a general power supply to reduce Power Supply Rejection Ratio (PSRR) introduced supply noise. Furthermore, the output of voltage regulator are connected with the parallel combination capacitors, thus the capacitor arrangement provide decoupling of both low frequency noise with a large amplitude and high frequency noise with a small amplitude [16].

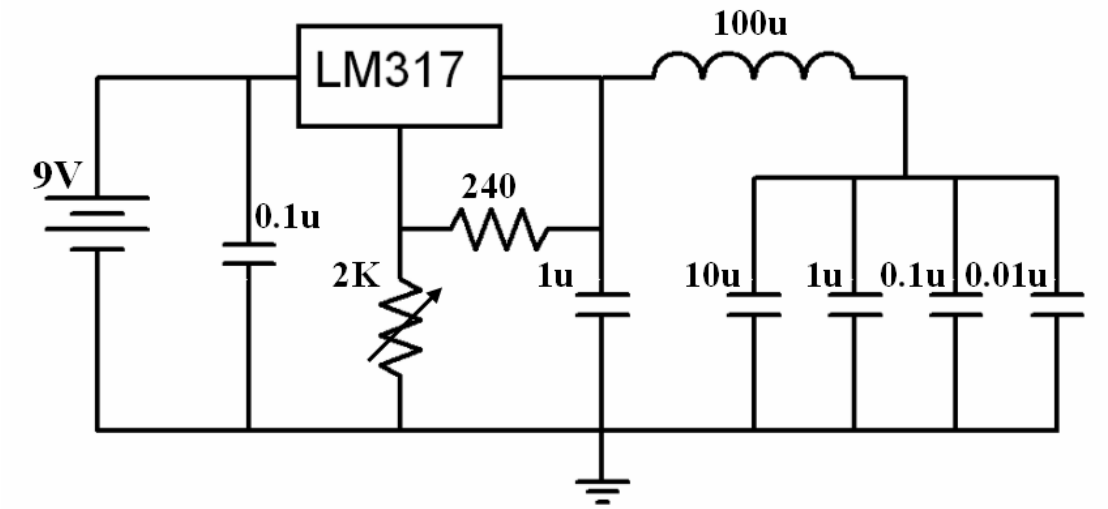

Figure 5.4 The schematic of the voltage regulator

An audio generator (HP 3325B) only provide AC component of input signal, the DC component have to originate from AC coupled circuits drawn in Figure 5.5. Because we can not ensure the common mode input matching, the adjustable resistances are adopted to tune the voltage right. Figure 5.6 shows the whole PCB and represent sub-circuit diagrammatically. Figure 5.7 is a series of two diagrams illustrating (a) the differential input signal (b) four clock signal with different phase.

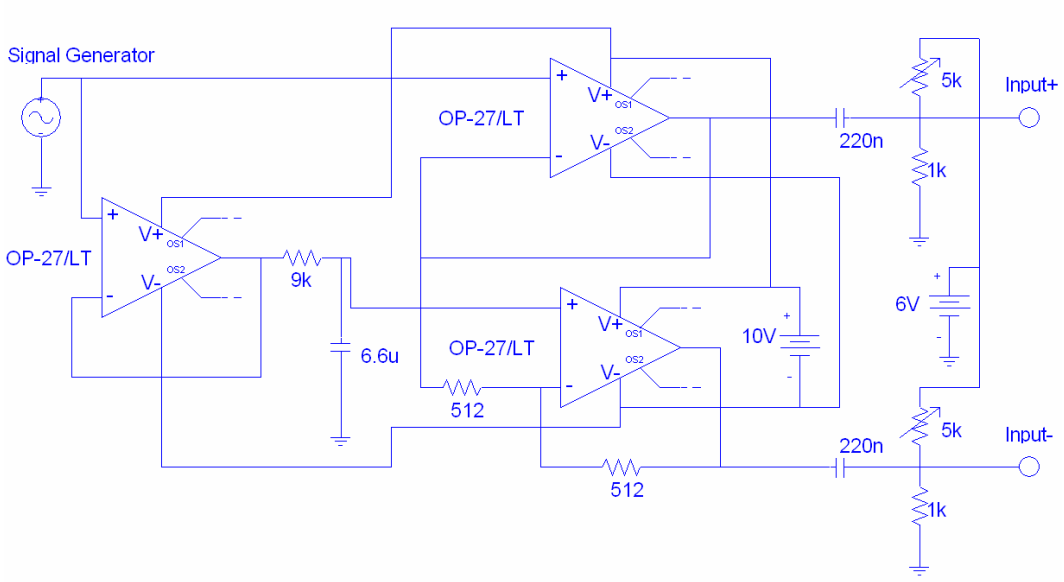

Figure 5.5 Input terminal circuit

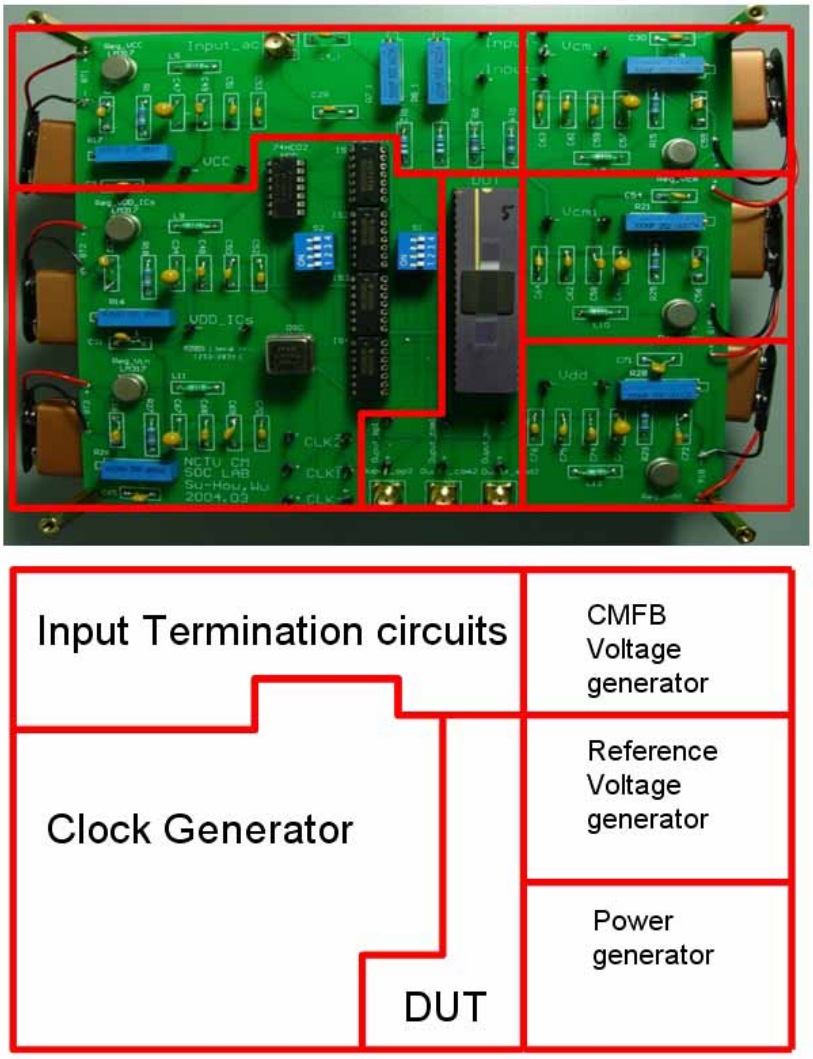

Figure 5.6 The photograph of the whole PCB

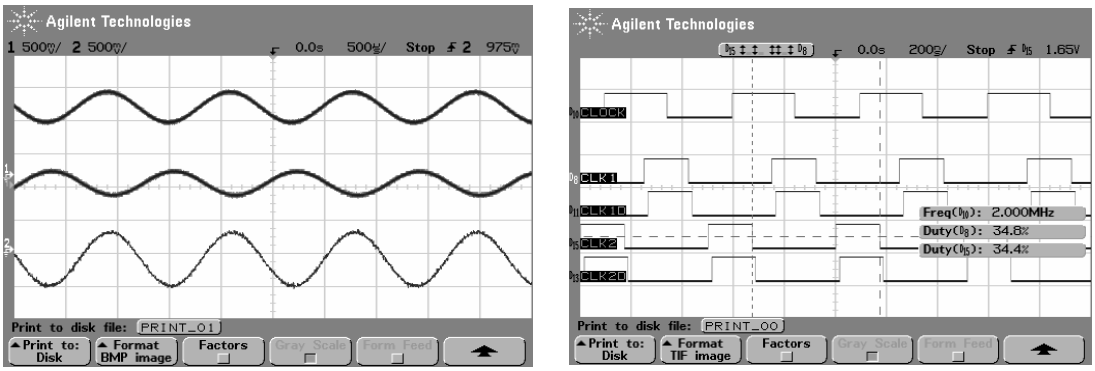

Figure 5.7 Measured input waveforms of the DUT

5.3 Performance Evaluations

The performances of SDM in this work were assessed by input it with a fully sinusoidal signal and acquired the digital output from a logic analyzer, after then transferring them into PC. Subsequent analysis contained digital filtering and frequency domain examination is performed by program MATLAB.

A die photograph of experimental SDM is shown in Figure 5.8, its active are is 0.16mm^2 including output buffers, sub-circuits for verification and bias circuits. This proposed SDM based on first-order structure are operating at OSR=64, clock rate is 2 MHz, and the corresponding bandwidth is 15.625 kHz. The time domain analysis is measured by an oscilloscope (Agilent 54641D) as well as the differential inputs and outputs of this prototype are shown in Figure 5.9, simultaneously, these waveforms without decimation filter and calculated by 2000 FFT with Hanning window are shown in Figure 5.10, which consists of the whole Nyquist bandwidth spectrum and the baseband spectrum. The bit-stream of SDM outputs drive a logic analyzer (HP16500B) and are evaluated digital signal processing (DSP) by MATLAB, the measured performance SNDR is 41 dB and SFDR is 42 dB by 4096 FFT with Hanning window. The log scale plot and linear scale plot are sequentially shown in Figure 5.11. Figure 5.12 exhibits the decimation filer outputs simulated in MATLAB SIMULINK to perform transient analysis, in which the pass-band frequency and stop-band frequency is π/64 and π/32 respectively. The static and dynamic performances of this SDM are summarized in Table 5.1 and Table 5.2.

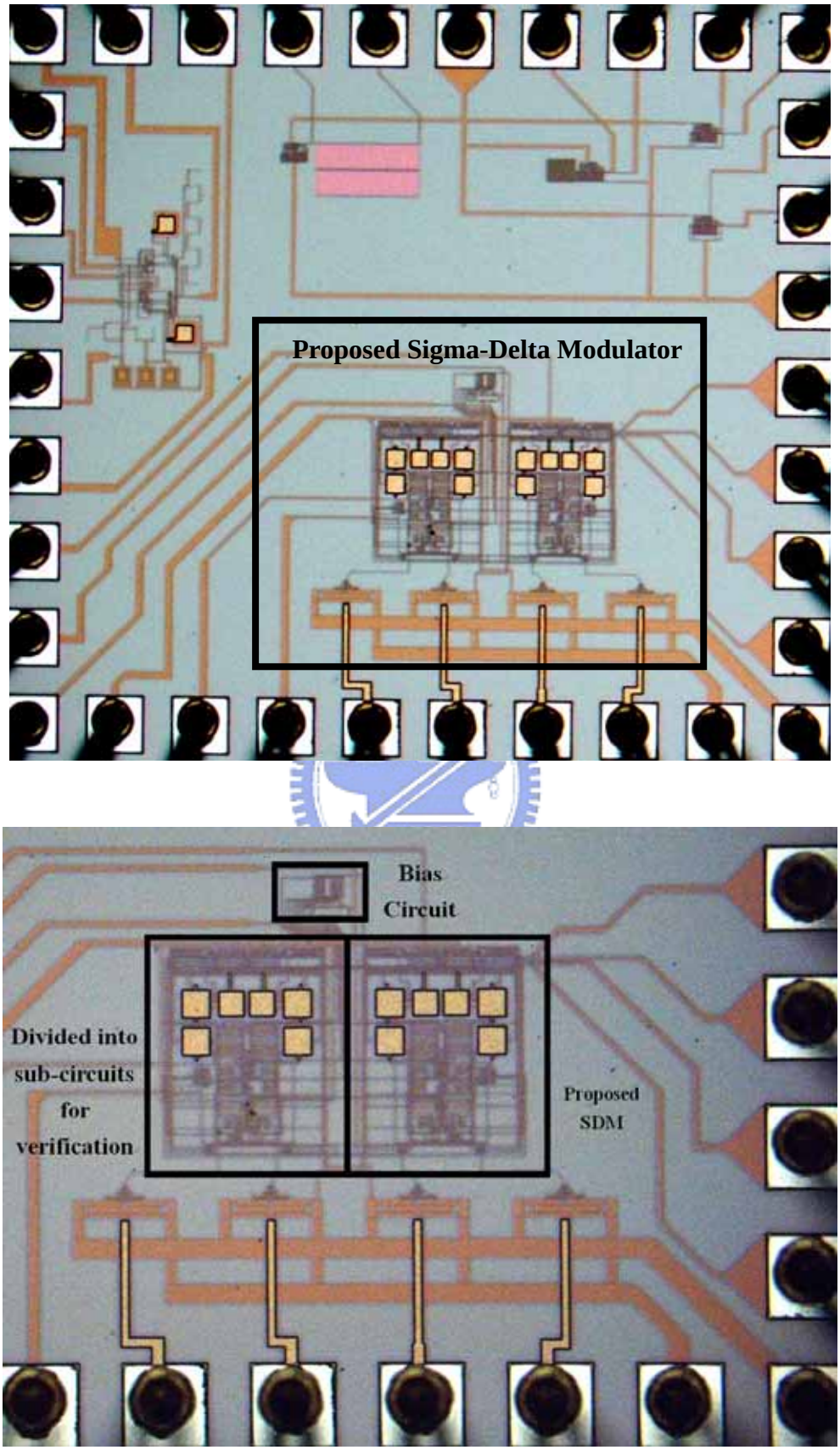

Figure 5.8 Die micrograph

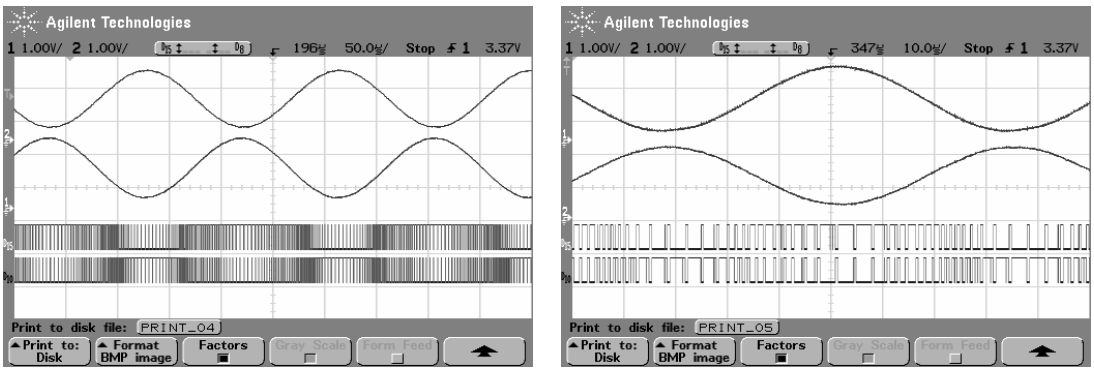

Figure 5.9 Measured output waveforms of the SDM

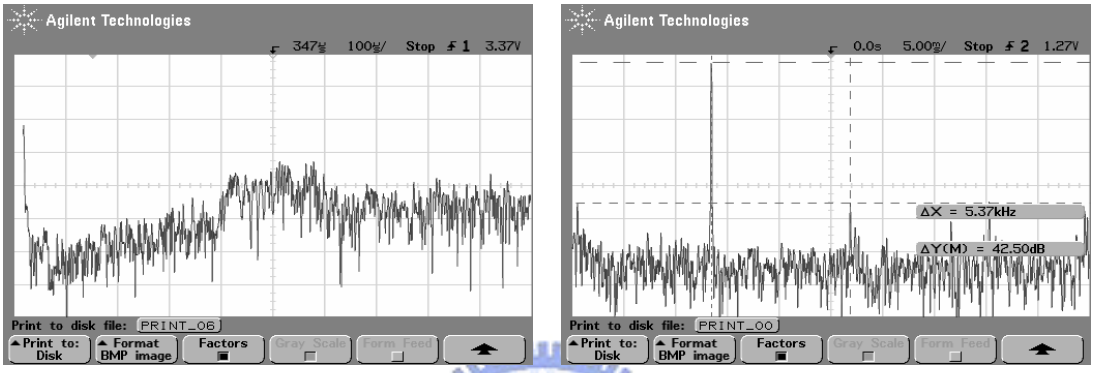

Figure 5.10 Measured output spectrum of the SDM (a) all-band (b) in-band

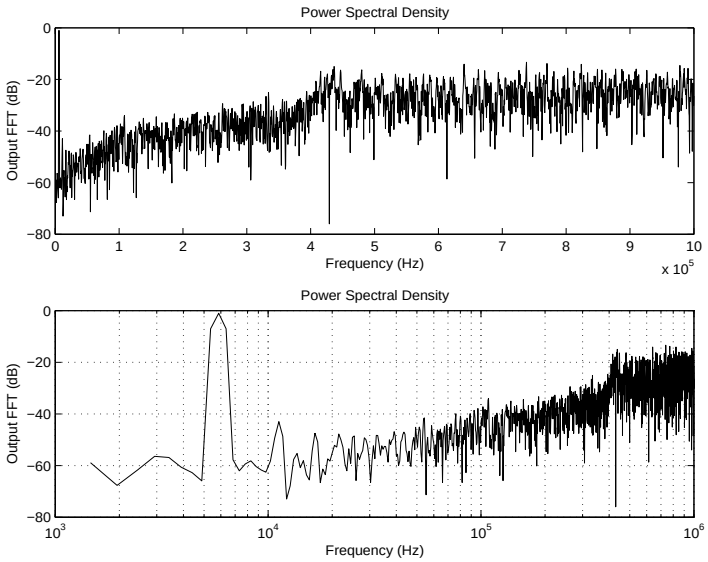

Figure 5.11 (a) linear scale PSD (b) log scale PSD

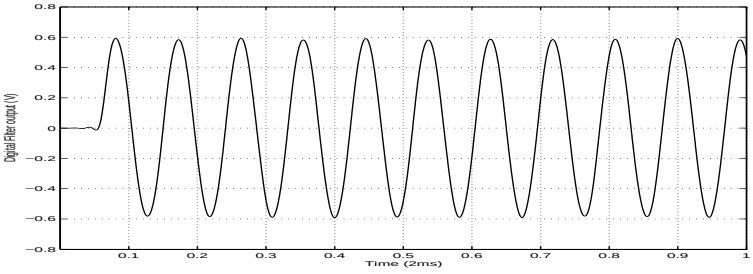

Figure 5.12 Digital output simulation

Table 5.1 Pin assignments

Pin	Name	Description	Experimental Voltage
5	Vi-	Input (180o)	1200±650mV Frequency<15kHz
6	Vcm	CMFB control voltage	2000±50mV
7	NC	No connection	-
8	Vcmi	CMFB control voltage	1250±50mV
9	Vi+	Input (0^o)	1000±750mV Frequency<15kHz
10	Vo_op-	OPAMP output (180^o)	Command mode=1700±100mV
11	Vo_op+	OPAMP output (0^o)	Command mode=1700±100mV
12	Vo_com+	Comparator output (0^o)	Command mode=1700±100mV
13	Vo_com-	Comparator output (180^o)	Command mode=1700±100mV
14	Vo_mod-	Modulator output (180^o)	Low=0V High=3.25V
15	Vo_mod+	Modulator output (0^o)	Low=0V High=3.25V
16	Vdd	DUT Power	3250±50mV
17	Gnd	DUT Ground	0±100mV
18	NC	No connection	-
19	CLK1	Clock 1	Low=0V High=3V Frequency=2M
20	CLK1d	Clock 1 delay	Low=0V High=3V Frequency=2M
21	CLK2d	Clock 2 delay	Low=0V High=3V Frequency=2M
22	CLK2	Clock 2	Low=0V High=3V Frequency=2M

Table 5.2. Performance Summary

Architecture	First order SDM
Process	Standard CMOS 0.25μm with MIM
Area	0.16mm^2 (including output buffers)
Sampling Rate	2 MHz
OSR	64
Input Bandwidth	15.625 kHz
DR	39 dB
Peak SNR	46 dB
Peak SNDR	41 dB
SFDR	42 dB
Power Dissipation	4.5mW

5.4 Summary

The circuit present in this chapter is implemented by design considerations described in Chapter 3 and circuit design approaches described in Chapter 4. This work emphasized the complete design flow for a thermal-aware ADC for thermal management system. However, the clock generators and voltage regulators are fulfilled on an external PCB which can not be tested at higher temperature environment, therefore the actual performance operated at elevated temperature are not accessed veridical.

The predicted resolution of this SDM is 8 bits (51 dB), but the actually ones is 6.5 dB (41 dB), the deviation is contributed by thermal noise, clock jitter, OPAMP performance decay, the harmonic distortion and the noise floor of the input signal. If these error mechanisms are considered into the behavior model of system level design, the experimental results will compatible with simulation. In order to meet the requirements of thermal management, there are four recommendations for further researchers:

(1) Integrating the input terminal circuit to reduce unpredicted effects.
(2) Increasing the OPAMP output swing or decreasing the input full scale.
(3) Adapting second-order SDM to suppress quantization noise.
(4) More margin to prevent performance decay.

Chapter6

Conclusion

This thesis describes the design criteria of sigma-delta modulator (SDM) for monolithic thermal sensors. Basic concepts including quantization noise, noise shaping technique and a rough overview of SDM are introduced. Error mechanisms, for example, finite loop filters specifications, thermal noise, clock jitter are addressed sequentially. After that a system level behavior model implemented in the program MATLAB SIMULINK is proposed to realize SDM characteristics and determine the circuit specifications. As well as design considerations at high temperature are studied, such as Zero-Temperature-Coefficient (ZTC) bias points and leakage current. Additionally, a detailed description and approaches of the sub-circuits provide practical stuff for first-order hand analysis prior to computer added design.

This thesis also proposed a switched-capacitor first-order SDM which is fabricated in TSMC CMOS 0.25um standard process. The experimental result reveals: (a) eight bits resolution to satisfy the sensitivity of on-chip temperature sensors; (b) low power to avoid being the thermal source of SoC system; (c) implementation in standard fabrication process and ultra-small area to be integrated in modern VLSI. The integration of monolithic temperature sensor, proposed ADC and thermal management unit keeps the progressing trend of modern VLSI and high-density circuits without thermal problems.

A prototype for thermal-aware SDM has been fulfilled. The next step is to integrate clock generators and differential input terminal circuits for thermal sensors to accomplish the frond-end of thermal management system. Therefore, the realization of adapt active heat dissipation mechanisms in VLSI and high-speed circuit can avert from overheating and confirm circuitry reliability. On the other hand, if (a) the system level behavior model is extent for high-order SDM; (b) the design approaches of sub-circuits is enriched with process scaling; the design flow of this work can be compatible to various applications for further researchers.

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