國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

熱退火處理對於大氣電漿沉積銦鎵鋅氧化物薄膜電晶體之特性影響

The effect of thermal annealing on IGZO TFT properties prepared by atmospheric pressure plasma jet

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中華民國一〇〇年八月

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電子工程學系　電子研究所碩士班

碩　士　論　文

A Thesis

Submitted to Department of Electronics Engineering and Institute of Electronics College of Electrical and Computer Engineering

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of Master

in

Electronics Engineering

August 2011

Hsinchu, Taiwan

中華民國一〇〇年八月

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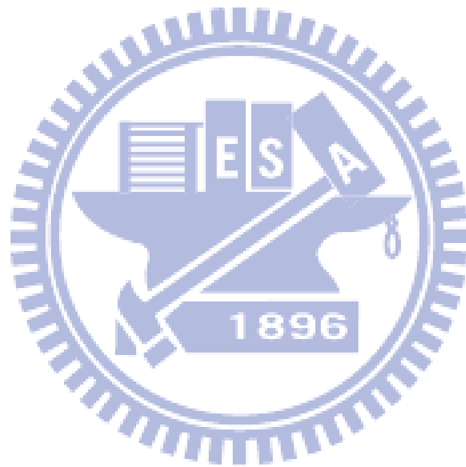
摘要

本論文利用大氣電漿沉積氧化銦鎵鋅作為元件的主動層，並且成功發展出高效能的薄膜電晶體。在X光繞射儀(XRD)分析中可以發現由大氣電漿沉積之氧化銦鎵鋅為非晶態。氧化銦鎵鋅薄膜對可見光的平均穿透率超過80%，並且具有3.78eV的能隙。這些特性使得大氣電漿沉積氧化銦鎵鋅具有應用於透明電路的潛力，以及能減少光漏電對元件的影響。我們利用矽晶片作為元件的基板並成長氧化矽當作絕緣層，隨後在沉積氧化銦鎵鋅薄膜後，對其在不同環境及不同溫度下進行退火處理，探討氧化銦鎵鋅薄膜在不同退火條件下對薄膜品質及元件特性的影響。我們在論文中使用X光繞射儀(XRD)、掃描式電子顯微鏡(SEM)、穿透式電子顯微鏡(TEM)、原子力顯微鏡(AFM)、X射線光電子能譜儀(XPS)，來分析及討論不同退火條件下氧化銦鎵鋅薄膜的表面形貌、缺陷密度、結晶型態等等，並且利用元件的I-V轉換曲線來進行元件特性探討。最後我們欲降低臨界電壓及次臨界擺幅

而使用高介電係數材料取代氧化矽作為元件的絕緣層，氧化銦鎵鋅薄膜在最佳退火條件下及使用氧化鋁作為絕緣層後，發展出開關電流比 1.04×10^{8}、電子遷移率 8.6 cm^2/V-s、臨界電壓 0.75 V、次臨界擺幅 0.28V/decade 的高性能薄膜電晶體。



The effect of thermal annealing on IGZO TFT properties prepared by atmospheric pressure plasma jet

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Abstract

In this paper, we have successfully developed a high performance thin film transistor (TFT) with indium gallium zinc oxide (IGZO) active layer deposited by atmospheric pressure plasma jet (APPJ). IGZO films show amorphous phase in XRD analysis. IGZO films have over 80% transmittance of visible light and band gap energy 3.78eV. Therefore, IGZO films deposited by APPJ are suitable for transparent devices. Wide band gap can release the issue of photo-excited leakage current. We deposited IGZO thin films on silicon wafer which was covered with SiO_2 and studied the effect of thermal annealing on IGZO films quality and properties of TFTs with IGZO as active layer. In this work, we discussed the IGZO films properties including surface morphology, roughness,

structure and crystallinity by analysis equipments including SEM, AFM, XRD, TEM and XPS. We also used Agilent 4156C to analyze IGZO TFTs electrical characteristic. At the final, we substituted high-k material for SiO_2 as gate dielectric for decreasing V_{th} and S.S. And the IGZO TFT with Al_2O_3 as gate dielectric shows excellent performance of μ = 8.6 $cm^2/V\text{-}s$, V_{th} = 0.75 V, SS = 0.28V/dec, I_{on}/I_{off} ratio of 1.04×10^8.

誌 謝

於本人碩士求學期間，我首先要感謝指導老師張國明教授，老師在碩士生涯兩年中不斷給予我人生方向的指引及學業上的諄諄教誨，讓我在作研究或是待人處世上都受益良多，僅此表達最深的謝意。

其次感謝實驗室學長們的熱心指導，尤其是黃菘宏學長，在我的研究上提供了許多寶貴的意見，讓我可以順利的進行自己的實驗研究。另外也要感謝工業技術研究院(ITRI)、國家奈米元件實驗室(NDL)與國立交通大學奈米中心(NFC)提供良好的研究機台和實驗環境，使我可以順利的進行實驗研究。

此外，我要感謝實驗室的同學吳金濘、謝政廷和張柏鈞在半導體元件上的知識交流以及撰寫論文時，提供寶貴意見來幫助我順利完成。另外，學弟吳致緯也在實驗上給予我協助，得以順利完成實驗。

最後，我要特別感謝家人在我碩士求學階段給予我的支持和幫助，女友旻芯和瓜瓜陪我度過在新竹兩年的碩士生活，提供精神上的支持，讓我可以順利的完成碩士學位。

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Chapter 1

Introduction

1.1 Forward

Recently, the display technologies have become an important industry in Taiwan. The products of display technologies include PC monitors，TV screens，notebooks，and cell phones in people daily life. The history of the TFT began with the work of P.K. Weimer at RCA laboratories in 1962. He used thin films of polycrystalline cadmium sulfide (Cds) as the active layer, silicon oxide (SiO_2) and gold (Au) as the insulator and electrodes. Now amorphous silicon (a-Si:H) and polycrystalline Si are used widely as the active layer of thin film transistors (TFT) for the drivers of Active Matrix Liquid-Crystal Display (AMLCD), which integrates TFT-LCD and backlight source module. Recently, the Active Matrix Organic Light Emitting Diode (AMOLED) has been the leading role of display technologies due to the thinner screens and wide angle of view.

But the issue of the material based on a-Si:H as active layer in TFT is low field effect mobility (~$1cm^2 \cdot V^{-1} \cdot S^{-1}$) [1], photo sensitivity (low band gap about 1.7eV) and rather high deposition temperature (~400°C) [2, 3]. Because of the low band gap of a-Si, the photo excited carriers (photo current effect) might make the array of AMLCD and AMOLED out of control in visible region. For the reason, the opaque metals to keep

a-Si based channel blind from visible light are integrated necessarily. This causes lower opening of AMLCD pixels and more complicated device fabrication.

Organic light emitting diodes (OLED) has been investigation and important target on the next generation of display technologies. The OLED of display technology is demonstrated to promising for providing power efficient, lightweight and high brightness performance at reasonable voltage and current levels. Because OLED can be lighted by itself, the AMOLED does not need backlight source module. But we need to solve the problem that driving OLEDs need higher voltage and driving current than LCDs for controlling circuit. However, it seems difficult that the a-Si based material low mobility limited on driving circuit.

1.2 Amorphous oxide semiconductors (AOS)

Amorphous oxide semiconductors (AOS) are the materials of high performance, low temperature fabrication even at room temperature (RT) that be used reasonably in flexible electronics. However AOS materials have unstable carriers that generated from oxygen vacancy. Consequently, the deposition process of oxygen pressure will determine the carrier concentration of AOS. So it is important to design and investigation a suitable material and control the oxygen pressure for both properties of large mobility and stable controllability carrier concentration in particular application.

Due to the intrinsic chemical bonding nature that the mobility of a-Si:H ($\sim 1\,\mathrm{cm^2 \cdot V^{-1} \cdot S^{-1}}$) is much lower than single crystalline Si

($\sim 200\ \mathrm{cm^2 \cdot V^{-1} \cdot S^{-1}}$). The average carrier transportation paths in covalent semiconductors, such as a-Si:H consist of strongly directive sp^3 orbitals. The bond angle alter fluctuation significantly the electronic levels that influence high density of deep tail-states as show in figure 1-1.

By contrast, transparent oxide constituting of heavy post transition metal ions with the $(n-1)d^{10}ns^0$ electron configuration where $n \geq 5$ are the transparent AOS candidates having high mobility comparable to those of the corresponding crystals. The electron pathway in oxide semiconductor is primarily composed of spatially spread ns orbitals with an isotropic shape as show in figure 1-1. The direct overlap among the neighboring ns orbitals is possible. The degree of overlap of the ns orbitals is insusceptible to the distorted metal-oxygen-metal bonding. The feature shows why the Hall mobility of AOS is similar to the corresponding crystalline phase even the thin films deposit at room temperature.

1.3 Transparent oxide semiconductors (TOS)

Currently, transparent oxide semiconductors (TOS) have attracted keen attention on applications of thin film transistors (TFT) for active layer in display, mobile electronics, optoelectronics, and military technologies [5,6]. Among of these TOS, amorphous indium-gallium-oxide (a-IGZO) TFTs [7-13] present promising alternative to a-Si TFTs, poly-Si TFTs and ZnO TFTs. There are many advantageous property of a-IGZO TFTs which high transparency, high field effect mobility, including the capability of large-area and uniform deposition at low temperature, such as room temperature for the

fabrication of flexible displays and computers on various substrates, such as glass, plastic and paper. Therefor the a-IGZO is the ideal material for active layer in TFTs which can achieve the purpose of efficient power consumption, low temperature deposition, high transparency, and well driving ability.

1.4 Motivation

The high filed effect mobility and transparent thin films of a-IGZO can be fabricated at low temperature on several substrates by variety of physical and chemical method, such as DC/ or RF magnetron sputtering [14, 15], pulse laser deposition (PLD) [16], molecular beam epitaxy (MBE) [17], sol gel [18, 19], chemical spray pyrolysis [20-23], ink-jet printing [24, 25], chemical bath, and atmospheric pressure plasma jet (APPJ).

In the above mentioned deposition methods, we determinate the APPJ system to deposit a-IGZO thin films because the deposition way has a lot of merits, such as it could be manufacture in the air ambient, economical, easy-to-handle, large area deposition feasibility and controlled quality [26, 27].

The high quality thin films can be deposited in the atmosphere ambient by APPJ, but can't use the PECVD based on the plasma used methods [28]. And deposit thin films by other plasma CVD processes also in low pressure conditions. The APPJ system is mainly used in high temperature arc plasma, for example, the plasma jet used for diamond synthesis [29] and the inductively coupled plasma (ICP) flash evaporation

process for producing ferrite films formation [30] is possible to generate atmospheric pressure cold glow plasma. The atmospheric pressure cold glow plasma which is used the nitrogen gas as a plasma gas, employed a high frequency power source over one kilohertz, and stetted an insulating between two electrodes [31].

Therefore, the APPJ would be quite advantageous than other plasma enhanced CVD from the viewpoint of process cost, and particularly in the application of thin films deposition on ready prepare glass substrates. Numerous films were fabricates by the APPJ system, such as SiO_x films [32], TiO_x films [33], ZnO films and Transparent Conductive Oxide (TCO). Consequently, we can mix two or more solutions that choose appropriate source material to be the precursor of deposition films for an APPJ system that it would be a convenient process for fabrication a variety of thin films, even though a-IGZO thin films.

In recent years, many researchers have been extensively studied targeting for transparent TFTs for the next display generation. Nowadays, various materials have been investigated as candidates of the channel semiconductors, such as hydrogenated amorphous silicon (a-Si:H) [34-36], polysilicon, organic semiconductor [37-41], metal-oxide semiconductors such as zinc oxide (ZnO) [42-47], and so on. The material of ZnO for channel TFT has attracted much attention with its notable advantages over the other semiconductors including high field effect mobility, wide bend gap of 3.37 eV, high transparency in the visible range, and good thermal stability. But the ZnO films examined are polycrystalline [48] even if formed at room temperature. These channels

have grain boundaries that deteriorate the TFT performance, stability, and uniformity of the TFT characteristics. However the a-IGZO films also has the similar properties to ZnO films and it can be formed amorphous at room temperature that has better stability and uniformity of TFT characteristics than ZnO TFT.

For the indium-gallium-zinc-oxide ternary system, the IGZO films ratio of indium, gallium, and zinc are very important to determinate the carrier concentration and mobility. The carrier concentration of IGZO is primary determined by the incorporation of cations with large ionic valance such as indium and zinc that are effective to control the carrier concentration due to their strong metal-oxygen bonds. Besides the mobility of IGZO is determined by the indium content fraction because only In^{3+} meets the electron configuration criterion $(n-1)d^{10}ns^{0}(n \geq 5)$ of heavy post transition metal cation for ionic AOS among the three cations [49]. In the other hand the gallium ions can effectively suppress the formation of oxygen vacancy and this reduce the carrier concentration in the film owing to the fact that gallium ion forms a stronger chemical bond with oxygen than zinc and indium ions [50]. Figure 1-2 shows the carrier concentration and electron mobility that evaluated by the Hall effect measurement for amorphous thin films deposition by PLD.

The continuous decrease of the thickness of gate oxides used in modern electronics has to confront the limit of material itself. In order to make a breakthrough on what is aforementioned, it is necessary to increase the physical thickness as well as the dielectric constant of the gate dielectrics. Unfortunately, most popular transparent TFT structure

employing SiO_2 as dielectric material that has low dielectric constant (k) resulting in low channel modulation effect. Therefore SiO_2-based structures should require higher driving voltage to achieve the same operating efficiency than the other structures incorporating high-k dielectrics. Moreover, in order to have the equivalent insulation efficiency, SiO_2 dielectric layer should be thicker than high-k materials. However, it has a critical drawback, high charge trap density mainly being concentrated into the interfaces between gate electrode and gate insulator, as well as gate insulator and channel layer [52, 53].

In this dissertation, for the purpose of high mobility, optical transparency, stability, wide band gap, room temperature process, and good uniformity over large area, we choose the IGZO thin film for TFTs active layer. Then, we prepared the precursor solution for IGZO film to blend the molarity ratio by dissolving indium, gallium, and zinc nitrate-based that was deposited by APPJ system. Because of the kind of APPJ does not require a complicated vacuum system which would reduce the cost of processing and enlarge the size limit [54]. Moreover, the deposition process is at low temperature which reducing the thermal damage of substrate and make sure the amorphous state of thin film of IGZO. After the thin film deposition, we discuss the influence of TFTs electric characteristic by different post annealing temperature. In the end, for lower driving voltage, lower leakage current, and higher capacitance we are going to substitute high-k material for SiO_2 in the TFTs of gate dielectric. We explore high-k dielectric materials to find that HfO_2 and Al_2O_3 are two of the most promising materials due to the properties of

high dielectric constant, relatively low leakage current, low synthesis temperature, wide band gap sufficient to yield a positive band offset with respect to IGZO, and high transparency in visible range [55, 56].

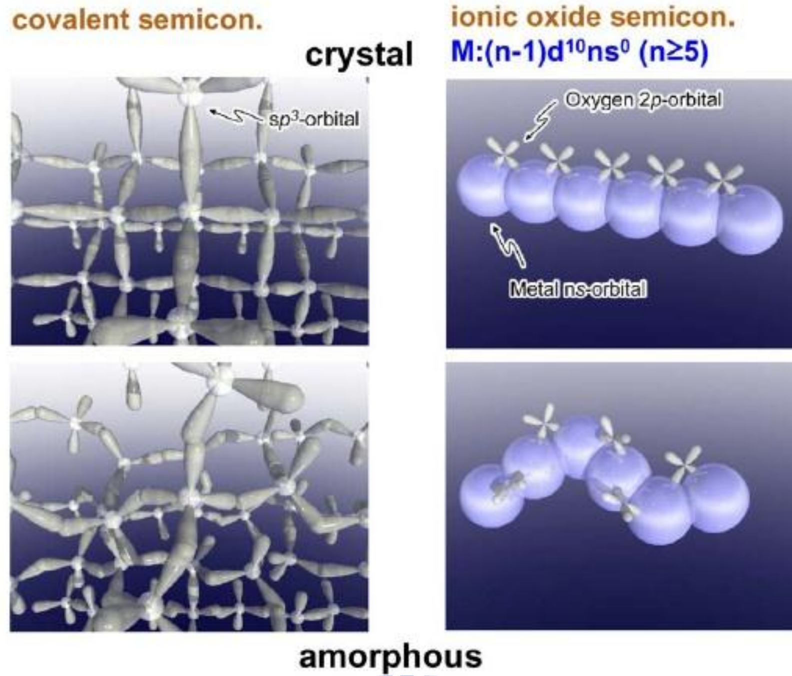


Figure 1-1 Schematic orbital drawing of electron pathway (conduction band bottom) in conventional silicon-base semiconductor and ionic oxide semiconductor [4].

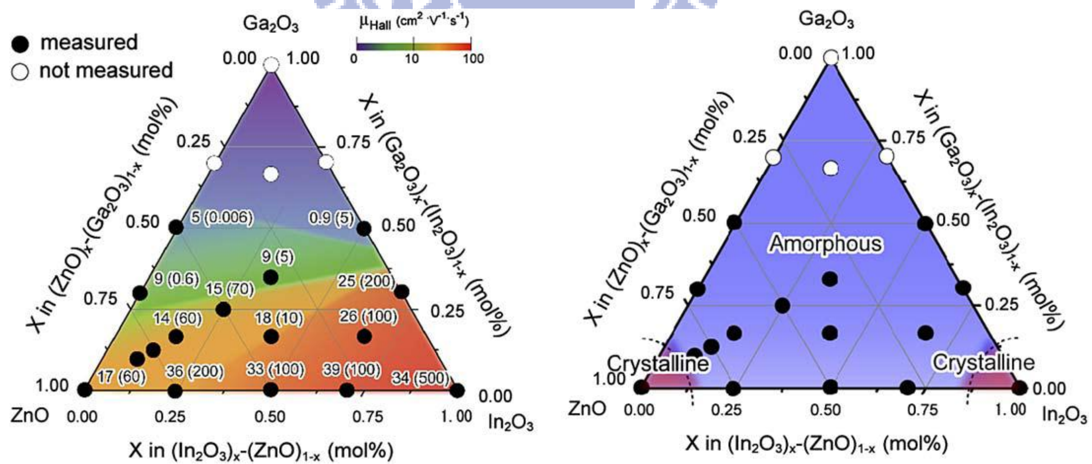


Figure 1-2 Room temperature Hall mobility and carrier concentration as function of chemical composition. Values outside and inside parentheses show Hall mobility in $cm^2 \cdot V^{-1} \cdot S^{-1}$ and carrier concentration in 10^{18} cm^{-3}, respectively [51].

Chapter 2

Literature Reviews

2.1 Reviews of thin film transistors applications

2.1.1 Thin film transistors

The structure and operation of thin film transistors (TFT) are similar to metal-oxide-semiconductor field-effect transistors (MOSFETs) which are widely used in single crystal silicon applications such as memory cells and microprocessors. TFTs are three terminal devices like the MOSFETs with a source terminal for injecting carriers, a drain terminal for extracting carriers, and a gate terminal for modulating the conductivity of channel. They are fabricated by subsequent deposition of conducting, insulating, and semiconducting thin films onto an insulating substrate. There have many advantages to use an insulating substrate, such as glass or plastic compared to using a semiconductor substrate. First is the substantially lower material cost and second is the insulating material inherently eliminates problems such as parasitic capacitances and latch-up which are either unavoidable or require additional isolation when using a semiconducting substrate [57]. Finally, since the semiconducting layer where the conducting channel is induced during device operation, is deposited onto rather than built into the substrate, there is more freedom in the way in which the device can be structured.

TFTs can be made using a wide variety of semiconductor materials

which common material is silicon. The characteristics of silicon based TFT depend on the crystalline state. The semiconductor layer can be either amorphous silicon, microcrystalline silicon, or it can be annealed into polysilicon. There are some materials have been used as semiconductors in TFTs include compound semiconductors such as cadmium selenide, metal oxides such as zinc oxide, and organic materials such as pentacene (referred to as an Organic TFT or OTFT), TFTs have also been made using AOS such as a-IGZO.

There are two main structures of TFTs which are shown in figure 2-1. The structure A and B are respectively top gate and bottom gate structure. We determine one of two structures in TFT fabrication by practical requirements and issues. The structure A of top gate has been used in normal field effect transistors for many years but it does not adapt to majority of TFTs fabrications.

The issue is that we must consider the process of dielectric layer deposited would influence semiconductor active layer by thermal treatment or other damage condition. Defects and interface charges would appear in active layer and the interface between dielectric layer and active layer. Therefore, the top gate structure of TFTs electrical properties become worse by defects and interface charges.

Hence, the most of advanced TFTs fabrication adopt bottom gate structure for better quality of semiconductor active layer than top gate structure because the active layer is deposited after gate dielectric layer. To use the bottom gate structure can avoid thermal treatment injuring active layer and also can fabricate devices on silicon substrate as gate

electrodes. Then the gate leakage would deal light influence to devices when we use thermal oxide to be gate insulator. But a problem of bottom gate structure we need to solve that is the stability of devices after active layer directly exposed to the air a long time. The reliability of devices became worse because the mists and particles would invade active layer. In this way, there is an effective method to solve this problem that is depositing preservation layer on active layer such as silicon nitride. Then, it can avoid mists and particles invading active layer. But the method would increase the prime cost and influence the active layer by deposition of preservation layer.

2.1.2 TFT as OLED drivers

Passive matrix organic light emitting diode (PMOLED) is a display technology as shown in figure 2-2 (a) [58-59]. The OLED present a specific type of display technology which does not require backlight. An OLED is driven by one data line and one scan line at one time order. Only one scan line would be grounded and other scan lines connect to broken circuit at one time order. The below scan line would be grounded at next time order. This is ordered from first scan line to last scan line and repeat time and again. It would be driven by data lines when one scan line became grounding and the OLEDs connected as shown in figure 2-2 (b) [60].

The main mechanism of PMOLED is persistence of vision to form images to our eyes because OLEDs keep radiating only during one time order. We need to drive OLEDs by large current and high voltage to

make them radiating more light for keeping ideal persistence of vision when monitors size became larger. But this movement would make OLEDs having short lifetime and large power consumption. So it is necessary to find out a method to keep OLEDs radiating before scan line connected to grounding and accepting data line at next time.

Active-matrix OLED (Active-matrix organic light-emitting diode) is a display technology for use in mobile devices and televisions. And Active-Matrix refers to the technology behind the addressing of pixels. AMOLED technology continues to make progress toward low-power, low-cost, and large size (e.g. 40-inch) for applications such as TV. An active-matrix OLED (AMOLED) display consists of OLED pixels that have been deposited or integrated onto a thin film transistor (TFT) array to form a matrix of pixels that generate light upon electrical activation as shown in figure 2-3 (a), which functions as a series of switches to control the current flowing to each of the pixels as shown in figure 2-3 (b).

Typically, this continuous current flow is controlled by at least two TFTs at each pixel, one to start and stop the charging of a storage capacitor and the second to provide a voltage source at the level needed to create a constant current to the pixel and eliminating need for the very high currents required for passive OLED matrix operation. Active-matrix OLED displays provide higher refresh rate than their passive-matrix OLED counterparts and they consume significantly less power. Because of this advantage, active-matrix OLEDs well suited for portable electronics, where power consumption is critical to battery life. The amount of power the display consumes varies significantly depending on

the color and brightness shown.

2.2 Thin-Film Transistor Operation

It is helpful to first examine the metal-insulator-semiconductor stack in three different conditions: zero, negative, and positive applied gate biases for understand the operation of a TFT. Under these three conditions, figure 2-4 illustrates the band bending in an unipolar n-type semiconductor and the relative shift of the metal Fermi level compared to the semiconductor Fermi level. The system is in equilibrium or a flat-band state and ideally there is no impact on the carrier concentration at the semiconductor-insulator interface with no applied bias, as depicted in figure 2-4 (a). These delocalized majority carrier electrons in the semiconductor are repelled and there is a depletion of majority carriers at the semiconductor-insulator interface when a negative bias is applied to the gate, as depicted by the positive curvature of bands in figure 2-4 (b). However, these delocalized electrons are attracted towards the interface and this creates an accumulation layer of free majority carriers when a positive bias is applied to the gate as shown in figure 2-4 (c). It is accumulation layer that is referred to as the induced channel in a TFT and it is what allows for conduction between source and drain terminals.

So as to induce a channel, and the source and drain terminals are now also considered if the gate is positively biased, current flow along the channel can be achieved by applying a positive voltage to the drain to extract electrons in the channel while keeping the source grounded. According to the square-law model of TFT behavior [61], the drain

current I_D is in the pre-saturation regime when the applied drain voltage V_{DS} is less than the pinch-off voltage (V_{DSAT}) and is described as

$$I_D = \frac{W}{L}\mu C_G\left[(V_{GS} - V_{ON})V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad (2\text{-}1)$$

Where C_G is the gate capacitance, the turn-on voltage V_{ON} is defined as the smallest applied gate voltage that causes a non-negligible increase in drain current for a given drain voltage, W and L are the TFT's width and length, and μ is the mobility.

The drain current ideally becomes independent of the drain voltage as the drain voltage increases and exceeds $V_{DSAT} \equiv V_{GS} - V_{ON}$, and is said to be in saturation regime where I_D is given by

$$I_D = \frac{1}{2}\frac{W}{L}\mu C_G(V_{GS} - V_{ON})^2 \qquad (2\text{-}2)$$

The TFT is said to be operating in the cutoff state if $V_{GC} < V_{ON}$ or if V_{DS} is negative and according to the simplistic square-law model, it is assumed that $I_D = 0$. These three equations for I_D and V_{DSAT} constitute the square-law model and allow the drain current to be modeled for any given combination of drain and gate voltages.

Thin film transistors are also classified by sign of V_{ON}. There are no current flows when the gate voltage bias is zero applied, if V_{ON} is positive for an n-channel TFT (i.e. the device is normally off) and the device is referred to as an enhancement mode device. There is a sufficiently high carrier concentration in the channel that even with no applied bias to the

gate if V_{ON} is negative, conduction between the source and drain can occur (i.e. the device is normally on). In this case, negative gate voltage is required to turn the TFT off and the transistor is referred to as a depletion mode device. Enhancement mode TFTs are generally preferred in circuit applications because of their normally off nature and lower power consumption, but depletion mode devices can be useful in certain circuit applications, e.g. as active loads.

2.3 Deposition methods of IGZO films

The methods of deposition IGZO films have distinct classification. In this paper, we categorize them in physical and chemical type that representing the source of films is solid and liquid. Following the exposition will discuss them in detail.

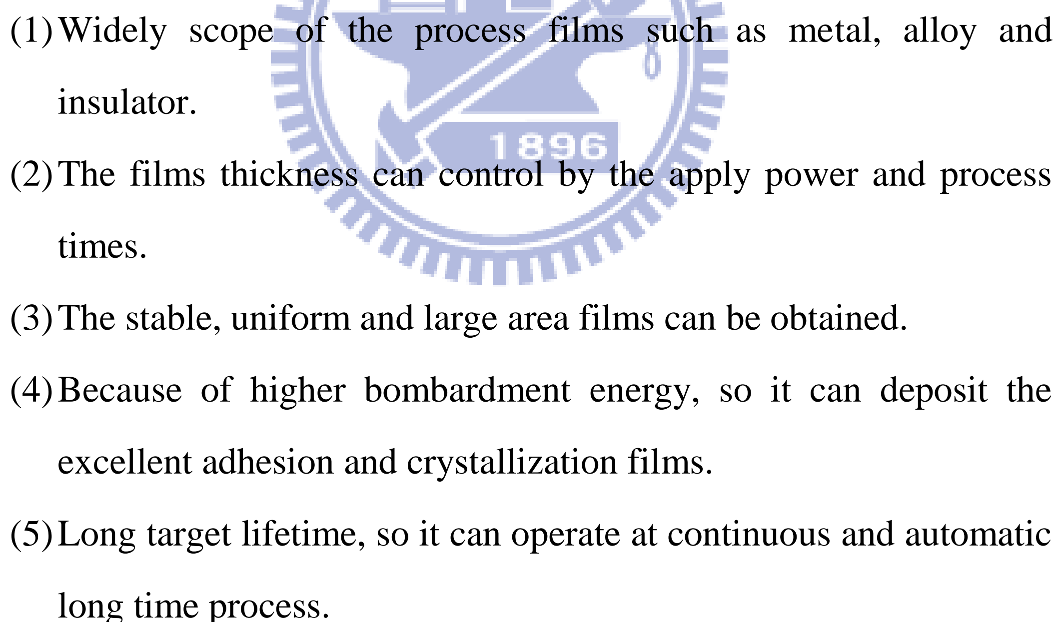
2.3.1 Magnetron sputtering

The sputtering method is working in the glow discharging region which has higher energy and density of electrons. To put the substrate at anode and set the targets at cathode in the argon ambient, then the cations which accelerated by the electrical field bombard the target. At this time, the targets of atoms are leaved out and going to the substrate to form the IGZO films. The reason of the cations which is driving to target is the potential of plasma always higher than chamber, target and substrate. Moreover, target connect with cathode will increase the potential difference between plasma and target. If setting a magnet under the target, there was an external magnetic field to increase the plasma density, so the

cations which bombard the target will increase simultaneously. It is difficult to discharge with the DC power when the low conductivity materials or insulators were to be the deposition substrate. So, there have to use the RF power which the frequency needs to reach the grade of megahertz (usually 13.56MHz) to be the power supply. Using the self-bias phenomenon in the RF discharge, it can make the target potential will always in negative values to ensure the bombardment will almost continuously which is same capability as the DC discharge.

So far, the sputtering technique is one of the most common in deposition the IGZO films, including electrodes of flat display and energy efficiency windows. The generally properties of sputtering are described following:

(1) Widely scope of the process films such as metal, alloy and insulator.



(2) The films thickness can control by the apply power and process times.

(3) The stable, uniform and large area films can be obtained.

(4) Because of higher bombardment energy, so it can deposit the excellent adhesion and crystallization films.

(5) Long target lifetime, so it can operate at continuous and automatic long time process.

There is another magnetron sputtering method which getting high density plasma by RF-DC couple manner. In general RF magnetron sputtering, the self-bias of the target can change with the RF frequency and power, and it controls the ion energy of bombarding to the target.

When the RF frequency increased, the self-bias of the target will decreased, the RF power increased, the self-bias of the target will also increase. However, in the RF-DC couple magnetron sputtering system, the RF power is mainly to generate high density plasma, and the DC power is to adjust the electric potential of the target, by doing that is easy to control the deposition conditions.

2.3.2 Pulsed laser deposition

Pulsed laser deposition (PLD) is a technology where a high energy density focusing pulsed laser beam is struck a target of the material that is to be deposited. The target is vaporized which deposits it as a thin film on substrate. This method can be applied on many materials, so it can deposit lots of thin films. But the growth rate of PLD is extremely slow; therefore, it is not a mass production technology. This process can occur in ultra-high vacuum or in the presence of a ambient gas, such as oxygen which is commonly used when depositing oxide to fully oxygenate the deposited films.

The PLD basic machinery is simple relative to many other deposition techniques, the physical phenomena between laser and target interaction and the film growth are quite complex. The absorption energy is converted to electronic excitation and thermal energy resulting in evaporation and plasma formation when the laser pulse is absorbed by the target. The ejected varieties full of the surrounding vacuum including atoms, molecules, electrons, ions, clusters, particulates and molten globules, before depositing on the typically hot substrate.

There are a number of advantages of PLD over other thin film deposition methods, these include:

(1) The most advantage is that it is versatile. This method can be applied on many thin films including metal, oxides, semiconductors and even polymer. It is unlike Molecular beam epitaxy (MBE) and Chemical vapor deposition (CVD), where different source of precursors are required for each element of the desired compound.

(2) It can be maintained the target composition in the deposited thin films. Because of the very short duration and high energy of the laser pulse, target material immediately toward the substrate, every component of the phase has an analogous deposition rate, so the thin films composition is almost unchanged.

(3) The energy associated with the high ionic content in laser ablation plumes and high particle velocities appear to aid crystal growth and lower the substrate temperature required for epitaxy.

(4) PLD is clean, low cost and capable of producing simply by switching several different targets.

There are also a heaps of advantages of PLD, these include:

(1) PLD brings difficulty to controlling thickness uniformity across the sample, but this problem can be overcome, to some extent, by scanning the laser beam on a larger size target.

(2) The plume of ablated material is highly forward directed, which causes poor conformal step coverage. It also makes thickness monitoring difficult.

(3) There is an intrinsic splashing associated with laser ablation itself, which produces droplets or big particles of the target material on the substrate surface. This is particularly serious as it will result in device failure from an industrial perspective.

2.3.3 Spray pyrolysis

Deposition IGZO thin films by spray pyrolysis has been used for a long time. The deposition material can use solid or liquid source, according to the previous statement of the definition of the deposition method, it may be categorized to the physical type, but it is similar to the CVD method, so we still categorizing it in chemical manner.

Spray pyrolysis is the most in common uses in the pyrolysis manners. The precursor solution is pulverized as affine mist via a spray nozzle and a carrier gas at high pressure in spray pyrolysis. The so produced mist condenses on a preheated substrate, and is instantly pyrolysed (spray pyrolysis). The process can be conducted in one or more pulses to obtain uniform films. Spray pyrolysis is suitable for substrate with complex geometry, and can be used for a variety of oxide materials. Although the first impression of spray pyrolysis is simple to do, but is concerns at least seven parameters, including heater temperature, carrier gas flow rate, gap distance, solution drop size, solution component, solution flow rate and substrate velocity through the heater.

There is different reaction with increasing the substrate temperature when the solution drops leave from nozzle to the substrate. From figure 2-7, in process A, the solution drop sprinkled on the substrate, vaporizes,

then leaves a dry precipitate in which decomposition occurs; in process B, the solvent evaporates before the solution drop arrives at the surface and the precipitate bombards upon the surface where decomposition occurs; in process C, the solvent vaporizes as the solution drop accesses the substrate, then the solid melts and vaporizes, its vapor diffuses to the substrate to undergo a heterogeneous reaction there; in process D, at the hugest temperatures, the metallic compound vaporizes before it arrives the substrate and the chemical reaction takes place in the vapor phase.

Apparently, we hope not to happen to the process A and D, because it will cause rough and viscosity thin films. So, select the appropriate substrate temperature and make the uniform and equal size of droplet will help the reaction perfectly.

The advantages of spray pyrolysis are summarized below:

(1) The spray pyrolysis can be easy and cheap.

(2) Substrate with complex geometries can be coated.

(3) Leads to uniform and high quality coatings.

(4) Low crystallization temperatures.

(5) Porosity can be easily tailored.

2.3.4 Sol gel coating

The sol-gel coating method is a chemical solution deposition in atmospheric pressure and a wet-chemical technique widely used in the fields of materials science and ceramic engineering. Such methods are used primarily for the fabrication of materials (typically a metal oxide) starting from a chemical solution which acts as the precursor for an

integrated network of either discrete particles or network polymers. Typical precursors are metal alkoxides and metal chlorides, which undergo various forms of hydrolysis and poly-condensation reactions.

In the chemical procedure, the sol (or solution) gradually evolves towards the formation of a gel-like diphasic system containing both a liquid phase and solid phase whose morphologies range from discrete particles to continuous polymer networks. In the case of the colloid, the volume fraction of particles (or particle density) may be so low that a significant amount of fluid may need to be removed initially for the gel-like properties to be recognized. This can be accomplished in any number of ways. The simplest method is to allow time for sedimentation to occur, and then pour off the remaining liquid. Centrifugation can also be used to accelerate the process of phase separation.

Removal of the remaining liquid (solvent) phase requires a drying process, which is typically accompanied by a significant amount of shrinkage and densification. The rate which the solvent can be removed is ultimately determined by the distribution of porosity in the gel. The ultimate microstructure of the final component will clearly be strongly influenced by changes imposed upon the structural template during this phase of processing.

Afterwards, it will be necessary that thermal treatment or firing process in order to favor further poly-condensation and enhance mechanical properties and structural stability via final sintering, densification and grain growth. One obvious advantage of using this method as compared to more traditional processing technology is to

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achieve densification at a much lower temperature.

The precursor sol can be cast into a suitable container with the desired shape or used to synthesize powders to deposit on a substrate to form a film. The sol-gel approach is a low-cost and low-temperature technique that allows the control of the chemical composition of fine products. Even small quantities of dopants, such as organic dyes and rare earth elements, can be introduced in the sol and end up uniformly dispersed in the final product. It can be used in ceramics processing and manufacturing as an investment casting material, or as a means of producing very thin films of metal oxides for various purposes.

2.3.5 Dip coating

Dip coating is a conventional method of deposition thin films for research purpose. Uniform films can be applied onto planar substrate. Spin coating is used more often for industrial processes. The process of dip coating is putted the substrate in the deposition solution first, and then pull up the substrate in regular speed, after that the successful thin film will obtained by drying and annealing. This way of deposition thin film is one of the most common used in sol-gel method.

There are many properties of dip coating manner:

(1) It can be deposited on the irregular surface or double-faced substrate.

(2) Few nanometers of thin films can be acquired.

(3) Simple operation, but usually unstable.

(4) Unfit to high viscosity fluid.

(5) The edge of substrate will gathered deposition solution to cause non-uniform films.

The dip coating process can be separated into five procedures:

(1) The substrate is immersed in the solution of the coating material at a constant speed.

(2) The substrate has remained inside the solution for a while and is started to been pulled up.

(3) The thin layer deposits itself on the substrate while it is pulled up. The withdrawing is carried out at a constant speed to avoid any vibration. The speed plays an important role to determine the thickness of the coating layer.

(4) Excess fluid will drain from the substrate surface.

(5) The solvent of the fluid will evaporate when forming the thin film. Evaporation starts already during the deposition and drainage steps for volatile solvents, such as alcohols.

2.4 Atmospheric pressure plasma system

2.4.1 Corona discharge

A corona is a process by which a current develops between two high-potential electrodes in air, by ionizing that fluid to create a plasma around one electrode, and by using the ions generated in plasma processes as the charge carriers to the other electrode.

It usually involves two asymmetric electrodes in corona discharge, one highly curved such as the tip of a needle or a narrow wire, and

another one of low curvature such as a plate or the ground. For the generation of the plasma, the high curvature assures a high potential gradient around one electrode.

Coronas can be positive or negative. It is calculated by the polarity of the voltage on the high curvature electrode. It will have a positive corona, if the curved electrode is positive associated to the flat electrode, and vice versa. The physics of positive and negative coronas are obviously different. This asymmetry structure is a result of the great difference in mass between electrons and positively charged ions, and so only the electron having the ability to undergo a significant degree of ionizing inelastic collision at common temperature and pressures.

2.4.2 Dielectric barrier discharge (DBD)

Dielectric barrier discharges involve a specific class of high voltage, ac, gaseous discharges that typically operate in the near atmospheric pressure range. Their defining feature is the presence of dielectric layers that make it impossible for charges generated in the gas to reach the conducting electrode surfaces. The voltage applied across the gas exceeds that required for breakdown with each half cycle of the driving oscillate, and the formation of narrow discharge filaments initiates the conduction of electrons toward the more positive electrode. The voltage drop across the filament is reduced until it falls below the discharge sustaining level as charge accumulates on the dielectric layer at the end of each filament, so the discharge is quenched. The low charge mobility on the dielectric not only contributes to this self-arresting of filaments but also limits the

lateral region over which the gap voltage is diminished, thereby allowing parallel filaments to form in close proximity to one another. Thus, the entire gas filled space between parallel electrodes can become, on average, uniformly covered by transient discharge filaments, each roughly 0.1mm in diameter and lasting only about 10ns.

The DBD's has provided the basis for a broad range of applications and fundamental studies, because of the unique combination of non-equilibrium and quasi-continuous behavior. It has generated interest in optimizing conditions for specific chemical reactions in industrial ozone reactors. To this end, experimental DBD studies have explored different gas mixtures, electrical characteristics, and geometries. The related work has focused on maximizing the ultraviolet radiation from excimer molecules produced in DBD's. Several researchers have designed single filament dynamics in order to account for the many reactions including electrons, ions, neutral atoms, and photons. These efforts have been moderately successful in explaining and predicting the chemical and radiative properties of different DBD systems. On another research effort, it has been seen that the transverse spatial distribution of discharge filaments in 2D, parallel plate DBD's can take the form of stable, large scale patterns reminiscent of those associated with magnetic domains. These patterns have been modeled with some success using methods that apply generally to pattern formation in nonlinear dynamical systems. Thus, the dynamical interactions between filaments, as well as the chemical and electronic interactions within filaments have proven interesting.

2.4.3 Atmospheric pressure plasma jet

Atmospheric pressure plasma jet is meaning that operating at atmospheric pressure and it is non-thermal glow discharge plasma system. The non-thermal plasma generates highly reactive ions, electrons and free radicals. The reactive species are directed onto a surface where the desired chemistry occurs. However the overall gas temperature remains quite cold, but the electrons are quite hot, typically 50-300°C.

2.4.4 Arc plasma

The operation of arc plasma is similar to an arc-welding machine, where an electrical arc is struck between two electrodes. The high energy of arc creates high temperatures ranging from 3000°C to 7000°C. The plasma is highly ionized gas which is enclosed in a chamber. The waste material is fed into the chamber and the intense heat of the plasma break down organic molecules into their elemental atoms. In the strict control of the process, these atoms recombine into harmless gases, such as carbon dioxide. Solids such as glass and metals are melted to form materials, similar to hardened lava, in which toxic metals are encapsulated. There is no burning or incineration and no formation of ash with plasma arc technology. There are two main types of plasma arc processes: plasma arc melter and plasma torch.

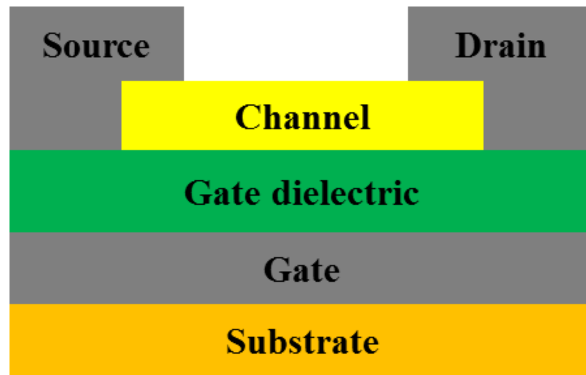
Plasma arc melters have very high destruction efficiency. They are very robust; they can treat any waste with minimal or no pretreatment; and they produce a stable waste form. The arc melter uses carbon electrodes to strike an arc in a bath of molten slag. The consumable

carbon electrodes are continuously inserted into the chamber, eliminating the need to shut down for electrode replacement or maintenance. The high temperatures produced by the arc convert the organic waste into light organics and primary elements.

Combustible gas is cleaned in the off-gas system and oxidized to CO_2 and H_2O in ceramic bed oxidizers. Due to the use of electrical heating in the absence of free oxygen, the potential for air pollution is low. The inorganic portion of the waste is retained in a stable, leach-resistant slag.

In plasma torch systems, an arc is struck between a copper electrode and either a bath of molten slag or another electrode of opposite polarity. Plasma torch systems have very high destruction efficiency with plasma arc systems; they are very robust; and they can treat any waste or medium with minimal or no pre-treatment. The inorganic portion of the waste is retained in a stable, leach-resistant slag. The air pollution control system is larger than for the plasma arc system, due to the need to stabilize torch gas.

A



B

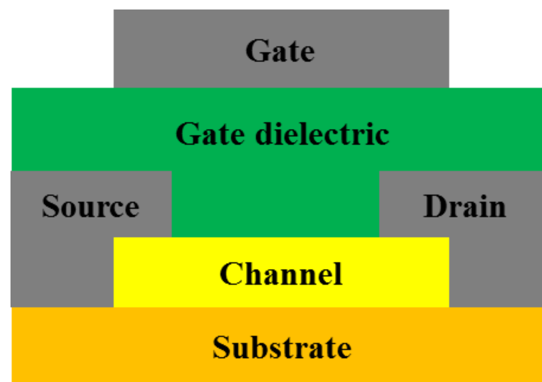
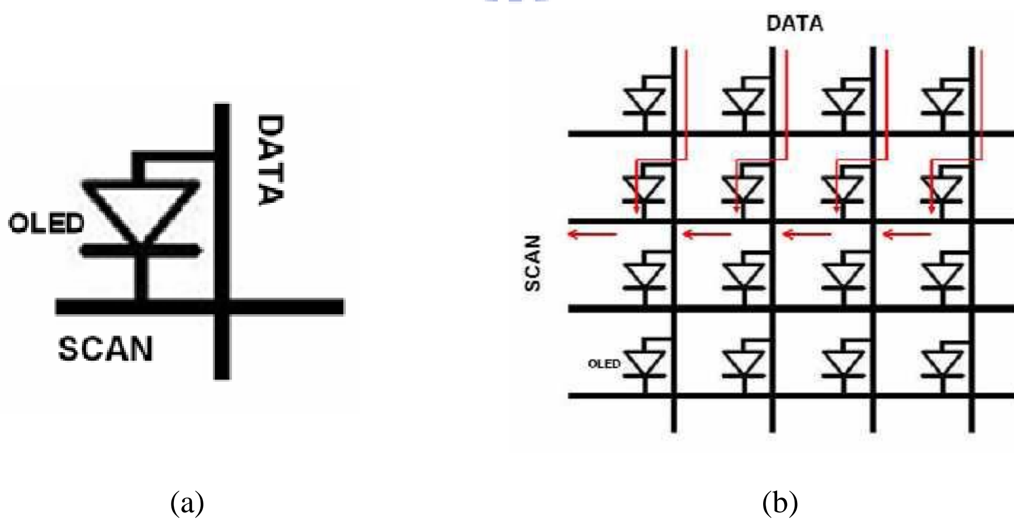
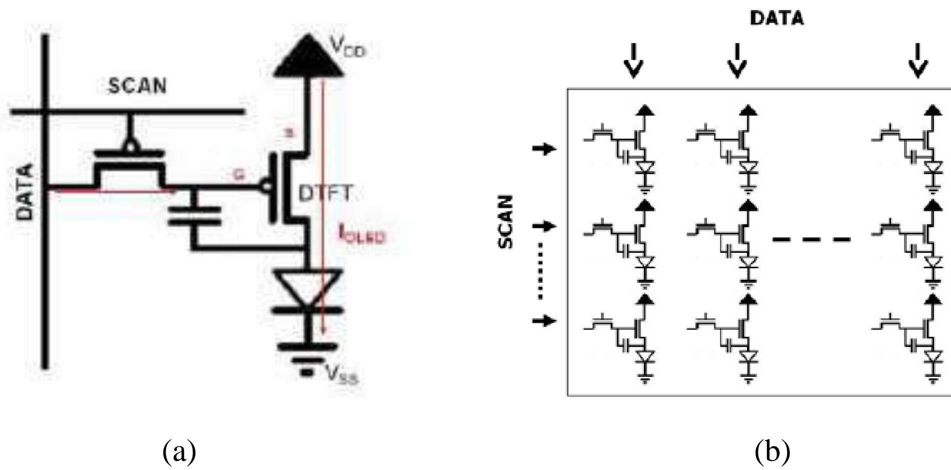


Figure 2-1 (a) Top Gate Structure (b) Bottom Gate Structure



(a) (b)

Figure 2-2 (a) PMOLED (b) PMOLED Control Circuit



(a) (b)

Figure 2-3 (a) AMOLED (b) AMOLED Control Circuit

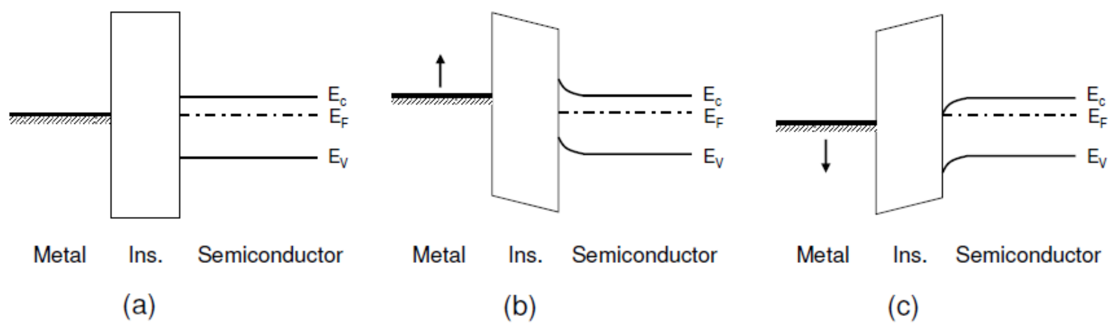


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Figure 2-4. Energy band diagrams for a metal-insulator-semiconductor capacitor, assuming a unipolar n-type semiconductor under three gate bias conditions: (a) no bias, (b) negative bias, and (c) positive bias.

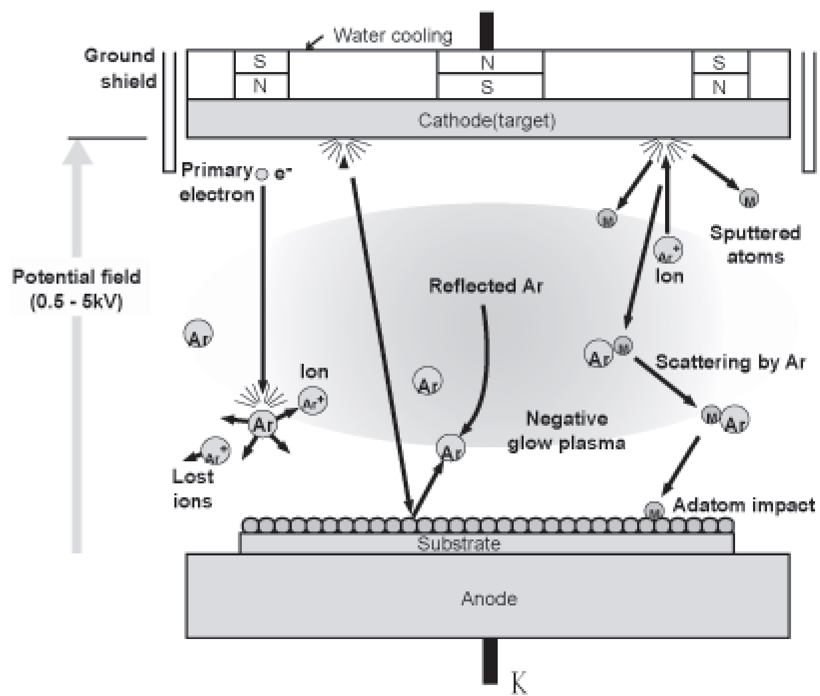


Figure 2-5 Schematic illustration of magnetron sputtering [62].

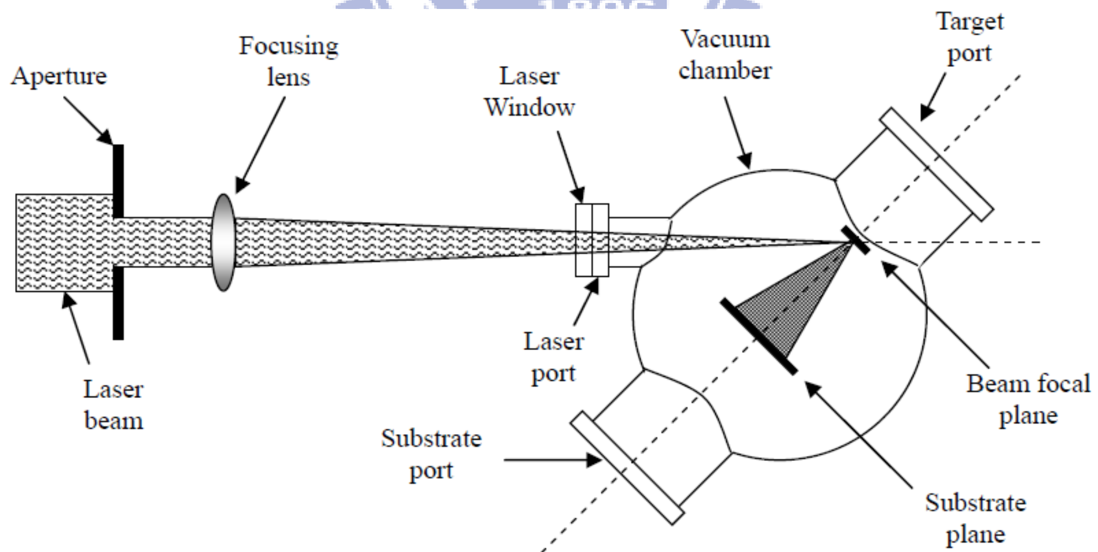


Figure 2-6 Schematic illustration of a Pulsed laser deposition system [63].

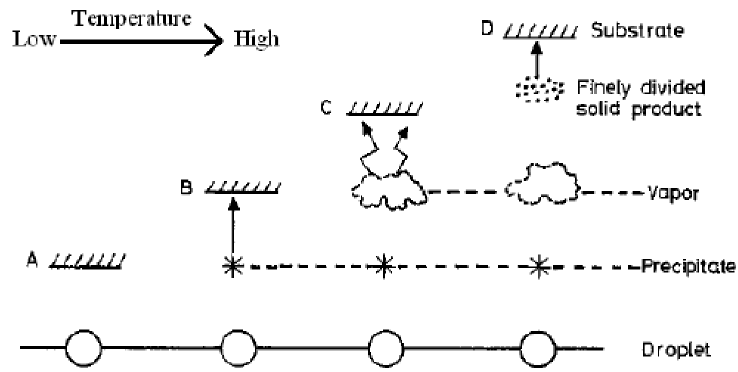


Figure 2-7 Description of the deposition process with raising the substrate temperature [64].

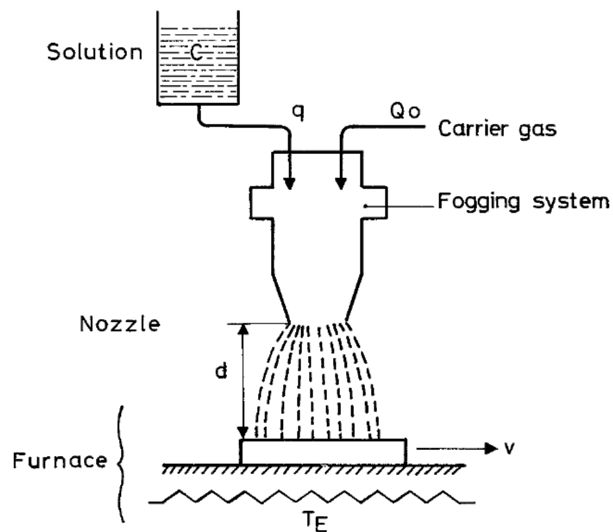


Figure 2-8 Schematic illustration of equipment for spray pyrolysis deposition [64].

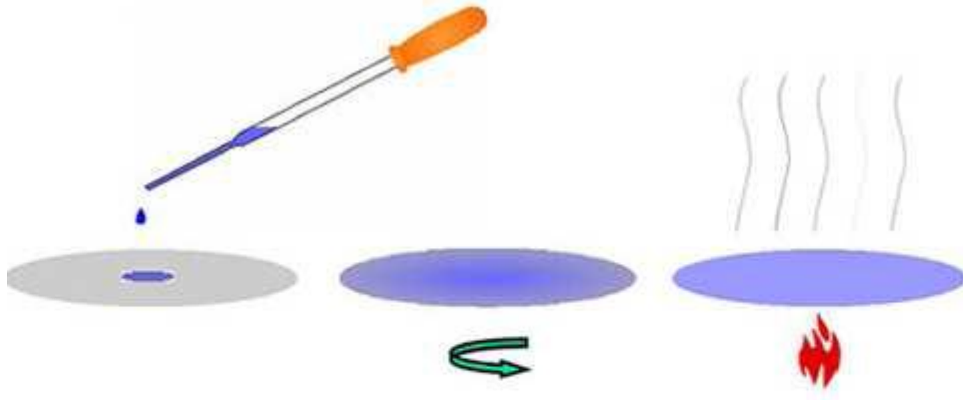


Figure 2-9 Sol-gel process

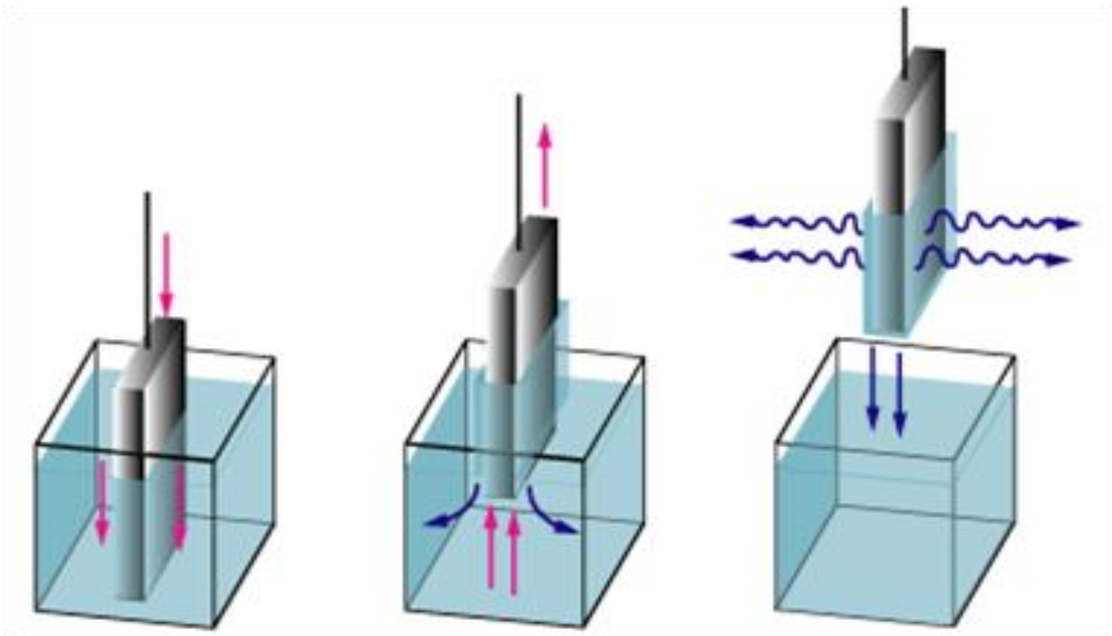


Figure 2-10 Steps of the dip coating process: dipping of the substrate into the coating solution, wet layer formation by withdrawing the substrate and gelation of the layer by solvent evaporation [65].

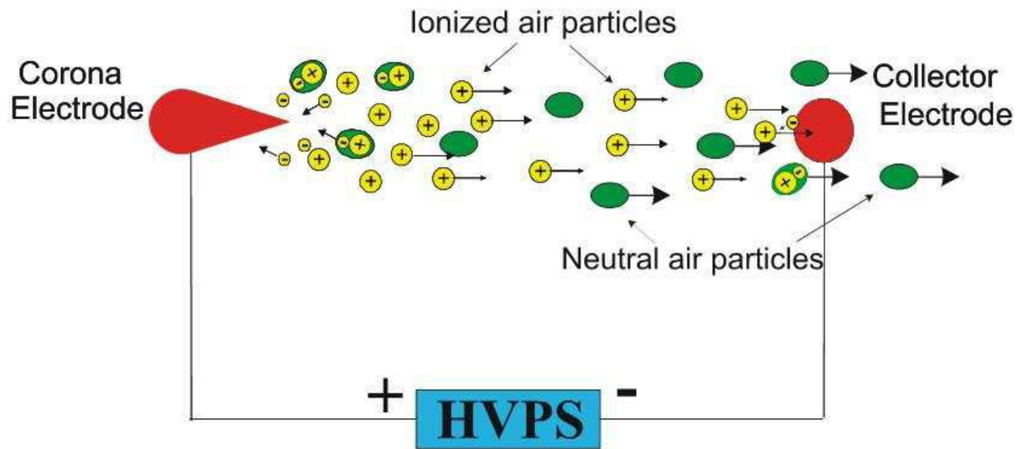


Figure 2-11 Schematic the principle of corona discharge [66].

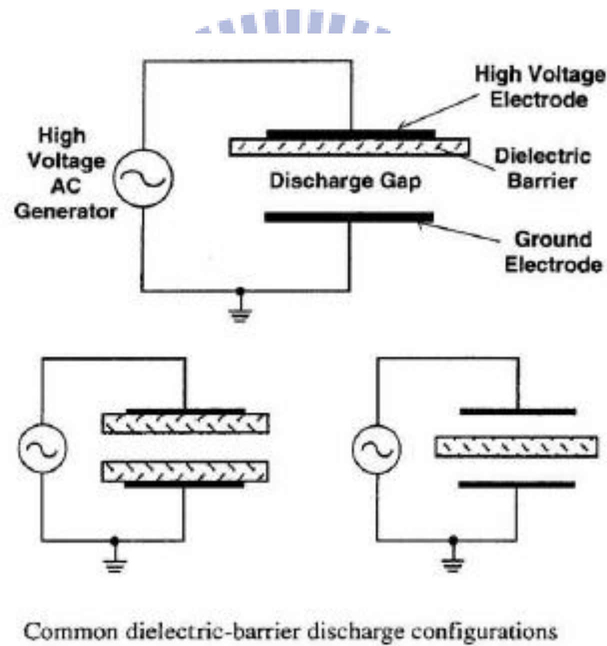


Figure 2-12 Schematic illustration of the DBD configurations [67].

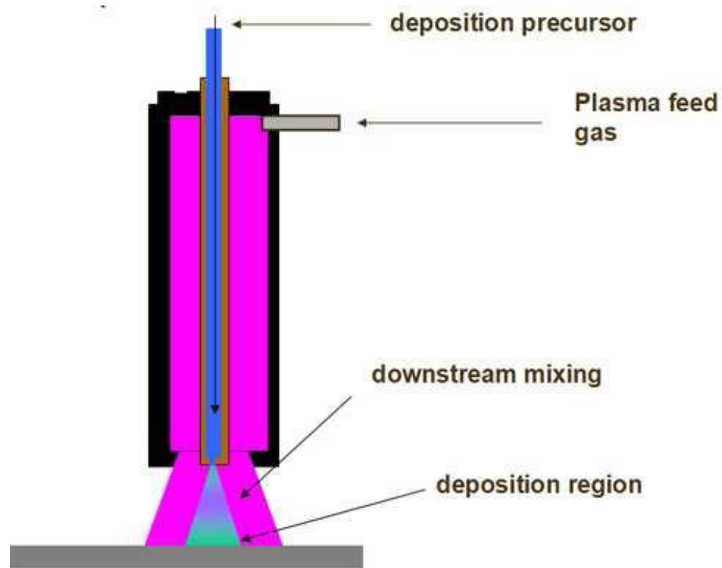


Figure 2-13 Schematic illustration of the AP plasma jet structures [68].

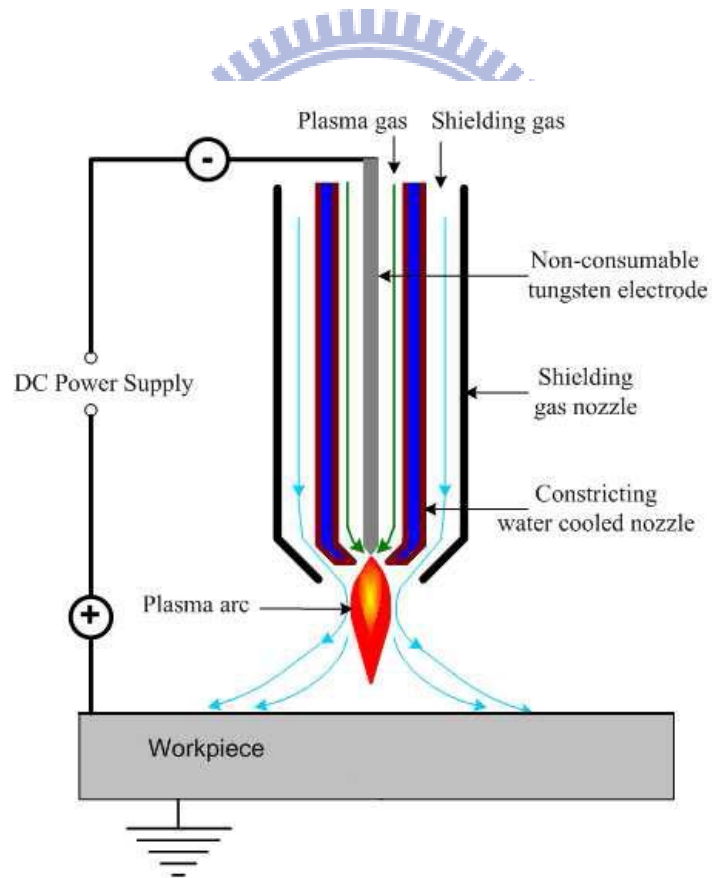


Figure 2-14 Schematic illustration of the arc plasma [69].

Table 2-1 Density of charge species in the plasma discharge [70]

Source	Plasma density (cm^{-3})
Low pressure discharge	10^{8}-10^{13}
Arc and plasma torch	10^{16}-10^{19}
Corona discharge	10^{9}-10^{13}
Dielectric barrier discharge	10^{12}-10^{15}
Capacitive discharge	10^{11}-10^{12}

Chapter 3

Experiments

3.1 Experimental Procedures

The experimental procedures listed below:

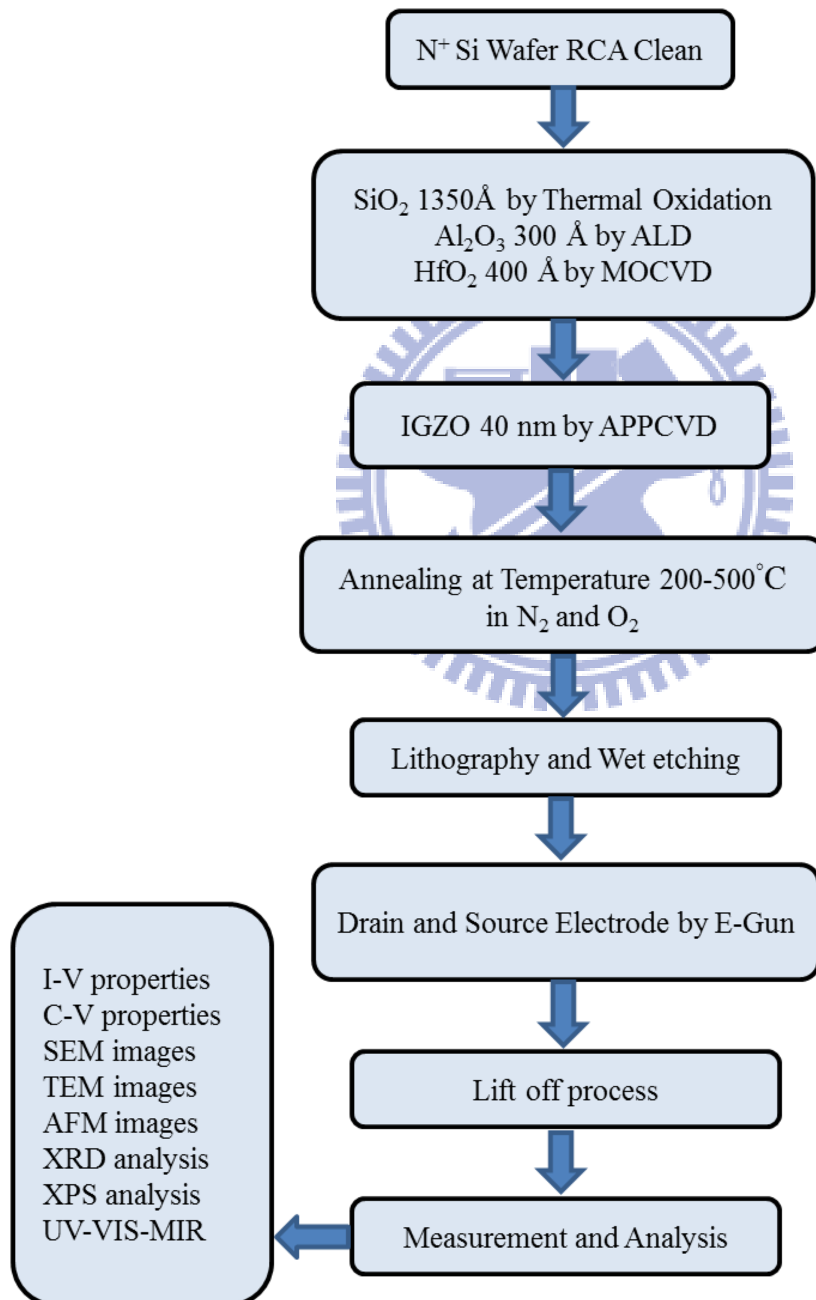


Figure 3-1 Schematic illustration of experimental procedures.

3.2 Experimental process step

3.2.1 The structure and gate dielectric of TFTs fabrication

In the Literature Reviews, the fabrication and properties of bottom gate type thin film transistors using IGZO film as active layers will be described. We use the bottom gate structure for TFTs fabrication on N^+-type silicon wafer as substrate. When using IGZO thin film as active channel material of TFT, usually adopt bottom gate structure for better quality of semiconductor active layer than top gate structure. Because of the active layer is deposited after gate dielectric layer. It will be avoided the plasma bombarding or thermal treatment damaging active layer when deposited gate dielectric layer. The silicon wafer be used as substrate and gate electrode of the TFTs fabrication, and chose N^+-type silicon wafer for lower resistance and bias voltage of gate electrode than N-type silicon wafer.

After RCA clean procedure, we choose three kinds of material for the gate insulator on silicon wafer. We describe it following: First we use silicon dioxide (SiO_2) as the gate insulator because it compatible with silicon wafer. The SiO_2 deposited by thermal oxidation in furnace setting the temperature at 1050°C with 80 minutes. The thickness of SiO_2 is 1350Å , and the slightly thick thickness can avoid the gate leakage current to influence device I-V properties. The other materials are Al_2O_3 and HfO_2 that have higher dielectric constant (k) than silicon dioxide (~3.9). In order to have the equivalent insulation efficiency, SiO_2 dielectric layer should be thicker than high-k materials. Therefore, we replace SiO_2 with the high-k materials which are Al_2O_3 (~9) and HfO_2 (~25) and we can

reduce the driving voltage to achieve the same operating efficiency compared with SiO_2-based structures. In addition, Al_2O_3 and HfO_2 have a large band gap (~8.8eV and ~5.68eV) sufficient to yield a positive band offset with respect to IZGO. So we respectively deposited Al_2O_3 300Å on silicon wafer by Atomic Layer Deposition (ALD) and HfO_2 400Å by Metal-organic Chemical Vapor Deposition (MOCVD).

3.2.2 IGZO thin film deposited by APPJ

First, the precursor solution for IGZO film was prepared by dissolving 0.067M of zinc nitrate hexahydrate [$Zn(NO_3)_2 \cdot 6H_2O$], 0.067M indium nitrate hydrate [$In(NO_3)_3 \cdot xH_2O$] and 0.067M gallium nitrate hydrate [$Ga(NO_3)_3 \cdot xH_2O$] in distilled water. These precursors were mixed at an atomic ratio of In:Ga:Zn = 1:1:1.

According to our group had been study of APPJ system, we could set a suitable deposition condition including gap distance, substrate temperature, carrier gas flow rate, main gas flow rate, and nozzle speed in APPJ system. When the precursor solution for IGZO was prepared already, the carrier gas carried mists of precursor solution to the plasma region. The carrier gas and mists of precursor solution were mixed with main gas, and these gases would become plasma by arcing mechanism because of high pulsed voltage. Precursor, carrier gas, and main gas would participate with some reactions in plasma region. And then main gas would carry these plasmas to substrate and reduce the plasmas temperature. We could use a computer to control scanning path including starting point and terminal point. The main gas carried plasmas to

substrate and the IGZO films were deposited by chemical vapor deposition.

Chemical vapor deposition (CVD) is the process of depositing a solid film on the wafer surface through one or more volatile precursors, which react or decompose on the substrate surface to produce the desired deposit. Frequently, volatile by-products are also produced, which are removed by gas flow through the reaction chamber. The sample surface or its vicinity is heated in order to provide additional energy to the system to drive the reactions. The plasma and radicals would cause reactions and nucleation on samples, and then IGZO films would grow from island shape to continuous films.

3.2.3 Annealing

After IGZO thin films deposited on the wafer covered with insulator by APPJ, we put these samples in furnace. Then, these samples were annealed for 30 min at various temperature in the range from 200 to 500°C in oxygen ambiance. We expect that oxygen atoms can diffuse in the films and repair oxygen vacancies which in the IGZO films. If in the transparent TFT fabrication, it will not suit for annealing in oxygen ambiance, because oxygen will influence the electrode and effect device electrical characteristics. So we also anneal for 30 min in nitrogen ambiance at various temperature in the range from 200 to 500°C, because nitrogen is inert gas.

3.2.4 Patterning

After IGZO deposited, the next step was to define each TFT's active layer region. This procedure was carried out in lithography area by photo resist spinner and mask aligner. The patterns on mask for defining active layer region, drain electrodes, and source electrodes is shown in figure 3-6. We etched IGZO thin film by 0.5% hydrochloric acid water solution after photo resist had been put cover over IGZO film as a barrier layer for the region which we wanted to reserve.

When IGZO film which we did not want to reserve had been etched completely, the next step was to define drain and source electrodes. At the first, we though the procedures of defining drain and source electrodes were depositing aluminum and etching it by lithography and wet etching. But the active layer was under drain and source electrodes. It is difficult to choose suitable acid solution which kept good etching selectivity between aluminum and IGZO. IGZO film would be etched faster than aluminum by any acid solution. Therefore, we use lift-off process to replace etching process to define drain and source electrodes on active layer.

3.2.5 Lift-off process

Lift-off process contains several steps, we first put photo resist as a cover over IGZO region which we did not want aluminum deposited. And then we used E-Gun evaporation to deposit aluminum about 1000Å on silicon wafer. At last, we set silicon wafer in acetone with ultrasonic shaking to lift off aluminum on the photo resist. Then, a part of aluminum would stay on active layer as drain and source electrodes. And the device

as shown in figure 3-8 would be measured electrical properties and the results would be discussed in next chapter.

3.3 Characterization analysis equipment

3.3.1 Scanning Electron Microscopy (SEM)

SEM stands for scanning electron microscope. The SEM is a microscope that substitute electron for light to form an image. Scanning electron microscopes have developed new areas of study in the medical and physical science communities since their development in the 1950. SEM uses a focused beam of high energy electrons to generate a variety of signals at the surface of solid samples. The signals that derive from electron and sample interactions reveal information about the sample including external morphology, chemical composition, and crystalline structure and orientation of materials making up the sample. The researchers can inspect a much larger variety of samples by SEM.

Accelerated electrons carry significant amounts of kinetic energy in the SEM. When the incident electrons are decelerated in the solid sample, this energy is dissipated as a variety of signals produced by electron and sample interactions. These signals include secondary electrons, backscattered electrons, diffracted backscattered electrons, photons and heat. Secondary electron and backscattered electrons are commonly used for imaging samples. Secondary electrons are most valuable for showing morphology and topography on samples and backscattered electrons are most valuable for illustrating contrasts in composition in multiphase sample. X-ray generation is produced by inelastic collisions of the

incident electrons with electrons in discrete orbital of atoms in the sample. X-rays are fixed wavelength as the excited electrons return to lower energy states. Thus, characteristic X-rays are produced for each element in a mineral that is excited by the electron beam. SEM analysis is considered to be non-destructive; that is, X-rays generated by electron interactions do not lead to volume loss of the sample, so it is possible to analyze the same materials repeatedly.

The SEM has many advantages over traditional microscopes. We describe it following:

(1) It has large depth of field, which allows more of a specimen to be in focus at one time.

(2) SEM has much higher resolution so closely spaced specimens can be magnified much higher levels.

(3) Researcher has more control in the degree of magnification, because of the SEM uses electromagnets rather than lenses.

3.3.2 Transmission electron microscopy (TEM)

Transmission electron microscopy (TEM) is a microscopy technique whereby a beam of electrons is transmitted through an ultra-thin specimen, interaction with the specimen as it passes through. The interaction of the electrons transmitted through the specimen form an image that is magnified and focused onto an imaging device, such as a fluorescent screen, on a layer of photographic film, or to be detected by a sensor such as a charge coupled device (CCD) camera.

Owing to the small de Broglie wavelength of electrons, TEMs are

capable of imaging at a significantly higher resolution than light microscopes. Therefore, the instrument's user to examine fine detail even as small as a single column of atoms, which is tens of thousands times smaller than the smallest resolvable object in a light microscope. TEM is an important analysis method in the physical and biological sciences fields that application in cancer research, virology, materials science as well as pollution, nanotechnology, and semiconductor research.

At smaller magnifications TEM image contrast is due to absorption of electrons in the material, due to the thickness and composition of the material. At higher magnifications complex wave interactions modulate the intensity of the image, requiring expert analysis of observed images. Alternate modes of use allow for the TEM to observe modulations in chemical identity, crystal orientation, electronic structure and sample induced electron phase shift as well as the regular absorption based imaging.

3.3.3 Atomic Force Microscopy (AFM)

Atomic force microscopy is a manner of measuring surface morphology on a scale from angstroms to 100 microns. The technique involves imaging a sample through the use of a probe or tip, with a radius of 20 nm. The tip is held several nanometers above the surface using a feedback mechanism that measures surface tip interactions. Variations in tip height are recorded while the tip is scanned repeatedly across the sample, producing a topographic image of the surface.

In addition to basic AFM, the instrument in the Microscopy Suite is

capable of producing images in a number of other modes, including tapping, magnetic force, electrical force and pulsed force. In tapping mode, the tip is oscillated above the sample surface, and data may be collected from interactions with surface morphology, stiffness and adhesion. This result in an expanded number of image contrast methods compared to basic AFM. Magnetic force mode imaging utilizes a magnetic tip to enable the visualization of magnetic domains on the sample. In electrical force mode imaging a charged tip is used to locate and record variations in surface charge. In pulsed force mode, the sample is oscillated beneath the tip, and a series of pseudo force distance curves are generated. This permits the separation of sample topography, stiffness, and adhesion values, producing three independent images, or three individual sets of data, simultaneously.

3.3.4 X-Ray Diffraction (XRD)

X-ray diffraction (XRD) is one of the most important techniques for qualitative and quantitative analysis of crystalline compounds. The XRD technique provides information includes types and nature of crystalline phase present structural makeup of phase, degree of crystallinity, amount of amorphous content which microstrain and size and orientation of crystallites.

When a sample is irradiated with a parallel beam of monochromatic X-ray, the atomic lattice of the sample acts as a three dimensional diffraction grating causing the X-ray beam to be diffracted to specific angles. The diffraction pattern that includes position (angles) and

intensities of the diffracted beam that provides several types of information about the sample which are discussed below:

Angles are used to calculate the interplanar atomic spacing (d-spacing). Because every crystalline material will give a characteristic diffraction pattern and can act as a unique "fingerprint", the position "d" and intensity "I" information are used to identify the type of material by comparing them with patterns for over 80,000 data entries in the International Powder Diffraction File (PDF) database. Hence, identification of any crystalline compounds, even in a complex sample by XRD.

The position "d" of diffracted peaks also provides information about how the atoms are arranged within the crystalline compound (unit cell size or lattice parameter). The intensity information is used to assess the type and nature of atoms. Determination of lattice parameter helps understand extent of solid solution (complete or partial substitution of one element for another, as in some alloys) in a sample.

Width of the diffracted peaks is used to determine crystallite size and microstrain in the sample. The "d" and "I" from a phase can also be used to quantitatively estimate the amount of that phase in a multicomponent mixture. As mentioned earlier, XRD can be used not only for qualitative identification but also for quantitative estimation of various crystalline phases. This is one of the important advantages of the X-ray diffraction technique.

3.3.5 Ultraviolet-Visible Spectroscopy

Ultraviolet-visible spectroscopy (UV-Vis) refers to absorption, transmission or reflectance spectroscopy in the ultraviolet-visible spectral region. This means it uses light in the visible and adjacent (near-UV and near-infrared (NIR)) ranges. The absorption, transmission or reflectance in the visible range directly affects the perceived color of the chemicals involved. In this region of the electromagnetic spectrum, molecules undergo electronic transitions. This technique is complementary to fluorescence spectroscopy, in that fluorescence deals with transitions from the excited state to the ground state, while absorption measures transitions from the ground state to the excited state [72].

Transmission spectroscopy is highly interrelated to absorption spectroscopy. This technique can be used for solid, liquid, and gas sampling. Here, light is passed through the sample and compared to light that has not. The output depends on the path -length or sample thickness, the absorption coefficient of the sample, the reflectivity of the sample, the angle of incidence, the polarization of the incident radiation, and, for particulate matter, on particle size and orientation. In the Beer-Lambert Law, the equation I_T/T_O is called transmittance. This form of spectroscopy has a setup similar to the one used for absorption.

Table 3-1 APPJ experimental parameters

Parameter	value
Substrate temperature (°C)	200
Gap distance (mm)	5
Scan times	10
Carrier gas flow rate (sccm)	30
Main gas flow rate (SLM)	35
Carrier gas	Nitrogen
Main gas	Nitrogen
Nozzle speed (mm/s)	20
Ultrasonic frequency (MHz)	2.45

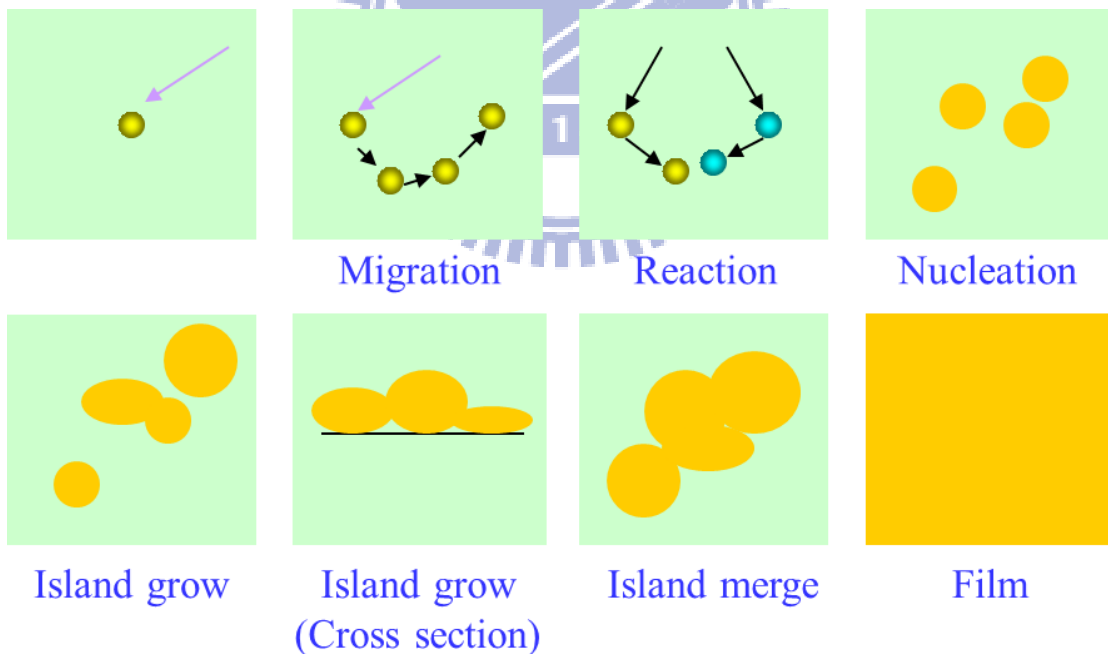


Figure 3-2 Schematic of CVD reaction steps [71]

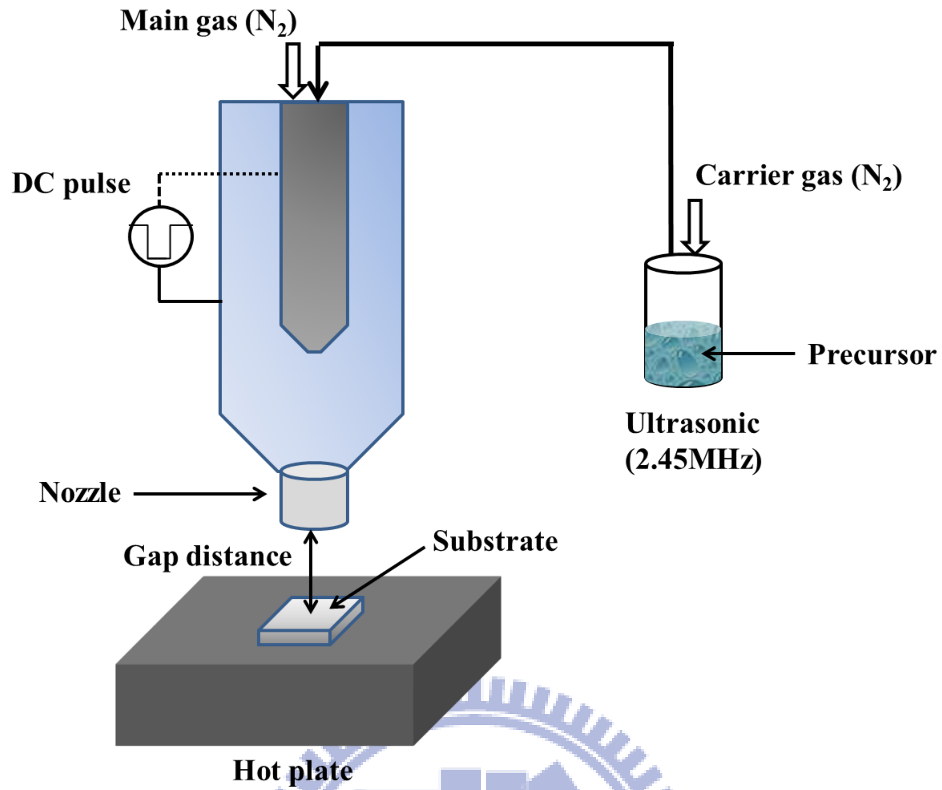


Figure 3-3 Schematic of APPJ system

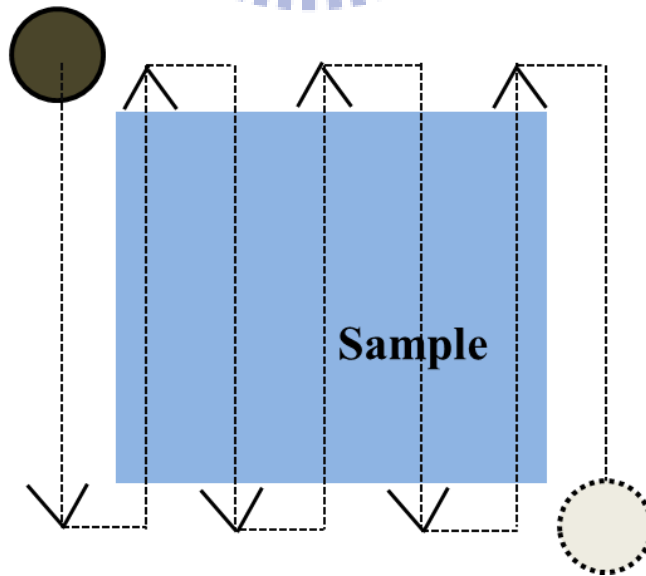


Figure 3-4 Scanning path

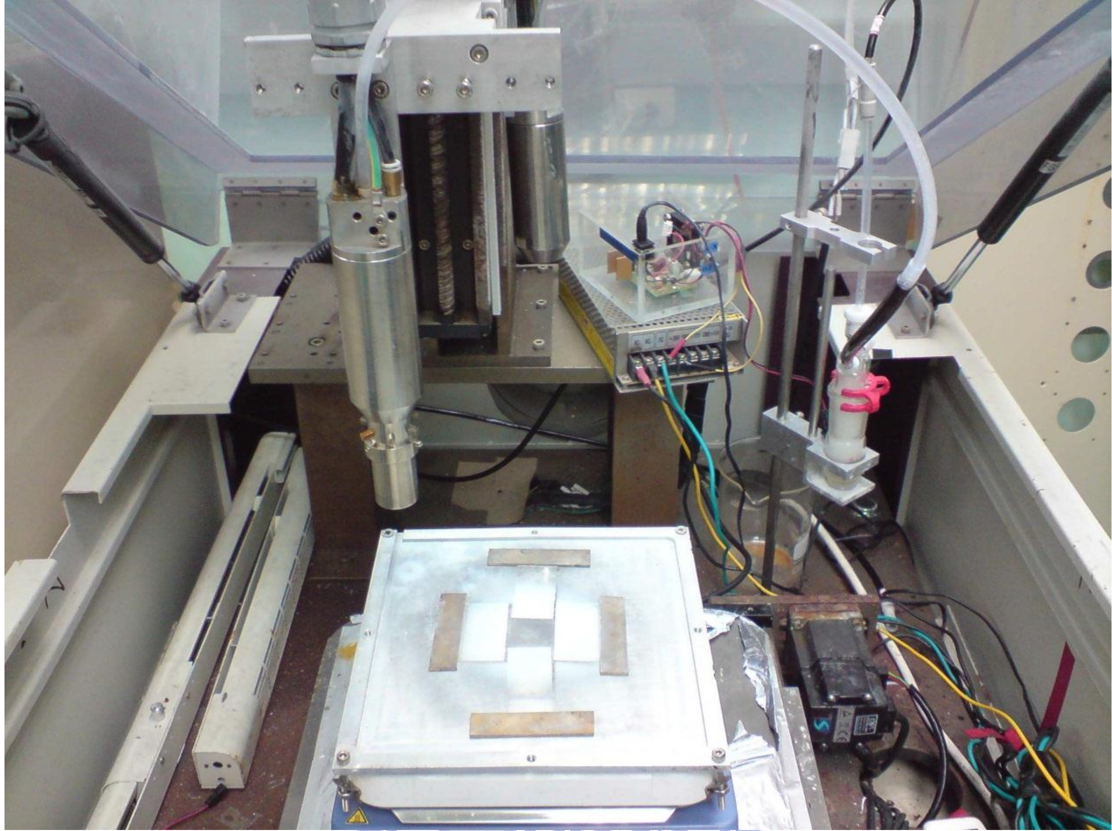


Figure 3-5 APPJ system of ITRI.

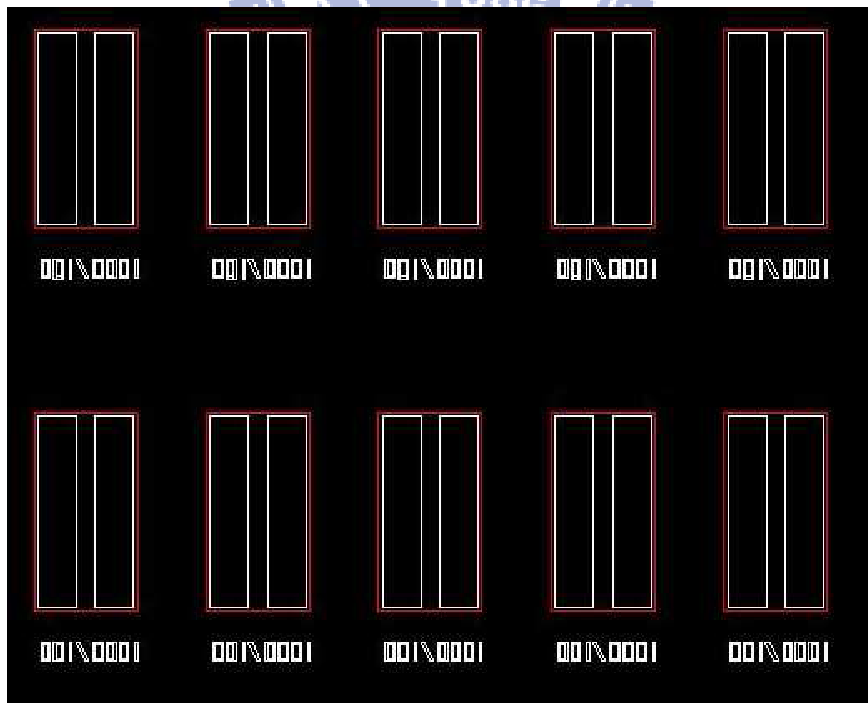
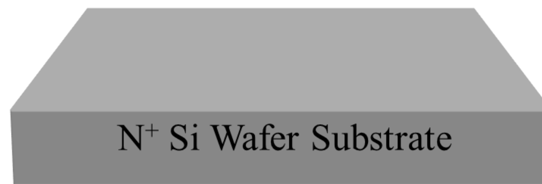
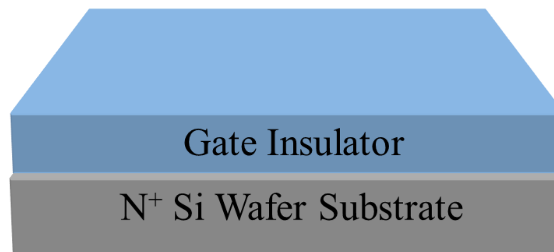


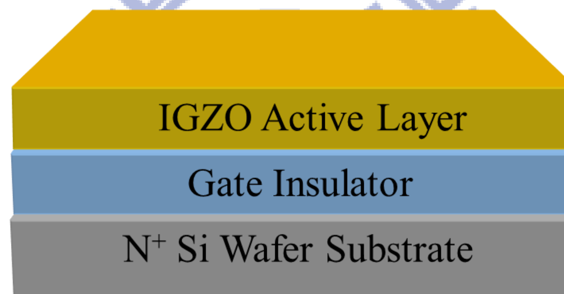
Figure 3-6 Patterns on mask



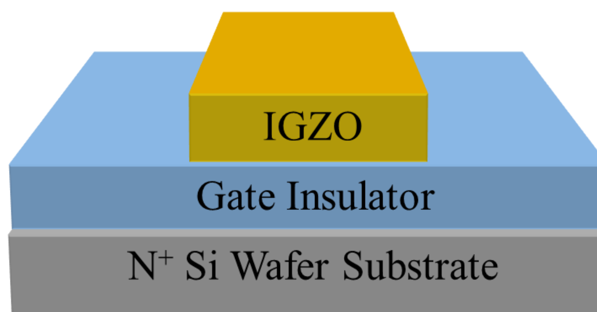
(a) N+ Silicon wafer after RCA Clean



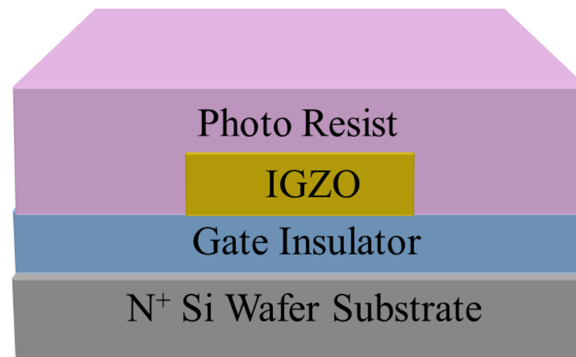
(b) Gate insulator deposited



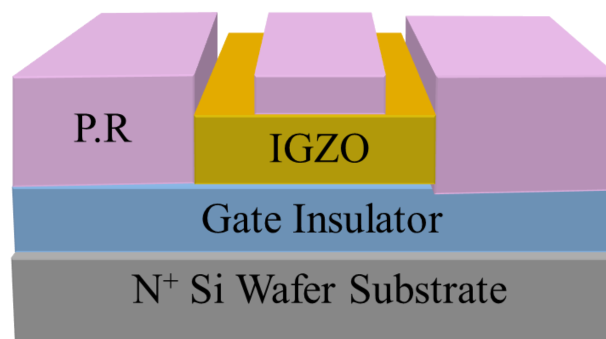
(c) IGZO thin film deposited by APPJ



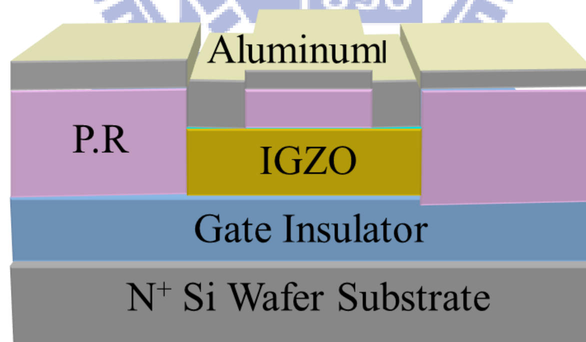
(d) Define active layer region



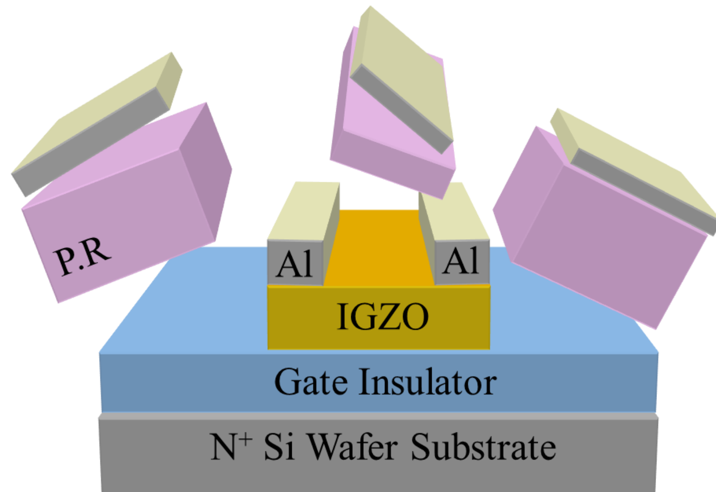
(e) Spin coating photo resist on Si wafer



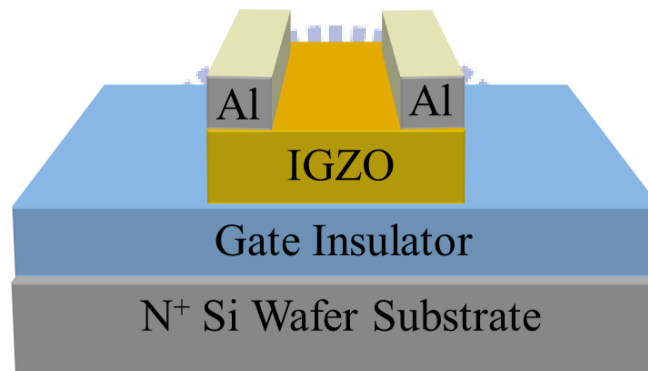
(f) Defined electrodes region



(g) Aluminum deposited by E-Gun



(h) Lift off P.R and Al on it



(i) Electrons stayed on active layer

Figure 3-7 Schematic of experimental procedures. Pictures (a) to (i) show the lift-off process.

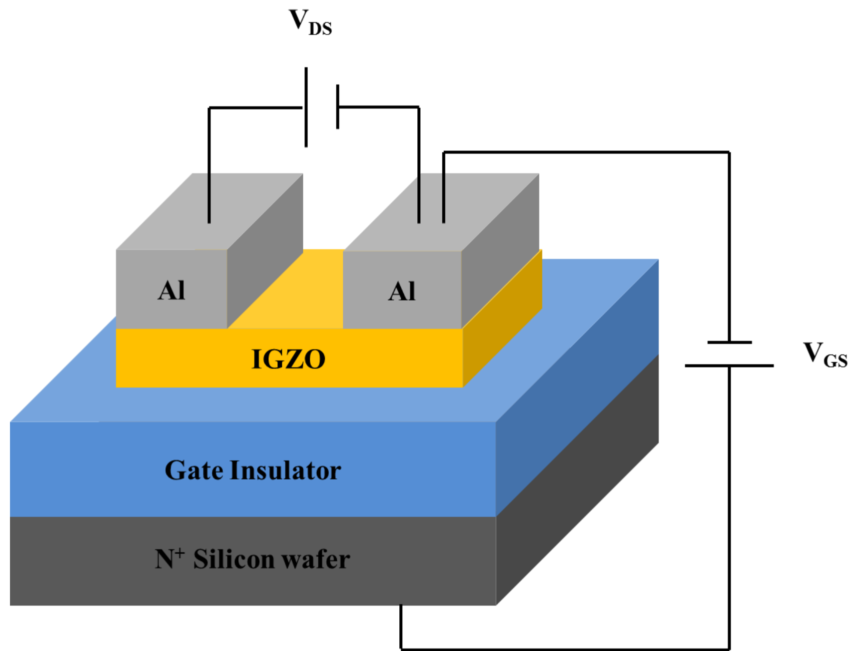


Figure 3-8 IGZO TFTs structure on silicon substrate

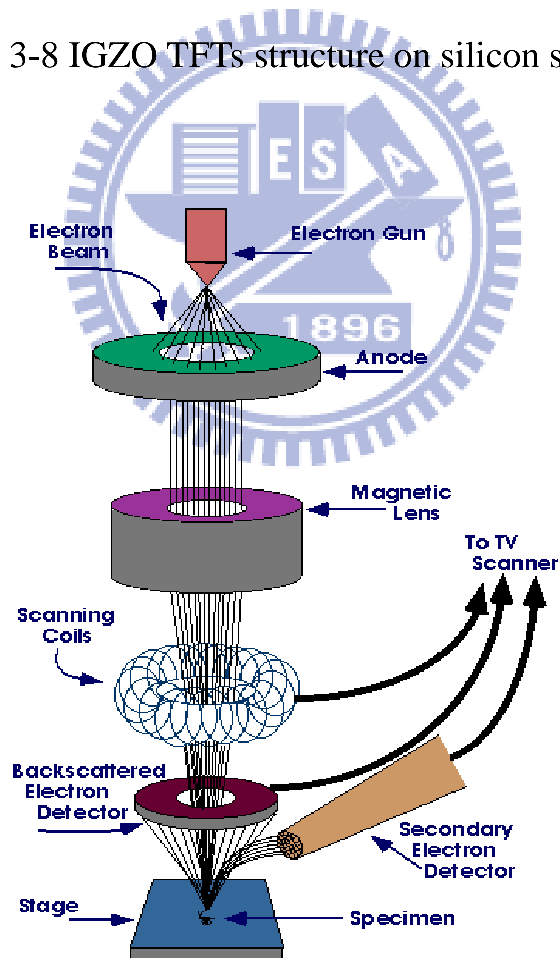


Figure 3-9 Schematic illustration of SEM instrument.

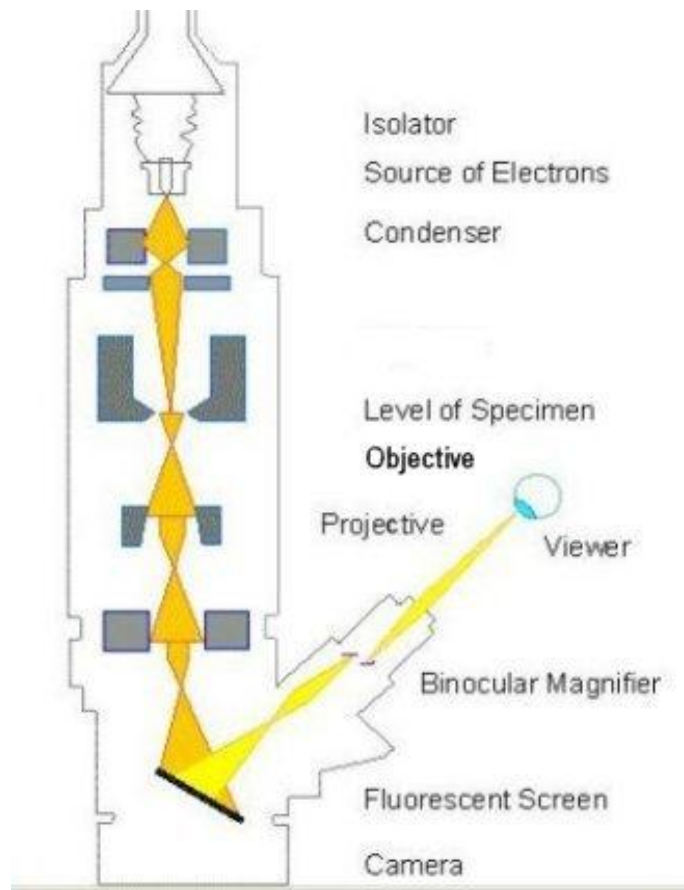


Figure 3-10 Schematic illustration of TEM instrument.

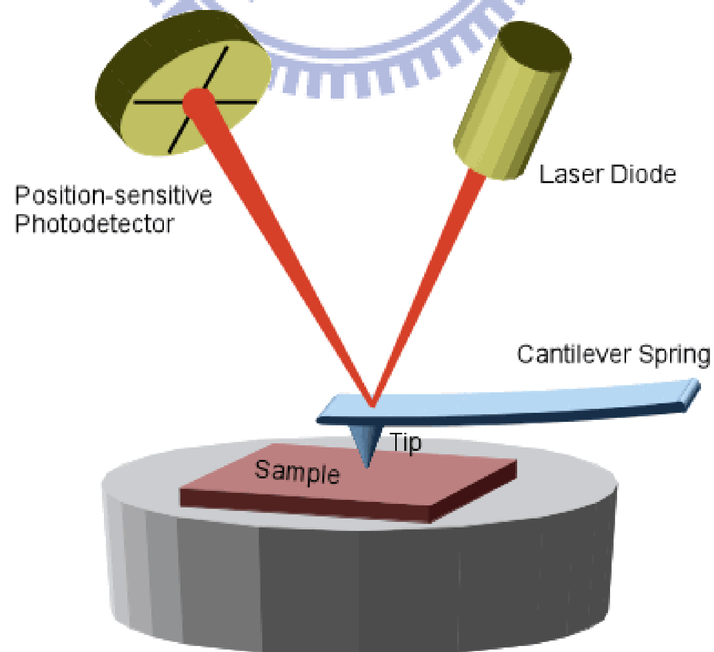


Figure 3-11 Schematic illustration of AFM instrument.

Table 3-2 Characterization analysis equipments

Instrument	Company and type
I-V	Agilent 4156C
SEM	Hitachi S-4700I
TEM	JEOL JEM-2010F
AFM	Veeco Dimension 3100
XRD	PANalytical X'Pert pro
XPS	PerkinElmer PHI1600
UV-VIS-MIR	VASCO V-570

Chapter 4
Results and Discussions

In this chapter, we will discuss and explain the characterizations of IGZO thin films and the effect of annealing on IGZO films by SEM, AFM, XRD, XPS, TEM and UV-VIS-MIR. Next, we will compare different annealing temperatures of TFTs electrical characteristics. Finally, to improve the TFT electrical characteristics and increase the applications of TFT, we substitute the insulator of SiO_2 with HfO_2 and Al_2O_3. We will compare the different high-*k* material for better gate dielectric and electrical characteristics. Consequently we will discuss the following conditions:

1. The annealing temperature :

   (1) 200°C (2) 300°C (3) 400°C (4) 500°C

2. The annealing ambiance :

   (1) N_2 (2) O_2

3. The gate insulator :

   (1) SiO_2 (2) HfO_2 (3) Al_2O_3

4.1 The characterization of IGZO films

4.1.1 Surface morphology

Figure 4-1 shows the SEM image of no thermal treatment IGZO sample. We can observe that lots of particles on IGZO thin film. From the view of CVD process, the precursor from the nozzle may be nucleation in the gas phase and then formation the particles fall on the thin film surface and then migrates on the surface, finally nucleation on the surface to form the IGZO thin films. Because of the sample had not be thermal treatment, the particles have not enough energy to migrate. Therefore, there are many particles on the thin film surface and the IGZO film is sparse.

Figure 4-2 and figure 4-3 show the top view of SEM images of IGZO thin films which represent the different annealing temperature in nitrogen and oxygen ambiance, respectively. We can observe that the IGZO thin films become denser and smoother with the higher thermal annealing. The samples which annealing 500°C compare with the figure 4-1, we observe obvious variation of these SEM images, the thermal treatment will change the surface morphology apparently. However in nitrogen or oxygen ambiance, the molecules and gas phase particles of IGZO films will get enough energy to decompose and recompose the structure of films by thermal annealing. Therefore, the surface of figure 4-2 (d) and figure 4-3 (d) are denser and smoother than figure 4-1 because of the particles decomposition and migration on the surface of IGZO films. Because the solution based IGZO thin film, there are many water molecules in the films. When the films are be thermal treated, the water molecules will be released from the IGZO films and the structure of films

become compact. Evidently, the IGZO thin films have greater quality with thermal annealing.

We also use the AFM to analyze the surface morphology which is show in figure 4-4 and figure 4-5 represented the IGZO thin films of different annealing temperature. The results of AFM analysis were consistent with SEM analysis. In summary, postannealing treatment can produce IGZO thin films that have better quality and reduce surface roughness for achieving good transfer characteristics and stability of TFTs.

4.1.2 Structure properties

Figure 4-6 and figure 4-7 show the XRD patterns with different annealing temperature in nitrogen and oxygen ambiance, respectively. In the figure 4-6, there is no prominent peak in XRD pattern which means that the sample of IGZO thin film with no annealing has an amorphous phase. So far, we understand that the IGZO thin film deposited by APPJ system is amorphous state, because we prepared IGZO thin films by solution based precursor and the process in APPJ system under low temperature. After thermal treatment from 200°C to 500°C, we observe that the XRD patterns without significant change between no annealing sample. Even at a relatively high annealing temperature of 500°C, the IGZO thin films have an amorphous phase. In the figure 4-7, we also observe that the XRD patterns which annealing in oxygen ambiance have no obvious peak similar to the XRD patterns which annealing in nitrogen ambiance, However, the IGZO thin films have an amorphous phase in the

different anneal ambiance. We successfully deposit IGZO thin films with amorphous state which conduce as active layer of TFT application.

The XRD results are in good agreement with the high-resolution TEM image of the sample annealed at 500°C shown in figure 4-8. In the case of the sample annealed at 600°C, it is observed that a very small amount of crystallization occurs with tiny nanoparticles being formed. In the figure 4-8 shows the nanocrystalline with a size less than 5 nm in the IGZO thin film. Because of the thermal treatment that provide thermal energy to change the phase, the partial structure of IGZO change phase from amorphous to nanocrystalline. However, the low density and small size of these crystals result in their producing no diffraction peaks in the XRD measurements.

In the figure 4-9, it shows the thickness of native oxide on silicon wafer. After the silicon wafer cleaned by RCA process, the wafer will temporarily expose to air environment when it prepared to deposit gate dielectric. The native oxide will add the thickness of gate dielectric and decrease the capacitance of gate dielectric. Because of the rough surface of native oxide, it maybe affects dielectric quality. The native oxide must be as thin as possible to reduce the influence on device property. In the figure 4-9, we can see the native oxide with a thickness of about 1.67 nm.

The IGZO thin films deposited by APPVCD are the most important key point of the electrical properties of devices. In APPJ system, we could control several conditions including scan times, carrier gas, main gas, hot plate temperature to influence the quality of IGZO. Electrical properties of devices including current on-off ratio, field effect mobility,

and threshold voltage are relative to thickness of IGZO thin films as active layer. We can use scan times to control the thickness of IGZO which the time of one scan cycle was 120 seconds. And the experiment conditions were shown in table 3-1. As shown in figure 4-10 the TEM results, the IGZO thin films have a thickness of about 40 nm and an amorphous-like phase. We could make sure that IGZO thin films grew about 4 nm in one scan time.

In the figure 4-10, we also see the Al_2O_3 with thickness of about 30.5 nm. Later, we would discuss the thickness of gate insulator relative to electrical properties.

In the figure 4-10, the result of XPS analysis shown In, Ga, Zn and O signals in the IGZO thin films which deposited by APPJ. It proved that we successfully deposited solution based IGZO thin films by APPJ system. We also observe the other signal like nitrogen and carbon. It is easy to understand that the IGZO deposited by APPJ under atmospheric, the atmosphere is formed by number of elements including nitrogen, oxygen, carbon, argon, hydrogen and so on. When depositing IGZO thin films, these elements maybe dissociated by plasma or thermal decomposition and then falling on the thin films. Furthermore, nitrogen of main gas accompany with precursor through plasma region, so nitrogen incorporation of IGZO effect on the stability and electrical performance of IGZO TFT [73]. Because the Ga Auger signal is similar to the signal of N1s in the IGZO films, nitrogen proportion in the films is not correct.

In the table 4-1 and table 4-2 shown the elements proportion of the IGZO thin films in different annealing ambiance respectively, but the

nitrogen content should be amend. We observed that In, Ga, and Zn ratio is inconsistent with previous preparation of precursor. When the precursor was atomized which delivered into plasma zone by carrier gas, electron would collide with these molecules and break the chemical bond to generate free radicals. Because indium has relatively inertia among gallium and zinc, indium nitrate would be hard dissociated to radicals. For this reason, the indium radicals were less than the others. Moreover, indium has lower reaction activity than gallium and zinc, even when they forming radicals, they would be recombination soon and take them away from substrate to air by main gas. In summary, indium radicals were difficult to react with gallium and zinc forming IGZO films when indium was dissociated by plasma.

4.1.3 Optical properties

The transmission of solution based IGZO thin films deposited on glass substrate with difference annealing temperature in the wavelength range from 300 to 900 nm is shown in figure 4-11 and 4-12. The spectrum shows that the IGZO thin film is highly transparent with above 80% transparency in the visible range. And we used the following functions to determine the optical band gap:

$$T = (1 - R^2)e^{-\alpha d} \qquad (4.1)$$

$$(\alpha h\nu)^2 = \left(h\nu - E_g\right) \qquad (4.2)$$

First, we extract optical absorption coefficient (α) by transmittance (T), reflectance (R) and thickness of IGZO (d). Second, we could use the optical absorption coefficient (α) to determine the optical band gap (E_g). The optical band gap can be determined by the extrapolation of the linear region from a plot of $(\alpha)^2$ vs. photon energy (hv) near the onset of the absorption edge to the photon energy axis. The optical band gap of the solution based IGZO thin film was measured to be 3.78 eV.

When the photon energy is more than 3.78 eV which the wavelength is less than 328 nm, the photon energy would be absorbed by electrons, and electrons transited form valance band to conduction band. Therefore, the high transmittance of IGZO thin film in visible range could be used extensively for display applications. figure 4-13 shows a photography image of 500°C annealed IGZO film on glass, clearly illustrating the transparency of the film.

4.2 The electrical characteristics of IGZO TFT

4.2.1 The effect on postannealing treatment

The IGZO TFTs fabricated with gate insulator of SiO_2 at different annealing temperature from 200°C to 500°C in nitrogen and oxygen ambiance had been measured by Agilent 4156C for I_D-V_G and I_D-V_D curves as shown in figure 4-14, figure 4-15, figure 4-16 and figure 4-17, respectively. We also compared the conditions between no thermal treatment and annealed at 500°C for IGZO thin films of devices I_D-V_G curves in figure 4-18.

First, we should define some important electrical properties of

devices:

Threshold voltage:

$$I_D = K \times (V_G - V_{th})^2 \qquad (4.3)$$

$$K = \frac{WC_{OX}\mu}{2L} \text{ (for } V_D > V_G - V_{th}) \qquad (4.4)$$

$$I_D^{1/2} = K^{1/2} \times (V_G - V_{th}) \qquad (4.5)$$

Mobility:

$$Mobility(\mu) = \frac{2KL}{WC_{OX}} \qquad (4.6)$$

$(W/L = 200\mu m/20\mu m)$

$(C_{OX} = 26.01\text{nF}/cm^2)$ for SiO_2

Subthreshold swing:

$$SS = \left(\frac{d \log I_D}{dV_G}\right)^{-1} \qquad (4.7)$$

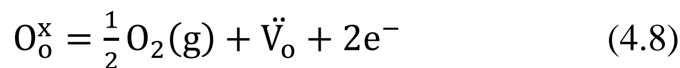
On-off ratio:

I_{max}/I_{min}

We extracted threshold voltage and field effect mobility in saturation mode by $I_D^{1/2}$-V_G curve. The slope of curve in saturation mode is $K^{1/2}$ and the intercept on x-axle is threshold voltage. And then we used K to calculate mobility. We also extracted subthreshold swing and on-off ratio by $\log I_D$-V_G curve which slope invert is S.S. and the value of maxima current dividing minima current is on-off ratio. The important electrical

properties are listed in table 4-3 and table 4-4. We could observe the three of IGZO TFT with no annealing treatment and annealing 200°C respectively, in nitrogen and oxygen ambiance samples which did not have TFTs device properties. These are indistinct on-off state in I_D-V_G curve, and these IGZO TFTs electrical properties in table 4-3 and table 4-4 are inaccurate.

Moreover, the IGZO TFT appear device properties when the annealing temperature higher than 300°C. The IGZO TFT with annealing 300°C had depletion mode, because threshold voltage are minus, and it would limit TFTs application in depletion mode. The TFTs electrical properties became better with increasing annealing temperature. When we deposited IGZO thin films by APPVCD, there are many defects in IGZO films. These defects are including oxygen vacancy, interstitial and impurity atom. After postannealing treatment, thermal energy provides atoms and molecules rearrangement in IGZO films and then enhanced IGZO structure becoming stronger and repaired these defects. Free electrons in the IGZO semiconductors are known to be mainly attributed to the generation of oxygen vacancies. And the oxygen vacancies were generated by the following reaction:



$$O_O^x = \frac{1}{2}O_2(g) + \ddot{V}_O + 2e^- \qquad (4.8)$$

The oxygen atoms can preferentially leave their original sites, resulting in the formation of carriers with two electrons per oxygen vacancy [74-76]. In our solution based prepared IGZO films by APPJ, oxygen vacancies decreased during annealing in nitrogen and oxygen ambiance, which is strongly dependent on the annealing temperature.

Thus, it is expected that annealing at a higher temperature reduced oxygen vacancies density. Therefore, a higher annealing temperature leads to less electron carriers and as a result, V_{th} shifts positively as the annealing temperature increase.

To consider about mobility, the mobility is relative to defects include oxygen vacancies and impurity atoms in the IGZO films. These defects would affect mobility seriously because defects lead to free electron scattering. Therefore, mobility decreases with high density of defects. For other reasons, surface morphology and interface between semiconductor and gate dielectric also influence the mobility. According to SEM and AFM analysis, we know that surface morphology would be modified when increase annealing temperature. And interface between IGZO films and gate dielectric also be modified because IGZO films have better quality as annealing temperature increase. In summary, the mobility would be effectively improved which is attributed to repairing defects of IGZO films, modification of the interface between IGZO films and gate dielectric, and atomic rearrangement with increasing annealing temperature. So, the IGZO TFT had best device properties than the others when annealing temperature at 500°C.

4.2.2 The effect on postannealing environment

After discuss the effect on annealing temperature for IGZO TFT properties, next we focus on the annealing environment. First, the IGZO thin films annealing in nitrogen ambiance have great quality which as channel of IGZO TFT with good properties consequently. By the way,

the ambient stability of IGZO-based materials is strongly related to the distribution of oxygen vacancies during the films deposition. The inactive oxygen from the IGZO backchannel region can react with the ambient atmosphere and causes a desorption reaction to form oxygen vacancies [77-78]. When IGZO annealed in nitrogen ambiance, the nitrogen would be incorporation of IGZO films and the nitrogen atoms can partially replace the inactive oxygen atoms and reduce the oxygen desorption effect. Thus, the interaction between the IGZO backchannel layer and the atmosphere can be effectively reduced and the ambient stability of IGZO TFT is enhanced consequently.

Second, the quality of IGZO thin films annealing in oxygen ambiance which is similar to annealing in nitrogen ambiance and the IGZO TFT also had good electrical properties. The electrons concentration were mainly contributed by oxygen vacancies which be formed when IGZO thin films deposited by APPJ. When IGZO films were annealed in oxygen ambiance, oxygen would diffuse in IGZO films and repaired oxygen vacancies. Thereby, the electrons concentration reduced as decreasing oxygen vacancies and leading to increasing in the V_{th} of the IGZO TFTs. Furthermore, the chemisorbed oxygen molecules on the IGZO films surface get ionized by capturing an electron from the conduction band and that the resulting oxygen species can exist in various forms such as O^{2-}, O^{-}, or O_2^{-}, as described by the following chemical reaction [79-81]:

$$O_2(g) + e^- \rightarrow O_2^-(ad) \quad (4.9)$$

As a result of charge transfer between adsorbed oxygen molecules

and IGZO channel, a depletion layer of electrons is formed beneath the oxide surface, thus lowering the conductivity and also leading to V_{th} shift positive.

On the other hand, oxygen diffused in IGZO films not only repaired oxygen vacancies but also formed oxygen interstitials. The oxygen interstitials are defects in IGZO films which conducing electron concentration increasing and then leading to decreasing in the V_{th} of the IGZO TFTs. In addition, the inactive oxygen from the IGZO films surface could react with the ambient atmosphere and causes a desorption reaction to form oxygen vacancies which leading to decrease V_{th}.

In conclusion, we deposited IGZO thin films by APPJ and annealing in nitrogen or oxygen ambiance. The IGZO TFTs electrical characteristic has excellent properties in the both of conditions. However we prefer to anneal IGZO thin films in nitrogen ambiance. When fabrication of transparent thin film transistor (TTFT), we must replace highly doping silicon with transparent conductor for gate electrode. When the IGZO thin films annealed in oxygen ambiance, the electrode would be oxidized. As a result, the TFTs electrical properties would be worse. Next, we focus on high-*k* dielectric of IGZO TFT with annealing temperature at 500°C in nitrogen ambiance.

4.2.3 High performance IGZO TFT with high-*k* dielectric

In the end, we expect to improve electrical properties of IGZO TFT which are low driving voltage and subthreshold swing. Therefore, we are going to substitute high-*k* material for SiO_2 as gate dielectric of TFTs.

And the high-*k* dielectric materials which HfO_2 and Al_2O_3 are two of the most promising materials for gate dielectric of TFTs due to the properties of high dielectric constant, relatively low leakage current, low synthesis temperature, wide band gap sufficient to yield a positive band offset with respect to IGZO, and high transparency in visible range.

In general, the dielectric constant of HfO_2 and Al_2O_3 are 25 and 9 respectively. And the both of dielectric constants are higher than SiO_2 which dielectric constant is 3.9. And then we define three importance electrical properties of IGZO TFT which are capacitance, threshold voltage and subthreshold swing as following equations. Consequently, we know that V_{th} and SS could be decreased due to HfO_2 and Al_2O_3 as gate dielectric of high capacitance.

Gate dielectric of Capacitance:

$$C_{ox} = \varepsilon_0 \frac{k}{t_{ox}} \tag{4.10}$$

Threshold voltage:

$$V_{th} = \emptyset_{ms} - \frac{Q_{tot}}{C_{ox}} - \frac{Q_{dep}}{C_{ox}} - 2\emptyset_F \tag{4.11}$$

Subthreshold swing:

$$\mathrm{SS} = \frac{kT}{q} \times \ln 10 \times \left[1 + \frac{(C_{it}+C_{dep})}{C_{ox}}\right] \tag{4.12}$$

We extracted the HfO_2 and Al_2O_3 capacitance density which are 247nF/cm^2 and 214nF/cm^2 by figure 4-19 and figure 4-20. The dielectric

constant which are 8.38 and 7.24 could be derived by equation of $k = t_{ox}\frac{C_{ox}}{\varepsilon_0}$. There is a great difference between real dielectric constant (8.38) and ideal dielectric constant (25) of HfO_2. It attribute to interfacial layer between Si and HfO_2 when growing HfO_2 on silicon wafer by MOCVD. The leakage current density of HfO_2 and Al_2O_3 are 1.4×10^{-7} A/cm^2 and 2.16×10^{-8} A/cm^2 under 1MV/cm^2, respectively. The Al_2O_3 as gate dielectric would effectively insulate electron than HfO_2 because of lower leakage current density. And the J-V characteristics of an Al/Al_2O_3/N^+Si gate capacitor are shown in figure 4-21.

The I_D-V_G and I_D-V_D curves of IGZO TFT with HfO_2 and Al_2O_3 gate dielectric as shown in figure 4-22, figure 4-23 and figure 4-24, respectively. And we extracted the electrical properties of devices to list in table 4-5. We could observe that the V_{th} is minus of the IGZO TFT with HfO_2 gate dielectric. The depletion mode TFT would increase power consumption, and limit it application, so we focus on the IGZO TFT with Al_2O_3 gate dielectric.

The I_D-V_G, I_G-V_G and $I_D^{1/2}$-V_G curves of IGZO TFT with gate dielectric as shown in figure 4-25, and we find that the drain leakage current trend is similar to gate leakage. This result indicates that the drain leakage current is attributed to gate leakage current. However, we successfully deposited IGZO thin films on Al_2O_3 as gate dielectric with excellent performance of device and compared with others solution based IGZO TFT listed in table 4-5.

The solution based IGZO TFTs with Al_2O_3 as gate dielectric shows promising results of low threshold voltage (V_{th} = 0.75 V), small

subthreshould swing (SS = 0.28V/dec), high mobility (μ = 8.6 cm^2/V-s), and good I_{on}/I_{off} ratio of 1.04×10^8 and have great potential to be applied in the next generation flexible displays.

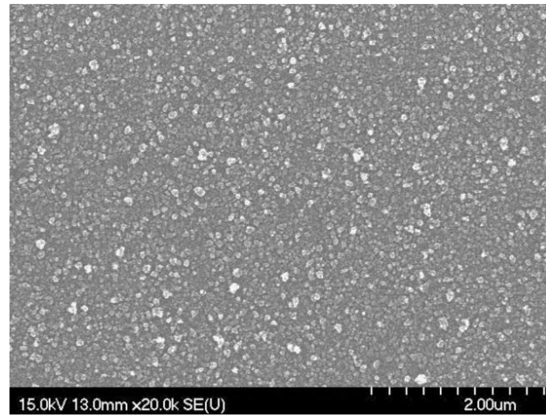
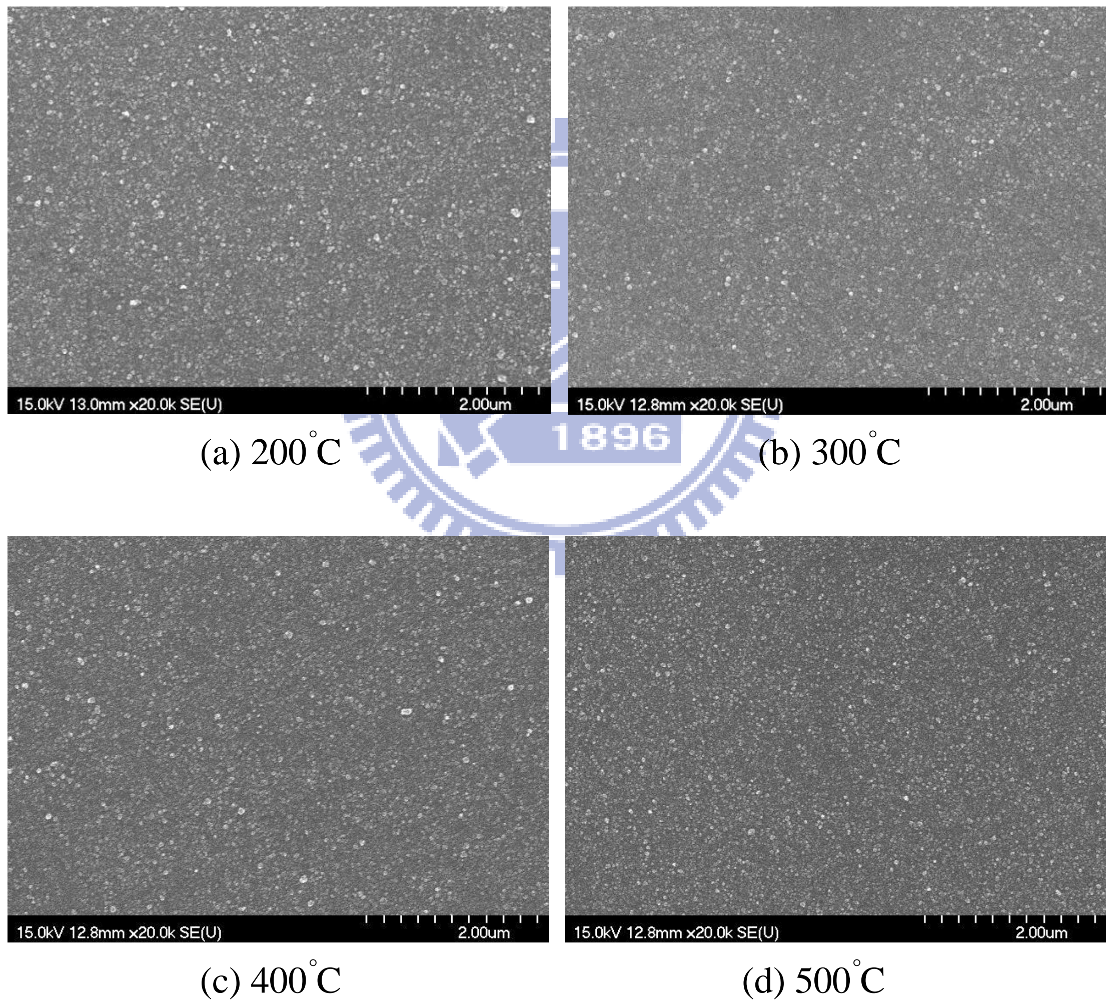


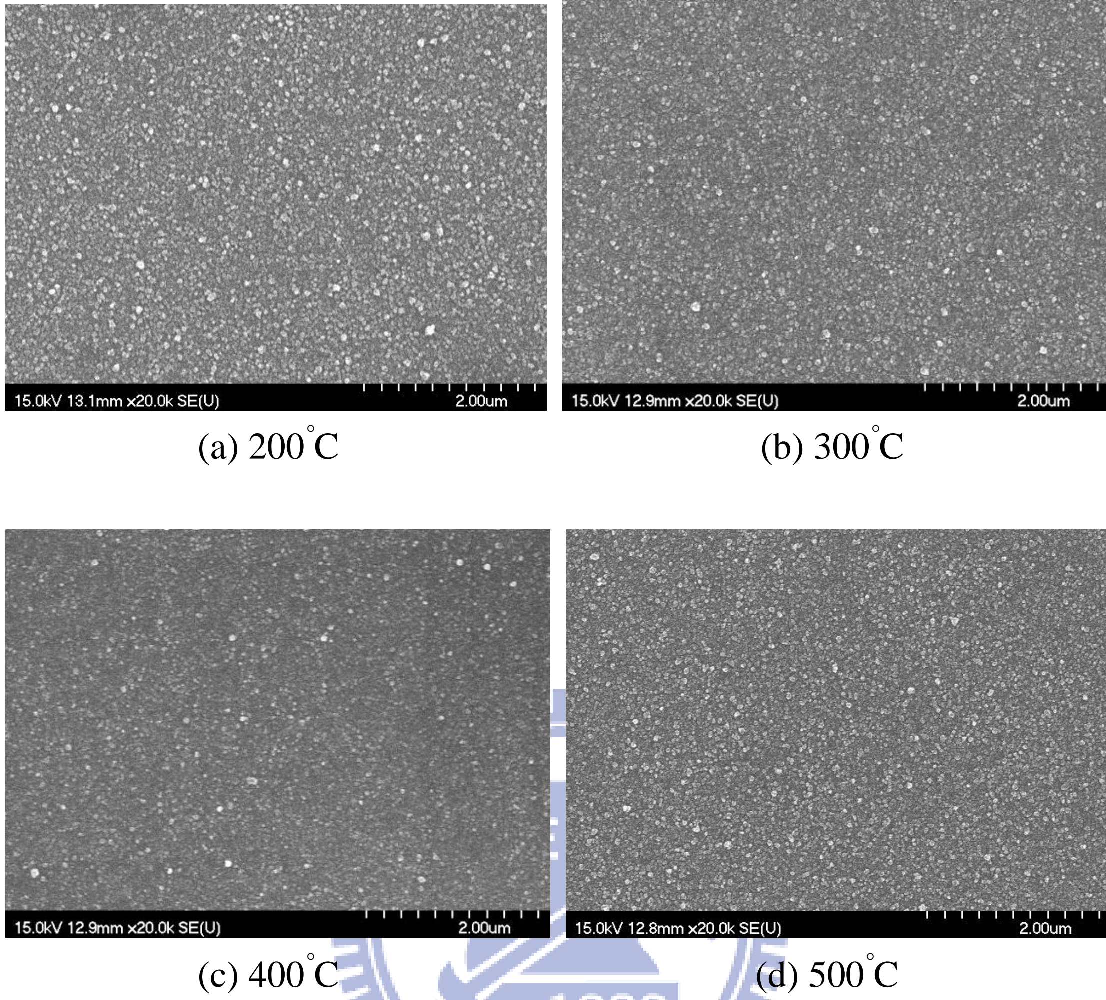
Figure 4-1 SEM image of IGZO thin film without thermal treatment



(a) 200°C (b) 300°C

(c) 400°C (d) 500°C

Figure 4-2 SEM images of deposited IGZO thin films which are annealed with different temperature in nitrogen ambiance (a) 200°C (b) 300°C (c) 400°C (d) 500°C.



(a) 200°C (b) 300°C

(c) 400°C (d) 500°C

Figure 4-3 SEM images of deposited IGZO thin films which are annealed with different temperature in oxygen ambiance (a) 200°C (b) 300°C (c) 400°C (d) 500°C.

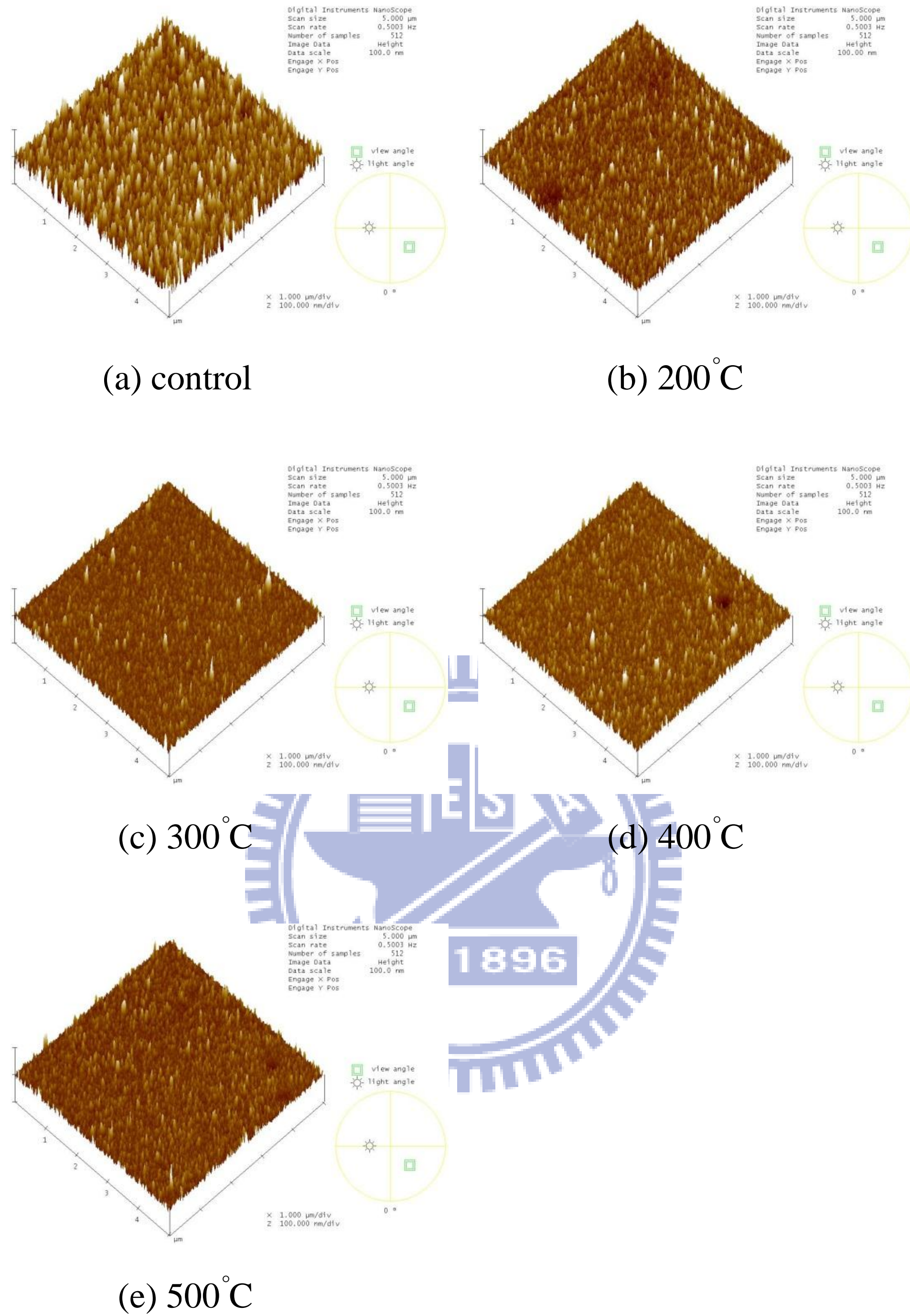


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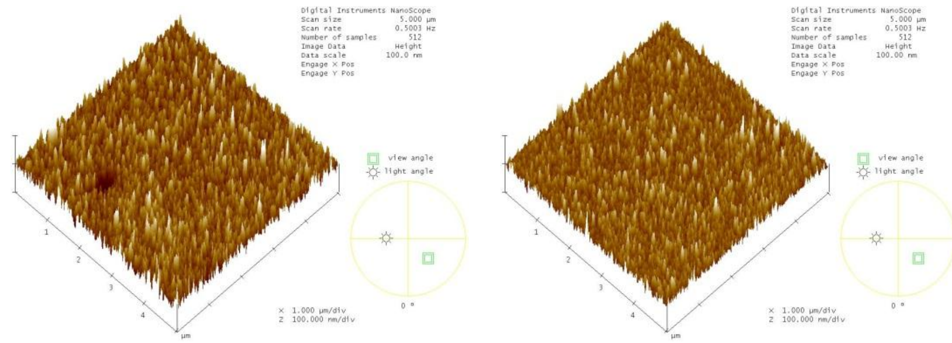
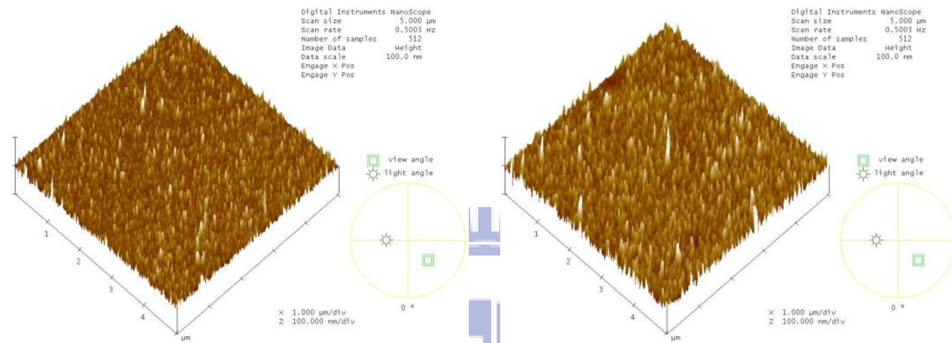
Figure 4-4 AFM images of deposited IGZO thin films which are annealed with different temperature in nitrogen ambiance (a) control (b) 200°C (c) 300°C (d) 400°C (e) 500°C.



(a) 200°C (b) 300°C



(c) 400°C (d) 500°C

Figure 4-5 AFM images of deposited IGZO thin films which are annealed with different temperature in oxygen ambiance (a) 200°C (b) 300°C (c) 400°C (d) 500°C.

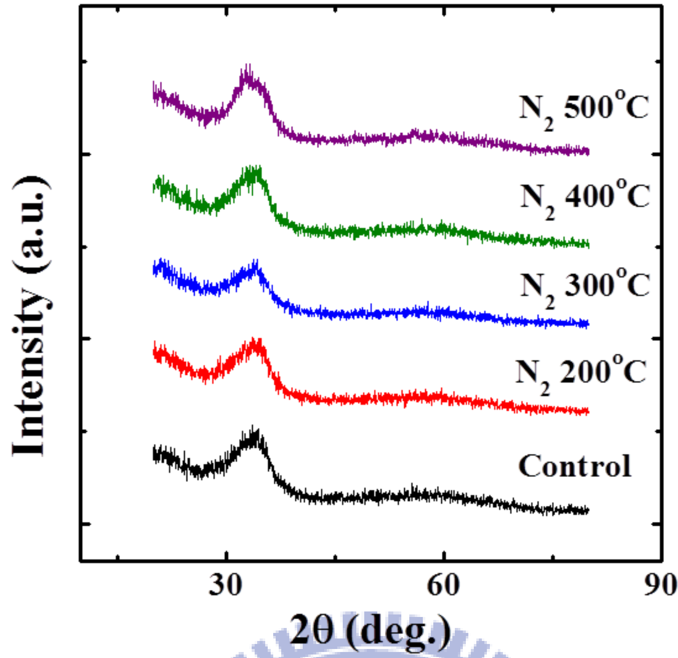


Figure 4-6 XRD patterns of IGZO thin films annealed with different temperature in nitrogen ambiance.

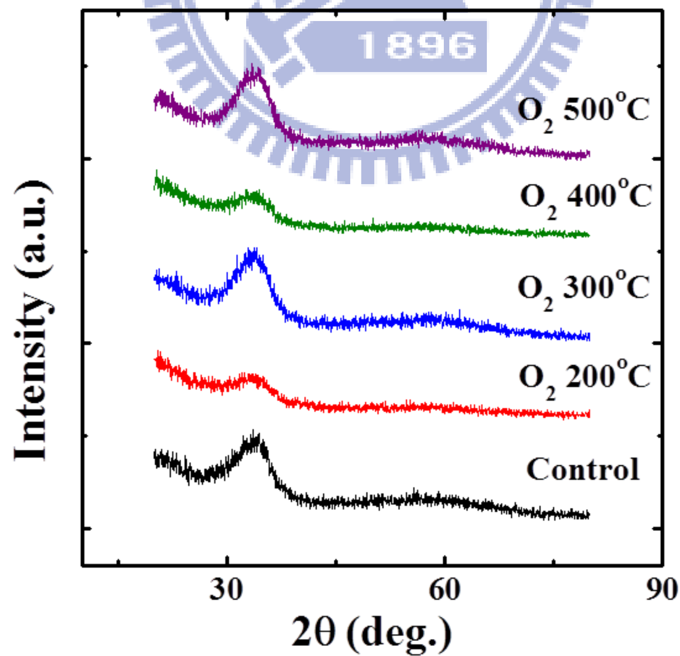


Figure 4-7 XRD patterns of IGZO thin films annealed with different temperature in oxygen ambiance.

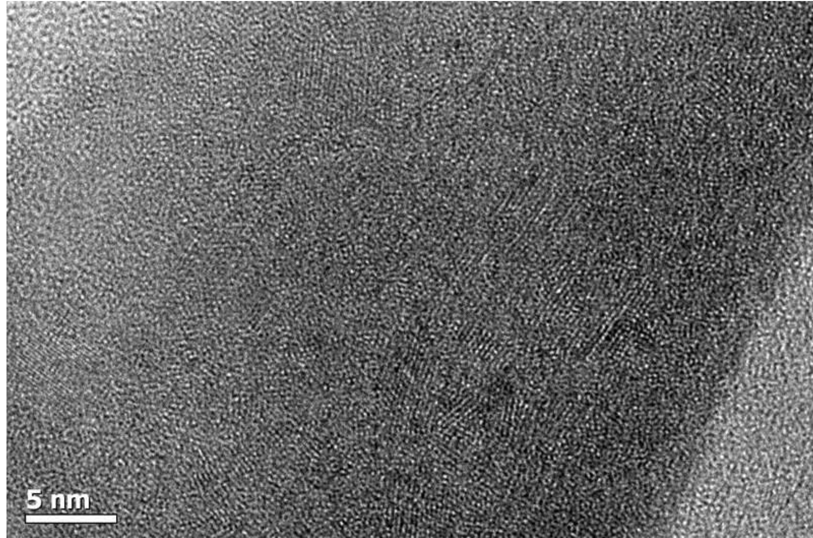


Figure 4-8 TEM image of IGZO thin films annealed at 500°C.

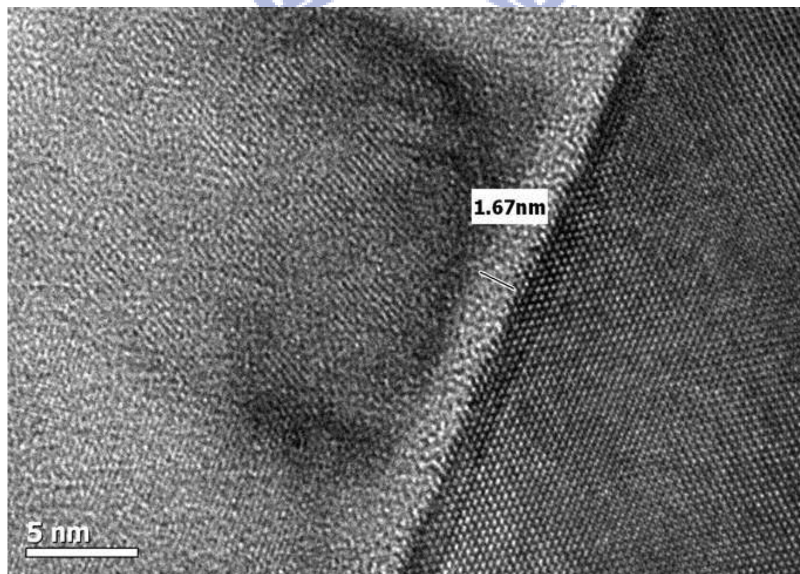


Figure 4-9 TEM image indicates a thickness of native oxide.

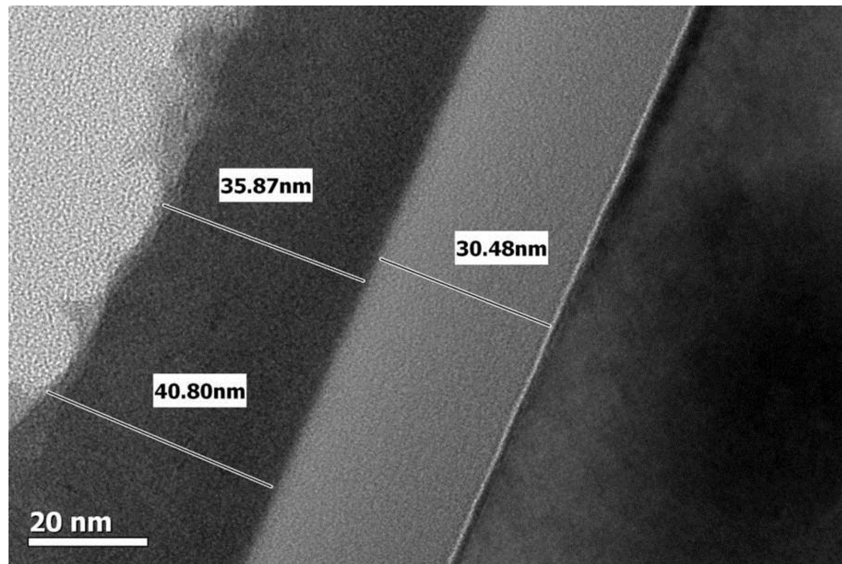
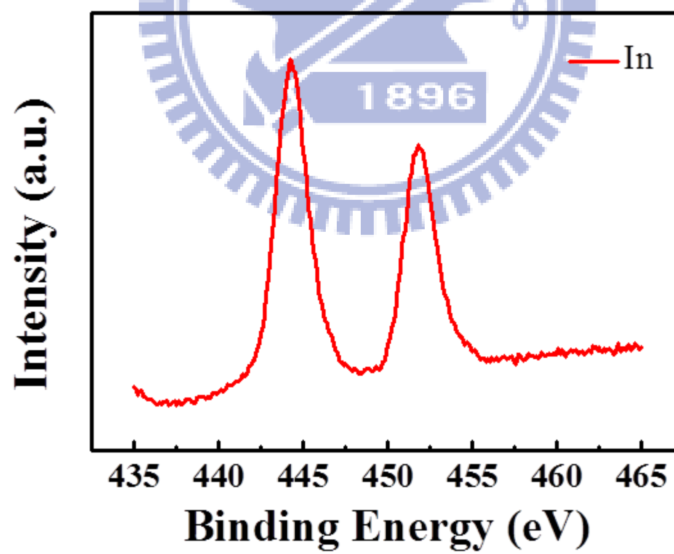
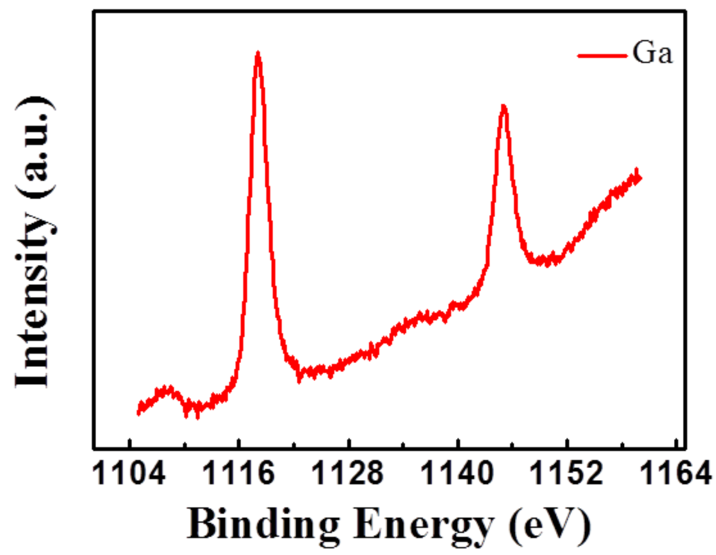


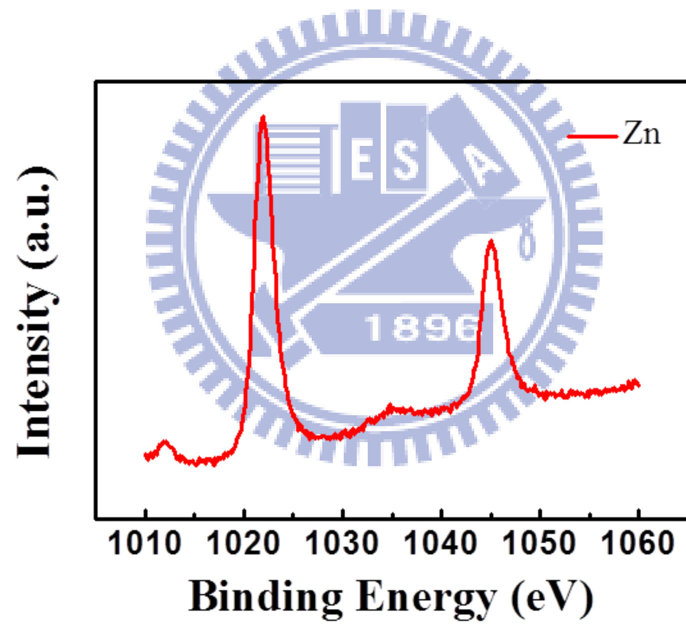
Figure 4-10 TEM image indicates a thickness of IGZO thin films about 40 nm and Al_2O_3 of gate dielectric with thickness about 30.5 nm (IGZO/ Al_2O_3/ Native oxide/ Si).



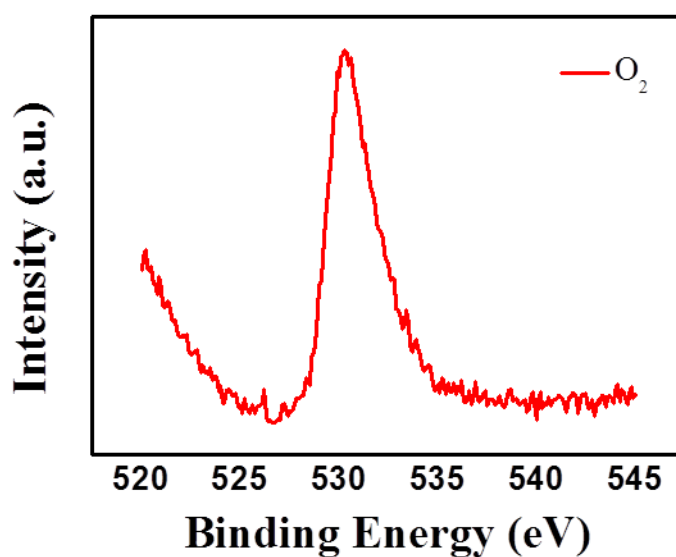
(a) Indium signal in IGZO films



(b) Gallium signal in IGZO films



(c) Zinc signal in IGZO films



(d) Oxygen signal in IGZO films

Figure 4-11 XPS analysis of IGZO thin films with annealing temperature 500°C in nitrogen ambiance (a) In signal (b) Ga signal (c) Zn signal (d) O signal.

Table 4-1 Element composition and percentage of IGZO thin films with annealing temperature 500°C in nitrogen ambiance

Name	At. %
C 1s	2.65
N 1s	11.1
In 3d5	6.63
O 1s	22.24
Zn 2p3	30.1
Ga 2p3	27.29

Table 4-2 Element composition and percentage of IGZO thin films with annealing temperature 500°C in oxygen ambiance

Name	At. %
C 1s	3.44
N 1s	13.35
In 3d5	6.78
O 1s	22.54
Zn 2p3	30.83
Ga 2p3	23.05

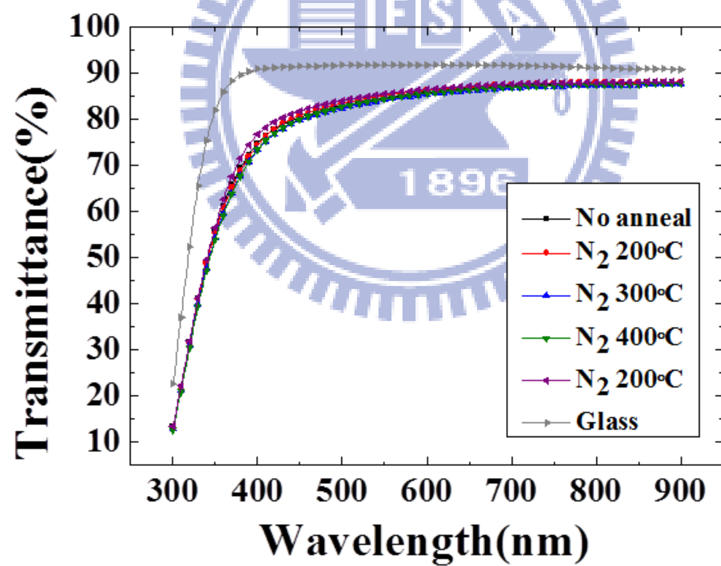


Figure 4-12 Optical transmittance spectra of IGZO thin films deposited on glass substrate with different annealing temperature in nitrogen ambiance.

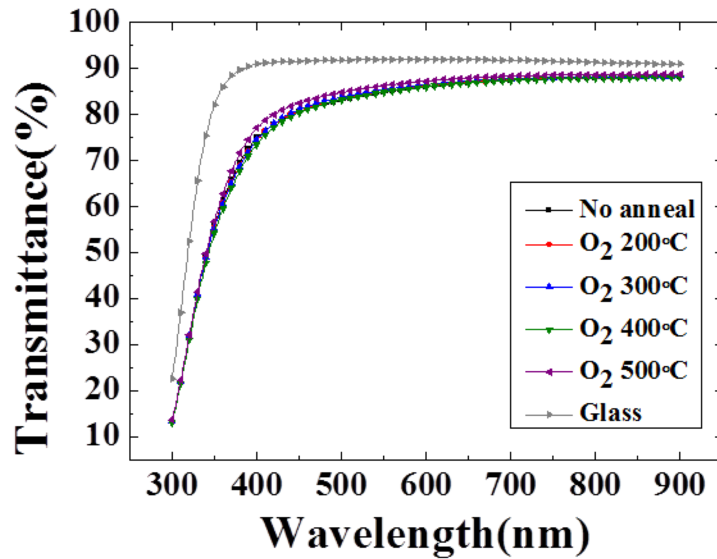


Figure 4-13 Optical transmittance spectra of IGZO thin films deposited on glass substrate with different annealing temperature in oxygen ambiance.

Figure 4-14 Photograph image of a 500°C annealed IGZO thin film on glass substrate placed on a logo.

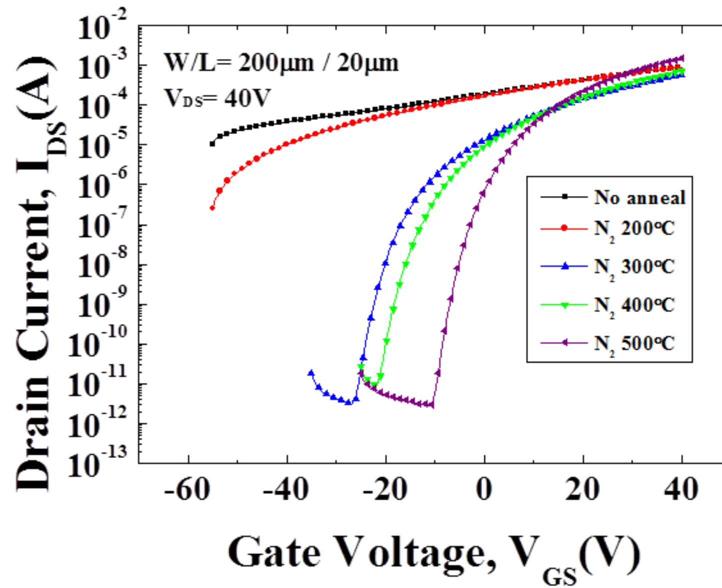


Figure 4-15 IGZO TFTs I_D-V_G curves with different annealing temperature in nitrogen ambiance.

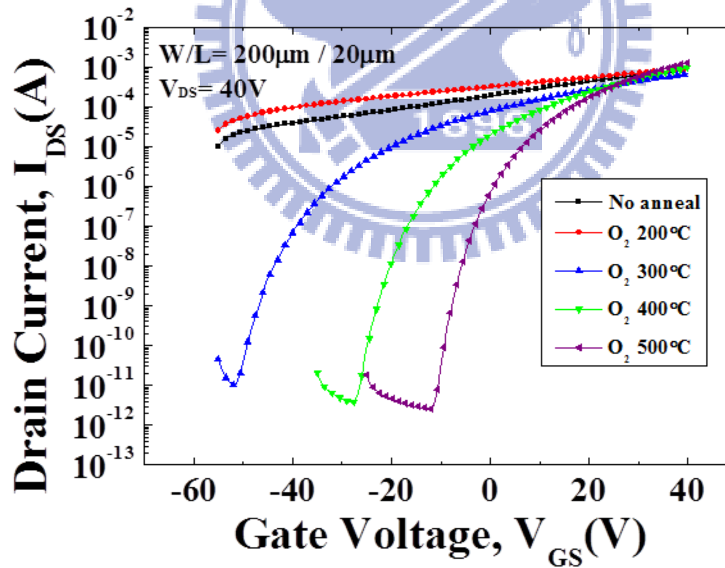
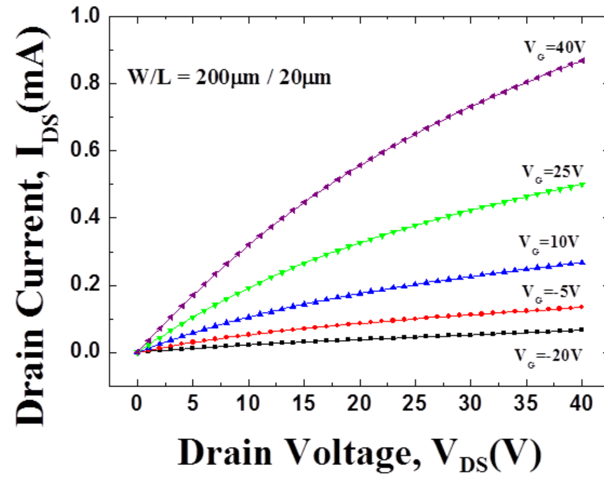
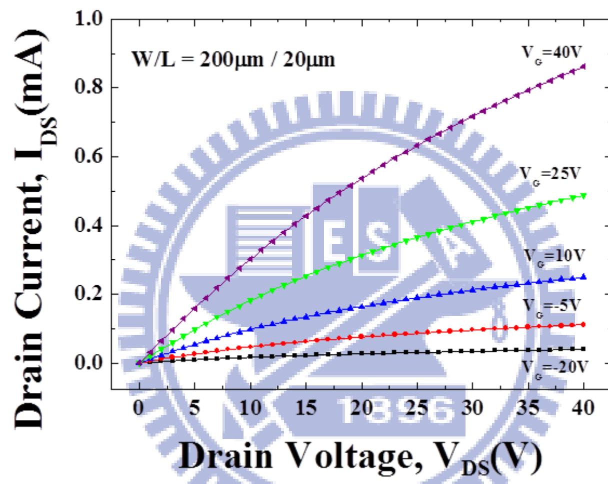


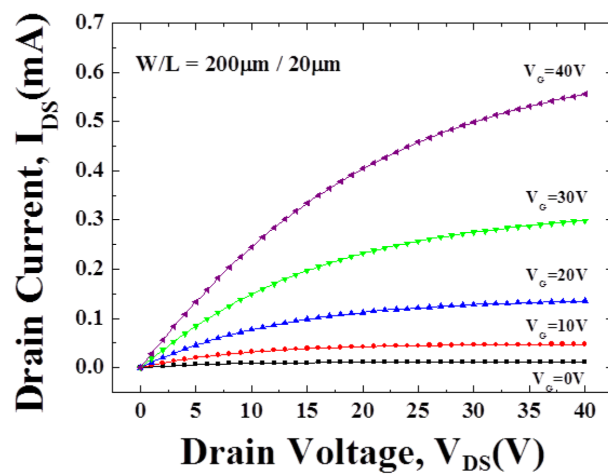
Figure 4-16 IGZO TFTs I_D-V_G curves with different annealing temperature in oxygen ambiance.



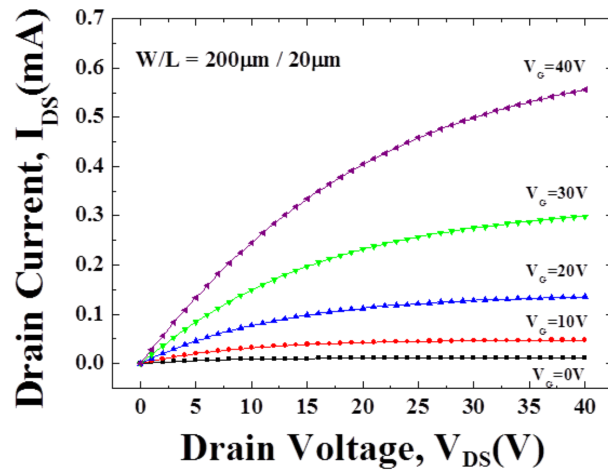
(a) No annealing



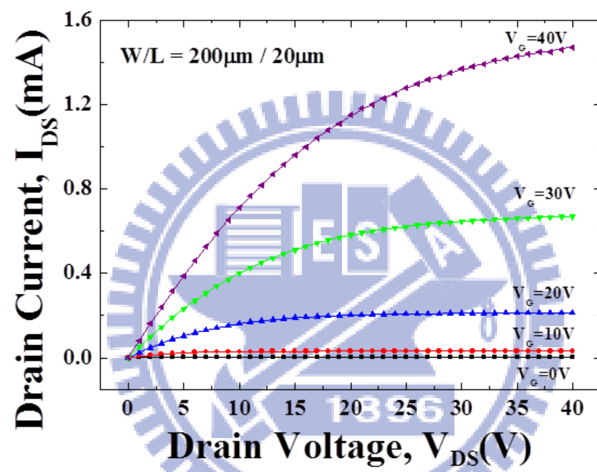
(b) 200°C in N_2



(c) 300°C in N_2

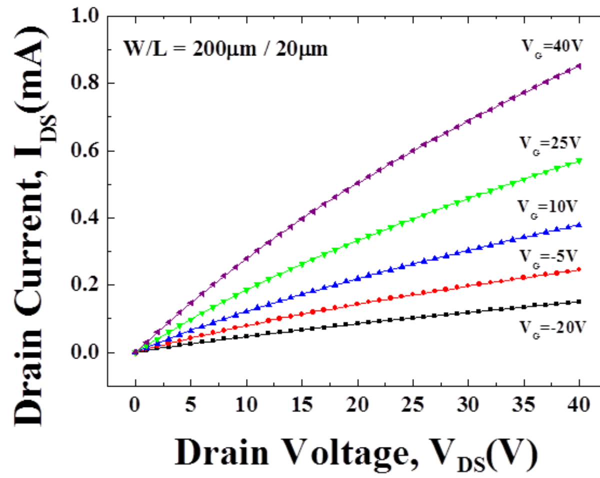


(d) 400°C in N_2

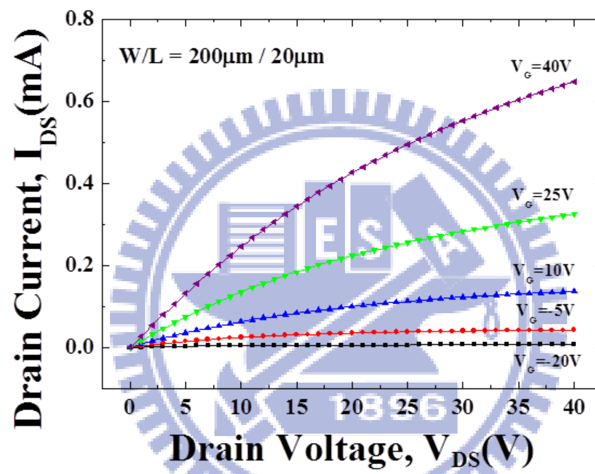


(e) 500°C in N_2

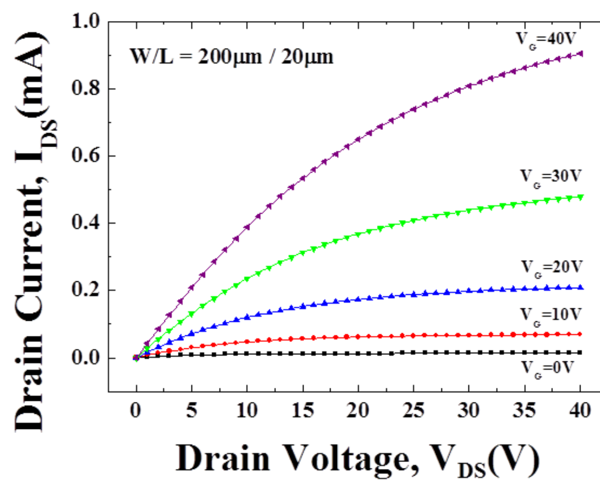
Figure 4-17 IGZO TFTs I_D-V_D curves with different annealing temperature in nitrogen ambiance (a) no annealed (b) 200°C (c) 300°C (d) 400°C (e) 500°C.



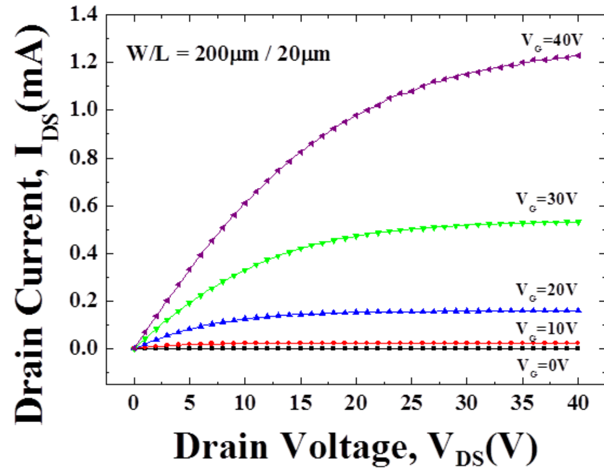
(a) 200°C in O_2



(b) 300°C in O_2



(c) 400°C in O_2



(d) 500°C in O_2

Figure 4-18 IGZO TFTs I_D-V_D curves with different annealing temperature in oxygen ambiance (a) 200°C (b) 300°C (c) 400°C (d) 500°C.

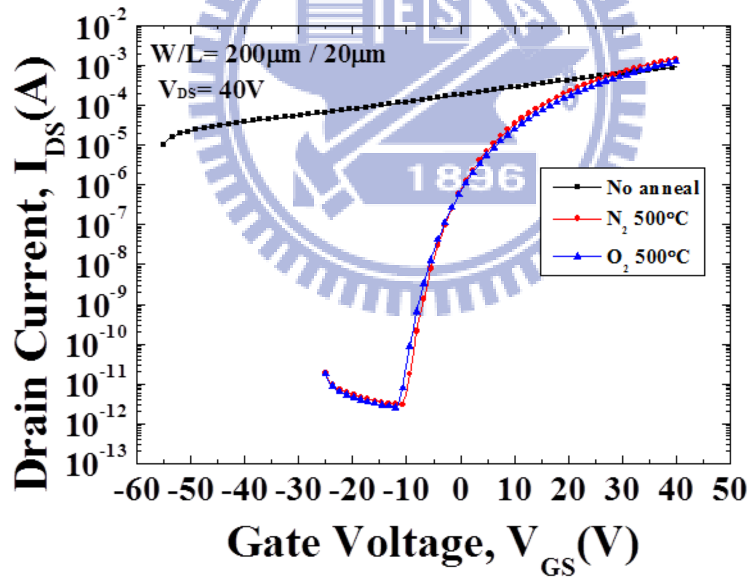


Figure 4-19 IGZO TFTs I_D-V_G curves with annealing temperature at 500°C in nitrogen and oxygen ambiance.

Table 4-3 Electrical properties of IGZO TFT with different annealing temperature in nitrogen ambiance

	Control	N_2-200°C	N_2-300°C	N_2-400°C	N_2-500°C
V_t (V)	-44.58	-29.79	-1.32	1.76	7.48
SS (V/dec.)	59.42	31.09	1.61	1.83	1.49
Mobility (cm^2/V-s)	0.81	1.35	2.49	3.58	10.39
I_{on}/I_{off} ratio	$8.99x10^1$	$3.58x10^3$	$1.88x10^8$	$7.63x10^7$	$5.13x10^8$

Table 4-4 Electrical properties of IGZO TFT with different annealing temperature in oxygen ambiance

	Control	O_2-200°C	O_2-300°C	O_2-400°C	O_2-500°C
V_t (V)	-44.58	-58.96	-19.00	0.81	8.72
SS (V/dec.)	59.42	78.25	2.63	2.05	1.65
Mobility (cm^2/V-s)	0.81	0.67	1.41	4.13	9.40
I_{on}/I_{off} ratio	$8.99x10^1$	$3.59x10^1$	$6.40x10^7$	$2.41x10^8$	$5.03x10^8$

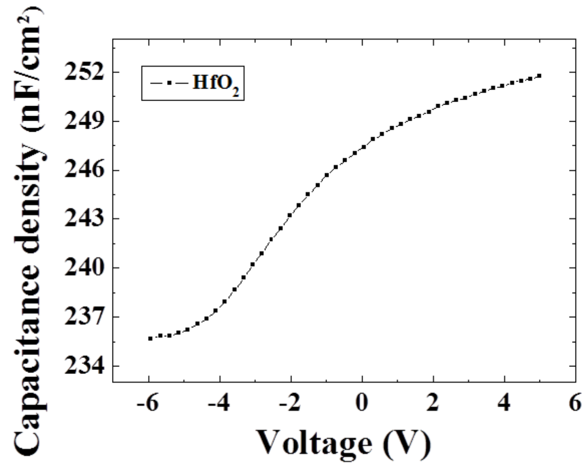


Figure 4-20 C-V characteristics of an Al/HfO_2/N^+Si capacitor.

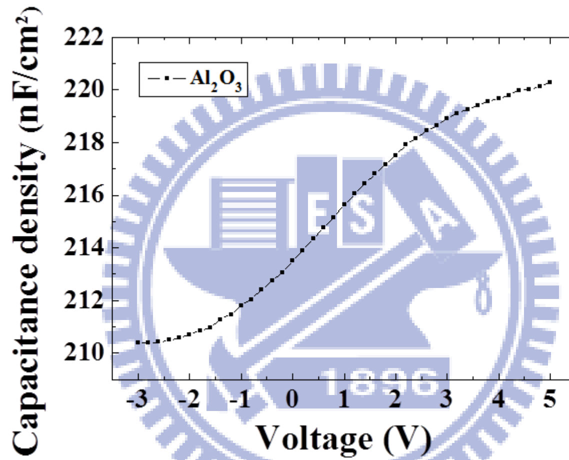


Figure 4-21 C-V characteristics of an Al/Al_2O_3/N^+Si capacitor.

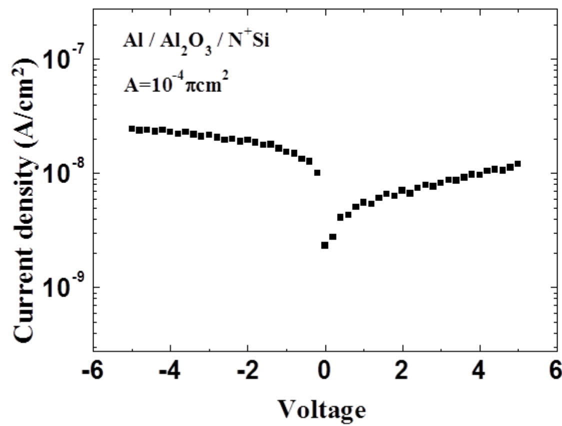


Figure 4-22 J-V characteristics of an Al/Al_2O_3/N^+Si capacitor.

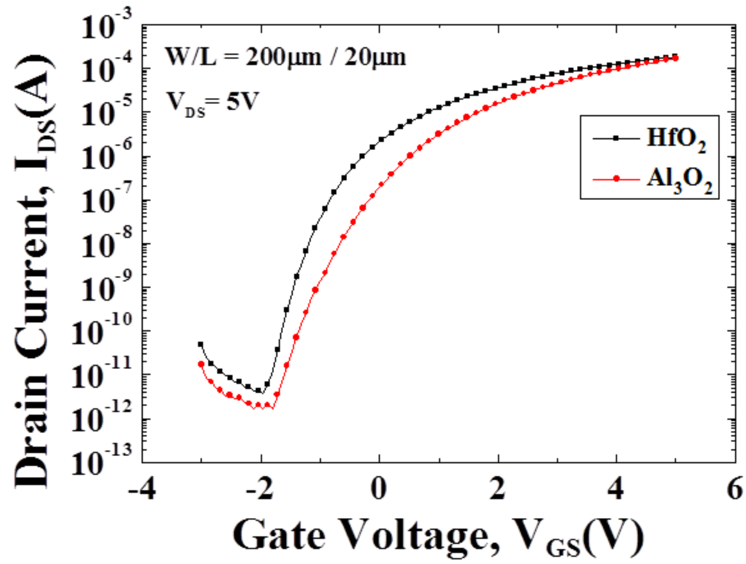


Figure 4-23 IGZO TFTs I_D-V_G curves with different gate dielectric of HfO_2 and Al_2O_3.

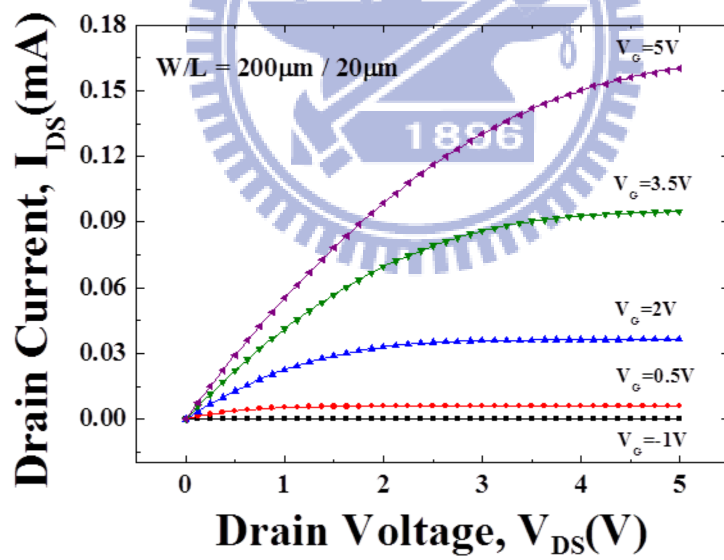


Figure 4-24 IGZO TFTs I_D-V_D curves with HfO_2 as gate dielectric.

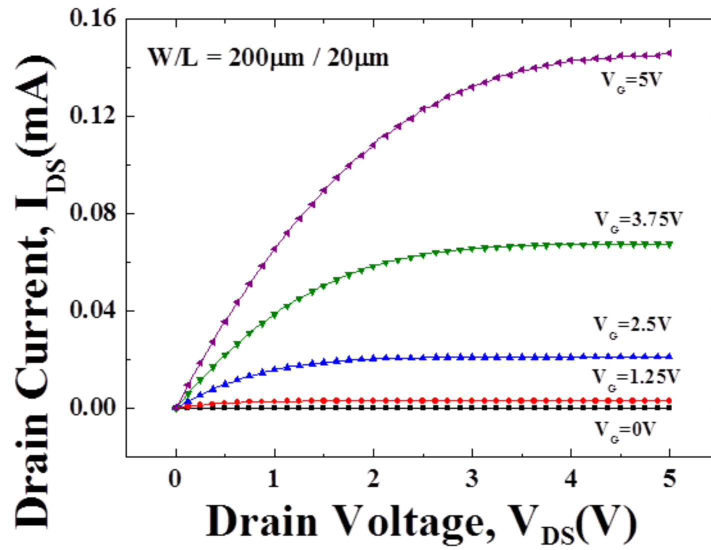


Figure 4-25 IGZO TFTs I_D-V_D curves with Al_2O_3 as gate dielectric.

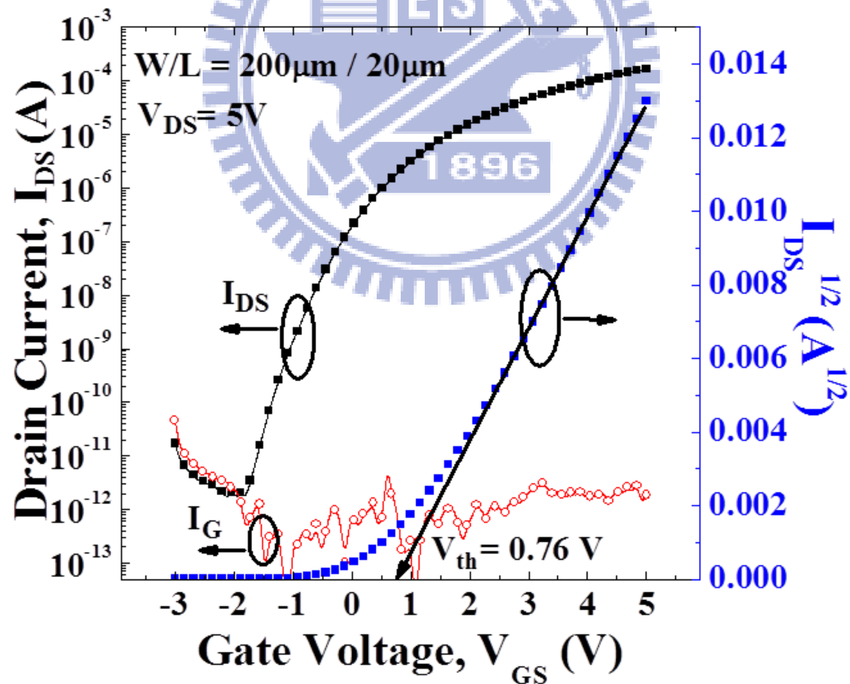


Figure 4-26 IGZO TFTs I_D-V_G, I_G-V_G and $I_D^{1/2}$-V_G curves with Al_2O_3 as gate dielectric.

Table 4-5 Electrical properties of IGZO TFT with high-*k* material as gate dielectric

	HfO_2	Al_2O_3
V_t (V)	-0.44	0.76
SS (V/dec.)	0.22	0.28
Mobility (cm^2/V-s)	5.14	8.60
I_{on}/I_{off} ratio	4.82×10^7	1.04×10^8

Table 4-6 Solution based IGZO TFTs electric properties.

	Deposition method	V_{th} (V)	Mobility (cm^2/V-s)	SS (V/dec.)	I_{on}/I_{off} ratio
APL(2010) [82]	Spin coating	8.1	5.8	0.28	6×10^7
EDL(2010) [83]	Spin coating	6.89	0.86	0.63	$\sim1\times10^6$
JECS(2009) [84]	Spin coating	7.8	0.96	1.39	$\sim1\times10^6$
APE (2010) [85]	Director transfer	0.9	3	0.86	4×10^5
TED(2011) [86]	Ink-jet printing	1	1.41	0.38	4.3×10^7
In this work	**APPJ**	**0.76**	**8.6**	**0.28**	$\mathbf{1\times10^8}$

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Chapter 5
Conclusions

We successfully deposited solution based indium-gallium-zinc oxide on oxide which covered with silicon wafer by atmospheric pressure plasma chemical vapor deposition system at room temperature.

The surface morphology and crystallinity of IGZO thin films were effectively improved after thermal treatment in nitrogen or oxygen ambiance because of the interface between semiconductor and insulator modification and local atomic rearrangement. And the IGZO thin films have an amorphous phase, even at a relatively high annealing temperature of 500°C.

The IGZO thin films deposited on glass which have highly transparent with above 80% transparency in the visible range because of the IGZO with wide band gap 3.78 eV.

Semiconducting IGZO thin films were deposited by APPJ and subjected to thermal annealing in nitrogen and oxygen respectively, leading to the successful fabrication of oxide TFTs. The IGZO TFT annealed at 500°C operated in enhancement mode and showed the better electrical properties including threshold voltage, subthreshold swing, mobility and on-off current ratio.

The TFTs with IGZO thin films as active layer which annealed in nitrogen or oxygen ambiance showed the similar performance. However we prefer to anneal IGZO thin films in nitrogen ambiance. When fabrication of transparent thin film transistor (TTFT), we must replace highly doping silicon with transparent conductor for gate electrode. When the IGZO thin films annealed in oxygen ambiance, the electrode would be oxidized. As a result, the TFTs electrical properties would be worse.

In the end, we expect to improve electrical properties of IGZO TFT which are low driving voltage and subthreshold swing. Therefore, we are going to substitute high-*k* material for SiO_2 as gate dielectric of TFTs. And the high-*k* dielectric materials which HfO_2 and Al_2O_3 are two of the most promising materials for gate dielectric of TFTs due to the properties of high dielectric constant, relatively low leakage current, low synthesis temperature, wide band gap sufficient to yield a positive band offset with respect to IGZO, and high transparency in visible range.

The IGZO TFT with HfO_2 as gate dielectric operated in depletion mode despite of good performance. However, we have successfully fabricated solution based IGZO TFTs with Al_2O_3 as gate dielectric shows promising results of low threshold voltage (V_{th} = 0.75 V), small subthreshould swing (SS = 0.28V/dec), high mobility (μ = 8.6 cm^2/V-s), and good I_{on}/I_{off} ratio of 1.04×10^8 and have great potential to be applied in the next generation flexible displays.

Chapter 6

Future works

It is well known that oxygen and water in the surrounding atmosphere affect the electrical characteristics of IGZO TFTs, Due to the charge transfer between the IGZO film and the adsorbed molecules, the adsorbed H_2O molecules enhance the conductance, while O_2 molecules adsorbed on the oxide surface lead to a decrease in conductivity in IGZO thin film. So we should cover passivation like SiO_2 or Si_3N_4 with IGZO surface to keep stability of TFTs characteristics.

In this paper, we only prepared solution based IGZO with atomic ratio of IGZO (In:Ga:Zn = 1:1:1). We can improve TFTs electrical characteristics to study different atomic ratio of IGZO as active layer in TFT, and achieve the best performance of device.

To reduce interface traps between gate dielectric and channel. High-k material as gate dielectric could be plasma treatment before deposited IGZO thin film. The TFTs electrical properties become better because the quality of interface between gate dielectric and channel has been improved.

In the future, the current of display market will highlight transparent products for convenient human live. Therefore, the transparent TFT plays

an important role of display technology. In this paper, we can transform the TFT to replace metal electrodes by TCO and fabricate transparent TFT with TCO as electrodes on glass substrate.

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