國　立　交　通　大　學

電子工程學系　　電子研究所碩士班

碩 士 論 文

一個十位元,每秒一千萬次取樣

低功率迴圈式類比數位轉換器

A 10bit, 10MS/s Low Power

Cyclic Analog to Digital Converter

研 究 生：陳建宏

指導教授：陳巍仁　教授

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研 究 生：陳建宏　　Student：Chien-Hung Chen

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國 立 交 通 大 學

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碩 士 論 文

A Thesis

Submitted to Department of Computer and Information Science

College of Electrical Engineering and Computer Science

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Master

in

Electronics Engineering

March 2012

Hsinchu, Taiwan, Republic of China

中華民國一〇一年三月

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摘　　要

操作在中速及中解析度之類比數位轉換器廣泛應用在可攜式電子產品中，其大約操作在每秒數十個百萬次的資料速度及 8 到 10 個位元解析度。在傳統倍乘數位類比轉換器架構中，運算放大器是最消耗功率的部分。本篇論文提出一個更節能的迴圈式類比數位轉換器的解決方案，每個轉換步驟 3.5 位元輸出加快轉換速度，以及在最後兩個處理週期使用時序重置技術以節省更多時間。此外背景校準電路無須額外的殘值放大器，可降低功率消耗和晶片面積。

本提出的迴圈式類比數位轉換器以 85nm CMOS 製程實作完成，晶片面積為 0.96×0.715 平方毫米。其可操作在每秒 10 個百萬次的資料速度及 10 位元解析度，量測結果顯示其微分和積分非線性誤差分別為+0.55/-0.82LSB 和+1.6/-1.5LSB。類比電路操作在 1.2 伏特工作電壓，而數位電路操作在 1 伏特工作電壓，整體功率消耗約 1.1 毫瓦，其 FOM 值達 0.45pJ/conv.-step。

A 10bit, 10MS/s Low Power Cyclic Analog to Digital Converter

Student: Chien-Hung Chen Advisors：Dr.Wen-Zen Chen

Department of Electronic Engineering National Chiao Tung University

ABSTRACT

ADCs which operate middle speed and medium resolution are widely applied in portable electronic devices. It is about several tens of MS/s and 8 to 10bit resolution. In conventional MDAC architecture, the operational amplifier is the largest consumer of power. The thesis presents a solution of the more power-efficient cyclic ADC. To speed up the conversion rate, there is 3.5bit conversion step, and the timing re-scheduled technique is utilized to save more time in the last two cycles. Besides, background calibration without extra residue amplifier to reduce power and chip area.

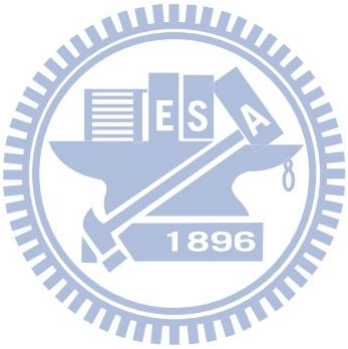
The proposed cyclic ADC has been fabricated in a 85nm CMOS technology, the chip size is $0.96\times0.715mm^2$. It can operate in 10MS/s and 10bit resolution. Experimental results reveal that the DNL and INL are +0.55/-0.82LSB and +1.6/-1.5LSB respectively at 10 MS/s. Analog circuits are operated under a 1.2V supply, and digital circuits are operated under a 1V supply. Total power dissipation is 1.1mW. The corresponding FOM (Figure of Merit) is 0.45pJ/conv.-step.

誌　　謝

兩年多的碩士班終於要畫下句點，在求學過程中遇到不少貴人的幫忙，感謝曾經指導過我、幫助過我的人，讓我在求學路上如此順利。感謝曾經批評過我、指責過我的人，因為你們的一句話，讓我有所成長。感謝老師、實驗室的同儕們，與你們互相切磋、學習，讓我在專業知識上有增長。感謝我的家人在我背後默默的付出，沒有你們就沒有今天的建宏。

最後，謝謝老天爺，我畢業了。

陳建宏 2012/3/19



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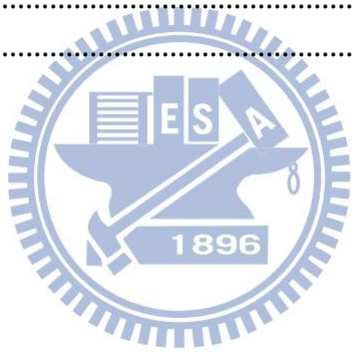

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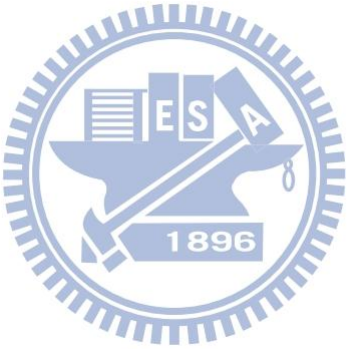


CHAPTER 1

INTRODUCTION

1.1 Motivation

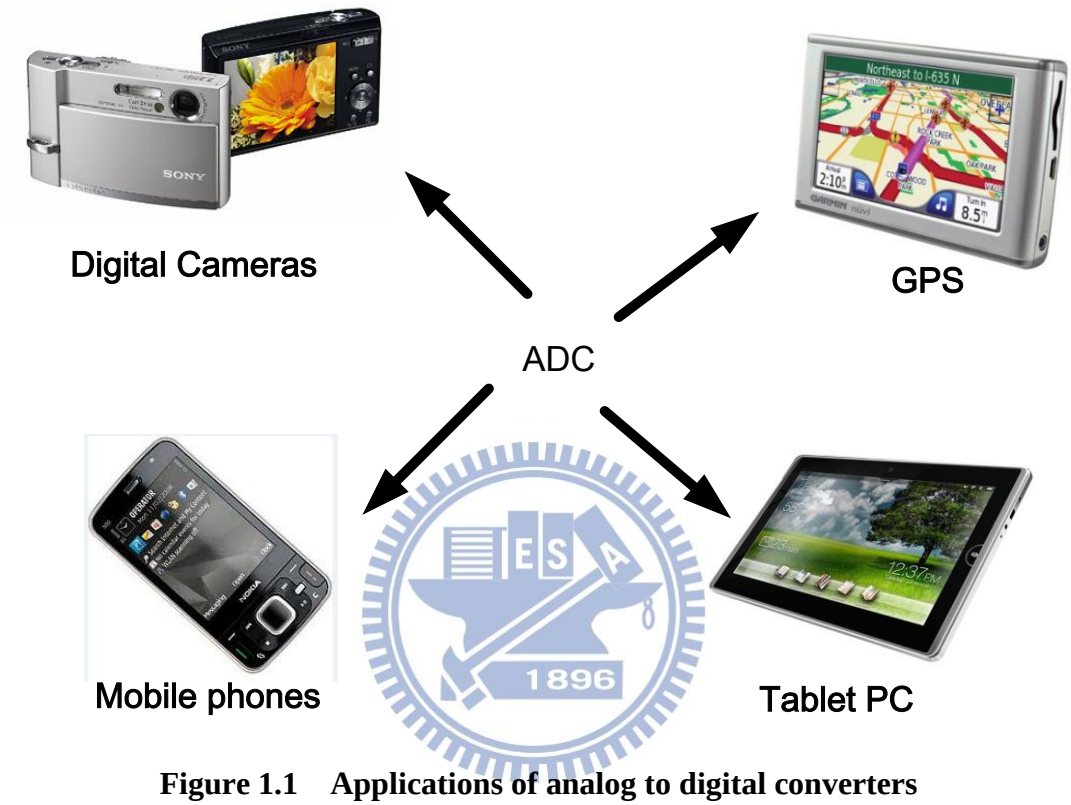


Figure 1.1 Applications of analog to digital converters

Based on the technology development, the portable devices and consumer electronics products are more popular in recent years. The characteristics of the products are light, small, and lasting. With the improvement of the techniques for semiconductor fabrication, the CMOS integrated circuits carry the advantages of faster speed and less power dissipation in a variety of applications.

Many of the communication systems today utilize the digital signal processing to resolve the transmitted information. Therefore, an analog-to-digital interface to connect discrete-time domains and continuous-time is required. Analog-to-digital converter (ADC) is one of the most important circuits, which achieves the digitization

of the received waveform, comes from physical world. To evaluate ADC's performance, the figure-of-merit (FOM) is defined as equation (1.1). Figure 1.2 [1] shows the surveys of ADC from 1997 to 2012, where ENOB means effective number of bit.

$$FOM = \frac{Power}{2^{ENOB} \times Conversion\ rate} \tag{1.1}$$

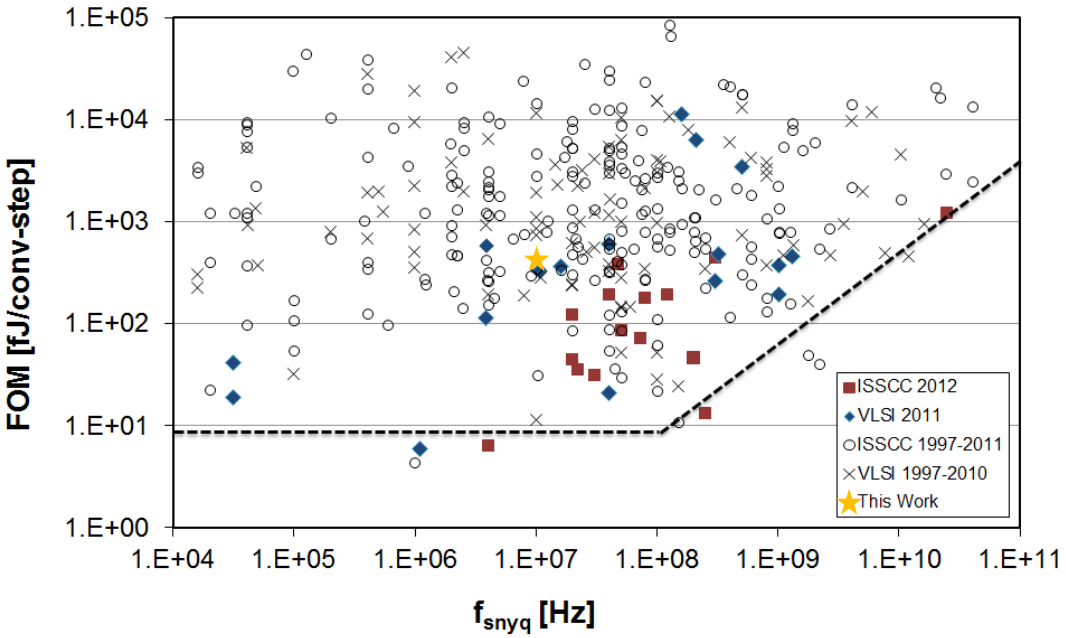


Figure 1.2 ADC performance survey from 1997 to 2012

Among many types of CMOS ADC architectures, a cyclic architecture achieves power-efficient consumption and chip area under middle sampling frequency and resolution which is about several tens of MS/s and 8 to 10bit. Low-power small-area ADCs with 10bit resolution and several tens of MS/s sampling rate are the significant components in battery-operated commercial applications including data communication and image signal-processing systems.

In this research, the power consumption is expected to be as low as possible

under 1.2 V power supply in whole circuit. A 10bit 10MS/s cyclic ADC has been designed and implemented with standard TSMC 85nm CMOS 1P6M process, and the total power consumption is about 1.04mW.

1.2 Thesis Organization

This thesis is organized into six chapters.

In Chapter 1, the motivation and the organization are briefly described. In Chapter 2, the fundamental concepts of analog-to-digital conversion and performance metrics used to characterize ADCs are introduced. Then the several ADC architectures are review, including flash ADC, successive-approximation-register (SAR) ADC, pipelined ADC, and cyclic ADC. The end of the chapter draws the summary.

In Chapter 3, the multiplying DAC (MDAC) is reviewed. The design issue is discussed in detail. Chapter 4 describes the detail design of each building block. The circuits used in the low-power cyclic ADC are presented. Among them are flip-around sample and hold, residue amplifier, comparators, calibration circuit, and timing re-scheduled clock generator. Then, transistor level simulated results of each circuit are shown.

Chapter 5 shows the experimental results, including the chip layout, the system simulation results, and the measurement considerations. The measurement results for the cyclic ADC fabricated in a standard TSMC 85nm CMOS technology are summarized.

In Chapter 6, the conclusions of this work are summarized. Additional directions and recommendations for future study are also suggested.

CHAPTER 2

NYQUIST RATE A/D FUNDAMENTALS

2.1 Introduction

In this chapter, the first describes the concept of analog-to-digital conversions and discusses some important performance characteristics to judge the Analog-to-digital converters (ADC). The second, it introduces some conventional ADC topologies and draws summary, including flash ADC, successive-approximation-register (SAR) ADC, pipelined ADC, and cyclic ADC.

2.2 ADC Performance Characteristics

The ADC converts the continuous analog signal to discrete digital codes for digital signal processing (DSP) in the next stage. Typically, the ADC divides the input analog signal into several sub-ranges, and converts to digital number proportional to the magnitude of the input analog signal during the process of conversion. ADCs are characterized by some different ways to indicate the performance, including resolution, SNR, SFDR, SNDR, dynamic range, DNL, and INL. Actually, the ADC has some non-ideal effects which cause performance to degrade.

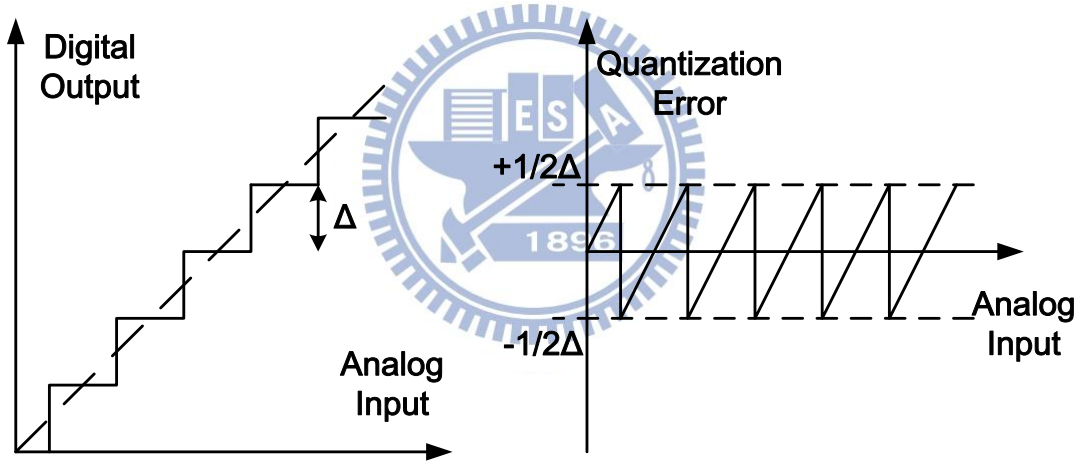
2.2.1 Resolution

Resolution indicates the number of discrete levels it can produce over the range of analog value. It describes the quantization accuracy of the ADC, which is also named as effective number of bits (ENOB). In other words, the higher resolution ADC means the more sub-ranges that input range is divided. In general cases, resolution is defined as the base 2 logarithm of sub-ranges and always affected by

noise and nonlinearity in circuits.

2.2.2 Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is defined as the power ratio of the signal to background noise at the ADC output. The ideal transfer characteristic curve of ADC is shown in figure 2.1(a). Figure 2.1(b) shows the quantization error which is the difference between actual analog value and quantized digital value. It defined as the difference between the dash line and the output signal in figure 2.1(a). The quantization error range is between $+\frac{1}{2}\Delta$ and $-\frac{1}{2}\Delta$.



(a) **(b)**

Figure 2.1 (a) Transfer characteristic curve (b) Quantization error

q(k) is the quantization noise due to quantization process. As figure 2.2(a) shows, quantizer can be model as input signal added by quantization noise. The symbol Δ presents the value of 1LSB expressed as equation (2.1). A_{FS} is full scale range of signal. N is the number of bits. By assumption, the quantization noise, *q(k)*,

is a uniformly distributed random variable between $+\frac{1}{2}\Delta$ and $-\frac{1}{2}\Delta$. In figure 2.2(b), it shows that the probability density function, *pdf(q)*, is a constant value between $+\frac{1}{2}\Delta$ and $-\frac{1}{2}\Delta$ and is independent of the sampling frequency f_s and input signal. The probability density function of the quantization error is expressed as equation (2.2).

$$\Delta = \frac{A_{FS}}{2^N} \tag{2.1}$$

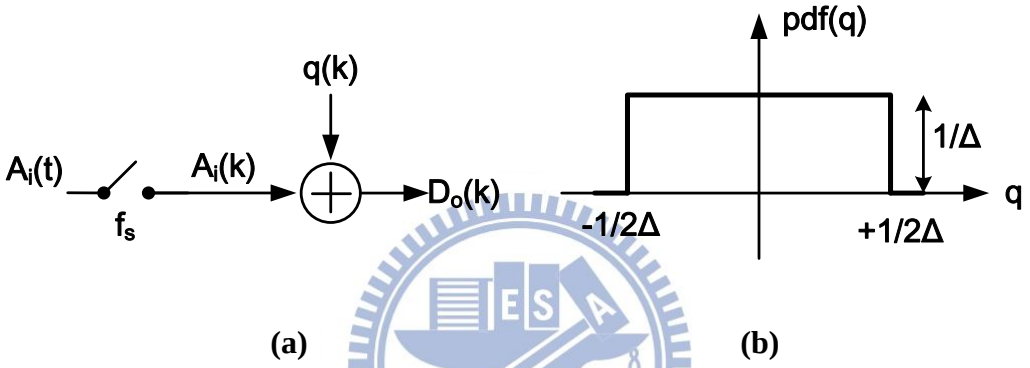


Figure 2.2 (a) Quantizer model

(b) The probability density function of the quantization error

$$pdf(q) = \left\{ \begin{array}{ll} \frac{1}{\Delta}, & -\frac{\Delta}{2} < q < \frac{\Delta}{2} \\ 0, & otherwise \end{array} \right\} \tag{2.2}$$

Hence, the quantization noise power is

$$P_{noise} = \overline{q^2} = \int_{-\infty}^{\infty} q^2 pdf(q) dq = \frac{1}{\Delta} \int_{-\frac{1}{2}\Delta}^{\frac{1}{2}\Delta} q^2 dq = \frac{\Delta^2}{12} \tag{2.3}$$

Assume that signal is a sinusoidal waveform and the amplitude is V_{Swing}. Thus, the signal power is

$$P_{signal} = \frac{V_{Swing}^2}{2} \tag{2.4}$$

Then, the SNR can be derived

$$SNR = 10\log_{10}\left(\frac{P_{signal}}{P_{noise}}\right) = 10\log_{10}\left(\frac{\frac{V_{Swing}^2}{2}}{\frac{\Delta^2}{12}}\right) = 10\log_{10}\left(6\frac{V_{Swing}^2}{\Delta^2}\right) \quad (2.5)$$

When the signal amplitude V_{Swing} is equal to $\frac{V_{FS}}{2}$, the maximum value of SNR is expressed as equation (2.6).

$$SNR_{\max} = 6.02 \times N + 1.76(dB) \quad (2.6)$$

The equation (2.6) shows the relation between SNR and the number of bit. As N increases by one, the SNR specification increases by 6dB. For example, SNR requires at least 62dB for 10 bit ADC.

2.2.3 Spurious Free Dynamic Range (SFDR) and Signal-to-Noise and Distortion Ratio (SNDR)

When a single frequency sinusoidal signal is applied to an ADC input, the ADC output usually contains a signal component at the input frequency. Due to distortion, it also contains signal components at harmonics frequency. Otherwise, quantization error is also injected to output during conversion. As the figure 2.3 shows, the output signal consists of three components, input signal, distortion and noise level. The spurious free dynamic range (SFDR) is the ratio of the fundamental signal component to the largest distortion component. The signal-to-noise and distortion ratio (SNDR) is the ratio of the signal power to the total noise and harmonic distortion power.

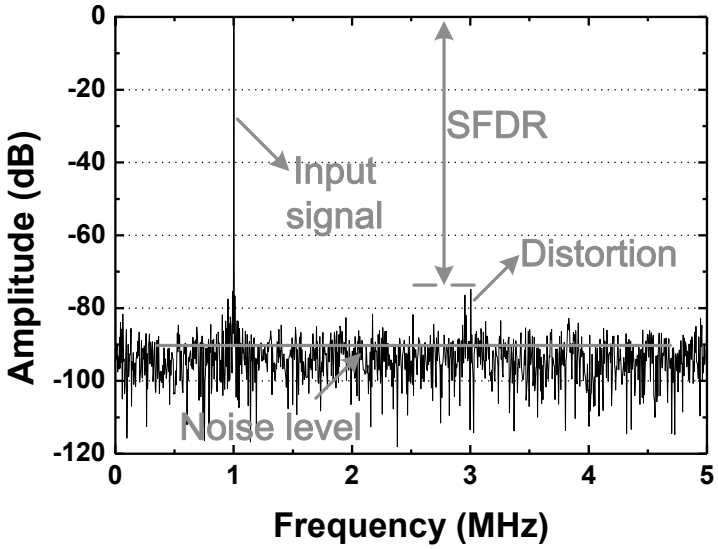


Figure 2.3 Frequency domain plot

2.2.4 Dynamic Range

Dynamic range is another performance for ADCs. It is defined as the ratio of the input signal level for maximum SNR to the input signal level for 0dB SNR. It means the range of input signal amplitudes for which useful output can be obtained from whole system. Figure 2.4 illustrates a plot of SNR versus input level. When the signal to noise ratio is 0dB, it means that it is the minimum detectable input signal power. If the noise power is independent of the level of the signal, the dynamic range is equal to the SNR at full scale. However, the noise power increases as the signal level increases in some cases. Therefore, the maximum SNR is less than dynamic range that degraded by the noise and the harmonic distortion.

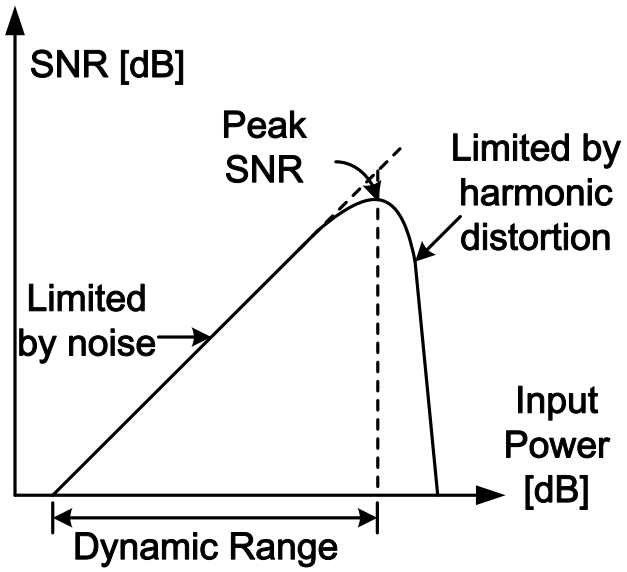
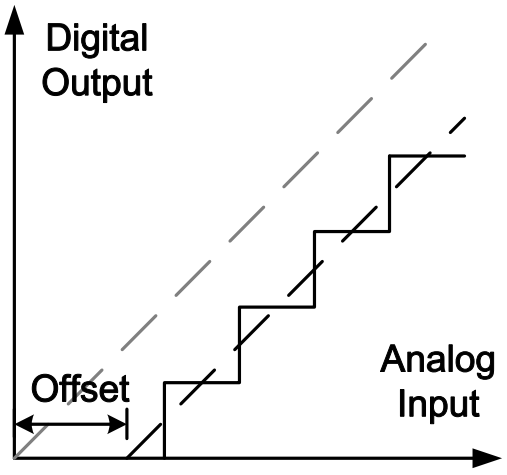


Figure 2.4 SNR versus input power

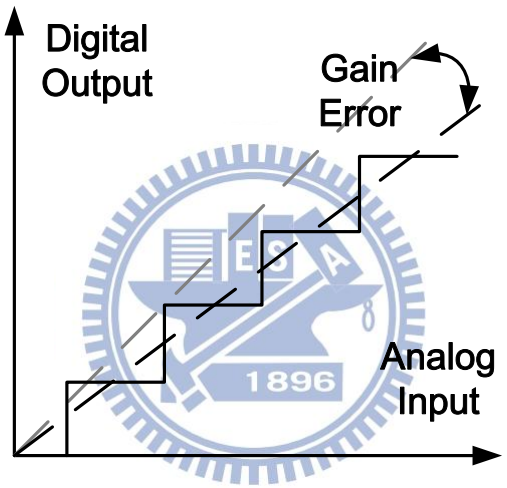
2.2.5 Non-ideality

The ideal ADC transfer characteristic progresses from low to high in series of uniform steps that approximates a straight line when the ramp signal is inputted the ADC. However, the transfer characteristic has several non-idealities such as offset, gain error, and non-linearity shown on the figure 2.5(a), (b) and (c) respectively.

In figure 2.5(a), the offset means the transfer curve shifts by a constant amount. And in figure 2.5(b), the transfer curve slope is not equal to ideal, which is named gain error. In figure 2.5(c), the non-linearity describes transfer curve steps are not uniform. These non-idealities may be caused by device mismatching, sampling capacitor mismatching, and insufficient gain of the operational amplifier. Usually, offset and gain error are tolerable in some applications.



(a)



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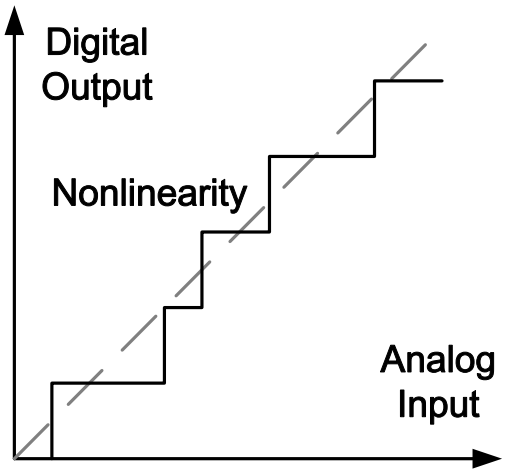


(c)

Figure 2.5 (a) Offset (b) Gain error (c) Non-linearity

2.2.6 Differential Non-Linearity (DNL) and Integral Non-Linearity (INL)

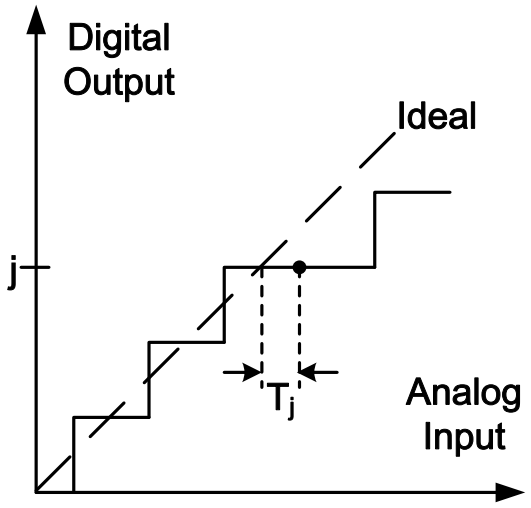
Both Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) are important parameter for linearity. DNL is defined as the difference between a real quantization step and an ideal quantization step. In other words, it is a term describing the deviation between two successive conversional values corresponding to adjacent input values. Figure 2.6(a) illustrates DNL, which can be expressed as equation (2.7). It cannot be smaller than -1. If DNL is equal to -1, a code is missing.

$$DNL(D_j) = \frac{S_j - \Delta}{\Delta} \text{ (LSB)} \tag{2.7}$$

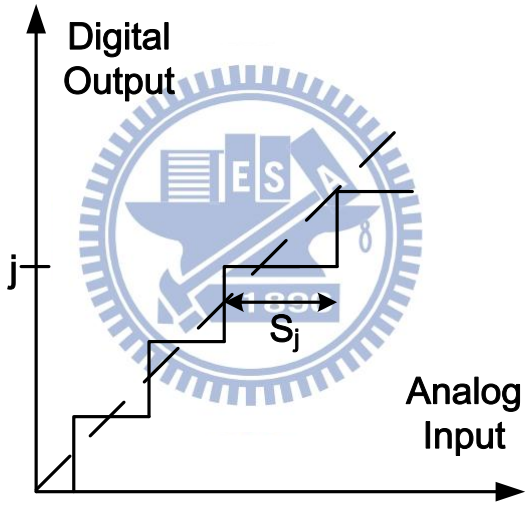
INL is defined as the deviation from the ideal slope of the ADC and the center of the real quantization step. It describes the difference between the actual transfer characteristic and the ideal transfer characteristic. Figure 2.6(b) illustrates INL, which can be expressed as equation (2.8).

$$INL(D_j) = \frac{T_j}{\Delta} \text{ (LSB)} \tag{2.8}$$

DNL and INL are both plotted as a function of code, and are usually expressed in terms of least significant bits (LSB) of the input.



(a)



(b)

Figure 2.6 (a) DNL (b) INL

2.3 ADC Architecture

2.3.1 Flash ADC

Flash ADC is the fastest architecture among all the ADCs. In Figure 2.7, the flash scheme includes a comparator array, a resistor string and an encoder. For *N*-bit resolution, it needs at least 2^N-1 comparators to distinguish the analog input from these 2^N-1 quantization levels. Every comparator compares the analog input with the reference voltage usually generated by resistor string which is connected between V_{REF} and $-V_{REF}$ to construct the overall reference voltages. If the analog input is larger than the reference voltage, the output of comparator is "1". Otherwise, the output of comparator is "0". Then the thermometer code is converted to *N*-bit binary code by a logic circuit, which also contains the functions for solving sparkle and metastability issues.

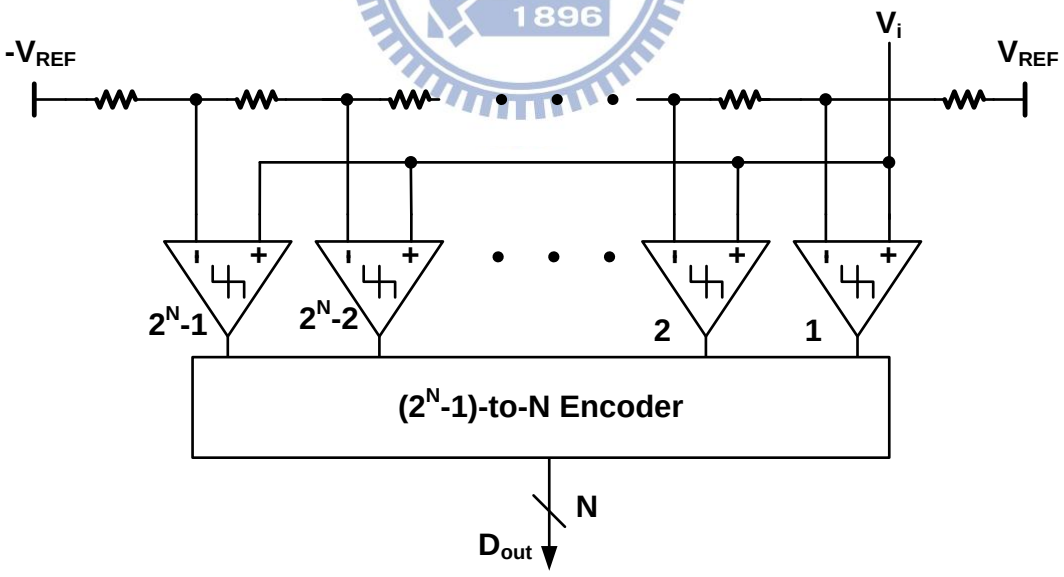


Figure 2.7 Flash ADC architecture

The flash ADC is favored for high speed converters since there is only one comparing cycle used. In other words, the number of comparators grows exponentially with the number of bits. On the other hand, increasing the quantity of the comparators enlarges the whole area and the power consumption dramatically. Additionally, the tolerable offset of the comparator become very small for high resolution application. It is a critical point in the circuit design, so it can be only applied in the low resolution. Thus several architectures are proposed, like subranging ADC and two-step ADC. These architectures are used to achieve higher resolution applications and reduce power consumption.

2.3.2 Pipelined ADC

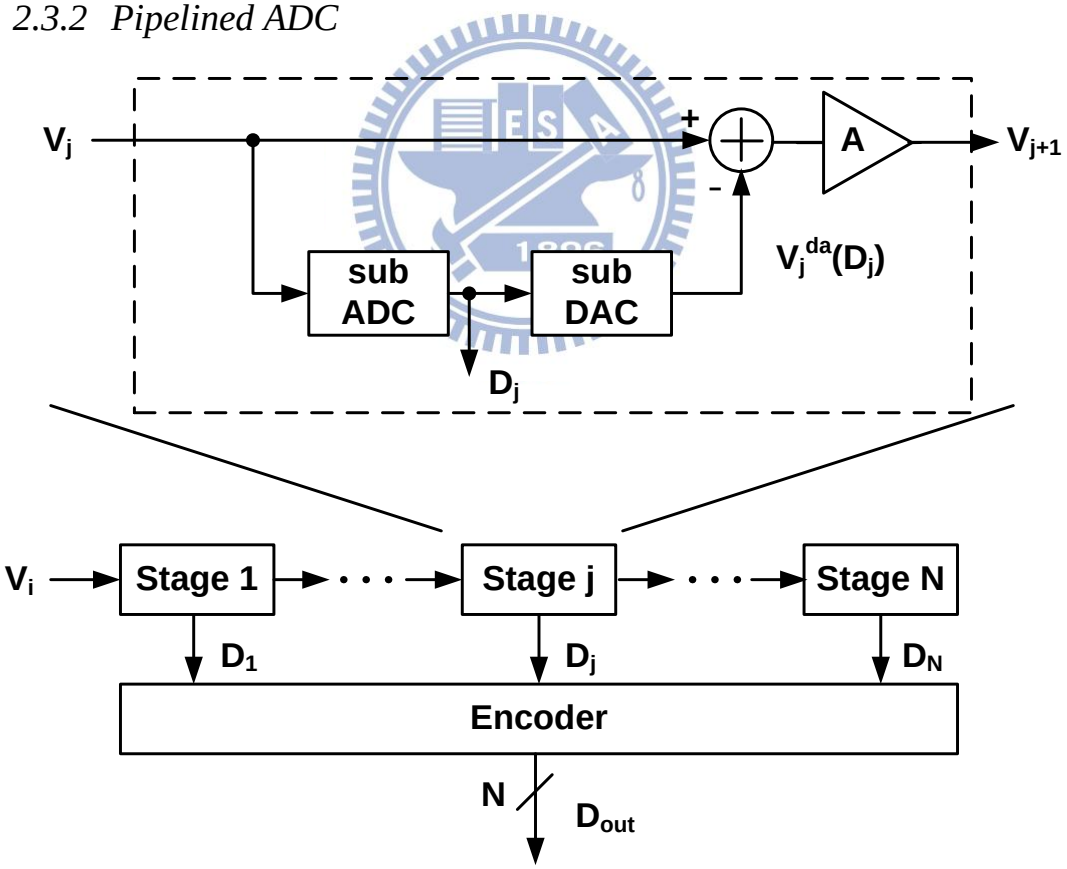


Figure 2.8 Pipelined ADC architecture

The block diagram of the pipelined ADC is shown in the figure 2.8. It consists of N stages, each including a sample-and-hold (SHA) circuit, a sub-ADC, a sub-DAC, subtraction, and a residue amplifier. Within each stage, the input signal from last stage is sampled and held. The SHA circuit takes more accurate data to reduce aperture jitter which happens from the instantaneous value of the analog input. After the SHA circuit, the analog input signal is quantized by a coarse sub-ADC. Then the sub-DAC adopts the appropriate reference voltage subtracted from original input signal to generate the residue signal. The residue signal is amplified and applied to the next stage for finer conversion. After the amplification, the first stage can start sampling a new analog input signal. All stages operate as same as the first stage. Finally, the digital outputs are collected by encoder to generate the final digital output.

2.3.3 Successive-Approximation-Register ADC

The block diagram of successive-approximation-register (SAR) ADC is shown in Figure 2.9(a). An *N*-bit SAR converters utilizes only one comparator with N-times quantization to complete a full conversion, which is similar to the pipelined ADC. At first, input signal compares with the reference voltage V_{da} which is the half of the full scale of signal. Then the comparison result is applied to the control logic, and it generates the appropriate V_{da} in the next sub-range. The quantization sequence is shown in Figure 2.9(b). The ADC repeats the procedure until the LSB is decided. The higher resolution need more quantization cycles. It has been a limitation in high speed operation. In recent years, a new topology of SAR ADC is proposed. Asynchronous technique is used to archive high speed operation.

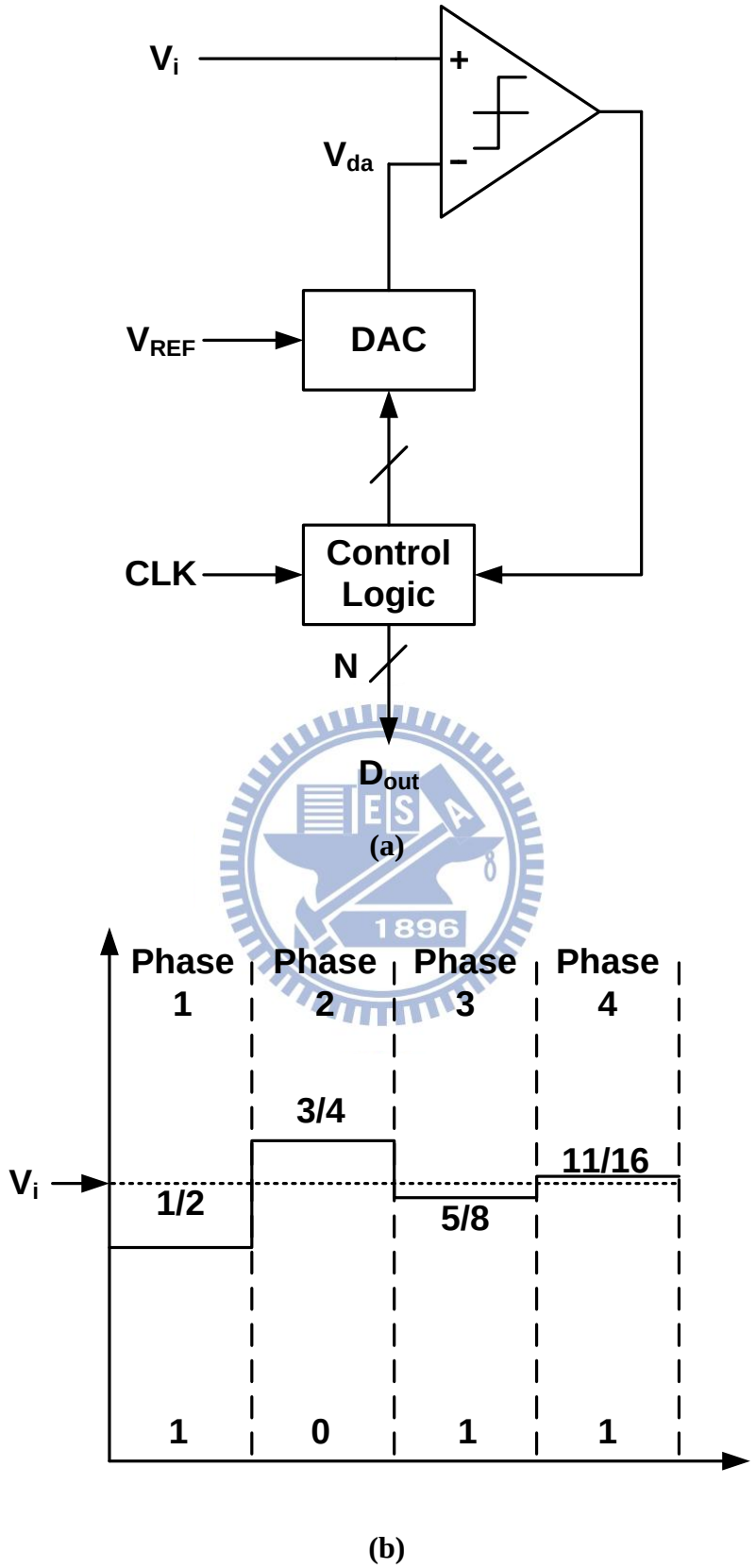


Figure 2.9 (a) SAR ADC architecture (b) Quantization sequence

2.3.4 Cyclic ADC

A cyclic ADC operates the same as a single stage pipelined ADC shown in the figure 2.10. When the conversion is finished in the clock cycle, the residue signal is amplified feedbacks to the input. Then the cyclic ADC converses the data again. Generally speaking, the cyclic ADC can reach the resolution as the pipelined ADC. The stage conversion time is also the same as the pipelined ADC, but the throughput rate is much less than the pipelined ADC. Even if the sampling rate is less than the pipelined ADC, the cyclic ADC takes advantages in hardware and power consumption because of only one stage is reused repeatedly. Therefore it is used for middle speed applications. In addition, the cost is more expensive in advanced CMOS technologies. Because the cyclic ADC can archive small area, it is advantage to cost down in advanced CMOS technologies in middle speed applications.

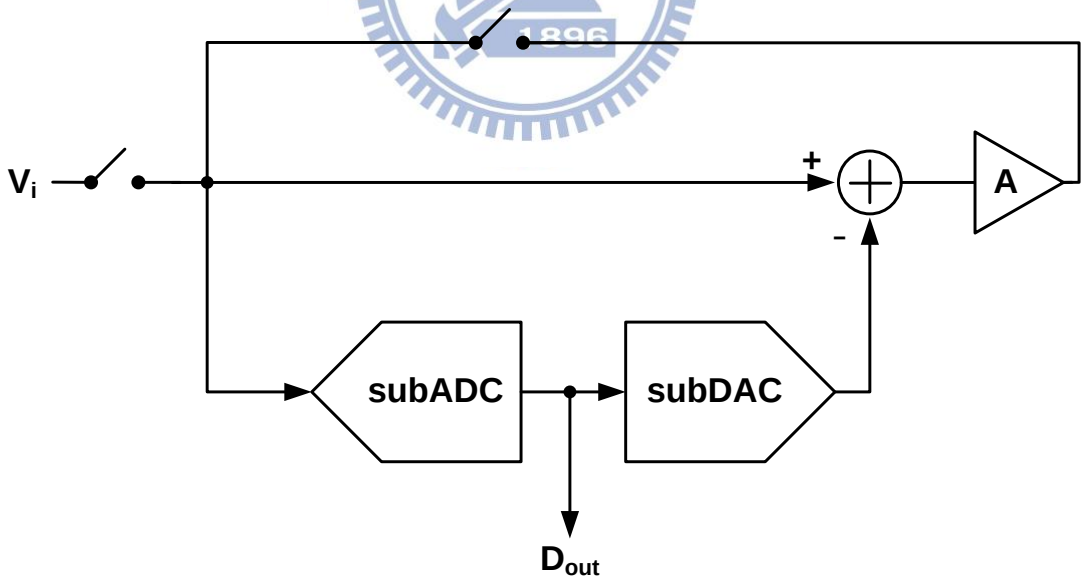


Figure 2.10 Cyclic ADC architecture

2.4 Summary

In this chapter, some ADC architectures are introduced. Base on operation of these ADCs, two categories are applied: flash architecture based and pipelined architecture based.

Flash ADC is the typical ADC of flash architecture based used to achieve high speed application. However, the power consumption and chip area increase dramatically for high resolution application. Due to the bottleneck of flash ADC, some architecture such as subranging ADC [3] or two-step ADC [4] are proposed. These architectures are similar to flash ADC and are used to achieve higher resolution requirement with lower power consumption.

Pipelined architecture based is contrast to the parallel operation, using N times quantization to complete a full conversion. It consists of pipelined ADC, SAR ADC and cyclic ADC. These Architectures can achieve higher resolution rather than flash ADC. However, the operational amplifier of pipelined ADC and cyclic ADC is the block of the most power consumption. Some power-efficient techniques are proposed such as double sampling, using open loop amplifier [6][9], capacitive charge pump [11] and opamp sharing [15]. In recent year, a new architecture, asynchronous SAR ADC [12][13], is popular to implement high speed application and more energy-efficient.

CHAPTER 3

CONVENTIONAL MULTIPLYING DAC

3.1 Introduction

In this chapter, the digital error correction and design issues of conventional multiplying DAC (MDAC) which is used for cyclic ADC and pipelined ADC will be discussed.

3.2 Digital Error Correction

The comparator is commonly used for in the most of the ADC. In pipelined ADC and cyclic ADC, the analog input is compared with the reference voltage by the comparator, and the residue is amplified to the full scale as the input range. For 1 bit conversion stage, the ideal stage gain is 2. The ideal transfer curve in 1bit conversion stage is shown in figure 3.1(a). If the input signal V_j is larger than zero, the output of comparator is "1". Otherwise, the output of comparator is "0". Then appropriate reference voltage is subtracted from the input signal V_j and the residue is amplified to the full scale $\pm V_r$.

However, the offset of the comparator is an issue to affect the accuracy of the comparison result. The transfer curve with comparator offset is shown in figure 3.1(b). It will bring out the wrong comparison result and cause the amplified residue overflow in the next stage. The influence will produce the missing code and degrades the performance of the ADC.

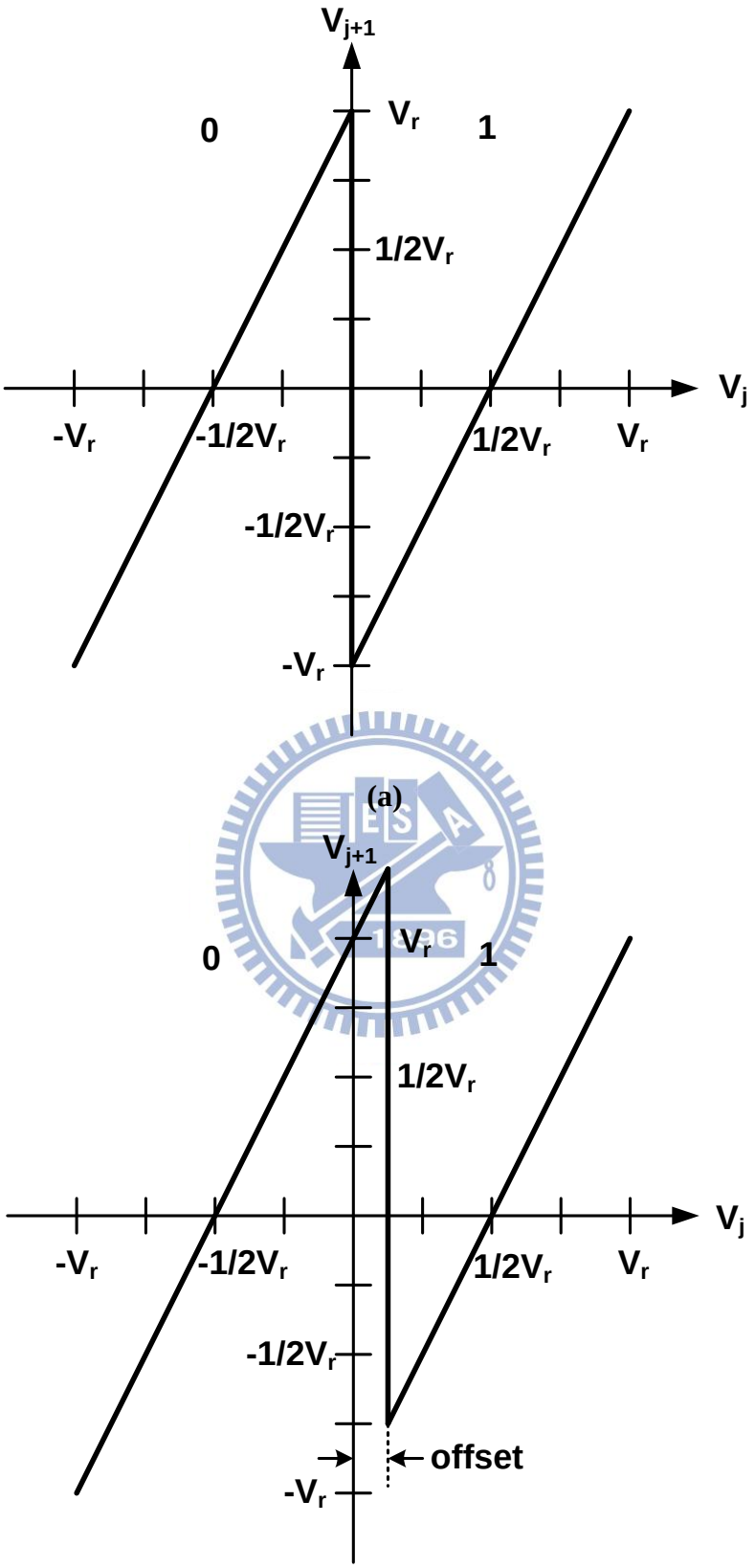


Figure 3.1 (a) Ideal 1 bit transfer curve (b) 1 bit transfer curve with offset

The digital error correction is utilized to tolerate the offset of the comparator without producing missing code. There are 2 comparators, which judge the analog input voltage to three quantization levels, “00”, “01” and “10”. Figure 3.2 shows the 1.5 bit transfer curve. In the next stage, the residue is still amplified to the full scale and compared with the same reference voltage. Afterward, imposing the digital codes from the first stage and the next stage can obtain the accurate 2 bit digital codes.

The tolerance of offset can reach up to ±1/4 V_{ref}. In other words, the digital codes in digital error correction do not produce missing codes. Due to the tolerable offset, this technique is extensively utilized.

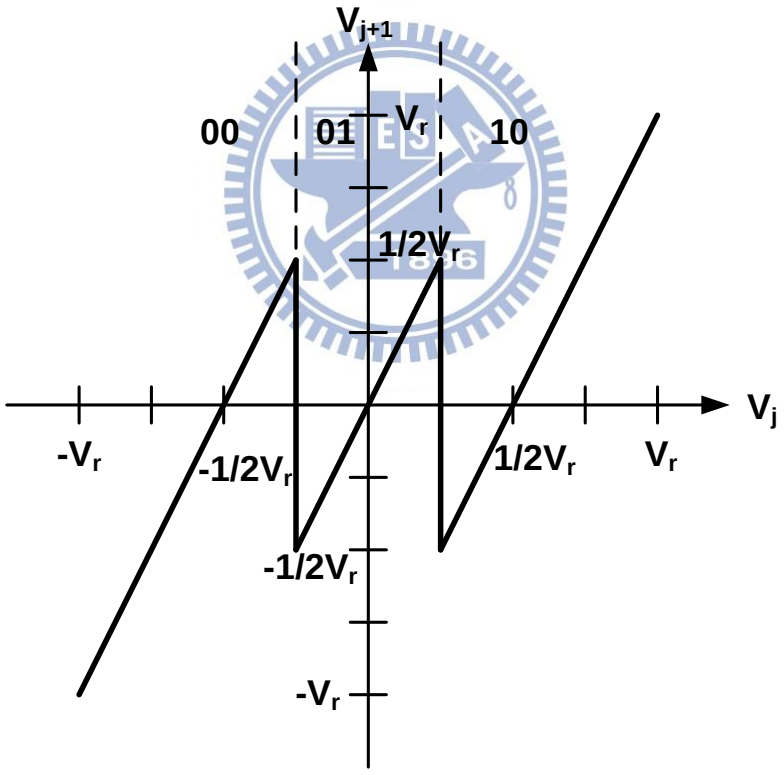


Figure 3.2 Ideal voltage transfer curve in 1.5bit ADC

3.3 Multiplying DAC(MDAC) Design

MDAC scheme is frequently adopted in pipelined and cyclic ADC because it is simple and includes full functions with the sub-DAC, the subtraction, and the amplification of the remainder. MDAC has two main specifications, accuracy and speed requirements. The accuracy requirement is dominated by the open-loop gain of the operational amplifier. The speed requirement is dominated by the unity-gain bandwidth of operational amplifier and the feedback factor. However, both the requirement of accuracy and speed are depend on the resolution in this stage and remained resolution in the next stage.

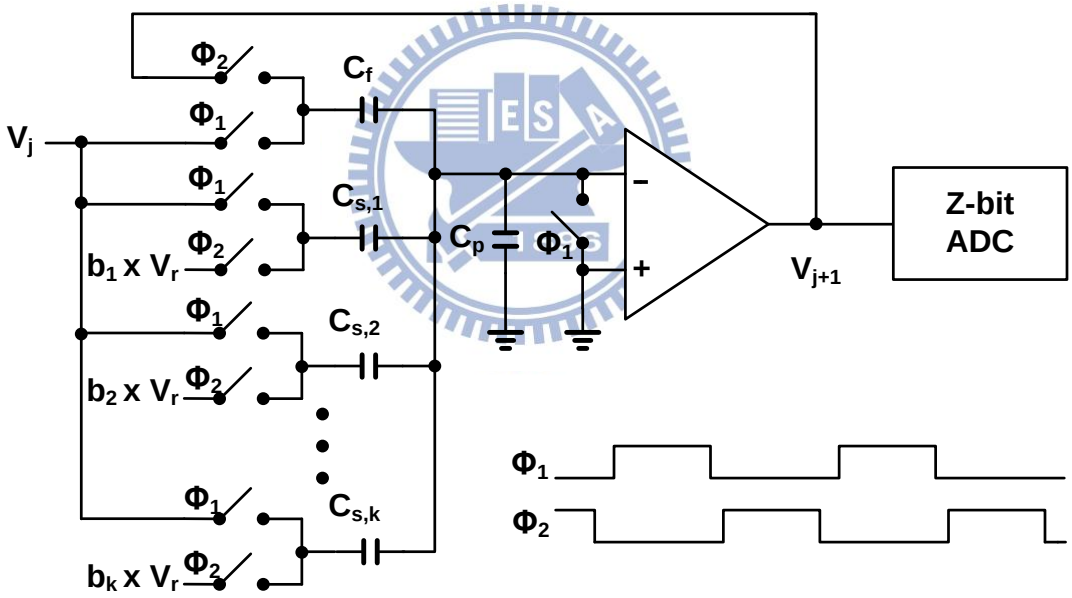


Figure 3.3 Conventional Multi-bit MDAC scheme and timing diagram

In the figure 3.3, the conventional MDAC are shown. In phase Φ1, the input V_j is sampled to both capacitors $C_{s,k}$ and C_f. At the same time, the operational amplifier is in reset. Then in phase Φ2, the operational amplifier operates in negative feedback, and the appropriate reference voltage from sub-DAC is switched to the capacitor $C_{s,k}$.

According to the charge redistribution, the transfer function between V_{j+1} and V_j is expressed as equation (3.1). The parameter ε is the error term shown in equation (3.3). It caused by the finite gain of the operational amplifier. The feedback factor β in closed-loop of MDAC is shown in equation (3.4), which C_p is the parasitical capacitor in the input of the operational amplifier.

$$V_{j+1} = \frac{1 + C_S / C_f}{(1+\varepsilon)} \left(V_j - A_j^{da}(D_j) \right) \tag{3.1}$$

$$C_s = \sum_k C_{s,k} \tag{3.2}$$

$$\varepsilon = \frac{1}{A} \left(\frac{C_S + C_f + C_P}{C_f} \right) \tag{3.3}$$

$$\beta = \frac{C_f}{C_S + C_f + C_P} \tag{3.4}$$

$$A_j^{da}(D_j) = V_r \sum_k \left(b_k \frac{C_{s,k}}{C_S + C_f} \right) \tag{3.5}$$

D_j is the output of subADC.

$$D_j = \{b_1, b_2, \ldots b_n\} \qquad b_k \in \{-1, 0, +\} \tag{3.6}$$

If the C_s and C_f are assumed identical to C, then the equation (3.1) could be simplified to the equation (3.7). When the error term ε is ignored, the equation (3.7) will be the ideal transfer function in a radix 2 stage.

$$V_{j+1} = \frac{2}{(1+\varepsilon)} \left(V_j - \frac{D_j}{2} V_r \right) \tag{3.7}$$

This gain error term should be less than 1LSB of the next stage resolution (Z-bit) to prevent the mistakes made by the finite gain of the operational amplifier. To resolve M-bit resolution in the j-th stage, the gain requirement of the operational amplifier can be expressed as equation (3.9).

$$\frac{C_S + C_f}{C_f} = 2^M \tag{3.8}$$

$$A > 2^{Z+M}\left(1 + \frac{1}{2^M}\frac{C_p}{C_f}\right) \tag{3.9}$$

The equation of the speed requirement for the operational amplifier is derived below. By assuming that the MDAC in hold mode is a single pole system and ignoring the slewing behavior. The settling error of a single pole system can be derived as equation (3.10).

$$e^{-T_{settle}/\tau} < 2^{-Z} \tag{3.10}$$

$$\tau = \frac{1}{2\pi f_u}\frac{C_f + C_s + C_p}{C_f} \tag{3.11}$$

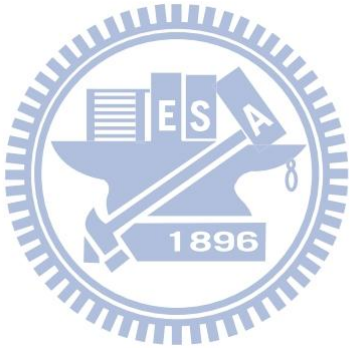
T_{settle} is the time in hold mode. τ is the closed-loop settling time constant. f_u is the unity-gain bandwidth of the operational amplifier in MDAC. Then the constraint of unity-gain bandwidth could be expressed as

$$f_u > 2^M \cdot Z\left(1 + \frac{1}{2^M}\frac{C_P}{C_f}\right)\frac{\ln 2}{2\pi T_{settle}} \tag{3.12}$$

From the equation (3.9) and (3.12), the gain and unity-gain bandwidth of the operational amplifier in MDAC can be well defined.

However, the operational amplifier in MDAC is usually the largest consumer of power in pipelined ADC or cyclic ADC. Due to constraint of feedback factor, the power consumption increases dramatically in high speed design. On the other hand, in pipelined ADC, the operational amplifier can be scaled for different stage, but it cannot be scaled in cyclic ADC. It is not power-efficient. For example, a 10bit 10MS/s cyclic ADC and 3.5bit conversion step, the gain and bandwidth requirements of operational amplifier are larger than 60dB and 600MHz, which are derived from equation (3.9) and (3.12).

In order to reduce power consumption, more power-efficient architectures are proposed. There are switched-opamp [20], opamp reuse [15], and opamp-less architecture [6][9][11]. Using switched-opamp, it can save about 50% power, but the operational speed is limited due to the turn-on delay. The opamp reuse is another power-efficient architecture. But there are some drawbacks, memory effect and complex control switch. Opamp-less architecture can save more power, but it usually require complex calibration circuit. In this work, a new power-efficient architecture is proposed. The details of proposed cyclic ADC will be introduced in next chapter.



CHAPTER 4

CIRCUIT DESIGN

4.1 Cyclic ADC Design

4.1.1 Design Issue

In this design, in order to propose low power consumption and efficiency of chip area, several techniques are implemented.

Generally, the cyclic ADC is operated lower than ten mega samples per second because there is only one or two stages hardware used which is less than in the pipelined ADC. Otherwise, the operational amplifier in MDAC will be difficult to design to operate in higher sampling rate. There are some challenges in gain-bandwidth and power consumption trade-off. In order to reduce the power consumption of the cyclic ADC, removing the input sample-and-hold circuit is one solution. Without sample-and-hold, aperture jitter will be induced. It is because the voltages caught by comparators and sub-DAC are not identical at the same time. This kind of error will lead to the wrong result and shift codes to the next stages, especially in the neighborhood of the reference voltage in comparators.

In this design, MDAC circuit is replaced to the flip-around SHA and residue amplifier. This architecture could relax the design requirement and reduce power consumption in operational amplifier. On the other hand, to enhance the total conversion rate, this work is adopted to produce 3.5bit per conversion step and timing re-scheduled technique.

4.1.2 Architecture

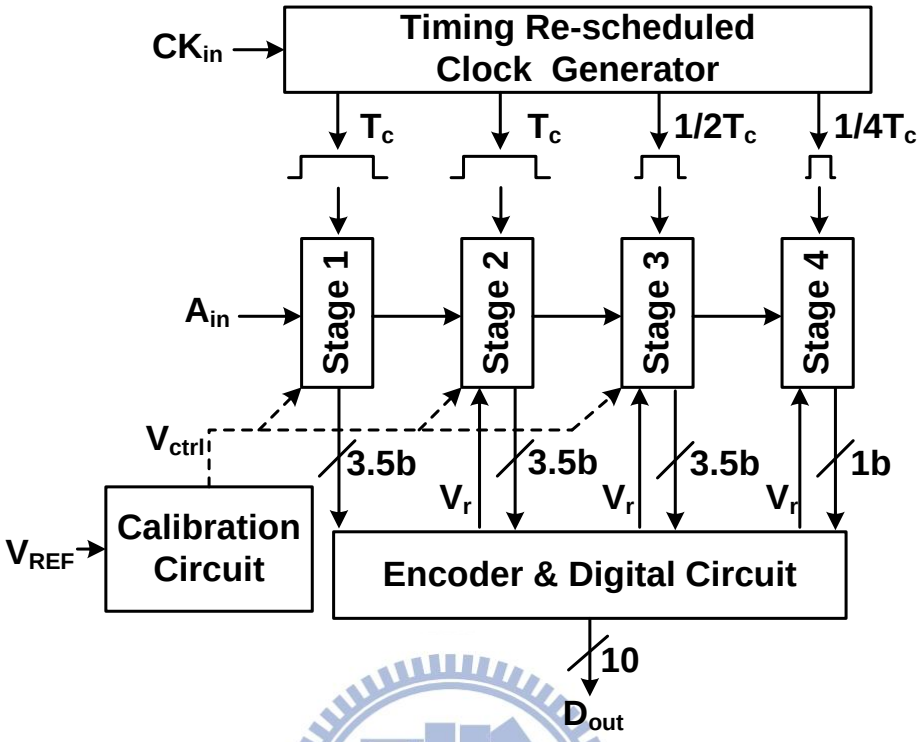


Figure 4.1 The proposed cyclic ADC architecture

Figure 4.1 shows the proposed cyclic ADC architecture. There are several techniques including the conventional MDAC replaced by flip-around SHA and residue amplifier, multi-bits processing, and timing re-scheduled technique are adopted to reduce power consumption and enhance the efficiency of the chip area. Because this work is used to process 3.5bit every conversion cycle, the calibration circuit is added to ensure the voltage gain of the residue amplifier is 8. In the end of the total conversion, 10bit digital codes will be produced.

The clock generator provides asynchronous clock pulse. The conversion time of the first 2 stages are longer, and the third conversion time is half of the first 2 stages. Then in the last conversion time is half of the third stage again. The timing re-scheduled technique could enhance the speed without extra power.

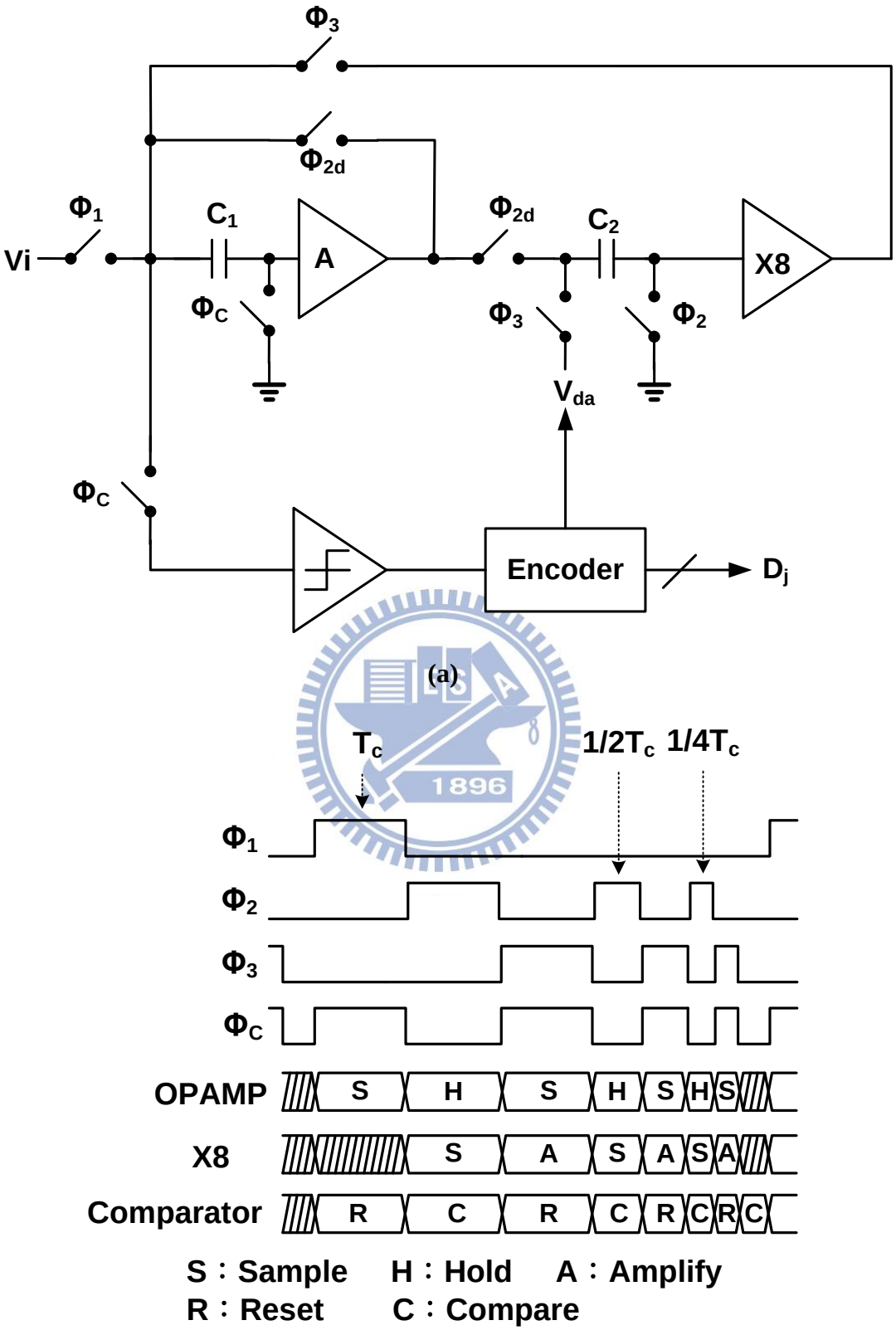


Figure 4.2 (a) The proposed cyclic ADC scheme (b) Timing diagram

The proposed cyclic ADC scheme and the timing diagram are shown in the figure 4.2. At the phase Φ1, the flip-around sample and hold circuit samples analog input signal. At the phase Φ2, the sampled signal is held and compared with the reference voltages by comparators. Later, the appropriate voltage is provided from the comparing result to be subtracted with the sampling voltage at the phase Φ3. Then the residue voltage after subtracting will be amplified by the residue amplifier. Then repeat the operation between amplifying and subtracting, until the last comparing cycle is finished. The details of each block in cyclic ADC will be introduced subsequently.

4.2 Each Block of Cyclic ADC

4.2.1 Flip-Around Sample And Hold

Considering quantization noise and thermal noise, the SNR can be expressed by equation (4.1). It is 62dB for 10bit resolution. The thermal noise should be less than quantization noise. The plot of SNR versus sampling capacitor is shown in figure 4.3. The full scale is 700mV and resolution is 10bit. The sampling capacitor is 500fF in this design.

$$SNR = 10\log\frac{\frac{1}{2}V_{FS}^2}{\frac{\Delta^2}{12}+\sigma^2} = 10\log\frac{\frac{1}{2}V_{FS}^2}{\frac{\left(2V_{FS}/2^N\right)^2}{12}+\frac{KT}{C}} \qquad (4.1)$$

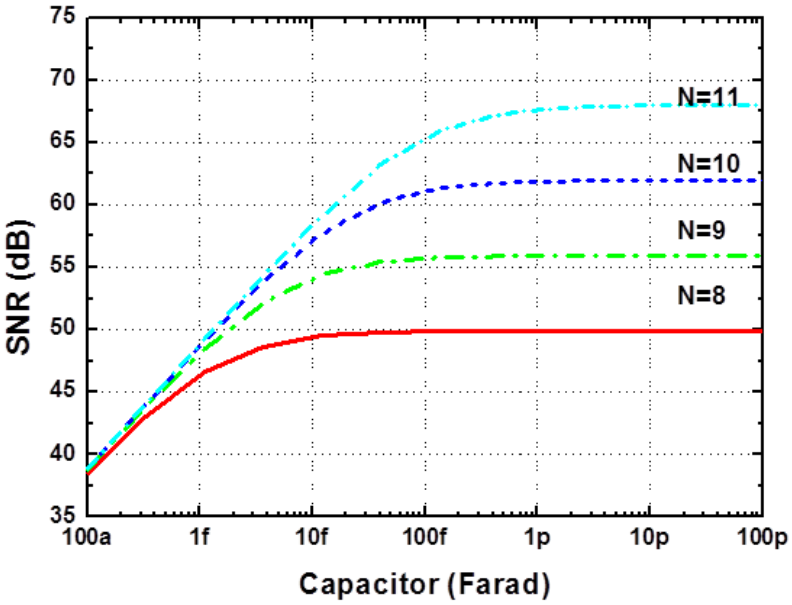


Figure 4.3 SNR versus sampling capacitor

On the other hand, the operational amplifier is the most critical circuit of flip-around sample and hold. The accuracy is determined by the dc gain of the operational amplifier, and the speed is determined by the unity-gain bandwidth. The proposed architecture relaxes the requirement of unity-gain bandwidth of the operational amplifier, and reduces the power consumption to achieve low power application.

The closed-loop gain of operational amplifier can be expressed by equation (4.2). The feedback factor β could be defined as the ratio between the feedback capacitor and sampling capacitor. Because the feedback capacitor is the same as sampling capacitor in the proposed architecture, β is about 1.

$$A_{close} = \frac{1}{1+\frac{1}{A\beta}} \tag{4.2}$$

$$\varepsilon_r = \frac{1}{A\beta} < \frac{1}{2^N} \tag{4.3}$$

According to the specification of the proposed cyclic ADC, the gain error

should be smaller than 1LSB. Therefore, the gain requirement of operational amplifier should be larger than 60dB.

On the other hand, the closed-loop step settling time is

$$T_{settle} = \tau_a \ln\left(\frac{1}{\varepsilon}\right) \tag{4.4}$$

To achieve ε been smaller than 1LSB, the unity-gain bandwidth can be expressed by equation (4.5).

$$f_u > \frac{N \ln 2}{2\pi T_{settle}} \tag{4.5}$$

Thus, the frequency requirement of operational amplifier is about 100MHz.

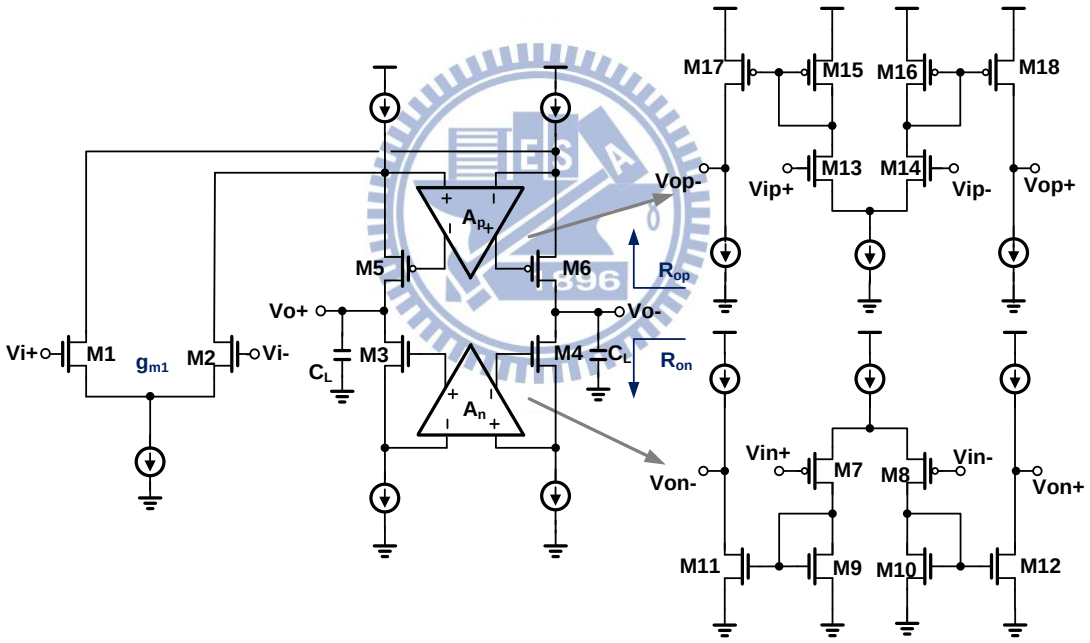


Figure 4.4 Gain boosting folded-cascode operational amplifier scheme

Due to lower transistors intrinsic gain in advanced CMOS technologies, the gain boosting folded-cascode operational amplifier shown in figure 4.4 is adopted. The dc gain of the gain boosting folded-cascode operational amplifier is

$$A_0 = g_{m1}(R_{op} \parallel R_{on}) \approx (g_m r_o)^3 \tag{4.6}$$

Because transistors intrinsic gain is about 25dB, the gain of the operational amplifier can provide over 60dB satisfied the specification of the cyclic ADC. On the other hand, the operational amplifier only has one dominant pole at the output. It can be stable in the closed loop without frequency compensation.

$$\omega_{pole} = \frac{1}{(R_{op} \parallel R_{on})C_{\mathrm{L}}} \tag{4.7}$$

Considering of 10bit ADC, the specification of the operational amplifier can be obtained from equation (4.3) and (4.5). So that the dc gain of the operational amplifier should be larger than 60dB, and the unity-gain bandwidth is about 100MHz. The output swing of the operational amplifier is ±350mV.

From the specification calculated from above, the simulation result of the operational amplifier is shown in Table 4.1. The specification is satisfied the requirements described above.

Table 4.1 Simulation result of operational amplifier

	Pre-simulation			**Post-simulation**		
Corner	**TT**	**FF**	**SS**	**TT**	**FF**	**SS**
Gain(dB)	72	71.5	72.5	72	70	73
f_u(MHz)	116	120	113	116	118	114
PM(°)	72	71	73	67	65	68
Power(mw)	256	260	253	263	269	258

4.2.2 Comparator

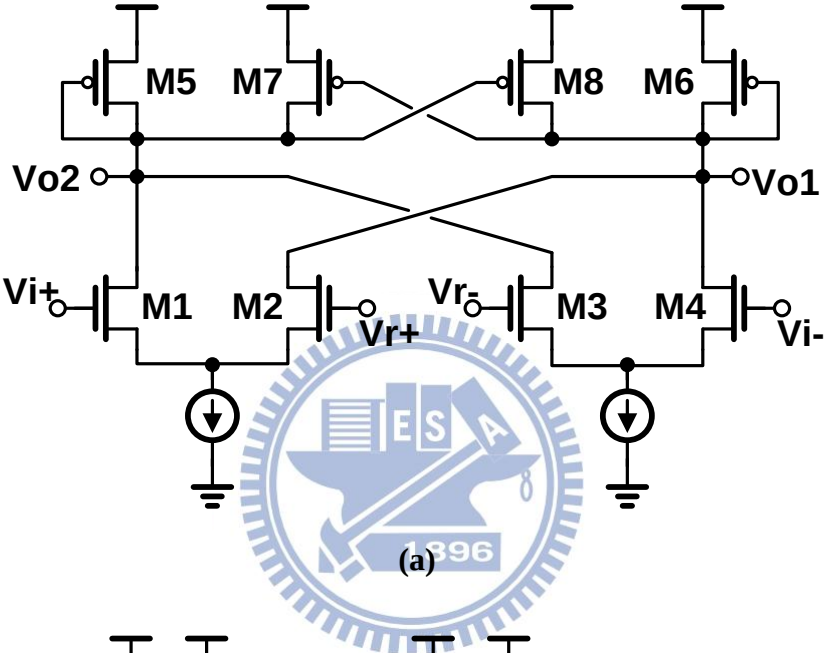
The schematic of comparator is shown in Figure 4.5, including a differential difference preamplifier and a regenerative latch. The differential difference preamplifier is used to reduce equivalent input offset.

$$V_{OS} = V_{OS,preamp} + \frac{V_{OS,latch}}{A_{preamp}} \tag{4.8}$$

It also provides input common mode rejection and kick-back noise reduction. Because

this cyclic ADC adopts 3.5bit per cycle, 15 sub-ranges that input range is divided, so that the number of the comparator is up to 14.

When CLK is low, regenerative latch operates in reset mode. At the same time, the preamplifier amplified the input signal. When CLK is high, the regenerative operates in evaluate mode, and the output keep the comparison result until next CLK pulse.



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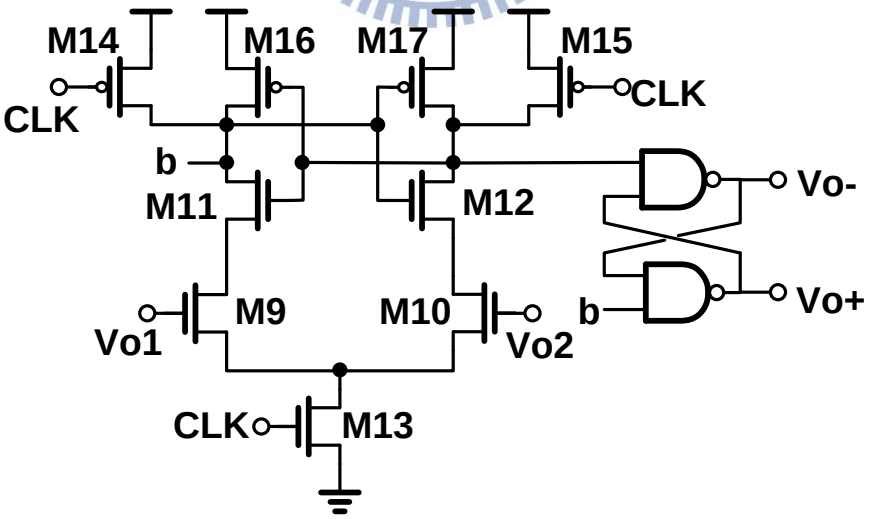


(b)

Figure 4.5 Comparator scheme

(a) Differential difference preamplifier (b) Regenerative latch

Considering the effect of device mismatch, the comparator will produce offset voltage. Because the full scale is 700mV, the comparator offset tolerance is about 22mV in this 3.5bit conversion step cyclic ADC. To simulate the effect of mismatches, randomly change the V_{th0}, channel width (W), and channel length (L) variations. The standard deviations are as below

$$\sigma^2(\Delta V_t) = \frac{A_{Vt}^2}{WL} \qquad \frac{\sigma^2(\Delta\beta)}{\beta^2} = \frac{A_\beta^2}{WL} \tag{4.9}$$

The input referred offset can be expressed as equation (4.10).

$$\sigma^2(V_{OS}) = \frac{1}{WL}\left(A_{Vt}^2 + \frac{V_{ov}^2}{4}A_\beta^2\right) \tag{4.10}$$

V_{ov} is overdrive voltage of input NMOS pair. A_{vt} and A_β are process parameter of TSMC 85nm CMOS technology. From 500 time Monte Carlo simulations, the standard deviation of offset voltage is about 7.2mV. The power consumption of all comparator is about 120μW.

4.2.3 Residue Amplifier

The residue amplifier provides the amplification for the residue to full scale. The basic degeneration differential amplifier is shown in Figure 4.6. The gain of basic degeneration differential amplifier is expressed as equation (4.11).

$$Gain = \frac{g_{m1}R_L}{1+\frac{1}{2}(g_{m1}+g_{mb1})R_S} \tag{4.11}$$

After the first conversion, the resolution of the residue is 7bit. To ensure the linearity of the residue amplifier, less than -42dB THD is required in the residue amplifier. The contribution of g_{m1} to the gain should be minimized. Therefore, the proposed residue amplifier is shown in Figure 4.7. M1-M8 is super source follower. Assume g_{m5} is equal to g_{m7}. The effective g_{meff} will be boosted by the feedback expressed as equation (4.12).

$$g_{meff} \approx \frac{1}{2}(g_{m1} + g_{mb1}) g_{m3} r_{o1} \tag{4.12}$$

The gain of proposed residue amplifier can be expressed as equation (4.13). If $1/g_{meff}$ is very smaller than R_S, it only depends on the ratio of resistor and device size.

$$Gain \approx \frac{\frac{1}{2}R_S}{\frac{1}{g_{meff}} + \frac{1}{2}R_S} \frac{R_L}{\frac{1}{2}R_S} \times \frac{g_{m11}}{g_{m3}} \tag{4.13}$$

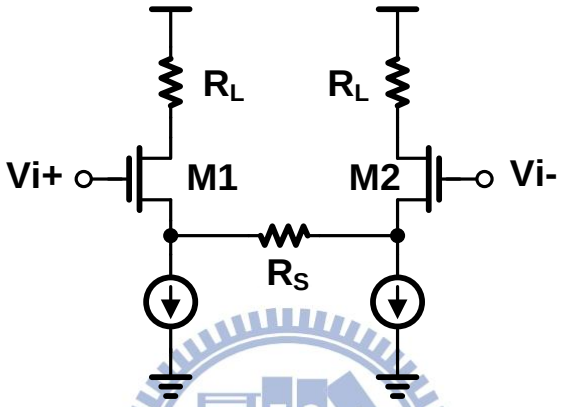


Figure 4.6 Basic degeneration differential amplifier

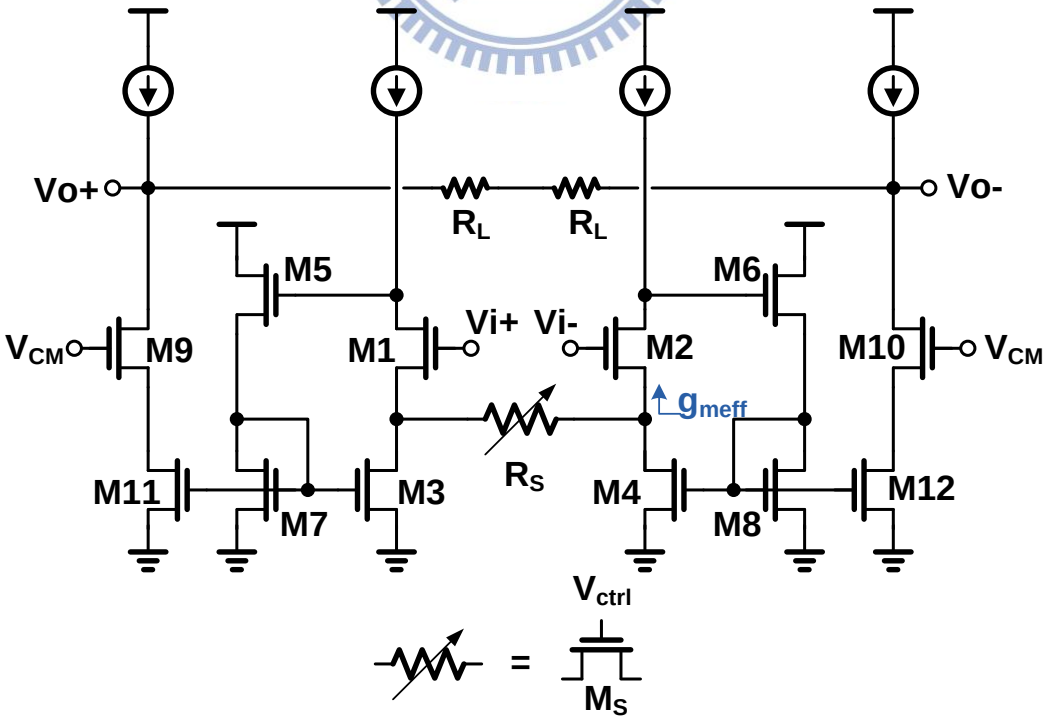


Figure 4.7 Proposed residue amplifier

Because of the charge sharing effect by the parasitic capacitor in the input of residue amplifier, the input voltage would be attenuated. The gain of it must be compensated. The degeneration resistor is implemented by a triode-region NMOS resistor replaces for gain tuning by adjusting the gate voltage. The calibration circuit could adjust the resistance of R_S to derive the amplified residue is as near 8 times as possible.

Besides considering of dc gain, the bandwidth is another important specification in the design of the residue amplifier. From the step settling response, the speed requirement, equation (4.14), can be derived. N is the residual resolution, τ_a is the time constant of the residue amplifier, and T_{settle} is the settling time. Therefore, the 3dB bandwidth can be expressed as equation (4.15)

$$T_{settle} > \tau_a N \ln 2 \tag{4.14}$$

$$f_{3dB} > \frac{N \ln 2}{2\pi T_{settle}} \tag{4.15}$$

The bandwidth from equation (4.15) should be larger than 50MHz. The simulation result is shown in table 4.3.

Table 4.3 Simulation result of residue amplifier

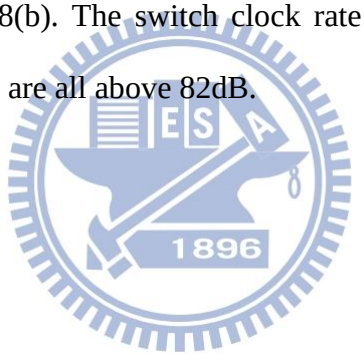
	Pre-simulation			**Post-simulation**		
Corner	**TT**	**FF**	**SS**	**TT**	**FF**	**SS**
Bandwidth(MHz)	66.5	66.8	66	63	72	56.8
THD(dB)	-49.8	-48.8	-49.3	-50.6	-45	-54.5
Power(μw)	436	441	431	445	449	441

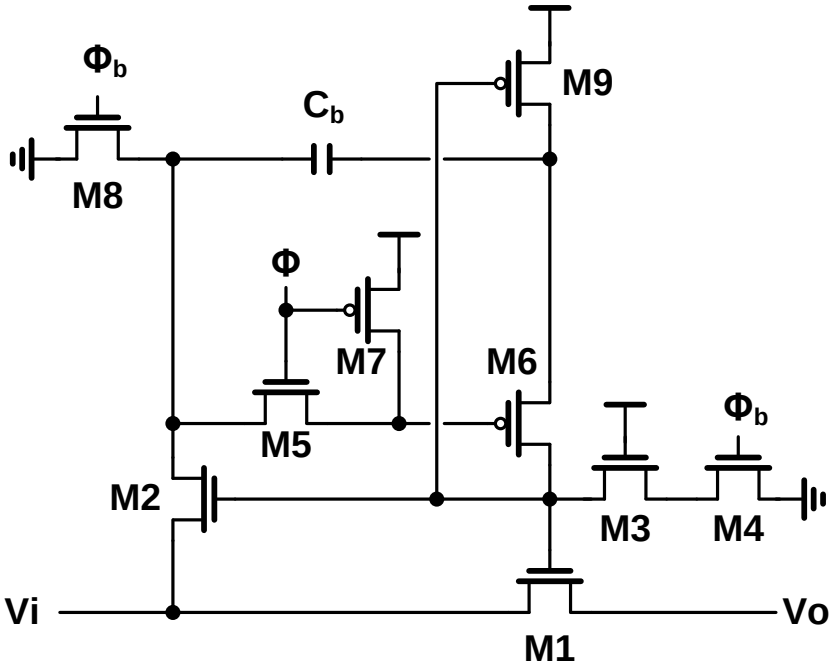
4.2.4 Bootstrapped Switch

Figure 4.8(a) shows the bootstrapped switch schematic. Bootstrapped switch provides constant impedance and is used to avoid the input dependent non-linearity. During Φ is low, the C_b stores the voltage drop VDD. During Φ is high, one terminal of C_b is connected to input Vi and the other terminal is pumped to 'Vi+VDD'. The gate to source voltage of M1 is VDD, which is independent to Vi. Therefore the impedance of M1 can be derived as equation (4.16).

$$R_{on,M1} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{DD} - V_t)} = const \tag{4.16}$$

Then change input frequency to plot the SFDR curve of output FFT. The simulated result is shown in figure 4.8(b). The switch clock rate is 25MS/s. From low input frequency to high, the SFDR are all above 82dB.





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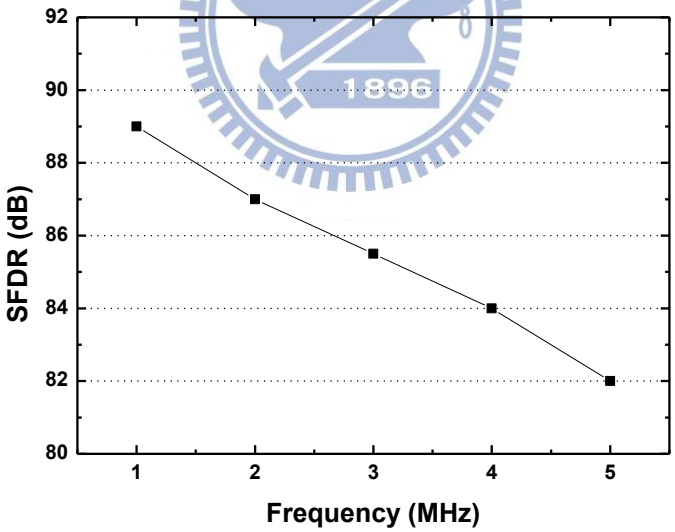


(b)

Figure 4.8 (a) Bootstrapped switch schematic (b) SFDR versus input frequency

4.2.5 Calibration Circuit

After the residue which subtracted by the analog input and the appropriate reference voltage is taken, it will be amplified to full scale and start the next cycle of conversion. Because of parasitic capacitor in the input node of residue amplifier, the input voltage would be attenuated. The calibration circuit is required to compensate the gain error. Figure 4.9 shows the fundamental gain control servo loop [9]. The control voltage V_{ctrl} is feedback to the gate of Ms of residue amplifier for gain control. The transfer equation is expressed as equation (4.17).

$$V_{j+1} = \frac{C_2}{C_2 + C_P} \times A_0 \times \left(V_{da} - V_j\right) \tag{4.17}$$

But the replica circuit consumes the extra power. Thus the proposed calibration architecture applied in the 3.5bit per cycle of the cyclic ADC is shown in figure 4.10. Using amplifier sharing technique and capacitor sharing technique, it do not need extra replica amplifier and sample capacitor. Thus, the power consumption can be saved dramatically.

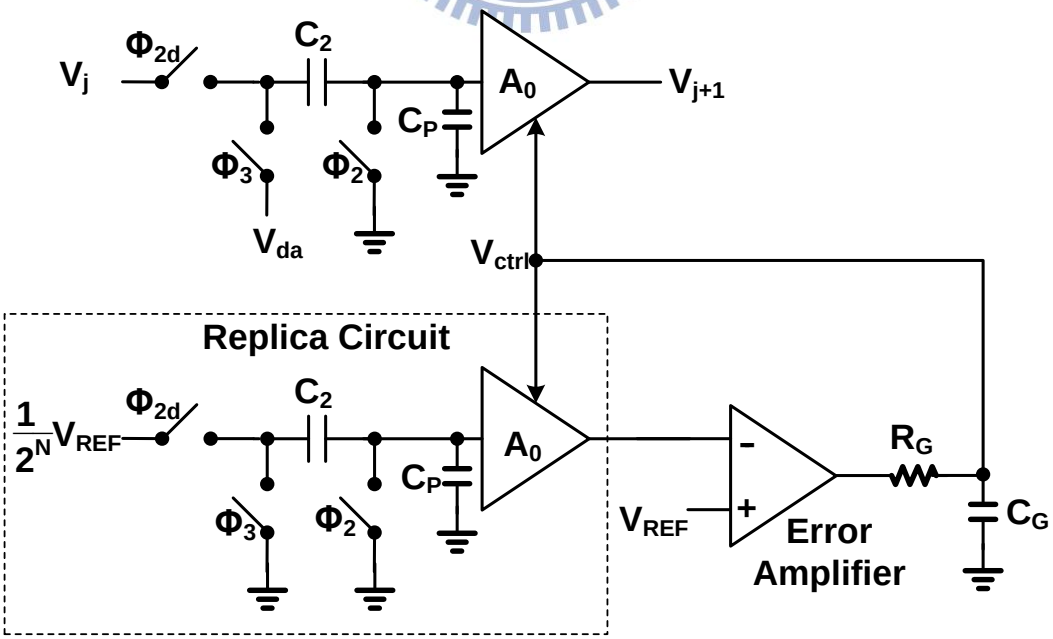
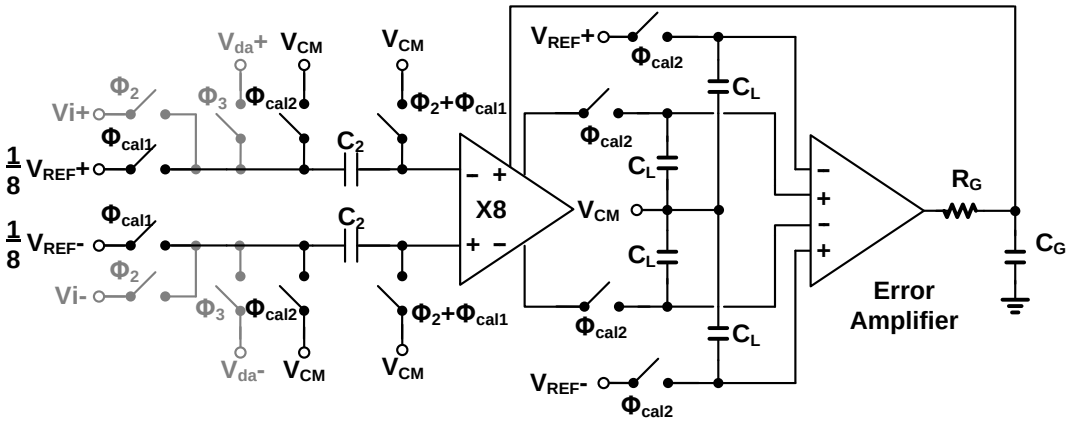
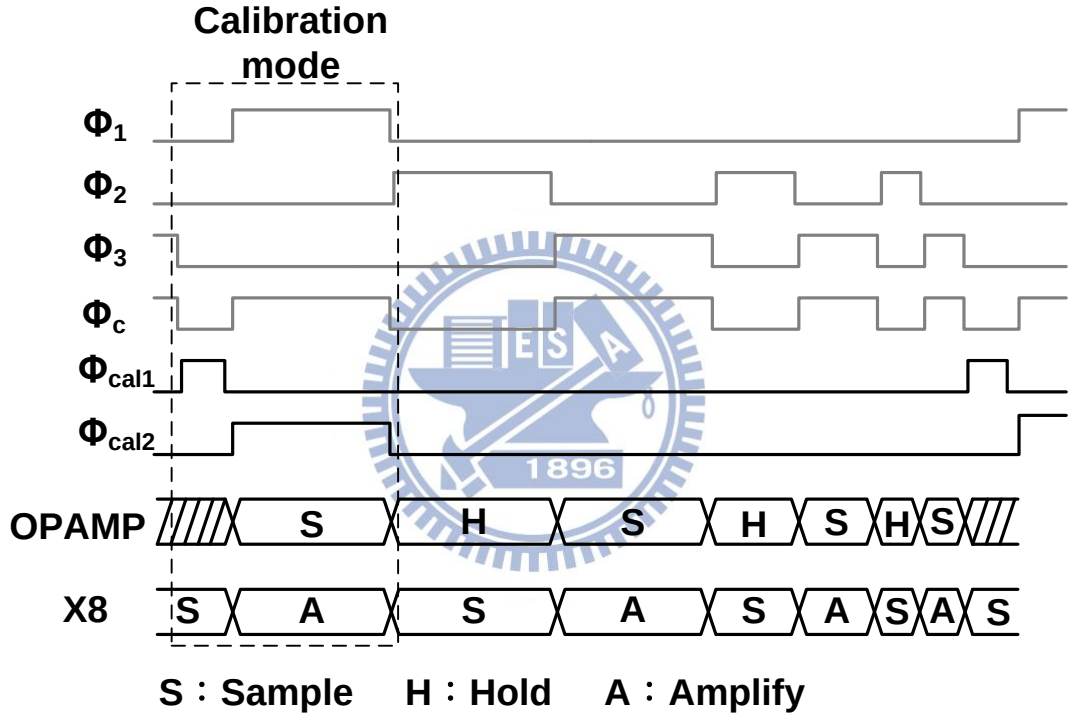


Figure 4.9 The fundamental gain control servo loop



(a)



(b)

Figure 4.10 (a) Calibration circuit (b) Timing diagram

For 3.5bit per cycle of the cyclic ADC, the calibration circuit with servo loop is adopted to control the stage gain to be 8. The operation of calibration mode is the same as the normal operation. In clock phase Φ_{cal1}, the $1/8V_{REF}$ is sampled into the capacitor C_2. Because of the charge sharing effect by the parasitic capacitor in the input, the input voltage would be attenuated at clock phase Φ_{cal2}. Finally, the V_{REF}

from dc will be compared with the amplified $1/8V_{REF}$ in the input of the error amplifier. After comparing the difference between V_{REF} and the amplified $1/8V_{REF}$, the output voltage of error amplifier passes through the RC low-pass filter and feedbacks to the gain control of residue amplifier in calibration. By adjusting the control voltage, it can fine tune the resistance in residue amplifiers so that it can control the stage gain is about 8 by the servo loop. The RC low pass filter dominates the loop bandwidth, which is about 10kHz. The detail of the error amplifier are introduced in the below.

4.2.6 Error Amplifier

The error amplifier in the calibration circuit is used to detect the difference between the sampled value and the reference voltage. Then, it is responsible to verify the comparison result, and drives the gain control of residue amplifier after a RC low pass filter. Because the RC low pass filter dominates the loop bandwidth, the phase margin and bandwidth of error amplifier are not stringent.

The scheme of the error amplifier is shown in figure 4.11. It consists of two stages. The first stage, M1-M4, is a dual source couple pair differential difference amplifier. Then M5-M6 transfers differential to single-ended. The second stage, M7, is a common source amplifier. The simulation result is shown in table 4.4. The dc gain of the error amplifier is above 40dB, and total power consumption is about 0.12mW.

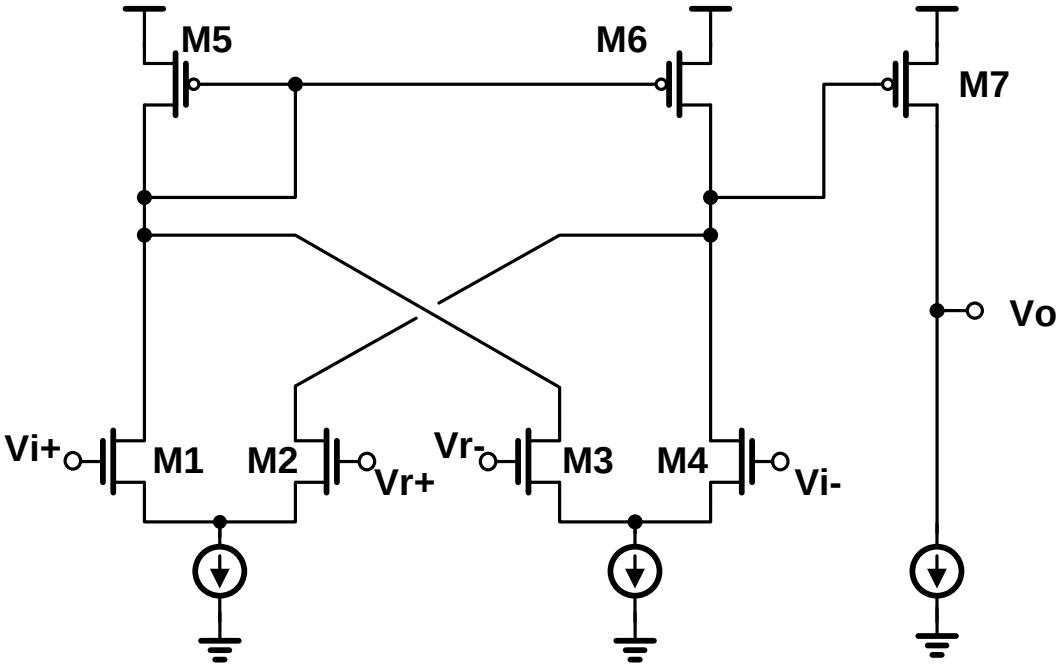


Figure 4.11 Error amplifier scheme

Table 4.4 Simulation result of error amplifier

	Pre-simulation			Post-simulation		
Corner	**TT**	**FF**	**SS**	**TT**	**FF**	**SS**
Gain(dB)	44	43.8	44.3	43	40	44.5
Power(μw)	118	122	114	122	126	118

4.2.7 Encoder And Clock Generator

Figure 4.12 shows the encoder and R-string DAC scheme. The encoder converts thermometer code from comparators to 4bit binary code, which also contains the functions for solving sparkle. Then it drives R-string DAC to generate the appropriate reference voltage V_{da} subtracted from the sampled signal. Figure 4.13 shows the digital error correction logic, which consists of half-adders and full-adders. In the end of the total conversion, 10bit digital codes will be produced.

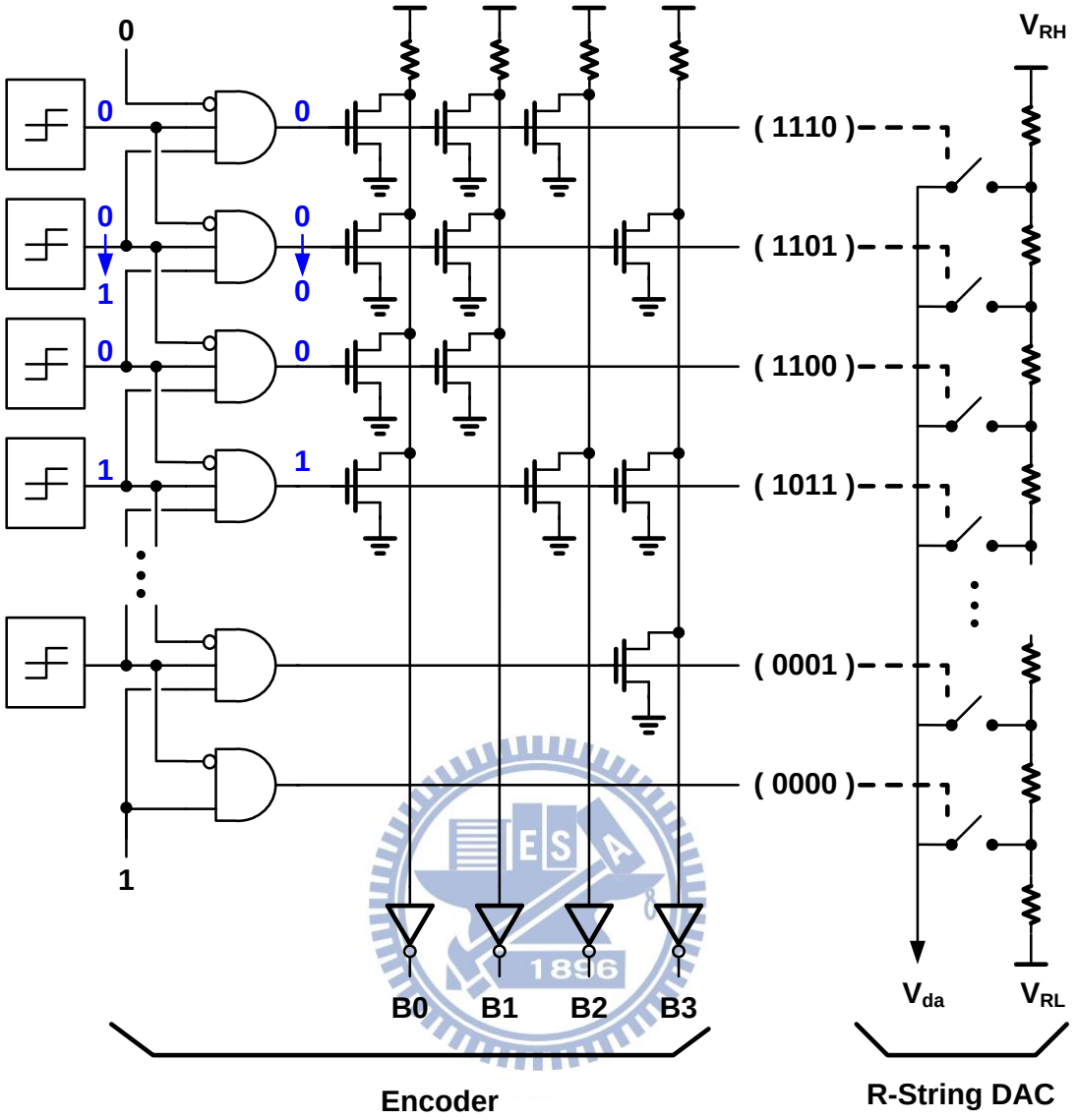


Figure 4.12 Encoder and R-string DAC scheme

```
                              B0  Stage 4
                        B0 B1 B2 B3  Stage 3
                  B0 B1 B2 B3        Stage 2
+ B0 B1 B2 B3                        Stage 1
-------------------------------------------
  D0 D1 D2 D3 D4 D5 D6 D7 D8 D9
```

Figure 4.13 Digital error correction logic

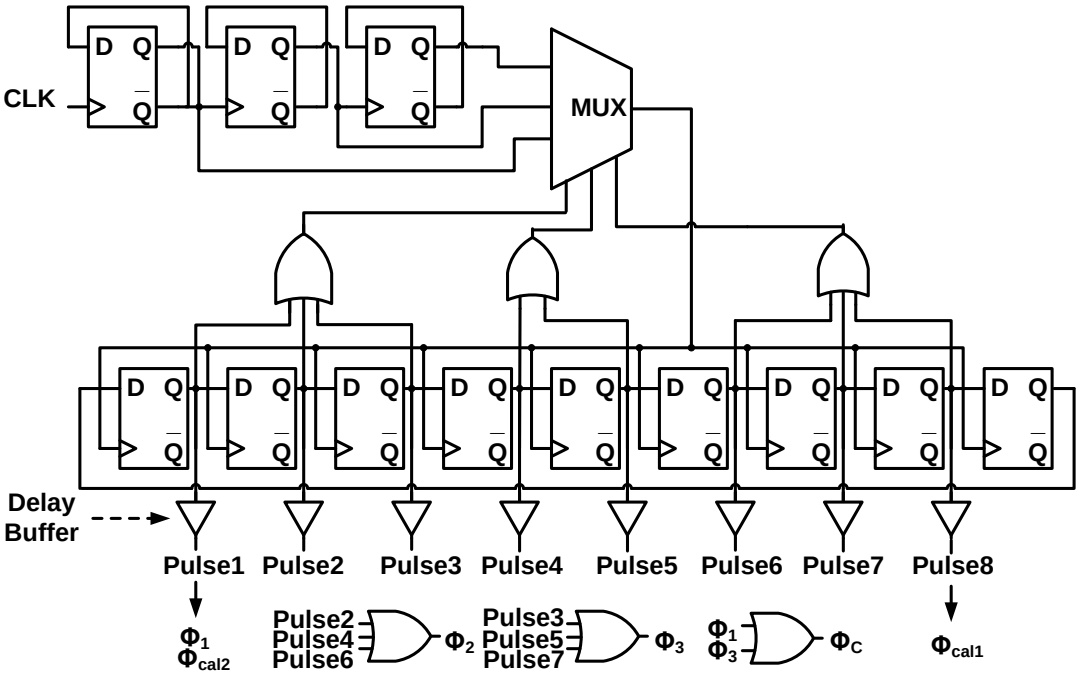
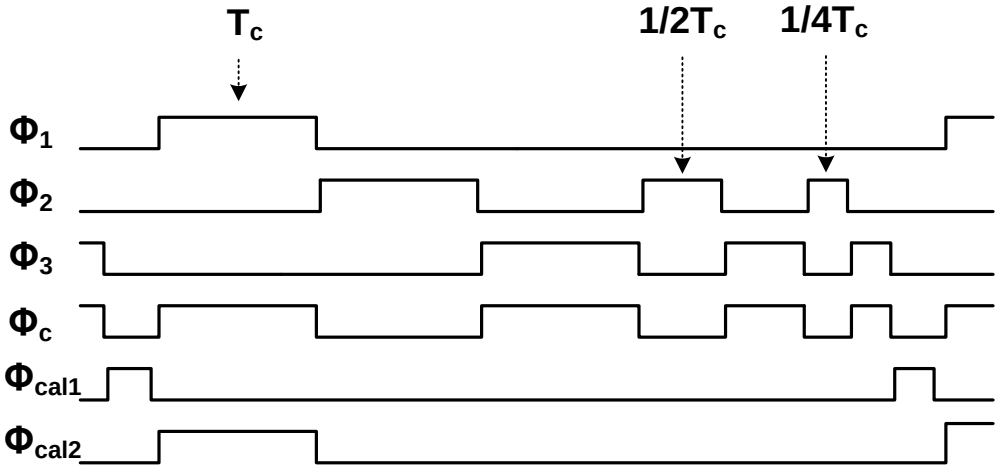
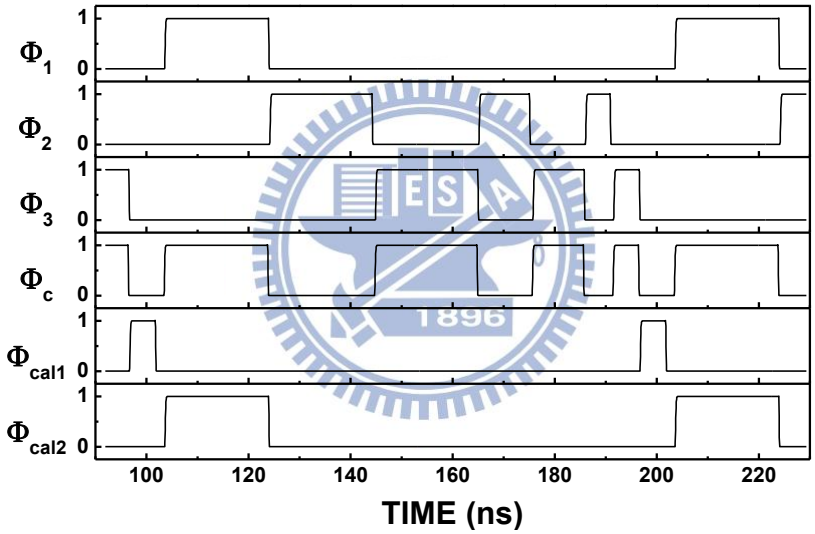


Figure 4.14 Clock generatior scheme

Figure 4.14 is the proposed clock generator architecture adopting the timing re-scheduled technique. It includes frequency dividers, the multiplexer, shift registers, delay buffers, and logic circuit. Initial value of one of D-Flip Flops output set to 1 and other reset to 0 before the clock generator starts up. When the 400MHz clock signal from outside pulse generator applies the input of frequency divides, the three frequency dividers in series connection divide the clock into 200MHz, 100MHz and 50MHz respectively. Finally, the delay buffers and the logic circuit compose the non-overlap timing re-scheduled clock for this cyclic ADC. The proposed timing re-scheduled waveform is shown as figure 4.15(a), and the simulation result is shown in figure 4.15(b). The conversion time T_c is 20 ns. The power consumption is 50μW in pre-simulation and 77μW in post-simulation.



(a)



(b)

Figure 4.15 Timing diagram

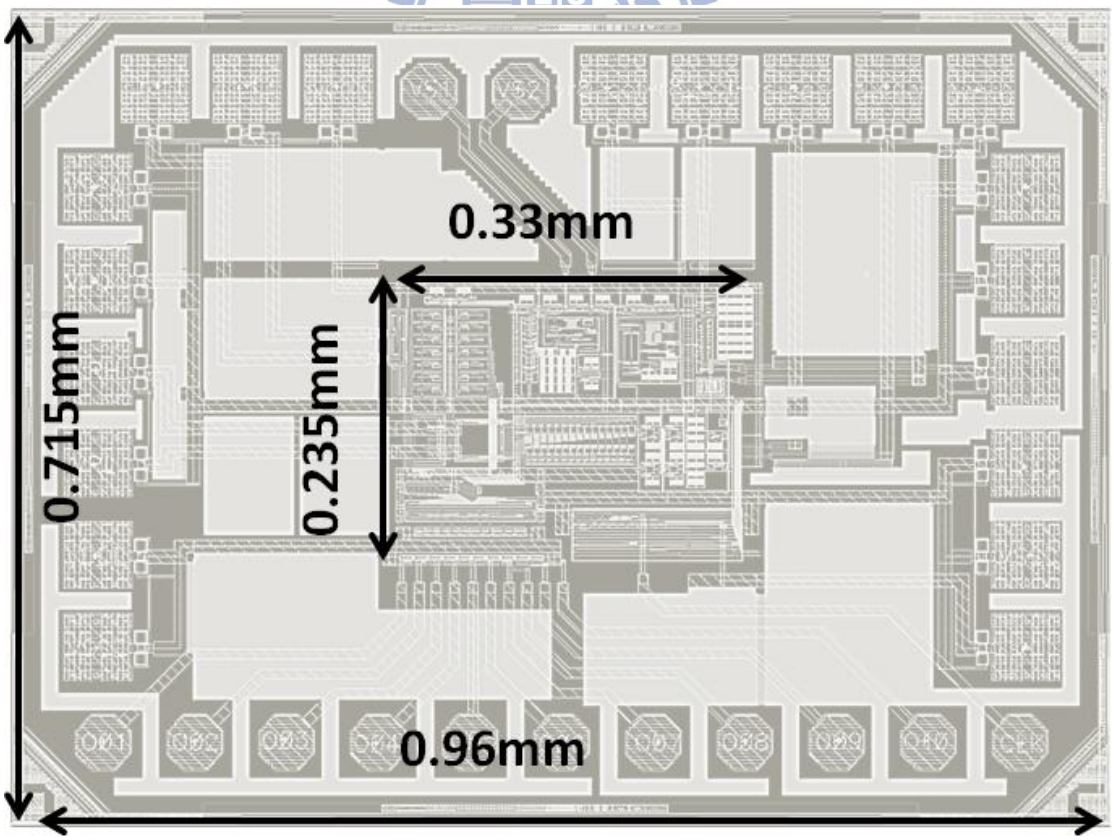
(a) Proposed timing re-scheduled waveform (b) Simulation result

CHAPTER 5

EXPERIMENT RESULT

5.1 Floor-planning and Layout

The implementation of the cyclic ADC has been integrated in TSMC 85nm CMOS technology. The 85nm CMOS process is 94% linear shrinkage from 90nm layout dimensions. The active area of the ADC is $0.33\times0.235mm^2$ with 94% linear shrinkage and the die size is $0.96\times0.715mm^2$ with 94% linear shrinkage. Figure 5.1 shows the layout and floor-planning of the chip. In order to isolate the couple noise, the analog and digital parts are separated. Switches and capacitors array are placed between digital circuit and analog circuits. Bypass capacitor which is implemented by fringe capacitor is used to stable the reference voltages.



(a)

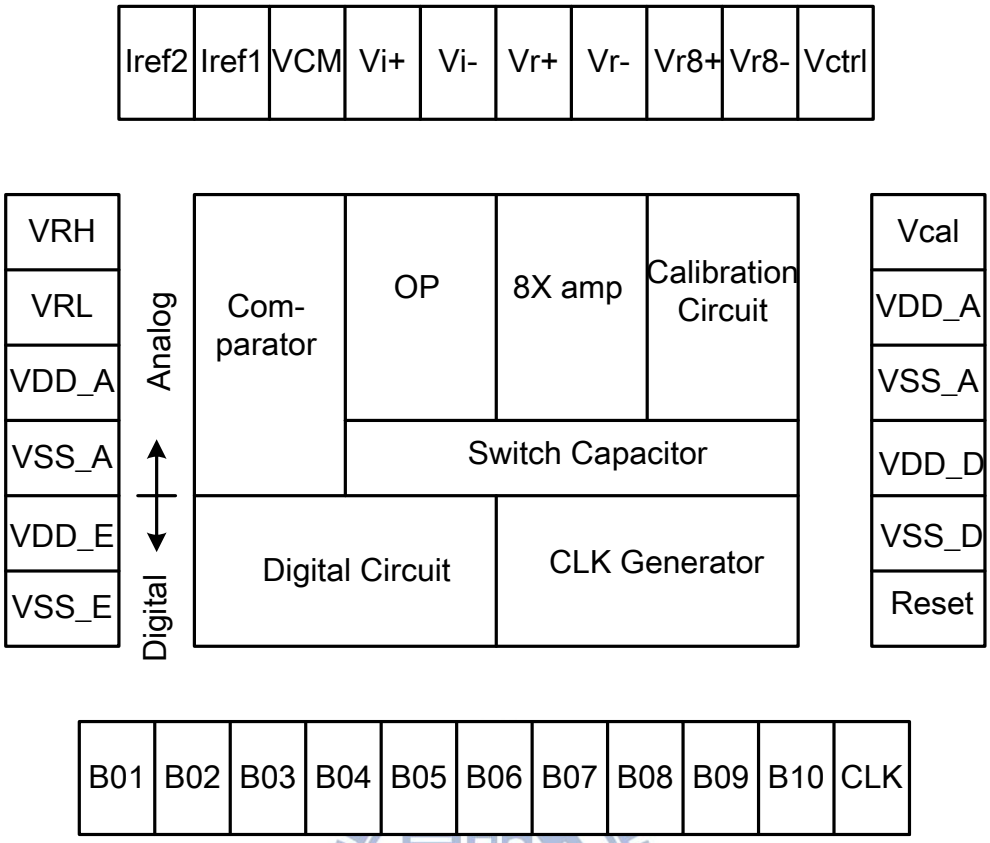


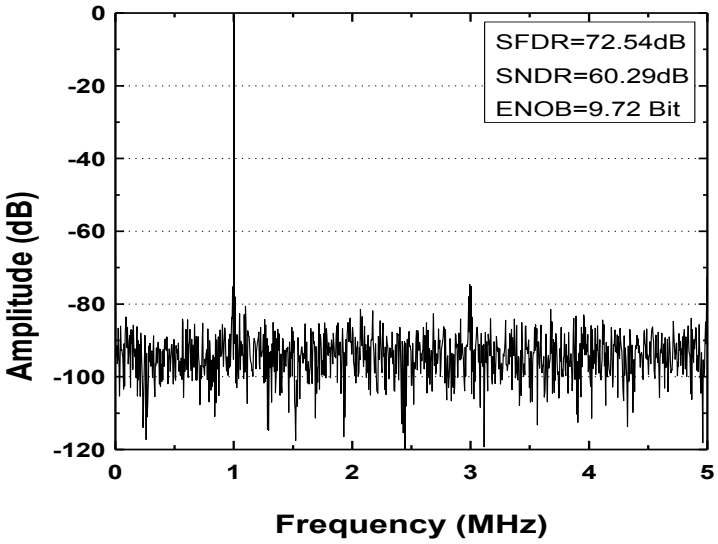
Figure 5.1 The diagram of chip (a) layout (b) floor-planning

5.2 System Simulation Result

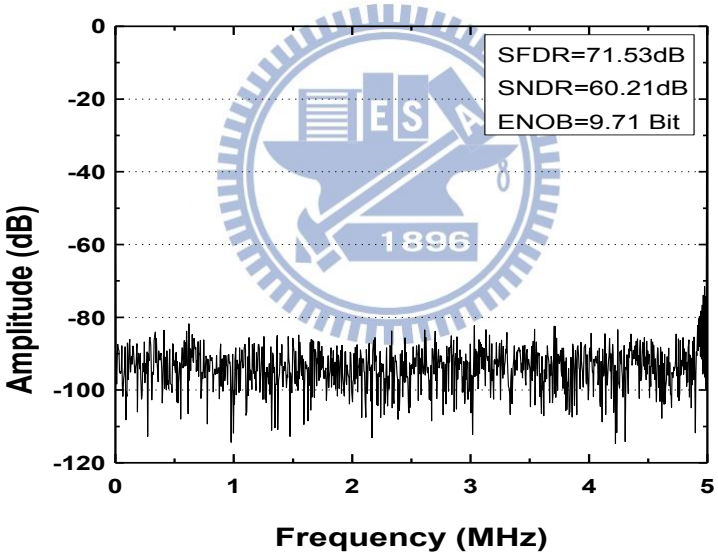
5.2.1 Dynamic Simulation

Figure 5.2 shows the pre-simulated and post-simulated FFT plot at 10MS/s sampling frequency in TT corner. The SFDR, SNDR, and ENOB at 1MHz and 5MHz input signal are shown in each top right corner of figure.

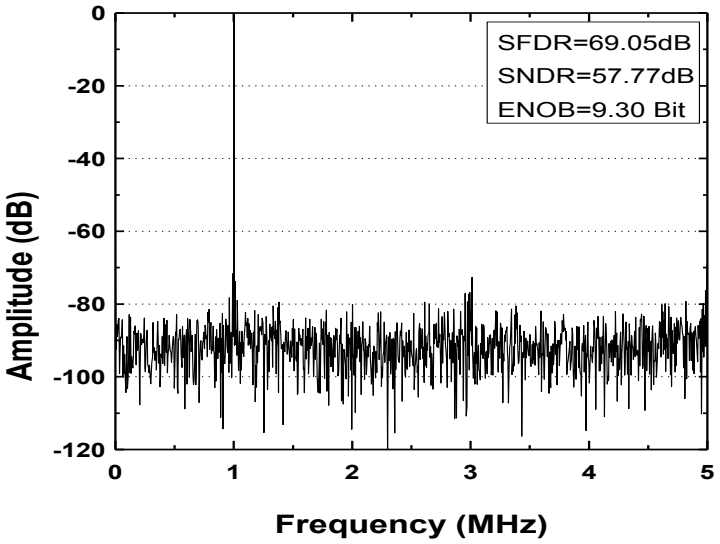
The SFDR when input is in 1MHz and 5MHz are 72.54dB and 71.53dB in pre-simulation. The ENOB when input is in 1MHz and 5MHz are 9.72bit and 9.71bit in pre-simulation respectively. The SFDR when input is in 1MHz and 5MHz are 69.05dB and 70.50dB in post-simulation. The ENOB when input is in 1MHz and 5MHz are 9.30bit and 9.31bit in post-simulation respectively.


SFDR=72.54dB
SNDR=60.29dB
ENOB=9.72 Bit
Amplitude (dB)
Frequency (MHz)
0
-20
-40
-60
-80
-100
-120
0
1
2
3
4
5

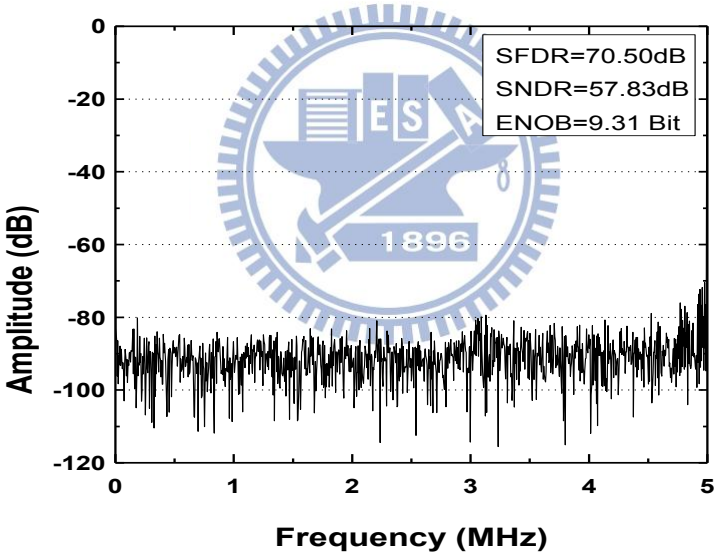
(a)


SFDR=71.53dB
SNDR=60.21dB
ENOB=9.71 Bit
Amplitude (dB)
Frequency (MHz)
0
-20
-40
-60
-80
-100
-120
0
1
2
3
4
5

(b)



(c)



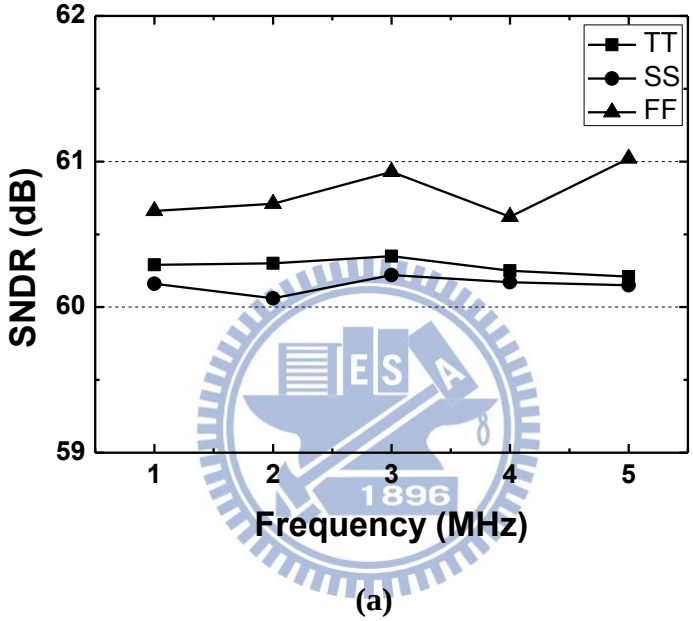
(d)

Figure 5.2 Simulated FFT at sampling rate=10MS/s

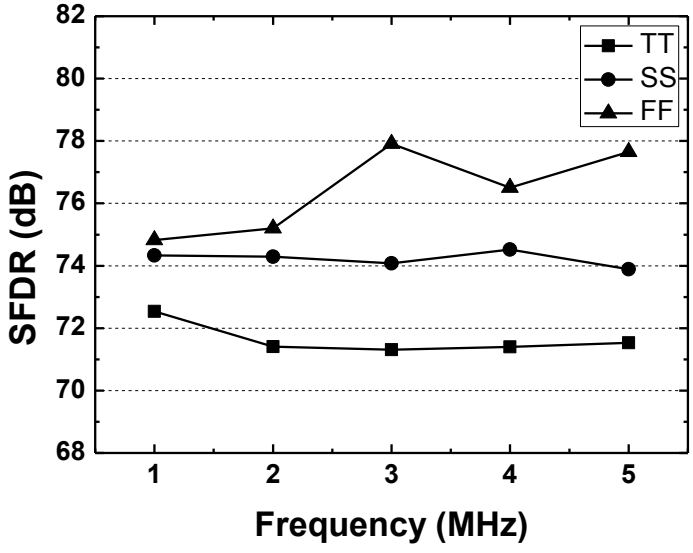
(a) Pre-simulation at 1MHz input (b) Pre-simulation at 5MHz input

(c) Post-simulation at 1MHz input (d) Post-simulation at 5MHz input

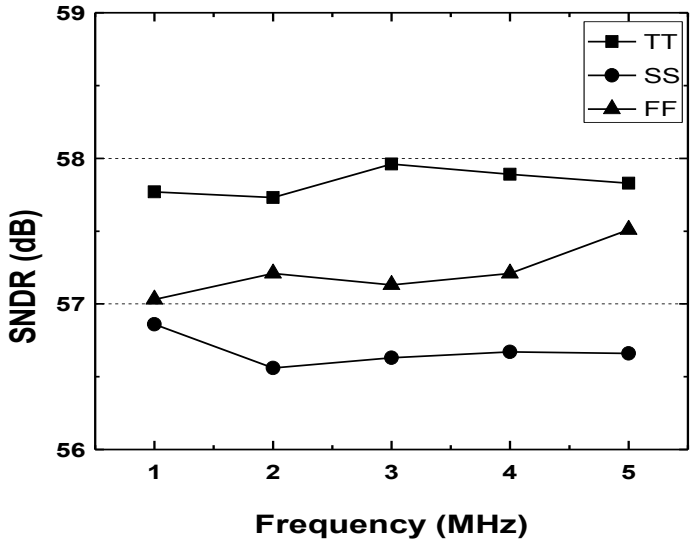
Due to PVT variation, corner simulations for TT, FF and SS are also needed. Figure 5.3 is the SNDR and SFDR plot which is pre-simulation and post-simulation result when input frequency is from 1MHz to 5MHz. In pre-simulation, the ENOB is above 9.7bit in all corners. In post-simulation, the best ENOB archive 9.3bit in TT corner. The worst case, the ENOB is 9.1bit in SS corner.



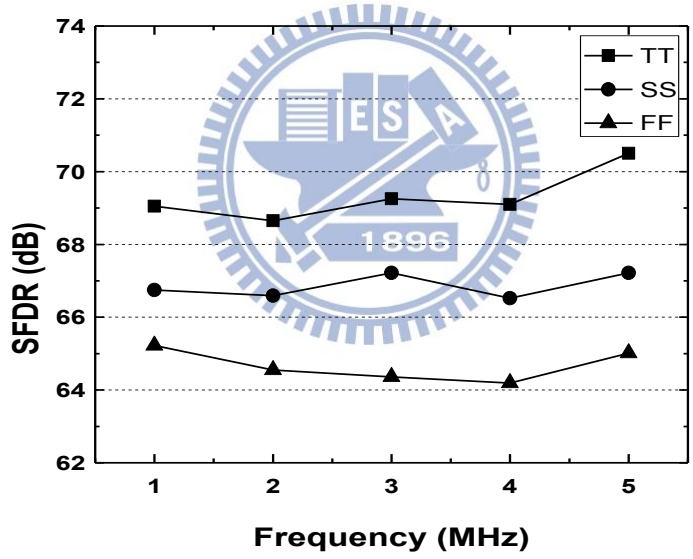
(a)



(b)



(c)



(d)

Figure 5.3 Pre-simulation and post-simulation in corner

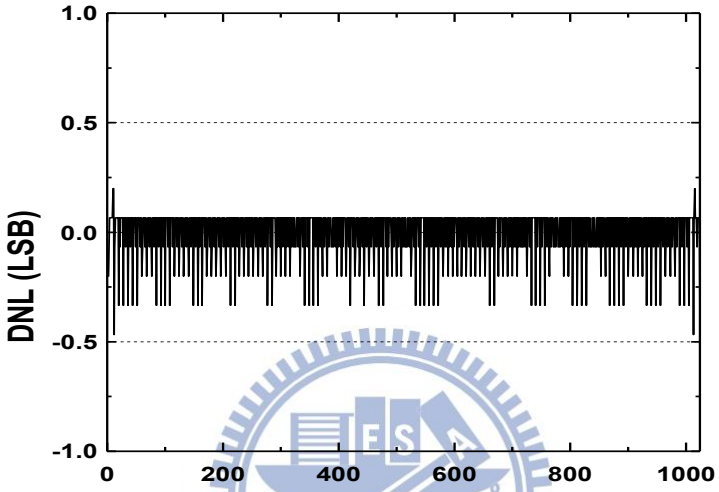
(a) Pre-simulation SNDR (b) Pre-simulation SFDR

(c) Post-simulation SNDR (d) Post-simulation SFDR

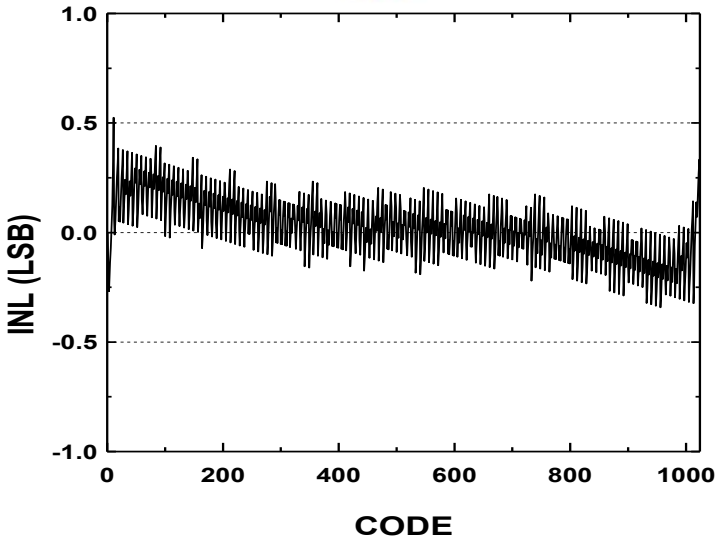
5.2.2 INL and DNL

INL and DNL show the non-linearity performance of ADC. Figure 5.4 (a) and

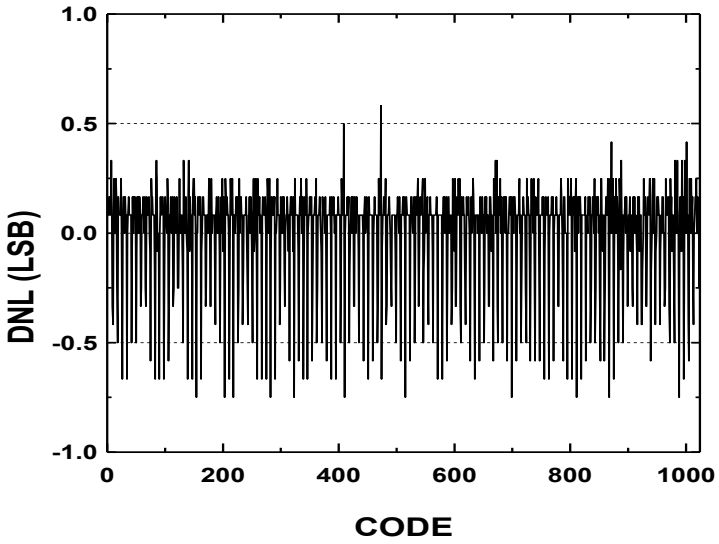
5.4 (b) is the DNL and INL plot in pre-simulation. The DNL is about 0.46LSB, and the INL is about 0.52LSB. In figure 5.4(c) and 5.4 (d), the DNL and INL plot in post-simulation is shown. The DNL is about 0.75LSB and the INL is 1.2 LSB. The linearity is worse in the full swing near ±350mV is because the linearity of residue amplifier is degraded. The LSB is 10bit resolution to full scale input.



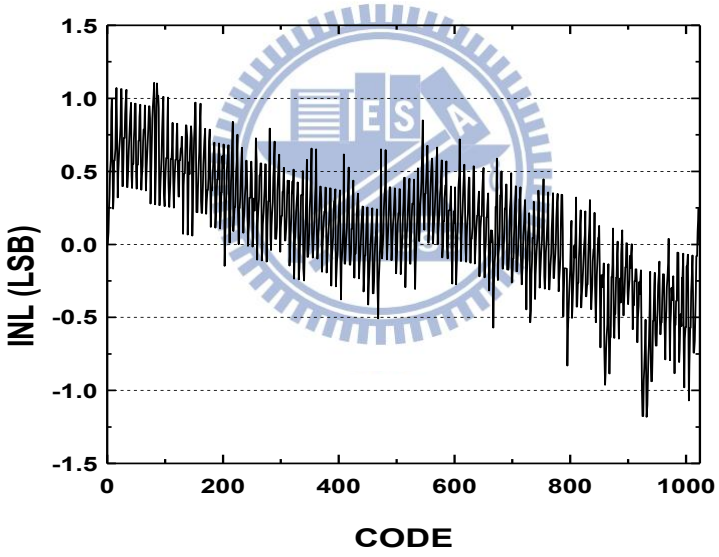
(a)



(b)



(c)



(d)

Figure 5.4 DNL and INL

(a) Pre-simulation DNL (b) Pre-simulation INL

(c) Pre-simulation DNL (d) post-simulation INL

5.2.3 Specification Table

Table 5.1 shows the performance summary simulated in 85nm TSMC CMOS process. The conversion rate is 10MS/s and the resolution is 10bit. In post-simulation, the ENOB is 9.3bit and 9.31bit when input frequency is 1MHz and 5MHz, respectively. The total power is 1.04mW. Then the digital circuit consumes about 0.1mW, and analog circuit consumes 0.94mW. The detailed power distribution is shown below in figure 5.5. The FOM is defined as

$$FOM = \frac{Power}{2^{ENOB} \times Conversion\ rate} \tag{5.1}$$

In this design, the FOM is 165fJ/conv.-step at input frequency is 1MHz and at post-simulation.

Table 5.1 ADC specification of pre-simulation and post-simulation

	Pre-sim	**Post-sim**
Technology	85 nm CMOS process	
Resolution	10 bit	
Supply voltage	1.2V [Analog] 1V [Digital]	
Signal Swing	+/-400mV	
Conversion rate	10MS/s	
SNDR	60.29dB @ 1MHz input 60.21dB @ 5MHz input	57.77dB @ 1MHz input 57.83dB @ 5MHz input
ENOB	9.72bit @ 1MHz input 9.71bit @ 5MHz input	9.30bit @ 1MHz input 9.31bit @ 5MHz input
Power consumption	0.94mW [Analog] 0.1mW [Digital]	
	1.04mW [Total]	
FOM	123fJ/conv.-step	165fJ/conv.-step

$$FOM = \frac{Power}{2^{ENOB} \times Conversion\ rate}$$

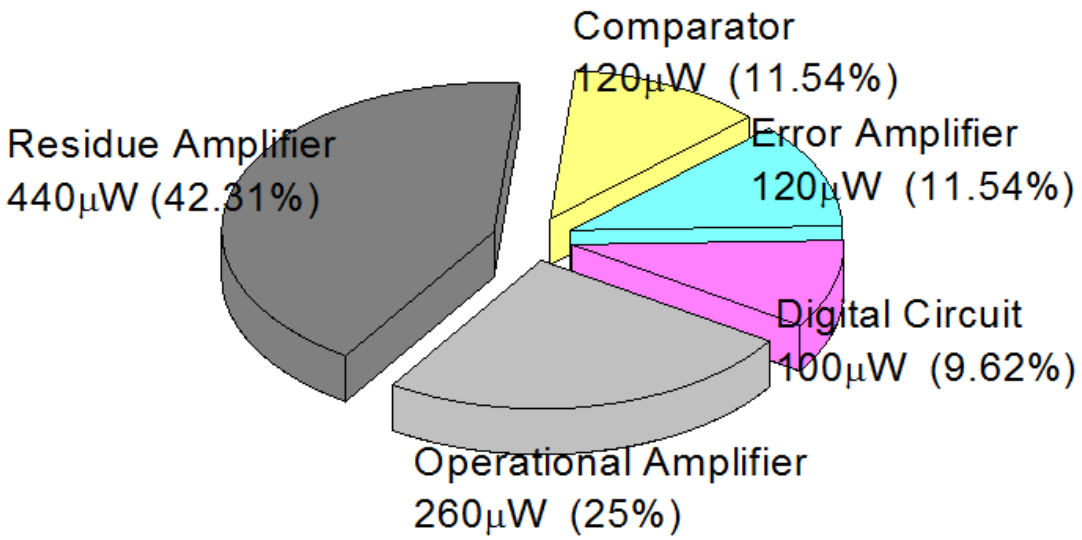


Figure 5.5 Power consumption of each block

5.3 Experimental Result

5.3.1 Measurement Consideration

The measurement setup is shown in figure 5.6. The supply voltages are generated by the power supply. In order to prevent the digital noise coupling to the analog circuits, analog and digital powers are isolated to each other in the PCB board. The analog input signal is generated from a high performance signal generator, Agilent E4438C. The clock pulse is generated from the pulse generator, Agilent 8133A. The output digital codes are sent to the logic analyzer, Agilent 16800. The data could be downloaded to the personal computer and processed to calculate the DNL, INL and FFT analysis by MATLAB.

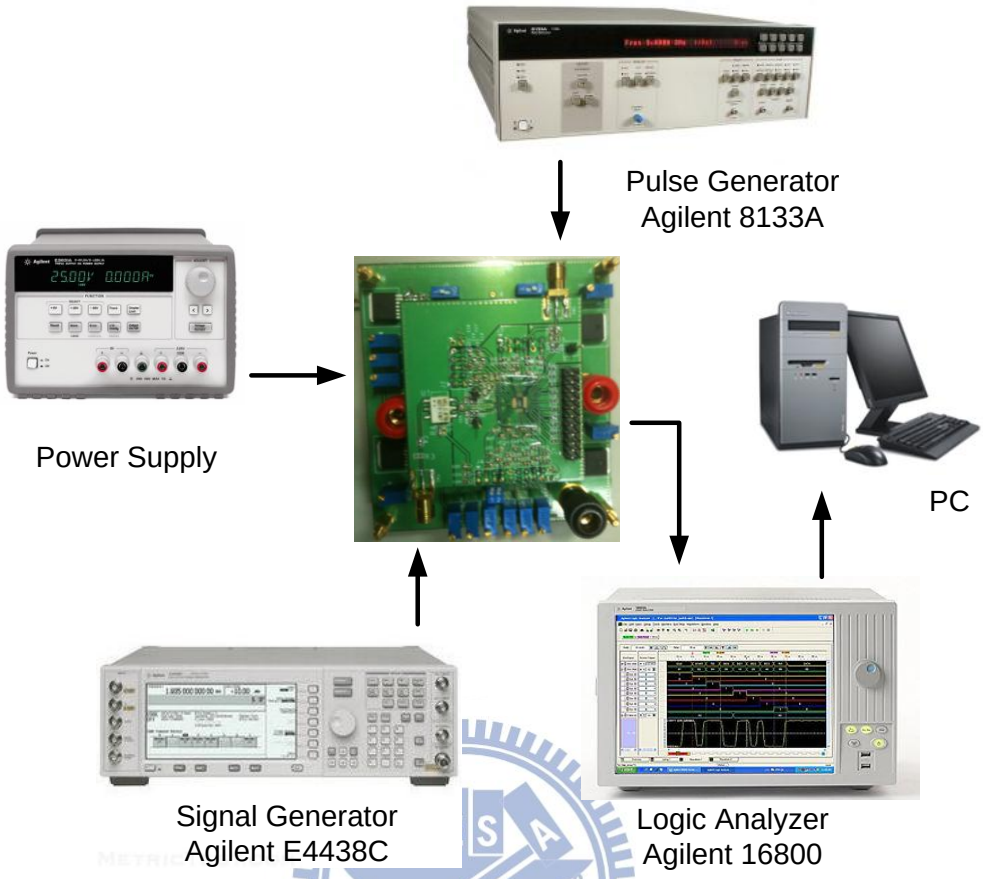


Figure 5.6 Measurement consideration

5.3.2 Measurement Result

The chip microphotograph of the fabricated ADC is shown in the figure 5.7. The active area of the ADC is 0.33×0.235mm^2 and the die size is 0.96×0.715mm^2. Figure 5.8 shows the ADC's FFT spectra at 10MS/s conversion rate. The input is differential 700mV$_{pp}$ 1MHz sinusoidal signal. The SNDR is 50.01dB and the SFDR is 59.95dB. The second harmonic tone is induced by the unbalanced differential signal. This could be found in post-simulation in FF corner. The opamp gain error and residue amplifier non-linearity induce the third harmonic tone. It can be improved by raising supply voltage and reducing input signal swing. The ENOB increases about 0.5bit when supply voltage is up to 1.4V. Figure 5.9 shows the ADC's measured SNDR, SFDR and ENOB versus input frequencies at 10MS/s conversion rate. The SNDR and SFDR decrease up to the Nyquist frequency.

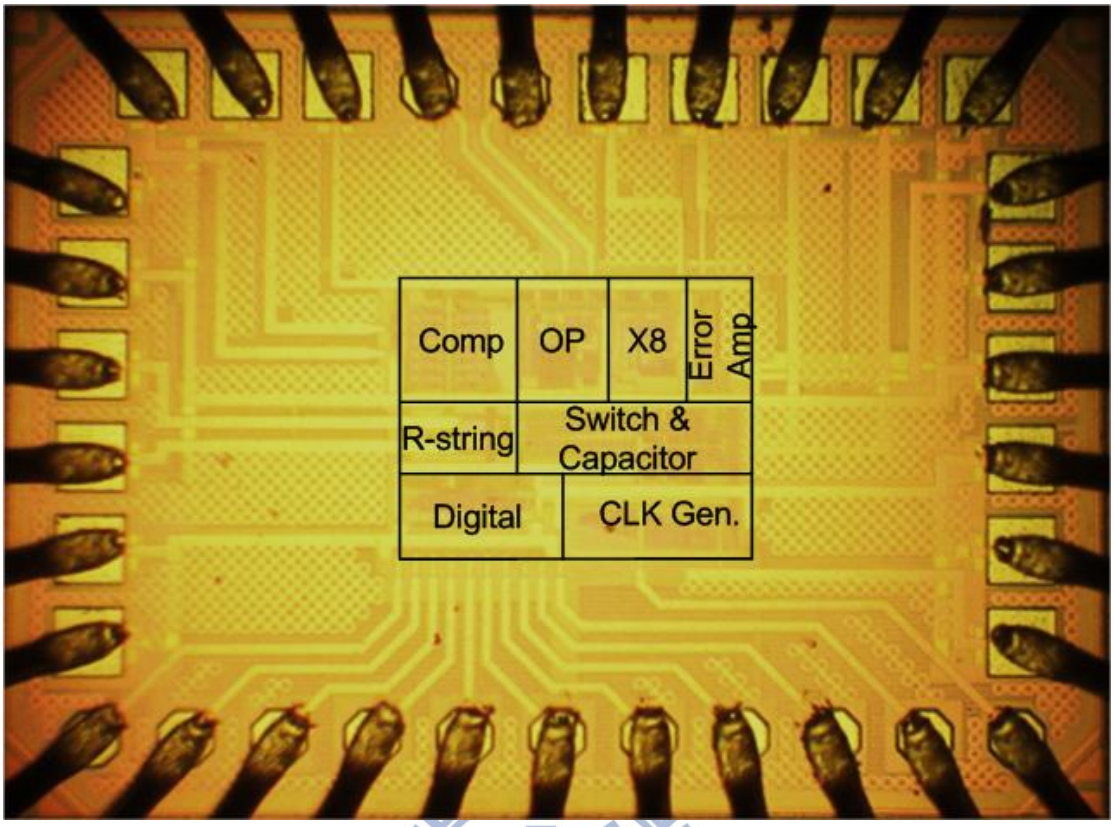


Figure 5.7 The chip microphotograph of the ADC

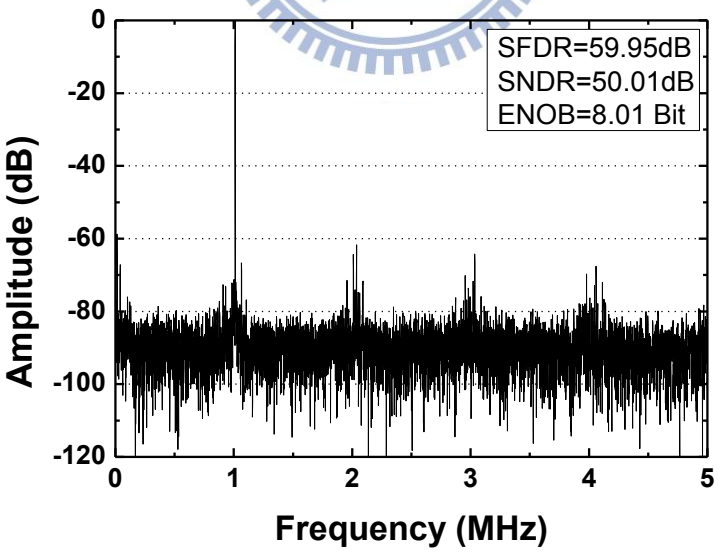
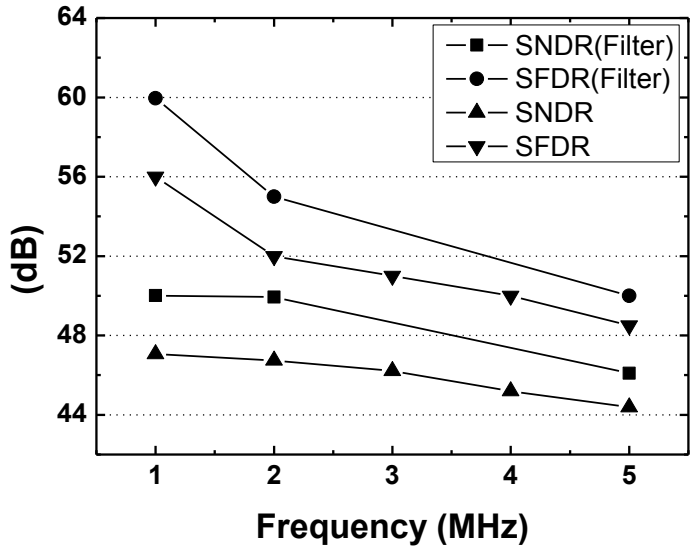
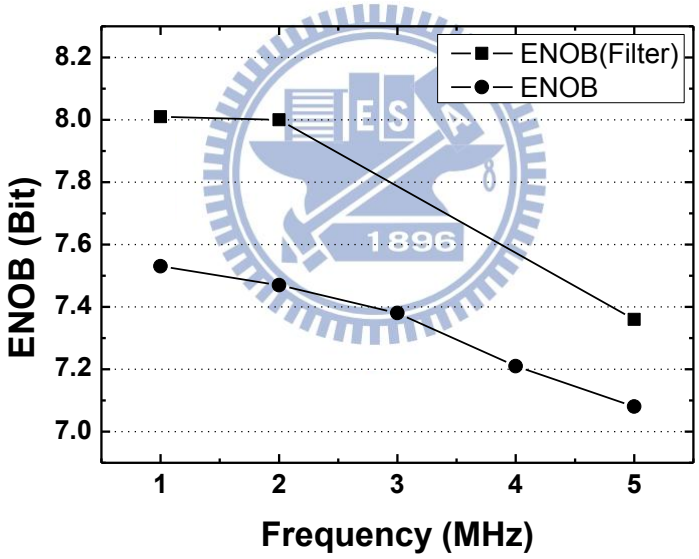


Figure 5.8 Measured output FFT spectra



(a)

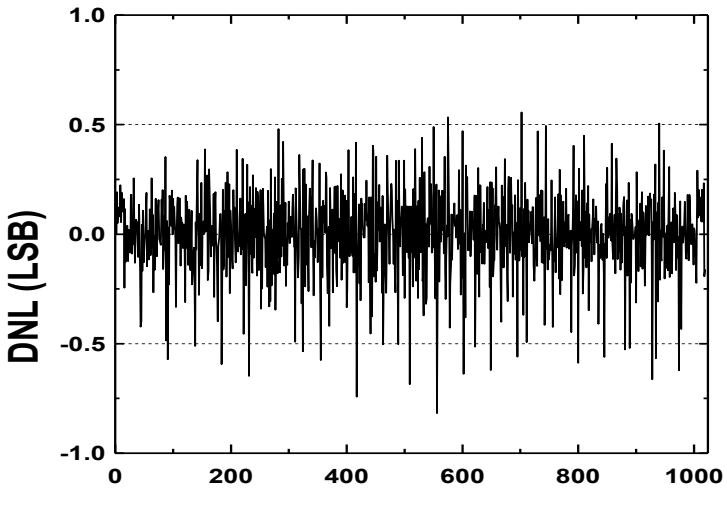


(b)

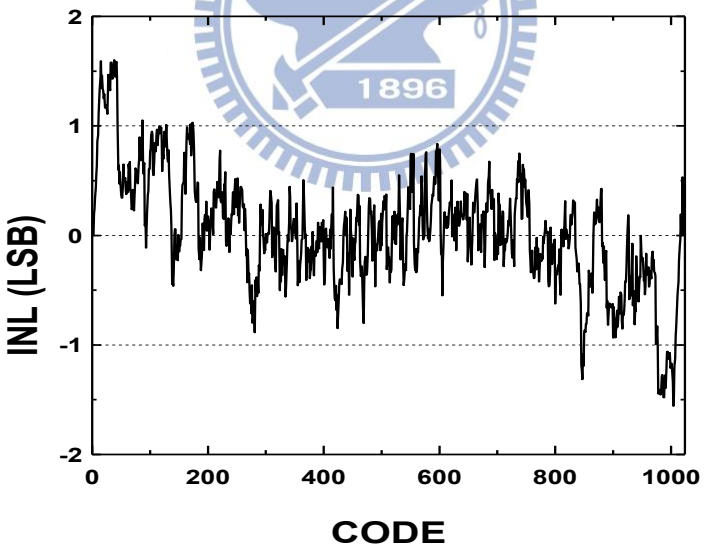
Figure 5.9 (a) SNDR and SFDR of the ADC (b) ENOB of the ADC

Figure 5.10 shows the ADC's DNL and INL characteristics obtained from code-density measurements. The LSB is normalized to 10bit resolution in those figures. The number of registered output code is 32768. The DNL is +0.55/-0.82 LSB and INL is +1.6/-1.5 LSB. The INL is the worst when signal is full-scale. It can be

improved by raising supply voltage. The transistors of residue amplifier have enough headroom at higher supply voltage operation. It is the same as simulation.



(a)



(b)

Figure 5.10 (a) DNL of the ADC (b) INL of the ADC

CHAPTER 6

CONCLUSION

Table 6.1 summarizes the benchmark of the performance for the proposed cyclic ADC. The power supplies are 1.2V and 1V in this work, and the SNDR is 49.5dB and ENOB is 7.93bit at sampling rate is 10MS/s and input frequency is 1MHz. The FOM shows 0.45pJ/conv.-step. Compare to other references shown in table I.

Table 6.1 Performance summary of cyclic ADC

	2009 JSSC[5]	2010 JSSC[7]	2010 JSSC[11]	2009 JSEN[15]	2011 JSSC[20]	This Work
Technology	90nm	90nm	0.18μm	0.18μm	0.18μm	85nm
Type	Pipelined	Cyclic	Pipelined	Cyclic	Pipelined	Cyclic
Supply Voltage	1.2	1V	1.8V	3.3V	1.8V	1.2V 1V
Resolution	9.4bit	9bit	10bit	10bit	12bit	10bit
Conversion Rate	50MS/s	50MS/s	50MS/s	14MS/s	50MS/s	10MS/s
SNDR	49.4dB	50.5dB	58.2dB	52.44dB	64dB	49.5dB
Power	1.44mW	6.9mW	9.9mW	15.8mW	18.4mW	1.1mW
DNL/INL	0.38/1.29	0.47/0.63	0.35/0.8	0.79/1.89	0.26/0.72	0.82/1.6
Active Area	0.123 mm^2	0.019mm^2	1.4mm^2	0.381mm^2	0.26mm^2	0.077mm^2
FOM(pJ/step)	0.12	0.5	0.3	3.3	0.28	0.45

$$FOM = \frac{Power}{2^{ENOB} \times Conversion\ rate}$$

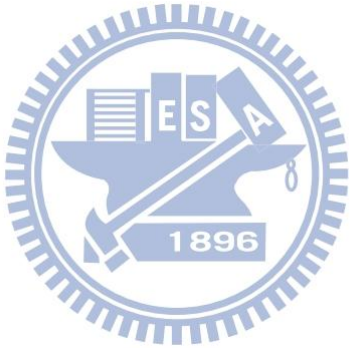
The low power 10bit, 10MS/s cyclic ADC was fabricated by 85nm 1P6M TSMC CMOS technology, and the chip size is 0.96×0.715 mm^2, the active area is 0.33×0.235mm^2. The techniques implemented in this design are summarized below:

(1) The conventional MDAC is replaced to flip-around SHA and residue amplifier can save power.

(2) Timing re-scheduled and 3.5bit conversion step to enhance conversion rate.

(3) Background calibration without extra residue amplifier to reduce power and chip area.

The total cyclic ADC consumes 1.1mW under 1.2V and 1V power supplies. It achieves 57.6dB SFDR and 49.5dB SNDR. DNL and INL are 0.82LSB and 1.6LSB, respectively. The ADC achieved good FOM of 0.45pJ/conv.-step at 10MS/s sampling rate and 1MHz sinusoidal input with 1.2 and 1V power supplies. There are some techniques which could improve the ADC performance. For example, more power can be saved by periodically turning on/off the calibration circuit.



REFERENCE

[1] B. Murmann, "ADC performance survey 1997-2012," *http://www.stanford.edu/~murmann/adcsurvey.html*.

[2] C. P. Hurrell, C. Lyden, D. Laing, D. Hummerston, and M. Vickery, "An 18b 12.5 MHz ADC with 93 dB SNR," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 378–379.

[3] K. Ohhata, K. Uchino, Y. Shimizu, K. Oyama, and K. Yamashita, "Design of a 770-MHz, 70-mW, 8-bit Subranging ADC Using Reference Voltage Precharging Architecture," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 2881–2890, Dec.2009.

[4] Y.-H. Chung and J.-T. Wu, "A CMOS 6-mW 10-bit 100-MS/s Two-Step ADC," in *Proc. IEEE Asian Solid-Sdtate Circuits Conference*, Nov. 2009, pp. 137–140.

[5] J. Hu, N. Dolev, and B. Murmann, "A 9.4-bit, 50-MS/s, 1.44-mW Pipelined ADC Using Dynamic Source Follower Residue Amplification," *IEEE J. Solid-State Circuits*, Vol. 44, pp. 1057-1066, Apr. 2009.

[6] B. Murmann and B. E. Boser, "A 12-b 75-MS/s pipelined ADC using open-loop residue amplification," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2040–2050, Dec. 2003.

[7] Y.-C. Huang and T.-C. Lee, "A 0.02-mm 9-Bit 50-MS/s Cyclic ADC in 90-nm Digital CMOS Technology," *IEEE J. Solid-State Circuits*, vol.45,no.3, pp.610-619, Mar. 2010.

[8] Y.-C. Huang and T.-C. Lee, "A 10b 100MS/s 4.5mW pipelined ADC with a time sharing technique," *ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 300-301.

[9] D.-L. Shen and T.-C. Lee, "A 6-bit 800-MS/s pipelined A/D converter with open-loop amplifiers," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 258-268, Feb. 2007.

[10] B.-G. Lee and R. M. Tsang, "A 10-bit 50 MS/s pipelined ADC with capacitor sharing and variable- opamp," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp.

883–890, Mar. 2009.

[11] I. Ahmed, J. Mulder, and D. A. Johns, “A low-power capacitive charge pump based pipelined ADC,” *IEEE J. Solid-State Circuits*, vol. 45, pp. 1016-1027, May 2010.

[12] S. W. M. Chen and R. W. Brodersen, “A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-μm CMOS,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 574–575.

[13] J. Yang, T. L. Naing, and R. W. Brodersen, “A 1-GS/s 6-bit 6.7-mW ADC in 65-nm CMOS,” in *Proc. IEEE CICC*, Sep. 2009, pp. 287–290.

[14] N. Sasidhar, Y.-J. Kook, S. Takeuchi, K. Hamashita, K. Takasuka, P.K. Hanumolu, and U.-K. Moon, “A low power pipelined ADC using capacitor and opamp sharing technique with a scheme to cancel the effect of signal dependent kickback,” *IEEE J. Solid-State Circuits*, vol.44, no. 9, pp. 2392–2401, Sep. 2009.

[15] J.-F. Lin, S.-J. Chang, C.-F. Chiu, H.-H. Tsai, and J.-J. Wang, “Low-power and wide-bandwidth cyclic ADC with capacitor and OPAMP reuse techniques for CMOS image sensor application,” *IEEE* Sensors Journal, vol. 9, no. 12, pp. 549-553, Dec. 2009.

[16] H. Hong and G. Lee, “A 65fJ/conversion-step 0.9-V 200-kS/s rail-to-rail 8-bit successive approximation ADC,” *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp.2161-2168, Jul. 2007.

[17] C.-C. Liu, S.-J. Chang, G.-Y. Huang and Y.-Z. Lin, “A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure,” *IEEE J.Solid-State Circuits*, vol. 45, no. 4, pp. 731-740, April 2010.

[18] C.-C. Liu, S.-J. Chang, G.-Y. Huang, Y.-Z. Lin, C.-M. Huang, C.-H. Huang, L. Bu, and C.-C. Tsai, “A 10b 100MS/s 1.13 mW SAR ADC with binary-scaled error compensation,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010. , pp. 386-387

[19] M. Furuta, M. Nozawa, and T. Itakura, “A 10-bit, 40-MS/s, 1.21 mW Pipelined SAR ADC Using Single-Ended 1.5-bit/cycle Conversion Technique,” *IEEE J.*

Solid-State Circuits, vol. 46, no. 6, pp. 1360-1370, June 2011.

[20] Y. J. Kim, H. C. Choi, G. C. Ahn, and S. H. Lee, "A 12b 50 MS/s CMOS Nyquist A/D converter with a fully differential class-AB switched op-amp," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 620–628, Dec. 2010.