國立交通大學

電子工程學系電子研究所碩士班

碩士論文

使用不易受偏移影響斜率偵測器之具有大輸入動態範圍可適性電纜等化器

Adaptive Equalizers with large Input Dynamic Range Using Offset-Insensitive Slope Detector

研 究 生：魏暐庭　　Wey-Tin Wei

指導教授：蔡嘉明　教授　　Prof. Chia-Ming Tsai

中 華 民 國 一 0 一 年 六 月

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摘　　要

本論文提出使用斜率偵測器之可適性等化器。此偵測機制可避免使用整流器而造成電路容易受偏移(offset)影響。而斜率偵測器會偵測訊號的斜率資訊用以判斷可適性等化器需要提供多少的增益補償。並且，使用了振幅偵測器及共模準位偵測器，增加可適性等化器所能承受的輸入動態範圍。為了使等化器可以減少功率消耗，提出了使用正迴授概念的等化器。而此可適性等化器使用了 65nm CMOS 製程做驗證，在 1.2 伏特的電壓供應器及 13.5Gb/s 的速度下，可補償 20.5dB 的通道損耗，並且只消耗了 14mW 的功率。並且在附錄 A 裡，描述一個使用了 0.18μm CMOS 製程做驗證的可適性等化器，在 1.8 伏特的電壓供應器及 6Gb/s 的速度下，可補償 23.3dB 的通道損耗，並且消耗了 27mW 的功率。

Adaptive Equalizers with large Input Dynamic Range Using Offset-Insensitive Slope Detector

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Abstract

The thesis presents adaptive equalizers using the slope detector. The detection mechanism avoids using the rectifiers for decreasing the sensitive of offset. The edge-speed is detected by slope detector to adjust the gain-boost of equalizer. Furthermore, with the help of swing detector and common-mode detector, it extends the input dynamic range of adaptive equalizer. In this work, we proposed the positive-feedback based adaptive equalizer to provide more gain-boost without scarifying the power consumption. This chip can work at 13.5Gb/s data rate, and compensates 20.5dB channel loss at Nyquist rate while consuming only 14mW (without output buffer) from a 1.2V power supply in 65nm CMOS technology. Furthermore, in the appendix A, we proposed a 6Gb/s adaptive equalizer using slope detector. It can compensate 23.3dB channel loss from a 1.2V power supply with 27mW power consumption in 0.18μm CMOS technology

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碩士班的生涯即將告一段落，誠摯的感謝求學期間所有協助過我的人。

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謹以此論文獻給摯愛的諸位。感謝你們。

魏暐庭

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Table of Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

With the rapidly-growing data communication of microprocessors and memories in recently years, the high speed data communication is an important issue in the modern technique. The conventional parallel communication becomes an inefficient way, because of it demands numerous transmission lines, pins and area which would increase the cost. Hence, the serial-link communication is a potential way for the high speed data communication. In the serial-link communication, the requirement of high bandwidth at I/O interface becomes the bottleneck, especially at tens Gb/s data rate. Consequently, the high speed adaptive equalizer plays a critical role in the serial-link communication for overcoming the inter-symbol interface (ISI) effect which resulted from the insufficient bandwidth. Furthermore, the insufficient bandwidth is caused by frequency-dependent loss of channel.

1.2 Wireline Communication

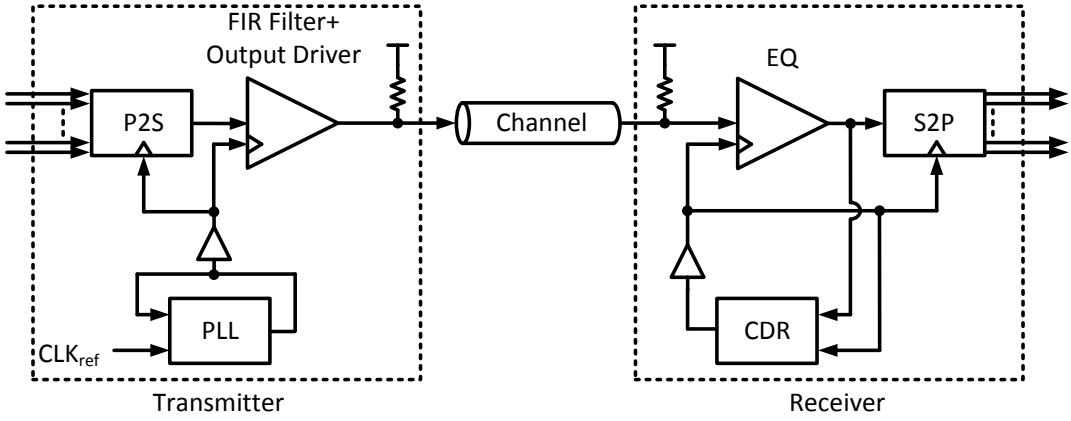


Fig. 1.1. Typical Serial Link Transceiver

For the high-speed application, the conventional parallel data communication is no longer useful. Because of numerous data pins increase loading which restricts the speed of data transferring. So, in the modern world, the high-speed serial link transceiver system is the popular system for high-data-rate wireline communication. Fig. 1.1 shows a typical serial link transceiver system. A typical serial link transceiver system consists three main parts: transmitter, channel and receiver.In the transmitter, a parallel-to-serial interface (P2S) would serialize parallel data to form serial data. A Phase-Locked Loop is an oscillator-generated signal which is phase and frequency locked to be a reference signal for the serial data. The finite impulse response (FIR) filter pre-distorts transmitted pulse in order to cancel the channel impulse response. And the output driver is designed for driving output loading, so it must provide sufficient driving current to produce enough output swing for the receiver.

The channel is responsible for delivering the serial data from the transmitter to the receiver. But the channel loss would degrade the high-frequency power of the

high-speed transferred data. The channel loss which caused by skin effect and dielectric loss will results in the high-speed transferred data suffers serious inter-symbol interface (ISI). The ISI will increase bit-error-rate (BER).

In the receiver, because of channel loss, we usually utilize equalizer (EQ) to compensate the high-frequency part of signal. In order to perform synchronous operation such as retiming and demultiplexing in random data, the receiver side demands a clock-and-data recovery (CDR). It can not only retime the data for less jitter, but also regenerate the noiseless data. And, at last, the serial data is deserialized to the parallel data by the serial-to-parallel interface (S2P).

As the mention before, for the high-speed serial data communication, we need to do equalization which can solve the effect of ISI. There are three ways to do equalization: pre-emphasis [1-2], linear equalizer (LEQ) [3-9] and decision feedback equalizer (DFE) [10-13]. The pre-emphasis is applied in the transmitter side. It pre-amplifies the high-frequency part of signal to resist the distortion which caused by channel. In the receiver side, LEQ and DFE are popular techniques to do equalization. The DFE can reduce the post-cursor and be more tolerable to noise. It also can retime the serial data to get smaller jitter and better signal-to-noise ratio. And there are some adaptive algorithms to be applied with DFE, such as least-mean-square (LMS). But DFE requires large digital schematicry and enormous power consumption for high-speed application. And it can’t equalize large channel loss which has resulted in small eye-opening. The LEQ, in contrast with DFE, is less power consumption and can compensate more channel loss. And there are also many the adaptive algorithms is popular and usable for LEQ to compensate different channel loss and robust to environment variation, like PVT variation. These different adaptive algorithms which had been published will be introduced in the later chapter.

1.3 Thesis Organization

This thesis is composed of six chapters.

Chapter 1 describes the background on the research topic and introduces wireline communication systems.

Chapter 2 describes the basic concepts of equalizer, and provides definition to commonly-used expressions, such as eye opening and jitter. In addition, this chapter will review the correlative research in recent years about the adaptive equalizers.

Chapter 3 introduces the design concept of slope detector.

Chapter 4 describes: “A 13.5Gb/s Positive-Feedback based Adaptive Equalizer with Large Dynamic Range Using Offset-Insensitive Slope-Detection”. The adaptive equalizer’s architecture and the design concept of positive-feedback based equalizer would be introduced with simulated results. Layout considerations are described and measured results are given. The chapter concludes with a comparison with recent related published works.

Chapter 5 gives a conclusion to this thesis, as well as a description of the potential possibilities of future research topics related to the works in this thesis.

Chapter 2

The Basic Concepts of Adaptive Equalizer

In this chapter, we introduce the necessarily basic concepts for analyzing and designing the adaptive equalizer. And then, we review the development of recently adaptive equalizer design, including linear equalizer (LEQ) schematics and adaptive algorithms.

2.1 Basic Concepts

2.1.1 Pseudo-Random Binary Sequence (PRBS)

A random binary data are composed with logical ZEROs and ONEs. If the time of one-bit is T_b seconds means the data rate is $1/T_b$ bits per second. The real random binary data may occur with the long string of consecutive logical ZEROs or ONEs. We call this string as “a low transition density”, also mean low speed. Such low transition density would make the trouble for the schematic design, like offset cancellation. So, we usually will specify the longest string of consecutive logical

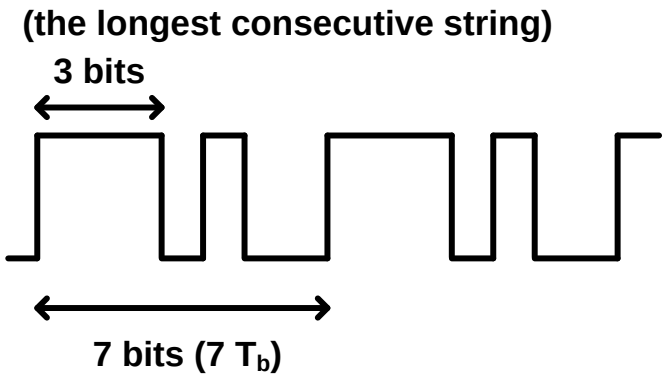


Fig. 2.1. The example of 2^3-1 PRBS.

ZEROs or ONEs. For the above reason, the pseudo-random binary sequence (PRBS) is the commonly used data pattern [14]. It can be generated by linear feedback shift register (LFSR) [15] which would generate a maximum sequence, 2^m-1 bits, and repeat the sequence again and again. Each sequence contains 2^{m-1}-1 ZEROs and 2^{m-1} ONEs, and the longest consecutive logical ZEROs or ONEs would equal to m bits. An example is depicted in Fig. 2.1.

2.1.2 Bandwidth requirement

In high-speed schematics design, how to design bandwidth is an important issue. The bandwidth trades with many other specifications, such as noise, power consumption and gain boost. For example, if we design a large bandwidth, the signal information can be preserved without distortion. But, in the meanwhile, the noise is also preserved which destroys the signal information. On the contrary, if we design a small bandwidth, although the noise could be decreased. But the signal is also distorted which is known as inter-symbol interface (ISI) [14] which due to insufficient bandwidth, insufficient

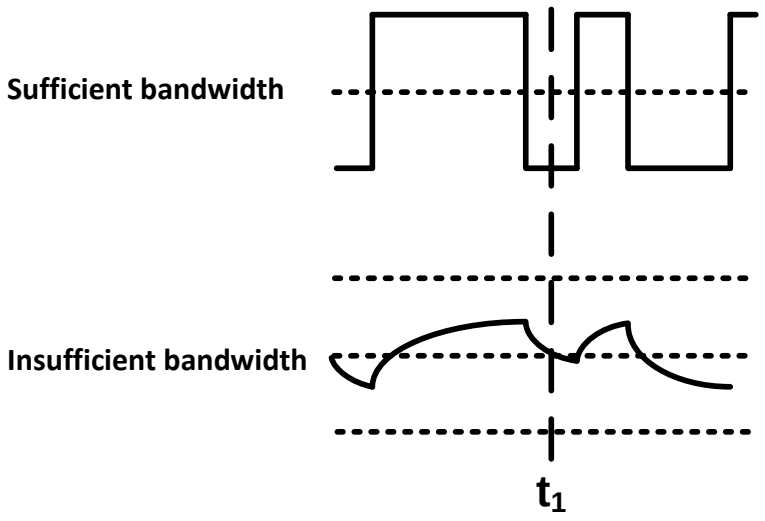


Fig. 2.2. Comparison between sufficient bandwidth and insufficient bandwidth.

phase linearity, and insufficient low-frequency cutoff, as depicted in Fig. 2.2. At t_1, the signal have the error bit. This undesired phenomenon would corrupt the voltage level of ZEROs and ONEs, and result in the error bits. The rule of thumb for optimum bandwidth is 0.7 of data rate, Eq. (2.1) [14-15]. However, for modern high-speed data communication, this rule of thumb is no longer suitable. Because of the trade-off between bandwidth, power consumption and other specifications in high-speed application, the recently published paper usually setting bandwidth to be 0.5 of data rate[4, 9, 16], especially when the data rate is more than 10Gb/s. Furthermore, we call the 0.5 of data rate to be “Nyquist rate”. And we always pay attention to how much gain boost can be provided by equalizer at the Nyquist rate in adaptive equalizer design.

2.1.3 Eye-diagram

An eye-diagram is formed by folding all of signal into a particular time. The eye-diagram could provide us a lot of useful signal information, such as ISI, noise,

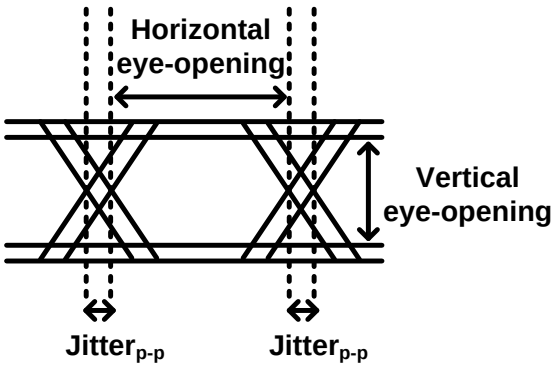


Fig. 2.3. Eye-opening.

signal slope and signal swing. And the eye-opening and jitter are the important specifications which can help us to judge the signal quality.

The eye-opening includes horizontal eye-opening and vertical eye-opening, as shown in Fig. 2.3. The horizontal eye-opening means the time interval which we successfully sample the signal's logical level. The vertical eye-opening means the tolerant noise for the signal, this can be explained by signal-to-noise ratio (SNR).

2.1.4 Jitter

Jitter is defined as the deviation of a timing event from its ideal position. We usually measure it from eye-diagram, and the peak-to-peak measurement is often used to represent the amount of jitter (jitter$_{p-p}$) which is shown in Fig. 2.3.

The jitter is composed with random jitter and deterministic jitter. The random jitter, as its name describing, is an unpredictable jitter. It's resulted from noise, such as thermal noise and flicker noise, which occurring from semiconductors and components. So, the random jitter can be well approximation by Gaussuan distribution, or called normal distribution. Because of that, we usually specify the random jitter by root-mean-square value which means the standard

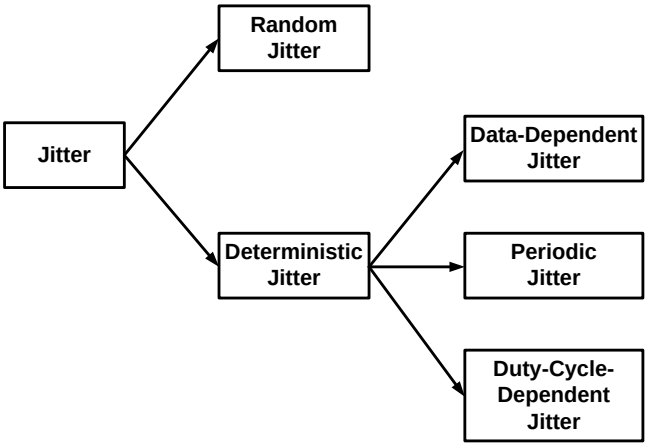


Fig. 2.4. Jitter classifications.

deviation of gaussian distribution. The deterministic jitter is a predictable jitter, and the peak-to-peak value is bounded. Furthermore, it can be divided into data-dependent jitter (DDJ), periodic jitter (PJ) and duty-cycle distortion jitter (DCDJ), as shown in Fig. 2.4. The value of DDJ is affected by the surrouding bits, in other word that is the ISI effect. The PJ is generated with the crosstalk. The DCDJ happens when the rising edges and falling edges of signal don't cross each other at decision threshold voltage.

2.1.5 Noise, SNR and BER

For the high-speed data communication, bit-error-rate (BER) which is defined as the ratio of number of error bits occurring to the number of transferred bits is a key issue. The BER is defined as

$$\mathrm{BER} = \frac{\text{the number of error bits}}{\text{the number of transferred bits}} \qquad (2.1)$$

For fitting in with a given BER. It can be designed by signal-to-noise ratio (SNR) [14], which is derived as

$$\mathrm{BER} = Q\left(\frac{V_{p-p}}{2V_{noise,rms}}\right) = Q\left(\frac{SNR}{2}\right) \qquad (2.2)$$

And the Q function is defined as:

$$Q(x) = \int_x^{\infty} \frac{1}{\sqrt{2\pi}} e^{(\frac{-u^2}{2})} du \qquad (2.3)$$

By the (2.2), for example, if we want the BER to be smaller than 10^{-12}, the SNR need to be larger than 14. That is to say when our signal swing is only $100mV_{p\text{-}p}$, the value of noise has only 7mV of tolerant range. In high-speed and low-power design, noise would be a serious limitation in the modern data communication. Thus, the BER can help us to know how much noise can be tolerated on the trade-off between noise and bandwidth, and power consumption.

2.1.6 Channel Characteristic and Modeling

As the description in chapter 1, we need a channel to transferred serial data from transmitter to receiver. The channel loss would degrade the high-frequency power of signal. The cause of channel loss are skin effect and dielectric loss. The skin effect causes the current tend to flow at the surface of conductor. This phenomenon results in more and more effective resistance for signal, especially at high frequency. The dielectric loss is resulted from the heating effect on the dielectric material.

When we model the channel loss, we also bring these two effects into the channel model. The channel model is shown in Fig. 2.5 [16].

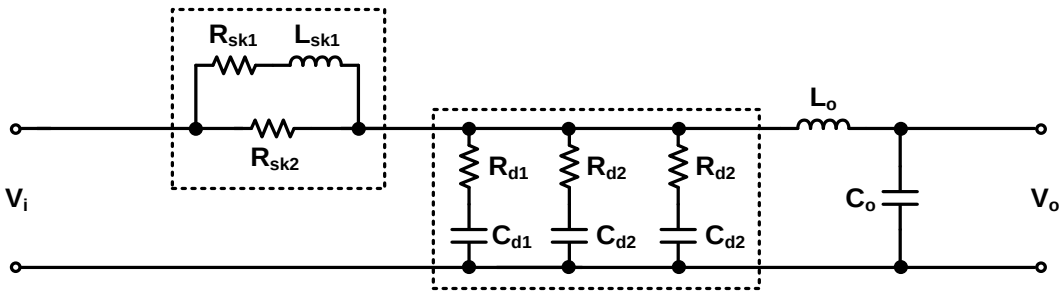


Fig. 2.5 Channel model with skin effect and dielectric loss consideration

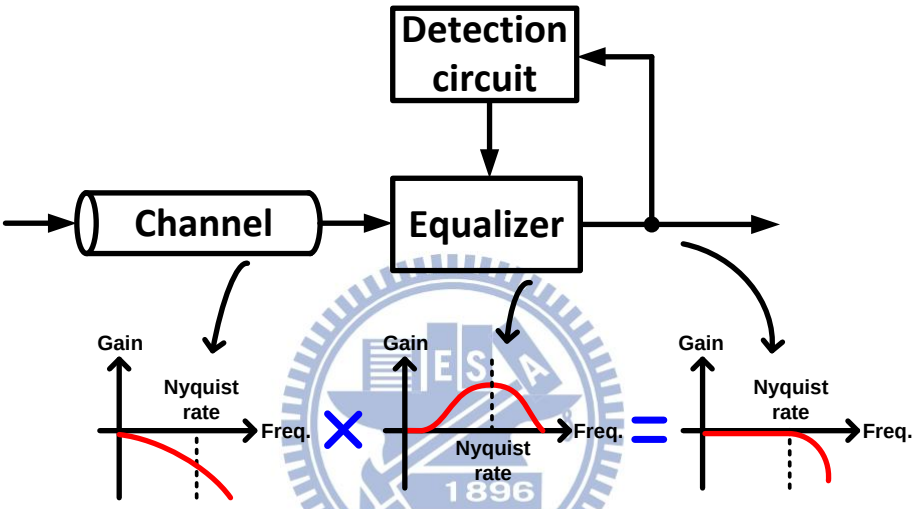


Fig. 2.6 Diagram of equalizer operation

2.1.7 Priciple of Adaptive Equalizer Operation

In the receiver equalization, the linear equalizer (LEQ) is usually called equalizer (EQ) for short. As Fig. 2.6 showing, the channel degrades the high-frequency gain of signal. Thus, we use EQ to compensate the channel loss from moderate-frequency to Nyquist rate. Because of the various channel loss when the channel length is changing, there is in want of a detection schematic to judge whether the channel loss is compensated well or not. If not, the detection schematic would adjust the gain-boost of EQ until the channel loss is compensated well.

2.2 High-frequency boosting technique review

2.2.1 RC degeneration technique

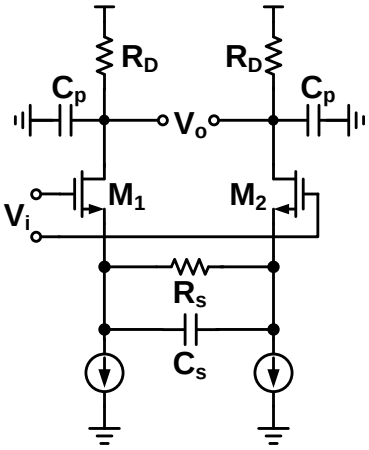


Fig. 2.7. Equalizing filter with RC degeneration technique.

A popular high-frequency gain boost approach is RC degeneration technique, as shown in Fig. 2.7. We obtain the transfer function as

$$\frac{V_o}{V_i}(s) = \frac{g_{m1}R_D}{1+\frac{g_{m1}R_S}{2}} \frac{1+\frac{s}{\omega_{z1}}}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} \qquad (2.4)$$

Where $\omega_{z1}=1/(R_SC_S)$, $\omega_{p1}=(1+g_{m1}R_S/2)/(R_SC_S)$, $\omega_{p2}=1/(R_DC_p)$, and g_{m1} means the transconductance of M_1 and M_2. Fig. 2.8 shows the magnitude response. However, this technique suffers the trade-off between maximum gain boost and DC gain. Because the ω_{p1} exceeds ω_{z1} by a factor of $(1+g_{m1}R_S/2)$, and the DC gain also decreases by the same factor. So, in the practical design, the RC degeneration technique needs utilize multiple cascaded stages to compensate large channel loss.

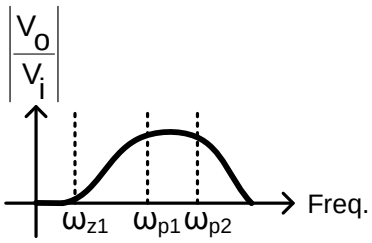


Fig. 2.8. Magnitude response of RC degeneration technique.

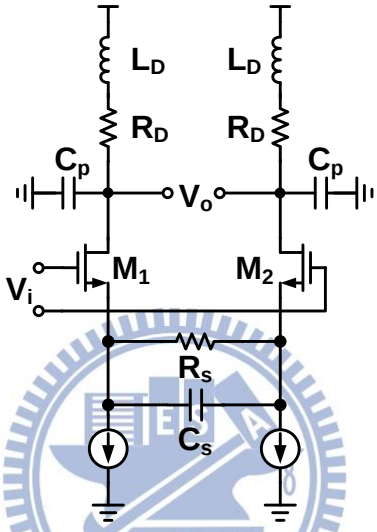


Fig. 2.9. Equalizing filter with inductive peaking technique.

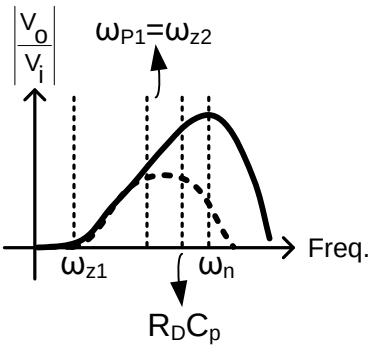


Fig. 2.10. Magnitude response of inductive peaking technique.

2.2.2Inductive peaking technique

To provide more gain boost at high-frequency, [4] brings up the improved capacitive degeneration techniqe which adding the inductive peaking technique, as shown in Fig. 2.9. We obtain the improved transfer function as

$$\frac{V_o}{V_i}(s) = \frac{g_{m1}R_D}{1+\frac{g_{m1}R_S}{2}} \frac{1+\frac{s}{\omega_{z1}}}{1+\frac{s}{\omega_{p1}}} \frac{1+\frac{s}{\omega_{z2}}}{(1+\frac{2\xi s}{\omega_n})(1+\frac{s^2}{\omega_n})} \qquad (2.5)$$

Where $\omega_{z2}=R_D/L$, $\xi = (R_D/2)\sqrt{C_p/L_D}$, $\omega_n = 1/\sqrt{C_p L_D}$, and $\omega_{z1}$and ω_{p1} remain the same equations. In ideal case, the inductive peaking technique can do the pole-zero cancellation of $\omega_{z2}$and ω_{p1}**.** It can help us obtain more gain boost at high-frequency. But the technique requires inductor which also indicating more area consumption.

2.3 Adaptive Equalizer Review

2.3.1 Adaptive equalizer with slope detectors [17]

The architecture of adaptive equalizer with slope-detectors is depicted in Fig. 2.11. The architecture uses a dual-paths equalizer which one path providing high-frequency gain boosting and the other one providing wide-bandwidth gain. And there are two slope detectors to detect the edge-speed of equalizer's output signal and slicer's output signal. The slicer generates a reference edge-speed for slope detector.

This architecture has two critical problems. The first problem is that this adaptive algorithm can't adapt different input swing, because of the reference signal' swing is fixed. That may cause the locking conditions are various for different input swings. The

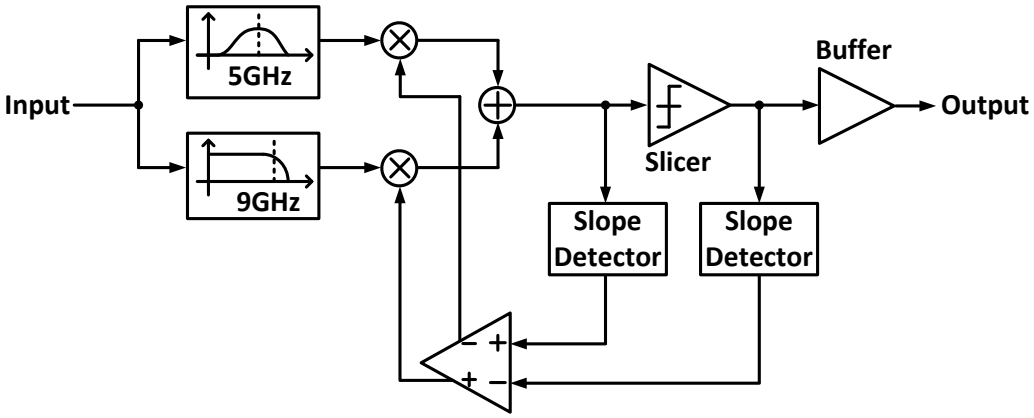


Fig. 2.11. Architecture of adaptive equalizer with slope detectors.

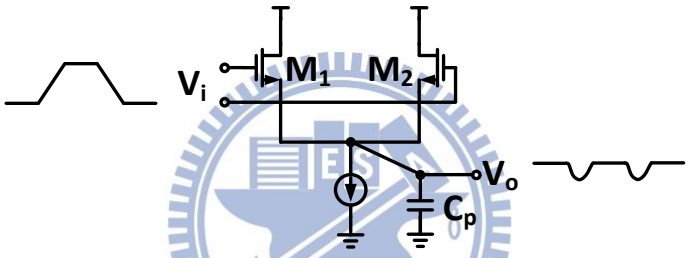
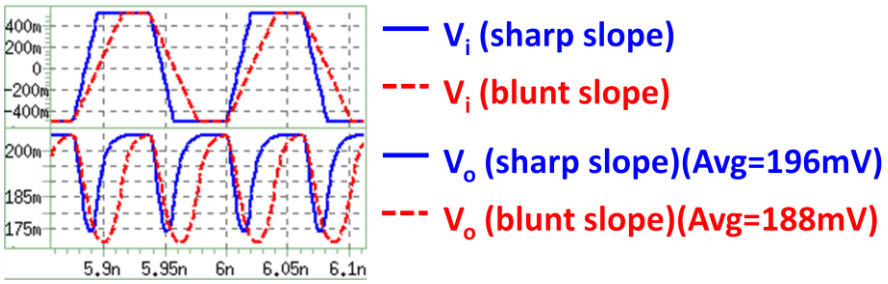
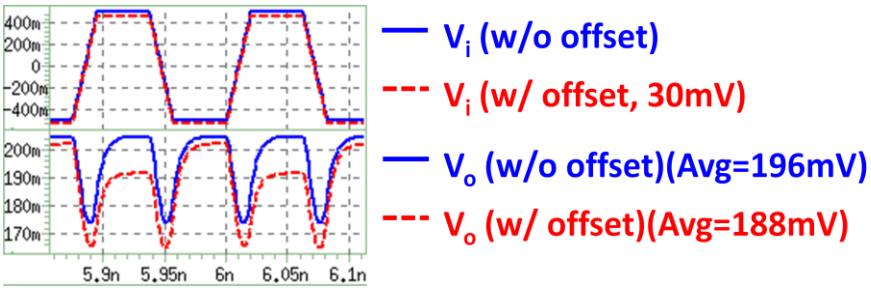


Fig. 2.12. Slope detector.

second problem is that the slope detectors are composed with rectifiers which are sensitive to offset. The slope detector is depicted in Fig. 2.12. The inputs are applied to the gate of M_1 and M_2. The V_o is extracted from the source of M_1 and M_2. Fig. 2.13(a) shows the comparison between sharp and blunt slope. The blunt slope has smaller average value (188mV) of V_o. Fig. 2.13(b) shows the comparison between w/o and w/ offset when the slopes are the same value. Because of the offset, V_o has the wrong average value (188mV) which would be considered as a blunt slope. Thus, the rectifier based slope detector is sensitive to offset.



(a)



(b)

Fig. 2.13. The transient response comparison of slope detector. (a) comparison between sharp and blunt slope (b) comparison between w/o and w/ offset

2.3.2 Adaptive equalizer using enhanced low-frequency gain control method [3]

The architecture of adaptive equalizer using enhanced low-frequency gain-control is shown in Fig. 2.14. The adaptive algorithm uses the comparator to generate a reference signal, and collocating with two adaptive loops. The high-frequency loop compares the high-frequency power of EQ filter's output signal and comparator's output signal, and then, adjusting the high-frequency gain boost of EQ filter. The low-frequency loop compares the low-frequency power of EQ filter's output signal and comparator's output signal, and then controlling the low-frequency gain of EQ filter.

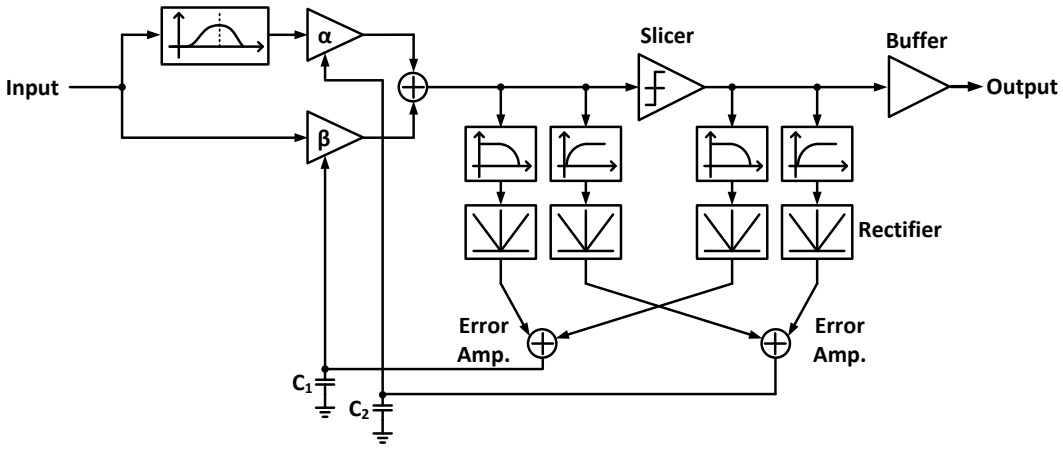


Fig. 2.14. Architecture of adaptive equalizer using enhanced low-frequency gain-control.

The additional low-frequency loop is design for conquering the drawback of adapting different input swings as the mentioned above.

However, the adaptive loops are still designed with rectifiers. And furthermore, the dual-loop would raise the stability issue.

2.3.3 Adaptive equalizer using direct measurement of the equalizer output amplitude [18]

As depicted in Fig. 2.15, the adaptive algorithm would equalize voltage amplitude of high-frequency and low-frequency components by measuring the equalizer output amplitude. And the output amplitude is measured by a full-wave rectifier which is shown in Fig. 2.16. In the ideal case, the low-frequency components, $V_{ave}(L)$, equal to V_{PP}, and the high-frequency components, $V_{ave}(H)$, equal to $(2/\pi)\times V_{PP}$. Hence, the locking condition of the adaptive algorithm is $V_{ave}(H)=(2/\pi)\times V_{ave}(L)$.

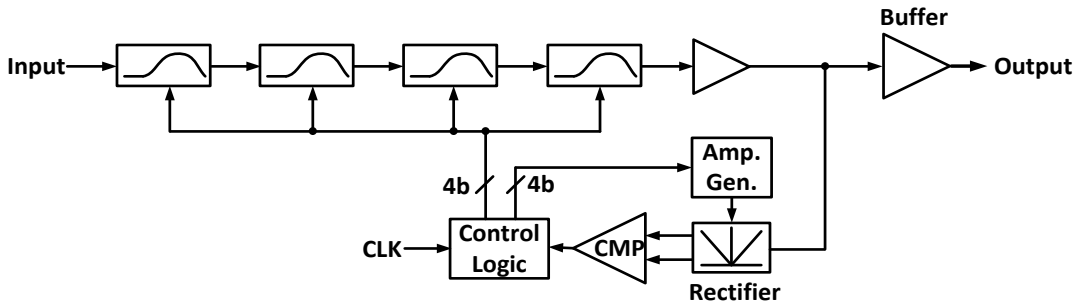


Fig. 2.15. Architecture of adaptive equalizer using direct measurement of the equalizer output amplitude.

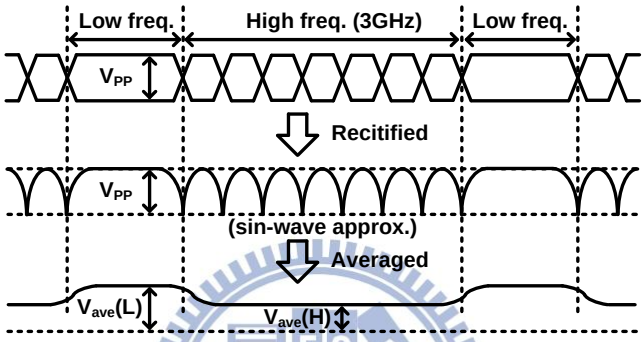


Fig. 2.16. The relation between high-frequency and low-frequency components.

However, due to the equalizer is control by digital logic, this may can't compensate any length of channel. And the algorithm needs external clock to help the digital control schematics, this would raise the design complexity.

2.3.4 Adaptive equalizer with spectrum-balancing technique

As depicted in Fig. 2.17, the adaptive equalizer incorporates spectrum-balancing technique and excludes the requirement of reference signal. The concept of the spectrum-balancing technique utilizes the ratio of high-frequency power over the low-frequency power. The locking condition is when P_H=P_L, as depicted in Fig. 2.18. The modified rectifier acts as a power detector, sensing when the power spectrum, and the V/I converter adjusts the gain-boost of the equalizing filter.

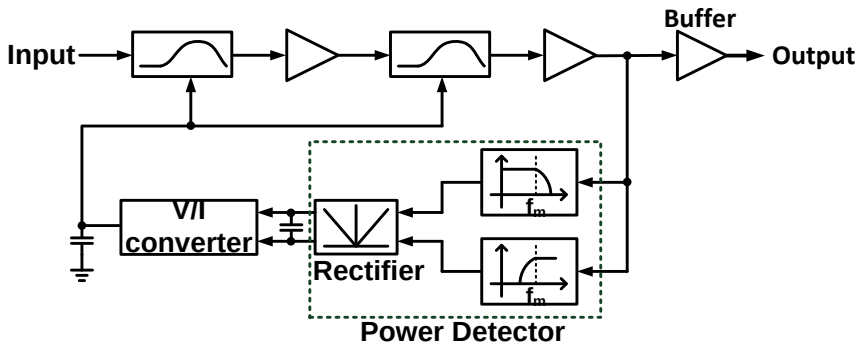


Fig. 2.17. Architecture of adaptive equalizer with spectrum-balancing technique.

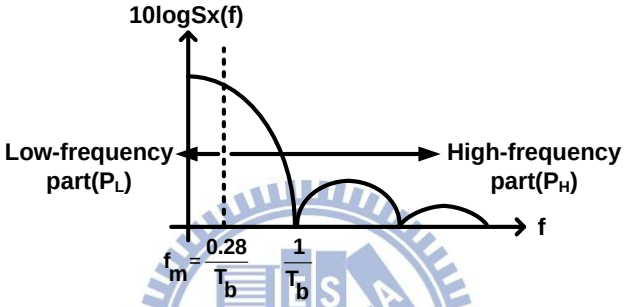


Fig. 2.18 Spectrum decomposition.

The spectrum balancing technique avoids the DC gain variation and swing issues of previous designs, because it can sense the low-frequency power. However, it requires precise design of the cutoff-frequency in power detector, f_m. Furthermore, it's also increasing the sensitive of PVT variation.

Chapter 3

The Design Concept of Slope Detector

3.1 Motivation

As described above, the detection mechanisms of previous published adaptive equalizers are usually employed with rectifiers. However, the rectifiers [3-4, 17-18] exhibit small detection gain and offset-sensitive. Moreover, they can’t suffer too small input swing, e.g. hundreds millivolts, or, a high-gain error amplifier is required. In addtion, many published detection mechanisms are proposed based on frequency-domain approach. These approaches demand precise frequency

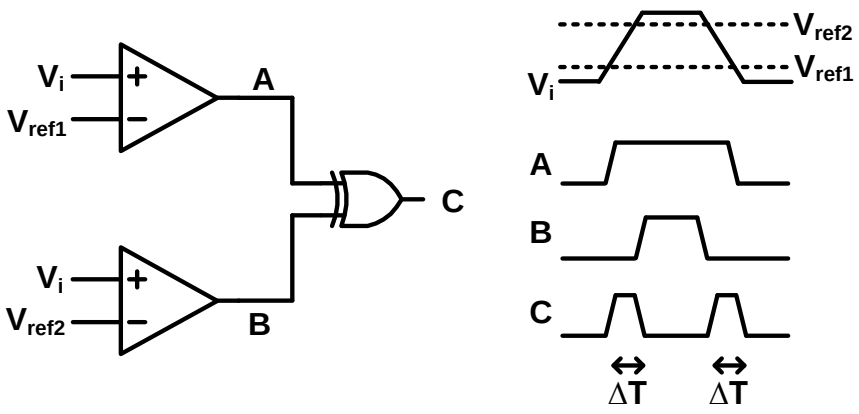


Fig. 3.1. The operation procedure of slope detector.

characteristics. Thus, we propose a time-domain approach which we call slope-detection technique. As the name called, we detect the slope of signal by the slope detector. With the slope information, we comprehend whether the signal requires more gain-boost.

3.2 The operation procedure of slope detector

Fig. 3.1 shows the operation procedure of slope detector [19-20]. Firstly, the slope detector requires two reference voltages, V_{ref1} and V_{ref2}. These two reference voltages compare with input signal (V_i), and then, the signals A and B are produced. The signal C is obtained from the signals of A and B by XOR gate. We derive the pulsewidth (ΔT) of signal C as:

$$\Delta T = \frac{V_{ref2} - V_{ref1}}{slope} = \frac{\Delta V_{ref}}{slope} \qquad (3.1)$$

With eq. (3.1), we obtain the slope, or calls edge-speed, of signal. Fig. 3.2 shows the comparison of ΔT between sharp slope and blunt slope. ΔT_s is narrower than ΔT_b.

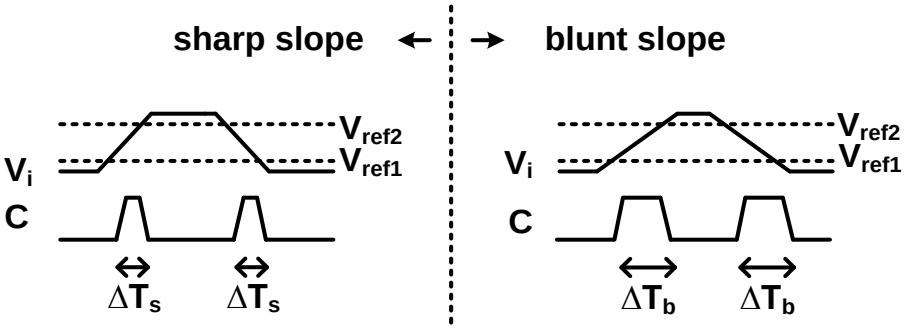


Fig. 3.2. The comparison between sharp slope and blunt slope.

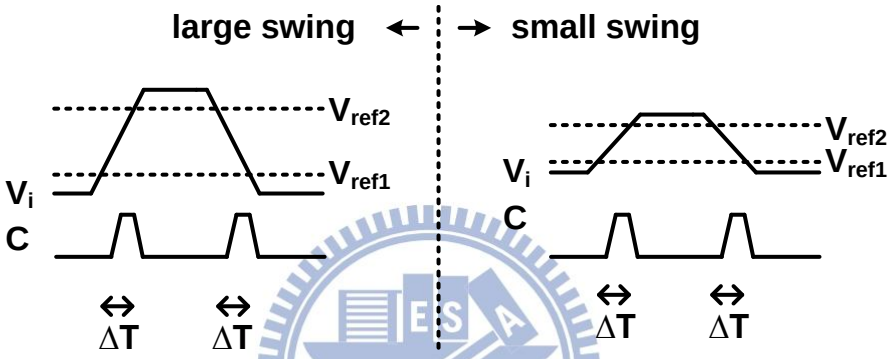


Fig. 3.3. The comparison between large swing and small swing.

In the adaptive equalizer applications, the input swing would be changed. For example, in USB 3.0 specification, the input swing range of receiver-end would be $400mV_{p\text{-}p}$ to $600mV_{p\text{-}p}$. Therefore, the adaptive equalizer needs to endure different input swing. However, when the signals' swing are different, the signals' slope are also different, as shown in Fig. 3.3. To obtain the same ΔT when input swings are different. V_{ref1} and V_{ref2} require to be adjusted with the different input swing. Hence, the slope detector can tolerate different input swing.

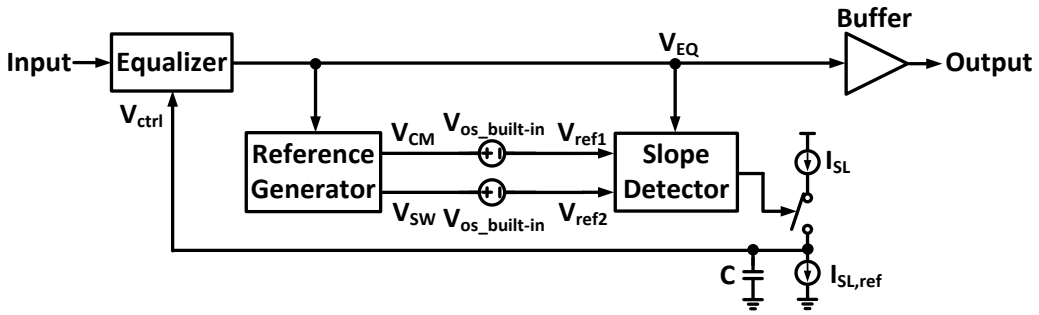


Fig. 3.4. The proposed architecture of adaptive equalizer using slope detector.

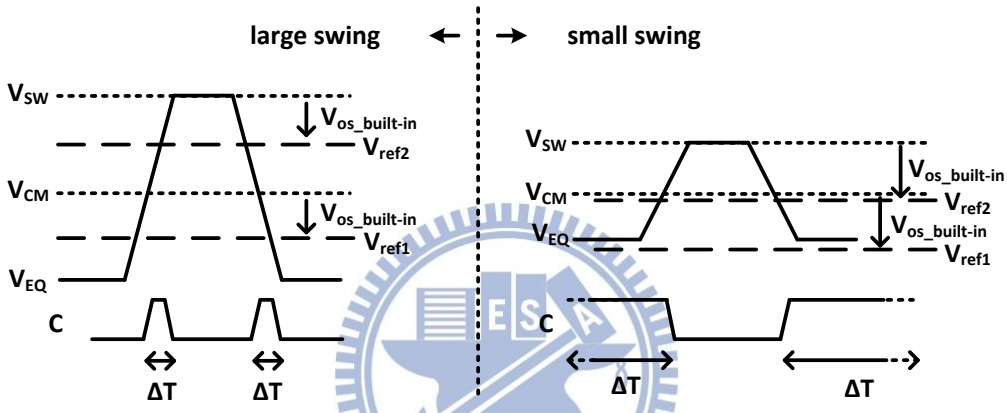
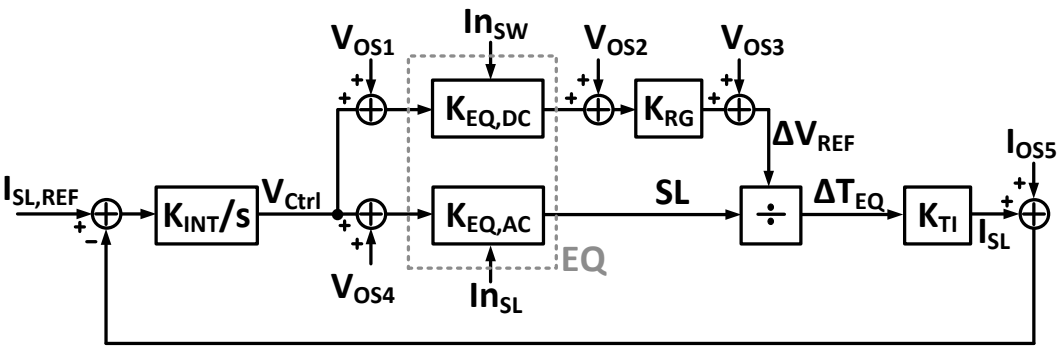


Fig. 3.5. The comparison between different swings when $V_{os\_built\text{-}in}$ is fixed.

Fig. 3.4 depicts the proposed architecture of adaptive equalizer using slope detector. The reference generator produces V_{CM} and V_{SW}. The slope detector generates the built-in offset ($V_{os\_built\text{-}in}$) for shifting V_{CM} and V_{SW} to be the V_{ref1} and V_{ref2}. At last, the slope information would be transformed to current by the switch and current source. Fig. 3.5 depicts the comparison between different swings when $V_{os\_built\text{-}in}$ is fixed. In the small swing, if the $V_{os\_built\text{-}in}$ is too large, ΔT would be the wrong value. Thus, $V_{os\_built\text{-}in}$ need to be smaller than $\frac{1}{2}\bullet(\text{input swing}_{\text{p-p}})$ for ensuring slope detector detects the correct ΔT. Furthermore, the proper relationship between $V_{os\_built\text{-}in}$ and swing is

$$V_{os\_built\text{-}in} = \frac{1}{4}\bullet(\text{input swing}_{\text{p-p}})$$



- INT : Integrator
- EQ : Equalizer
- RG : Reference Generator
- SLD : Slope Detector
- TI : time-to-current converter
- SW: the swing of signal
- SL : the slope of signal
- V_{OS1} : input-referred offset of $K_{EQ,LF}$
- V_{OS2} : input-referred offset of K_{RG}
- V_{OS3} : input-referred offset of SLD
- V_{OS4} : input-referred offset of $K_{EQ,HF}$
- I_{OS5} : input-referred offset of summer
- In_{SW}: the swing of input signal
- In_{SL} : the slope of input signal

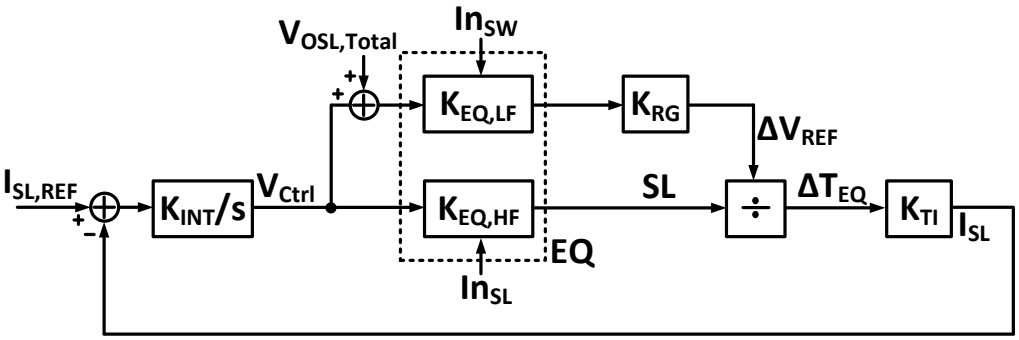
Fig. 3.6. The linear model of adaptive equalizer using slope detector with offset consideration.

Fig. 3.6 depicts a simple model of adaptive equalizer which includes the offset sources. For analyzing the offset sensitivity, we merge all offset sources into one equivalent offset source, as shown in Fig. 3.7. Fig. 3.7(a) show the equivalent model with input referred offset ($V_{OSL,Total}$) at the low-frequency path. The I_{SL} is derived as

$$I_{SL} = \frac{\left[\frac{K_{INT}}{s}\frac{K_{EQ,LF}K_{RG}K_{TI}}{K_{EQ,HF}} + V_{OSL,Total}K_{EQ,LF}K_{RG}K_{TI}\right]}{1+\left[\frac{K_{INT}}{s}\frac{K_{EQ,LF}K_{RG}K_{TI}}{K_{EQ,HF}} + V_{OSL,Total}K_{EQ,LF}K_{RG}K_{TI}\right]} I_{SL,REF}$$

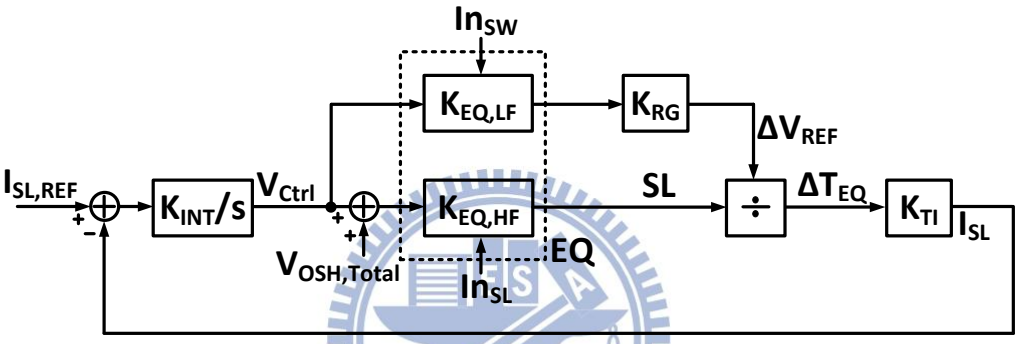
Hence, the sensitive is

$$\text{Sensitivity}_{V_{OSL,Total}}^{I_{SL}} = \frac{V_{OSL,Total}K_{EQ,LF}K_{RG}K_{TI}}{\left[(K_{EQ,LF}K_{RG}K_{TI})^2 \cdot (\frac{K_{INT}}{s \cdot K_{EQ,HF}} + V_{OSL,Total})^2\right] + \left[(K_{EQ,LF}K_{RG}K_{TI}) \cdot (\frac{K_{INT}}{s \cdot K_{EQ,HF}} + V_{OSL,Total})\right]}$$



$$V_{OSL,Total} = \frac{I_{OS5}}{K_{EQ,LF}K_{RG}K_{TI}} + \frac{V_{OS3}}{K_{EQ,LF}K_{RG}} + \frac{V_{OS2}}{K_{EQ,LF}} + V_{OS1}$$

(a)



$$V_{OSH,Total} = \frac{I_{OS5}}{\frac{K_{TI}}{K_{EQ,HF}}} + V_{OS2}$$

(b)

Fig. 3.7. The linear model for offset sensitivity analysis. (a) the offset effect at low-frequency path (b) the offset effect at high-frequency path

From the above equation, we know $K_{EQ,LF}$, K_{RG}, K_{INT} and K_{TI} need to be as large as possible for suppressing the offset effect.

Fig. 3.7(b) show the equivalent model with input referred offset ($V_{OSH,Total}$) at the high-frequency path. The I_{SL} is derived as

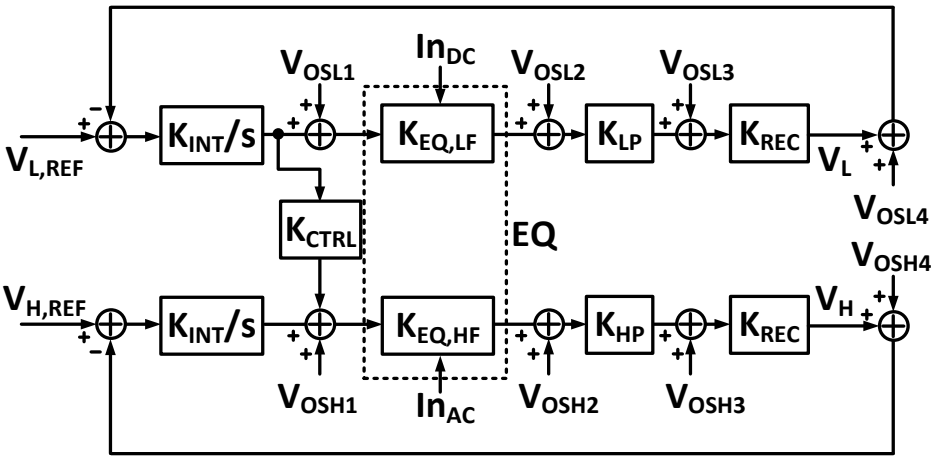


Fig. 3.8. The linear model of adaptive equalizer using duo-loop control with offset consideration.

$$I_{SL} = \frac{\left[\frac{K_{INT}}{s}\frac{K_{EQ,LF}K_{RG}K_{TI}}{K_{EQ,HF}} + \frac{K_{TI}}{K_{EQ,LF}}\frac{1}{V_{OSH,Total}}\right]}{1+\left[\frac{K_{INT}}{s}\frac{K_{EQ,LF}K_{RG}K_{TI}}{K_{EQ,HF}} + \frac{K_{TI}}{K_{EQ,LF}}\frac{1}{V_{OSH,Total}}\right]} I_{SL,REF}$$

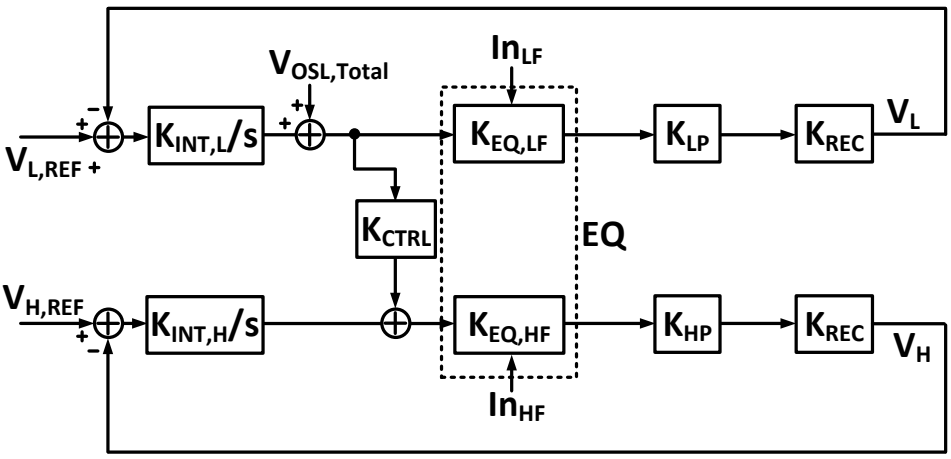
Hence, the sensitive is

$$\text{Sensitivity}_{V_{OSH,Total}}^{I_{SL}}$$

$$= \frac{-\frac{K_{TI}}{K_{EQ,LF}}\frac{1}{V_{OSH,Total}}}{\left[(\frac{K_{TI}}{K_{EQ,LF}})^2 \cdot (\frac{K_{INT}K_{EQ,LF}K_{RG}}{s \cdot K_{EQ,HF}} + \frac{1}{V_{OSH,Total}})^2\right] + \left[(\frac{K_{TI}}{K_{EQ,LF}}) \cdot (\frac{K_{INT}K_{EQ,LF}K_{RG}}{s \cdot K_{EQ,HF}} + \frac{1}{V_{OSH,Total}})\right]}$$

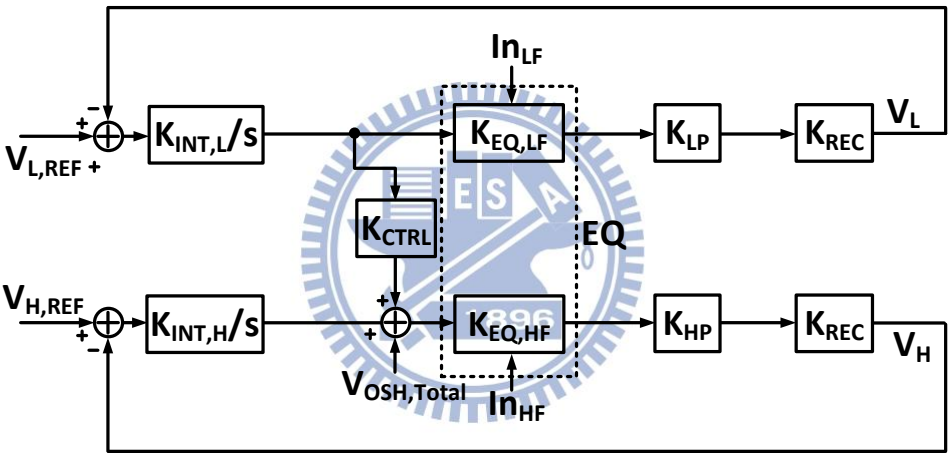
From the above equation, we know $K_{EQ,LF}$, K_{RG}, K_{INT} and K_{TI} also need to be as large as possible for suppressing the offset effect.

For comparing with the conventional adaptive equalizer, Fig. 3.8 depicted the inear model of adaptive equalizer using duo-loop control [3], which also including the offset consideration. Similarly, all the offset sources are merged in two cases, as shown in Fig. 3.9. In Fig. 3.9(a), V_L is derived as



$$V_{OSL,Total} = \frac{V_{OSL4}}{K_{EQ,LF}K_{LP}K_{REC}} + \frac{V_{OSL3}}{K_{EQ,LF}K_{LP}} + \frac{V_{OSL2}}{K_{EQ,LF}} + V_{OSL1}$$

(a)



$$V_{OSH,Total} = \frac{V_{OSH4}}{K_{EQ,HF}K_{HP}K_{REC}} + \frac{V_{OSH3}}{K_{EQ,HF}K_{HP}} + \frac{V_{OSH2}}{K_{EQ,HF}} + V_{OSL,Total}K_{CTRL} + V_{OSH1}$$

(b)

Fig. 3.9. The linear model for offset sensitivity analysis. (a) the offset effect at low-frequency path (b) the offset effect at high-frequency path

$$V_L = \frac{\left[\frac{K_{INT,L}}{s}K_{EQ,LF}K_{LP}K_{REC} + V_{OSL,Total}K_{EQ,LF}K_{LP}K_{REC}\right]}{1+\left[\frac{K_{INT,L}}{s}K_{EQ,LF}K_{LP}K_{REC} + V_{OSL,Total}K_{EQ,LF}K_{LP}K_{REC}\right]}V_{L,REF}$$

Hence, the sensitive is

$$\text{Sensitivity}_{V_{OSL,Total}}^{V_L} = \frac{K_{EQ,LF}K_{LP}K_{REC}V_{OSL,Total}}{\left[(K_{EQ,LF}K_{LP}K_{REC})^2 \bullet (\frac{K_{INT,L}}{s} + V_{OSL,Total})^2\right] + \left[(K_{EQ,LF}K_{LP}K_{REC}) \bullet (\frac{K_{INT,L}}{s} + V_{OSL,Total})\right]}$$

From the above equation, we know $K_{EQ,LF}$, K_{LP}, K_{REC} and K_{INT} need to be as large as possible for suppressing the offset effect.

Fig. 3.9(b) show the equivalent model with input referred offset ($V_{OSH,Total}$) at the high-frequency path. The V_H is derived as

$$V_H = \frac{\left[\frac{K_{INT,H}}{s}K_{EQ,HF}K_{HP}K_{REC} + K_{EQ,HF}K_{HP}K_{REC}V_{OSH,Total}\right]}{1+\left[\frac{K_{INT,H}}{s}K_{EQ,HF}K_{HP}K_{REC} + K_{EQ,HF}K_{HP}K_{REC}V_{OSH,Total}\right]}V_{H,REF} + \frac{\left[\frac{K_{INT,L}}{s}K_{CTRL}K_{EQ,HF}K_{HP}K_{REC}\right]}{1+\left[\frac{K_{INT,L}}{s}K_{EQ,LF}K_{LP}K_{REC}\right]}V_{L,REF}$$

Hence, the sensitive is

$$\text{Sensitivity}_{V_{OSH,Total}}^{V_H} = \frac{K_{EQ,HF}K_{HP}K_{REC}V_{OSH,Total}}{\left[(K_{EQ,HF}K_{HP}K_{REC})^2 \bullet (\frac{K_{INT,H}}{s} + V_{OSH,Total})^2\right] + \left[(K_{EQ,HF}K_{HP}K_{REC}) \bullet (\frac{K_{INT,H}}{s} + V_{OSH,Total})\right]}$$

From the above equation, we know $K_{EQ,HF}$, K_{HP}, K_{REC} and K_{INT} also need to be as large as possible for suppressing the offset effect.

However, the K_{REC} is quite small in this adaptive mechanism. Thus, our proposed architecture is more insensitive to offset due to the K_{TI} can be quite large.

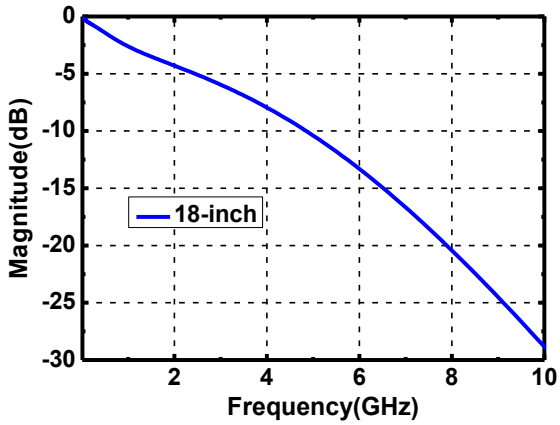
Chapter 4

A 13.5Gb/s Positive-Feedback based Adapative Equalizer with Large Input Dynamic Range Using Offset-Insensitive Slope Detector

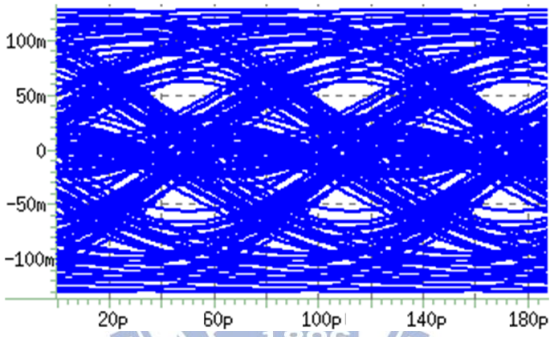
4.1 Motivation

With the progress in communication transmission, the operation data rate increases up to tens of Gb/s is the predictable trend in the future days. The power consumption is important issues in the schematic design, especially the equalizer schematic. This work proposes a positive-feedback based equalizer which regenerating gain at high-frequency for saving power consumption. Moreover, to decrease area consumption, the equalizer doesn’t use inductive peaking technique.

4.2 Specification



(a)



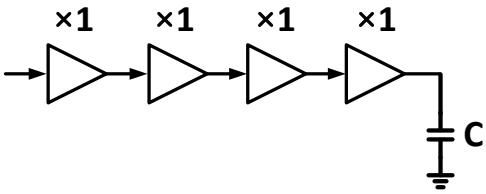
(b)

Fig. 4.1. (a) The magnitude response of 18-inch channel

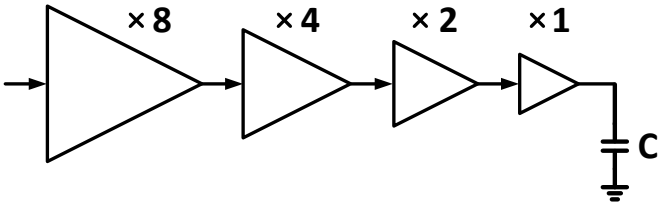
(b) The Transient response of 18-inch channel

In this work, we utilize 65nmCMOS technology. Due to the testing instruments limitations, the data rate is set at 16Gb/s. The channel loss of 18-inch is 21dB at 8GHz, as shown in Fig. 4.1. Fig. 4.2 shows the eye-diagram under 18-inch.

We utilizes four cascaded differential pair to compensate 21dB channel loss, and the reverse scaling technique [16] are used. We compare the performance between with and without revers scaling, as shown in Fig 4.2. In Fig. 4.2(b), the reverse scaling factor



(a)



(b)

Fig. 4.2. Cascading four differential pairs to compensate 18-inch channel.

(a) Without reverse scaling technique

(b) With reverse scaling technique

Table 4.1 The comparison between without and with reverse scaling.

	w/o reverse scaling	**w/ reverse scaling**
DC-Gain*	**1**	**1**
Bandwidth*	**0.56**	**1**
Output noise*	**2**	**1**
Power*	**0.27**	**1**

*** Normalized based on the value of w/ reverse scaling**

is 2. Table 4.1 shows the overall performance of Fig. 4.2 (a) and (b). It reveals the revers scaling technique can provide better bandwidth and noise performance.

4.3 Circuit Design

4.3.1 Equalizer

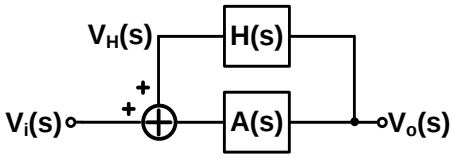


Fig. 4.3. The block diagram of positive-feedback system.

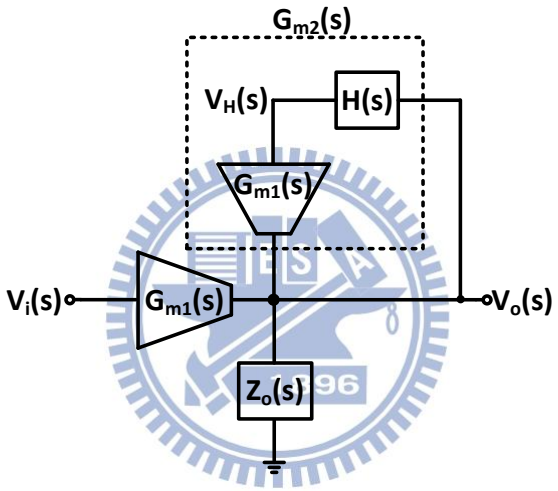
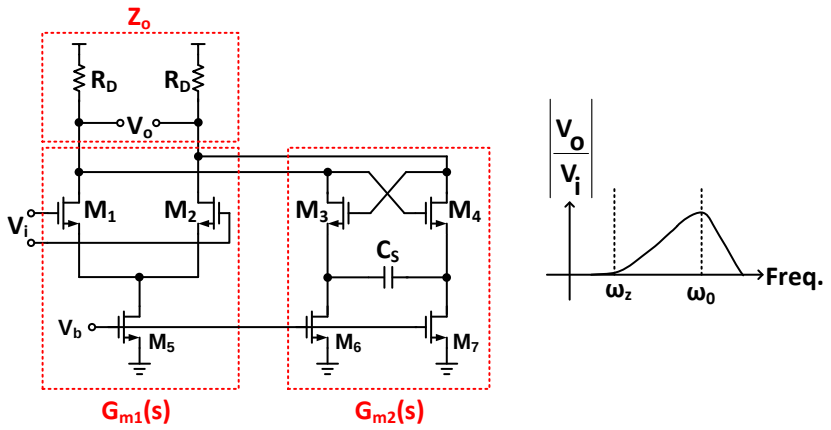


Fig. 4.4. The improved positive-feedback system.

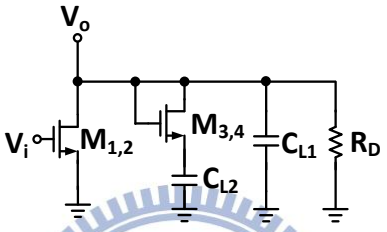
Fig. 4.3 shows a basic positive-feedback system. For more detail analysis in the positive-feedback, the adder and A(s) are replaced by $G_{m1}(s)$ and $Z_o(s)$, as shown in Fig. 4.4. The transfer function is derived as

$$\frac{V_o(s)}{V_i(s)} = G_{m1}(s) \bullet Z_o(s) \frac{1}{1 - G_{m1}(s) \bullet H(s) \bullet Z_o(s)} = G_{m1}(s) \bullet Z_o(s) \frac{1}{1 - G_{m2}(s) \bullet Z_o(s)} \qquad (4.2)$$

where $G_{m1}(s)$ and H(s) are merged as $G_{m2}(s)$. As long as $G_{m2}(s) \cdot Z_o$ to be close to 1, the closed-loop gain reaches infinity. For example, if $G_{m1}(s) \cdot Z_o(s)$ is 1, as long as $G_{m1}(s) \cdot Z_o(s)$ is 0.5, the gain would be 2. Unlike RC degeneration technique, the DC-gain need to be 2 for generating gain-boost of 2.



(a)



(b)

Fig. 4.5. (a)The basic implemented schematic and magnitude response of positive-feedback based equalizer. (b) the half-circuit of (a)

A basic schematic of the positive-feedback based equalizer is implemented, as shown in Fig. 4.5(a). M_1, $M_2$and M_5 realize $G_{m1}(s)$. M_3, M_4, M_6, M_7 and C_S realize $G_{m2}(s)$. And the Z_o is realized by R_D and C_p. From Fig. 4.5(b), we derive the transfer function as :

$$\frac{V_o(s)}{V_i(s)} = \frac{g_{m1,2}}{C_{L1}} \frac{s+\omega_z}{s^2 + s\frac{\omega_0}{Q} + \omega_0^{\,2}} \qquad (4.3)$$

$$\omega_z = \frac{g_{m3,4}}{2C_s + C_{L2}} \ , \ \omega_0 = \sqrt{\frac{g_{m3,4}}{C_{L2}(2C_s + C_{L2})}}$$

$$\frac{\omega_0}{Q} = \frac{g_{m3,4}R_D C_{L1} + (2C_s + C_{L2}) - g_{m3,4}R_D(2C_s + C_{L2})}{C_{L2}(2C_s + C_{L2})}$$

where $g_{m1,2}$ means the transconductance of M_1 and M_2, $g_{m3,4}$ means the transconductance of M_3 and M_4, $g_{ds6,7}$ means the reciprocal of M_6 and M_7's output resistor, $C_{L1}=C_{gd1,2}+4C_{gd3,4}+C_{p,Vo}$, $C_{L2}=2C_{gs3,4}+C_{gd6,7}+2C_s+C_{p,Vs3,4}$. As the transfer function showing, not only ω_z provide peaking, but also complex poles (Q) generate peaking. As the magnitude response showing in Fig. 4.5, ω_z provides low-frequency gain-boost and the complex poles (Q) provide gain-boost at high-frequency.

Considering the stability of positive-feedback, the complex poles' real parts couldn't be positive. The complex poles are derived as

$$s=\frac{-\frac{\omega_0}{Q}\pm\sqrt{(\frac{\omega_0}{Q})^2-(2\omega_0)^2}}{2}$$

Thus,

$$\frac{\omega_0}{Q}=\frac{g_{m3,4}R_DC_{L1}+(2C_s+C_{L2})-g_{m3,4}R_D(2C_s+C_{L2})}{C_{L2}(2C_s+C_{L2})}\geq 0$$

$$\Rightarrow g_{m3,4}R_D\leq\frac{2C_s+C_{L2}}{2C_s+C_{L2}-C_{L1}},\ \text{where}\ \frac{2C_s+C_{L2}}{2C_s+C_{L2}-C_{L1}}\approx 1$$

$$\Rightarrow g_{m3,4}R_D\leq 1$$

Hence, as long as $g_{m3,4}R_D\leq 1$, ω_0/Q would be larger than 0. This can confirm the positive-feedback system to be stable.

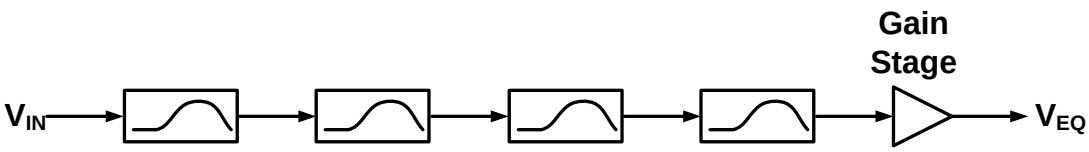


Fig. 4.6. Block diagram of Equalizer.

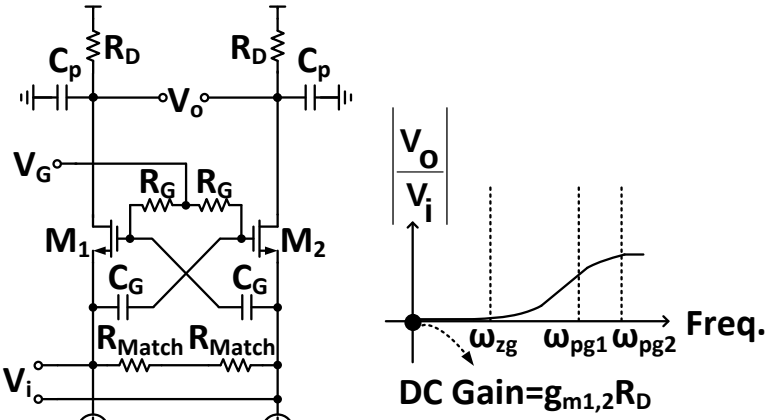


Fig. 4.7. The schematic and magnitude response of gm-boosted technique.

Fig. 4.6 depicts the proposed equalizer which is composed with five stages, including four peaking stages and one gain stage. The first four stages providing about 20dB gain-boost, and the last stage operates as a buffer to decreasing the loading effect. The first stage not only uses positive-feedback based equalizer, but also utilizing the gm-boosted technique [21-22] for providing large peaking at high frequency. This stage has a 8dB of gain-boost at 8GHz. The second stage combines RC degeneration technique with positive-feedback based technique. It also has a 8dB of gain-boost at 8GHz. The third stage only utilizes positive-feedback based technique, which provides a 6dB of gain-boost at 8GHz. The fourth stage also uses positive-feedback based technique, however, it provides low-frequency gain-boost and delay equalization. The fifth stage operates as a buffer to isolate the loading effect from the following circuits.

The basic gm-boosted technique schematic is depicted in Fig. 4.7. The transfer

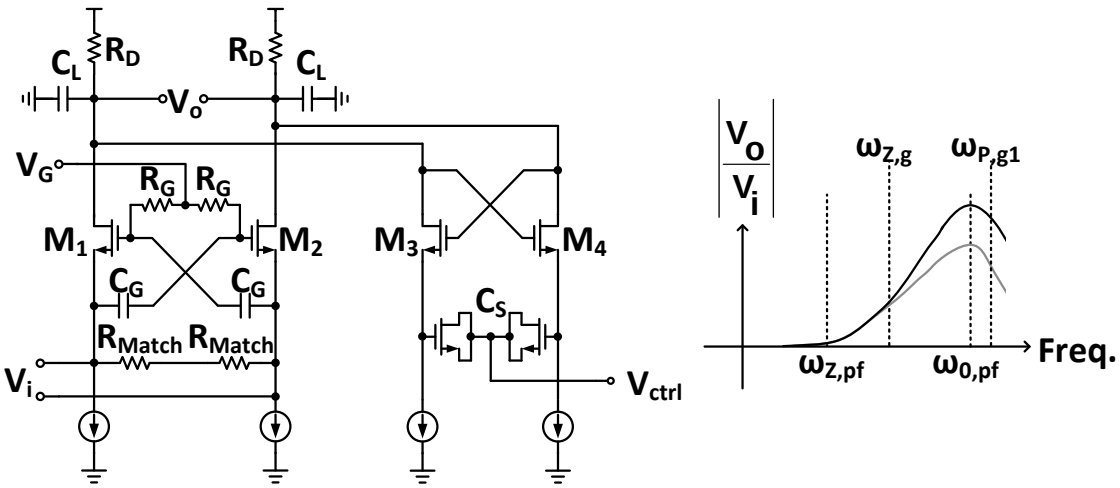


Fig. 4.8. The schematic and magnitude response of the first stage.

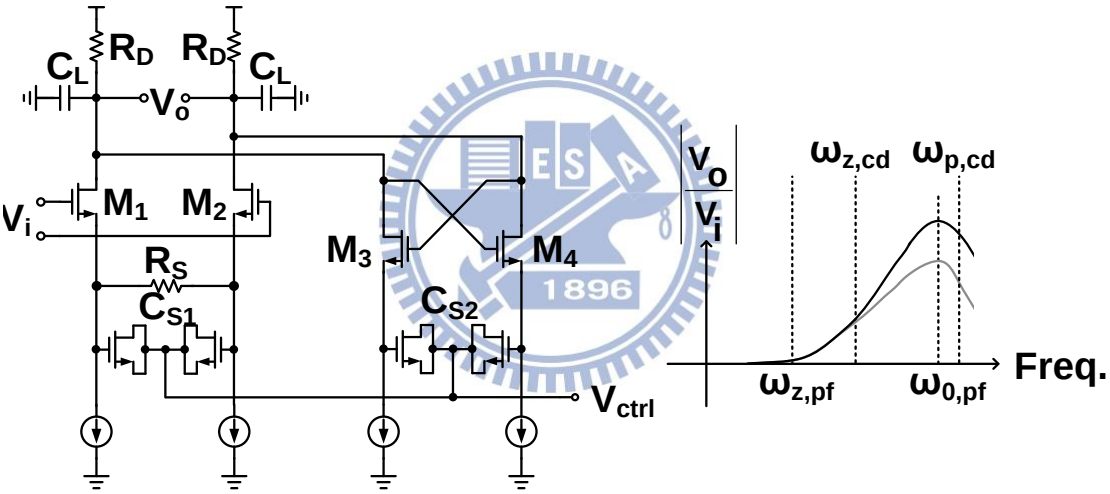


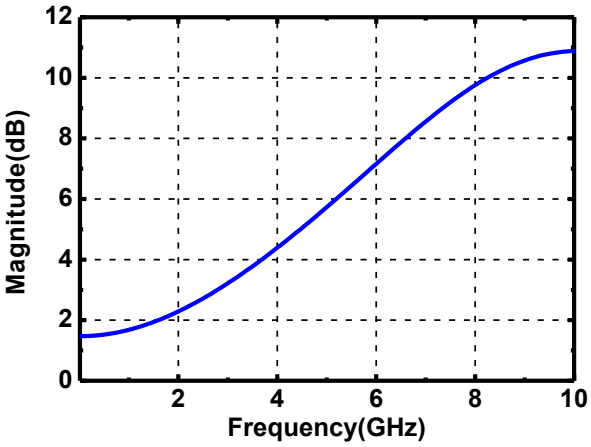
Fig. 4.9. The schematic and magnitude response of the second stage.

function is derived as:

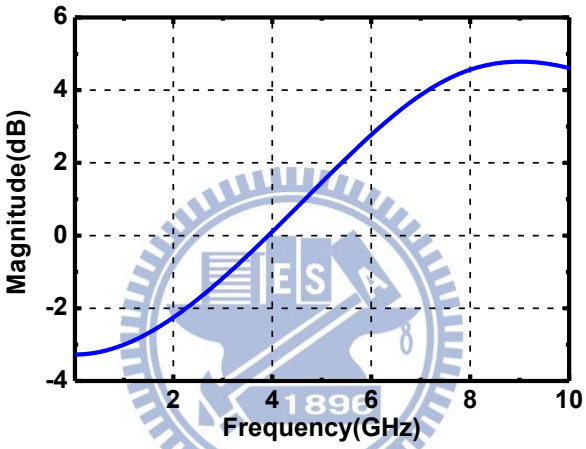
$$\frac{V_o(s)}{V_i(s)} = \frac{(s+\omega_{z,g})}{(s+\frac{1}{\omega_{p1,g}})(s+\frac{1}{\omega_{p2,g}})} 2g_{m1,2}R_D \quad (4.4)$$

$$\omega_{z,g} = \frac{1}{2R_GC_G},\ \omega_{p1,g} = \frac{1}{R_GC_G},\ \omega_{p2,g} = \frac{1}{R_DC_L}$$

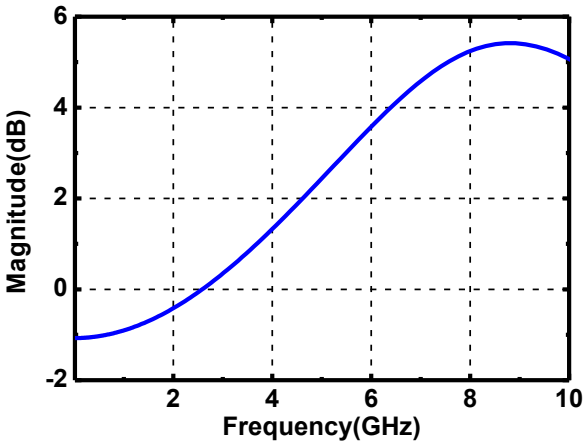
where $g_{m1,2}$ means the transconductance of M_1 and M_2.The magnitude response is also



(a)



(b)



(c)

Fig. 4.10. The magnitude response of the first three stage.

(a) the first stage (b) the second stage (c) the third stage

shown in Fig. 4.7, which $\omega_{p1,g}$ is two times of $\omega_{z,g}$. Moreover, the gm-boosted technique can only utilized at the first stage, due to the input node is a low input impedance. The proposed schematic of first stage is shown in Fig. 4.8. The R_{Match} is designed for matching 50Ω impedance of the instrument. $\omega_{z,pf}$ and $\omega_{z,g}$ are designed at 3.6GHz and 6.8GHz. And, the Q is about 2.5. Fig. 4.9 shows the schematic of the second stage. In this stage, $\omega_{z,pf}$ and $\omega_{z,cd}$ are designed at 4GHz and 6GHz. And, the Q is about 2.3. The third and the fourth stages use the basic schematics of positive-feedback based equalizer, which has been shown in Fig. 4.5. In the third stage, $\omega_{z,pf}$ is designed at 5GHz. And, the Q is about 2. The simulated magnitude response of the first three stages are shown in Fig. 4.10. As described above, the first stage provides 8dB of gain-boost, the second stage provides 8dB of gain-boost, and the third stage provides 6dB of gain-boost.

Specifically, the fourth stage is designed for both magnitude and delay equalization [23]. Due to Q is utilized in the previous stages for large gain-boost at high-frequency, the group-delay has large difference between low-frequency and high-frequency. According to eq. (4.3), the transfer function of fourth stage is derived as, we set $s_n = s/\omega_o$,:

$$\frac{V_o(s_n)}{V_i(s_n)} = \frac{g_{m1,2}}{C_p} \frac{s_n\omega_0 + \omega_z}{s_n\omega_0^{\,2} + s_n\omega_0 \dfrac{\omega_0}{Q} + \omega_0^{\,2}} \qquad (4.5)$$

And then from above equation, we know :

$$\theta(\omega_n) = \tan^{-1}\left(\frac{\omega_n\omega_0}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_n / Q}{1-\omega_n^{\,2}}\right) \qquad (4.6)$$

We do differentiation on $\theta(\omega_n)$ to get delay :

$$D(\omega_n) = \frac{d\theta(\omega_n)}{d\omega} = \frac{1}{\omega_0}\frac{(1/Q)(1+\omega_n^{\,2})}{(1-\omega_n^{\,2})^2 + (\omega_n/Q)^2} - \frac{\omega_z}{\omega_z^{\,2} + (\omega_n\omega_0)^2} \qquad (4.7)$$

$$= \frac{1}{\omega_0}\frac{(1/Q)(1+\omega_n^{\,2})}{(1-\omega_n^{\,2})^2 + (\omega_n/Q)^2} - \frac{1}{\omega_z + \dfrac{(\omega_n\omega_0)^2}{\omega_z}} \approx \frac{1}{\omega_0}\frac{(1/Q)(1+\omega_n^{\,2})}{(1-\omega_n^{\,2})^2 + (\omega_n/Q)^2}$$

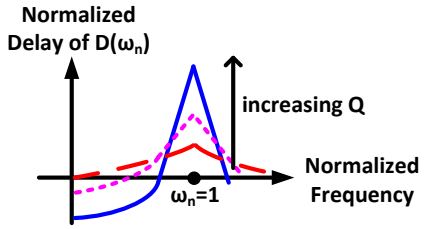


Fig. 4.11. The normalized delay response of equalizer.

As the above equation showing, we get the maximum delay when $\frac{dD(\omega_n)}{d\omega_n} = 0$. At this time,

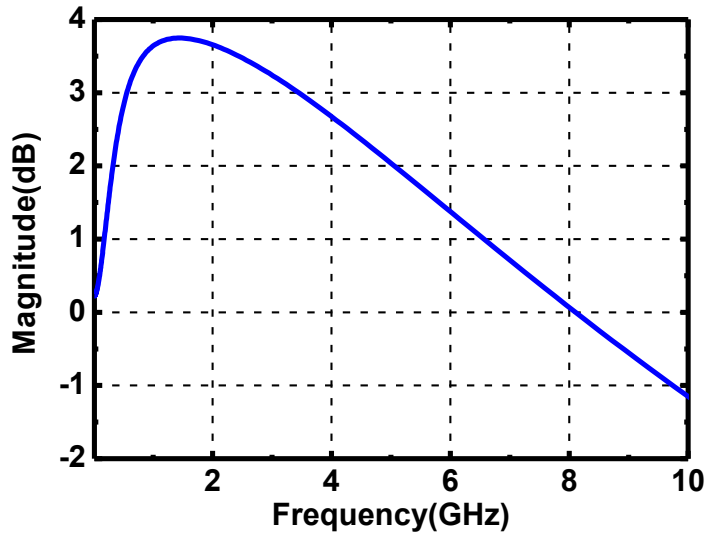
$$\omega_n = \sqrt{-1+\sqrt{4-Q^2}} \approx 1 \text{ , when } Q>1$$

Finally, when $\omega_n \approx 1$,

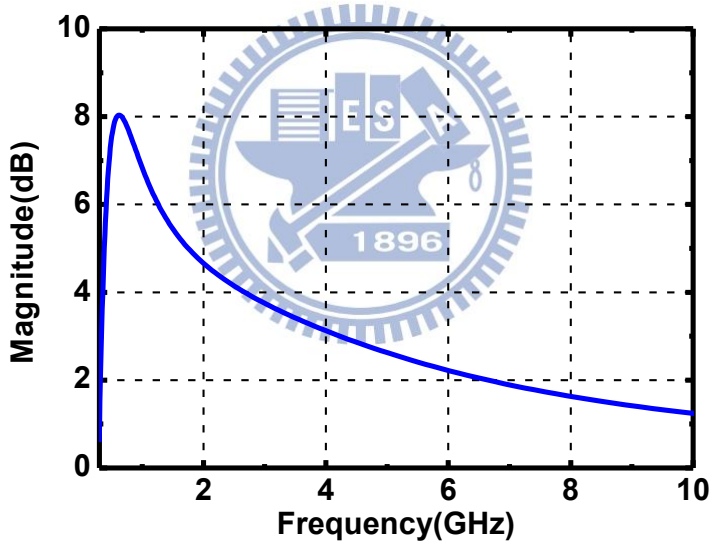
$$D_{max} \approx \frac{2Q}{\omega_0} \propto Q \qquad (4.8)$$

That is to say, if we want more delay, the Q needs to be larger as shown in Fig. 4.11. in our design, the ω_o is designed at low frequency to decrease the group-delay difference. Fig. 4.12 shows the magnitude and group delay response of fourth stage. The peaking is designed at 1.8GHz, and the maximum delay equalization isdesigned at 0.5GHz.

Fig. 4.13 and Fig. 4.14 show the comparison between with and without the fourth stage when the channel has been compensated by the previous three stages. When the channel is equalized with the fourth stage, not only the magnitude response is compensated well, but also group delay is improved with less difference between low-frequency and high-frequency. Thus, the eye-diagram is also recovered well with less jitter.

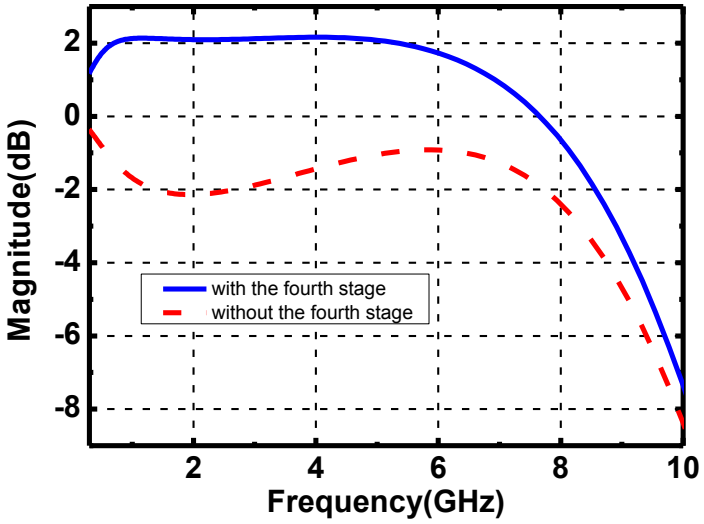


(a)

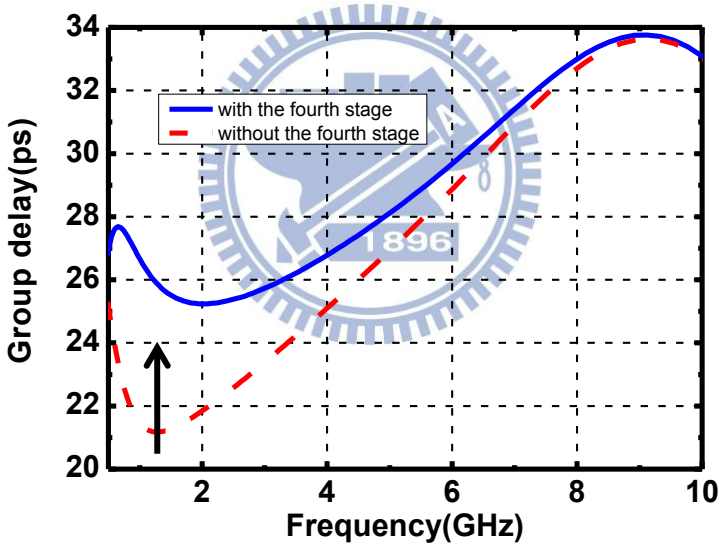


(b)

Fig. 4.12. (a) Magnitude response of the fourth stage. (b) Group delay response the fourth stage.

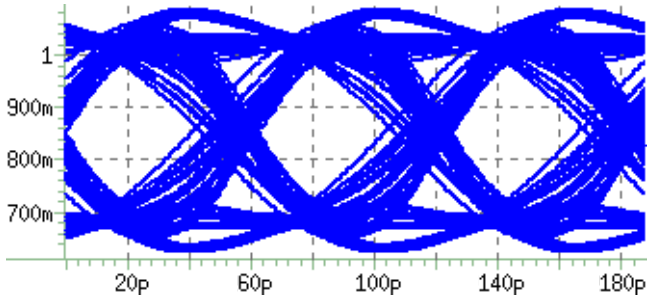


(a)

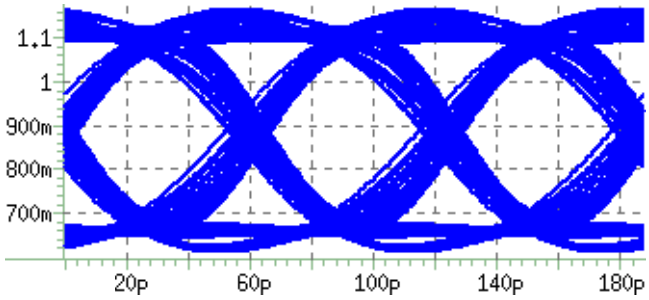


(b)

Fig. 4.13. (a) Magnitude response comparison. (b) Group delay response comparison.



(a)



(b)

Fig. 4.14. Eye-diagrams comparison (a) without the fourth stage (b) with the fourth stage

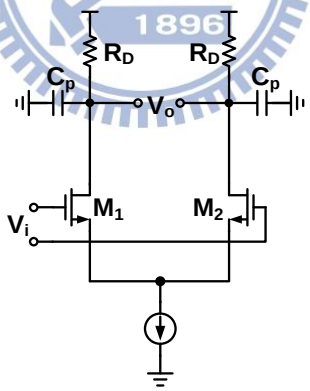


Fig. 4.15. The schematic and magnitude response of the fifth stage.

At last, the schematic of the fifth stage is depicted in Fig. 4.15. It decreases the parasitic effect from next stage (detection schematics).

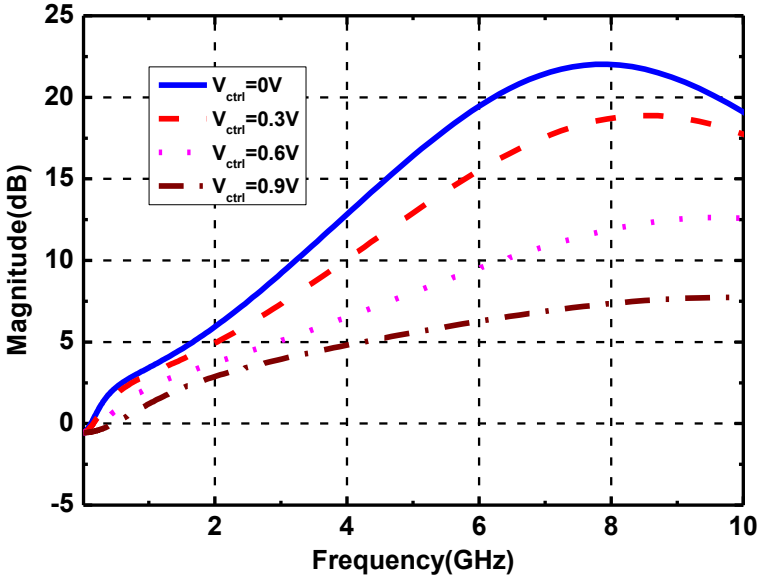


Fig. 4.16. The magnitude response of equalizer under different Vctrl.

Fig. 4.16 shows the simulated magnitude response of equalizer under different V_{ctrl}. It provides about 22.5dB at 8GHz under V_{ctrl}=0V.

4.3.2 Common-mode Detector

The schematic of common-mode detector is depicted in Fig. 4.17. It utilizes the differential signal, V_{EQ+} and V_{EQ-}, to cancel the input feedthrough signal from each other, and then only keeps the DC information of signal by low-pass filter.

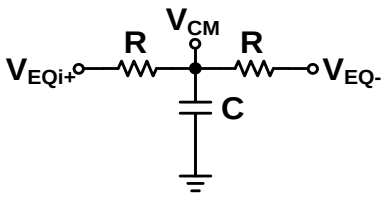


Fig. 4.17. The schematic of common-mode detector.

4.3.3 Swing Detector

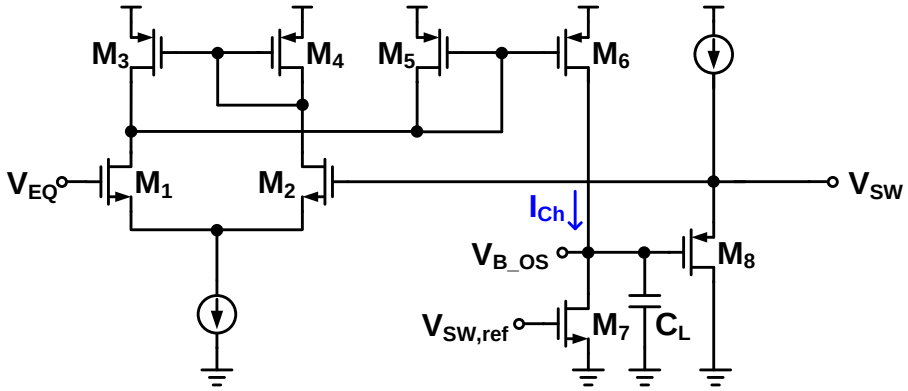


Fig. 4.18. The schematic of swing detector.

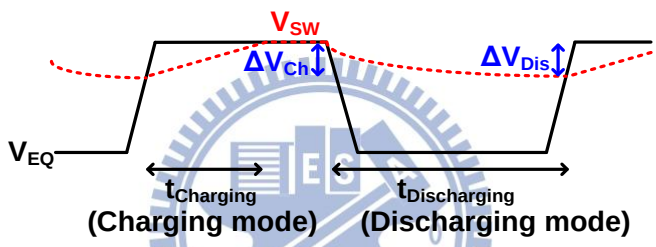


Fig. 4.19. The relation of V_{EQ} and V_{SW}.

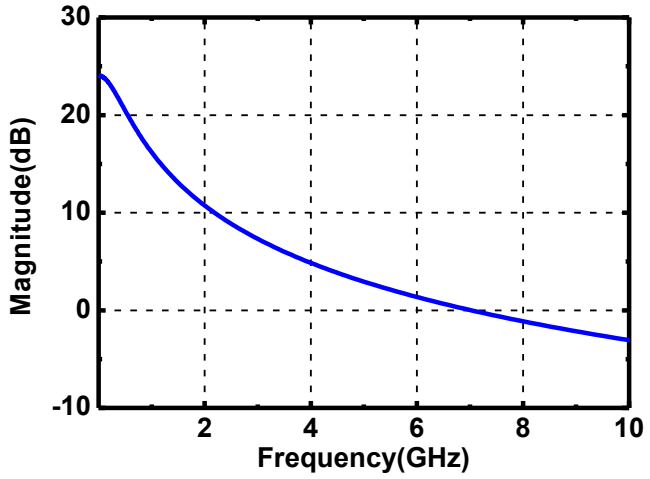
The circuit of swing detector is depicted in Fig. 4.17 [24] , it's improved from previous paper [25-26] which is called peak detect and hold (PDH) circuit. The V_{SW} would follow the V_{B_OS} by the source follower (M_8). As the Fig. 4.18 showing, when the swing detector is in charging mode, the increased voltage of V_{SW} is ΔV_{Ch}. ΔV_{Ch} can be calculated as :

$$\Delta V_{Ch} = \frac{I_{Ch}}{C_L} t_{Charging} \qquad (4.9)$$

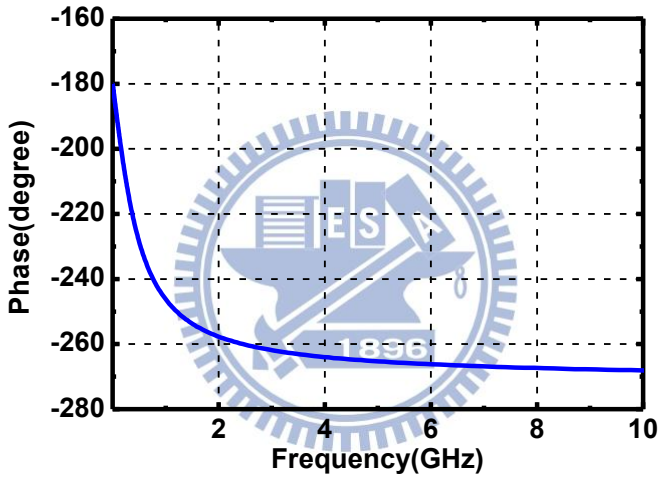
And during holding mode, the ΔV_{Dis} can be calculated as :

$$\Delta V_{Dis} = -V_{B\_OS}(0)(1 - e^{\frac{-t_{Discharging}}{\tau_{V_{B\_OS}}}}) \qquad (4.10)$$

where $\tau_{V_{B\_OS}}$ is the RC time-constant at V_{B_OS}. The worst case occurs when a long



(a)



(b)

Fig. 4.20. (a) Magnitude response of swing detector. (b) Phase response comparison of swing detector.

$t_{Discharging}$ followed by 1-bit $t_{Charging}$. At this time, V_{SW} (V_{B_OS}) would have the maximum error voltage. For a PRBS7 data pattern with 16Gb/s data rate. The long $t_{Discharging}$ is 0.438ns, and the 1-bit $t_{Charging}$ is 0.063ns. To guarantee the error voltage of V_{SW} to be

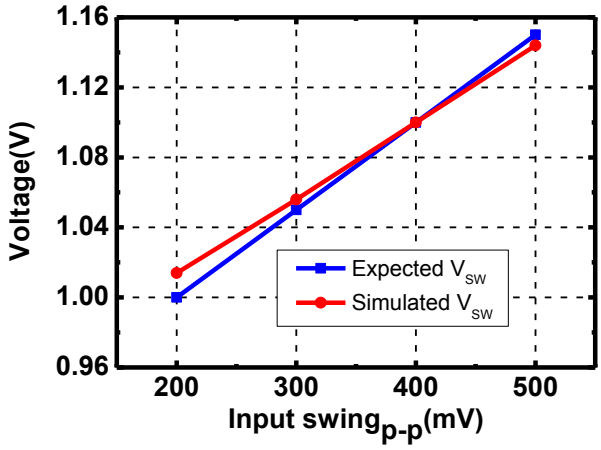


Fig. 4.21. The relations between input swing$_{p-p}$, expected V_{SW} and simulated V_{SW}.

smaller than 10%, we can derive the $\tau_{V_{B\_OS}}$ as, by eq. (4.10), :

$$\frac{\Delta V_{Dis}}{V_{B\_OS(0)}} = (1 - e^{\frac{-t_{Discharging}}{\tau_{B\_OS}}}) \leq 10\%$$
$$\Rightarrow \tau_{V_{B\_OS}} \geq 4.16\text{ns}$$

Thus, r_{o7} can be a quite large value. And moreover, to save the power consumption, the I_{D7} is designed to be a few-micro Amperes which also increases r_{o7}. Fig. 4.19 and Fig. 4.20 shows the open-loop magnitude and phase response of swing detector. The phase margin has 94 degree which is a one-pole system. Fig. 4.21 shows the relations between input swing$_{p-p}$, expected V_{SW} and simulated V_{SW}. The simulated V_{SW} is almost the same as expected V_{SW}.

4.3.4 Slope Detector, Current Mirror and Integrator

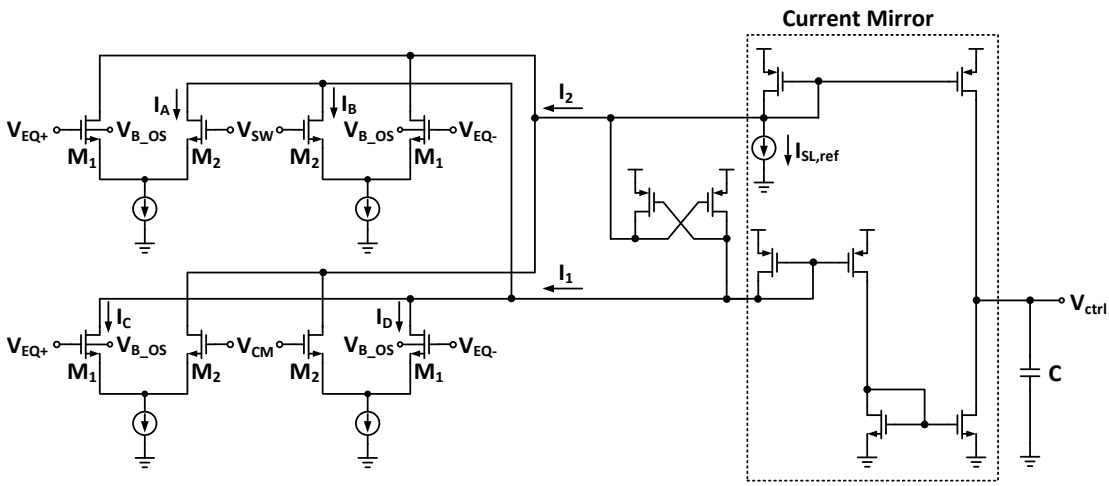


Fig. 4.22. The schematic of slope detector, current mirror, and integrator.

Fig. 4.22 depicts the schematic of slope detector, current mirror and integrator. Firstly, for shifting V_{CM} and V_{SW} to be V_{ref1} and V_{ref2}, as described in Fig. 4.2. The amount of $V_{os\_built\text{-}in}$ need to be in direct proportion with input $swing_{p\text{-}p}$ for making slope detector tolerate different input $swing_{p\text{-}p}$. We utilize body-controlling technique to produce the built-in offset voltage ($V_{os\_built\text{-}in}$) in each four differential pairs. The body-controlling voltage (V_{B_OS}) is extracted from swing detector. The built-in offset voltage ($V_{os\_built\text{-}in}$) is derived as

$$
\begin{aligned}
V_{os\_built\text{-}in} &= V_{th1} - V_{th2} = \gamma\left[\left(\sqrt{V_{SB1}+2\phi_F}\right)-\left(\sqrt{V_{SB2}+2\phi_F}\right)\right] \\
&\approx \gamma\sqrt{\frac{1}{8\phi_F}}\left(V_{SB1}-V_{SB2}\right) = \gamma\sqrt{\frac{1}{8\phi_F}}V_{B\_OS} = \gamma\sqrt{\frac{1}{8\phi_F}}(V_{SW}-V_{SG8}) \\
&= \gamma\sqrt{\frac{1}{8\phi_F}}(\text{input swing}_{p\text{-}p}+V_{CM}-V_{SG8})
\end{aligned}
$$

As long as $V_{CM}=V_{SG8}$

$\Rightarrow V_{os\_built\text{-}in} \propto \text{input swing}_{p\text{-}p} \propto V_{B\_OS}$

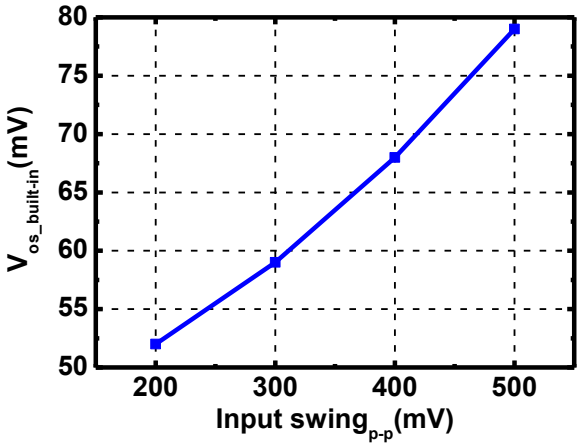


Fig. 4.23. The relations between input swing$_{p-p}$ and simulated $V_{os\_built-in}$.

where V_{th1} and V_{th2} are the threshold voltage of M_1 and M_2. V_{SB1} and V_{SB2} are the source-body voltage of M_1 and M_2. The ϕ_F is the Fermi level. V_{SG8} is the source-gate voltage of M_8 in Fig. 4.17. Fig. 4.23 shows the simulated relationship between input swing$_{p-p}$ versus $V_{os\_built-in}$. To avoid the $M_{1,2}$ being latch-up, we would make the V_{B_OS} be 0V by external biasing voltage initially.

The schematic operation procedure of slope detector is depicted in Fig. 4.24. V_{EQ+} and V_{EQ-} compare to V_{SW} and V_{CM}. And then, I_1 is obtained by summing I_A, I_B, I_C and I_D. I_2 is obtained in the similar way. I_1-I_2 acts as I_{SL} which is shown in Fig.4.1. The current mirror amplifies I_1-I_2 and $I_{SL,ref}$ to charge V_{ctrl}. By the way, we utilize negative resistor technique [27] to decrease the output impedance for I_1 and I_2.

Fig. 4.25 shows the simulated transient response of slope detector. The ΔT is about 60ps when the input signal is an ideal data pattern with 27ps of rising and falling time. Fig. 4.26. depicts the simulated $(I_1\text{-}I_2)_{avg}$ when input signal is attenuated with different channel loss. The optimal-compensation is that $(I_1\text{-}I_2)_{avg}$=202uA.

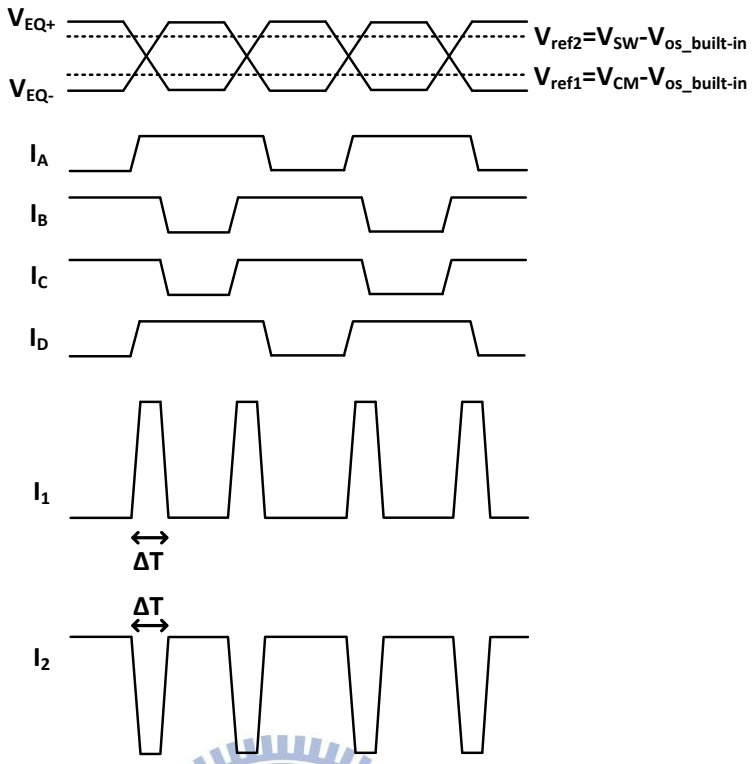


Fig. 4.24. The relationship between V_{EQ+}, V_{EQ-}, I_A, I_B, I_C, I_D, I_1 and I_2.

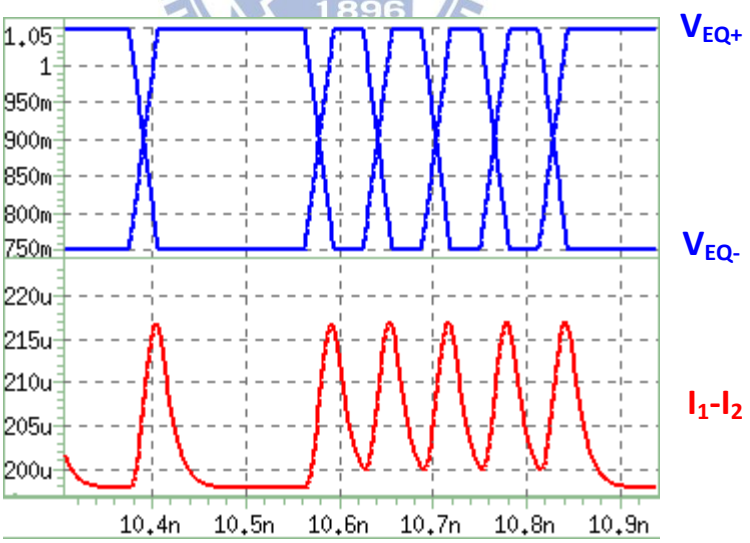


Fig. 4.25. The simulated transient responseof V_{EQ+} , V_{EQ-} and I_1-I_2.

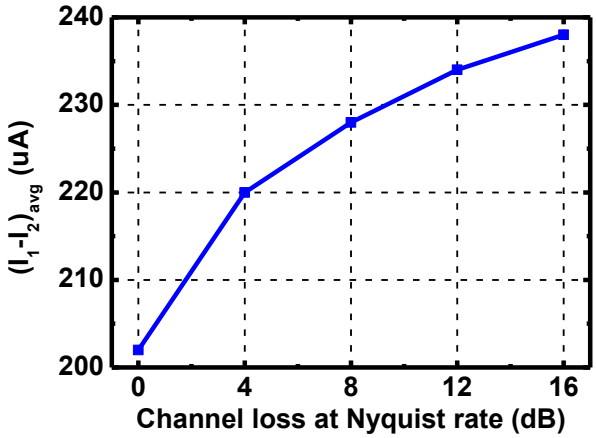


Fig. 4.26. The simulated $(I_1\text{-}I_2)_{avg}$ when input signal is attenuated with different channel loss.

Furthermore, according to the derivation of $\text{sensitivity}_{V_{OSL,Total}}^{I_{SL}}$ in chapter 3, the sensitivity of the offset in slope detector can be derived as

$$\text{Sensitivity}_{V_{OS,SLD}}^{I_{SL}} \approx \frac{V_{OS,SLD}}{\left[(K_{EQ,LF}K_{RG}K_{TI})\cdot\left(\frac{K_{INT}}{s\cdot K_{EQ,HF}}\right)^2\right]}$$

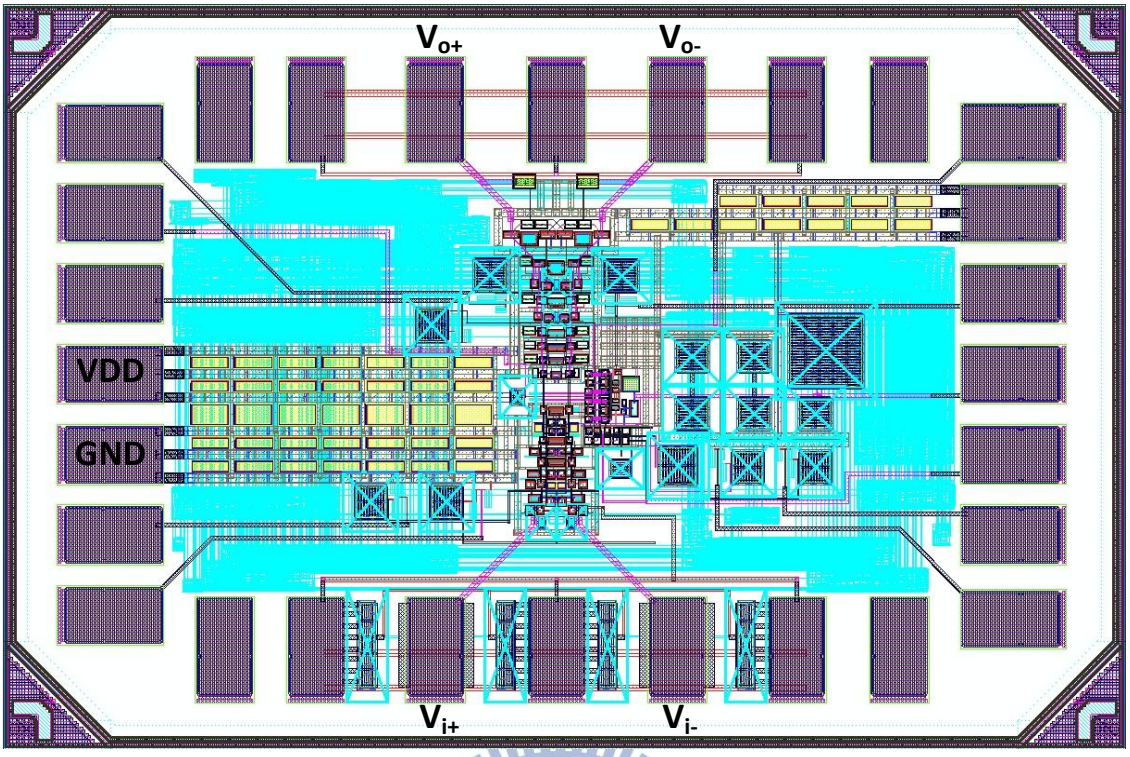
If $K_{EQ,LF}$=1, $K_{EQ,HF}$=10, K_{RG}=1, K_{TI}=10 and K_{INT}/s=100, the sensitivity would be 0.001. Hence, as long as K_{TI} and K_{INT}/s are designed extremely large, the effect of $V_{OS,SLD}$ can be minimized.

4.4 Layout and Simulation Results of Complete Chip

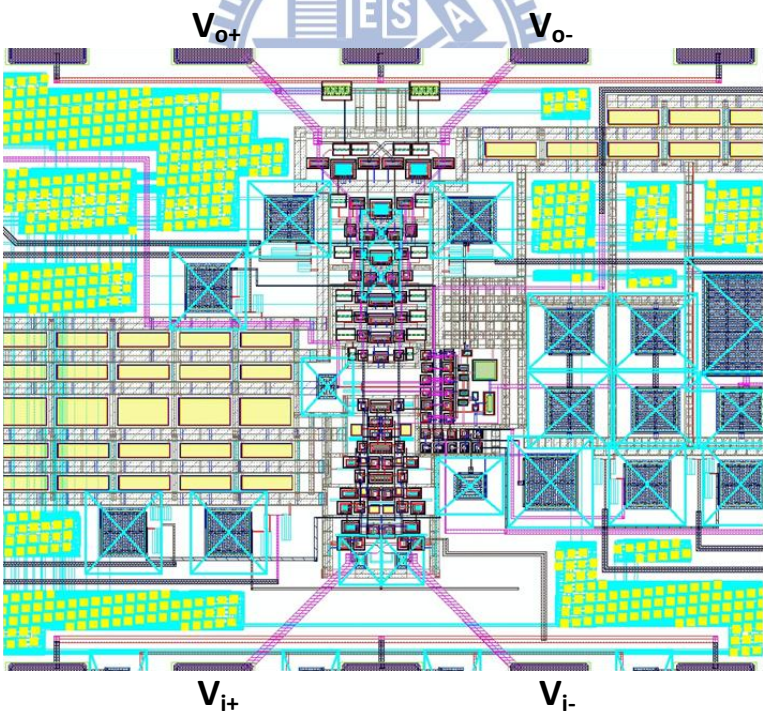
4.4.1 Layout Design

The adaptive equalizer has been fabricated by TSMC 65nm 1P9M CMOS technology. The overall layout view is shown in Fig. 4.27(a). The total area occupies 0.94×0.62 mm^2 (including pads and seal-ring), and the active area only occupies 0.255×0.110 mm^2. The differential input pads are placed at the bottom side and the differential output pads are placed at the top side. To minimum the layout parasitic effect, we make the signal paths as short as possible. The power source pads, VDD and GND, are placed at the left side. For decreasing the voltage drop from pads to active schematics, power lines need to be as wider as possible. Furthermore, in every power paths, we utilize two parallel layers to mitigate the parasitic effect, especially parasitic resistors. And between VDD and GND power lines, we place a lot of decoupling NMOSCAP to reduce the bonding-wire effect.

Fig. 4.28 (b) shows the zoom-in layout view of active schematics. As mentioned above, we put the equalizer and buffer schematics as impact as possible for reducing the signal paths length. And the detection schematic is placed at right side.



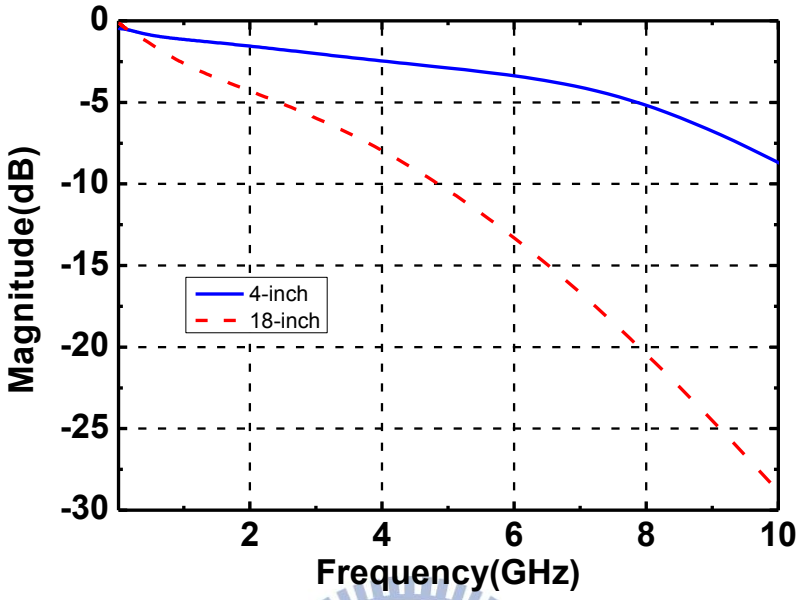
(a)



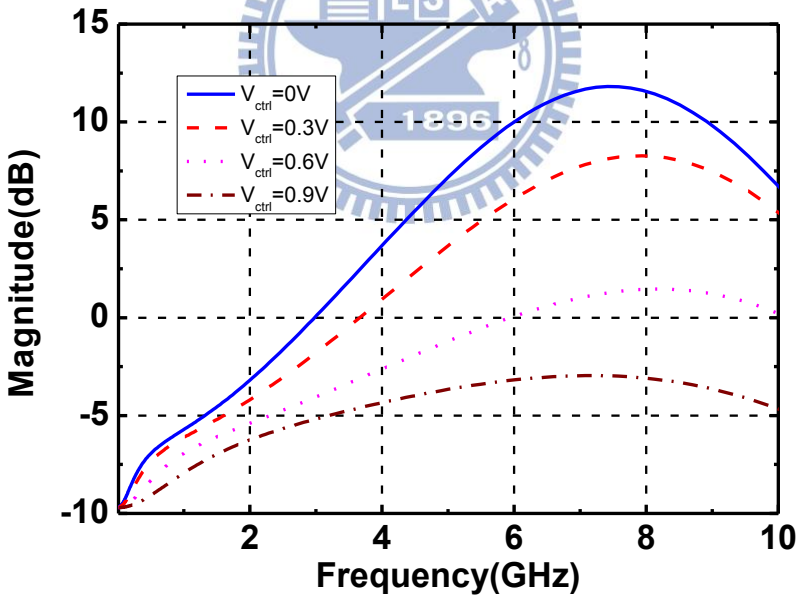
(b)

Fig. 4.27. (a) The overall layout view of chip. (b) The zoom-in view of active schematics.

4.4.2 Simulation results of complete chip



(a)

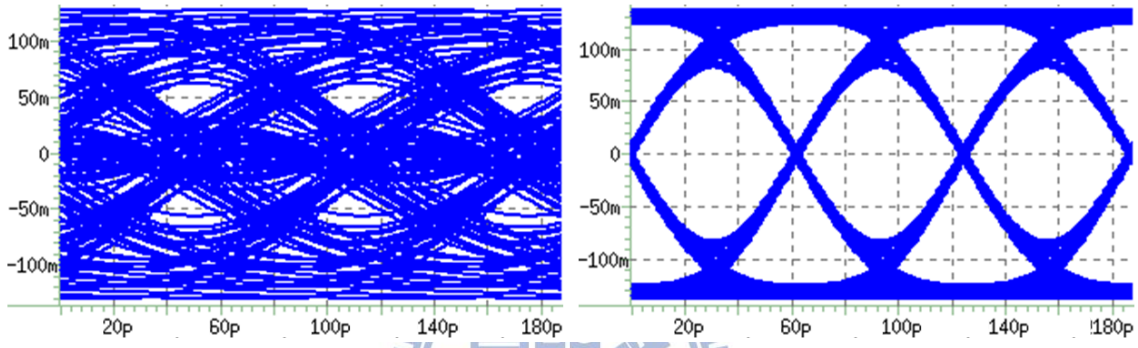


(b)

Fig. 4.28. The magnitude response of (a) channels (b) equalizer under different V_{ctrl}.

In our simulation of complete chip, the input signal pattern is PRBS7 and 16Gb/s data rate. Fig. 4.28 depicted the magnitude response of (a) channels and (b) whole chip

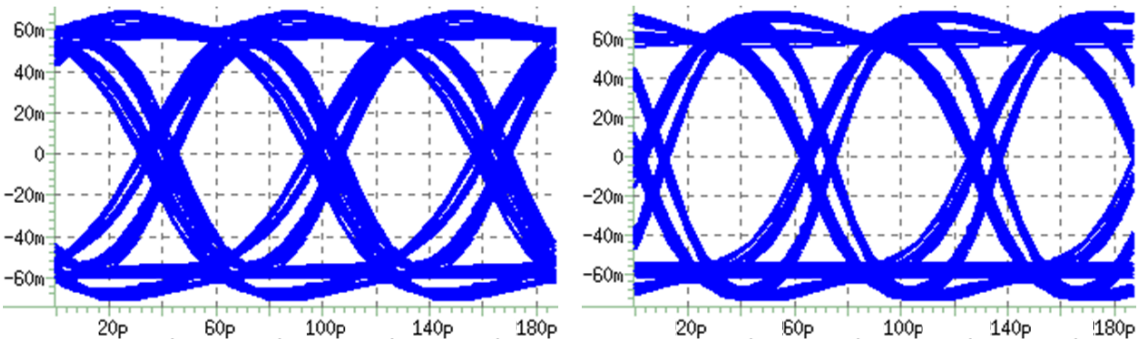
under different V_{ctrl}. The channel loss of 18-inch is 21dB at 8GHz. The maximum peaking is about 21.5dB at 7.5GHz. Fig. 4.29 shows the simulated eye-diagrams which are before equalization with different channel lengths, 18-inch and 4-inch. Fig. 4.30 shows the simulated eye-diagrams which are after equalization with closed-loop mechanism under channel lengths, 18-inch and 4-inch.The results indicate the jitter are less than 0.1UI and eye-opening are open enough.



(a) (b)

Fig. 4.29. Simulated eye-diagrams which is before equalization with

(a) 18-inch (b) 4-inch



(a) (b)

Fig. 4.30. Simulated eye-diagrams which is after equalization with

(a) 18-inch (b) 4-inch

4.5 Experimantal Results

4.5.1 Die Photo

Fig. 4.31 is the die photograph of the overall chip.

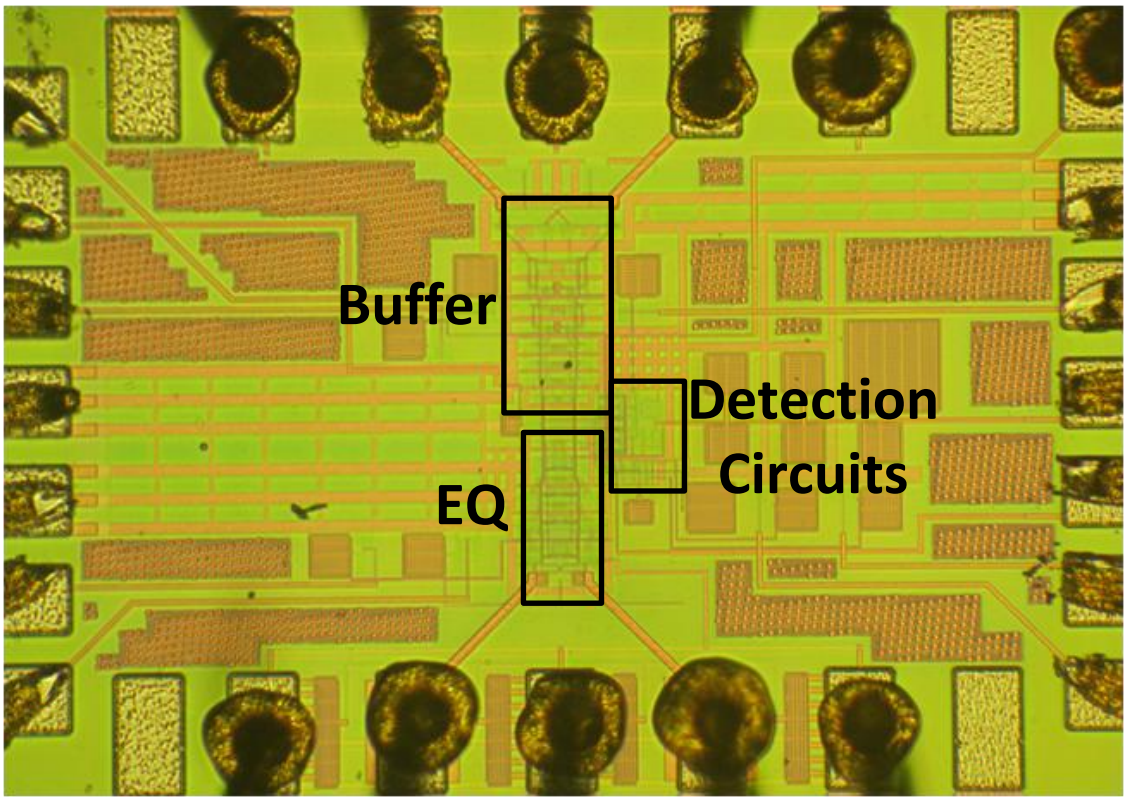


Fig. 4.31. Die photograph of chip.

4.5.2 Chip Measurement

The S_{21} testing setup of channel is depicted in Fig. 4.32. It utilizes the network analyzer, Agilent E8364B PNA, to measure S_{21}. We use the testing results to help us knowing the profile of channels, and then, design the gain-boost of equalizer.

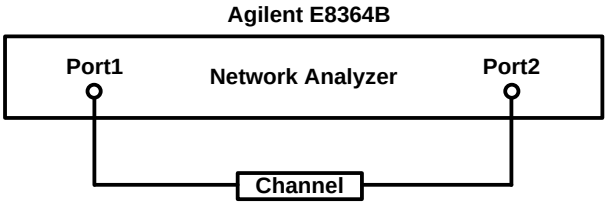


Fig. 4.32. S_{21} testing setup of channel

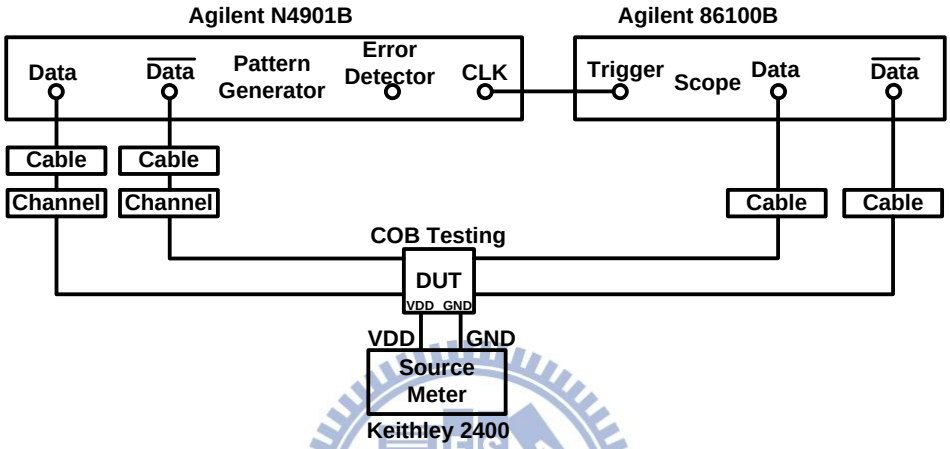


Fig. 4.33. Time-domain testing setup of chip, including channels and cables.

When we measure the eye-diagram of chip with time-domain instruments, the testing environmental loss can't be neglected anymore, especially as the data rate increasing up to tens Gb/s. The time-domain testing setup of chip is depicted in Fig. 4.33. The data pattern is generated by pattern generator, Agilent N4901B serial BERT. In this work, the chip is demonstrated with 13.5Gb/s data rate and PRBS7 data pattern. According to Fig. 4.33, these external losses are resulted from signal traces on PCB and Cables. Fig. 4.34 shows the signal traces on PCB, which the length are totally about 2-inch of length from input-end to output-end. Hence, we would measure such loss to know how much external loss from signal traces, and the test kit is shown in Fig. 4.35. Furthermore, we set the 2-inch as our shortest channel length in COB testing assembly. Fig. 4.36 and Fig. 4.37 show the measured S_{21} of channels and cable (60cm). The maximum channel loss

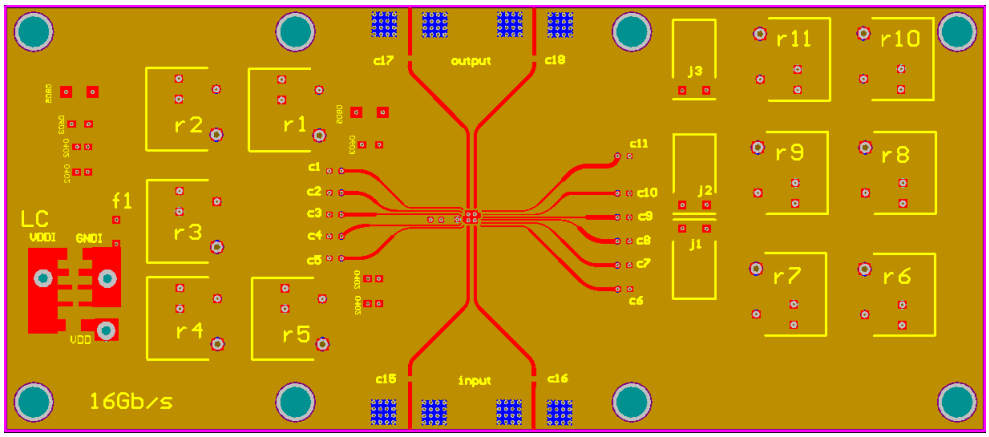


Fig. 4.34. PCB layout view.

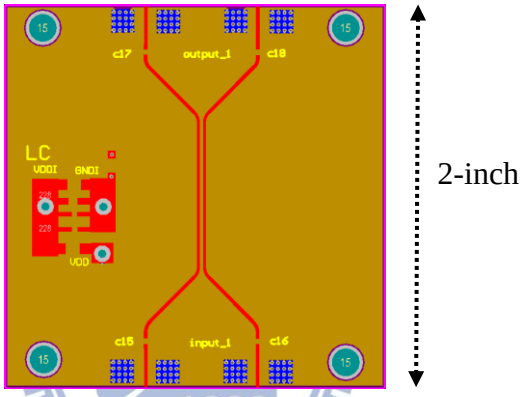


Fig. 4.35. Test kit of PCB trace, about 2-inch of length.

of the longest channel, 20-inch, is 19.3dB at 6.75GHz. The 2-inch has about 3dB loss at 6.75GHz. The cable results in 0.6dB of external loss at 6.75GHz. Thus, the overall loss that the equalizer need to compensate is 20.5dB at 6.75GHz.

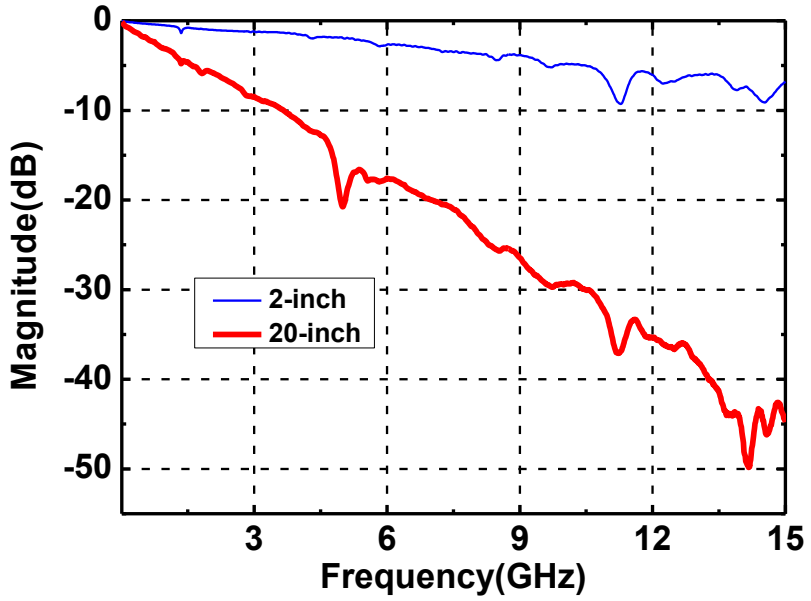


Fig. 4.36. Measured S_{21} of channels.

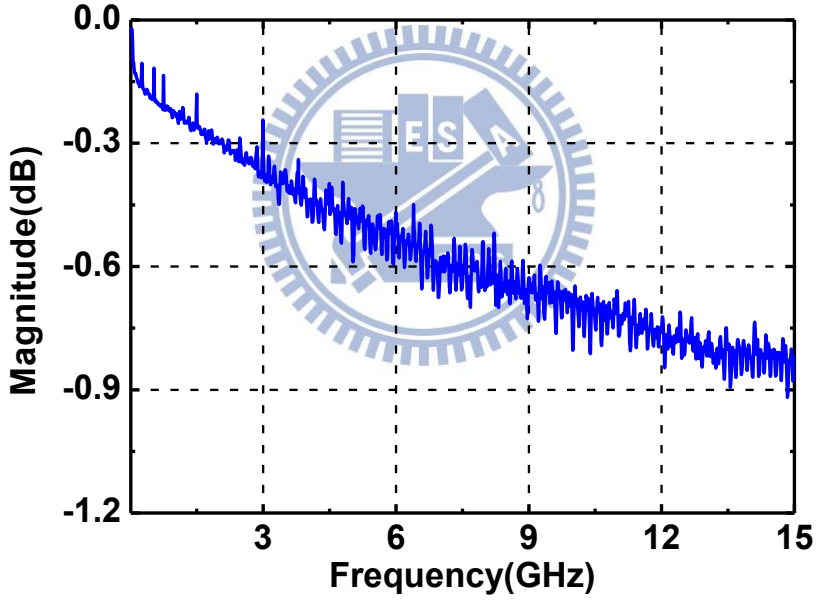


Fig. 4.37. Measured S_{21} of cable.

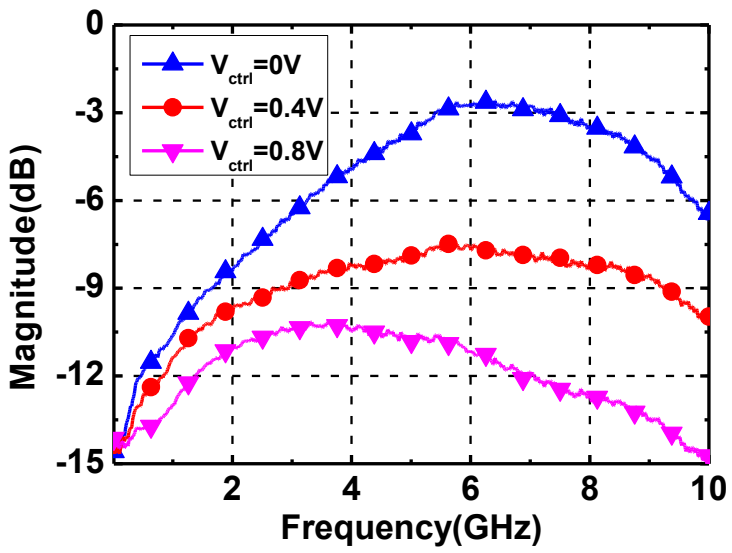
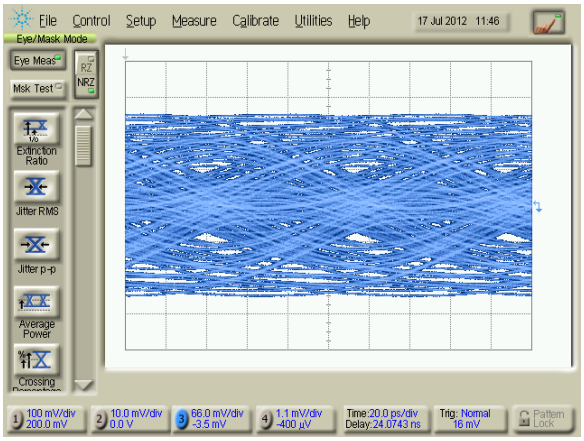
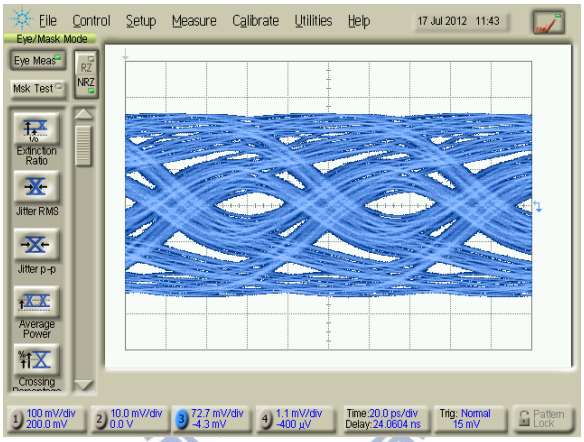


Fig. 4.38. Measured S_{21} of overall chip.

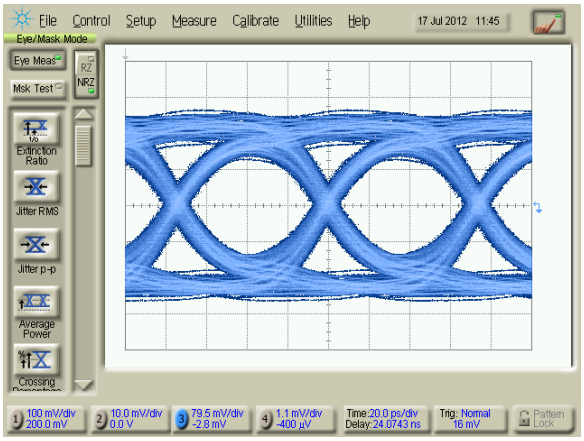
Fig. 4.38 depicts the measured S21 of overall chip. The maximum peaking is about 12dB. Fig. 4.39 shows the measured eye-diagrams which are before equalization with different channel lengths, 20-inch and 2-inch. We see the eye-diagram of 20-inch before equalization is closed. Fig. 4.40, Fig. 4.41, Fig. 4.42 and Fig. 4.43 show the measured eye-diagrams which are after equalization under different input swings and different channel lengths, 20-inch, 8-inch and 2-inch.



(a)

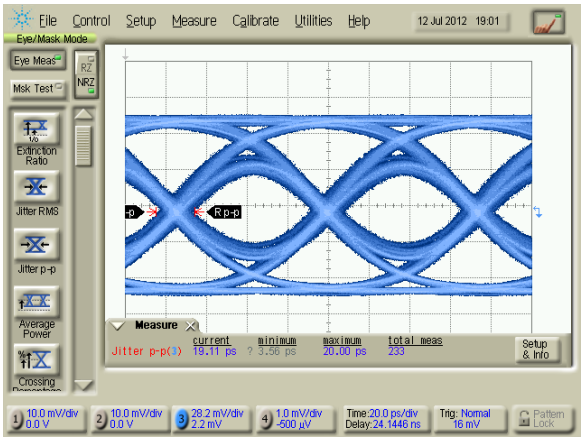


(b)

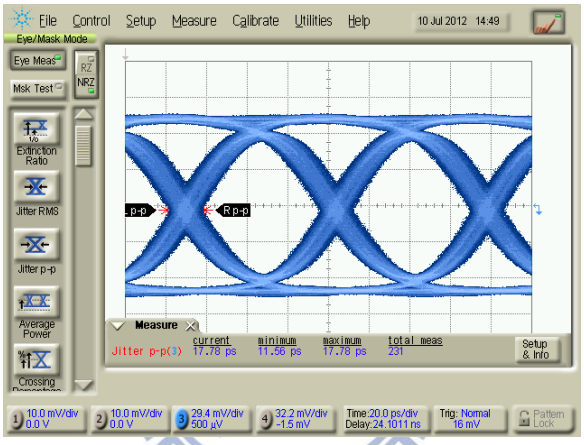


(c)

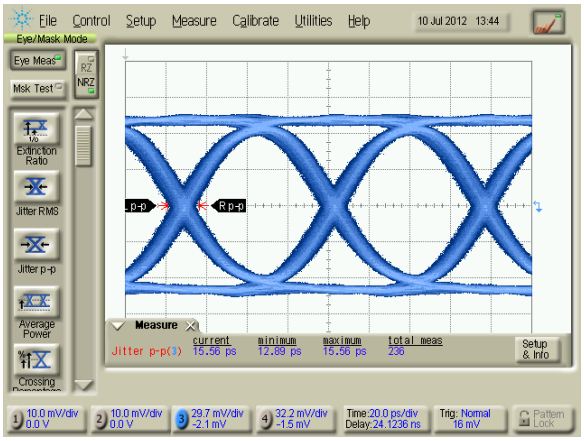
Fig. 4.39. Measured eye-diagrams which is before equalization with 400mV input swing and (a) 20-inch (b) 14-inch (c) 2-inch



(a)

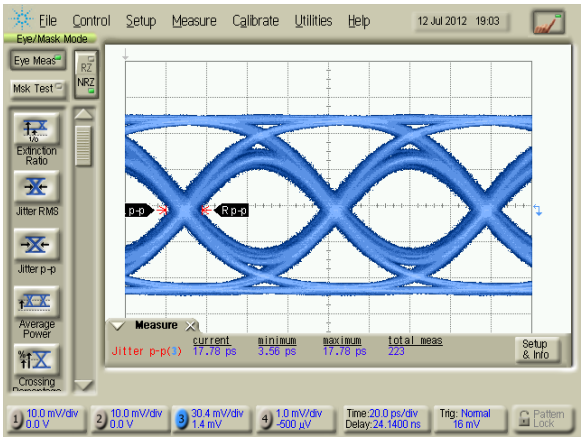


(b)

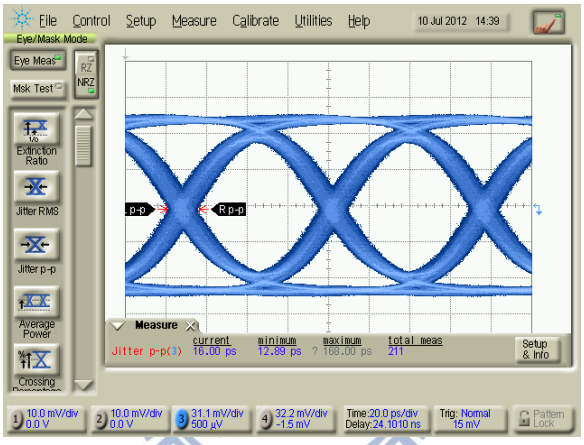


(c)

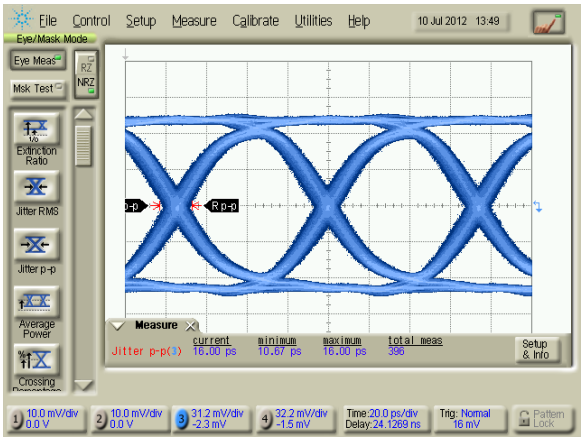
Fig. 4.40. Measured eye-diagrams which is after equalization with 300mV input swing and (a) 20-inch (b) 14-inch (c) 2-inch



(a)

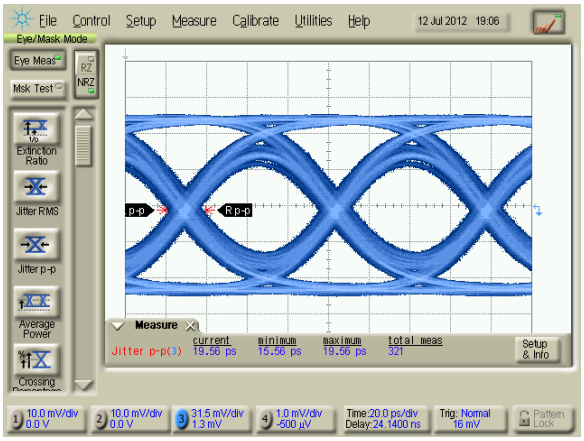


(b)

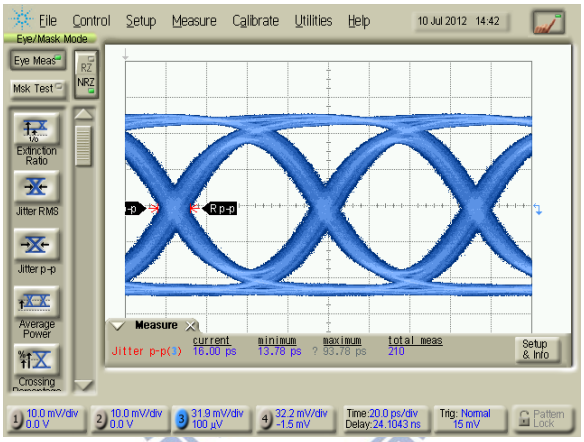


(c)

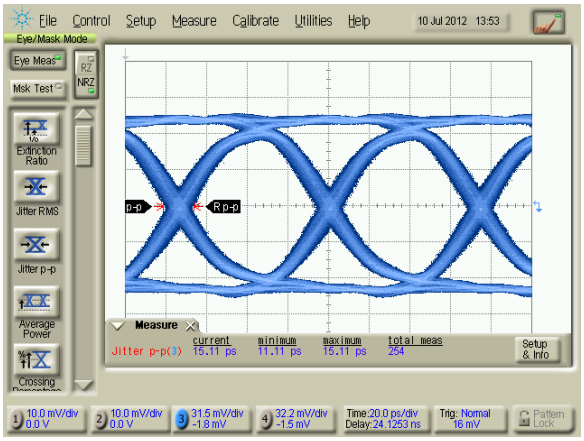
Fig. 4.41. Measured eye-diagrams which is after equalization with 400mV input swing and (a) 20-inch (b) 14-inch (c) 2-inch



(a)

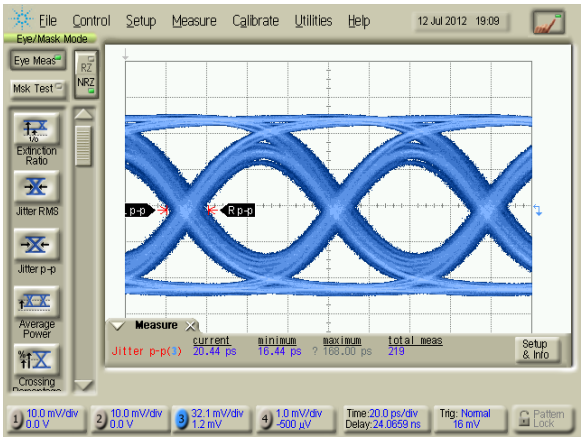


(b)

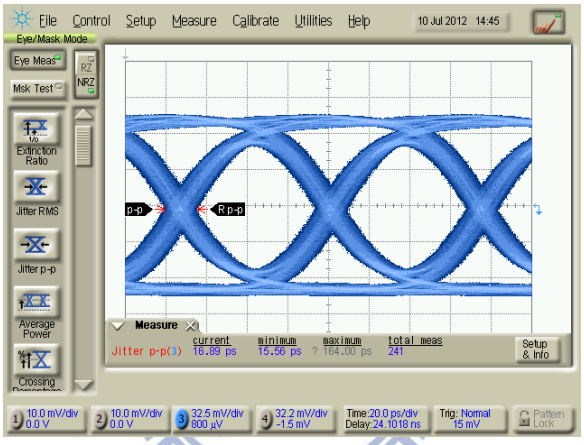


(c)

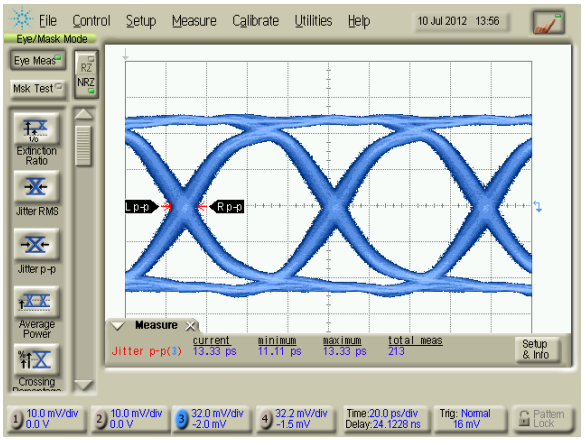
Fig. 4.42. Measured eye-diagrams which is after equalization with 500mV input swing and (a) 20-inch (b) 14-inch (c) 2-inch



(a)



(b)



(c)

Fig. 4.43. Measured eye-diagrams which is after equalization with 600mV input swing and (a) 20-inch (b) 14-inch (c) 2-inch

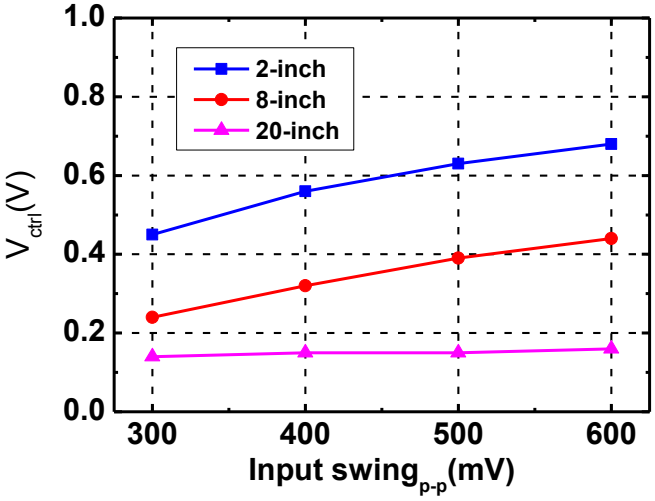


Fig. 4.44. The jitter comparison.

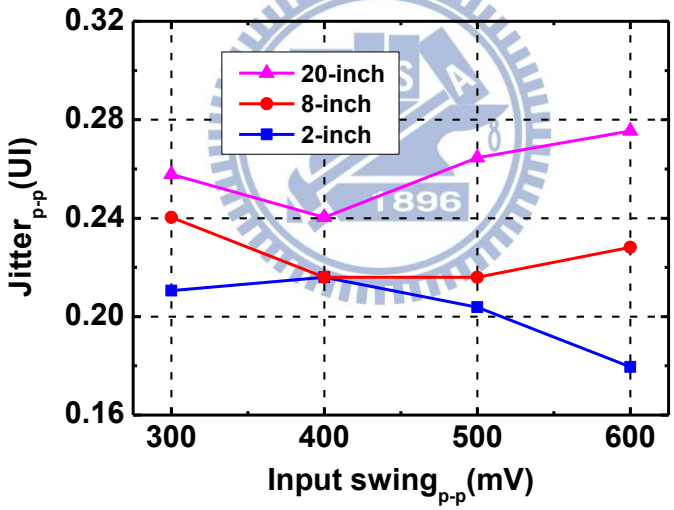
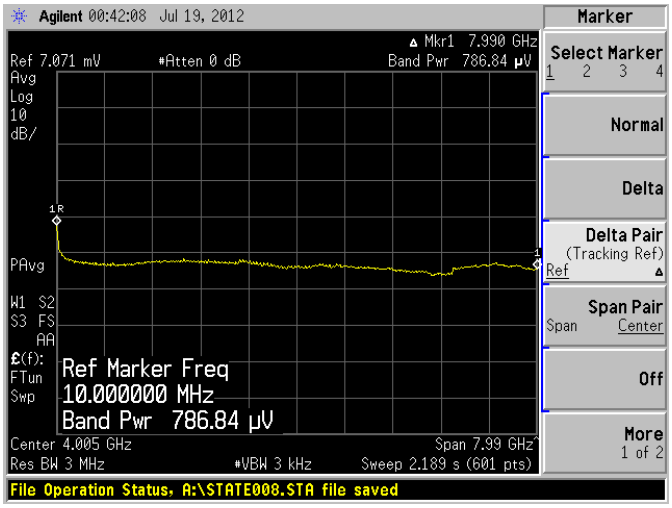
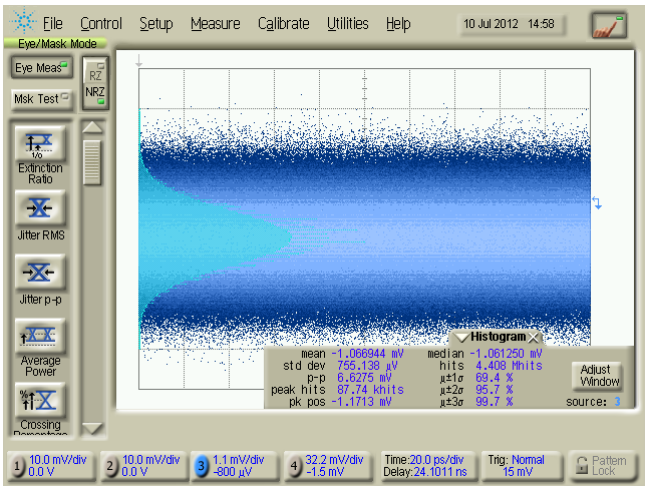


Fig. 4.45. The V_{ctrl} comparison.

The measured jitter performance is shown in Fig. 4.44. The maximum jitter is less than 0.31UI. Fig. 4.45 depicted V_{ctrl} comparison. Fig. 4.46 shows the measured noise of



(a)



(b)

Fig. 4.46. The measured results of chip. (a) utilizing Spectrum analyzer (Agilent E4440A) (b) utilizing oscilloscope (Agilent 86100A)

chip by two testing instruments. The noise are 0.78mV$_{rms}$ and 0.76mV$_{rms}$, and the simulated noise is about 0.8mVrms. According to eq. (2.2), as long as the output swing$_{p\text{-}p}$ is larger than 12.6mV, the BER could be smaller than 10^{-12}. Fig. 4.47 depicted BER results, and the input swing can be decreased to 80mV$_{p\text{-}p}$ which the BER still smaller than 10^{-12}. Table 4.1 shows the overall performance comparison of this work.

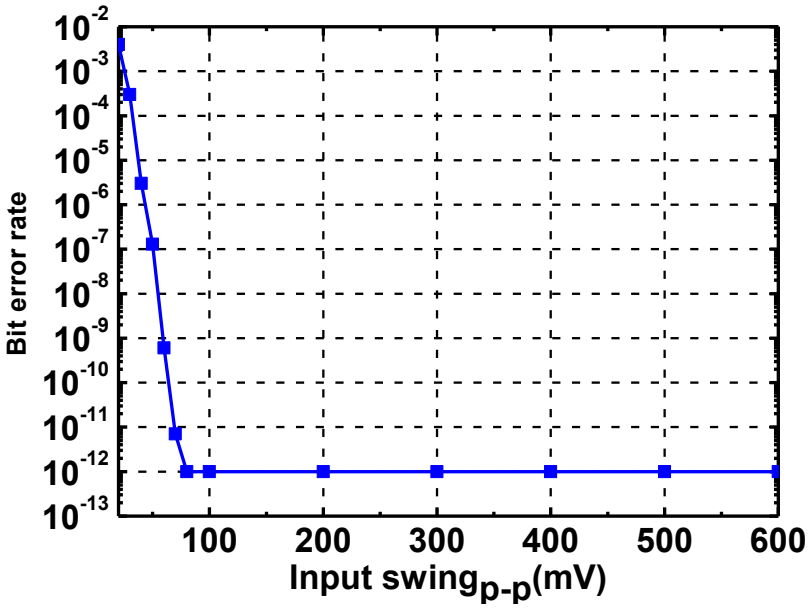


Fig. 4.47. The BER results with different input $swing_{p\text{-}p}$.

Table 4.1 Performance Comparison with Previous Papers.

	JSSC'10 [10]	ISSCC'10 [11]	ISSCC'11 [13]	This work	
				Simulation	Measurement
Technology	65nm CMOS	90m CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Supply Voltage (V)	1.2	1	1.2	1.2	1.2
Data rate (Gb/s)	20	20	20	16	13.5
Channel Loss (dB)	11.7	24	22	21	20.5
Using Inductor	Yes	Yes	Yes	No	No
Using DFE	Yes	Yes	Yes	No	No
$Jitter_{p\text{-}p}$ (ps)	0.2	N.A.	0.28	0.1	0.28
Adaptive Mechanism	No	No	Yes	Yes	Yes
Input Swing (mV)	320	250	175	300~600	80~600
Power (mW)	42*	40*	52	13.2	14
Area** (mm^2)	0.035	0.09	0.1	0.028	0.028
FoM	0.18*	0.08*	0.12	0.04	0.05

* without adaptive schematics' power

**only active schematics

$$\text{FoM} = \frac{\text{Power}}{\text{DataRate} \times \text{Loss}}$$

Chapter 5

Conclusion and Future Work

This thesis proposes a positive-feedback based equalizer using slope detector. With the help of slope detector, we avoid the requirement of using offset-sensitive rectifiers. And the adaptive equalizer tolerates large input dynamic range, or called large input swing. Since the equalizer dominates the power consumption, we utilize the positive-feedback based equalizer to save power consumption. Furthermore, in the recently published papers, the compensating channel loss is about 20dB at Nyquist rate. The channel loss may can be compensated up to 30dB.

Appendix A

A 6Gb/s Adapative Equalizer with Large Input Dynamic Range Using Offset-Insensitive Slope Detector

This appendix presents a 6Gb/s adaptive eequalizer using the slope deteector. The adaptive equalizer is capable of compensating the channel loss of 22dB at Nyquist rate by 0.18μm CMOS technology.

Fig. B.1 depicts the architecture of the proposed 6Gb/s adaptive equalizer with slope detector. The detection schematics include swing detector, common-mode detector (CM detector), reference generator, and slope detector. Fig. B.2 shows the relations between V_i, V_{SWD}, V_{CM}, V_{ref1} and V_{ref2}. The swing detector and CM detector can detect the swing voltage level (V_{SW}) and common-mode voltage level (V_{CM}) of signal, V_i. And the V_{ref1} and V_{ref2} can be generated by reference generator according to the voltage level of V_{SWD} and V_{CM}.

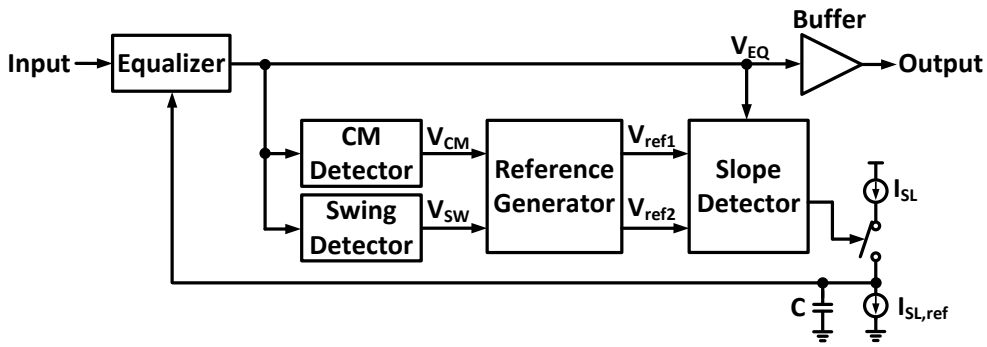


Fig. B.1. The architecture of adaptive equalizer with slope detector.

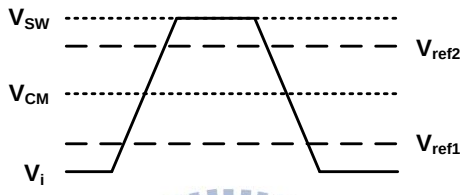


Fig. B.2. The relations between V_i, V_{SWD}, V_{CM}, V_{ref1} and V_{ref2}.

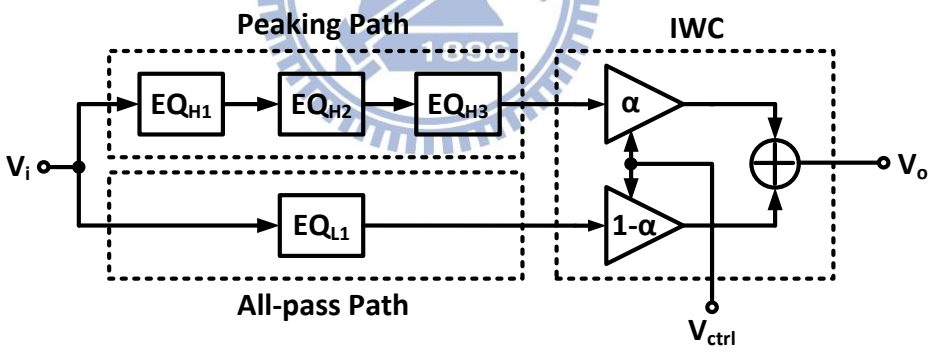


Fig. B.3. Block diagram of Equalizer.

The proposed block diagrams of equalizer is depicted in Fig. B.3. The equalizer's gain-boost is tuned by interpolation weighting controller (IWC) between peaking path and all-pass path. Furthermore, we say the peaking tuning is control by the coefficient of α. the range of α is between 0 and 1. The peaking path provides the fixed peaking response which is combined with three peaking stages, EQ_{H1}, EQ_{H2} and EQ_{H3}.

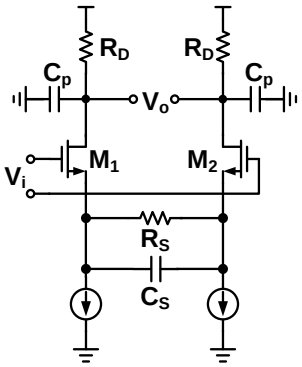


Fig. B.4. The schematic of EQ_{H2} with RC degeneration technique.

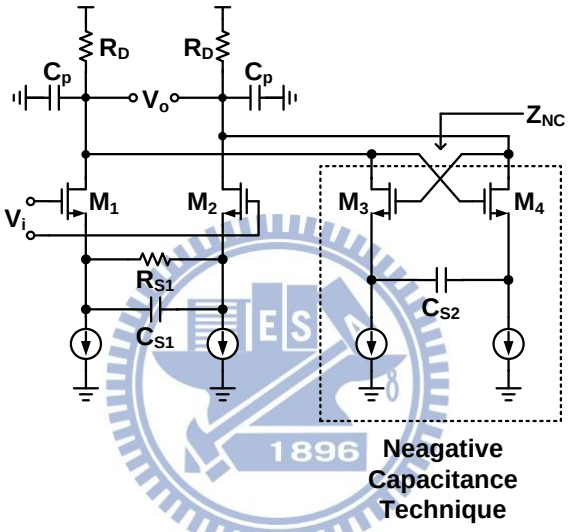


Fig. B.5. The schematic of EQ_{H1} and EQ_{H3} with RC degeneration and negative capacitive techniques.

And the all-pass path provides the wide and flatness response. For group-delay consideration, the all-pass path utilizes one wide-bandwidth stage, EQ_{L1}, to overcome the disparate group-delay through two parallel paths of equalizer. Fig. B.4 and Fig. B.5 depict the schematics of peaking path. The EQ_{H2} use RC degeneration technique, and EQ_{H1} and EQ_{H3} use the RC degeneration and negative capacitance techniques. Fig. B.6 depicts the schematic of all-pass path. It only utilizes source degeneration technique. The interpolation weighting controller (IWC) is designed for

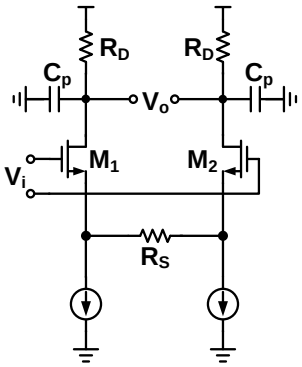


Fig. B.6. The schematic of EQ_{L1} with source degeneration technique.

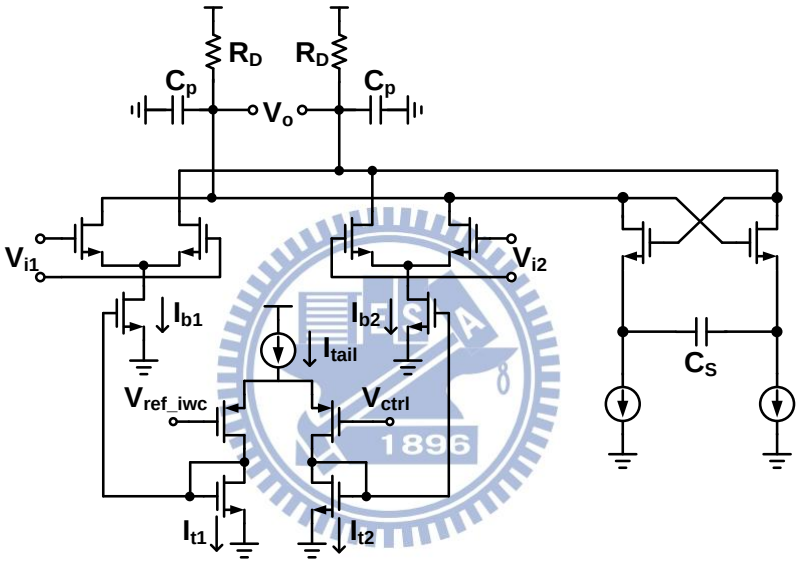


Fig. B.7. The schematic of interpolation weighting controller (IWC).

controlling the parameter of α which can tune the gain-boost of equalizer, as shown in Fig. B.7. Fig. B.8 shows the magnitude response of equalizer under V_{ctrl} varying from 0.4V to 1.2V. The maximum gain-boost is about 18dB at 3GHz when V_{ctrl}=1.2V.

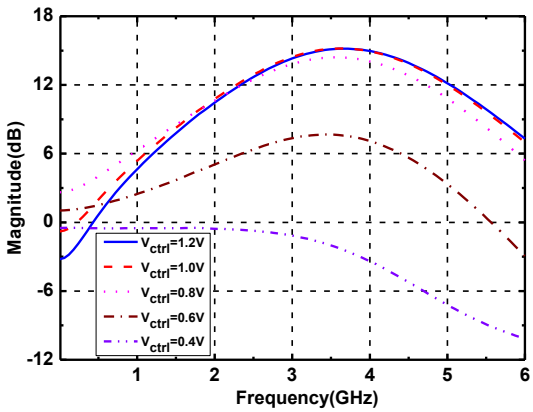


Fig. B.8. Simulated frequency response of equalizer with different voltage of V_{ctrl}.

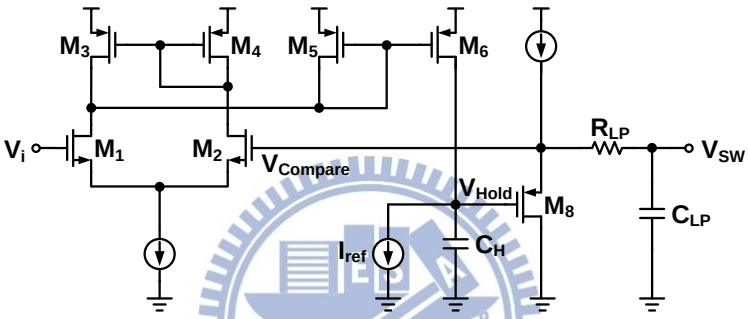


Fig. B.9. The schematic of swing detector.

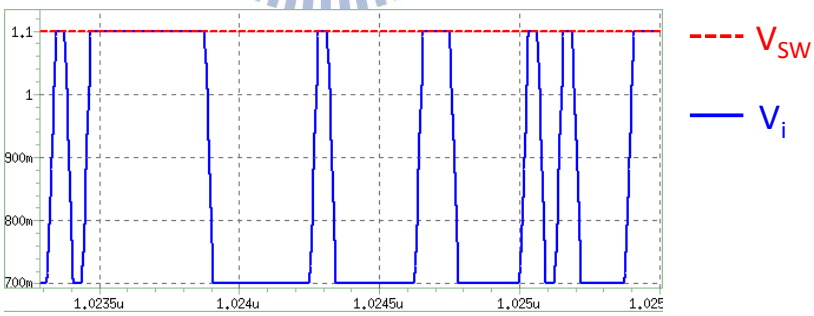


Fig. B.10. The transient response of swing detector.

The proposed schematic of swing detector is depicted in Fig. B.9, it's improved from previous paper [25-26] which is called peak detect and hold (PDH) schematic. And Fig. B.10 shows the transient response of swing detector. V_{SW} is almost the same to the swing voltage of signal, almost obtains the correct value of swing.

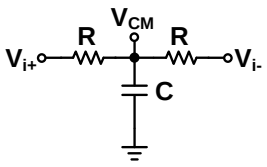


Fig. B.11. The schematic of common-mode detector.

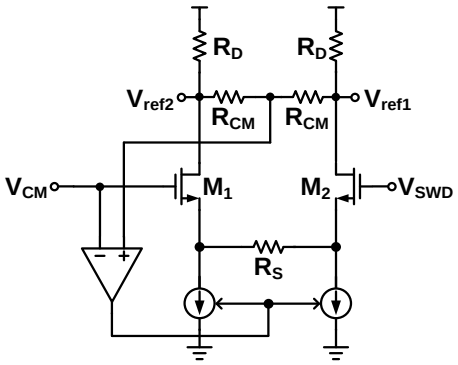


Fig. B.12. The schematic of reference generator.

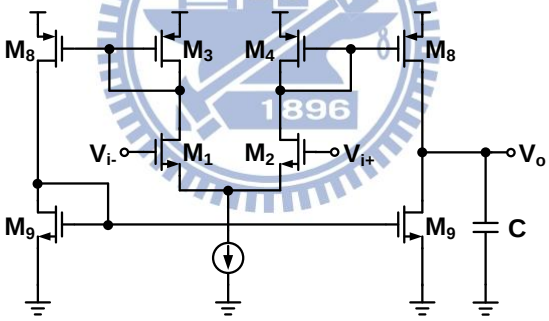


Fig. B.13. The schematic of operation-amplifier in CMFB path.

The schematic of common-mode detector is depicted in Fig. B.11. It utilizes the differential signal, V_{i+} and V_{i-}, to cancel input feed-through from each other. And then, only keeps the DC information of signal.

As the mentioned in Fig. B.2, we utilize V_{SW} and V_{CM} to generate V_{ref1} and V_{ref2}. Fig. B.12 depicts the proposed reference generator to accomplish this requirement.

The transfer function is derived as :

$$\left|\frac{V_{ref2}-V_{ref1}}{V_{SW}-V_{CM}}\right| = A = \frac{g_{m1}R_D}{2+g_{m1}R_S} \approx \frac{R_D}{R_S}$$

where g_{m1} means the transconductance of M_1 and M_2. In our work, we choose A=1.5, the reason will be explain in later. In addition, we apply common-mode feedback (CMFB) to control the output common-mode voltage for avoiding the common-mode variation when the V_{SW} is changed with the signal swing. The schematic of operation amplifier (OP) in the CMFB path is depicted in Fig. B.13. And we should assure the stability of CMFB.

Fig. B.14. shows the proposed slope detector, current mirror and integrator. Fig. B.15 depicts the transient response of the average current of I_1-I_2 (I_{avg},) in slope detector when the input signal is ideal PRBS7.

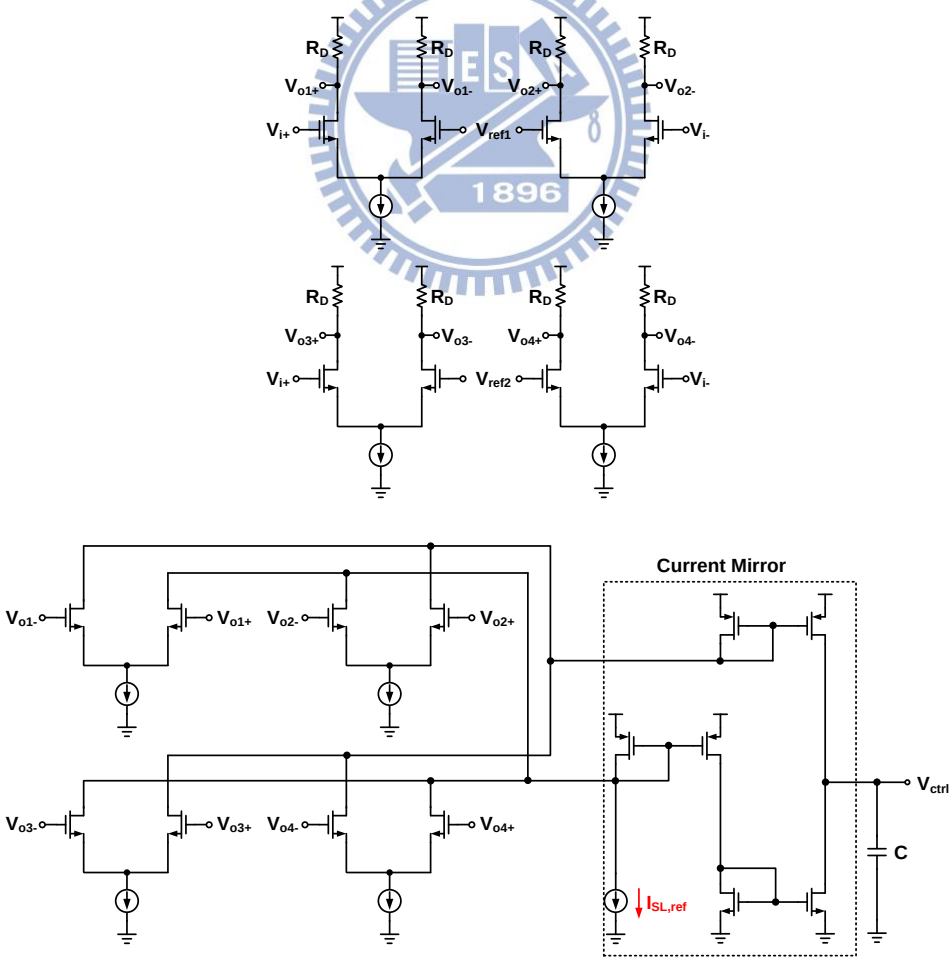


Fig. B.14. The schematic of slope detector, current mirror and integrator.

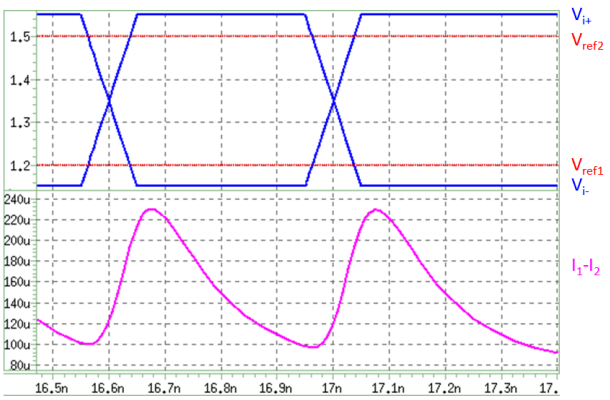


Fig. B.15. The transient response of slope detector.

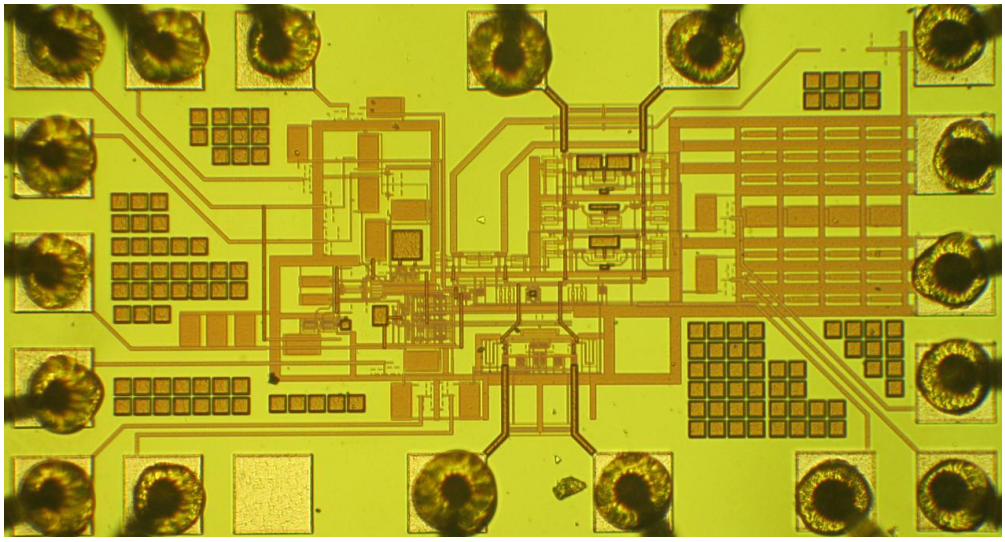


Fig. B.16. Die photograph.

Fig. B.16 is the die photograph of the chip.

Fig B.17 shows the measured S_{21} of channels. The maximum channel loss of the longest channel, 61-inch, is 23.3dB at 3GHz. Fig. B.18 shows the measured eye-diagrams which are before equalization with different channel lengths, , 61-inch , 28-inch 12-inch and 0-inch. We see the eye-diagram of 61-inch before equalization is closed. Fig. B.19, Fig B.20, Fig. B.21 and Fig. B.22 show the measured eye-diagrams which are after equalization under different input swing and different channel length.

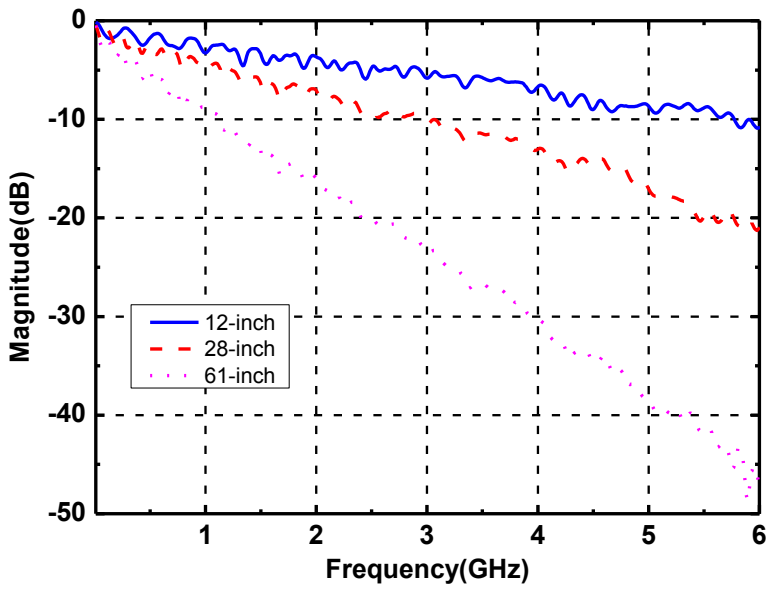


Fig. B.17. Measured S_{21} of channels.

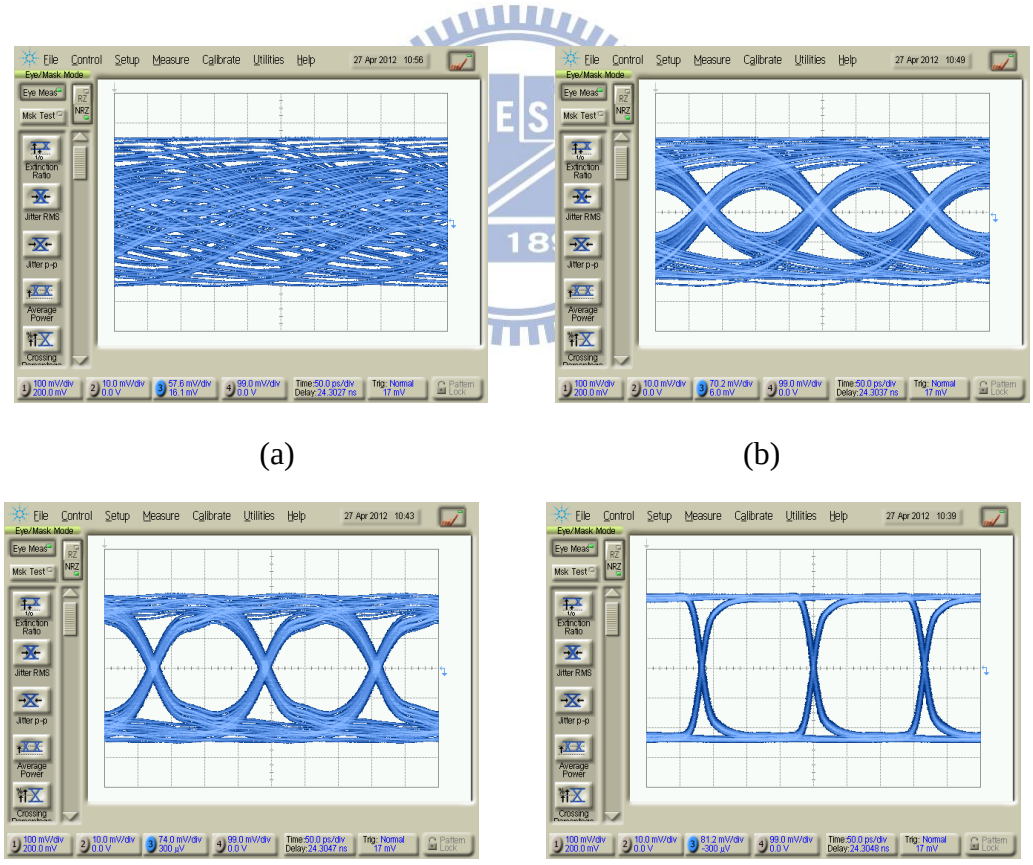
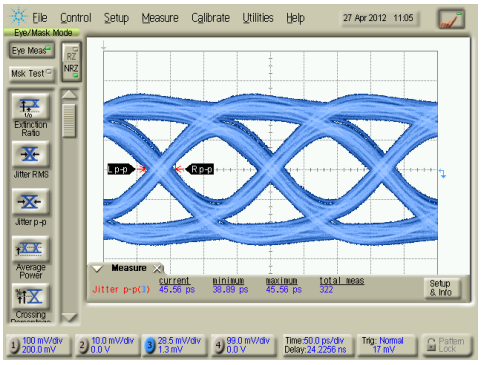
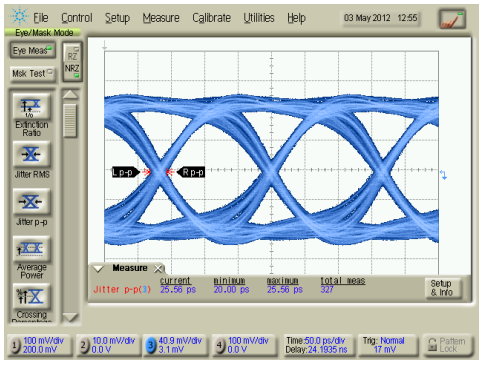


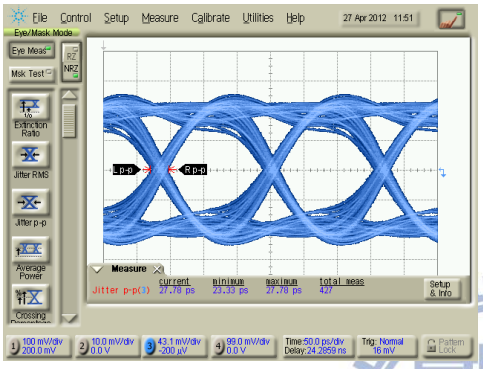
Fig. B.18. Measured eye-diagrams which is before equalization under 400mV input swing with (a) 61-inch (b) 28-inch (c) 12-inch (d) 0-inch



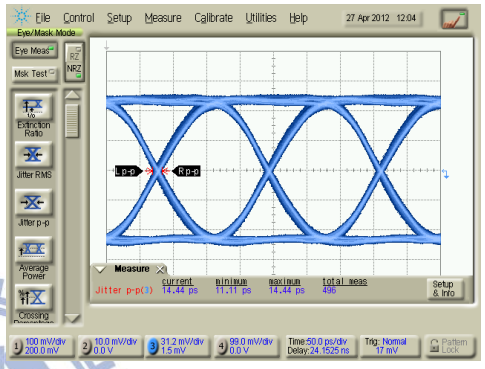
(a)



(b)

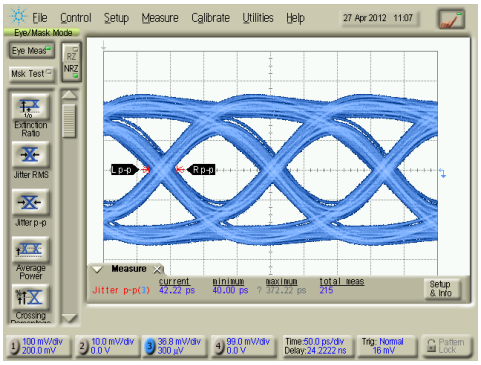


(c)

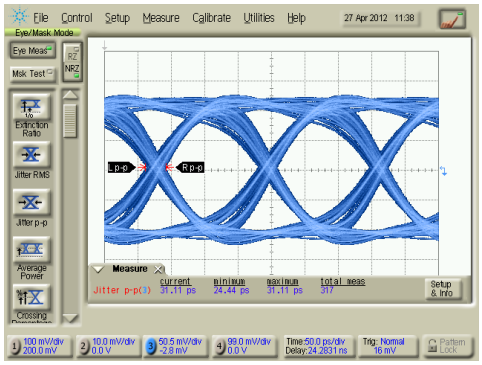


(d)

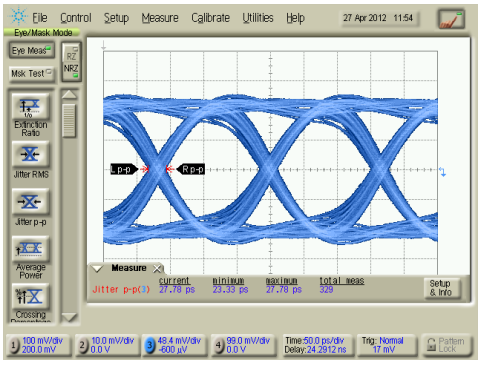
Fig. B.19. Measured eye-diagrams which is after equalization under 300mV input swing with (a) 61-inch (b) 28-inch (c) 12-inch (d) 0-inch



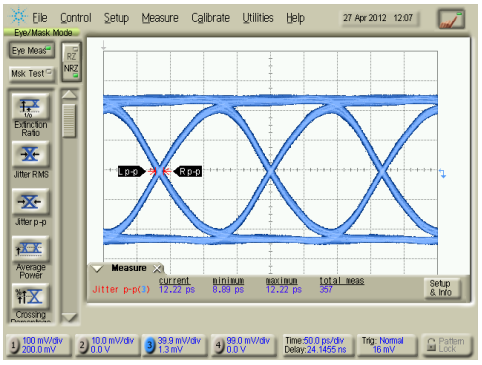
(a)



(b)

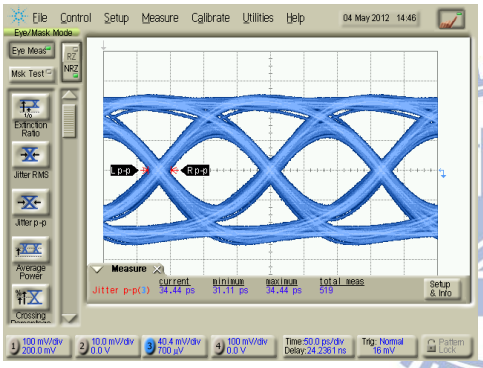


(c)

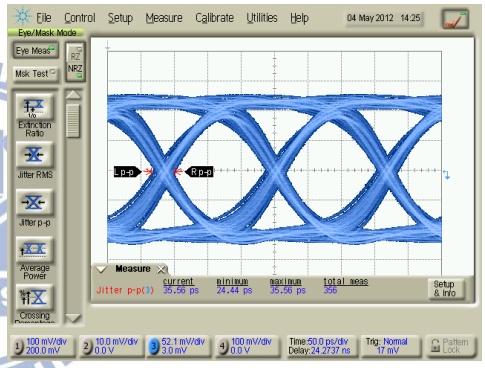


(d)

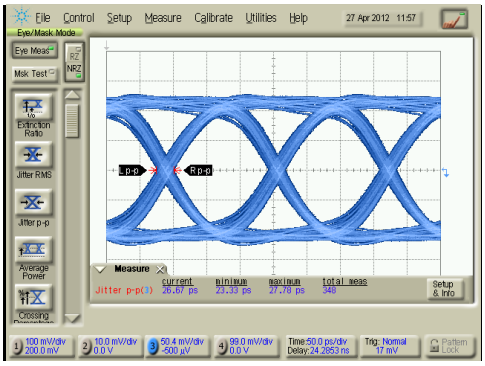
Fig. B.20. Measured eye-diagrams after equalization when input swing is 400mV$_{p\text{-}p}$ under (a) 61-inch (b) 28-inch (c) 12-inch (d) 0-inch



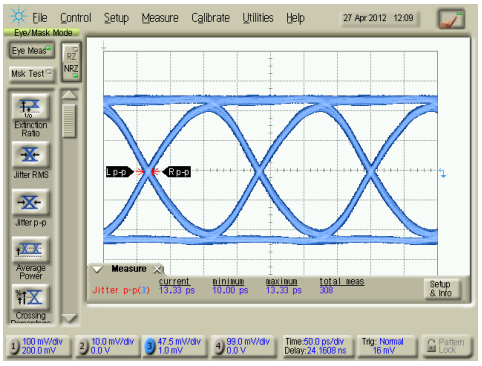
(a)



(b)

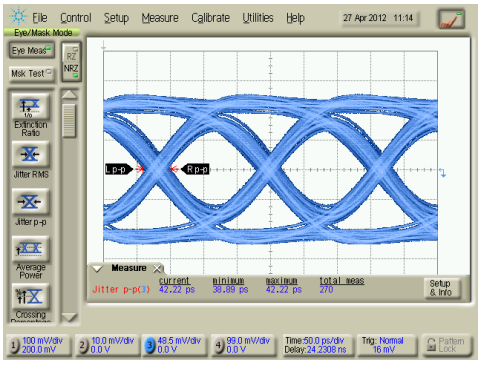


(c)

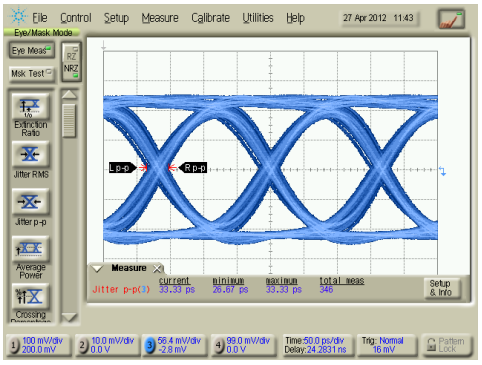


(d)

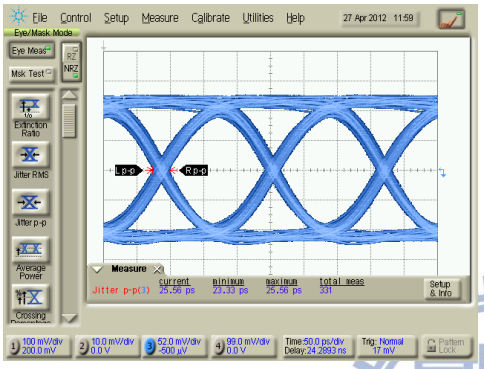
Fig. B.21. Measured eye-diagrams after equalization when input swing is 500mV$_{p\text{-}p}$ under (a) 61-inch (b) 28-inch (c) 12-inch (d) 0-inch



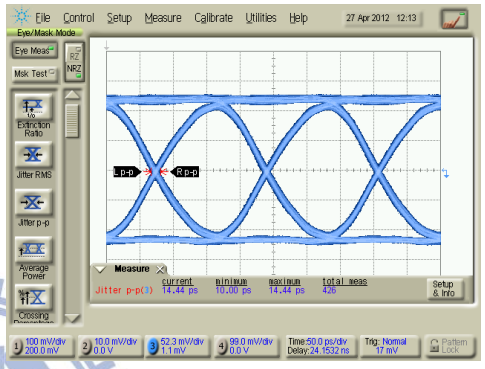
(a)



(b)



(c)



(d)

Fig. B.22. Measured eye-diagrams after equalization when input swing is 600mV$_{p\text{-}p}$ under (a) 61-inch (b) 28-inch (c) 12-inch (d) 0-inch

Table B.1 shows the performance comparison of this work. This chip demonstrates well adaptive equalization at 6Gb/s data rate for trace lengths up to 61 inches in 0.18μm CMOS technology while consuming only 27mW (without output buffer) from a 1.8V power supply.

Table B.1 Performance Comparison

	JSSC'03 [2]	**JSSC'04 [3]**	**TCAS-II'10 [28]**	**This work**
Technology	0.13μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS
Supply Voltage (V)	1.5	1.8	1.6	1.8
Data rate (Gb/s)	5	3.5	5	6
Channel Loss (dB)	18*	16	14	23.3
$Jitter_{p\text{-}p}$ (UI)	0.39	0.39	0.28	0.25
$Input\ Swing_{p\text{-}p}$ (V)	N.A.	0.6~1.4	0.75	0.2~0.6
Power(mW)	10*	80	17.6	27
Area (mm^2)	0.1*	0.35**	0.1**	0.09**
FoM	0.11	1.43	0.25	0.19

* Only equalizer **Only active schematics

$$\mathrm{FoM} = \frac{\mathrm{Power}}{\mathrm{DataRate} \times \mathrm{Loss}}$$

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