國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

應用於無線感測網路之低功率 1.4-GHz 射頻前端接收器與傳送器電路設計

Low-Power 1.4-GHz Transceiver Front-End Circuit Design for Wireless Sensor Network Application

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碩士論文

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摘要

本篇論文的主要目的在設計應用於無線感測網路之低功率射頻前端接收器與傳送器電路。此接收器與傳送器被實現於一顆聯電 90 奈米 CMOS 製程的晶片當中，整顆晶片的大小為 1360μm×1210μm。所設計之接收器為一組操作在 1.4-GHz 的低功率射頻前端接收電路，其包含有一顆低雜訊放大器、I/Q 降頻混頻器以及一顆用以將此前後兩級交流耦合之變壓器。設計以共源級放大器串疊架構來實現低雜訊放大器，適用於在低功率操作之下做高效率之訊號放大以及電壓對電流之轉換。並且，設計三端變壓器將單端訊號轉換成為雙端訊號，進一步地省去訊號轉換之功率消耗。最後，設計以雙平衡混頻器之架構來實現降頻混頻器，把訊號降頻後再輸出。論文中針對變壓器的架構以及其共振操作加以分析與設計，用以提供最大電流轉換增益。所設計之傳送器為一組操作在 1.4-GHz 的低功率射頻前端傳送電路，其包含有一顆升頻混頻器、一顆前級驅動器以及一顆功率放大器。設計以被動架構來實現升頻混頻器，用以省去升頻混頻器之功率消耗。並且，設計以反向器架構來實現前級驅動器，其適用於在低功率操作之下對訊號的電壓擺幅做高效率的驅動。最後，設計以 A 類放大器架構來實現功率放大器，用以完成高線性度的功率放大器。本論文將低雜訊放大器之輸入阻抗匹配的電感和功率放大器之輸出阻抗匹配的電感整合於晶片當中，進一步地在晶片上實現系統整合。此接收器與傳送器不只是針對低功率消耗還設計其符合無線遠距醫療服務 Wireless Medical Telemetry Service (WMTS) 的 1.4-GHz 頻帶的各項規格。

Low-Power 1.4-GHz Transceiver Front-End Circuit Design

for Wireless Sensor Network Application

Student：Hui-Shun Huang　　Advisor：Prof. Chien-Nan Kuo

Department of Electronic Engineering & Institute of Electronics

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ABSTRACT

This thesis aims to design a low-power 1.4-GHz transceiver front-end circuit for wireless sensor network application. The whole transceiver is implemented on a single chip by using UMC 90-nm CMOS technology, and the chip size is only 1360μm×1210μm. The designed receiver contains a low noise amplifier, I/Q down-conversion mixers, and a transformer which conducts AC coupling between the LNA and the mixers. The LNA is realized in the common-source cascode architecture which has high gain efficiency even in low-power operation. The 3-terminal transformer transfers the single-end signal to the differential form without power consumption. The I/Q down-conversion mixers are in the double-balance structure which is favorable for the direct-conversion receivers. This thesis focuses on the analysis of the transformer resonance operation for realizing the maximal current gain. The designed transmitter is composed of an up-conversion mixer, a pre-amplifier, and a power amplifier. The up-conversion mixer is realized in the passive architecture on the purpose of saving power consumption. The inverter-based pre-amplifier has efficient voltage gain with consuming a little DC current. The PA is realized by a class-A amplifier under the linearity consideration. The two inductances in the LNA input matching and the PA output matching are both integrated on this chip in order to achieve the sub-system integration. This transceiver is designed to not only reduce the power consumption but also meet all specifications of the 1.4-GHz band in Wireless Medical Telemetry Service.

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待人處世。我永遠忘不了當我的 VGA 設計有困難時，子超學長在一想到解決方法時，當下就把點子告訴我，也協助我順利完成後續的設計。

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碩士班兩年多，最後要感謝我的好兄弟凱翔，不論是在課業、研究、生活、感情、人生和家庭，真的很開心能夠在交大認識這一位無所不談、互相加油打氣的好朋友，我永遠不會忘記在修習數位通訊時，凱翔多次特別為我補習，協助我修得學分，碩士班兩年多來，大大小小各種困難，凱翔都給我許多幫助，暉舜永遠銘記在心。

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黃暉舜

民國 100 年九月

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Chapter 1 Introduction

1.1 Wireless Sensor Network in Medical Application

Recently, because the development of modern technology, the wireless sensor network (WSN) are widely used in medical service. In medical application, the WSN is usually employed in health monitoring. This WSN in medical application is called wireless body area network (WBAN), as shown in Fig. 1.1. A number of miniature sensor nodes are installed at human body and connected wirelessly together. The sensor nodes monitor the health conditions of human beings and communicate the biological signals to a center node by electrical signals. The center node collects all data and transmits it to other devices like cell phones by a telecommunication standard such as Wireless Local Area Network.

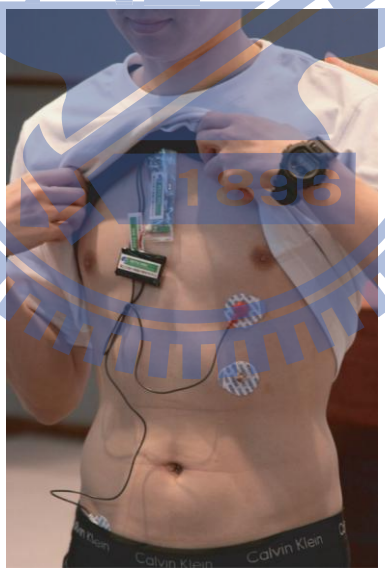

Fig. 1.1 Wireless body area network

Hospitals and telemedical centers use the WBAN system to continuously monitor the health conditions of patients and conduct appropriate treatments earlier in emergencies. Because the sensor nodes of the WBAN are made in very small sizes and connected wirelessly together, patients would feel comfortable and their health conditions can be well controlled. To realize the miniature sensor nodes and

extend the lifetime of these devices with small batteries carried by patients, the circuits in the sensor nodes should be realized with high integration level, and the power consumption must be reduced.

1.2 Literature Survey of Low-Power Transceiver

Using passive circuits, current reuse technique, and low supply voltage are three major way to reduce circuit power consumption. In this section, we introduce three low power circuits using these techniques.

In reference [11], a low-power 2.4-GHz direct-conversion RF transceiver is presented. The transceiver schematics are as shown in Fig. 1.3 (a) and (b).

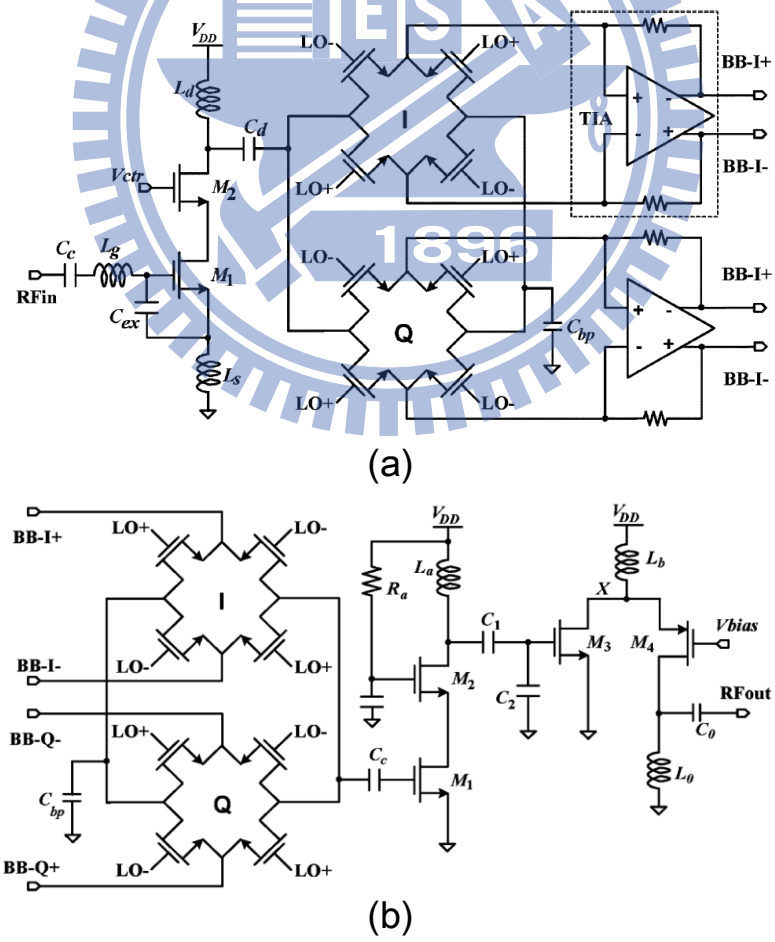

Fig. 1.2 Low-power 2.4-GHz direct-conversion (a) receiver (b) transmitter

The mixers in the transmitter and the receiver are both the passive CMOS mixer for saving power consumption. The driver amplifier of the transmitter is composed of two stages which are gain and out stages. The gain stage is the conventional cascode amplifier on the purpose of achieving high gain in low power operation. The folded-cascode architecture is employed in the output stage for higher voltage headroom under low supply voltage, thereby improving the linearity. The passive CMOS mixer is also employed in the transceiver in this thesis for saving power consumption.

In reference [13], a low-power 868/915-MHz transceiver for wireless sensor network is introduced. The transceiver block diagram is as shown in Fig. 1.3.

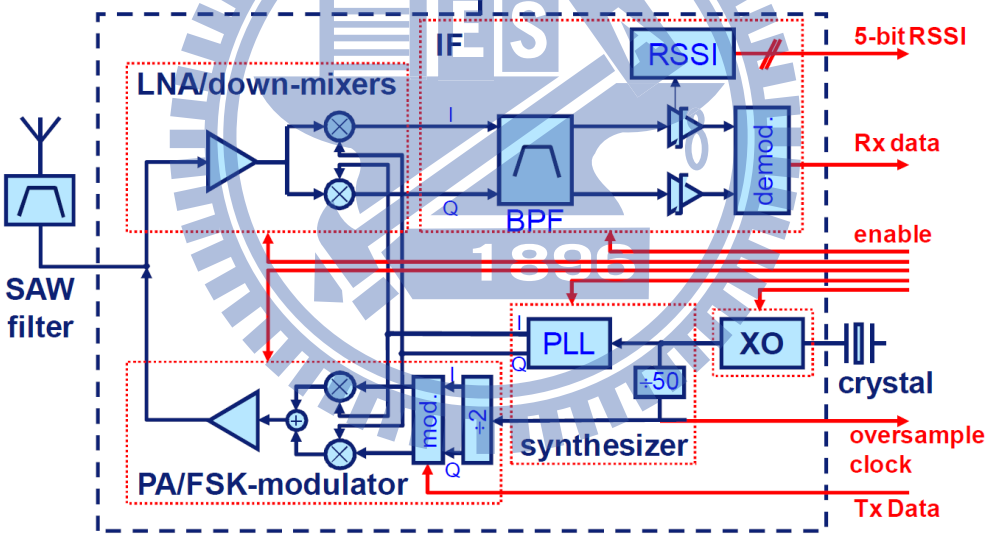

Fig. 1.3 Low-power 868/915-MHz transceiver

The most outstanding feature of this transceiver is the PA, as shown in Fig. 1.4. The author cascades three push-pull amplifiers at one current path. This current reuse architecture greatly enhances the PA efficiency. However, the PA output voltage swing is limited because the six cascode transistors. This current reuse architecture is only used in the low output power application.

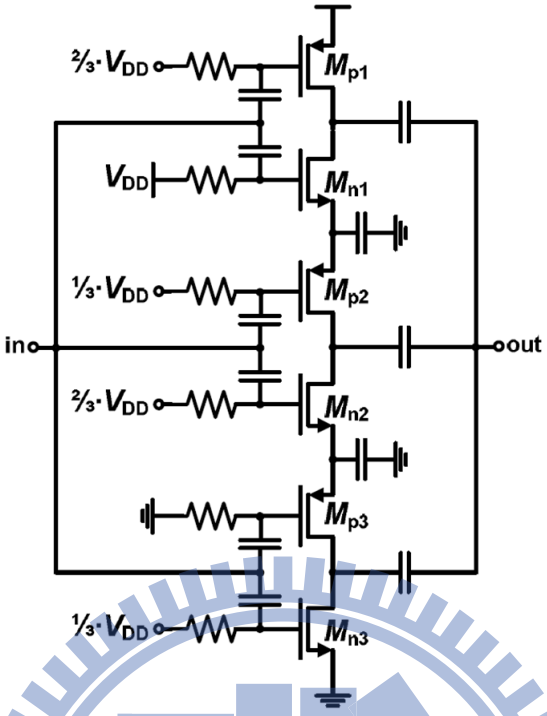

Fig. 1.4 Current reuse low power PA

In reference [14], a low power mixer is introduced. The mixer schematic is as shown in Fig. 1.5.

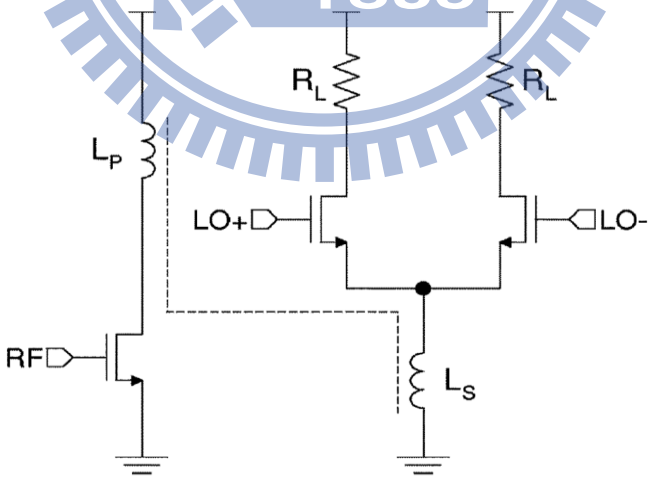

Fig. 1.5 Transformer based low power mixer

The transformer coupling effect is used between the transconductance stage and the switching stage of the mixer. The transformer based architecture reduces the supply voltage, and further saves the power consumption. The proposed equivalent model

of the transformer in reference [14] is as shown in Fig. 1.6.

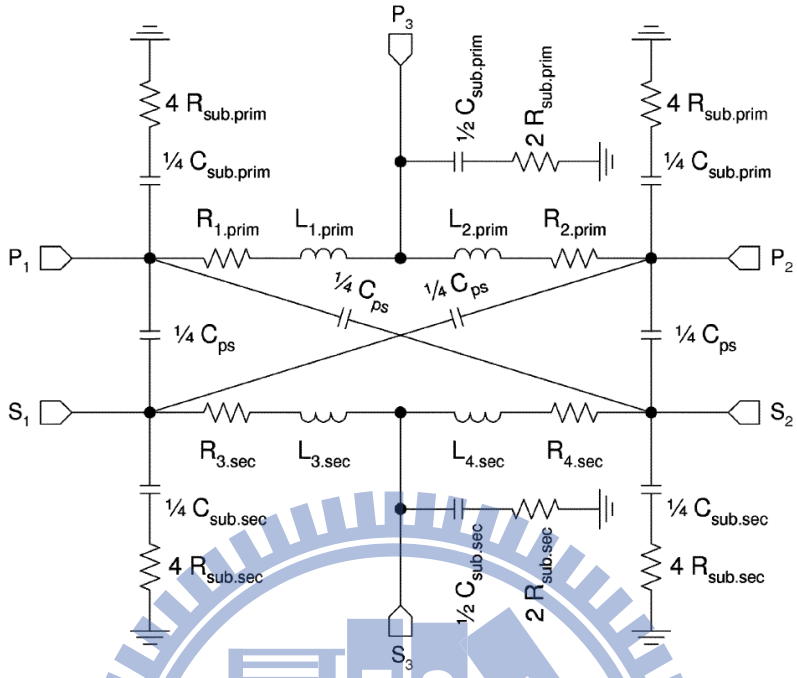

Fig. 1.6 The proposed equivalent model of the transformer in reference [14]

The proposed equivalent model of the transformer in reference [14] is analyzed by the multivariate analysis. The multivariate analysis causes the difficulty to optimize the transformer.

The transformer technique is also used in the transceiver of this thesis for saving the power consumption. We propose a more efficient way to design an optimal transformer.

1.3 Thesis Organization

In Chapter 2, the system application scenario, specification and structure of the low-power 1.4-GHz transceiver are introduced, respectively. In Section 2.1, the system application scenario will be introduced. The system specifications of the transceiver are defined in Section 2.2. The proposed system structure for these specifications especially for low power consumption is presented in Section 2.3.

In Chapter 3, the designed structure of the low-power 1.4-GHz receiver and the circuit design of each block are introduced, respectively. Section 3.1 shows the designed structure of the receiver. A LNA in common-source cascade topology with

inductive degeneration is introduced in Section 3.2. Section 3.3 presents the double balance down-conversion mixer. The analysis and design of the transformer resonant operation are introduced in Section 3.4. Section 3.5 gives a summary of the designed receiver.

In Chapter 4, the designed structure of the low-power 1.4-GHz transmitter and the circuit design of each block are introduced, respectively. Section 4.1 shows the designed structure of the transmitter. A passive up-conversion mixer is introduced in Section 4.2. Section 4.3 presents a class-A power amplifier. An inverter-based pre-amplifier is introduced in Section 4.4. Section 4.5 gives a summary of the design transmitter.

In Chapter 5, the chip implementation, measurement setups, and measurement results are introduced. Section 5.1 presents the chip implementation. The chip measurement setups and measurement results are putted in Section 5.2.

In Chapter 6, a conclusion and the future work are introduced. Section 6.1 gives a conclusion of this designed transceiver. Section 6.2 presents the future work of this topic.

Chapter 2

System Application Scenario, Specification and Architecture

2.1 System Application Scenario

The system application scenario of the WBAN which this transceiver applies to is as showed in Fig. 2.1.

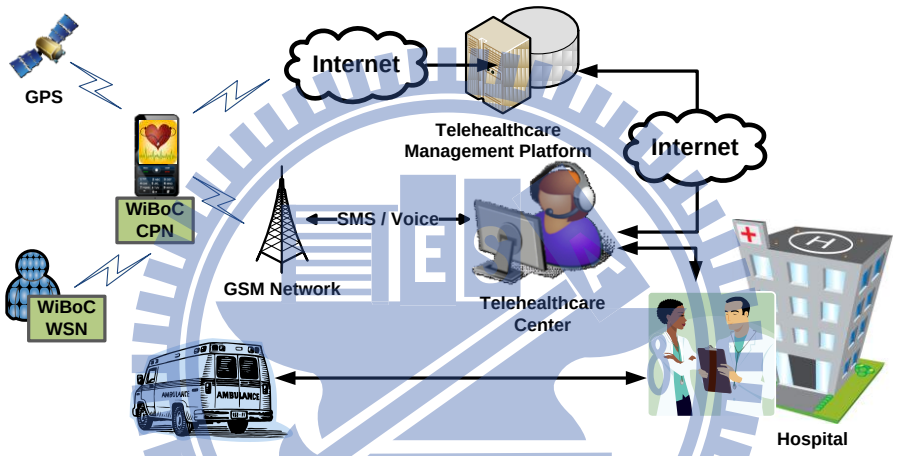

Fig. 2.1 System application scenario of the wireless body area network

Telemedical centers use this WBAN system to continuously monitor the health condition of patients, especially disabled old persons. This WBAN are composed of wireless sensor nodes, electrocardiogram sensors (ECG sensors), cell phone system, and the expert system algorithm. The wireless sensor nodes are installed at the upper bodies of human beings. The sensor nodes sense the heartbeat, and communicate the electrocardiogram data to a center node by electrical signals. The center node collects all electrocardiogram data and updates it to telemedical centers through cell phone system. The expert system algorithm, which is installed in the cell phone, determines that the current electrocardiogram data is regular or not, and gives an alarm to telemedical centers or hospitals when the heat beat is not regular.

Telemedical centers use this system to continuously monitor the current electrocardiogram of patients and make appropriate medical treatments earlier for emergencies.

Fig. 2.2 shows the structure of the wireless sensor node this low-power transceiver applies to. The wireless sensor node is composed of an antenna, RF circuits, analog baseband circuits, digital baseband circuits, a micro controller unit (MCU), memories, and an ECG Sensor.

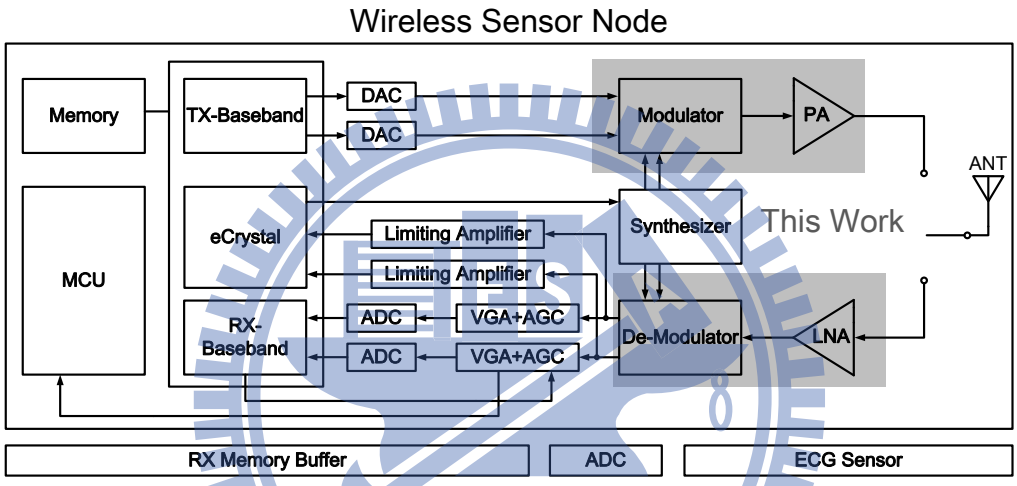

Fig. 2.2 Structure of the wireless sensor node

This thesis focuses on the implementation of the RF transceiver front-end circuits of the wireless sensor nodes, as showed in Fig. 2.3. This transceiver consists of an up-conversion mixer, a PA, a LNA, and I/Q down-conversion mixer. All circuits must be integrated and realized on a single chip of 90-nm CMOS process. All circuits except PA operate under 1-V V_{DD}. In the transmitter, the up-conversion mixer transfers the analog baseband signal to RF signal, and the PA provides the RF signal with power gain and outputs it to the antenna. In the receiver, the LNA amplifies the RF signal, and the I/Q down-conversion mixers transfer the RF signal to analog baseband signal. Both the transmitter and the receiver are direct-conversion structure.

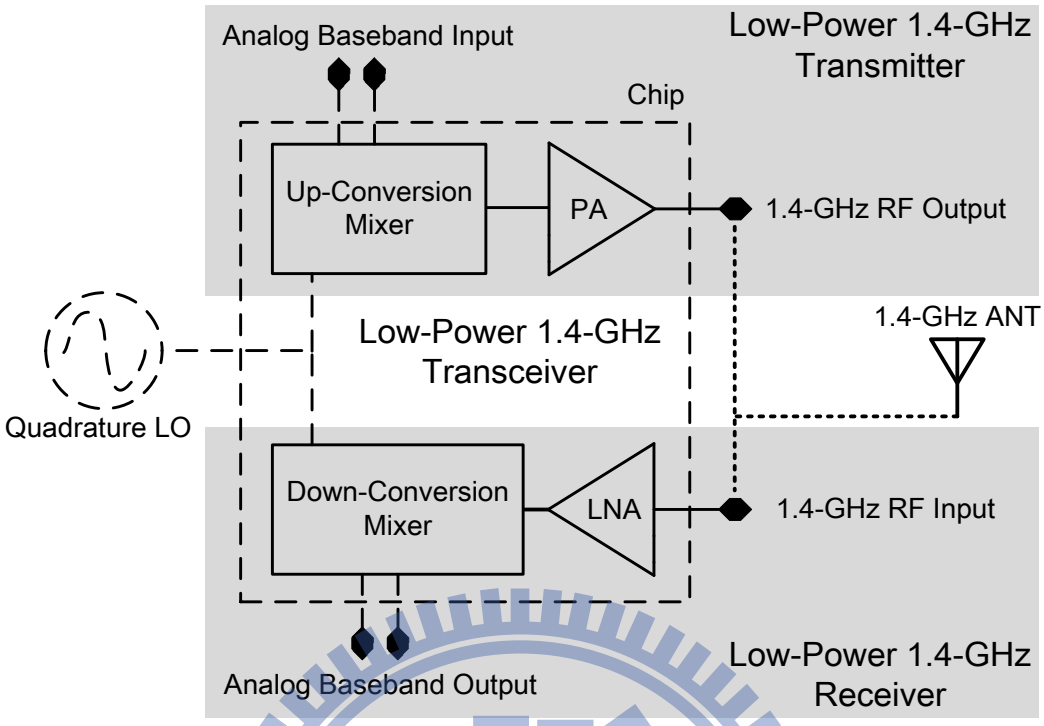

Fig. 2.3 RF transceiver front-end circuit blocks of the wireless sensor node

2.2 System Specification

For the WSN application, power consumption is the specification with top priority. The power consumption specification of the transmitter and the receiver are 25-mW and 6-mW, respectively. The frequency channel is 1395-1400 MHz, which is one band of Wireless Medical Telemetry Service.

In this WBAN system application, the peak output power of the transmitter is 4-dBm, and the average output power of the transmitter is -3 dBm with 7 dB peak to average power ratio. According to the 4 dBm transmitter peak output power and 10% efficiency specification, the power consumption specification of the transmitter is 25-mW.

In this WBAN system application, the conversion gain specification of the receiver is 20 dB. System designer limits the receiver NF referred to the antenna

terminal to 7 dB with 6-mW power consumption. The linearity specification of the receiver is -25 dBm P_{1dB}. Table 2.1 and Table 2.2 make the summary of the specifications of the transmitter and the receiver, respectively.

Table 2.1 Transmitter specification

Peak Transmit Power	4 dBm
Average Transmit Power	-3 dBm
DC Power Consumption	25mW
Efficiency	10%

Table 2.2 Receiver specification

Conversion Gain	20 dB
Noise Figure	7 dB
DC Power Consumption	6 mW
P_{1dB}	-25 dBm

2.3 Proposed System Structure

Fig. 2.4 shows the proposed system structure of the low-power 1.4-GHz transceiver.

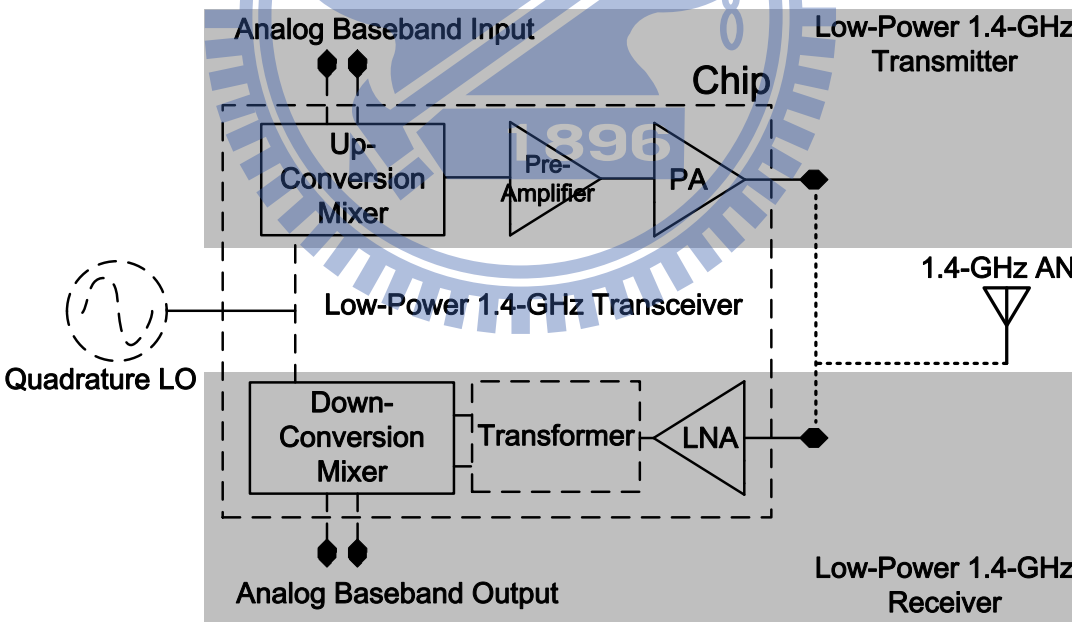

Fig. 2.4 Proposed system structure of the low-power 1.4-GHz transceiver

In this receiver, the first stage is a LNA which amplifies the 1.4-GHz RF signal and compresses noise of the receiver train, the second stage is a 3-terminal transformer as a passive balun which transfers the single-end signal to differential form without

power consumption, and the final stage is I/Q down-conversion mixers which transfer the 1.4-GHz RF signal to the analog baseband signal with I/Q output. In the transmitter, the first stage is an up-conversion mixer which transfer the analog baseband signal to the 1.4-GHz RF signal, the second stage is a pre-amplifier which provides the RF signal with efficient voltage gain in order to give enough voltage signal swing to the PA stage, and the final stage is a PA, which provides the RF signal with power gain and outputs it to the antenna. Both the transmitter and the receiver take the off chip quadrature local oscillation (LO) signal source.

Chapter 3 Receiver Circuit Design

3.1 Structure of the Low-Power 1.4-GHz Receiver

The designed structure of the low-power 1.4-GHz direct-conversion receiver is showed in Fig. 3.1, which is composed of a common source cascade LNA with inductive degeneration, a 3-terminal transformer as a passive balun, and I/Q double balance down-conversion mixers. The LNA completes both the input impedance matching and the noise matching at 1.4-GHz, amplifies the received RF signal and transfers it to current form. The 3-terminal transformer transfers the single-end RF current signal to differential form without DC power consumption, and passes it from the LNA to the mixers in the highest efficiency by the resonator coupling operation. The double balance down-conversion mixers, which are appropriately designed in the trade-off between the conversion gain and the linearity, transfer the 1.4-GHz RF signal to the analog baseband signal with I/Q output.

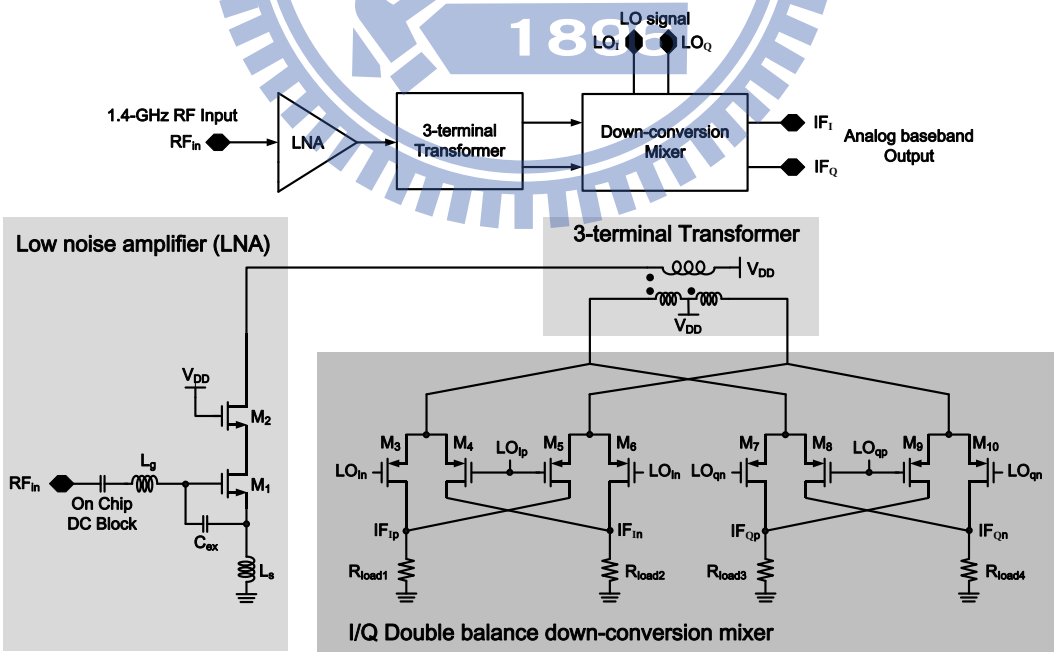

Fig. 3.1 Schematic of the receiver core circuit

3.2 Low Noise Amplifier

The first stage of the receiver is a common source cascode amplifier with inductive degeneration. This LNA is composed of a common source amplifier M_1, two inductances L_g and L_s, an external capacitor C_{ex}, and a common gate amplifier M_2, as shown in Fig. 3-1. This type of amplifier has good gain efficiency which is an appropriate choice for the low-power application. The source degeneration inductance L_s is in order to generate a real term in the input impedance of the LNA, and we can choose appropriate value of L_s to generate a 50-Ω real term in the input impedance. The gate inductance L_g is used to set the resonant frequency after L_s is chosen in order to produce a pure 50-Ω input impedance matching in which the imaginary term is equal to zero. The external capacitor C_{ex} is used to compensate the small parasitic capacitor between gate and source of M_1 in order to help L_g and L_s to simultaneously complete the input impedance matching and the noise matching at 1.4-GHz. This type of input impedance matching is a narrow band input matching, as shown in Fig. 3.2.

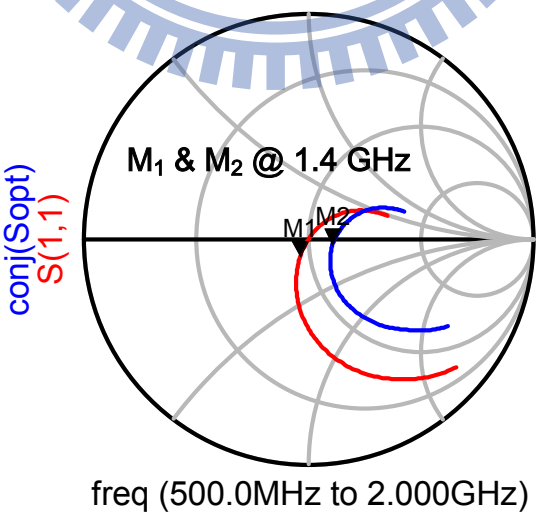

Fig. 3.2 Smith chart of LNA input matching

However, the wireless sensor network application is also a narrow band application. The operation frequency is from 1.395 to 1.400-GHz, so the narrow band input impedance matching is not a limitation. The common gate amplifier M_2 provides low impedance at the output node of common source amplifier M_1, and leads to negligible Miller effect of M_1. M_2 also provides high impedance at the output node of M_2 itself, which leads the LNA high gain in high frequency. Two inductances L_g and L_s, and capacitor C_{ex} complete both input impedance matching and noise matching [6]. The input impedance and noise factor of this type of LNA can be expressed as:

$$Z_{in}(s) = s(L_s + L_g) + \frac{1}{s(C_{gs}+C_{ex})} + \left(\frac{g_{m1}}{C_{gs}+C_{ex}}\right)L_s \tag{3.1}$$

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s \left(\frac{\omega_0}{\omega_T}\right)^2 \tag{3.2}$$

where C_{gs} represents the parasitic capacitor between gate and source of M_1, g_{m1} is the transconductance of M_1, R_l is the series resistance of L_g, R_s is the source resistance, γ is a bias-dependent factor, g_{d0} is the zero-bias drain conductance of transistor M_1. By eq. (3.1) and (3.2), we can design appropriate values of V_{gs}, L_g, C_{ex}, L_s, and the transistor sizes of M_1 and M_2 for specifications of the receiver. Here we choose V_{gs}=0.43 V, L_g=7.6 nH with Q = 5.7, C_{ex}=1.6 pF, L_s=0.7 nH, $(\frac{W}{L})_1 = \frac{90\text{ um}}{0.09\text{ um}}$, and $(\frac{W}{L})_2 = \frac{90\text{ um}}{0.09\text{ um}}$ for the optimum noise matching and 50-Ω input impedance matching in 4.5 mW DC power consumption. It can achieve simulated performance of -21.8 dB input insertion loss, 2.5 dB noise figure.

3.3 Down-Conversion Mixer Design

The third stage of the receiver is I/Q double balance down-conversion mixers. In the system application, the receiver has to have I/Q analog based band output, so the

I/Q double balance mixers are used here. The I/Q double balance mixers are composed of eight pMOS transistors $M_{3\text{-}10}$ as the switching stage and four resistors $R_{load1\text{-}4}$ as loads, as shown in Fig. 3-1. The double balance mixer has advantages of better port-to-port isolation and less even-order distortion [2]. The letter is especially critical in the direct-down-conversion mixer.

A common mixer such as Gilbert Cell is composed of a transconductance stage, which transfers input RF voltage signal to current form, a current switching stage, which uses local oscillation signal to switching RF current signal and transfers it to analog baseband signal, and a load resistor stage. In this receiver, the LNA and the transconductance stage of mixers are combined together in order to save the DC power consumption of the transconductance stage of the mixers. The LNA amplifies the received RF signal and transfers the voltage signal to current form, and the 3-terminal transformer transfer the single-end RF current signal to differential form and passes it to the switching stage of the mixers. Finally, the current switching stage uses local oscillation signal to switch the RF current signal, and transfers it to the analog baseband signal.

pMOS transistors are employed in the switching stage of mixers, because pMOS transistor has better flicker noise performance as compare to nMOS transistor [6]. The ideal switching stage has that only one transistor of the switching pair is turned ON at the same time, and the current is equal to zero when the switch is turned OFF. Therefore, to make the switching stage more ideal, the transistors with bigger size are used, and the DC gate voltage bias is set to near threshold voltage. The load resistors are related to conversion gain and linearity of the mixers, as shown in Fig. 3.3.

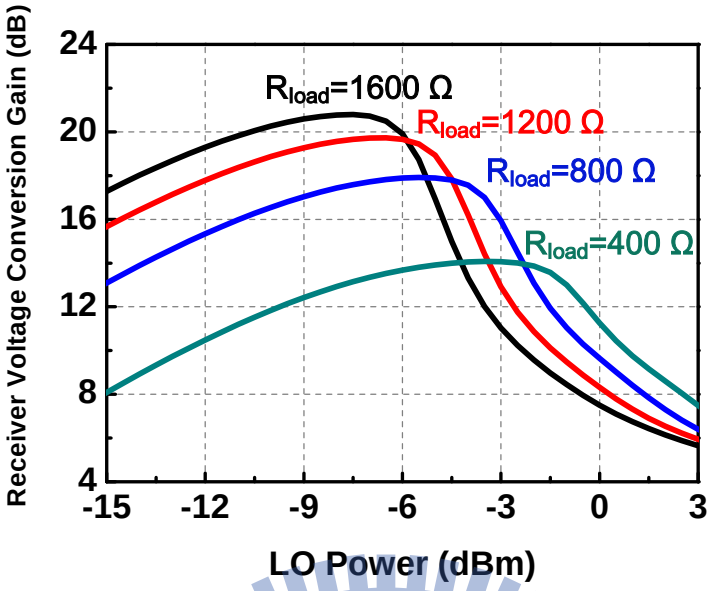

Fig. 3.3 Receiver voltage conversion gain versus LO power

In Fig. 3.3, the maximal conversion gain of the receiver is approximately proportional to the value of the load resistors. The bigger load resistors are used, the maximal conversion gain is higher, and the LO power of the maximal conversion gain is lower. However, the linearity of the receiver becomes worse with the increasing of the conversion gain. In the system application, there is a linearity specification of the receiver is -25 dBm P_{1dB}. The appropriate value of the load resistors can be found by trade-off between the linearity and the conversion gain of the receiver.

In the design of the mixers, each value of each component can be defined by following above design considerations. The transistor sizes of $M_{3\text{-}10}$ is $(\frac{W}{L})_{3-10} = \frac{80\text{ um}}{0.09\text{ um}}$, the DC gate voltage bias of the switching stage is 0.2-V V_{SG}, and the load resistors $R_{load1\text{-}4}$ are 800 Ω. The total DC power consumption of two double balance mixers is 0.5-mW. The LO power of maximal conversion of the designed receiver is -5 dBm, which is lower than the LO power of the common receivers.

3.4 Transformer Design

Between the LNA and the mixers, there is a 3-terminal transformer, as shown in Fig. 3.4. The 3-terminal transformer needs to be carefully designed to transfer the single-end RF current signal to differential form with the maximal current gain.

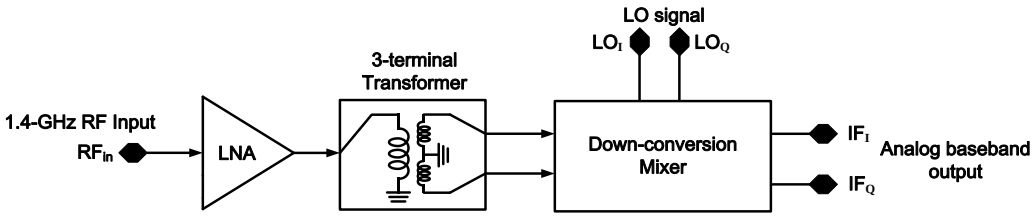

Fig. 3.4 Block diagram of the receiver

The 3-terminal transformer is composed of two coupled resonators, which is called resonator coupling network (RCN). Under the critical resonance condition, the RCN can provide the maximal current gain at resonance frequency, which is almost equivalent to an ideal transformer [6]. Fig. 3.5 (a) shows the transformer used in the receiver. It can be modeled into the resonator coupling network, as shown Fig. 3.5 (b).

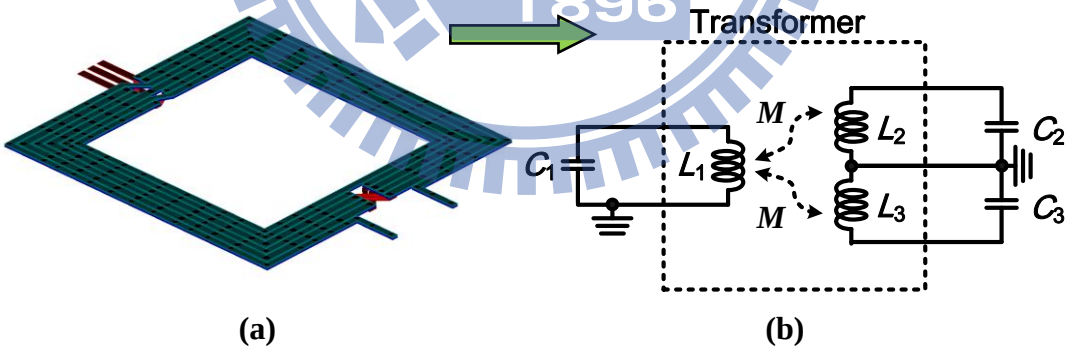

Fig. 3.5 (a) Designed 3-terminal transformer, (b) Resonator coupling network

In Fig. 3.5 (b), L_1 is the primary coil of the transformer, L_2 and L_3 are two secondary coils of the transformer with the same value, and M is the mutual inductance between primary and secondary coils. C_1 and L_1 form a resonator which connects to the output node of the LNA, and L_2, C_2, L_3, and C_3 form two resonators which connect to the

input nodes of the mixers. The whole receiver is modeled into the equivalent network, as shown in Fig. 3.6. In Fig. 3.6, R_{LNA} and C_{LNA} model the output impedance of the LNA, L_1 and C_{p1} model the inductance and parasitic capacitor of the primary coil of the transformer, $L_{2\text{-}3}$ and $C_{p2\text{-}p3}$ model the inductances and parasitic capacitors of the secondary coils of the transformer, and $C_{Mixer1\text{-}4}$ and $R_{Mixer1\text{-}4}$ model the input impedance of the mixers. The two parallel capacitors C_{LNA} and C_{p1} form the C_1 of the RCN, and $C_{p2\text{-}p3}$ and $C_{Mixer1\text{-}4}$ form the C_2 of the RCN.

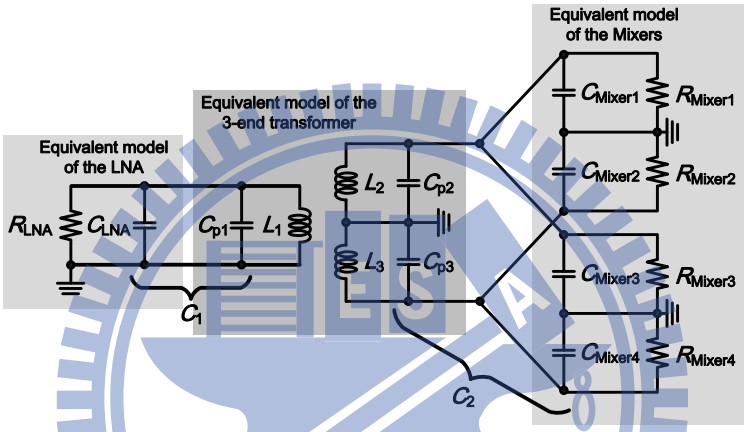

Fig. 3.6 Resonator coupling network

The transformer connects two identical parallel double balance mixers, so these two mixers can be basically simplified into a mixer with double size. Moreover, because the transformer is symmetric to the virtual ground of secondary coil, the RCN can be analyzed by the two-port network, as shown in Fig. 3.7. I_{in} represents the RF current signal from the LNA, C_1 includes the parasitic capacitors of the LNA and the primary coil of the transformer and C_2 includes the parasitic capacitors of the mixers and the secondary coils of the transformer.

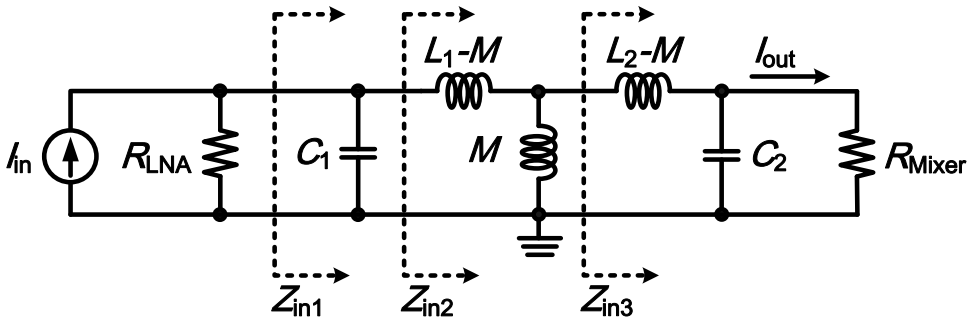

Fig. 3.7 Two-port network of the RCN

The resonance frequencies of primary and secondary uncoupled resonators are defined as ω_1 and ω_2, and m is the ratio of these two resonance frequencies.

$$\omega_1 \equiv \frac{1}{\sqrt{L_1 C_1}} \qquad \omega_2 \equiv \frac{1}{\sqrt{L_2 C_2}} \qquad \omega_1 \equiv m\omega_2 \tag{3.3}$$

The mutual inductance between the primary and secondary coils is M, and the coupling coefficient is defined as

$$k \equiv \frac{M}{\sqrt{L_1 L_2}} \tag{3.4}$$

In the coupled network, the resonance frequencies would shift to other two frequencies, as shown in Fig. 3.8. These two resonance frequencies in coupled network can be expressed in term of m, k, and ω_2, as shown in eq. (3.5) and (3.6) [6].

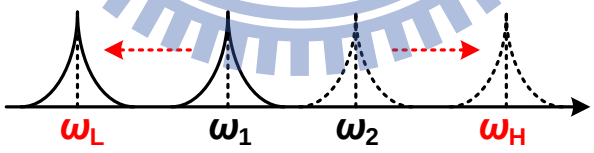

Fig. 3.8 Resonance frequencies of the RCN

$$\omega_H = \omega_2 \sqrt{\frac{1+m^2+\sqrt{m^4+2(2k^2+1)+m^2+1}}{2(1-k^2)}} \tag{3.5}$$

$$\omega_L = \omega_2 \sqrt{\frac{1+m^2-\sqrt{m^4+2(2k^2+1)+m^2+1}}{2(1-k^2)}} \tag{3.6}$$

At these two resonance frequencies ω_H and ω_L, the transformer passes the RF current signal from the LNA to the mixers in highest efficiency. Either resonance frequency can be chosen as the operating frequency.

In the two-port analysis, the transfer function from I_{in} to I_{out} at the resonance frequency is derived as

$$\left|\frac{I_{out}}{I_{in}}\right|_{\omega_H,\omega_L} = \frac{R_{LNA}}{R_{LNA}+\left\{\frac{n}{k}[1-(1-k^2)r^2]\right\}^2 R_{Mixer}} \times \frac{n}{k}[1-(1-k^2)r^2]$$

$$= \frac{AR_{LNA}}{R_{LNA}+A^2R_{Mixer}}$$

$$\text{where } A = \frac{n}{k}[1-(1-k^2)r^2] \qquad n = \sqrt{\frac{L_1}{L_2}} \qquad r = \frac{\omega_0}{\omega_2} \qquad (3.7)$$

The k is the coupling coefficient between the primary coil and the secondary coils, and n is the ratio of the inductance of the primary coil to the inductance of one secondary coil. The k and n of the maximal current gain condition can be found by the partial differential equation of eq. (3.7) for k and n. These two partial differential equations are

$$\frac{\partial I_{out}/I_{in}}{\partial k} = 0 \qquad \frac{\partial I_{out}/I_{in}}{\partial n} = 0 \qquad (3.8)$$

These two partial differential equations lead the result as

$$R_{LNA} = Z_{in1}|_{\omega_0} = \frac{n^2}{k^2}[1-(1-k^2)r^2]^2 \times R_{Mixer} \qquad (3.9)$$

Eq. (3.9) means the impedance matching between the LNA and the transformer. The impedance matching also happens at the interface between the transformer and the mixers. Under the critical coupling condition, the RF current signal is coupled from the LNA to the mixer in the highest efficiency. From eq. (3.7) and (3.9), the maximal current gain under the critical coupling condition is

$$\left|\frac{I_{out}}{I_{in}}\right|_{max,\omega_H,\omega_L} = \frac{1}{2}\sqrt{\frac{R_{LNA}}{R_{Mixer}}} \qquad (3.10)$$

Eq. (3.10) means that the maximal current gain of the transformer is determined by R_{LNA} and R_{Mixer}. The RCN gets the same result of the maximal current gain like an ideal transformer as *k* and *n* are chosen appropriately. eq. (3.10) also means that the maximal current gain is higher with higher R_{LNA} and lower R_{Mixer}. This result corresponds to the simple circuit theory. Current is injected from high impedance to

low impedance. With the same voltage drop between the high impedance node and the low impedance node, more current is injected when the high-impedance is higher and the low-impedance is lower.

The higher impedance ratio of R_{LNA}/R_{Mixer} is design to get the higher maximal current gain under the critical coupling condition. Under the condition of that all performances of the receiver meet all specifications, the output impedance of the LNA and the input impedance of the mixer are designed to as higher and as lower as possible, respectively. In this receiver, R_{LNA} is designed to be 552 Ω and R_{Mixer} is designed to be 15 Ω. Therefore, maximal current gain $\left|\frac{I_{\mathrm{out}}}{I_{\mathrm{in}}}\right|_{max,\omega_H,\omega_L}$ is equal to about 3. After getting the value of maximal current gain of the RCN, the corresponding ratio of $n = \sqrt{\frac{L_1}{L_2}}$ and the ratio of $r = \frac{\omega_0}{\omega_2}$ need to be chosen to realize the transformer with the maximal current gain at 1.4 GHz. In the current gain contour plots mapping *k* and *r* of n=1~4, as shown in Fig. 3.8, there are two areas of maximal current gain when $r > 1$ and $r < 1$ in each contour plot, that represents two resonance frequencies of the RCN ω_H and ω_L. The maximal current gain of $r > 1$ operates at ω_H and the other one operates at ω_L. The area of the maximal current gain at ω_L is bigger than the other one at ω_H, so the RCN is designed at ω_L can be more tolerant of the variation of r and k. Therefore, the RCN at ω_L is easier to be realized and more tolerant of process variation.

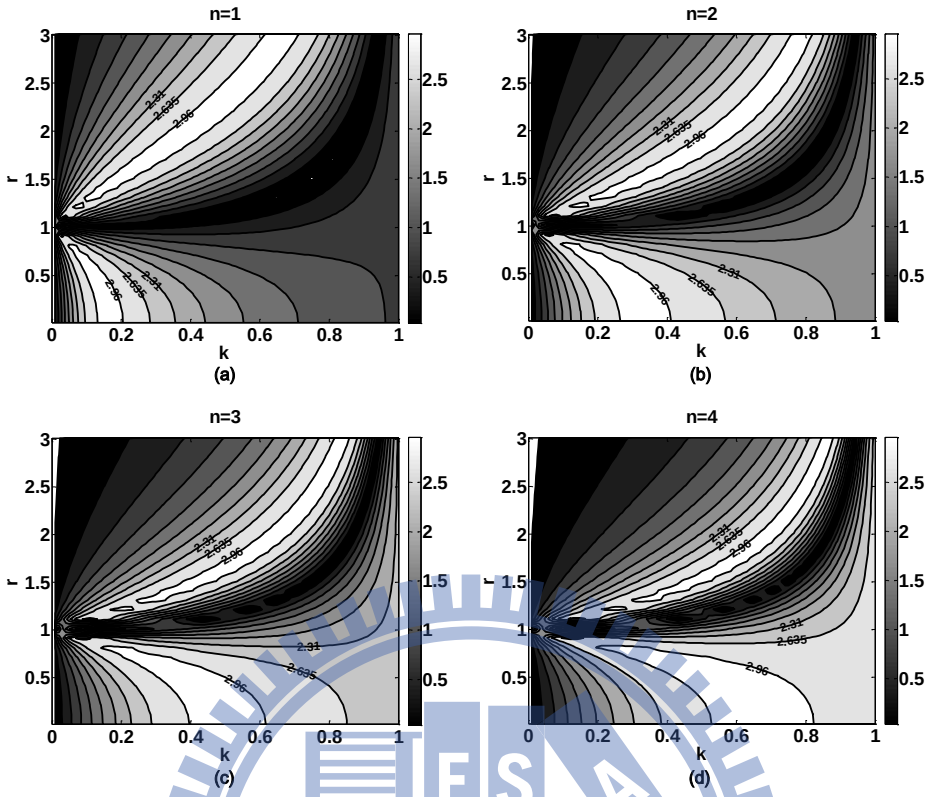

Fig. 3.9 Current gain contour plots mapping *k* and *r* (a) n=1(b) n=2(c) n=3(d) n=4

Here, *n* is chosen as 3. In Fig. 3.9 (c), the current gain degrades very little when *k* ranges from 0.4 to 0.6. The designed transformer is as shown in Fig. 3.10, in which W_1 = 8 μm, W_2 = 10 μm, OD = 400 μm. Table 3.1 shows each parameter of the RCN.

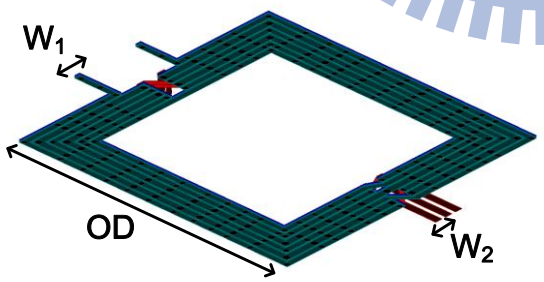

Fig. 3.10 Designed transformer

Table 3.1 The RCN realization

L_1	11.53 nH
L_2	1.79 nH
C_1	0.35 pF
C_2	3.3 pF
n	2.54
k	0.55

Because the designed RCN needs bigger capacitances C_1 and C_2 which are bigger than the total capacitance of the parasitic capacitances of the LNA and primary coils of the transformer and the parasitic capacitance of the secondary coils of the transformer and the mixers. Therefore, there are two additional capacitors $C_{1'}$ and $C_{2'}$

putted between the LNA and the transformer and between the transformer and the mixers in order to compensate the parasitic capacitances to realize the needed C_1 and C_2, as shown in Fig. 3.11.

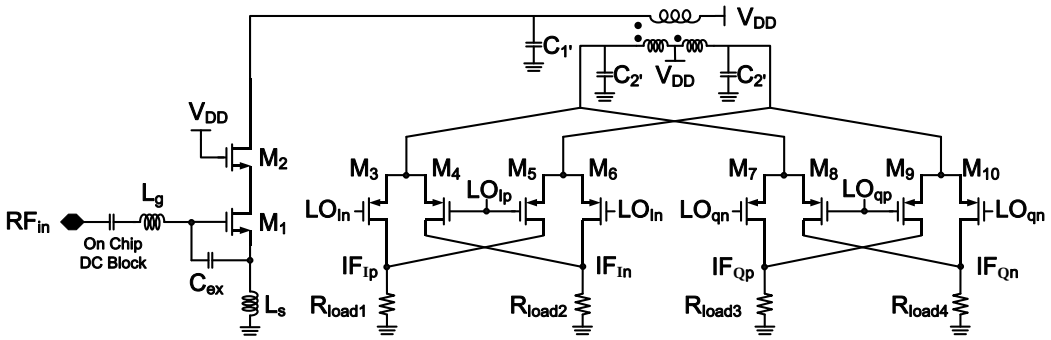

Fig. 3.11 Receiver schematic with C_1 and C_2

3.5 Summary of the Receiver

The low-power 1.4-GHz receiver can be realized by following the design procedure in Section 3.1, 3.2, and 3.3. Moreover, there is a micro control unit (MCU) in each wireless sensor node which would switch all active circuits ON/OFF by digital signal Vc, as shown in Fig. 3.12. This power switch function can save more power consumption by tuning active circuits OFF when they are not needed. Therefore, there are power switches in the bias circuits of all active circuits which can switch the active circuits by changing the bias, as shown in Fig. 3.12.

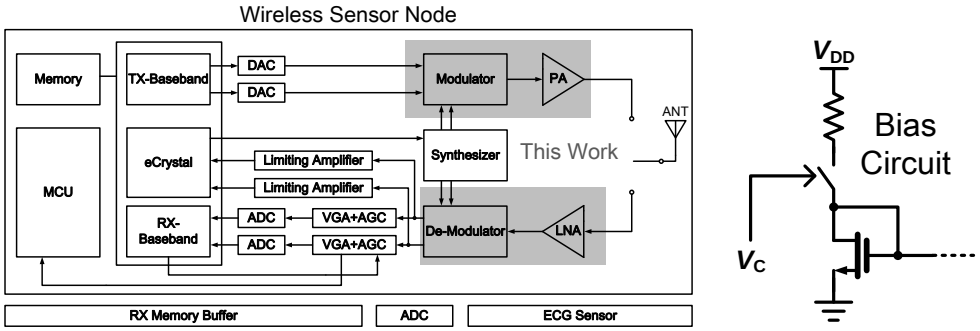

Fig. 3.12 Wireless sensor node and the power switch in the bias circuit

After the mixers, there are source follower output buffers, as shown in Fig. 3.13. The output buffers are for the output 50-Ω impedance matching under measurement consideration. The gain of the output buffer is about 8.4 dB in simulation when the loads are 50-Ω resistors.

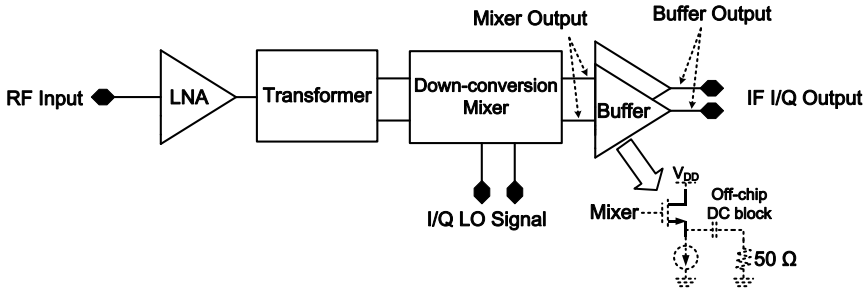

Fig. 3.13 Output buffer of the receiver

The receiver can achieve the simulated performance of 27.7 dB conversion gain before buffer, 19.3 dB conversion gain after buffer, -21 dBm P_{1dB}, -13 dBm IIP_3, and 3.1 dB noise figure, as shown in Fig. 3.14 and Fig. 3.15. The DC power consumption of the whole receiver is 6 mW. Table 3.2 makes the summary of all simulated performance and the specifications of the receiver.

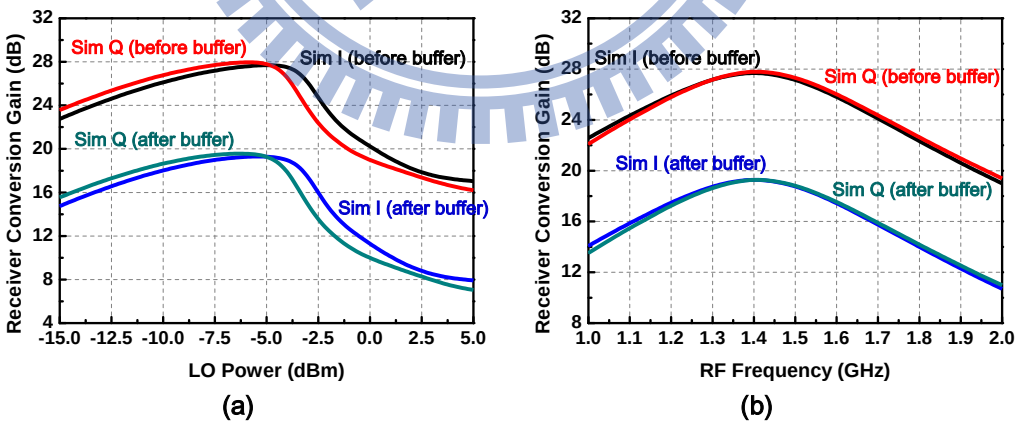

Fig. 3.14 Simulated receiver performance (a) Gain versus LO power (b) Frequency response

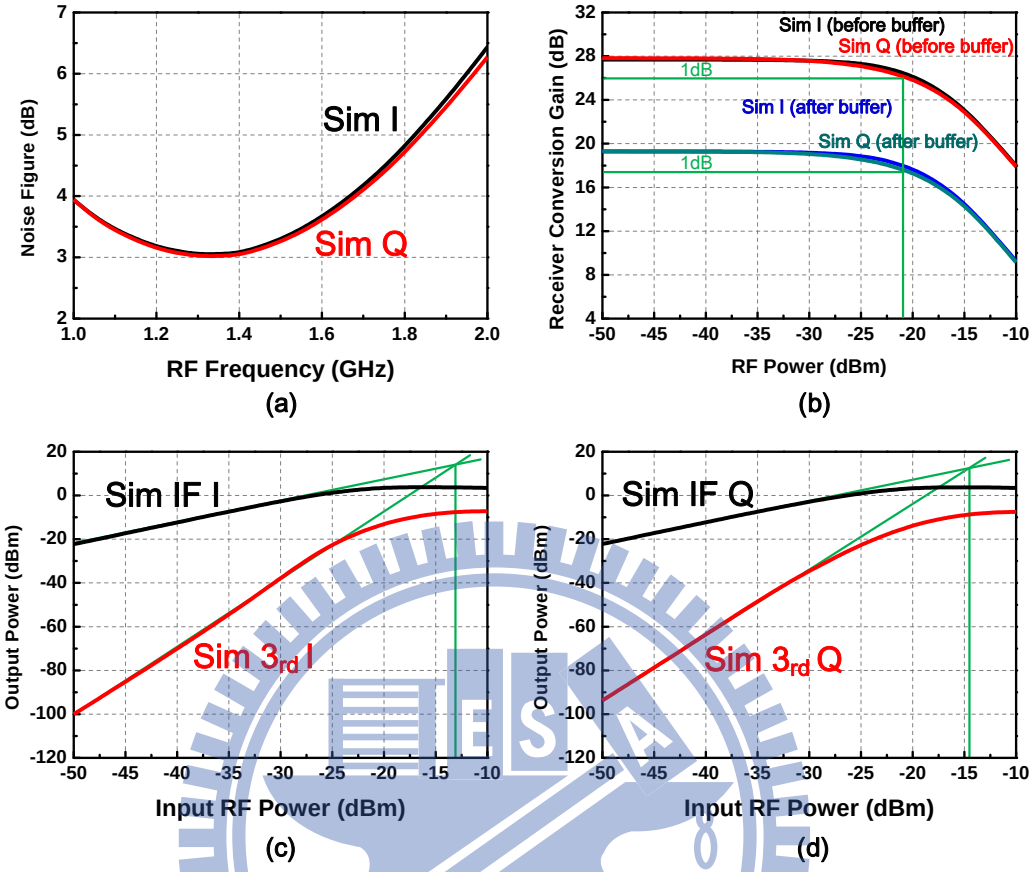

Fig. 3.15 Simulated receiver performance (a) Noise figure (b) P_{1dB} (c) IIP3 of I

Table 3.2 Summary of the simulated receiver performance

	Path I	Path Q	Specification
Conversion Gain	27.7 dB	27.8 dB	20 dB
P_{1dB}	-21 dBm	-23 dBm	-25 dBm
IIP_3	-13 dBm	-14.5 dBm	N/A
Noise Figure	3.1 dB	3.1 dB	7 dB
Power Consumption	Total power consumption = 6 mW		6 mW

Chapter 4 Transmitter Circuit Design

4.1 Structure of the Low-Power 1.4-GHz Transmitter

The designed structure of the 1.4-GHz low-power direct-conversion transmitter is showed in Fig. 4.1, which is composed of a passive CMOS up-conversion mixer, an inverter-based pre-amplifier, and a class-A power amplifier (PA) with resistor feedback network.

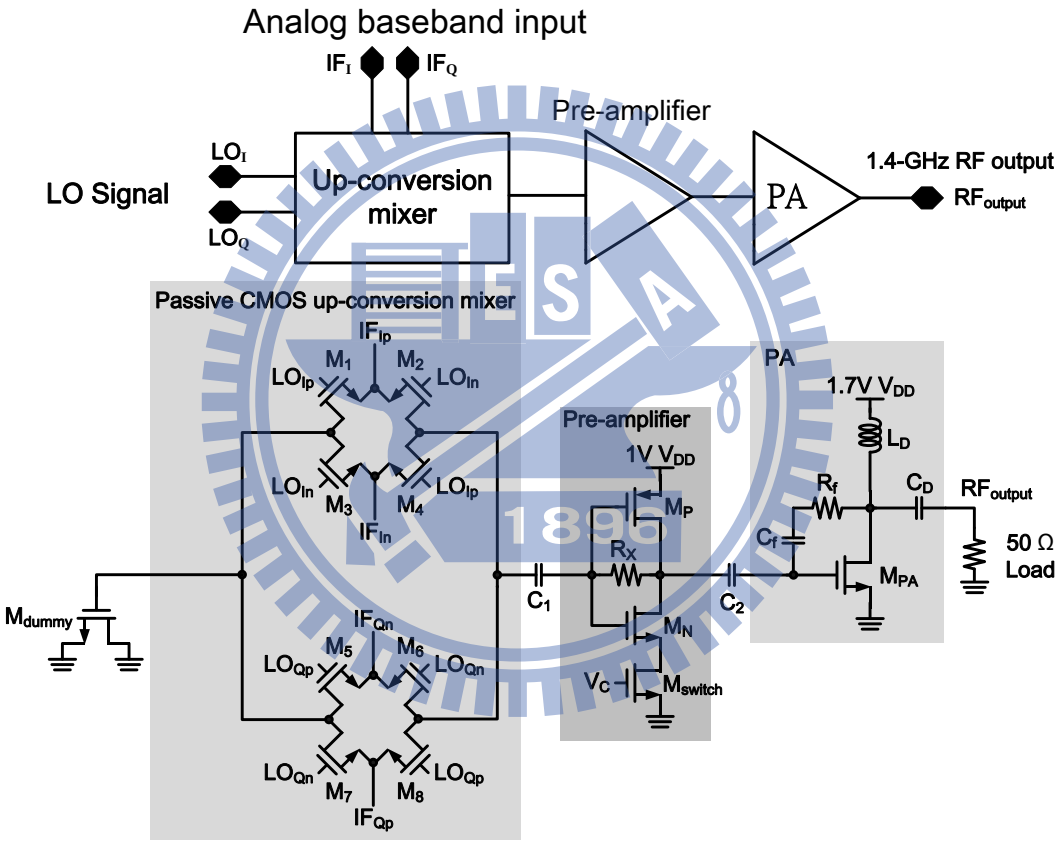

Fig. 4.1 Schematic of transmitter core circuit

The passive CMOS up-conversion mixer transfers the analog baseband signal to 1.4-GHz RF signal without DC power consumption. The dummy transistor M_{dummy} is used to make mixer operate more symmetrically. The inverter-based pre-amplifier amplifies the RF voltage signal and provides sufficient voltage signal swing to PA. The class-A power amplifier with resistor feedback network provides

the RF signal with power gain and outputs it to a 50-Ω load. The on-chip inductance L_D is used as a RF choke, C_D completes output power matching of the PA, and R_f and C_f form a feedback network for stability consideration. C_1 and C_2 are on chip DC blocks.

4.2 Up-conversion Mixer Design

The first stage of the low-power 1.4-GHz transmitter is a passive CMOS up-conversion mixer. The passive mixer is composed of eight transistors $M_{1\sim8}$, as shown in Fig. 4.1. This mixer modulates the QPSK analog baseband signal to 1.4-GHz RF signal, and suppresses the LO leakage. In order to reduce DC power consumption of the transmitter and put more budget of power consumption into the PA stage for achieving higher signal output power, the passive mixer is employed. In the implementation, CMOS technology is chosen to realize the passive mixer, because of its good switching property [16]. The nMOS transistor is used to realize the passive CMOS mixer, because that nMOS transistor has better switching performance due to the higher mobility of electrons than holes. The up-conversion mixer is composed of two double balance mixers, as shown in Fig. 4.3, so this mixer naturally has the advantages of double balance mixer. The double balance mixers provides good LO leakage suppression, because the good port-to-port isolation.

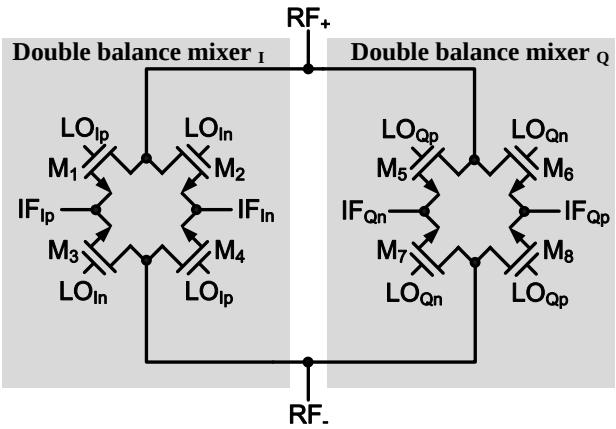

Fig. 4.2 Passive CMOS mixer

In this transmitter, there is no differential-to-single-end circuit between the mixer and the pre-amplifier for saving power consumption. One path of the mixer differential output is connected to the pre-amplifier, and the other one path is terminal to the dummy transistor M_{dummy}. The transistor size of M_{dummy} is designed to create the similar impedance looking into the pre-amplifier in order to balance the differential output load of the mixer. The mixer operates more symmetrically, the better LO leakage and RF image rejections would be obtained.

The conversion gain and linearity are two critical points which should be considered in the mixer design. Fig. 4.3 shows that the conversion gain of the passive mixer is higher when the bigger switching size is used, but its linearity is worse in the same case. Therefore, there is a trade-off between conversion gain and linearity in the mixer design. The size of the passive CMOS mixer is chosen as 16μm/0.09μm in consideration of both conversion gain and linearity. This mixer achieves the performances of conversion gain A_{mixer} = -6.5 dB, and linearity IP_{1dB} = 0 dBm.

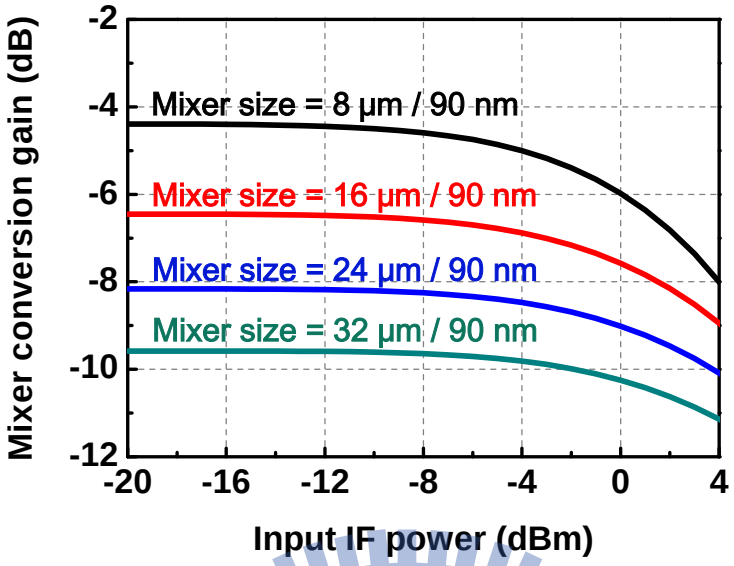

Fig. 4.3 Conversion gain of the passive CMOS SSB mixer

4.3 Power Amplifier

The output stage of the low-power 1.4-GHz transmitter is a class-A power amplifier (PA) with resistor feedback network. The PA is composed of M_{PA}, L_D, C_D, R_f, and C_f, as shown in Fig. 4.1. The on chip inductance L_D is used as a RF choke, C_D completes output power matching of the PA, and R_f and C_f form a feedback network for stability consideration. The peak transmit power of the transmitter is 4 dBm, so a high linear PA is needed here. In this transmitter design, a class-A amplifier is employed in the PA stage due to the advantage of high linearity [7], which is critical for this work. The power consumption and the efficiency are other two specifications the transmitter must meet. The maximal total power consumption of the transmitter is 25 mW, and the efficiencyη which is defined in eq. (4.1) of the transmitter must be higher than 10%.

$$\eta = \frac{\text{Signal power delivered to the 50 Ω load}}{\text{Total DC power consumption of transmitter}} \quad (4.1)$$

The class-A amplifier is biased in the condition of that the transistor is always

ON and it always conducts the quiescent current. The signal conduction angle of class-A amplifier is 360°, as shown in Fig. 4.4.

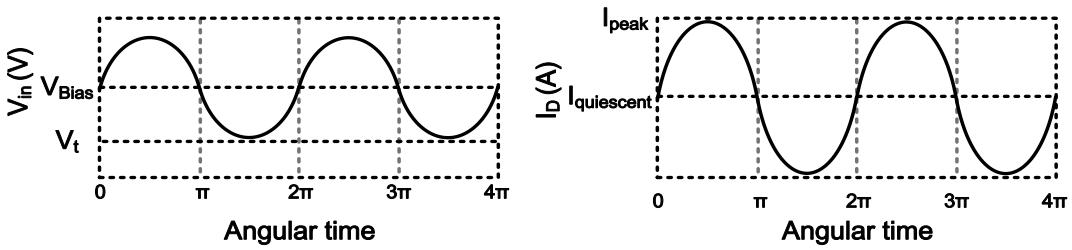

Fig. 4.4 Signal conduction angle of class-A amplifier

There are two types of RF transistors in UMC CMOS 90-nm technology, which are 1-V RF MOS and 2.5-V RF MOS. Under the same current bias condition, 1-V RF MOS has higher transconductance than 2.5-V RF MOS has, but 2.5-V RF MOS has higher linearity than 1-V RF MOS has. For the linearity consideration, the 2.5-V RF nMOS is employed to realize the PA stage. Fig. 4.5 (A) and (B) show the I-V curve of the 2.5-V RF nMOS .

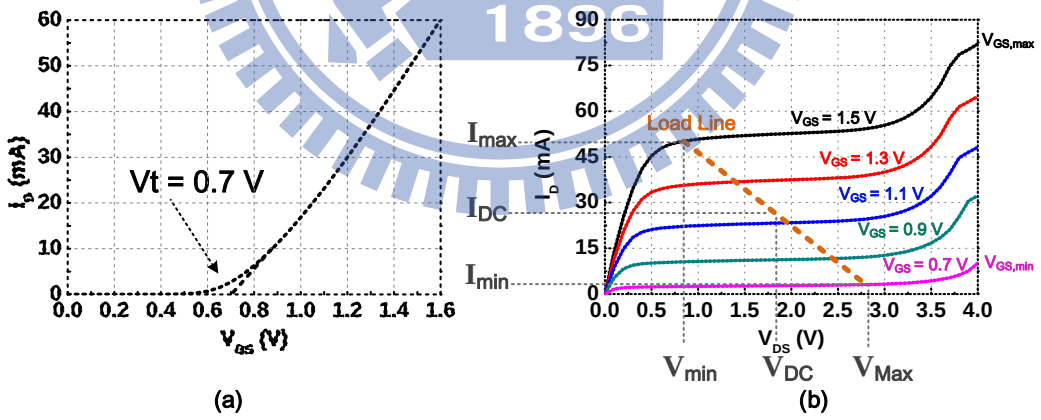

Fig. 4.5 I-V curve of 2.5-V RF nMOS (A) I_D versus V_{GS}, and (B) I_D versus V_{DS}

Fig. 4.5 (a) shows I_D-V_{GS} curve of the 2.5-V RF nMOS. In the real design environment, there is no specific corner point of the threshold voltage V_t in the I_D-V_{GS} curves. Here we define that the corner point is located at the cross point of the extended tangent lines of the pinch-off region and the saturation region. V_t can

be figured out by the above definition, and its value is 0.7 V. Therefore, the gate voltage bias V_{Bias} of the class-A PA must be higher than 0.7 V for the 360° signal conduction angle. Fig. 4.5 (b) shows the I_D-V_{DS} curve of the 2.5-V RF nMOS, and the load line analysis. A linear amplifier always operates in the saturation region which is between the triode region and the breakdown region. In the load line analysis, V_{min}, which is defined as $V_{min} = V_{GS} - V_t$, is the lowest output voltage. The corresponding current of V_{min} is the maximum output current I_{max}. The breakdown voltage of the 2.5-V RF MOS is very high when V_{GS} is low. I_D increases very slowly as V_{GS} = 0.7 V, as shown in Fig. 4.5 (b), so the transistor breakdown is not the limitation of linearity. Here we define that V_{max} is the V_{DS} with 1 dB increasing of I_D in the saturation region as $V_{GS} = V_t = 0.7$ V, its value is equal to 2.8 V. The corresponding current of V_{max} is the minimum output current I_{min}. From the above definition, the maximum output power of the trasistor can be expressed as

$$P_{out} = I_{rms} \times V_{rms} = \frac{I_{max} - I_{min}}{2\sqrt{2}} \times \frac{V_{max} - V_{min}}{2\sqrt{2}} = \frac{(I_{max} - I_{min})(V_{max} - V_{min})}{8} \quad (4.2)$$

By eq. (4.2), the maximum output power in different cases can be obtain. For example, the output voltage is from 0.9 V to 2.8 V as input voltage V_{in} is from 1.6 V to 0.7 V, as shown in Fig. 4.5 (b). The corresponding I_{max} and I_{min} are 57.9 mA and 3.1 mA, respectively. Therefore, the maximum output power is $\frac{(57.9\text{mA} - 3.1\text{mA})(2.8\text{V} - 1.0\text{V})}{8} = 13.0\ \text{mW} = 11.14\ \text{dBm}$. The corresponding gate voltage bias V_{Bias} is $\frac{1.6\text{V} + 0.7\text{V}}{2} = 1.15\ \text{V}$, and V_{DS} is $\frac{2.8\text{V} + 0.9\text{V}}{2} = 1.85\ \text{V}$. Under this bias condition, the DC current I_D can found out in Fig. 4.5 (a), and I_D in this case is 26.67 mA. The RF choke used in the PA is a 9.5-nH inductance, and its parasitic resistor is 6 Ω. Therefore, the appropriate V_{DD} is $V_{DD} = V_{DS} + I_D \times 5\Omega = 1.85\text{V} + 26.67\text{mA} \times 6\Omega = 2.01\ \text{V}$. The DC power consumption is $P_{DC} = I_D \times V_{DD} =$

$26.67\text{mA} \times 2.01\text{V} = 53.6\text{ mW}$. The efficiency of the PA is $\eta = \frac{P_{out}}{P_{DC}} = \frac{13.0\text{ mW}}{53.6\text{ mW}} =$ 24.3%. Fig. 4.6 (a) and (b) make the summaries of the maximum output power, the DC power consumption, the power gain, the efficiency of the PA as V_{Bias} is from 0.75 V to 1.15 V.

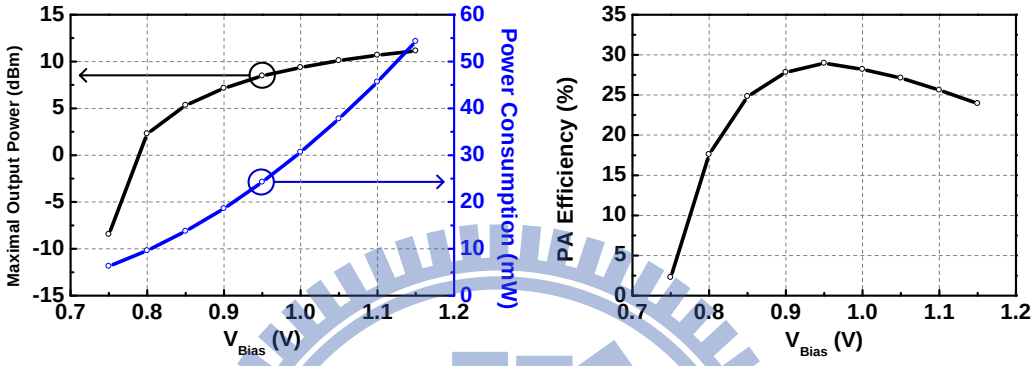

Fig. 4.6 (a) Maximum output power and power consumption versus V_{Bias} (b) Gain and efficiency versus V_{Bias}

Fig. 4.6 (a) and (b) show that the maximum output power is higher with higher DC power consumption. However, the maximum output power is not proportional to the DC power consumption. With V_{Bias} increasing, the growth rate of power consumption increases, but the growth rate of the maximum output power decreases. Therefore, there is a V_{Bias} of the highest efficiency can be obtained, as shown in Fig. 4.6 (b). The V_{Bias} of the highest efficiency is 0.95 V and the efficiency changes slowly as V_{Bias} is from 0.9 V to 1.0 V. The corresponding V_{DD} of the V_{Bias} in this range is from 1.67 V to 1.8 V, and the same bias condition of high efficiency would be obtained in the different transistor sizes. In this work, the V_{Bias} is chosen to be 0.92 V, the corresponding V_{DD} is 1.7, and the transistor size is 288μm/0.36μm. This PA can achieve the simulated performance of OP_{1dB} = 6 dBm and 19.2% efficiency with 20.7 mW power consumption.

Fig. 4.7 shows the output power matching by Smith chart in the simulation. S11

is the output impedance, and maker M1 marks the impedance at 1.4 GHz, which is $56.4 + j74.9\ \Omega$. S22 is the impedance looking into the matching network, and maker M2 marks the impedance at 1.4 GHz, which is $51.0 - j59.9\ \Omega$. The value of C_D is chosen to be 1.8 pF to achieve the output impedance matching.

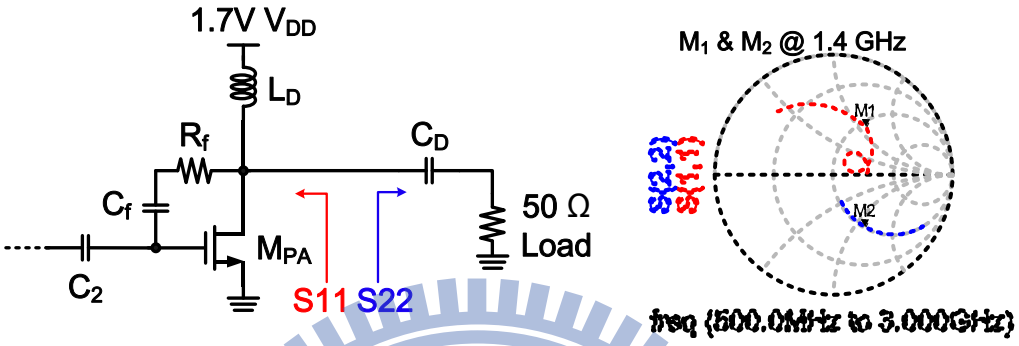

Fig. 4.7 Output power matching of the PA

R_f and C_f form a feedback network for stability consideration. Fig. 4.9 (a), (b), (c), and (d) are the stability simulation results of PA by the simulation setup in Fig. 4.8 (a) and (b). Fig. 4.9 (a) shows the source stability circle and input return loss S11 of PA without feedback network. Fig. 4.9 (c) shows the load stability circle and output return loss S22 of PA without feedback network. In Fig. 4.9, the areas inside the blue circles and outside the red circles are the areas of stable input and output impedance at each frequency. The input and output impedance of the PA should be designed in the stable impedance area. In Fig. 4.9 (a), the input impedance points are near the unstable area. In Fig. 4.9 (c), some output impedance points are in the unstable area. R_f = 2.5 kΩ and C_f = 2.7 pF are used to complete the feedback network to solve the stability issue, as shown in Fig. 4.8 (b). Fig. 4.9 (b) and (d) show the simulation results of stability of the PA with the feedback network. In Fig. 4.9 (b), the input impedance points shift a little bit away from the unstable area. In Fig. 4.9 (d), all output impedance points are in the stable impedance area.

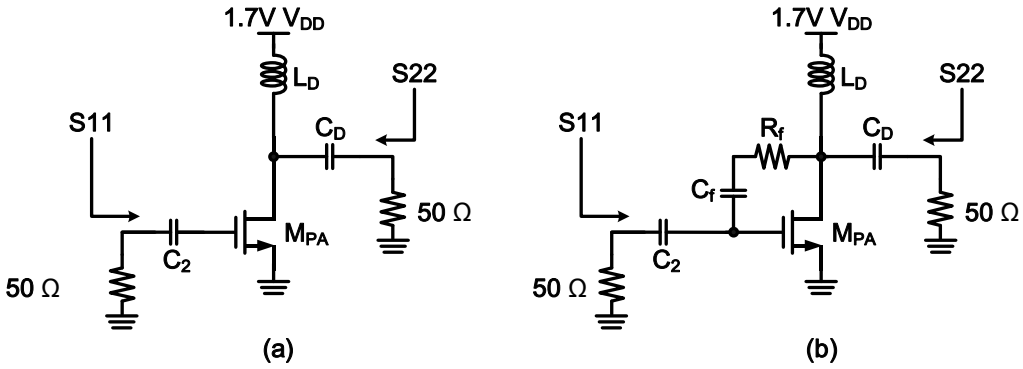

Fig. 4.8 (a) Stability simulation setup of the PA without feedback network
(b) Stability simulation setup of the PA with feedback network

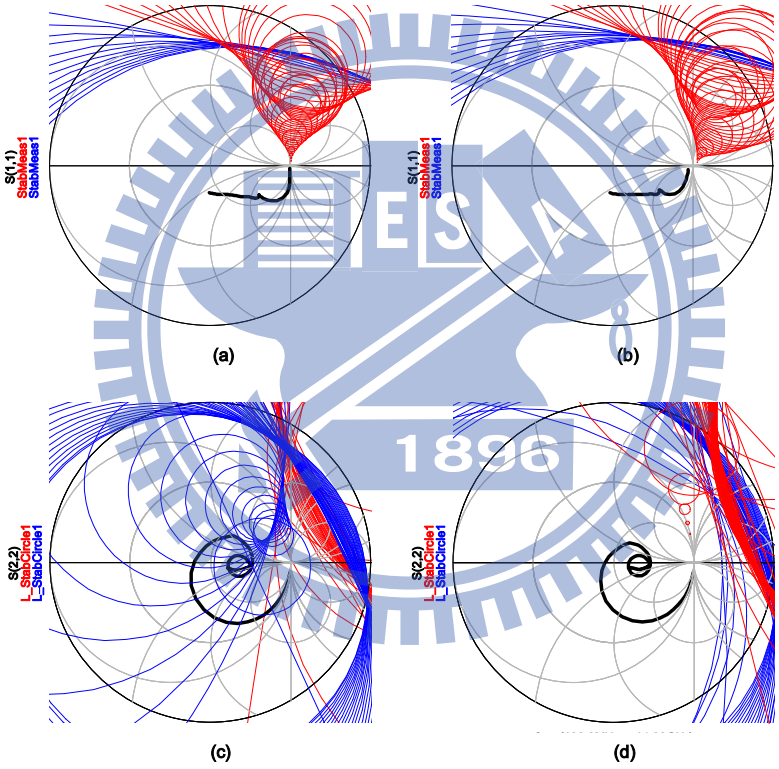

Fig. 4.9 Stability simulation results of PA

(a) Source stability circle and input impedance S11 of PA without feedback network

(b) Load stability circle and output impedance S22 of PA without feedback network

(c) Source stability circle and input impedance S11 of PA with feedback network

(d) Load stability circle and output impedance S22 of PA with feedback network

4.4 Pre-Amplifier

There is an inverter-based pre-amplifier between the up-conversion mixer and the power amplifier. The pre-amplifier is composed of a pMOS common source amplifier M_P, a nMOS common source amplifier M_N, a power switch M_{switch}, and a resistor R_X, as shown in Fig. 4.1. The pre-amplifier is used to amplify the voltage swing of the RF signal and provides sufficient signal voltage to the PA. These two common source amplifiers share one DC current path, and the pre-amplifier is self-biased with the 12.5-kΩ resistor R_X. Fig. 4.10 shows the AC signal model of the pre-amplifier.

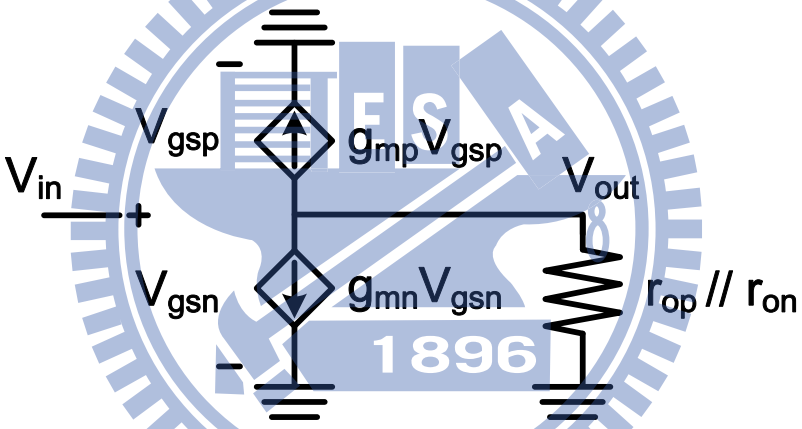

Fig. 4.10 AC signal model of the pre-amplifier

The g_{mp} and g_{mn} are the transconductance of M_p and M_n, and r_{op} and r_{on} are the output resistance of M_p and M_n. The voltage gain of the pre-amplifier is

$$A_{pre-amplifier} = (g_{mp} + g_{mn})(r_{op} + r_{on}) \quad (4.3)$$

This type of amplifier has two transconductance gains with one current path, so it can provides signal with efficient voltage gain in low power operation [5]. The DC voltages at V_{out} and V_{in} are self biased at $V_{DD}/2$ for maximum voltage swing. The mobility ratio of the 1-V RF pMOS to 1-V RF nMOS in UMC 90-nm is about 1:2. Therefore, the transistor size ratio of $(\frac{W}{L})_p/(\frac{W}{L})_n$ is chosen as 2/1 to

bias the DC voltages at V_{out} and V_{in} to $V_{DD}/2$. The input voltage swing of the PA is 0.26 V as its output power reach OP_{1dB}. Therefore, the pre-amplifier must has efficient voltage gain to provide sufficient voltage to the PA. The power consumption budget of the whole transmitter is 25 mW and the PA consumes 20.7 mW, so the leaved remained power consumption budget for the pre-amplifier is 4.3 mW. Fig. 4.11 shows the voltage gain and the power consumption of the pre-amplifier versus the transistor size of M_n with $(\frac{W}{L})_p/(\frac{W}{L})_n$=2/1. Both L_p and L_n always keep the smallest size of 90 nm for maximal voltage gain.

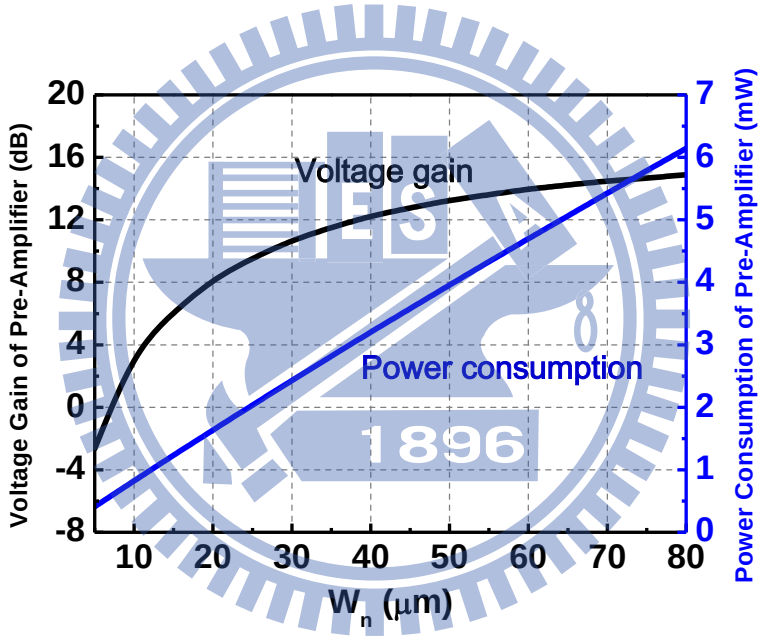

Fig. 4.11 Voltage gain and the power consumption of the pre-amplifier versus the transistor size of M_n on the condition of $(\frac{W}{L})_p/(\frac{W}{L})_n$=2/1

In this work, the transistor sizes of the pre-amplifier are $(\frac{W}{L})_n = \frac{48\mu m}{90nm}$ and $(\frac{W}{L})_p = \frac{100\mu m}{90nm}$ for optimal voltage self bias at $V_{DD}/2$. This pre-amplifier achieves the performances of voltage gain $A_{pre-amp} = 13.6$ dB with 3.9 mW DC power consumption. The transistor M_{switch} is a DC power switch to control ON/OFF for saving the power consumption.

4.5 Summary of the Transmitter

Like the receiver, there are also power switches in the transmitter for saving power consumption. The PA power switch is in the bias circuit of PA, as shown in Fig. 4.12 (a). The pre-amplifier power switch is in the pre-amplifier core circuit because of the self-bias architecture, as shown in Fig. 4.12 (b).

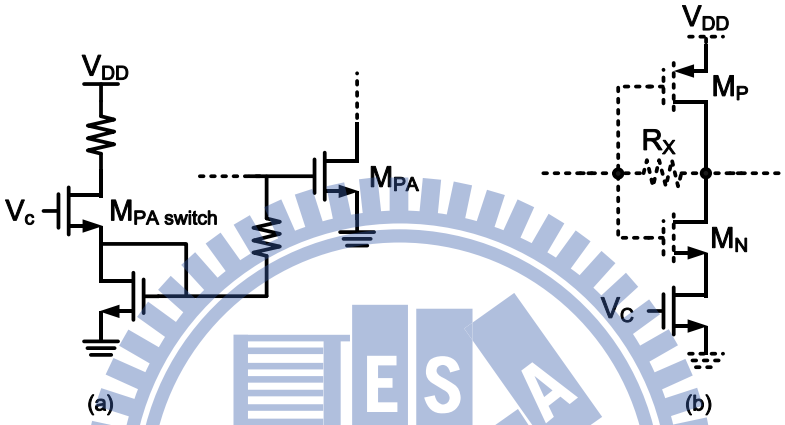

Fig. 4.12 (a) PA power switch (b) Pre-amplifier power switch

The designed transmitter is achieve the simulated performances of 12.4 dB conversion power gain, 6 dBm OP_{1dB}, 37 dB LO leakage rejection, and 27.5 dB RF image rejection, as shown in Fig. 4.13. Table 4.1 makes the summary of these performances of the designed transmitter.

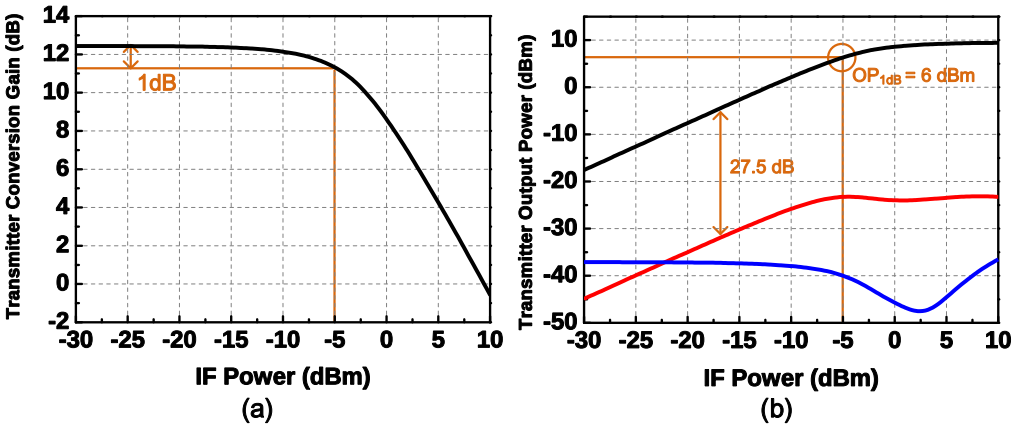

Fig. 4.13 Simulated transmitter performance (a) Conversion gain (b) Output power

Table 4.1 Summary of the simulated transmitter performance

	This Work	Specification
Conversion Power Gain	12.4 dB	N/A
OP_{1dB}	6 dBm	4 dBm
Efficiency	16.4%	10%
Power Consumption	24.3 mW	25 mW

Chapter 5

Chip Implementation and Measurements

5.1 Chip Implementation

This transceiver is fabricated by the UMC 90-nm CMOS low-power process. The top metal layer M9 of this process is comparatively thinner than the top metals of the normal RF process. In the RF integrated circuits implementation, the inductances are realized on the top metal layer because it's the thickest metal layer in all metal layers. The inductance of thinner metal layer has larger parasitic resistor, and this resistor would reduce the quality factor Q of the inductances. In this work, the inductance L_g are implemented in 3 metal of top metal M9, M8, and M7, and connected together by the contacts to form a thicker inductance, as shown in Fig. 5.1.

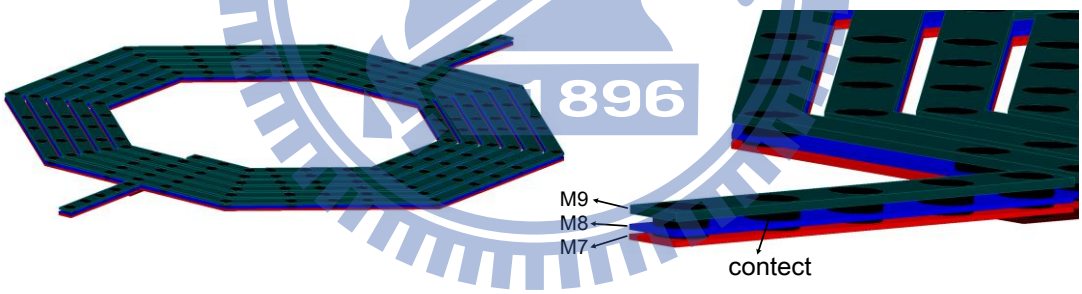

Fig. 5.1Inductance implemented in 3 metal layers

The L_g of 3 metal layers has higher Q value than the L_g of 1 or 2 metal layers has. The inductance with higher Q value would restrain the noise figure of the receiver, as shown in Fig. 5.2. Moreover, the RF choke inductance L_D of the PA is also implemented by 3 metal layers for higher Q value. The transformer is analyzed without loss like an ideal transformer. Therefore, both the primary and secondary coils of the transformer are realized by two metal layers in order to reduce the parasitic resistor.

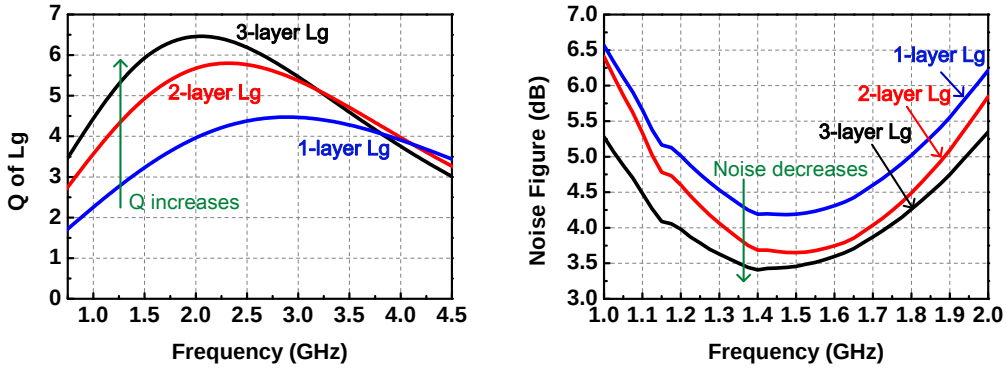

Fig. 5.2 (a) Q factor of the inductances of 1, 2, and 3 metal layers (b) Noise figure of the receiver with the inductances of 1, 2, and 3 metal layers

The whole transceiver is implemented on a single chip by the UMC 90-nm CMOS technology, as shown in Fig. 5.3. The chip size is 1360μm × 1210μm. The DC, RF signal, LO signal and IF signal are all inputted to the chip through wire bonding.

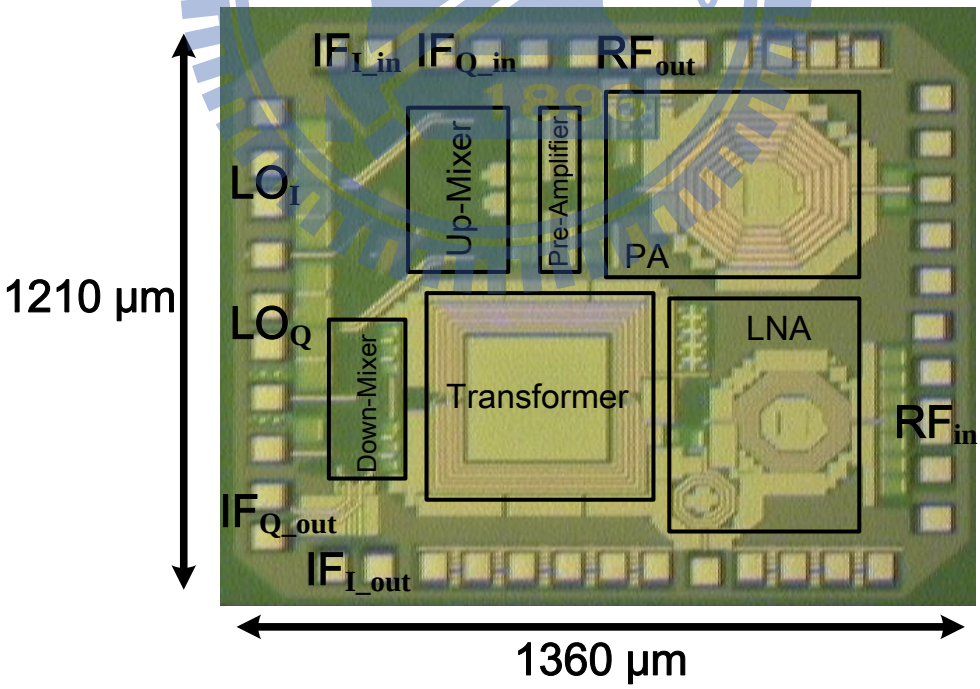

Fig. 5.3 Chip photo of the low-power 1.4-GHz transceiver

5.2 Chip Measurement

The transceiver is measured by the way of chip on board. The measurement setups of the receiver for conversion gain, IIP3 by two tone test, and noise figure are shown in Fig. 5.4(a), (b), and (c), respectively.

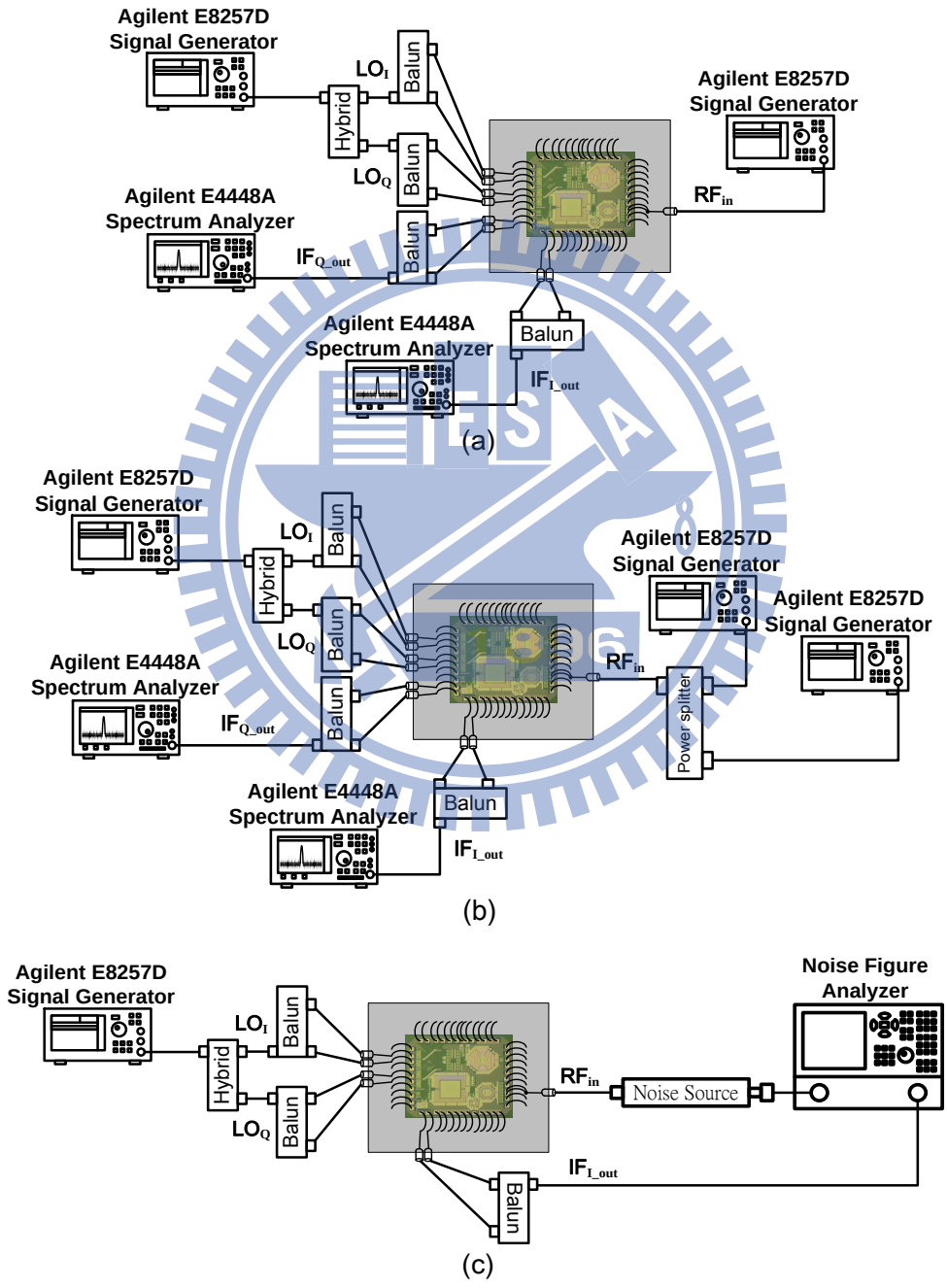

Fig. 5.4Measurement setups of the receiver for (a) Conversion gain (b) IIP3 by tone test (c) Noise figure

Because there are some problems in the tape out procedure, the digital pads of power switching don't work. In order to solve this problem, we use laser to burning some nodes of the transceiver to short these nodes and V_{DD}, as shown in Fig. 5.5. Using laser burning we successfully turn on the receiver, but there is no appropriate node of pre-amplifier for laser burning to turn it. Consequently, we can turn ON the receiver and measure it on the non optimal bias, and we measure the transmitter on the unable condition.

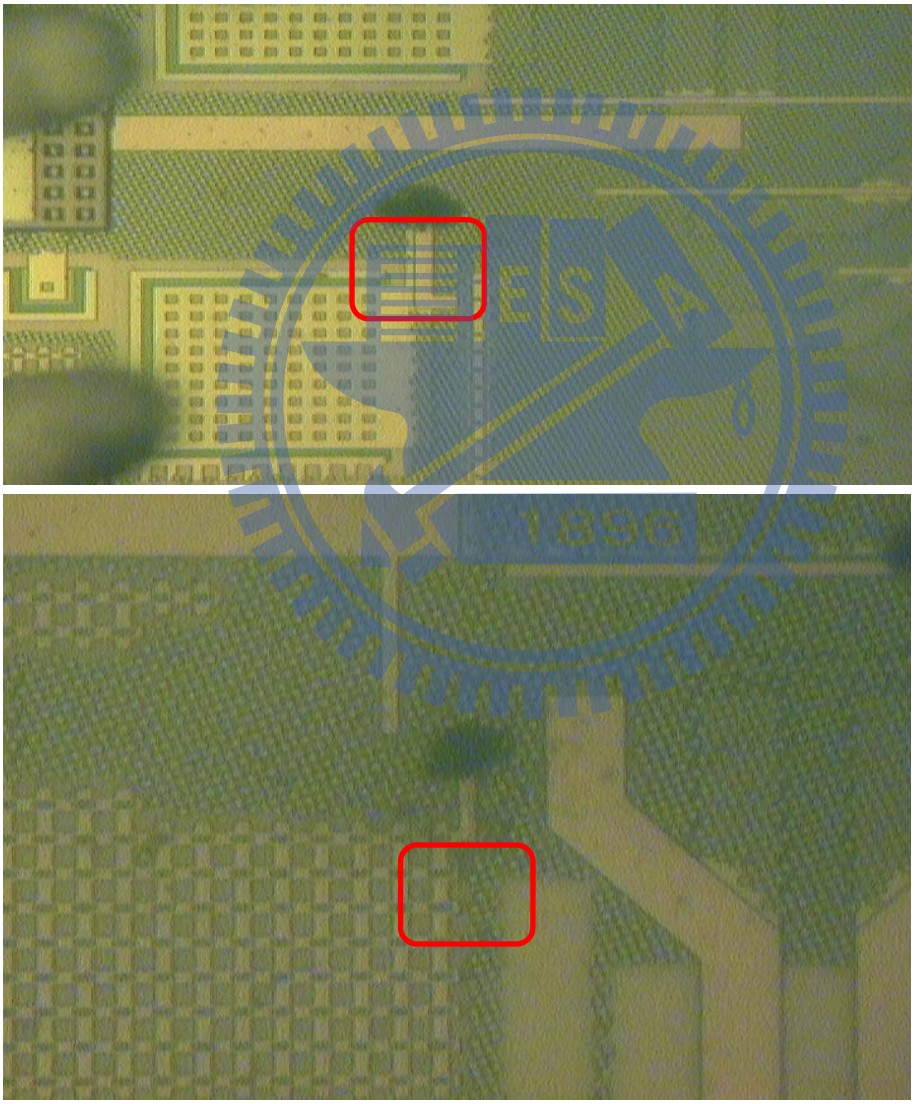

Fig. 5.5 Laser burning

The receiver frequency response measurement results shows that the additional capacitor $C_{1'}$ is a little bigger than the appropriate capacitance. It

causes the peak of the frequency response shift from 1.4 GHz to lower frequency, as shown in Fig. 5.7. Therefore, we used the laser cut to cut out $C_{1'}$ and used only the parasitic capacitances of the LNA and the primary coils of the transformer to form the C_1 of the RCN, as shown in Fig. 5.6. Finally, we made the peak of the frequency shift back the higher frequency, as shown in Fig. 5.7.

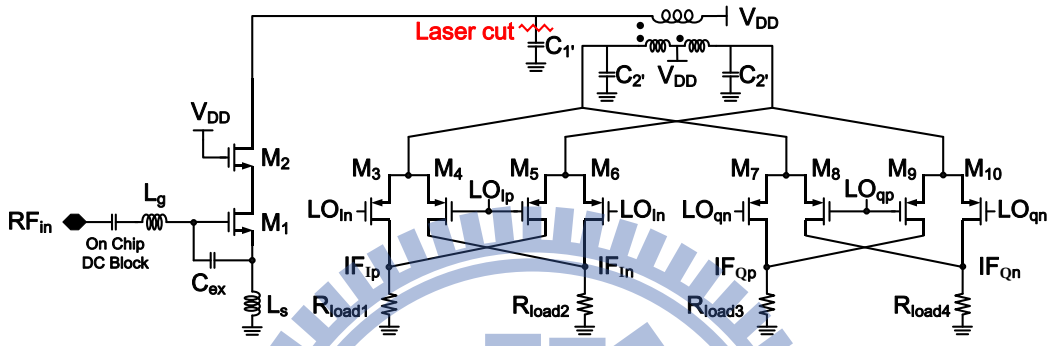

Fig. 5.6 The laser cut of $C_{1'}$

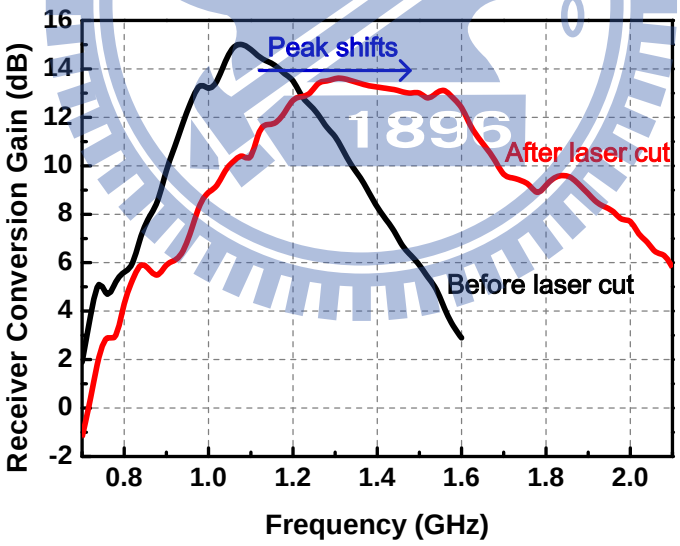

Fig. 5.7 Peak shifts due to the laser cut of $C_{1'}$

The receiver measurement results of conversion gain versus LO power, frequency response, noise figure, P_{1dB}, IIP3_I, and IIP3_Q are shown in Fig. 5.5(a), (b), (c), (d), (e), and (f), respectively.

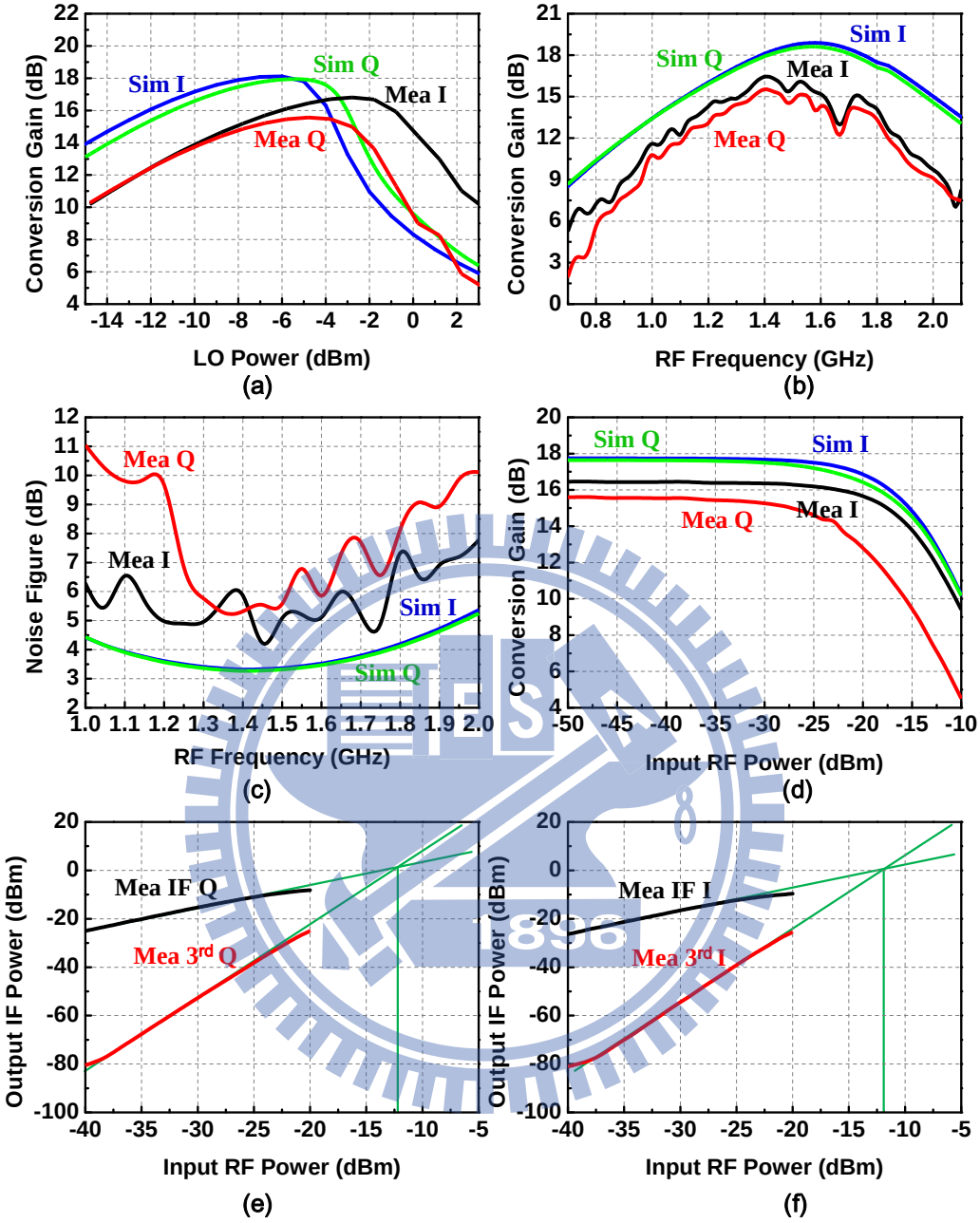

Fig. 5.8 Measurement results of (a) Conversion gain versus LO power, (b) Frequency response, (c) Noise Figure, (d) P_{1dB}, (e) IIP3_I, and (f) IIP3_Q

The conversion gains of the receiver in Fig. 5.5 (a), (b), and (c) are measured after the output buffer with 7 dB buffer loss. Both in the simulations and the measurements of frequency response, noise figure, P_{1dB}, and IIP3, the LO power is chosen as -5 dBm for the maximal conversion gain in Q path and smaller gain mismatch consideration.

Fig. 5.5 (a) shows the conversion gain of the receiver versus LO power as RF frequency is 1.4 GHz. The simulated LO power of the maximal conversion gain of I path is -6 dBm, and of Q path is -5 dBm. The measured LO power of the maximal conversion gain of I path is -3 dBm, and of Q path is -5 dBm. The measurement results prove that the conversion gain of the receiver using the RCN technique has a peak at low LO power. Compared to the normal receivers, the designed receiver only needs comparative low LO power to achieve high conversion gain. The low LO power characteristic of the receiver is very suitable for the low power application.

Fig. 5.5 (b) shows the frequency response of the receiver. The simulated maximal conversion gains of I path and Q path are both at 1.58 GHz. The measured maximal conversion gains of I path and Q path are both at 1.4 GHz. The peak of the conversion gain is at the designed resonant frequency ω_L. The measurement results approve that the receiver using the RCN technique can get high conversion gain at low power operation as long as the operation frequency ω_0 is designed at one of the resonant frequencies of the RCN ω_L and ω_H.

Fig. 5.5 (c) shows the noise figure of the receiver. The simulated noise figures at 1.4-GHz RF frequency of I path and Q path are both 3.32 dB. The measured noise figure at 1.4-GHz RF frequency of I path is 5.86 dB, and of Q path is 5.32 dB. The noise figures of I path and Q path are both meet the specification of noise figure less than 7 dB.

Fig. 5.5 (d), (e), and (f) show the linearity measurement results. The P_{1dB} of I path is -19 dBm, and of Q path is -24 dBm. The IIP3 of I path is -11 dBm, and of Q path is -13 dBm. The linearity of the receiver also meets the specifications.

Table 5.1 makes the summary of the measured receiver performance.

Table 5.1 Summary of the measured receiver performance

	Measured performances	Specification
Conversion Gain	I: 16.44 dB, Q: 15.53 dB *	20 dB
Noise Figure	I: 5.86 dB, Q: 5.32 dB	7 dB
DC Power Consumption	6 mW	6 mW
P_{1dB}	I: -19 dB, Q: -24 dB	-25 dBm

*The conversion gain is measured after output buffer with 7.6 dB buffer loss.

The measurement setup of the transmitter is shown in the Fig. 5.6.

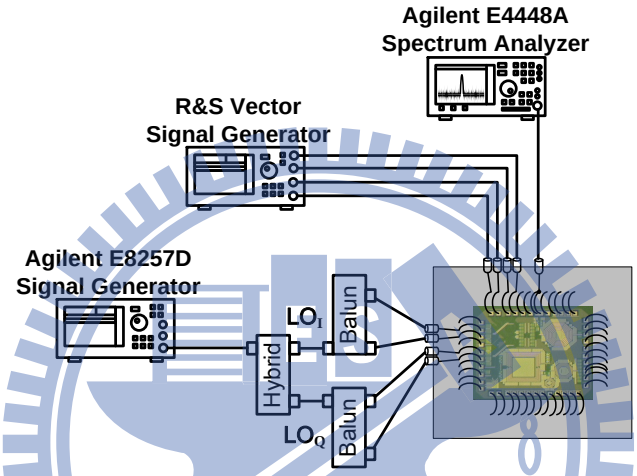

Fig. 5.9 Measurement setup of the transmitter

The measurement results of the transmitter are shown in Fig 5.7.

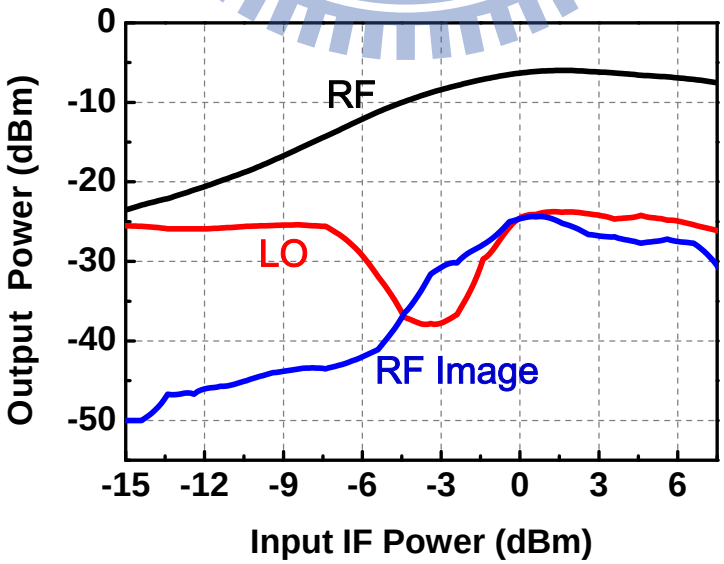

Fig. 5.10 Measurement results of the transmitter

The switch of the pea-amplifier M_{switch} can't be turned ON. Under this condition, the pre-amplifier doesn't work and can't provide the RF signal voltage gain. Consequently, the input signal of the PA is too small the output power of the transmitter is also on the low power level. Even though the transmitter doesn't entirely work, the LO leakage rejection of the transmitter still can be observed in the measurement results. From the measurement results the LO-RF leakage is -25 dB. Table 5.2 males the summary of the measured transmitter performance

Table 5.2 Summary of the measured transmitter performance

	Measured performances	Specification
Peak transmitter power	-6 dBm	4 dBm
Average transmitter power	-13 dBm	-3 dBm
Power consumption	22 mW	25 mW
Efficiency	1.2%	10%

5.3 Summary of the Measurement Results

Table 5.3 is the performances comparison table. The voltage conversion gain with 7.6 dB buffer loss of this 1.4-GHz receiver is 16.44 dB is close to the gain of [12]. The power consumption and the linearity of this receiver are at the same order of other three works. The noise figure is the best among these works.

The linearity and the LO leakage of this 1.4-GHz transmitter are at the same order of other three works. The power consumption of this transmitter is the critical part we must improve.

Table 5.3 Comparison table

	[10]	[11]	[12]	This Work
Frequency	2.4 GHz	2.4 GHz	2.4 GHz	1.4 GHz
Technology	0.18 μm CMOS	0.18 μm CMOS	0.35 μm BiCMOS	90 nm CMOS
RX Structure	Direct conversion	Direct conversion	Direct conversion	Direct conversion
P_{DC}	5.3 mW	6.3 mW	8.6 mW	6 mW
Gain	>10 dB	30 dB	26 dB	16.44 dB * (Mea) 27.7 dB (Sim)
IIP3	N/A	-8 dB	-13 dB	-11 dBm (Mea) -13 dBm (Sim)
Noise Figure	<8 dB	7.3 dB	8.7 dB	5.86 dB (Mea) 3.1 dB (Sim)
TX structure	Direct conversion	Direct conversion	Direct conversion	Direct conversion
P_{DC}	6.11 mW	5.4 mW	16 mW	25 mW
P_{out} (OP_{1dB})	-10 dBm	0 dBm	6 dBm	-6 dBm (Mea) 6 dBm (Sim)
LO leakage	N/A	-30 dB	N/A	25 dB (Mea) 37 dB (Sim)

*Including 8.4 dB buffer loss

Chapter 6 Conclusion and Future Work

6.1 Conclusion

In this work, we fabricated a low-power 1.4-GHz transceiver for wireless sensor work on a single chip by UMC 90-nm CMOS technology.

Our analysis of the RCN provides an efficient way to design an optimal transformer. The resonator coupling network with 2-metal-layer transformer provides the receiver high transfer current gain in the low power operation. The 3-metal-layer on chip inductance L_g really complete the input 50-Ω matching and noise matching of the receiver. The noise figure of this receiver is comparative lower in the low power operation. The needed LO power of this receiver with the RCN is lower than the LO power of other common receivers. The low LO power characteristic can reduce the loading of VCO, reduce the VCO power consumption, and further achieve the target of low power consumption.

The problems of the digital pads cause the transmitter unable to work regularly. However, based on the simulation results, we know that the low power target could be achieved by this transmitter architecture.

The measured results of the receiver and simulated results of the transmitter all meet the specifications which are based on the 1.4-GHz band in Wireless Medical Telemetry Service.

The whole chip size of the RF transceiver is only 1210μm*1360μm. The small chip size endues the transceiver with low cost advantage.

6.2 Future Work

Nowadays, the low-power application is becoming more and more important application. In Table 5.3, the noise performance is better than other works. The noise figure is the most flexible part we can alter in the next design. The power consumption of the receiver can be reduced more by sacrificing some noise performance. In the transmitter, the power consumption is the critical part we must improve. Using other classes of amplifier would raise the efficiency of the PA, and further reduce the power consumption.

In the chip layout of this 1.4-GHz transceiver, the pads of LO signal and analog baseband signal are set up under the consideration of the integration of this transceiver, a 1.4-GHz frequency synthesizer, and the analog baseband circuits. This chip layout contributes convenience to the circuit integration in the future.

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