國 立 交 通 大 學

電 信 工 程 學 系 碩 士 班

碩 士 論 文

單晶片溫度感測器中的正比絕對溫度

參考電壓之設計與製作

The Design and Implementation of CMOS PTAT

References for Monolithic Temperature Sensors

研 究 生：張 智 閔

指導教授：闕 河 鳴 博士

西元二００四年七月

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研 究 生：張智閔　　Student：Chih-Ming Chang

指導教授：闕河鳴　博士　　Advisor：Dr. Herming Chiueh

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碩 士 論 文

A Thesis

Submitted to Department of Communication Engineering

College of Electrical Engineering and Computer Science

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master of Science

in

Communication Engineering

July 2004

Hsinchu, Taiwan.

西元二００四年七月

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中文摘要

這篇論文使用 0.25 微米互補式金氧半標準製程設計並實現了一個正比絕對溫度參考電壓源. 過去的研究提出將金氧半電晶體操作在弱反轉區可用來取代傳統電路中的雙極性電晶體以實現正比絕對溫度的電路．然而，這些電路在高溫時都會有非線性的現象產生, 本論文提出的電路運用了一個補償的技巧以改善其在高溫時的線性度．量測結果顯示此電路的線性工作區間可延伸到至少 155°C，此電路只需要校正因製程飄移所產生的偏移電壓．因此，製程後段所需的校正工作將可減低至最低．另外，此電路可以容易的與其他任何的數位系統整合．

The Design and Implementation of CMOS PTAT References for Monolithic Temperature Sensors

Student: Chih-Ming Chang Advisor: Dr. Herming Chiueh

Department of Communication Engineering

National Chiao Tung University

Hsinchu, Taiwan

ABSTRACT

A pure CMOS proportional-to-absolute temperature (PTAT) reference circuit has been designed and implemented in a standard 0.25-*m*m CMOS technology. Previous research has proposed the use of MOS transistors operating in the weak inversion region to replace the bipolar devices in conventional PTAT circuits. However, such solutions often have nonlinearity problem in high temperature. The proposed circuitry applied a compensation technique to enhance the linearity of high temperature behavior. The experimental results show the linear range of the voltage output has been expand to at least 155℃, which implies that the temperature sensor requires calibration only of its offset. Thus, the effort for after process calibration is minimized. The proposed circuit can be integrated to any digital systems with minimal efforts.

誌謝

本篇論文可以順利完成，首先要感謝我的指導教授闕河鳴博士．每當我在研究的過程中遇到瓶頸時，闕老師總是能適時地引導我，給予寶貴的建議並指引正確的方向．另外，老師平日培養學生獨立思考與分析問題的能力，更讓我理解到做研究時正確的態度與方法．

其次，我要由衷的感謝謹鴻、志軒、明治、書豪四位同窗與我一同努力奮鬥，並在研究與生活上給予我許多的幫助，尤其感謝書豪從大學到研究所這段期間給予我的幫助及啟發．此外，也要感謝所有關心我的朋友以及晶片系統設計實驗室的學弟、學妹們，有了各位的支持與相伴，讓我在碩士學習生涯中，能更過的更多采多姿，也讓我的研究生活增色不少．

最後，我要感謝一直支持我的父母以及四位姐姐，有你們的支持才有現在的我．

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Increases in circuit density and clock speed in modern VLSI design brought thermal issues into the spotlight of high-speed VLSI design [1]. Previous research has indicated that the thermal problem in modern integrated circuits can cause a significant performance decay [2] as well as reducing of circuitry reliability [3]-[6]. Local overheating in even one spot of high density circuits, such as CPUs and high-speed mixed-signal circuits [7], [8] can cause the whole system crashed. The reasons include clock synchronization problems, parameter mismatches or other coefficient changes due to the uneven heat-up on a single chip [2]. In order to avoid thermal damages, early detection of overheating and properly handling such event are necessary. Recent research has proposed the utilization of a thermal management system [9], [10] for large scale integrated circuits. In such design, adapting cooling and temperature monitoring mechanisms are widely used. Fig. 1.1 shows the block diagram of an on-chip thermal aware system. This thesis focuses on the design and analysis of the suitable temperature sensor in the system.

Recent research has indicated that the best candidate for a fully-integrated temperature sensor is the proportional-to-absolute temperature (PTAT) circuit [11]. The PTAT sources are usually implemented using parasitic vertical BJTs in any standard CMOS technology. These circuits require resistors which may vary from different technology. Also, the power consumption of the BJT based references is relatively high for low power applications. The PTAT generator of Vittoz and Fellrath [12] takes advantage of MOS transistors operating in subthreshold region; the power

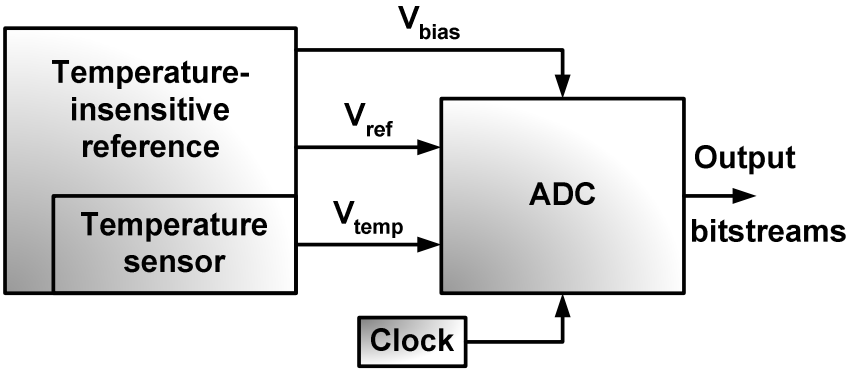


Figure 1.1 Block diagram of a thermal aware system.

consumption is made minimal due to the inherently low currents in that region. However, this circuit does not allow strong supply voltage scaling in deep-submicron technology. Serra-Graells and Huertas [13] introduced an all-MOS implementation exhibiting enough low-voltage capabilities by the use of MOS subthreshold techniques. However, this circuit has nonlinearity problem in high temperature. The nonlinearity behavior is a crucial effect to implement a complete thermal management system within a digital circuit since such circuitries require more effort and cost for after process calibration.

In this thesis, we propose a new method to improve temperature performance of the PTAT circuit for monolithic temperature sensors. This sensor is designed for the temperature range from 0°C to 150°C. The proposed PTAT circuitry has a linear temperature reading in high temperature, which requires minimum after-process tuning, and can be fully-integrated in a standard CMOS process to reduce the cost.

1.2 Organization

Chapter 2 begins with the overview of a subthreshold MOSFET analytical model which is suitable for circuit design. Then an effective method to use this simple model is introduced and demonstrated on a deep-submicron technology. Finally, we discuss about the matching properties of MOS transistors.

Chapter 3 introduces the MOS PTAT reference prototypes. These circuits are thoroughly analyzed in this chapter. In addition, low-voltage PTAT generators which are applicable in deep-submicron technology are also investigated. The effects of leakage current are discussed and a compensation technique is then proposed.

In Chapter 4, the implementation issues of experimental PTAT references are described in detail. The test setup and measurement environment are also presented. Experimental results for the PTAT references fabricated in a standard 0.25-μm COMS technology are reported and discussed in the end of this chapter.

The conclusions of this work are given in Chapter 5.

CHAPTER 2

SUBTHRESHOLD OPERATION OF MOS TRANSISTORS

This chapter begins with the derivation of a subthreshold MOSFET model dedicated to the design and analysis of low-voltage, low-current analog circuits. Following the brief review of both analytical and accurate models, an effective approach to link these two models is demonstrated on a deep-submicron technology. The mismatch models for MOS transistors and matching properties in the weak inversion region are then discussed in the end of this chapter.

2.1 Introduction

It is well know that when the gate-to-source voltage of a MOS transistor is reduced below the threshold voltage defined by the usual strong inversion characteristics, the channel current decreases approximately exponentially. In this case, the transistor is in weak inversion and is said to be operating in the subthreshold region.

At the first, subthreshold MOSFET conduction attracted attention as the leakage current and should be eliminated if possible [14]. However, as the circuit density continuously increases in modern VLSI design, the weakly inverted MOSFET becomes a very attractive device for low-power low-voltage designs. There are many advantages for operating MOSFETs in subthreshold or weak inversion region: i) extremely low power consumption due to the inherently low currents in that region, ii) low voltage swing, and iii) the exponential natural of the I-V characteristic.

Before we can utilize the subthreshold MOS transistors in very low power

designs, we have to be familiar with the weakly inverted MOSFET in the aspects of circuit design. For this reason, we first investigate the analytical MOS transistor model in weak inversion region in the following section.

2.2 Analytical Model [15]

Subthreshold operation of MOS transistors has long been utilized to implement very low power, low voltage analog circuits. The performance of these analog circuits strongly depends on how the characteristics of the transistors are exploited and mastered. Designers therefore need a model of subthreshold MOS transistor that is suited not only to final numerical circuit simulation but also to the task of exploring new circuits. In this section, an analytical MOS transistor model in weak inversion region which is based on previous publications and suitable for circuit design is introduced.

The cross section of a typical enhancement-mode *n*-channel MOS transistor is depicted in Fig. 2.1. In order to exploit the intrinsic symmetry of the device in the model, the source voltage V_S, the gate voltage V_G, and the drain voltage V_D are all referred to the local substrate. All the symbols adopted in the following paragraphs are reported for clarity in Table 2.1. The Fermi potential f_f is defined as the quasi-Fermi potential of the majority carriers and the channel potential V_{ch}, which depends on the position along the channel, as the difference between the quasi-Fermi potential of the carriers forming the channel f_n and the quasi-Fermi potential of the majority carriers f_p. Since the current density of majority carriers (holes in an *n*-channel transistor) is

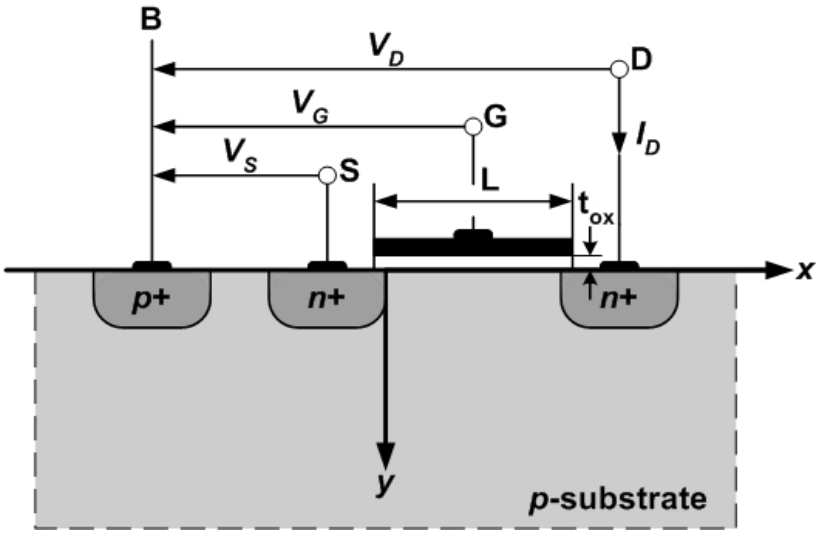


Figure 2.1 Cross section of a typical enhancement-mode *n*-channel MOS transistor.

assumed to be negligible, the quasi-Fermi potential of majority carriers f_p is equal to the Fermi potential f_f and thus the channel potential is simply equal to the difference $f_n - f_f$.

Table 2.1 Definitions used in the model.

Symbols	Description
Q	Electron charge
m_n	Mobility of electrons in the channel
$U_t=(k\cdot T)/q$	Thermal voltage
n_i	Intrinsic carrier concentration
e_s , e_{ox}	Dielectric constant of Si and SiO_2
N_{sub}	Substrate doping concentration
V_{FB}	Flat-band voltage
$f_f=U_t\cdot ln(N_{sub}/n_i)$	Substrate Fermi potential
$f_s=f(y=0)$	Surface potential
$V_{ch}=f_n-f_p=f_n-f_f$	Channel potential
$C¢_{ox}$	Oxide capacitance per unit area
$Q¢_{inv}$	Mobile inversion charge per unit area

The different charges appearing across the MOS structure are represented in Fig. 2.2. The gate charge $Q¢_G$ is balanced by the fixed charged $Q¢_{ox}$ trapped at the $Si-SiO_2$ interface, the inversion charge $Q¢_{inv}$, and the depletion charge $Q¢_B$. The derivation of the characteristics of MOS transistors operating in subthreshold region begins by investigating the inversion charge in strong inversion. By integrating Poisson's

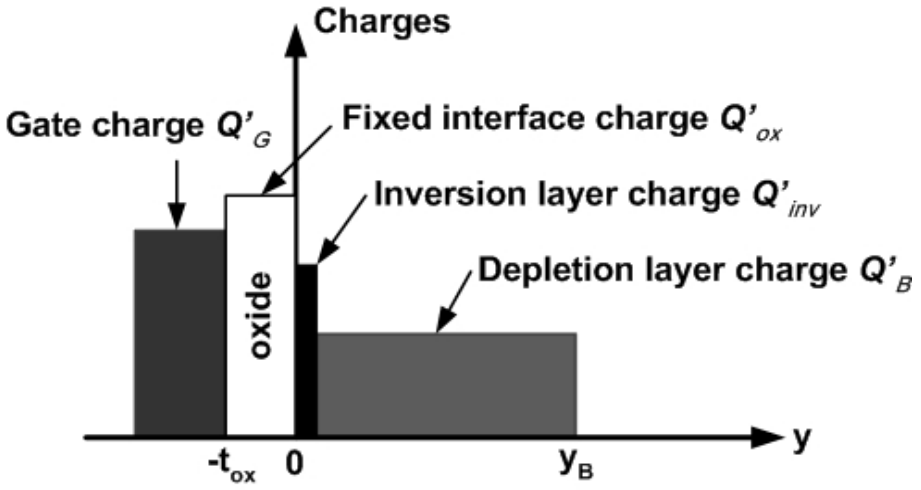


Figure 2.2 Charges appearing across the MOS structure.

equation, the mobile inversion charge density Q'_{inv} can be expressed as a function of f_s and V_{ch}. In the inversion region, f_s is much larger than U_t and the mobile charge density Q'_{inv} simplifies to

$$Q'_{inv} = -g \cdot C'_{ox} \cdot \sqrt{U_t} \cdot \left\{ \sqrt{\frac{f_S}{U_t} + exp\left[\frac{f_S - 2f_f - V_{ch}}{U_t} \right]} - \sqrt{\frac{f_S}{U_t}} \right\} \tag{2.1}$$

A relation between gate voltage and f_s is obtained by applying Gauss' law:

$$V_G = V_{FB} + f_S + g \cdot \sqrt{f_S} - \frac{Q'_{inv}}{C'_{ox}} \tag{2.2}$$

where ? is the body effect coefficient defined as

$$g = \sqrt{\frac{2 \cdot q \cdot e_S \cdot N_{sub}}{C'_{ox}}} \tag{2.3}$$

In strong inversion, the surface potential f_s can be approximated by a constant f_0 + V_{ch} where $f_0 = 2f_f$ + several U_t. Replacing f_s by f_0 + V_{ch} in Equation 2.2 leads to an expression of the inversion charge per unit area valid in strong inversion:

$$Q'_{inv} = -C'_{ox} \cdot [V_G - V_{tB}] \tag{2.4}$$

where V_{tB} is the gate threshold voltage referred to the local substrate and defined as

$$V_{tB} \equiv V_{FB} + f_0 + V_{ch} + g \cdot \sqrt{f_0 + V_{ch}} \tag{2.5}$$

When the channel is at equilibrium (V_{ch} = 0), the gate threshold voltage becomes

$$V_{tB}\big|_{V_{ch}=0} \equiv V_{t0} = V_{FB} + f_0 + g \cdot \sqrt{f_0} \tag{2.6}$$

The inversion charge Q'_{inv} becomes zero for a particular value of the channel potential V_p defined as the pinch-off voltage. The relation between V_p and the gate voltage is obtained from Equation 2.4 to Equation 2.6:

$$V_G\big|_{V_{ch}=V_p;Q'_{inv}=0} = V_{tB}\big|_{V_{ch}=V_p} = V_{t0} + V_p + g \cdot \left[\sqrt{f_0 + V_p} - \sqrt{f_0} \right] \tag{2.7}$$

Each value of the gate voltage corresponds to a different value of the pinch-off voltage. By inverting Equation 2.7, the pinch-off voltage can be expressed in terms of the gate voltage:

$$V_p = V_G - V_{t0} - g \cdot \left[\sqrt{V_G - V_{t0} + \left(\sqrt{f_0} + \frac{g}{2} \right)^2} - \left(\sqrt{f_0} + \frac{g}{2} \right) \right] \tag{2.8}$$

The slope factor n is defined as the derivative of the gate voltage with respect to the pinch-off voltage and is given by

$$n \equiv \frac{dV_G}{dV_p} = 1 + \frac{g}{2 \cdot \sqrt{f_0 + V_p}} \tag{2.9}$$

Since V_p depends on V_G, the slope factor can also be expressed directly as a function of V_G:

$$\frac{1}{n} = \frac{dV_p}{dV_G} = 1 - \frac{g}{2 \cdot \sqrt{V_G - V_{t0} + \left(\sqrt{f_0} + \frac{g}{2} \right)^2}} \tag{2.10}$$

This expression is useful for evaluating n at a certain operating point.

For the values of ? and f_f used in practice, the pinch-off voltage is almost the linear function of the gate voltage and can be approximated by

$$V_p \approx \frac{V_G - V_{t0}}{n} \tag{2.11}$$

where n is evaluated from Equation 2.10. Fig. 2.3 shows the pinch-off voltage calculated using Equation 2.8 and Equation 2.11 respectively. Process parameter values used for calculation are extracted from TSMC 0.25-mm CMOS process. From Fig. 2.3 we can observe that Equation 2.11 gives a good approximation for V_p when the gate voltage is below 1.1 V.

The inversion charge $Q¢_{inv}$ does not vanish abruptly when V_{ch} reaches V_p, but decays smoothly as the channel leaves strong inversion. For V_{ch} somewhat larger than V_p, the channel is in weak inversion and the inversion charge is much less than the charge in the depletion region. By neglecting the $Q¢_{inv}$ term in Equation 2.2 and introducing the definition of V_{t0}, the relation between the surface potential and the gate voltage is obtained:

$$V_G = V_{t0} + (f_S - f_0) + g \cdot \left(\sqrt{f_S} - \sqrt{f_0} \right) \tag{2.12}$$

The pinch-off voltage, which is originally defined in strong inversion, can also be used in weak inversion to approximate the surface potential. Comparing Equation 2.12

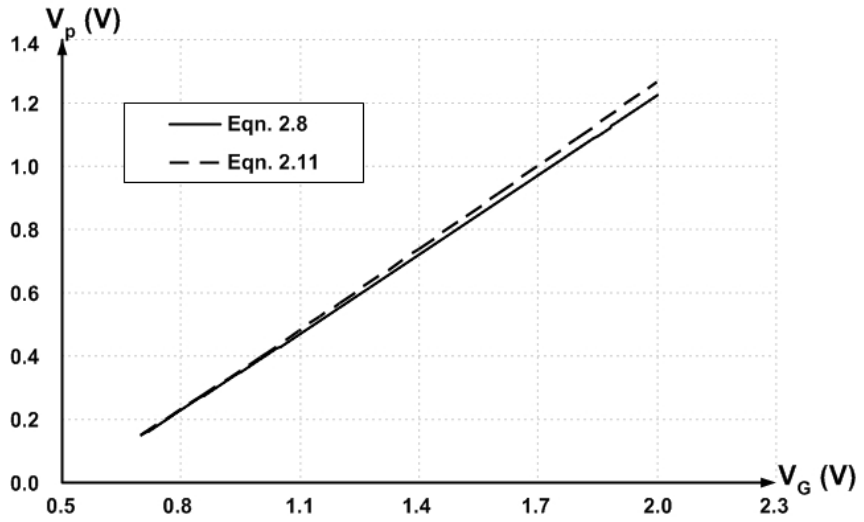


Figure 2.3 Pinch-off voltage versus gate voltage.

to Equation 2.7 gives

$$f_S = f_0 + V_p \tag{2.13}$$

The surface potential can finally be expressed as

$$f_S = \begin{cases} f_0 + V_p & for\ V_{ch} > V_p\ (weak\ inversion) \\ f_0 + V_{ch} & for\ V_{ch} \le V_p\ (strong\ inversion) \end{cases} \tag{2.14}$$

In weak inversion, the surface potential is smaller than $2f_f + V_{ch}$. The exponential term appearing in the general expression of the inversion charge given by Equation 2.1 is thus much smaller than f_s / U_t. The square root term in Equation 2.1 can then be written as

$$\sqrt{\frac{f_S}{U_t} + exp\left[\frac{f_S - 2f_f - V_{ch}}{U_t}\right]} \approx \sqrt{\frac{f_S}{U_t}} \cdot \left\{1 + \frac{U_t}{2 \cdot f_S} \cdot exp\left[\frac{f_S - 2f_f - V_{ch}}{U_t}\right]\right\} \tag{2.15}$$

Thus the expression of the inversion charge is simplified to

$$Q'_{inv} \approx -C'_{ox} \cdot \frac{g}{2 \cdot \sqrt{f_S}} \cdot U_t \cdot e^{\frac{f_S - 2f_f - V_{ch}}{U_t}} \tag{2.16}$$

Substituting $f_s = f_0 + V_p$ into Equation 2.16 gives

$$Q'_{inv} \approx -K_w \cdot C'_{ox} \cdot U_t \cdot e^{\frac{V_p - V_{ch}}{U_t}} \tag{2.17}$$

where

$$K_w = (n-1)\cdot e^{\frac{f_0 - 2f_f}{U_t}} \tag{2.18}$$

Assuming that the mobility m_n is constant along the y axis, a general expression for the drain current including both the diffusion and the drift mechanisms can be expressed as

$$I_D = W\cdot(-Q'_{inv})\cdot m_n \cdot \frac{dV_{ch}}{dx} \tag{2.19}$$

The drain current is then obtained by integrating Equation 2.19 from the source, where $V_{ch} = V_S$ to the drain, where $V_{ch} = V_D$:

$$I_D = m_n \cdot C'_{ox}\cdot\frac{W}{L}\cdot\int_{V_S}^{V_D}\frac{-Q'_{inv}}{C'_{ox}}\cdot dV_{ch} = b\cdot\int_{V_S}^{V_D}\frac{-Q'_{inv}}{C'_{ox}}\cdot dV_{ch} \tag{2.20}$$

where it has been assumed that the mobility is also independent of x. The above equation is valid in all regions of operation since no assumption has been made on the mode of operation of the transistor. The drain current in weak inversion is simply obtained by integrating Equation 2.17:

$$I_D = K_w \cdot b \cdot U_t^2 \cdot \left(e^{\frac{V_P - V_S}{U_t}} - e^{\frac{V_P - V_D}{U_t}} \right) \tag{2.21}$$

Substituting Equation 2.11 into Equation 2.21 gives

$$I_D = K_w \cdot b \cdot U_t^2 \cdot e^{\frac{V_G - V_{t0}}{n\cdot U_t}} \cdot \left(e^{-\frac{V_S}{U_t}} - e^{-\frac{V_D}{U_t}} \right) \tag{2.22}$$

The slope factor n can be evaluated from the gate voltage by using Equation 2.10.

Figure 2.4 plots the drain current versus the drain-source voltage for three values of V_G - V_{t0}, with b = 160 mA／V^2, K_w = 3, and n = 1.5. Notice that the drain current is almost constant when $V_{DS} > 4U_t$, because the last term in Equation 2.22 is negligible in this case. Therefore, unlike in strong inversion, the minimum drain-source voltage required to force the transistor to operate as a current source in weak inversion is independent of the overdrive. Table 2.2 summarizes all the expressions for the drain current in weak inversion. The current in reverse saturation is not shown, but can be obtained by simply replacing V_S by V_D in the expression valid in the forward saturation region.

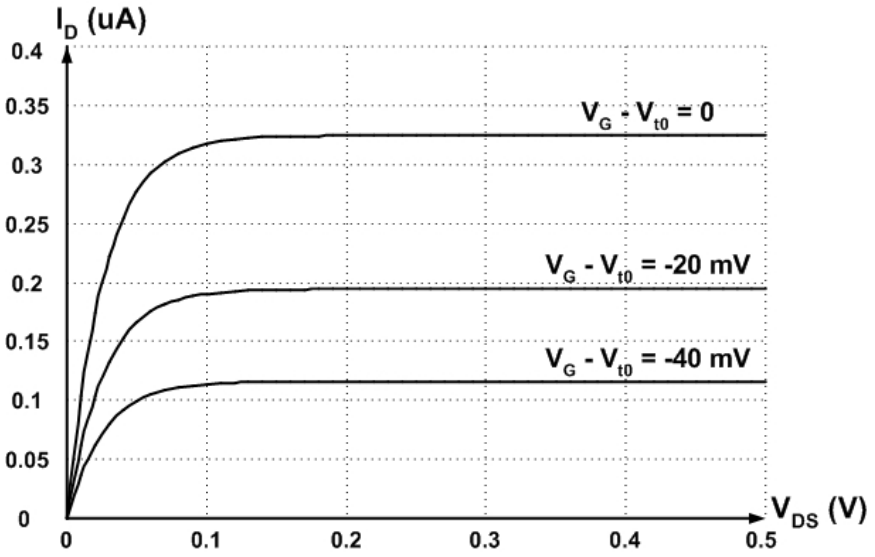


Figure 2.4 Drain current versus drain-source voltage in weak inversion.

Table 2.2 Drain current in weak inversion.

Mode	Conditions	Drain Current
Conduction	$V_S > V_p$ $V_D > V_p$ $V_S \approx V_D$	$K_w \cdot b \cdot U_t^2 \cdot e^{\frac{V_G - V_{t0}}{n \cdot U_t}} \cdot \left(e^{-\frac{V_S}{U_t}} - e^{-\frac{V_D}{U_t}} \right)$
Forward Saturation	$V_S > V_p$ $V_D > V_p$ $V_D - V_S \geq 4 \cdot U_t$	$K_w \cdot b \cdot U_t^2 \cdot e^{\frac{V_G - V_{t0} - n \cdot V_S}{n \cdot U_t}}$
Blocked	$V_S >> V_p$ $V_D >> V_p$	0

Equation 2.22 describes the general behavior of drain current in weak inversion. This expression, which is a good compromise between accuracy and simplicity, supports creative synthesis and is suitable for circuit design. Considerations for using subthreshold MOSFETs in circuit design will be discussed in the later sections.

2.3 Efficient Design [16]

In very low power applications, the use of MOS transistors operating in the weak inversion region is very attractive. However, it is not easy to manipulate the weakly inverted MOSFETs in today's CMOS technology. The derivation of the model

introduced in the previous section did not take higher order effects such as non-uniform doping and short-channel effects into account. On the other hand, the very accurate BSIM model is so complicated that hand calculation for an initial design is very difficult. In a design stage, we need analytical model to create a novel circuit. At the same time, we also rely on simulation results to confirm whether the circuit works. Hence, link both models together is essential in circuit design. In this section, an effective method is introduced to obtain an accurate model for initial hand calculations by extracting key parameters from simulation data.

According to the analytical model introduced in the previous section, the drain current in weak inversion saturation is

$$I_D = K_w \cdot b \cdot U_t^2 \cdot e^{\frac{V_G - V_{t0}}{n \cdot U_t}} \cdot e^{-\frac{V_S}{U_t}} = I_0 \cdot \frac{W}{L} \cdot e^{\frac{V_G}{n \cdot U_t}} \cdot e^{-\frac{V_S}{U_t}} \tag{2.23}$$

where

$$I_0 = K_w \cdot m_n \cdot C'_{ox} \cdot U_t^2 \cdot e^{-\frac{V_{t0}}{n \cdot U_t}} \tag{2.24}$$

By examining Equation 2.23, it may be seen that that the equation is suitable for hand calculation in design stages. The parameter I_0, which is a weak function of biases and thus can be regarded as a constant, comprises all process parameters of the drain current equation. The only two process parameters in Equation 2.23 are I_0 and n. The remaining terms are design parameters W/L, V_G, and V_S set by designers. Traditionally, parameters I_0 and n are evaluated using the process parameters provided by the foundry. Although I_0 and n are calculated from process parameters, the corresponding drain current I_D do not match well to the I_D resulting from simulation due to the inaccuracy of the simple model. Instead of evaluating the two parameters directly, we extract these values from simulation. The method to accurately obtain I_0 and n will be presented later.

The Berkeley Short-Channel IGFET Model (BSIM) is an accurate short-channel MOS transistor model which added numerous empirical parameters to simplify physically meaningful equations. The complete model includes very accurate expressions for DC, capacitance characteristics, and extrinsic components. For channel lengths as low as 0.25 μm, BSIM3 provides reasonable accuracy for subthreshold operation. However, BSIM3 requires approximately 180 parameters which are not directly listed in the SPICE parameter file and thus is not suitable for hand calculation.

To match the analytical I_D equation in Equation 2.23 to the accurate I_D curves from SPICE simulation, parameter extraction for I_0 and n is addressed here. Performing DC analysis on SPICE for the circuit in Fig. 2.5(a) with a given value of W/L, we obtain the $ln(I_D)$-V_G characteristic as plotted in Fig 2.5(b). From Fig. 2.5(b) we can measure the slope of the $ln(I_D)$-V_G curve. The slope can be also determined from Equation 2.23 by differentiating the drain current:

$$slope = \frac{\partial \ln I_D}{\partial V_G} = \frac{1}{n \cdot U_t} \tag{2.25}$$

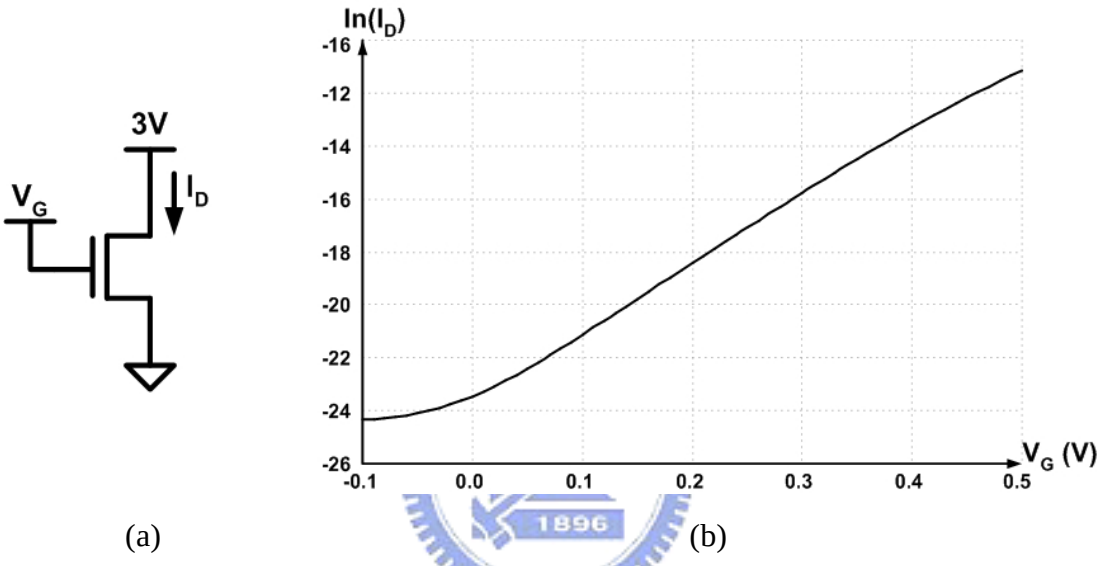


Figure 2.5 (a) Tested circuit. (b) The $ln(I_D)$-V_G characteristic.

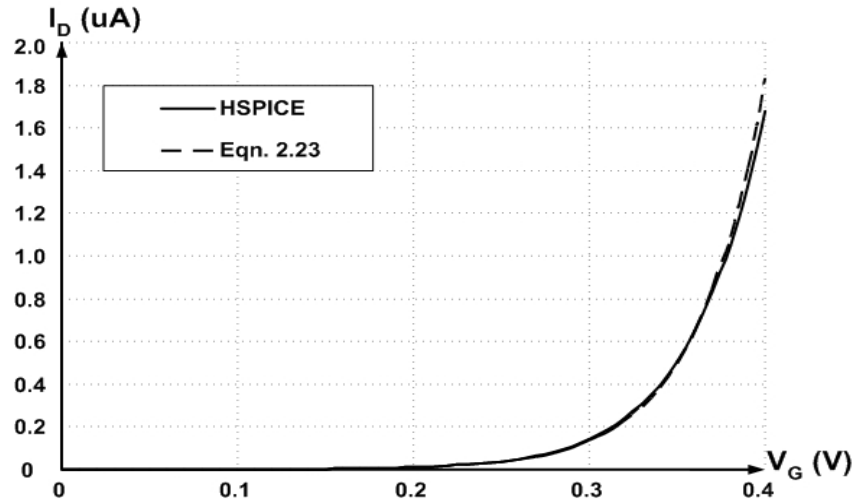
From the measured slope, the slope factor n can be calculated using Equation 2.25 and should have a value between 1.3 and 2. With W/L, V_G, V_S, I_D, and n, the parameter I_0 can be evaluated as follows:

$$I_0 = \frac{I_D}{W/L} \cdot e^{-\frac{V_G}{n \cdot U_t}} \cdot e^{\frac{V_S}{U_t}} \tag{2.26}$$

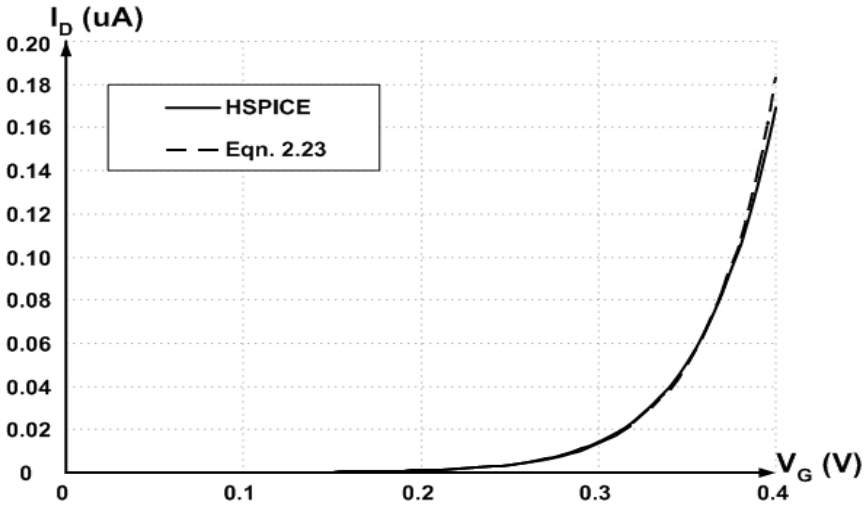
The value of I_0 is obtained by averaging the values of all I_0 obtained from every simulated drain current in weak inversion. Finally, with the extracted parameters I_0 and n, the I_D equation in Equation 2.23 can be used as the accurate and simplified model for the weakly inverted MOSFETs.

Experiments have been done by making the comparisons of I_D plots from the simplified equation and those from HSPICE with three different gate width to length

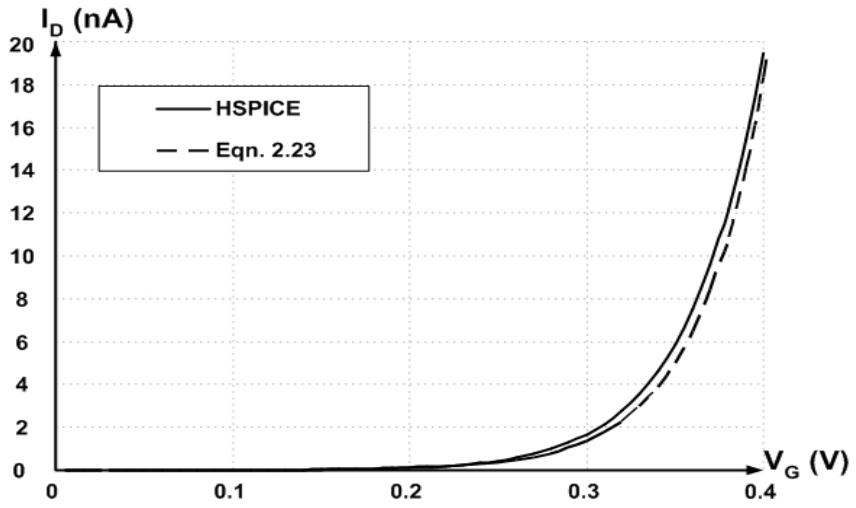
ratios of 400 *m*m／4 *m*m, 40 *m*m／4 *m*m, and 4 *m*m／4 *m*m in a 0.25-*m*m CMOS process. I_0 and n were extracted from the $ln(I_D)$-V_G curve, where W/L was set to 400 *m*m／4 *m*m. Then we used the same I_0 and n but changed W/L to 40 *m*m／4 *m*m and 4 *m*m／4 *m*m to make additional comparisons. Fig. 2.6 shows the results of the comparisons of I_D from the equation and HSPICE with I_0 = 532.16f and n = 1.48. From Fig. 2.6(a) and (b), it is seen that the I_D plots from the equation match well to those from HSPICE. The upper-end curves start splitting from each other since the MOSFET is changing from weak inversion to strong inversion. In Fig. 2.6(c), the I_D curves from the equation and HSPICE do not match well because the I_0 and n were extracted when W/L was 400 *m*m／4 *m*m but in (c) they were used again with W/L = 4 *m*m／4 *m*m. The gate width to length ratio has changed by a factor of 100. There is no problem between the plots in (a) and (b) even though the W/L ratio has changed by a factor of 10. Therefore, the changes of the W/L ratio should be less than a factor of 100 when we use the simplified equation.



(a) W/L = 400 *m*m／4 *m*m



(b) W/L = 40 *m*m／4 *m*m

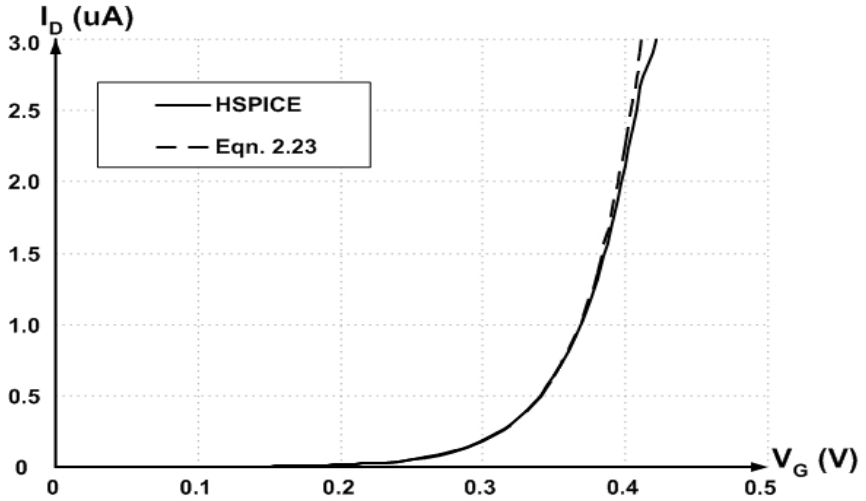


(c) W/L = 4 mm/4 mm

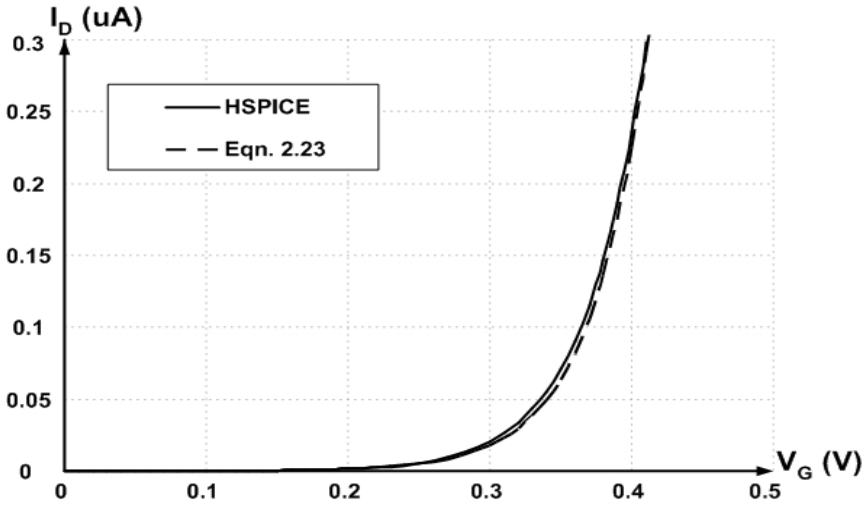
Figure 2.6 Drain current versus gate voltage with different W/L ratios for L = 4 mm.

The same comparisons have also been done for short-channel devices with W/L ratios of 36 mm/0.36 mm, 3.6 mm/0.36 mm, and 0.36 mm/0.36 mm. With I_0 = 874.53f and n = 1.53, extracted from the 36 mm/0.36 mm transistor, the I_D curves are plotted in Fig. 2.7. From Fig. 2.7 we can observe that the simplified model fails to describe the drain current in weak inversion for short-channel devices if the change of the W/L ratio is larger than a factor of 10.

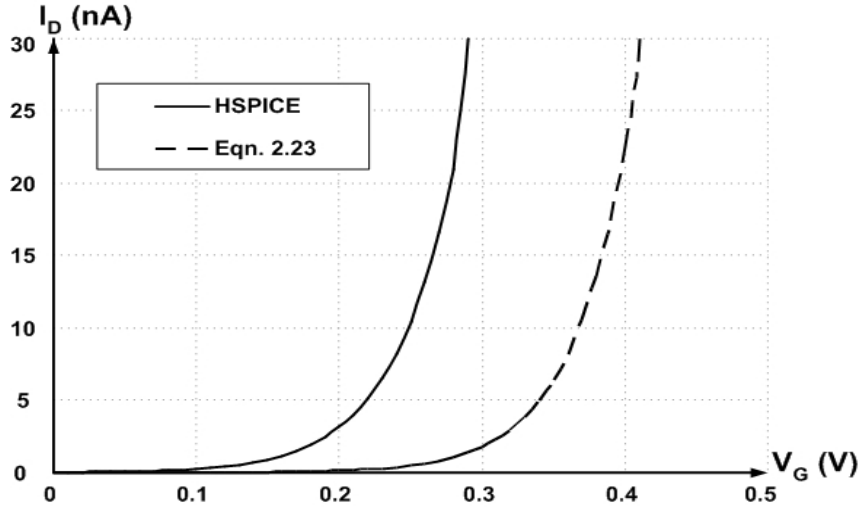
To further investigate the simple model, the drain current plots for different bias conditions have been compared. Fig. 2.8 shows the simulated and calculated I_D curves



(a) W/L = 36 mm/0.36 mm



(b) W/L = 3.6 mm/0.36 mm

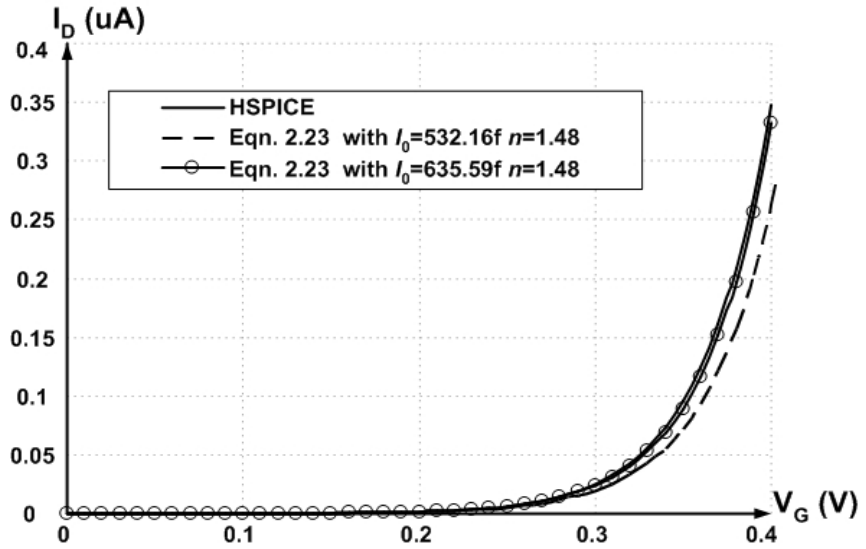


(c) W/L = 0.36 mm/0.36 mm

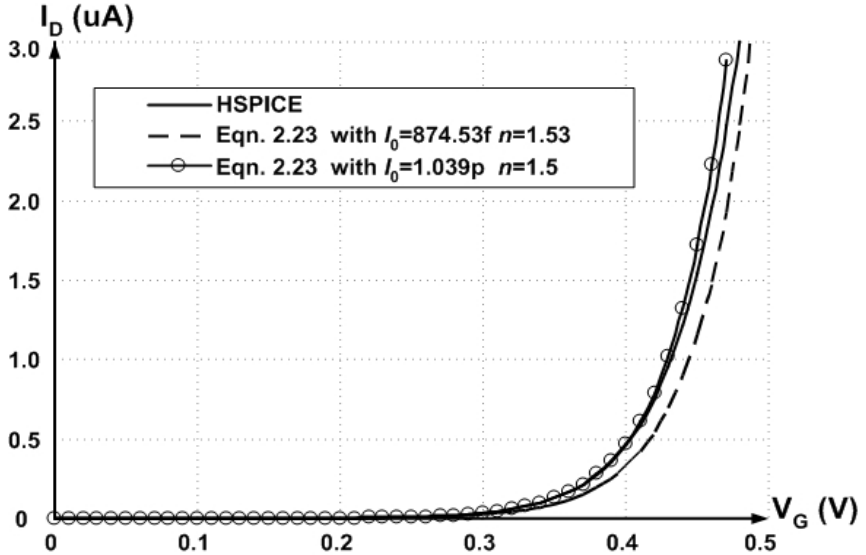
Figure 2.7 Drain current versus gate voltage with different W/L ratios for L = 0.36 mm.

versus gate voltage at V_S = 50 mV for two different W/L ratios of 400 mm/4 mm and 36 mm/0.36 mm. In Fig. 2.8, deviations are observed between the I_D curve calculated using previously extracted parameters and the simulated I_D curve. By re-extracting I_0 and n at V_S = 50 mV, the curves from the equation and simulation become matched.

The technique described in this section maps the BSIM model to an analytical model. This gets accuracy from the accurate model and puts it into a simpler model. The experimental results have confirmed that the technique is useful for low-power low-voltage designs using subthreshold MOSFETs.



(a) W/L = 400 mm／4 mm



(b) W/L = 36 mm／0.36 mm

Figure 2.8 Drain current versus gate voltage at V_S = 50 mV with different W/L ratios.

2.4 Mismatch

Mismatch is the differential performance of two or more devices on a single integrated circuit (IC). It is widely recognized that mismatch is key to precision analog IC design. As stated above, subthreshold operation is attractive for low-power design. The exponential dependence of drain current on gate-to-source voltage provides a very useful property for many applications. However, one of the major disadvantages associated with weakly inverted MOSFETs is the current mismatch between identical drawn devices. Owing to exponential dependencies on the process

variations, devices in subthreshold usually exhibit larger mismatch in drain current as compared with that in above-threshold [14]. The effect of MOS transistor mismatch is therefore prominent for using subthreshold MOSFETs in circuit design. In the following paragraphs, the mismatch models for MOS transistors and matching properties in the weak inversion region are discussed.

MOSFET current mirrors and differential pairs, which are widely used in analog integrated circuits, are usually investigated for transistor mismatch characterization [17]-[24]. Assuming that the drain current is a function of the overdrive V_G - V_{t0} rather than a function of V_G and V_{t0} separately, the mismatch of drain currents in two identical transistors which have the same gate voltage can be modeled as

$$\frac{\Delta I_D}{I_D} = \frac{\Delta \beta}{\beta} - \frac{g_m}{I_D} \cdot \Delta V_{t0} \tag{2.27}$$

where ΔV_{t0} and $\Delta \beta / \beta$ are the threshold voltage mismatch and the current factor mismatch respectively. The current mismatch is maximum in weak inversion, for which g_m / I_D is maximum, and only comes down to $\Delta \beta / \beta$ when the transistors operate deeply in strong inversion.

The threshold voltage mismatch ΔV_{t0} and the current factor mismatch $\Delta \beta / \beta$ are usually used as the two parameters to characterize the matching properties of MOS transistors. Pelgrom et al. [17] introduced a powerful spatial Fourier transform technique to build a general frame for mismatch parameters. Neglecting the separation-dependant mismatch effects, the standard deviations of the threshold voltage mismatch and the current factor mismatch are inversely proportional to the square root of the transistor area:

$$\begin{aligned} \sigma(\Delta V_{t0}) &= \frac{A_{V_{t0}}}{\sqrt{W \cdot L}} \\ \frac{\sigma(\Delta \beta)}{\beta} &= \frac{A_\beta}{\sqrt{W \cdot L}} \end{aligned} \tag{2.28}$$

where $A_{V_{t0}}$ and A_β are the size proportionality constants for $\sigma(\Delta V_{t0})$ and $\sigma(\Delta \beta)/\beta$ respectively. Experimental results showed that Equation 2.28 could predict the threshold voltage mismatch and the current factor mismatch. The two proportionality constants, $A_{V_{t0}}$ and A_β, could be derived from the measured mismatch in threshold voltage and current factor. It was also observed that the threshold voltage mismatch decreased with thinner gate oxides, whereas the current factor mismatch remained almost constant.

With respect to the mismatch in subthreshold MOSFETs, Forti and Wright [18] measured the current mismatch in MOS differential pairs operated in the weak inversion region. They measured a total of about 1400 NMOS and PMOS transistors produced in four different processes with different oxide thickness and feature sizes. Using the scaled current $I_{\ddot{y}} = I_D / (W/L)$, a fairly good uniformly response was found over a wide variety of sizes and V_{GS} values. The measured weak inversion current mismatch was essentially independent of current density as expected and it was observed to be proportional to the inverse square root of device area except for the big transistors and for the PMOS transistors. Furthermore, the substrate bias was judged to be responsible for significant degradation in match.

Chen et al. [19], [20] measured and analyzed the current mismatch of weakly inverted MOS transistors with substrate-to-source junction forward and reverse biased. The MOS transistor with substrate-to-source junction slightly forward biased acts as a high gain gated lateral bipolar transistor in low level injection. The measured mismatch data exhibited that i) subthreshold circuits should be carefully designed for suppression of mismatch arising from back-gate reverse bias, and ii) the current match in weak inversion can be substantially improved by the gated lateral action, especially for small size transistors. An analytical statistical model with back-gate forward bias and device size both as input parameters for optimizing the match can be found in [20].

The mismatch model of MOS transistors derived in [17] has been found in good agreement with experimental results for a device size above 2 μm. However, it was observed that the threshold voltage mismatch linear dependence on the inverse of the square root of the device area no longer holds for transistors with $L = 0.7$ μm [21]. Due to the strong dependence of the threshold voltage and of the effective mobility on channel length for short-channel transistors, the mismatch model described in Equation 2.28 is not applicable for submicron devices. The mismatch model proposed by Croon et al. [22], [23] is based on parametric extensions of [17] and is validated on a 0.18-μm technology. The mismatch model contains four parameters: one parameter (DV_{t0}) to describe the mismatch in the threshold voltage, and three (Db_0, Dz_{sr}, and Dz_{sat}) to describe the mismatch in the current factor. The parameter Db_0 is the low field current factor for long transistors while the other two parameters, Dz_{sr} and Dz_{sat}, are used to model the higher order effects such as surface roughness scattering, series resistance, and velocity saturation. These mismatch parameters are modeled by the complete Pelgrom model [17]:

$$s^2(DP) = \frac{A_{P,0}^2}{W \cdot L} + \frac{A_{P,L}^2}{W \cdot L^2} + \frac{A_{P,W}^2}{W^2 \cdot L} \tag{2.29}$$

The first term of the right-hand side models the variance for a large device, while the second and third terms describe the variation in short and narrow channel effects. The correlation factors between mismatch parameters can also be modeled by

$$r_{P_1,P_2} = A_{P_{12},0} + \frac{A_{P_{12},L}}{L} + \frac{A_{P_{12},W}}{W} \tag{2.30}$$

The first term on the right-hand side gives the correlation for large transistors, while the second and third terms account for short and narrow channel effects. The detailed mismatch model in drain current and the procedure for extracting the mismatch parameters can be found in [23].

CHAPTER 3

CMOS PTAT REFERENCES

This chapter deals with the analysis and design of MOS PTAT references. We describe the operation principles of MOS PTAT prototypes and analyze these circuits in detail. In addition to this, low-voltage PTAT generators which are applicable in deep-submicron technology have been also investigated. In the end of this chapter, the effects of leakage current at high temperature are discussed and a compensation technique to enhance the linearity is proposed.

3.1 Introduction

The PTAT circuits generate an output voltage proportional to absolute temperature and have been widely used in temperature-insensitive voltage and current references. In a thermal management system, the PTAT reference is also the best candidate for a fully-integrated temperature sensor. Traditionally, PTAT references are implemented using parasitic substrate bipolar transistors available in all standard CMOS processes. A typical PTAT generator using parasitic BJTs is shown in Fig. 3.1. When both transistors are at the same temperature, the difference between emitter-to-base voltages, DV_{EB}, of two diode-like bipolar transistors can be written as

$$DV_{EB} = V_{EB1} - V_{EB2} = U_t \cdot ln\left(\frac{I_1}{I_2}\frac{I_{S2}}{I_{S1}}\right) \tag{3.1}$$

where U_t is the thermal voltage and I_{S1} as well as I_{S2} are the saturation current for Q1 and Q2 respectively. If the two transistors are matched, DV_{EB} is directly proportional to absolute temperature, *i.e.*, it is a PTAT signal.

Various on-chip PTAT references have been extensively implemented using

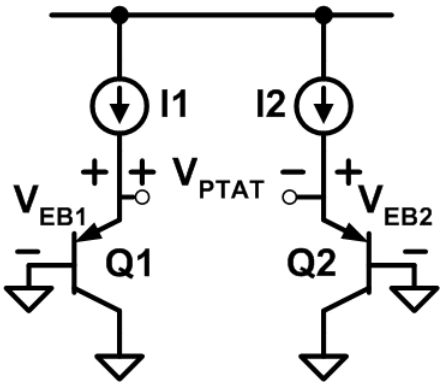


Figure 3.1 Typical PTAT generator.

parasitic BJTs because of the ease of design. In some CMOS process, however, obtaining reliable BJTs is very costly and the desirable performance from these parasitic devices is hard to expect. Also, the power consumption of the BJT based references is relatively high and an alternative approach is preferred, especially in low power applications.

Several PTAT references using the subthreshold MOS transistors have been studied and applied in low-power low-voltage designs [12], [13], [25]-[30]. These circuits take advantage of MOS devices operating in the weak inversion region in two respects: i) the exponential I-V characteristic is used to generate a PTAT voltage, and ii) the power consumption is made minimum due to the inherent low currents in that region. The properties of MOS PTAT references make them an excellent temperature sensor in a thermal management system. To implement the competitive temperature sensors in deep-submicron technology, we first analyze the prototype circuits of MOS PTAT references in the following section.

3.2 MOS PTAT Generator Prototypes

Several kinds of MOS PTAT generators have been reported for use in a wide range of applications. All of these PTAT circuits can be categorized into three types. In this section, the prototype circuits of MOS PTAT generators will be introduced and analyzed.

3.2.1 Prototype I: Diode Connection

The first MOS PTAT prototype [25] is shown in Fig. 3.2. If transistors M1 and M2 operate in weak inversion, the drain currents of M1 and M2 are given by

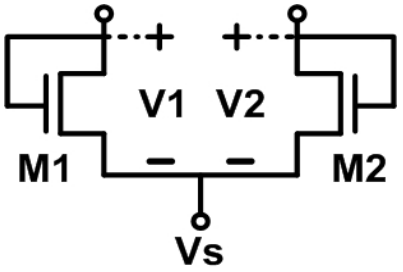


Figure 3.2 MOS PTAT generator prototype I: diode connection.

$$I_{D1} = K_{w1} \cdot b_1 \cdot U_t^2 \cdot e^{\frac{V_1 - V_{t0,1} - (n_1 - 1)V_S}{n_1 \cdot U_t}}$$
$$I_{D2} = K_{w2} \cdot b_2 \cdot U_t^2 \cdot e^{\frac{V_2 - V_{t0,2} - (n_2 - 1)V_S}{n_2 \cdot U_t}} \tag{3.2}$$

where it is assumed that $V_{1,2} >> U_t$. Equation 3.2 can be derived to

$$V_1 = V_{t0,1} + (n_1 - 1) \cdot V_S + n_1 \cdot U_t \cdot ln\left(\frac{I_{D1}}{A_1}\right)$$
$$V_2 = V_{t0,2} + (n_2 - 1) \cdot V_S + n_2 \cdot U_t \cdot ln\left(\frac{I_{D2}}{A_2}\right) \tag{3.3}$$

where

$$A_{1,2} = K_{w1,2} \cdot b_{1,2} \cdot U_t^2 \tag{3.4}$$

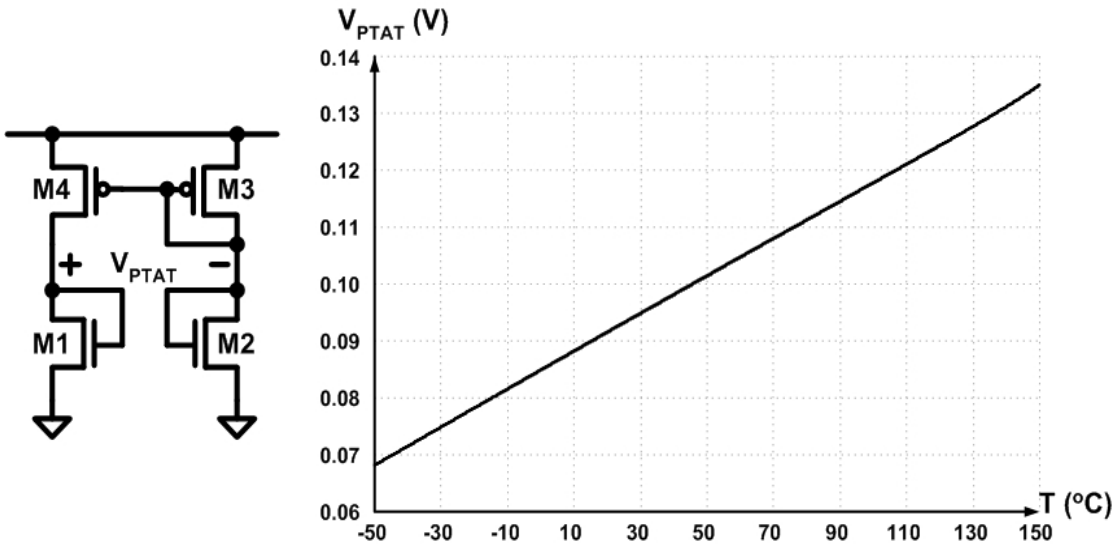
If M1 and M2 are matched, the PTAT voltage can be obtained from the difference in V_1 and V_2:

$$V_{PTAT} = V_1 - V_2 = n \cdot U_t \cdot ln\left(\frac{I_{D1}}{I_{D2}} \cdot \frac{S_2}{S_1}\right) \tag{3.5}$$

where S_1 and S_2 are the W/L ratios of M1 and M2 respectively. To examine the temperature characteristic of the prototype, we have simulated the circuit shown in Fig. 3.3(a) in a 0.25-*m*m CMOS process. In this circuit, *p*-channel MOSFETs M3 and M4 act as a current mirror and the minimum supply voltage for which M3 and M4 operate in the strong inversion saturation region is

$$V_{DD,min} = V_{GS,w} + V_{SG,p} \tag{3.6}$$

where $V_{GS,w}$ represents the gate-source voltage of the transistor in weak inversion and $V_{SG,p}$ is the source-gate voltage of PMOS transistors. In the simulation, the device sizes S_1 and S_2 are set to equal while the current ratio I_{D1}/I_{D2} is 10. The PTAT voltage



(a) (b)

Figure 3.3 Simulation of MOS PTAT prototype I. (a) Simulation circuit. (b) PTAT voltage versus temperature.

versus temperature plot is shown in Fig. 3.3(b).

Equation 3.5 is based on the assumption that transistors M1 and M2 are perfectly matched. In reality, however, nominally identical devices suffer from a finite mismatch due to uncertainties in each step of the manufacturing process. To take into account the threshold voltage and the current factor mismatch in the circuit shown in Fig. 3.3(a), we now define average and mismatch quantities as follows:

$$V_{t0} = \frac{V_{t0,1} + V_{t0,2}}{2}$$
$$DV_{t0} = V_{t0,1} - V_{t0,2} \tag{3.7}$$

$$b_1 = S_1 \cdot b_{w1}$$
$$b_2 = S_2 \cdot b_{w2}$$
$$b_w = \frac{b_{w1} + b_{w2}}{2} \tag{3.8}$$
$$Db_w = b_{w1} - b_{w2}$$

$$b_3 = S_3 \cdot b_{p3}$$
$$b_4 = S_4 \cdot b_{p4}$$
$$b_p = \frac{b_{p3} + b_{p4}}{2} \tag{3.9}$$
$$Db_p = b_{p3} - b_{p4}$$

These relations can be inverted to give the original parameters in terms of the average and the mismatch parameters. For example,

$$\begin{aligned} b_1 &= S_1 \cdot \left(b_w + \frac{Db_w}{2} \right) \\ b_2 &= S_2 \cdot \left(b_w - \frac{Db_w}{2} \right) \end{aligned} \tag{3.10}$$

Applying this set of equations for the various parameters in Equation 3.3 and solving for V_1- V_2, we obtain

$$V_1 - V_2 = DV_{t0} + n \cdot U_t \cdot \left[ln\left(\frac{S_4}{S_3} \cdot \frac{S_2}{S_1} \right) + ln\left(\frac{1 - Db_p/2 \cdot b_p}{1 + Db_p/2 \cdot b_p} \right) + ln\left(\frac{1 - Db_w/2 \cdot b_w}{1 + Db_w/2 \cdot b_w} \right) \right] \tag{3.11}$$

If $Db_{p,w} / 2 \cdot b_{p,w} << 1$, the last two terms in the above equation can be written as

$$ln\left(\frac{1 - Db_{p,w}/2 \cdot b_{p,w}}{1 + Db_{p,w}/2 \cdot b_{p,w}} \right) \approx ln\left(1 - \frac{Db_{p,w}}{2 \cdot b_{p,w}} \right)^2 \approx -\frac{Db_{p,w}}{b_{p,w}} \tag{3.12}$$

Substituting these approximations into Equation 3.11 gives

$$\begin{aligned} V_1 - V_2 &\approx n \cdot U_t \cdot ln\left(\frac{S_4}{S_3} \cdot \frac{S_2}{S_1} \right) - n \cdot U_t \cdot \left(\frac{Db_p}{b_p} + \frac{Db_w}{b_w} \right) + DV_{t0} \\ &= V_{PTAT,ideal} - n \cdot U_t \cdot \left(\frac{Db_p}{b_p} + \frac{Db_w}{b_w} \right) + DV_{t0} \end{aligned} \tag{3.13}$$

Equation 3.13 indicates that the accuracy of the PTAT signal is strongly dependent on the mismatch in transistors since the value of V_{PTAT} is usually smaller than 100 mV at room temperature.

3.2.2 Prototype II: Cascode Configuration

The second MOS PTAT prototype [26], [27] is shown in Fig. 3.4. In the elementary cell, the two transistors M1 and M2 both operate in the subthreshold region. Because M2 is diode connected, it operates in the forward saturation mode and forces M1 to operate in the conduction mode. Since M2 operates in the saturation mode,

$$I_D = K_{w2} \cdot b_2 \cdot U_t^2 \cdot e^{\frac{V_G - V_{t0,2} - n_2 \cdot V_2}{n_2 \cdot U_t}} \tag{3.14}$$

Since M1 operates in the conduction mode,

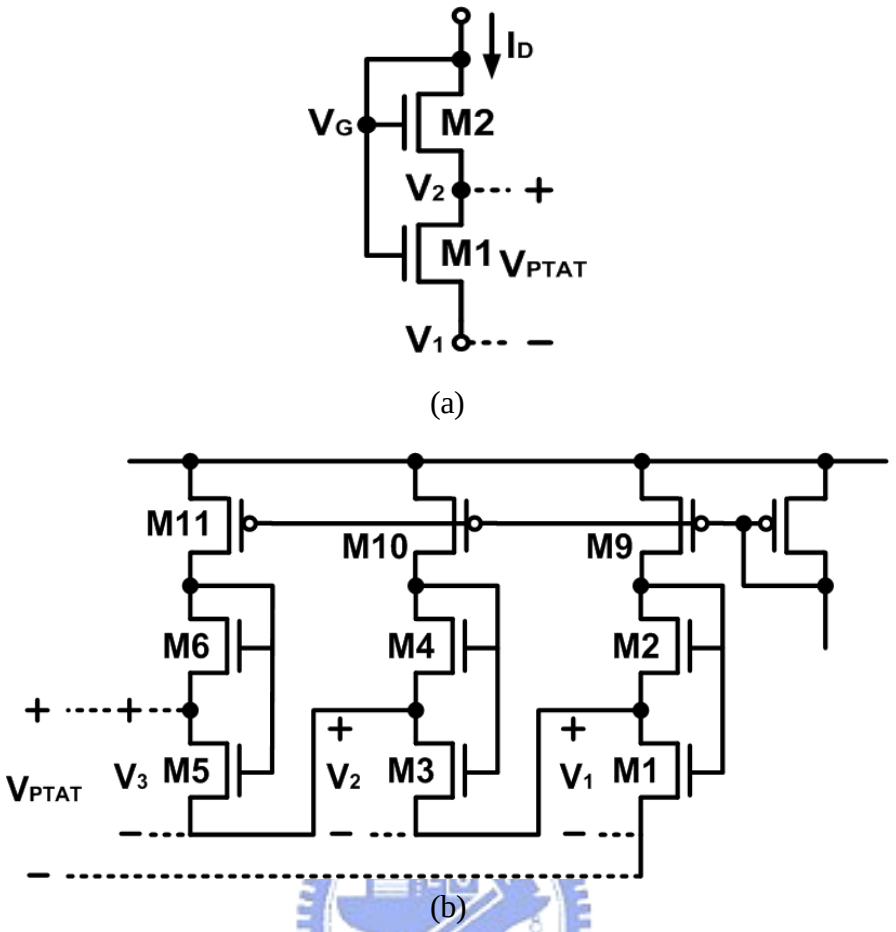


Figure 3.4 MOS PTAT generator prototype II: cascode configuration. (a) Elementary cell. (b) Stack of elementary cells.

$$I_D = K_{w1} \cdot b_1 \cdot U_t^2 \cdot e^{\frac{V_G - V_{t0,1}}{n_1 \cdot U_t}} \cdot \left(e^{-\frac{V_1}{U_t}} - e^{-\frac{V_2}{U_t}} \right) \tag{3.15}$$

If M1 and M2 are matched, the PTAT voltage can be derived from Equation 3.14 and Equation 3.15:

$$V_{PTAT} = V_2 - V_1 = U_t \cdot ln\left(1 + \frac{S_2}{S_1}\right) \tag{3.16}$$

where S_1 and S_2 are the W/L ratios of M1 and M2 respectively. Values of V_{PTAT} practically obtainable from an elementary cell are limited to about 100 mV. Higher values may be obtained by stacking a certain number of cells as shown in Fig. 3.4(b). In this circuit, the voltage V_{PTAT} is composed of three sections. The mode of operation is still the same, except that the current supplied to each cell goes through the bottom transistor of all subsequent cells. For instance, the PTAT voltage formed by section

M1-M2 is given by

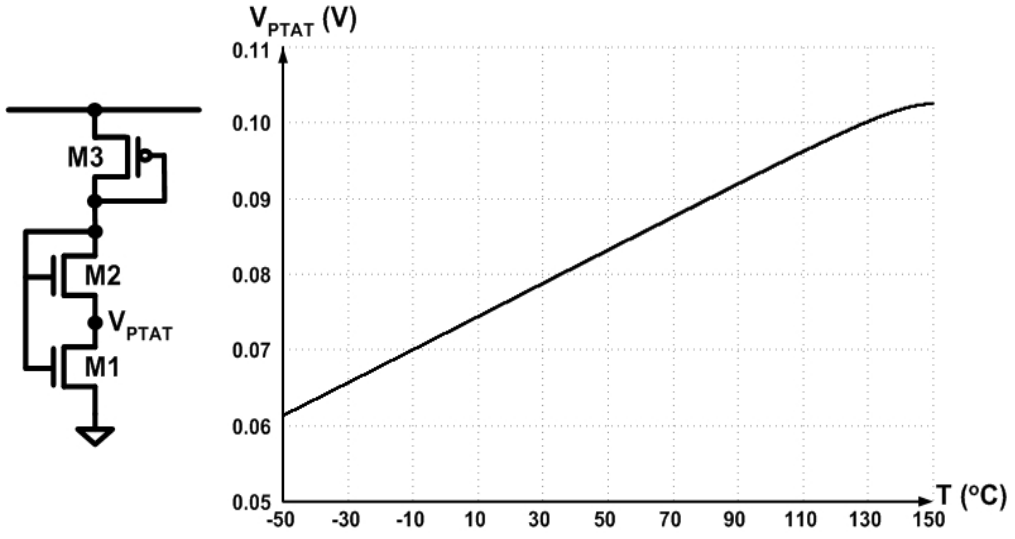
$$V_1 = U_t \cdot ln\left(1 + \frac{S_2}{S_1} \cdot \frac{S_9 + S_{10} + S_{11}}{S_9}\right) \tag{3.17}$$

where S_9, S_{10}, and S_{11} are W/L ratios of the respective MOSFETs.

Fig. 3.5 shows the simulated circuit and the PTAT voltage plot of this prototype. In Fig. 3.5(a), the transistor M3 which operate in strong inversion serves as a current source and the minimum supply voltage is given by

$$V_{DD,min} = V_{GS,w} + V_{SG,p} \tag{3.18}$$

Fig. 3.5(b) shows the simulated V_{PTAT} with S_2/S_1 = 9. The curve deviates from the straight line at high temperature due to the effect of leakage currents.



(a) (b)

Figure 3.5 Simulation of MOS PTAT prototype II. (a) Simulation circuit. (b) PTAT voltage versus temperature.

We now consider the effect of transistor mismatch in the circuit shown in Fig. 3.5(a). Applying the expressions in Equation 3.7 and Equation 3.8 and neglecting high-order terms, we obtain

$$V_{PTAT} \approx U_t \cdot ln\left[1 + \frac{S_2}{S_1} \cdot \left(1 - \frac{Db_w}{b_w}\right) \cdot e^{\frac{DV_{t0}}{n \cdot U_t}}\right] \tag{3.19}$$

If $S_2 >> S_1$, the PTAT voltage can be rewritten as

$$\begin{aligned} V_{PTAT} &\approx U_t \cdot ln\left(\frac{S_2}{S_1}\right) - U_t \cdot \frac{Db_w}{b_w} + \frac{DV_{t0}}{n} \\ &= V_{PTAT,ideal} - U_t \cdot \frac{Db_w}{b_w} + \frac{DV_{t0}}{n} \end{aligned} \tag{3.20}$$

In Fig. 3.4(b), the PTAT voltages V_1, V_2, and V_3 can also be derived similarly and have the same mismatch terms as in Equation 3.20 except the presence of Db_p / b_p due to the current mismatch in the PMOS current mirror. Since the voltage variations of the three cells are not statistically correlated, the standard deviation of the voltage variation is therefore multiplied by $\sqrt{3}$ and the spread of V_{PTAT} is reduced.

3.2.3 Prototype III: Common Gate Connection

Fig. 3.6 shows the third MOS PTAT prototype [12], [13], [27]-[30]. If transistors M1 and M2 are in weak inversion and their drain-source voltages are both much larger then U_t, the drain currents can be expressed as

$$\begin{aligned} I_{D1} &= K_{w1} \cdot b_1 \cdot U_t^2 \cdot e^{\frac{V_G - V_{t0,1} - n_1 \cdot V_1}{n_1 \cdot U_t}} \\ I_{D2} &= K_{w2} \cdot b_2 \cdot U_t^2 \cdot e^{\frac{V_G - V_{t0,2} - n_2 \cdot V_2}{n_2 \cdot U_t}} \end{aligned} \tag{3.21}$$

Assuming that M1 and M2 are matched, the PTAT signal can be obtained and is given by

$$V_{PTAT} = V_1 - V_2 = U_t \cdot ln\left(\frac{I_{D2}}{I_{D1}} \cdot \frac{S_1}{S_2}\right) \tag{3.22}$$

where S_1 and S_2 are the W / L ratios of M1 and M2 respectively.

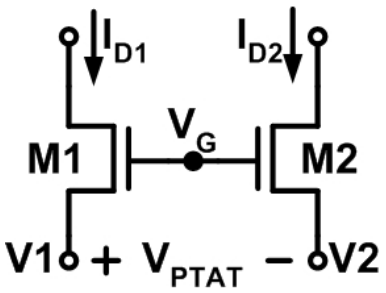
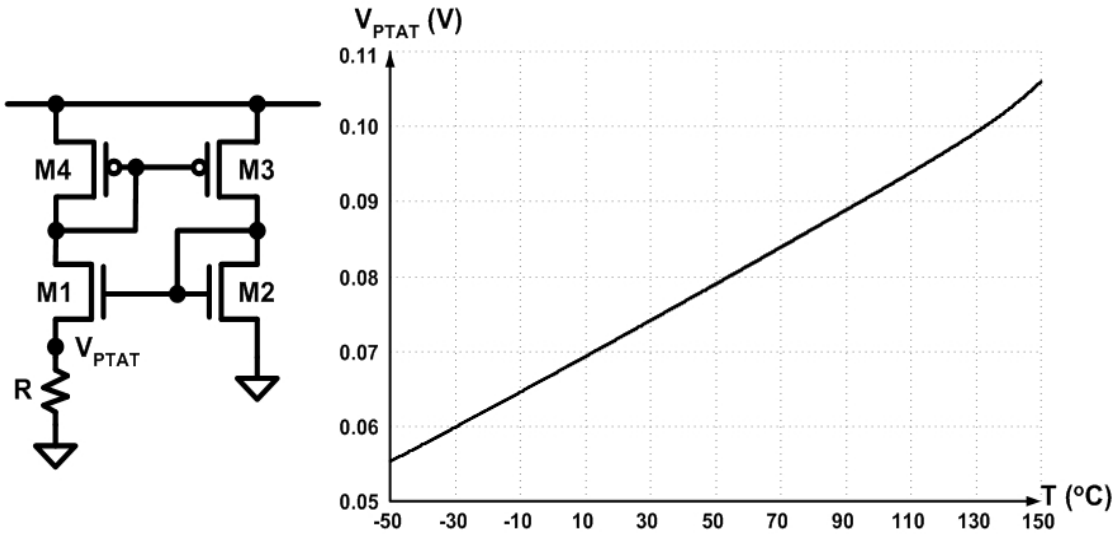


Figure 3.6 MOS PTAT generator prototype III: common gate connection.

We also examine the temperature characteristic of this prototype circuit through simulation. The simulated circuit shown in Fig. 3.7(a) is derived from a circuit used with bipolar transistors and has been utilized in several designs. The *p*-channel MOSFETs M3 and M4 act as a current mirror and the minimum supply voltage is given by

$$V_{DD,min} = V_{PTAT} + V_{DS,w} + V_{SG,p} \tag{3.23}$$

where $V_{DS,w}$ is the drain-source voltage of the transistor in weak inversion. In the simulation, the device size ratios S_1 and S_2 are set to equal while the current ratio I_{D2} / I_{D1} is 10. Fig. 3.7(b) shows the PTAT voltage V_{PTAT} versus temperature. At high temperature, deviations from the ideal PTAT behavior due to leakage currents are also observed.



(a) (b)

Figure 3.7 Simulation of MOS PTAT prototype III. (a) Simulation circuit. (b) PTAT voltage versus temperature.

Consider the circuit shown in Fig. 3.7(a). The variation of V_{PTAT} may come from threshold voltage and current factor mismatch in M1-M2 pair and the current mismatch in the current mirror formed by M3 and M4. Applying the mismatch parameters defined by Equation 3.7 to Equation 3.9 in the derivation of V_{PTAT}, we obtain

$$V_{PTAT} \approx U_t \cdot ln\left(\frac{S_1}{S_2}\cdot\frac{S_3}{S_4}\right)+U_t\cdot\left(\frac{Db_w}{b_w}+\frac{Db_p}{b_p}\right)-\frac{DV_{t0}}{n}$$
$$= V_{PTAT,ideal}+U_t\cdot\left(\frac{Db_w}{b_w}+\frac{Db_p}{b_p}\right)-\frac{DV_{t0}}{n} \quad (3.24)$$

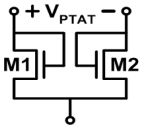
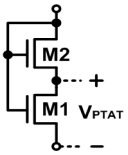
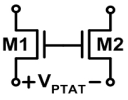
Note that the mismatch terms in Equation 3.24 are almost the same as those in Equation 3.20. In this circuit, the mismatch of resistor does not affect the PTAT voltage as long as M1 and M2 both operate in weak inversion.

3.2.4 Summary

The temperature and mismatch characteristics of MOS PTAT prototypes have been addressed in the previous paragraphs. These results are summarized in Table 3.1. The Db_p/b_p terms are omitted in expressions of DV_{PTAT} since the current factor mismatch in strong inversion is negligible compared to that in weak inversion.

The PTAT signal of prototype I is proportional to nU_t while the other two prototype circuits generate output voltages proportional to U_t. The value of the slope factor n ranges usually from 1.3 to 2 and a larger V_{PTAT} can be obtained in prototype I. In a standard CMOS process, however, the slope factor is not a reliable parameter and its value depends slightly on the bias conditions. Furthermore, the higher supply voltage requirement due to diode-connected transistors makes prototype I incompatible with low-voltage operation.

Table 3.1 Characteristics of MOS PTAT prototypes.

Prototype	V_{PTAT}	DV_{PTAT}	$V_{DD,min}$	
I 	$n\cdot U_t\cdot ln\left(\frac{I_{D1}}{I_{D2}}\cdot\frac{S_2}{S_1}\right)$	$\pm n\cdot U_t\cdot\frac{Db_w}{b_w}\pm DV_{t0}$	$V_{GS,w}+V_{SG,p}$	[25]
II 	$U_t\cdot ln\left(1+\frac{S_2}{S_1}\right)$	$\pm U_t\cdot\frac{Db_w}{b_w}\pm\frac{DV_{t0}}{n}$	$V_{GS,w}+V_{SG,p}$	[26] [27]
III 	$U_t\cdot ln\left(\frac{I_{D2}}{I_{D1}}\cdot\frac{S_1}{S_2}\right)$	$\pm U_t\cdot\frac{Db_w}{b_w}\pm\frac{DV_{t0}}{n}$	$V_{PTAT}+V_{DS,w}+V_{SG,p}$	[27] | [30]

The characteristics of prototypes II and III are very similar. Prototype II provides a floating PTAT voltage and the elementary cells can be stacked to produce PTAT voltages of the order of a few hundreds of millivolts. As an additional advantage, the mismatch between transistors is averaged out in a stacked PTAT generator. The spread of V_{PTAT} can be reduced at the expense of a larger supply voltage.

3.3 Low-Voltage PTAT References in Deep-Submicron Technology

Low-voltage implementations for PTAT references are necessary for the complete system-on-chip such as thermal management system. Such PTAT references must exhibit the best compatibility in deep-submicron technology. In the following paragraphs, we will investigate the low-voltage MOS PTAT references in detail.

3.3.1 Power-Supply Rejection Ratio (PSRR)

The MOS PTAT prototype circuit shown in Fig. 3.7(a) seems suitable for low-voltage designs. However, the power-supply rejection ratio (PSRR) of this circuit deteriorates sharply in deep-submicron technology. Fig. 3.8 shows the low-frequency small-signal model of the MOS PTAT generator shown in Fig. 3.7(a). From Fig. 3.8, the small-signal gain v_{ptat}/v_{dd} can be derived to

$$\frac{v_{ptat}}{v_{dd}} = \frac{R \cdot g_4 \cdot \left(g_2' \cdot g_{o1} + g_{m1} \cdot g_{o3}\right)}{g_2' \cdot \left(g_{o1} + g_4 + g_1 \cdot g_4 \cdot R\right) - g_{m1} \cdot g_{m3}} \tag{3.25}$$

where $g_2' = g_2 + g_{o3}$. In most practical cases, $g_{m1} >> g_{o1}$, $g_{m2} >> g_{o2} + g_{o3}$, and $g_{m4} >> g_{o4} + g_{o1}$. Then

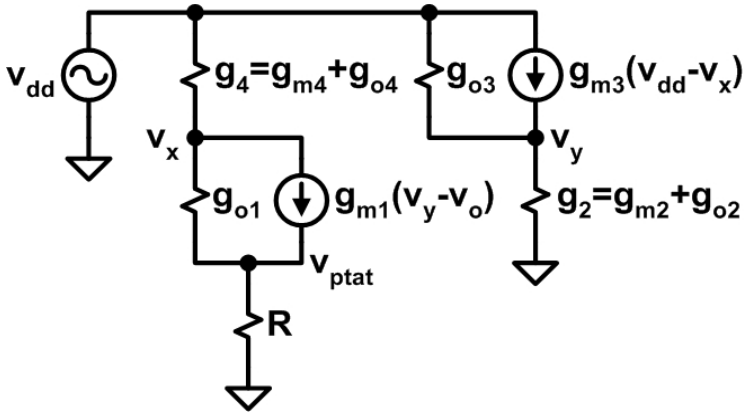


Figure 3.8 Low-frequency small-signal model of the MOS PTAT generator shown in Fig. 3.7(a).

$$\frac{v_{ptat}}{v_{dd}} \approx \frac{R \cdot g_{m4} \cdot (g_{m2} \cdot g_{o1} + g_{m1} \cdot g_{o3})}{g_{m2} \cdot g_{m4} \cdot (1 + g_{m1} \cdot R) - g_{m1} \cdot g_{m3}} \tag{3.26}$$

Since M1 and M2 are in weak inversion and M3 and M4 act as a current mirror,

$$\frac{g_{m2}}{g_{m1}} = \frac{I_{D2}}{I_{D1}} = \frac{S_3}{S_4} = \frac{g_{m3}}{g_{m4}} \equiv P \tag{3.27}$$

Substituting Equation 3.27 into Equation 3.26, we have

$$\frac{v_{ptat}}{v_{dd}} \approx \frac{g_{o1} + g_{o3}/P}{g_{m1}} \tag{3.28}$$

In deep-submicron technology, the ratio g_{m1} / g_{o1} is typically smaller than 200 and the resulting static PSRR$^+$ is usually smaller than 50 dB. Fig 3.9 shows the simulated V_{PTAT} and static PSRR$^+$ versus supply voltage at room temperature for the PTAT generator shown in Fig. 3.7(a). For PSRR(DC)$^+$ > 40 dB, the minimum supply voltage is 1.5 V.

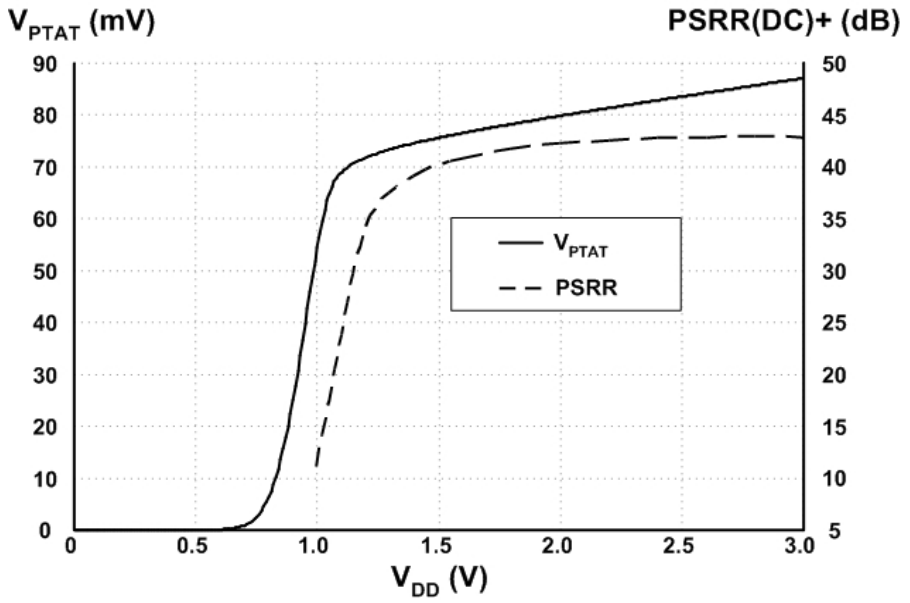


Figure 3.9 Simulated V_{PTAT} and static PSRR$^+$ versus supply voltage at room temperature for the PTAT generator shown in Fig. 3.7(a).

A low-voltage MOS PTAT reference based on the same prototype [13] is depicted in Fig. 3.10. The simple current mirror in Fig. 3.7(a) is replaced by the operational transresistance amplifier (ORA) composed of M3-M8. The role of the ORA is to ensure the current ratio I_{D2} / I_{D1}, as well as an almost equal voltage biasing for both drain voltages of M1 and M2. Thanks to the latter, the channel length modulation effects in M1-M2 can be minimized.

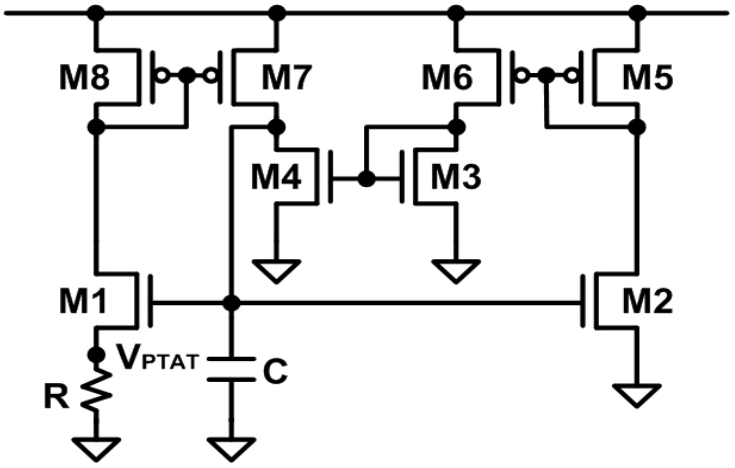


Figure 3.10 The low-voltage MOS PTAT reference.

The small-signal DC gain v_{ptat}/v_{dd} of this circuit can be derived from the low-frequency small-signal model shown in Fig. 3.11. Assume $g_o << g_m$ for all transistors, then

$$\frac{v_{ptat}}{v_{dd}} \approx \frac{R \cdot g_{m4} \cdot g_{m6} \cdot g_{m8} \cdot (g_{m2} \cdot g_{o1} - g_{m1} \cdot g_{o2})}{g_{m2} \cdot g_{m4} \cdot g_{m6} \cdot g_{m8} \cdot (1 + g_{m1} \cdot R) - g_{m1} \cdot g_{m3} \cdot g_{m5} \cdot g_{m7}} \tag{3.29}$$

If $g_{m3} = g_{m4}$ and $g_{m6} = g_{m7}$, the above equation can be rewritten as

$$\frac{v_{ptat}}{v_{dd}} \approx \frac{R \cdot g_{m8} \cdot (g_{m2} \cdot g_{o1} - g_{m1} \cdot g_{o2})}{g_{m2} \cdot g_{m8} \cdot (1 + g_{m1} \cdot R) - g_{m1} \cdot g_{m5}} \tag{3.30}$$

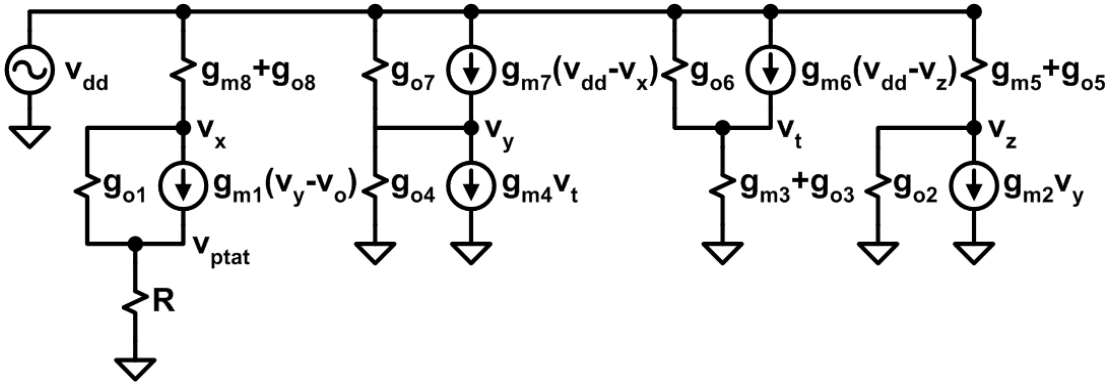


Figure 3.11 Low-frequency small-signal model of the MOS PTAT reference shown in Fig. 3.10.

Ideally, $g_{m1,2}$ and $g_{o1,2}$ are all proportional to their drain currents since M1 and M2 are both in weak inversion. As a result, $g_{m2} \cdot g_{o1} = g_{m1} \cdot g_{o2}$ and $PSRR^+$ approximates to infinity for low frequencies. The finite static $PSRR^+$ may arise from the higher order

effects in g_m and g_o in reality. Fig. 3.12 shows the simulated V_{PTAT} and PSRR(DC)$^+$ versus supply voltage at room temperature for the low-voltage PTAT reference. From Fig. 3.12 we can observe that the static PSRR$^+$ is improved significantly. For PSRR(DC)$^+$ > 40 dB, the minimum supply voltage is 1.1 V and the PSRR$^+$ is greater than 70 dB for V_{DD} = 1.5 V.

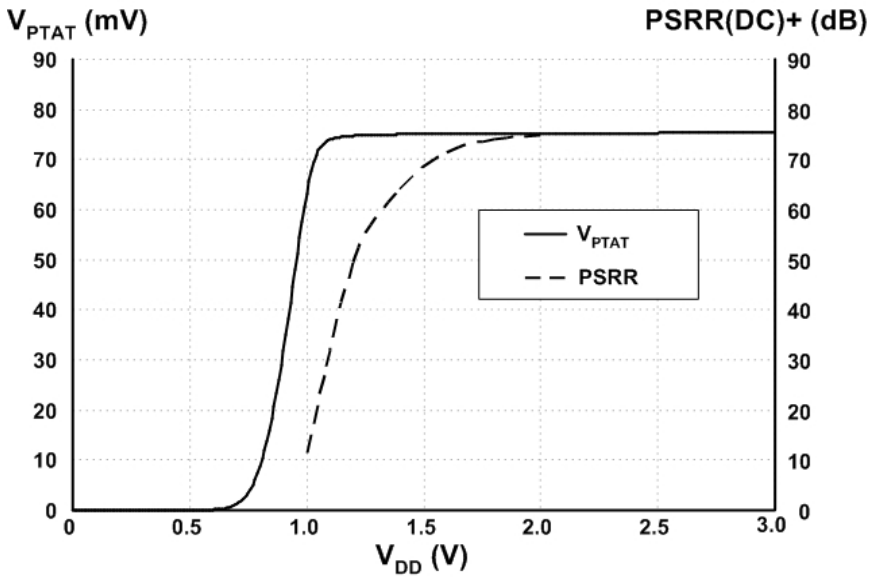


Figure 3.12 Simulated V_{PTAT} and static PSRR$^+$ versus supply voltage at room temperature for the low-voltage PTAT reference shown in Fig. 3.10.

3.3.2 Accuracy

The use of ORA in the low-voltage PTAT reference may lead to a larger spread of V_{PTAT} due to the extra current mirrors. Defining average and mismatch quantities, we have

$$\begin{aligned} V_{t0} &= \frac{V_{t0,1} + V_{t0,2}}{2} \\ DV_{t0} &= V_{t0,1} - V_{t0,2} \end{aligned} \tag{3.31}$$

$$\begin{aligned} b_1 &= S_1 \cdot b_{w1} \\ b_2 &= S_2 \cdot b_{w2} \\ b_w &= \frac{b_{w1} + b_{w2}}{2} \\ Db_w &= b_{w1} - b_{w2} \end{aligned} \tag{3.32}$$

$$\begin{aligned} b_3 &= S_3 \cdot b_{n3} \\ b_4 &= S_4 \cdot b_{n4} \\ b_n &= \frac{b_{n3} + b_{n4}}{2} \\ Db_n &= b_{n3} - b_{n4} \end{aligned} \tag{3.33}$$

$$b_{5-8} = S_{5-8} \cdot b_{p5-8}$$
$$b_{p5-8} = b_p \pm \frac{Db_p}{2} \tag{3.34}$$

Applying this set of equations in the derivation of V_{PTAT}, we obtain

$$\begin{aligned} V_{PTAT} &\approx U_t \cdot \left[ln\left(\frac{S_1}{S_2} \cdot \frac{S_3}{S_4} \cdot \frac{S_7}{S_6} \cdot \frac{S_5}{S_8} \right) + \frac{Db_n}{b_n} + \frac{2 \cdot Db_p}{b_p} + \frac{Db_w}{b_w} \right] - \frac{DV_{t0}}{n} \\ &= V_{PTAT,ideal} + U_t \cdot \left(\frac{Db_n}{b_n} + \frac{2 \cdot Db_p}{b_p} + \frac{Db_w}{b_w} \right) - \frac{DV_{t0}}{n} \end{aligned} \tag{3.35}$$

In this circuit, the V_{PTAT} variation due to current factor mismatch in strong inversion is approximately three times as large as that in conventional MOS PTAT circuits.

3.3.3 Circuit Compensation

The low-voltage MOS PTAT reference has two feedback paths and may require proper compensation. Consider the open-loop circuit shown in Fig. 3.13. The first feedback path consists of a common-source stage with source degeneration and a current mirror. Therefore, the small-signal current i_1' can be expressed as

$$i_1' = \frac{g_{m1} \cdot r_{o1} \cdot v_i}{r_{o1} + \left[1 + (g_{m1} + g_{mb1}) \cdot r_{o1}\right] \cdot R} \cdot \frac{S_7}{S_8} \tag{3.36}$$

The second path consists of a common-source stage and two current mirrors and the small-signal current i_2' is given by

$$i_2' = g_{m2} \cdot v_i \cdot \frac{S_6}{S_5} \cdot \frac{S_4}{S_3} \tag{3.37}$$

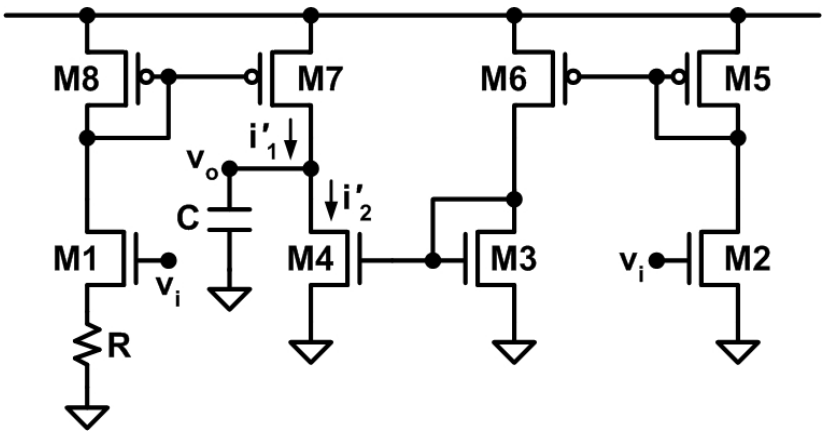


Figure 3.13 Open-loop circuit of the low-voltage MOS PTAT reference.

The small-signal gain v_o / v_i is thus

$$A_0 = \frac{v_o}{v_i} = -\frac{i_2' - i_1'}{v_i} \cdot (r_{o4} \,||\, r_{o7}) \tag{3.38}$$

If $S_3 = S_4$, $S_6 = S_7$, and $S_5 = P \cdot S_8$, then A_0 becomes

$$A_0 = -g_{m1} \cdot \frac{S_6}{S_8} \cdot \left(1 - \frac{r_{o1}}{r_{o1} + [1 + (g_{m1} + g_{mb1}) \cdot r_{o1}] \cdot R} \right) \cdot (r_{o4} \,||\, r_{o7}) \tag{3.39}$$

In general, $(g_{m1} + g_{mb1}) \cdot r_{o1} >> 1$ and the above equation can be rewritten as

$$A_0 = -g_{m1} \cdot \frac{S_6}{S_8} \cdot \frac{(g_{m1} + g_{mb1}) \cdot R}{1 + (g_{m1} + g_{mb1}) \cdot R} \cdot (r_{o4} \,||\, r_{o7}) \tag{3.40}$$

The dominant pole is located at the output node and is given by

$$p_1 = \frac{1}{(r_{o4} \,||\, r_{o7}) \cdot C} \tag{3.41}$$

Therefore, the gain-bandwidth product can be expressed as

$$w_{GB} = \frac{g_{m1}}{C} \cdot \frac{(g_{m1} + g_{mb1}) \cdot R}{1 + (g_{m1} + g_{mb1}) \cdot R} \cdot \frac{S_6}{S_8} \tag{3.42}$$

Values of g_{m1} and C must be designed so that the gain-bandwidth product is well below the other poles arising from parasitic capacitances. Fig. 3.14 shows the simulated frequency response of the open-loop circuit for three values of g_{m1} / C. The unit-gain frequency is found proportional to g_{m1} / C as described in Equation 3.42.

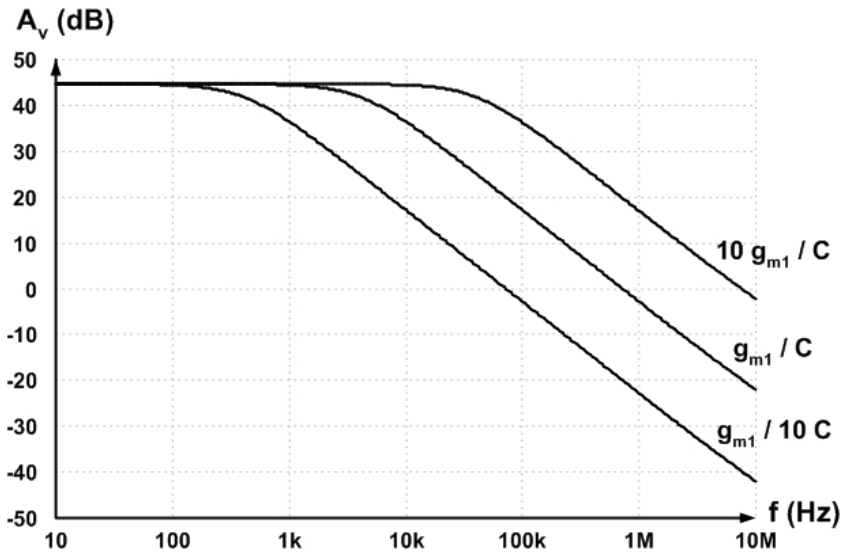
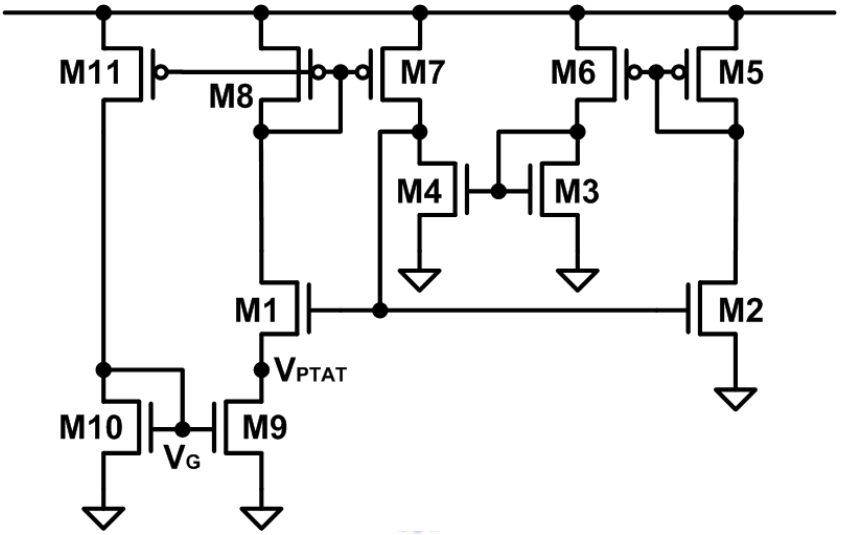


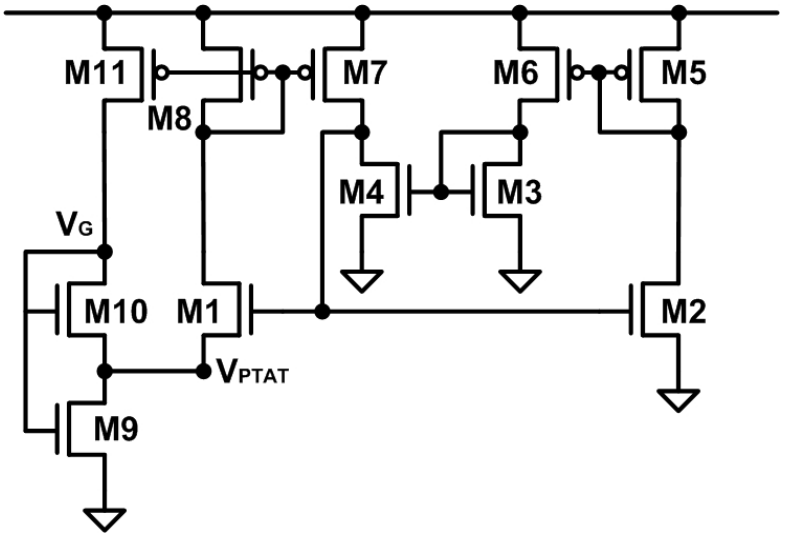
Figure 3.14 Frequency response of the open-loop circuit shown in Fig. 3.13.

3.3.4 All-MOS Implementations

The presence of the resistor may be a drawback in a low-voltage MOS PTAT reference. For an extremely low bias current, a high value resistance is required which takes a large surface area. The resistivity is also not guaranteed by some foundries and may vary with technology. The resistor of the PTAT generator in Fig. 3.10 can be replaced by a MOSFET working below saturation [13], [29]. Fig. 3.15 depicts the all-MOS implementations for the low-voltage PTAT reference. In both circuits, transistor M9 operates in the strong inversion conduction mode while M10 and M11 are in the strong inversion saturation mode.



(a)



(b)

Figure 3.15 Low-voltage MOS PTAT references with all-MOS implementation.

The drain currents of M9 and M10 are given by [15]

$$I_{D9} = b_9 \cdot \left(V_G - V_{t0} - \frac{n}{2} \cdot V_{PTAT} \right) \cdot V_{PTAT}$$
$$I_{D10} = \frac{1}{2 \cdot n} b_{10} \cdot (V_G - V_{t0})^2 \tag{3.43}$$

For the circuit in Fig. 3.15(a),

$$\frac{I_{D9}}{I_{D10}} = \frac{I_{D8}}{I_{D11}} = \frac{S_8}{S_{11}} \tag{3.44}$$

Substituting Equation 3.43 into Equation 3.44 and solving for V_G- V_{t0}, we obtain

$$V_G - V_{t0} = n \cdot V_{PTAT} \cdot \left(K + \sqrt{K \cdot (K-1)} \right) \tag{3.45}$$

where

$$K = \frac{S_9}{S_{10}} \cdot \frac{S_{11}}{S_8} \tag{3.46}$$

Therefore, the drain current of M9 in Fig. 3.15(a) is

$$I_{D9} = I_{D1} = b_9 \cdot n \cdot V_{PTAT}^2 \cdot \left(K - \frac{1}{2} + \sqrt{K \cdot (K-1)} \right) \tag{3.47}$$

For given values of V_{PTAT} and I_{D1}, the transistor size S_9 can be evaluated from Equation 3.47.

Similarly, the drain current of M9 in Fig. 3.15(b) can also be obtained in the same way. Assume that $S_{10} = N \cdot S_9$ and $S_{11} = M \cdot S_8$, then

$$\frac{I_{D9}}{I_{D10}} = 1 + \frac{1}{M} \tag{3.48}$$

The drain current of M9 in Fig. 3.15(b) can therefore be derived to

$$I_{D9} = (1+M) \cdot I_{D1} = b_9 \cdot n \cdot V_{PTAT}^2 \cdot \left[\frac{M}{N \cdot (1+M)} \cdot \left(1 + \sqrt{1 + N + \frac{N}{M}} \right) + \frac{1}{2} \right] \tag{3.49}$$

Also, for given values of the PTAT voltage and the bias current, the transistor size S_9 can be determined.

3.4 Leakage Currents and Proposed Compensation Technique

There are at least three essential requirements for the PTAT reference in an on-chip temperature sensor: i) the circuit must exhibit the best compatibility against process scaling, ii) the supply voltage should be compatible with the complete system-on-chip, and iii) the PTAT signal must be linear over a wide range of temperature. The low-voltage PTAT generators described in the previous section fulfill the first two requirements for a complete temperature sensor. However, these circuits suffer from the nonlinearity problem if the temperature is higher than 100°C. This nonlinear behavior mainly results from the junction leakage currents in MOS transistors at high temperature. In this section, we first discuss the effect of leakage currents and then a compensation technique is proposed to enhance the linearity of high temperature behavior.

In the CMOS structure, the source/drain implants and the substrate (or the *n*-well) form the *pn* junction diodes and may conduct leakage currents in the devices. Fig. 3.16 illustrates the leakage currents through the junction diodes in MOS transistors. These leaky diodes are generally reverse-biased since the bulk of *n*-channel MOSFETs is tied to the ground and that of *p*-channel MOSFETs to the most positive supply voltage. The leakage current which is the reverse-bias saturation current of the diode is associated with the doing concentrations and is strongly dependent on temperature.

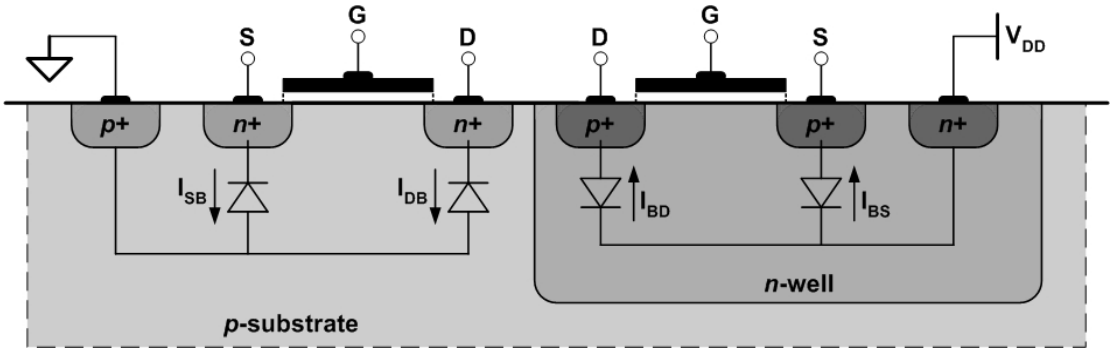


Figure 3.16 The leaky junction diodes in MOS transistors.

At room temperature, these leaky diodes conduct almost no current and do not influence the operation of transistors. However, the leakage current increases sharply in high temperature and degrades the performance of analog circuits. Fig. 3.17 shows the leakage current versus temperature in a 0.25-*m*m CMOS process. Leakage currents

in both *n*-channel and *p*-channel MOSFETs with different channel widths and lengths are plotted in this figure. The leakage current is found slightly dependent on the channel length and proportional to the gate width since the current in a diode is proportional to its area. Furthermore, *n*-channel MOSFETs have larger leakage currents due to the lower channel doping concentration.

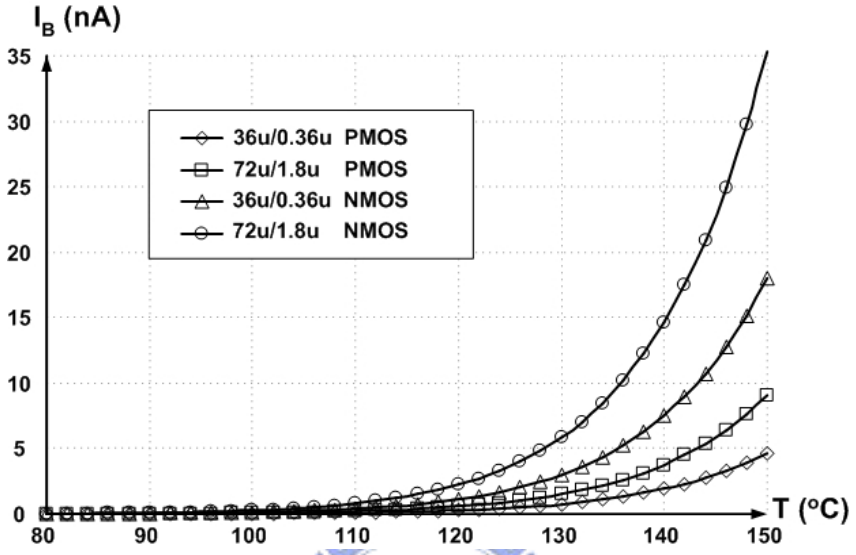


Figure 3.17 Leakage current versus temperature.

Due to the extremely low current in weak inversion, the leakage current becomes comparable to the current level in a MOS PTAT generator. Fig. 3.18 shows the V_{PTAT} curves of the circuit in Fig. 3.15(a) with different values of I_{D1}. For smaller bias current level, the influence of leakage currents on the PTAT voltage is more severe.

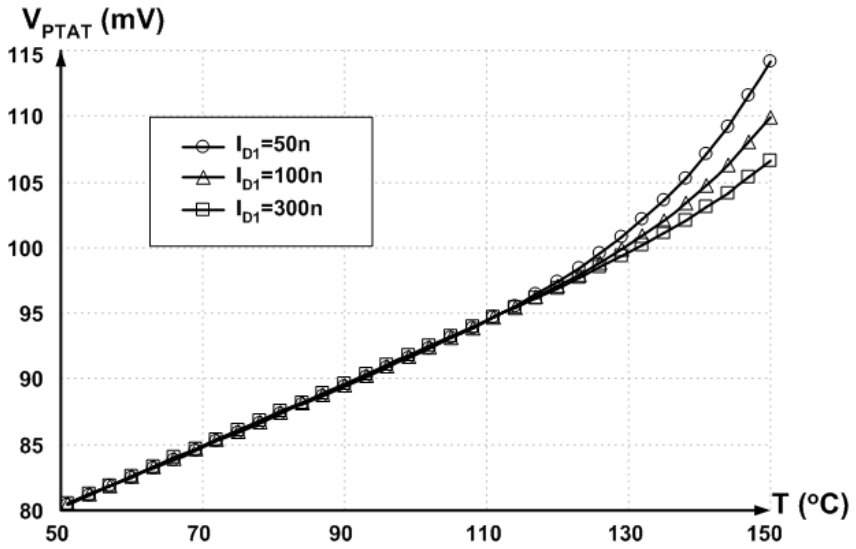


Figure 3.18 V_{PTAT} curves of the circuit in Fig. 3.15(a) with different I_{D1}.

Consider the MOS PTAT reference shown in Fig. 3.15(a). As described before, the PTAT voltage V_{PTAT} is determined by the product of transistor size ratio S_1/S_2 and current ratio I_{D2}/I_{D1}. Taking the leakage currents into account in high temperature, the expression of V_{PTAT} becomes

$$V_{PTAT} = U_t \cdot ln\left[\frac{S_1}{S_2}\cdot\frac{I_{D5}(T)+I_{BD5}(T)-I_{DB2}(T)}{I_{D8}(T)+I_{BD8}(T)-I_{DB1}(T)}\right] \tag{3.50}$$

where $I_{DB1}(T)$, $I_{DB2}(T)$, $I_{BD5}(T)$, and $I_{BD8}(T)$ are leakage currents in M1, M2, M5, and M8 respectively. Since the leakage currents in M3-M8 are balanced,

$$\frac{I_{D5}(T)+I_{BD5}(T)}{I_{D8}(T)+I_{BD8}(T)} = \frac{I_2(T)}{I_1(T)} = \frac{S_3}{S_4}\cdot\frac{S_7}{S_6}\cdot\frac{S_5}{S_8} \equiv P \tag{3.51}$$

where $I_1(T) = I_{D1}(T) + I_{DB1}(T)$ and $I_2(T) = I_{D2}(T) + I_{DB2}(T)$. Substituting Equation 3.51 into Equation 3.50 with $S_1 = S_2$ gives

$$\begin{aligned} V_{PTAT} &= U_t \cdot ln\left[\frac{I_2(T)}{I_1(T)}\cdot\frac{1-I_{DB2}(T)/I_2(T)}{1-I_{DB1}(T)/I_1(T)}\right] \\ &= U_t \cdot ln\,P - U_t \cdot ln\left[\frac{1-I_{DB1}(T)/I_1(T)}{1-I_{DB1}(T)/P\cdot I_1(T)}\right] \end{aligned} \tag{3.52}$$

The last term in the above equation is the non-PTAT term. If $I_{DB1}(T)/P{\cdot}I_1(T) << 1$, this nonlinear term can be rewritten as

$$e(T) \equiv U_t \cdot ln\left[\frac{1-I_{DB1}(T)/I_1(T)}{1-I_{DB1}(T)/P\cdot I_1(T)}\right] \approx U_t \cdot ln\left[1-\frac{I_{DB1}(T)}{I_1(T)}\cdot\left(1-\frac{1}{P}\right)\right] \tag{3.53}$$

Fig 3.19 shows the nonlinearity of PTAT voltage in the circuit shown in Fig. 3.15(a).

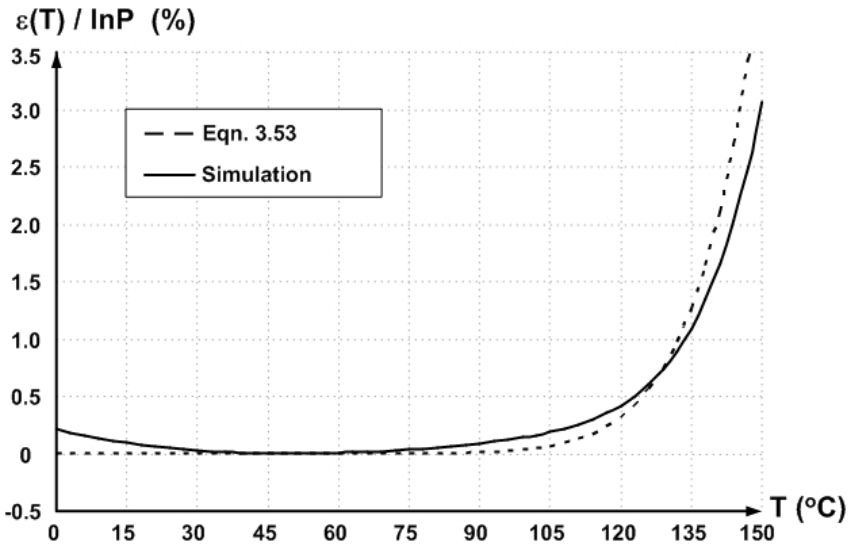


Figure 3.19 Nonlinearity of the PTAT voltage in the circuit show in Fig. 3.15(a).

From Fig. 3.19 we can observe that the nonlinear behavior in high temperature primarily results from the leakage currents and it can be described by Equation 3.53.

The nonlinearity behavior is a crucial effect to implement a complete thermal management system within a digital circuit since such circuitry requires more effort and cost for after process calibration. As a result, solutions for improving the linearity of high temperature behavior are necessary. Fig. 3.20 depicts the schematic of all-MOS PTAT reference with leakage compensation. Compensation transistors M_{C1} and M_{C2} are attached to the drain terminals of M1 and M2 respectively. The effects of leakage currents in M3-M8 are eliminated since the leakage currents are proportional to device sizes and thus are all balanced in these transistors. At room temperature, the two compensation transistors M_{C1} and M_{C2} do not interfere with normal operation of the circuit since the gate of M_{C1} is connected to V_{DD} and that of M_{C2} to the ground. In high temperature, additional leakage currents come from M_{C1} and M_{C2} will compensate the leakage currents in M1 and M2 as illustrated in Fig. 3.20.

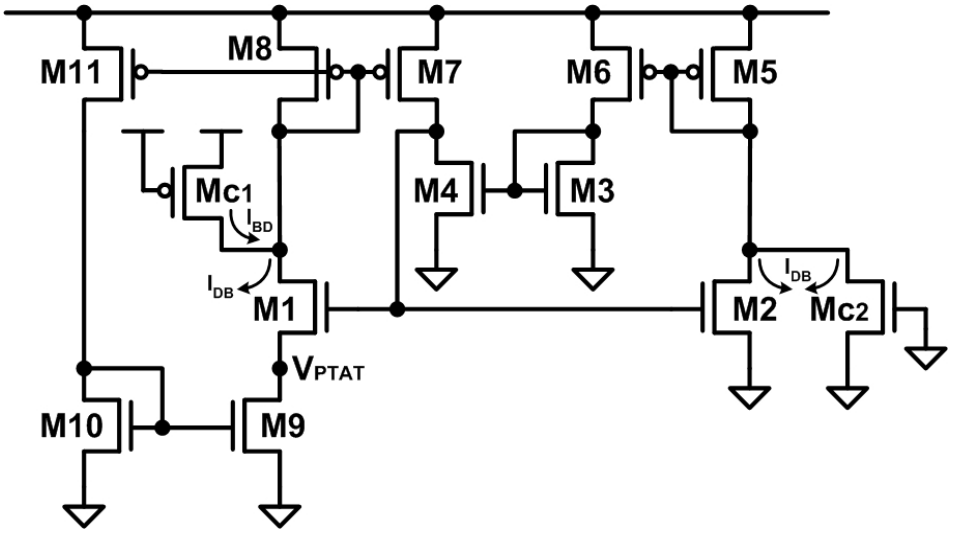


Figure 3.20 All-MOS PTAT reference with leakage compensation.

Fig. 3.21 presents the simulated temperature characteristics of V_{PTAT} for all-MOS and compensated PTAT references. The linearity at high temperature is improved significantly in the proposed compensated PTAT reference. From this figure we can observe that the PTAT circuit with compensation may extend the temperature range at least 30°C.

The MOS PTAT reference with leakage current compensation can exhibit the best compatibility against supply scaling in deep-submicron technology. The power consumption is also made minimum due to the inherently low currents in subthreshold

MOSFETs. Furthermore, the PTAT signal exhibits high linearity over a wide range of temperature. Hence, the proposed compensation technique allows the integration of PTAT references in deep-submicron technology for complete temperature sensors.

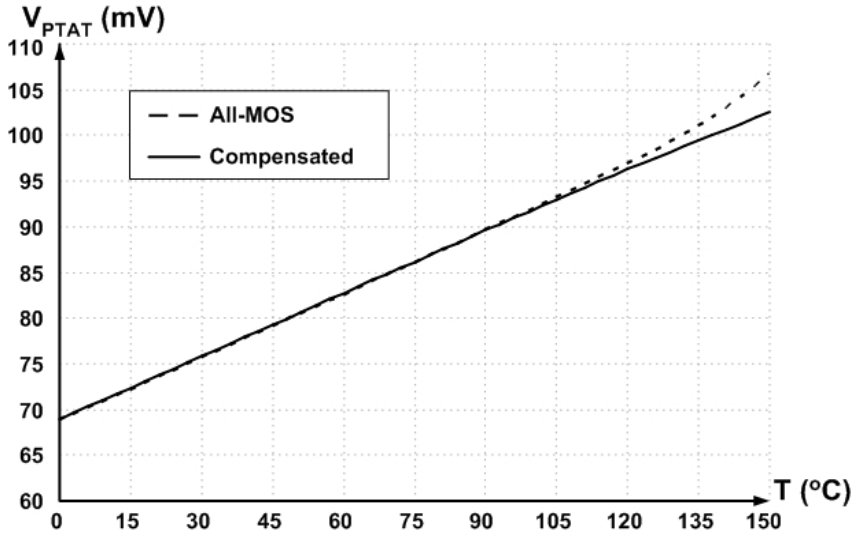


Figure 3.21 Simulated V_{PTAT} versus temperature for all-MOS and compensated PTAT references.

CHAPTER 4

IMPLEMENTATION OF CMOS PTAT REFERENCES

Experimental implementations of the MOS PTAT references including leakage-compensated circuit have been fabricated in TSMC 0.25-*m*m double-poly five-metal CMOS process. Design issues as well as layout considerations of the MOS PTAT references are thoroughly discussed in this chapter. Following the description of test setup, the experimental results are presented and discussed. The characteristics of experimental PTAT references are summarized in the end of this chapter.

4.1 Realization

In order to demonstrate the applicability of the proposed leakage compensation technique, so as to implement the competitive temperature sensors in deep-submicron technology, three MOS PTAT references are designed and implemented in a 0.25-*m*m CMOS technology. In this section, implementation issues of the experimental PTAT references are described in detail.

The first implemented circuit is the resistor-based MOS PTAT reference which has been discussed in Chapter 3. The schematic is redrawn in Fig. 4.1. The circuit is designed to exhibit an output voltage of about 60 mV at room temperature. Device sizes of M1 and M2 which operate in weak inversion are set to equal for matching consideration. As a result, the current ratio I_{D2}/I_{D1} = 10 is chosen here to generate the required V_{PTAT}. It is important for M1 and M2 to operate in weak inversion region. Therefore, the current gain factors of the two transistors have to be larger than the value corresponding to the limit of weak inversion region [12]:

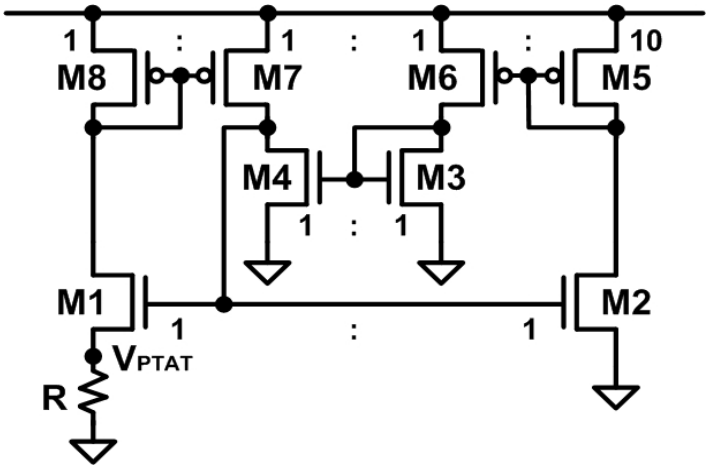


Figure 4.1 The R-based MOS PTAT reference.

$$b_{1,2} = S_{1,2} \cdot m_n \cdot C'_{ox} >> \frac{I_{D1,2}}{U_t^2} \tag{4.1}$$

The minimum value of $S_{1,2}$ ensuring subthreshold operation can thus be calculated from this relation. With $m_n \cdot C'_{ox}$ = 150 mA／V^2 in this 0.25-mm technology, $S_{1,2}$ > 100 is required for the drain currents of few microamperes. In the circuit, the gate voltage of M1-M2 pair is design to be well below the threshold voltage and the current I_{D1} is chosen as 300 nA. Using Equation 2.23 along with the extracted parameters, I_0 and n, a value of about 140 for $S_{1,2}$ can be obtained. In addition, a resistor $R \approx 200$ kΩ is required for this bias current.

An important aspect of the performance of the PTAT reference is its accuracy. As discussed in Chapter 3, the variance of the relative variation in the PTAT voltage can be expressed as

$$\frac{s^2(DV_{PTAT})}{V_{PTAT}^2} = \frac{U_t^2}{V_{PTAT}^2} \cdot \left[\frac{s^2(Db_n)}{b_n^2} + 2 \cdot \frac{s^2(Db_p)}{b_p^2} + \frac{s^2(Db_w)}{b_w^2} \right] + \frac{s^2(DV_{t0})}{(n \cdot V_{PTAT})^2} \tag{4.2}$$

Applying the Pelgrom model described in Equation 2.28 to the mismatch parameters, the above equation can be rewritten as

$$\frac{s^2(DV_{PTAT})}{V_{PTAT}^2} = \frac{U_t^2}{V_{PTAT}^2} \cdot \left[\frac{A_{b_n}^2}{(W \cdot L)_{3,4}} + \frac{2 \cdot A_{b_p}^2}{(W \cdot L)_{6,7}} + \frac{A_{b_w}^2}{(W \cdot L)_{1,2}} \right] + \frac{1}{(n \cdot V_{PTAT})^2} \cdot \frac{A_{V_{t0}}^2}{(W \cdot L)_{1,2}} \tag{4.3}$$

Values of these proportionality constants in a 0.35-mm technology are: A_{bn} = 1.9 %·mm, A_{bp} = 2.25 %·mm, and A_{Vt0} = 9 mV·mm [31]. In general, the accuracy of the

PTAT voltage is dominated by the threshold voltage mismatch. For relative deviations $(DV_{PTAT}/V_{PTAT}) \le 5\%$, which corresponds to $\sigma(DV_{PTAT}/V_{PTAT}) \le 2.5\%$ when a 2σ law is used, the required device area for the M1-M2 pair $(W \cdot L)_{1,2} = 16\ \mu m^2$ is obtained.

To minimize the current mismatch in current mirrors, transistors M3-M8 are designed to operate in deep strong inversion. Device sizes of M3 and M6 are designed identical to those of M4 and M7 respectively for matching consideration. Furthermore, the drain currents in M7 and M8 are also designed equal to reduce the power consumption. Designing the overdrive V_{ov} = 150 mV for all transistors in strong inversion, the device sizes of M3-M8 can be roughly obtained from square law:

$$S_{3-8} = \frac{2 \cdot I_{D3-8}}{\mu \cdot C_{ox}' \cdot V_{ov}^2} \tag{4.4}$$

The values of $\mu \cdot C_{ox}'$ for NMOS and PMOS in this 0.25-μm technology are about 150 $\mu A/V^2$ and 40 $\mu A/V^2$ respectively.

The other two experimental circuits are all-MOS and compensated all-MOS PTAT references. The condensed scheme of these two circuits is shown in Fig. 4.2. In the all-MOS implementation, the PTAT core, M1-M2, and the ORA, M3-M8, are all designed identical to those in the R-based PTAT reference. The transistor sizes of M9-M11 are derived from Equation 3.49 and from power considerations: M = 1 and N = 1.5. In the compensated version, an n-channel MOSFET is used for matching consideration.

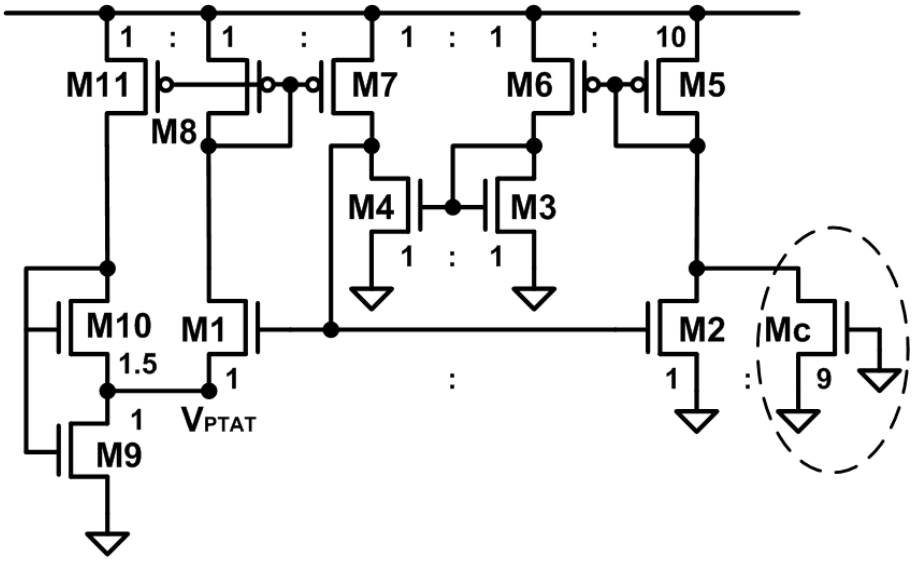


Figure 4.2 All-MOS and compensated all-MOS PTAT references.

According to the discussions above, the transistor aspect ratios are summarized in Table 4.1 for the three experimental circuits.

Table 4.1 MOS PTAT references component values.

R-based		**All-MOS**		**Compensated**	
Component	Value	Component	Value	Component	Value
M1, M2	48／0.36	M1, M2	48／0.36	M1, M2	48／0.36
M3, M4	0.6／2.8	M3, M4	0.6／2.8	M3, M4	0.6／2.8
M5	6.4／0.6	M5	6.4／0.6	M5	6.4／0.6
M6-M8	0.64／0.6	M6-M8, M11	0.64／0.6	M6-M8, M11	0.64／0.6
R	245.6 kΩ	M9	0.6／2	M9	0.6／2
		M10	0.6／2.8	M10	0.6／2.82
				Mc	432／0.36

Figs. 4.3-4.6 present the simulation results of these three experimental circuits. Fig. 4.3 shows the PTAT voltage versus supply voltage at room temperature. In this figure, curves for all-MOS and compensated all-MOS PTAT references are the same.

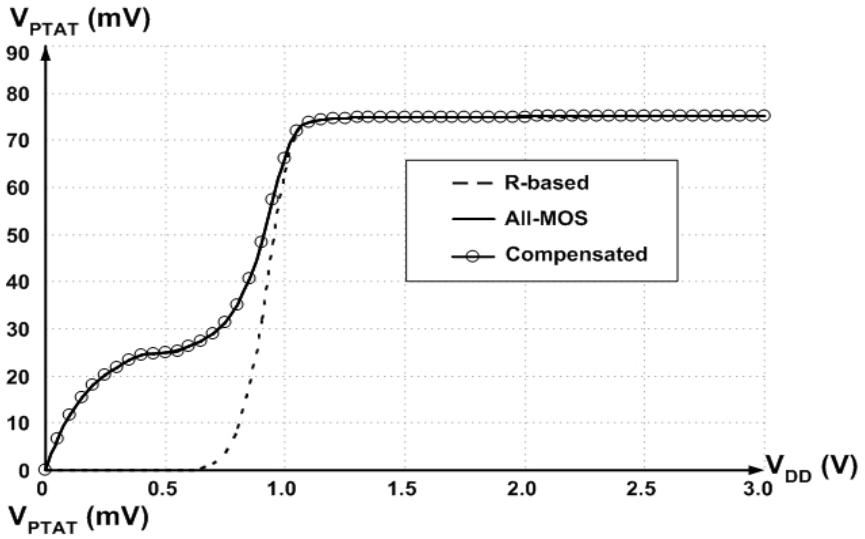


Figure 4.3 Simulated V_{PTAT} versus V_{DD} at room temperature.

Fig. 4.4 presents the temperature characteristics of these PTAT references. The R-based and all-MOS versions have similar temperature behavior and they both encounter nonlinearity problem in high temperature.

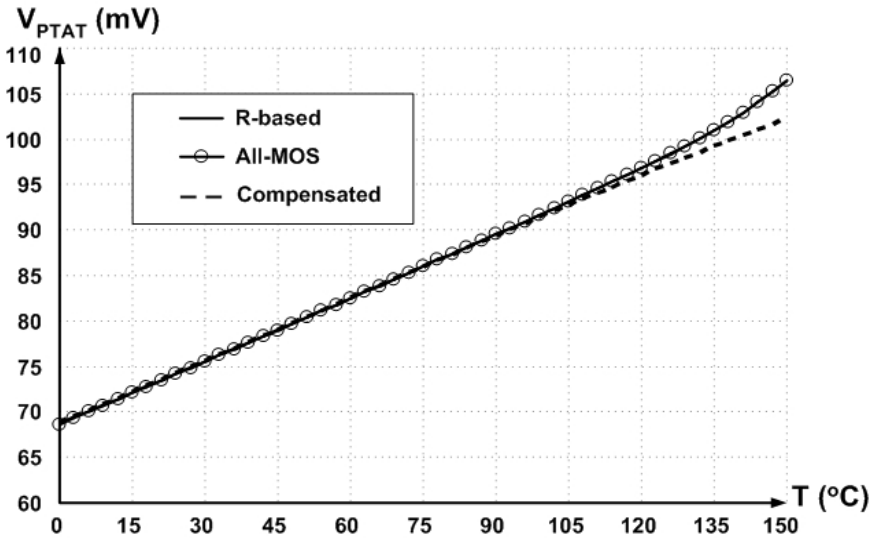


Figure 4.4 Simulated V_{PTAT} versus temperature.

The V_{PTAT} histogram plots for R-based and all-MOS PTAT references are shown in Fig. 4.5 and Fig. 4.6 respectively. The result of the compensated circuit is quite similar to that of the all-MOS version and is not shown for simplicity.

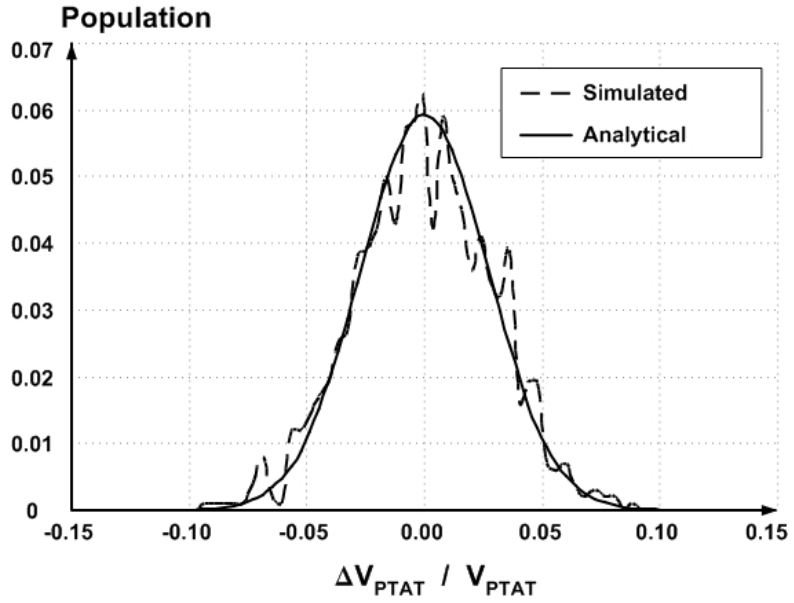


Figure 4.5 V_{PTAT} histogram at room temperature from 1000 Monte Carlo runs for the R-based PTAT reference.

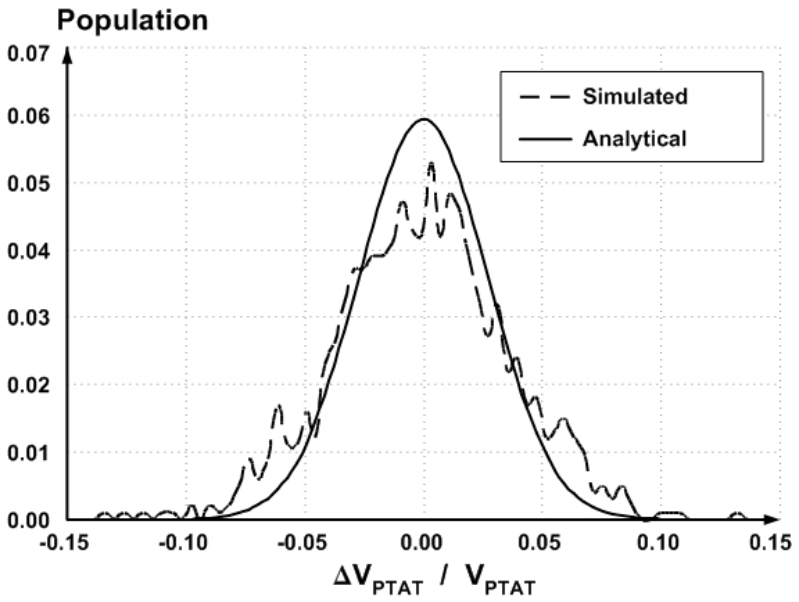


Figure 4.6 V_{PTAT} histogram at room temperature from 1000 Monte Carlo runs for the all-MOS PTAT reference.

Since the PTAT voltage is sensitive to the device mismatch, a good layout should group the transistors in the following manner:

Group N1: M1, M2, and Mc (weak inversion)

Group N2: M3 and M4 (strong inversion)

Group N3: M9 and M10 (strong inversion)

Group P: M5-M8, M11 (strong inversion)

In each group, the transistors are in the same orientation and have the minimum separation allowed in design rule. The most important devices in the PTAT references are the subthreshold MOSFETs M1 and M2. They are decomposed into identical unit transistors of exactly the same geometry and these unit transistors are interleaved and have a common centroid.

The experimental chip is fabricated in TSMC 0.25-*m*m single-poly five-metal CMOS technology. The resistor in the R-based circuit is implemented by the *p*+ poly resistor for resistivity and temperature coefficients considerations. Fig. 4.7 shows the microphotographs of the R-based and the compensated all-MOS circuits. The right side of the compensated circuit is the all-MOS PTAT reference. Surface areas for R-based, all-MOS, and compensated circuits are about 10,000 mm^2, 900 mm^2, and 2000 mm^2 respectively.

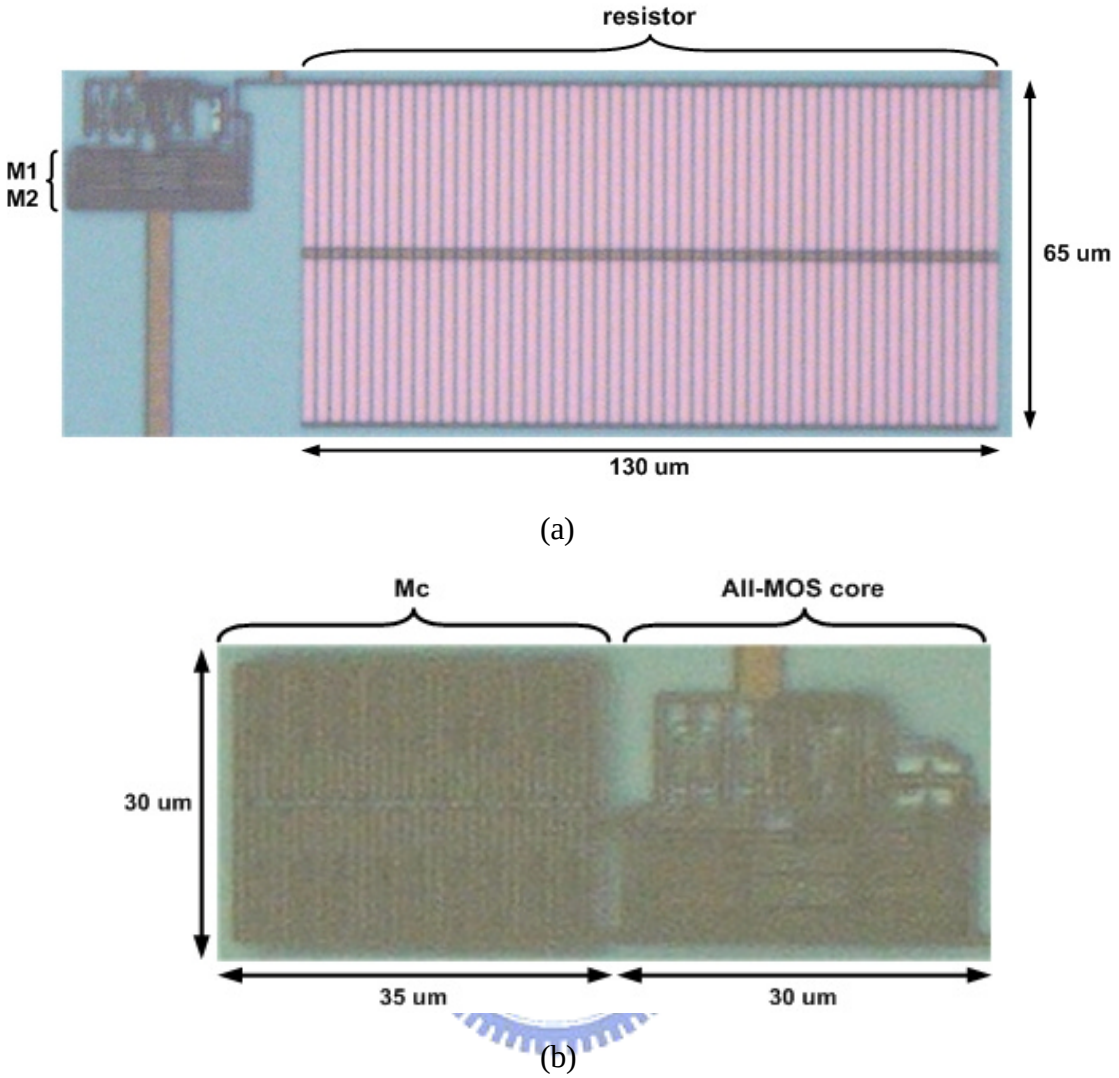


Figure 4.7 Microphotographs of (a) R-based and (b) compensated all-MOS PTAT references.

4.2 Measurement Setup

Fig. 4.8 depicts the measurement setup used to access the performance of the experimental PTAT references. A PCB which combines a voltage regulator and the DUT is designed to measure the temperature characteristics of the chip in a thermal bath. The chip temperature is monitored by a thermocouple tied closed to the die and measured by the thermometer. The output PTAT voltage of the DUT is fed to the Agilent 54622A oscilloscope.

The supply voltage is generated by LM317 adjustable regulator and a 9 V battery as shown in Fig. 4.9. We use the 9 V battery for better power supply noise. Moreover,

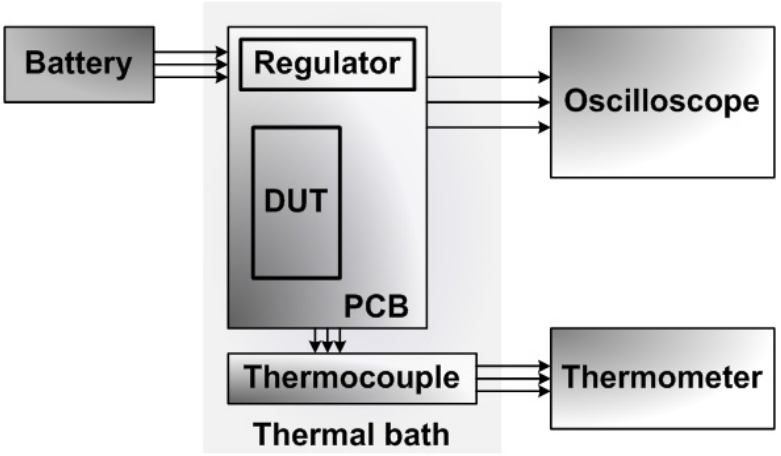


Figure 4.8 Measurement setup.

the voltage regulator output is connected to the parallel combination capacitors to provide decoupling of both low frequency noise with large amplitude and high frequency noise with small amplitude.

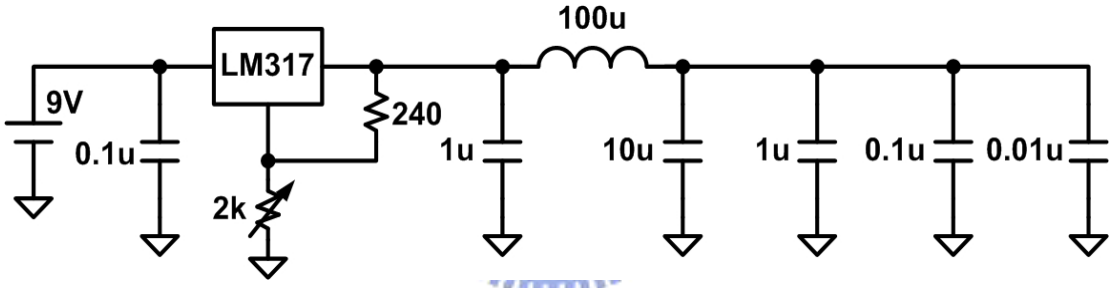


Figure 4.9 The voltage regulator with bypass filter.

Figs. 4.10 and 4.11 show the photographs of the PCB and the measurement environment respectively. The experimental results will be presented in the following section.

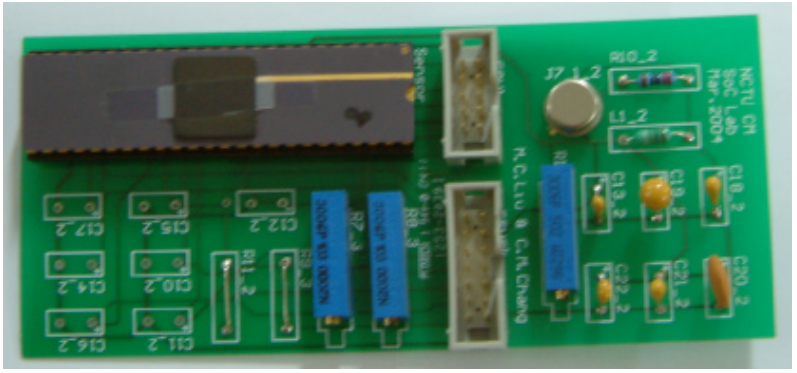


Figure 4.10 Photograph of the PCB.

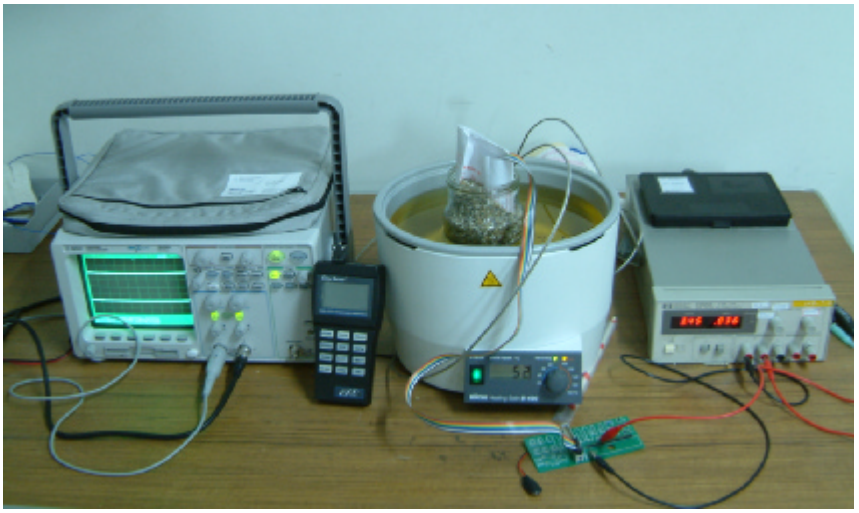


Figure 4.11 The measurement environment.

4.3 Experimental Results

The output voltages of the experimental PTAT references are measured by an oscilloscope. Table 4.2 lists the measured PTAT voltages for each circuit at room temperature. A fairly large spread in voltage values of about 15% is observed. This is likely because the mismatches in subthreshold MOSFETs and small transistors are larger than the predicted values from Pelgrom model.

Fig. 4.12 shows the PTAT voltage versus temperature for all-MOS and compensated PTAT references. The dashed lines are the regressions of measured data from 35°C to 95°C for each circuit. The V_{PTAT} curve of the all-MOS version deviates from the straight line when temperature is above 95°C. The R-squares of all-MOS and compensated circuits are 0.994 and 0.868 respectively. The temperature behavior of the R-based PTAT generator is similar to the all-MOS version and is shown in Fig. 4.13. Its R-square is only 0.79.

Table 4.2 Measured PTAT voltage at room temperature.

		Avg.	Max.	Min.	Variation
V_{PTAT} (mV)	**R-based**	70.01	74.65	61.12	12.64%
	All-MOS	63.67	71.38	59.14	12.11%
	Compensated	43.77	50.22	39.43	14.74%

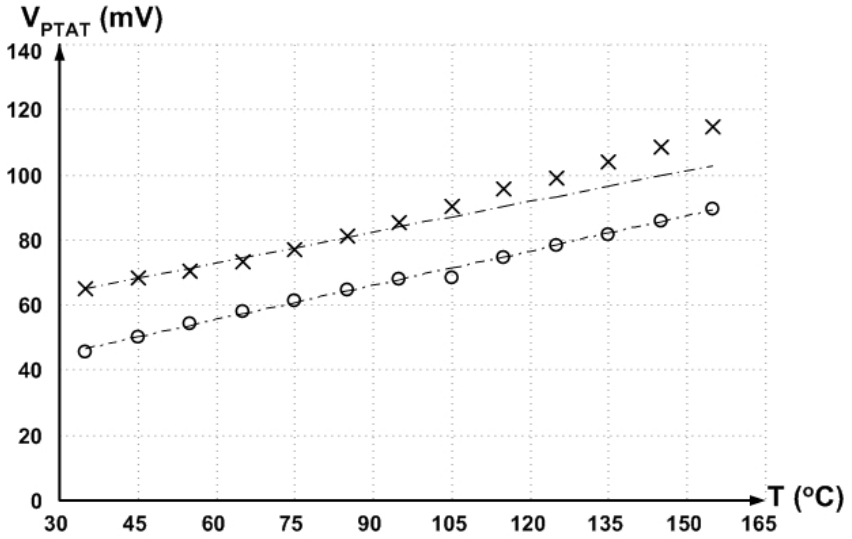


Figure 4.12 Measured PTAT voltage versus temperature for all-MOS (crosses) and compensated (circles) PTAT references.

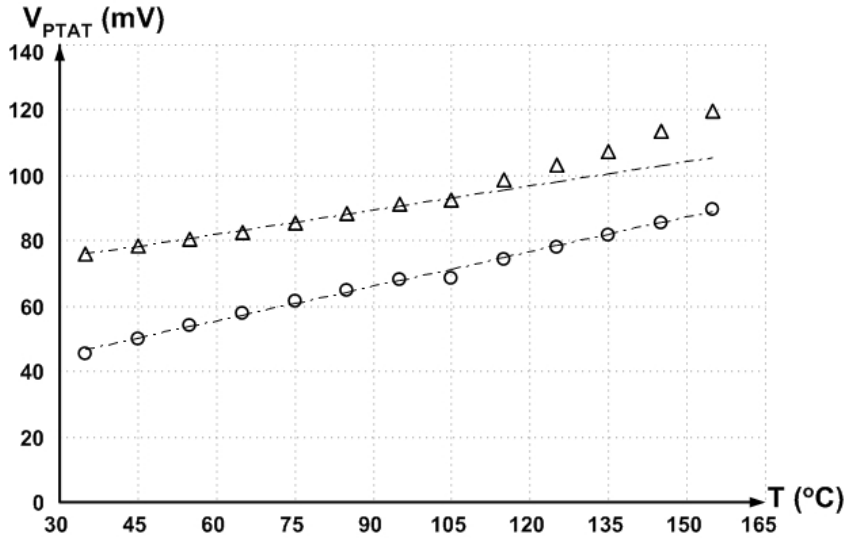


Figure 4.13 Measured PTAT voltage versus temperature for R-based (triangles) and compensated (circles) PTAT references.

Fig. 4.14 shows the spread of V_{PTAT} for the compensated PTAT reference. The offset comes from the process variation and is dominated by the threshold voltage mismatch DV_{t0} as described in section 4.1. Since DV_{t0} is insensitive to temperature, the offset of PTAT voltages is almost a constant in the whole temperature range. Therefore, the offset error can be easily calibrated by other circuits in the thermal management system.

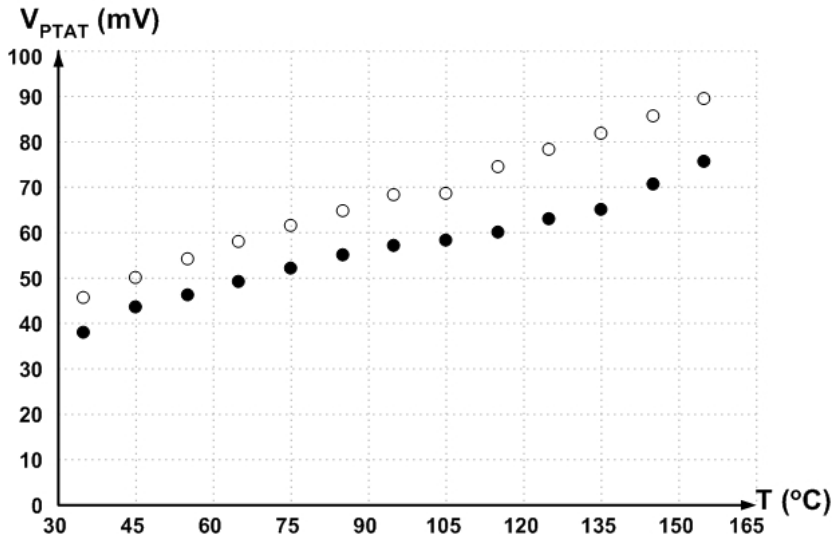


Figure 4.14 The spread of measured PTAT voltages for the compensated PTAT reference.

4.4 Summary

This chapter described in detail the implementation of MOS PTAT references in a 0.25-*m*m CMOS process and presented the experimental results. The experimental results show that the PTAT reference without compensation has severe nonlinearity problem in high temperature. The linearity is improved significantly in the proposed compensated circuit and the operating temperature range of this circuit can be extended to at least 155°C. A large spread of V_{PTAT} due to process variation is also observed. This is not a relevant problem for our application since the offset can be easily calibrated by digital circuits.

CHAPTER 5

CONCLUSIONS

The utilization of subthreshold MOSFETs has been shown to be an attractive means of implementing low-voltage low-power PTAT references. This thesis has demonstrated the feasibility of using such approach in deep-submicron technology. This work has focused on three major topics: the subthreshold operation of MOS transistors, the analysis and design of the MOS PTAT references, and a leakage compensation technique.

We introduced the analytical subthreshold MOSFET model and the effective approach to link both analytical and accurate models. The simple equation describes the simulated drain current in weak inversion well and the technique, which maps the accurate BSIM to a simple conventional model, makes designs using the weakly inverted MOSFET more efficient.

Analysis of the MOS PTAT references based on the analytical model identified the topology as suitable for low-voltage and low-power applications. Experimental PTAT references based on the analysis presented in this work were designed and integrated in TSMC 0.25-*m*m 1P5M standard CMOS technology. Experimental results confirmed the feasibility of the PTAT circuits in deep-submicron technology. Precautions have to be taken against the large spread of the PTAT voltage.

A pure CMOS PTAT reference, which applied a compensation technique to enhance the linearity of high temperature behavior, has also been implemented in this 0.25-*m*m technology. Testing results showed that the linear range of the voltage output has been expanded to at least 155°C, which implies that the temperature sensor requires calibration only of its offset. Thus, the effort for after process calibration is minimized.

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