國立交通大學

電信工程學系碩士班

碩 士 論 文

使用 0.25μm CMOS 技術製作的一個完全積體化共模三頻帶低雜訊放大器及兩個改良型混頻器電路設計

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中文摘要

在此篇論文研究中，主要探討三個主題；第一個主題是設計一個完全積體化共模三頻帶 CMOS 低雜訊放大器，它的設計理念是來自原本的共模雙頻帶低雜訊放大器，輸入及輸出匹配電路經過改良設計後，可提供在所希望的三個頻段(1.8GHz, 2.45GHz, 5.25GHz)相當好的匹配，結合偏壓電流重新利用技巧的雙級架構，可用來同時達到較高的增益，卻不需大量的功率損耗，除此之外，此電路亦在這三個不同頻率呈現出相當高的線性度；最後，經由模擬及量測結果中，我們驗證了這個設計理念的可行性，並探討其間的差異性。第二個主題是設計一個操作在 2.1GHz 整合低雜訊放大器的雙平衡混頻器電路，此電路架構是將低雜訊放大器和混頻器以電流模式串疊起來，因此可以消去傳統以電壓模式串疊架構之中間節點，並去除相關之線性度瓶頸；此外，此電路亦包含兩種改良機制，第一，加入一對共閘 NMOS 電晶體於共源低雜訊放大器及切換混頻對尾端之間，以提昇 LO 至 RF 之隔絕度，第二，加入一對共源 PMOS 電晶體同時扮演除了可改善線性度、增益及降降雜訊指數之分流源外，也可透過兩個耦合電容來作小訊號共源放大器以提昇增益；同樣的，經由模擬及量測結果中，我們亦驗證了這個設計改良的理念。最後一個主題是設計一個全新的 CMOS 微混頻器，它的設計理念是源自目前的 BJT 微混頻器，一般來說，因為成效不佳的關係，此電路架構並不適合應用在 CMOS 上，但經過改良設計後之新架構，不但可達到相當不錯的成效，且所損耗的功率亦非常低，在新架構中，除了加入一對 LC tank 及一對耦合電容外，亦增加了一對 NMOS 電晶體，它可同時用來當作改善線性度、增益和降低雜訊指數之分流源以及可提昇增益之高頻電流放大器，最後，我們亦經由模擬及量測結果中驗證了這個設計改良的理念。以上三組電路皆已透過 CIC 於台積電以 0.25μm CMOS 技術實現及製作出來，並皆已完成各電路所有參數量測工作，在此篇論文中，我們會在每一個電路設計之最後，針對量測及模擬結果做進一步的比較和討論。

The Design of A Fully Integrated Concurrent Triple-Band LNA and Two Modified Mixer Circuits Fabricated using 0.25um CMOS Technology

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Abstract

This thesis contents three works. First, we design a novel fully integrated concurrent triple-band CMOS LNA. The design idea originates from the concurrent dual-band LNA. The input and output matching circuits have been modified to provide good matching at all desired triple bands (1.8GHz, 2.45GHz, and 5.25GHz). A two-stage topology conjunction with bias-current reuse technique has been used to simultaneously achieve high gain without large amount of power consumption. Besides, it also exhibits high linearity at these three different frequencies. Finally, we have demonstrated this design idea through post simulation and measurement results and discuss the differences between them. The second work is the design of a modified double-balanced mixer merged LNA which can be operated at 2.1GHz. This architecture is a current-mode cascade of LNA and mixer, so that it can eliminate the intermediate node of the conventional voltage-mode cascade architecture and remove the associated bottleneck to linearity. Besides, two kinds of improving mechanisms are included in this circuit. First, a pair of common-gate NMOS transistors is added between common-source LNA and the tail of commutating mixer pair to improve

LO-to-RF Isolation. Second, a pair of PMOS transistors is added to simultaneously act as not only bleeding-current sources to improve linearity, gain, and noise figure but also small signal common-source amplifiers to achieve higher gain through two coupling capacitors. Similarly, we have demonstrated this design idea through post simulation and measurement results. The last work is the design of a new CMOS RF MICROMIXER. The design idea originates from the current BJT counterpart. In general, this topology is unsuited for CMOS applications due to worse performance. But the new topology modified here can achieve better performance with very low power dissipation. In addition to LC tank pair and coupling capacitor pair, a pair of NMOS transistors is also added in the new architecture that can be used as not only bleeding-current sources to improve linearity, gain, and noise figure but high frequency current amplifiers to increase gain. Finally, we also have demonstrated this design idea through post simulation and measurement results. These circuits all have been implemented and fabricated using TSMC 0.25μm CMOS technology through CIC. And then we have completed all parameter measurements for each work. Throughout this thesis, we will make advanced comparison and discussion between measurement and simulation results in the end of each circuit design.

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Chapter 1

Introduction

1.1 Background

In the recent years, the wireless communications have been rapidly progressing and have necessitated their applications with more functionality and flexibility, such as cellular phones from simple AMPS and GSM moving toward to the integration of GPS and GPRS or WLNA from single-standard 802.11a moving toward to multi-standard 802.11a/b/g. These not only have provided people more convenient services but also have made enormous business profits. These benefits also greatly promote the economy along with the openness and competition to the communications market in the worldwide. These keen competitions have urged the large demand of compact, low-cost, good-performance, and high-integration SOC (System-On-a-Chip) solutions. Since only CMOS technology can offer a solution for integration RF and base-band circuits on a chip due to its already mature digital/analog circuit designs, it seems a good candidate for these requirements. In addition, with great development in CMOS process, modern CMOS technology has accommodated for applications at much higher frequency. The modern CMOS transistors already have better performances than before and can be applied to radio frequency, its cut-off frequency as high as 40GHz. In the prospective future, the new systems of wireless communications will be innovated continuously and people of the researches and developments will have to face and overcome more and more challenges, especially for radio frequency part in CMOS technology.

Since highly integrated RF front-end circuits play a significant role in the modern wireless communications, we will focus on various fully integrated CMOS

circuit designs of RF front-end circuits and make advanced detailed researches throughout this thesis. So that this thesis contains three major works, including a novel concurrent triple-band LNA, a modified double-balanced mixer merged LNA, and a new RF MICROMIXER. All of them are fabricated using 0.25um CMOS technology and, of course, can be easily integrated with other blocks in the future to meet the requirements of modern wireless communications. In the subsequent sections, we will describe motivations of our designs, associated recent works, and organization of this thesis.

1.2 Motivations and Associated Recent Works

1.2.1 Concurrent Triple-Band CMOS LNA

Since modern wireless applications necessitate communication systems with more functionality and flexibility, multi-standard RF transceivers integrated using CMOS technology are predicted to play a critical role in the future wireless communication systems. If we can combine two or more RF standards into one receiver, it will greatly reduce cost and improve integration in advanced. However, low noise amplifier is one of the most critical building blocks in modern integrated RF receiver. A suitable multi-band LNA must be designed and realized before implementing a multi-standard receiver. In Chapter 3, we will briefly describe that a concurrent multi-band LNA is the appropriate candidate for such a receiver. [1]

Recently, many researches about concurrent dual-band LNA have been studied and reported. [2-5] However, concurrent triple-band LNA is rarely cited and neither of them is concurrent or fully integrated. So that a novel fully integrated concurrent triple -band CMOS LNA is first proposed in our thesis that is capable of simultaneous

operation at all three different frequency bands (1.8GHz, 2.45GHz, and 5.25GHz) without dissipating triple as much power or significantly increasing in cost and footprint. Besides, it can also be easily integrated on a triple-band receiver.

1.2.2 CMOS Double-Balanced Mixer Merged LNA for WCDMA

The third generation of global wireless cellular systems is based on wide-band code-division multiple access (WCDMA). Direct sequence spread spectrum at 4–16 Mchips/s expands data into 5-MHz-wide channels. The spread data modulates the carrier with quadrature-phase-shift keying (QPSK). The WCDMA handset is full duplex, that is, it transmits in the 1.9-GHz band at the same time as it receives in the 2.1-GHz band. These features pose special challenges in the receiver, such as linearity performance. [6]

We undertake the work present here in search of a more linear RF front-end. Let us start with the shortcomings of the cascade of a conventional LNA and mixer. In Chapter 4, we will briefly describe that an intermediate node exists between the cascade architecture of conventional LNA and Mixer and it will greatly degrade the linearity of whole receiver. If we can eliminate this node, it will remove the associated bottleneck to linearity. [6] So that a CMOS double-balance mixer merged LNA is presented in this thesis, which is a current-mode cascade of LNA and mixer. Since two power-hungry blocks are merged into one, such a merged CMOS LNA and Mixer not only can improve linearity but also can greatly reduce its cost and power consumption. Besides, the circuit presented in this thesis is also fully integrated and it also can be integrated with other blocks easily.

Recently, although some advanced researches of stacked CMOS LNA and Mixer using bias-current reuse technique are proposed to save power [7], however, this

architecture is still a voltage-mode cascade of LNA & Mixer and remains this intermediate node as shown in Fig.1.2.1 (b). Fig. 1.2.1 shows the simplified diagrams of these two different ways of merge LNA and Mixer, and we can see that the current-mode cascade of merged LNA and Mixer theoretically should perform better linearity than voltage-mode one due to elimination of this linearity bottleneck, while both of them have the same advantages of low power and high integration capabilities. Furthermore, to demonstrate this superiority of current-mode cascade architecture in advanced, we also have listed a comparison table as shown in Table. 1.2.1, including two works using these two different approaches and one work we will propose and briefly describe in chapter 4. Obviously, two works in current-mode cascade, [6] and this work, actually can achieve better linearity than that in voltage-mode cascade, [7].

1.2.3 New RF CMOS MCROMIXER

The mixers always play an indispensable role as frequency-translation devices in the RF transceivers of communication systems. It can perform frequency translation to a higher frequency (up-conversion) or to a lower frequency (down-conversion). System integrated monolithic mixers often use a topology called the Gilbert mixer, especially in CMOS technology. However, its RF input stage, usually a simple differential pair or sometimes using source degeneration, sets fundamental limits to the attainable dynamic range. Further, these RF stages do not provide an accurate match to the source, even when using various types of impedance-transformation methods. Accordingly, another topology, named the MICROMIXER, adopts a quite different approach to improve dynamic range. It follows the general form of the Gilbert mixer, except for the use of a bisymmetric Class-AB RF stage based on translinear principles. [8]

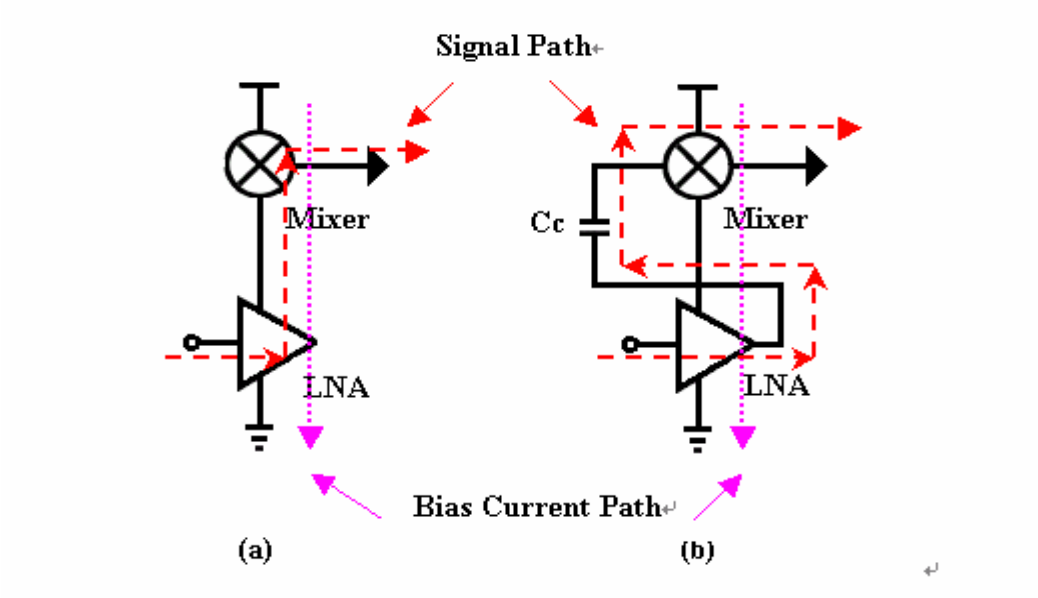


Fig. 1.2.1 (a) current-mode cascade (b) voltage-mode cascade of LNA & Mixer

Specification	voltage-mode [7]	current-mode [6]	This Work
RF Input Matching (dB)	-12	-15	-13.7
Voltage Gain (dB)	29.0	23.0	18.2
Power Gain (dB)	N/A	N/A	9.0
Noise Figure (dB)	6.0	3.4	N/A
P1dB (dBm)	N/A	-19.0	-19.0
IIP3 (dBm)	-16.0	-1.5	-4.8
LO-to-RF Isolation (dB)	N/A	<-71	-48.4
Power dissipation (mW)	6.25	21.6	18.8
Operation Freq. (GHz)	2.4	2.1	2.1
CMOS Process	0.25	0.35um	0.25um

Table 1.2.1 current-mode cascade [6], voltage-mode cascade [7] of LNA & Mixer, and our design measurement performance comparison summary

Although MICROMIXER provides a well-defined matching impedance and much lower input related nonlinearity, it is always more suited for BJT technology and exhibits poor performances in CMOS technology due to restriction by the trade-off of gain, noise figure and power dissipation. To accommodate it in CMOS technology, we will propose a modified topology based on this original basic MICROMIXER in this thesis, that is fully integrated and capable of operation at 2.45GHz band with higher gain, lower noise, higher linearity and lower power dissipation than those of basic one in CMOS technology.

The simulation results compared between basic and proposed new architecture of CMOS MICROMIXER are shown in Table 1.2.2, we can see these disadvantages (low gain, high noise figure and power dissipation) and design difficulties of basic MICROMIXER in CMOS technology obviously. That is why MICROMIXER in BJT form is generally studied and reported, but that in CMOS form is almost not investigated and presented up to now. In contrast, our proposed new RF CMOS MICROMIXER can achieve much higher gain, lower noise, better linearity, wider dynamic range and lower power consumption than the basic one in CMOS process.

Specification	Basic MICROMIXER	New MICROMIXER
RF Port Input RL (dB)	11.7	23.5
LO Port Input RL (dB)	12.9	19.3
Voltage Gain (dB)	-1.5	10.4
Noise Figure (dB)	20.1	11.4
P1dB (dBm)	-11.5	-10.1
IIP3 (dBm)	-1.5	-0.7
Power Consumption (mW)	15.0	3.7

Table 1.2.2 Simulation Comparison between Basic and New MICROMIXER

1.3 Thesis Organization

This thesis contains six chapters. In addition to Chapter 1, the introduction of our circuit design motivations and associated recent works for wireless communication systems, other chapters are organized as follows:

In Chapter 2, we will introduce some basic CMOS technology applied to RF integrated circuits. We will also briefly describe some basic on-chip components and models, such as MOSFET, MIM capacitors, and spiral inductors, which can be applied to RF front-end circuit.

In Chapter 3, we will present the design and implementation of a concurrent triple-band (1.8GHz, 2.45GHz and 5.25GHz) CMOS LNA. We will also introduce the concepts of concurrent triple-band receiver topology.

In Chapter 4, we will present the design and implementation of a CMOS double-balanced mixer merged LNA for WCDMA.

In Chapter 5, we will present the design and implementation of a new RF CMOS MICROMIXER for 2.45GHz.

In the final Chapter 6, we will make a conclusion and discuss the future works.

Chapter 2

RF IC Components and Models In CMOS Technology

2.1 Choice of Technology for RF Circuits

The viable IC technology for RF circuits continues to grow up. Performance, cost, and time to market are three critical factors influencing the choice of technologies in the competitive RF industry. Besides, the issues such as level of integration, form factor, and prior experience also play an important role in the decisions made by the designers. At present, a lot of technologies constitute the major section of the RF market, including GaAs, silicon bipolar, SiGe, CMOS, BiCMOS, and so on. [9] Usually viewed as low-yield, high power, high cost options, GaAs field-effect and heterojunction devices nonetheless have maintained a strong presence in RF products, especially in power amplifiers and front-end switches.

While GaAs processes offer useful features such as higher breakdown voltage, higher cutoff frequency, semi-insulating substrate, and high-quality inductors and capacitors, silicon devices in a VLSI technology can potentially provide both higher levels of integration and lower overall cost, as demonstrated in complex circuits such as frequency synthesizers. In fact, all building blocks of typical transceivers are available in silicon bipolar technologies from many manufactures. [25]

Although silicon bipolar and SiGe can provide good performance for RF ICs, CMOS technology still predominates over RF IC markets due to its advantages of lower cost, higher integration, more flexible size-scaling, superior linearity, and wider dynamic range. Besides, with rapidly developments in semiconductor process and

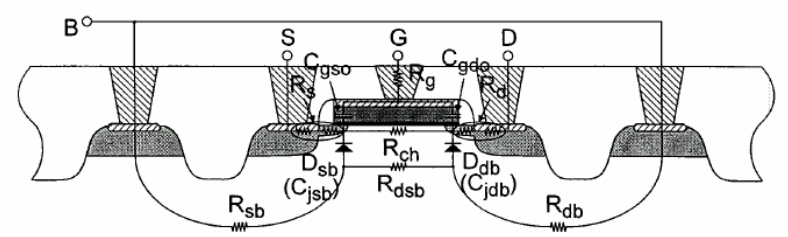
fabrication, scaling-down CMOS devices have achieved higher transit frequencies, such as tens of gigahertz in the 0.18-μm generation, and have fulfilled the requirements for RF IC applications. Furthermore, another noticeable advantage over the CMOS technology is that CMOS RF IC can be easily integrated with other mature base-band or mixed-signal parts for system-on-a-chip (SOC), supported by the enormous momentum of the digital market. However, this advantage of CMOS technology will inevitably face a lot of difficulties for its SOC applications.

"CMOS RF IC" has suddenly become the topic of active research. CMOS technology must nevertheless resolve a number of practical issues, such as substrate coupling, parameter variation with temperature and process, and device modeling for RF operation. COMS technology is inborn for logic application, so that the high frequency unpredictable characteristic will be a challenge for designer. To achieve better performance, it is necessary to build up more accurate and reliable RF models toward active and passive devices.

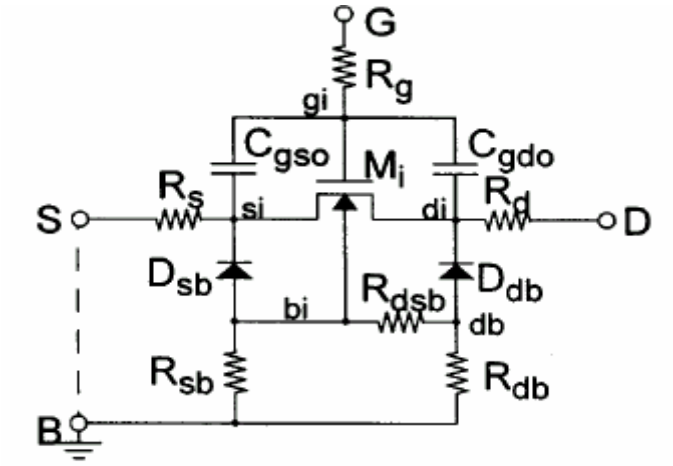
2.2 Active Device and RF Model

MOSFET is the most important and widely used among all of devices in RF CMOS technology. The structure and RF small signal model based on the sub-circuit approach are given in Fig. 2.2.1(a-b). This small signal model includes all parasitic components at the gate, source, drain, and substrate of transistor. The values of these parasitic components strongly depend on the layout and process fabrication of MOSFET. It can be used to model the MOSFET nonlinear characteristics at radio frequency. The intrinsic core model is based on the SPICE BSIM3v3 model. In this BSIM3v3 model, it has built in thermal noise characteristics as shown in Fig. 2.2.1(c). [10] However, this BSIM3v3 model is actually not an accurate noise model for radio frequency applications, so that the simulation results of noise parameters using this

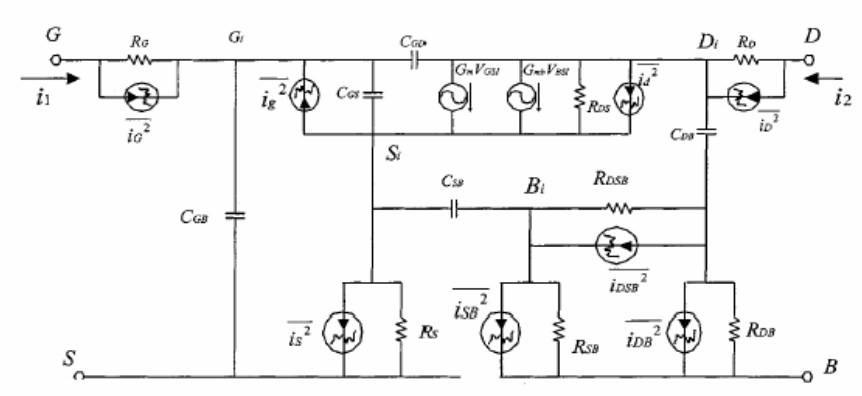
RF equivalent model are just approximations and can not be convinced completely. Therefore, a more accurate RF noise model is indeed required to be built up in advanced for precise RF noise performance estimation.



(a)



(b)



(c)

Fig. 2.2.1 (a) Cross-section view of MOSFET structure (b) Schematic of the equivalent circuit model for RF MOSFET (c) The equivalent sub-circuit including noise characteristics in the BSIM3v3 core model

As described previously, the physical layout is strongly associated with the parasitic components in the equivalent MOSFET model at high frequency. Since the foundry usually provides some standard physical layouts corresponding to separate equivalent circuit models extracted from testkey measurements, the physical layout of MOSFET must fit in with the choice of circuit model in the original circuit design procedure. Fig. 2.2.2 shows a case of MOSFET standard layout provided by foundry. It is found that the multi-finger structure can uniform signal or current paths and largely decrease gate resistance. In addition, many significant issues, such as current endurance, heat distribution, and ac signal coupling etc, must be considered carefully in a practical circuit layout to achieve desired good performance.

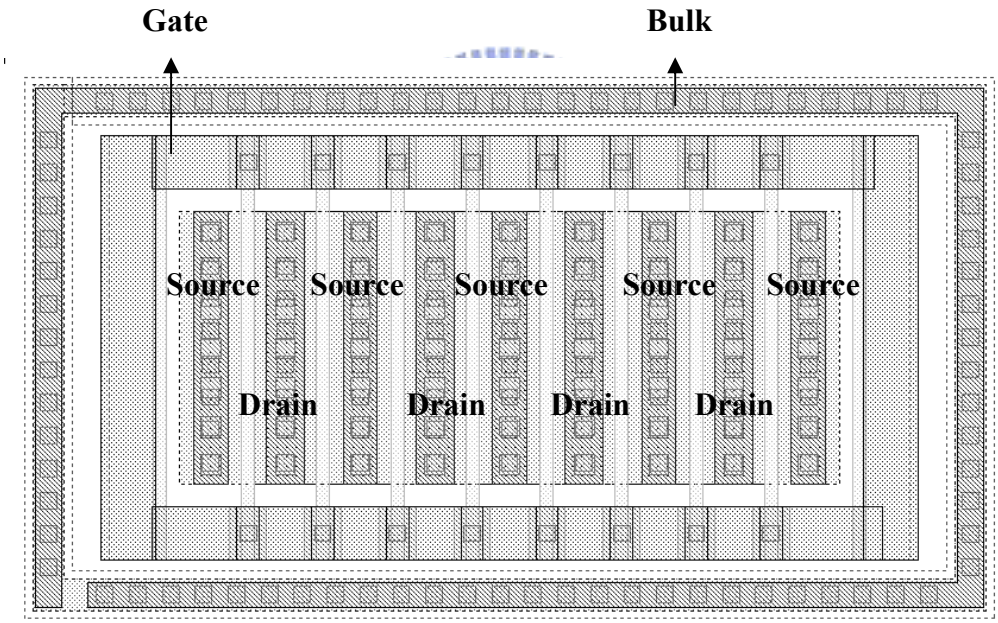


Fig. 2.2.2 Layout of Multi-finger RF MOSFET

2.3 Passive Device and RF Model

In the design of analog or RF IC, the passive devices, such as the poly resisters, MIM or POLY capacitors, and spiral inductors, always play significant roles toward circuit performance. They are usually used for dc bias, dc or RF blocking, impedance matching, and gain enhancement etc. For this reason, to realize and build up accurate

models of passive devices is an inevitable work for CMOS IC designers. Two passive devices, MIM capacitor and spiral inductor, are especially important and suitable for CMOS RF IC applications and thus are described in subsequent sections.

2.3.1 De-embedding Procedure

Before the formal descriptions of passive device models, an important method called "de-embedding procedure" must be introduced first. It is very useful for the testkey design and device modeling. In high frequency measurement, the purpose of de-embedding is to exclude the parasitic effects that are not associated with the device itself, such as those in pads. A simplified diagram of de-embedding procedure is shown in Fig. 2.3.1. When we design a "whole" testkey of device to build up its equivalent circuit model, the testkies of "open" and "through" must be also involved to completely exclude all parasitic effects. However, in general, if the operating frequency for device modeling is lower than 6GHz, the only dominant parasitic effect is in "open" pad. Consequently, we usually just consider the effect of "open" pad while neglecting the effects of "through" and "short" in the de-embedding procedure.

Furthermore, a simplified procedure of de-embedding can be proceeding as follows: First, transform the measured S-parameters of "whole" testkey and its "open" pad to Y-parameters. Here, the transformation to Y-parameters will greatly facilitate the calculations of de-embedding because both of their equivalent circuits are in parallel. Second, subtract the Y-parameter of "open" pad (Y_{open}) from that of "whole" testkey (Y_{total}) and have Y_{de}. Finally, transform Y_{de} back to the de-embedded S-parameter (S_{de}) we desired. The simplified expression is as follows:

$$S_{de} = S[Y_{total} - Y_{open}] = S[Y_{de}]$$

Thus, we can build up accurate device models using these de-embedded S-parameters.

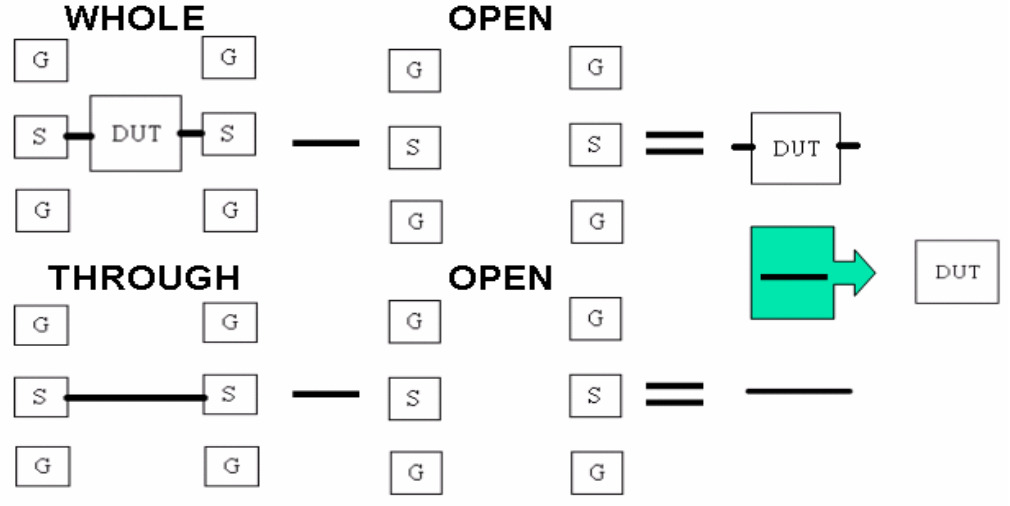


Fig. 2.3.1 Simplified block diagram of de-embedding procedures

2.3.2 MIM Capacitors

The most linear on-chip capacitors are in metal-insulator-metal (MIM) structures and are so called MIM capacitors as shown in Fig. 2.3.2. In the 1P5M (one POLY and five Metal layers) 0.25-μm CMOS technology, MIM capacitor consisted of Metal 4 layer as bottom plate and an additional layer, called CTM (Capacitor Top Metal), as top plate is one of two-port parallel plate's structures, where CTM layer is connected out via Metal 5 layer and the thin oxide dielectric layer is placed in between CTM and Metal 4 layer. The principle of parallel plate capacitors is applied to MIM capacitors and thus its capacitance can be approximately estimated by the formula:

$$C \approx \varepsilon \frac{A}{d} = \varepsilon \frac{W \cdot L}{d}$$

where ε is the dielectric constant, A is the overlapping area between CTM and Metal 4 layers calculated by multiplication of width W and length L, and d is the distance between top and bottom plate. [11] In theory, if fixed ε and d, we can get any desired capacitances flexibly by adjusting W and L. However, although the capacitance is proportional to the area of MIM capacitor, the larger area will decrease the Q (Quality factor) value of it due to fringing effects and the smaller area will also cause more

deviations in capacitance value due to process variations in practical fabrication. Typically, the capacitance of MIM capacitor is designed in the range of 0.2pF to 10pF and the Q value of it is in the range of 20 to 80 that is strongly depended on the area and operating frequency. Finally, Fig. 2.3.3 shows the equivalent circuit model for MIM capacitor that is capable of correctly modeling its RF characteristics. It includes the undesired effects from the lossy silicon substrate and other parasitic effects. In this equivalent circuit model, the inter-metal dielectric capacitance Cs is the main element of the capacitor, Rs and Ls are the parasitics existing in the electrodes, interconnections, metal plates, and dielectric loss, Cp and Rp are parasitics that represent the capacitance and resistance to ground between bottom plate metal and substrate.

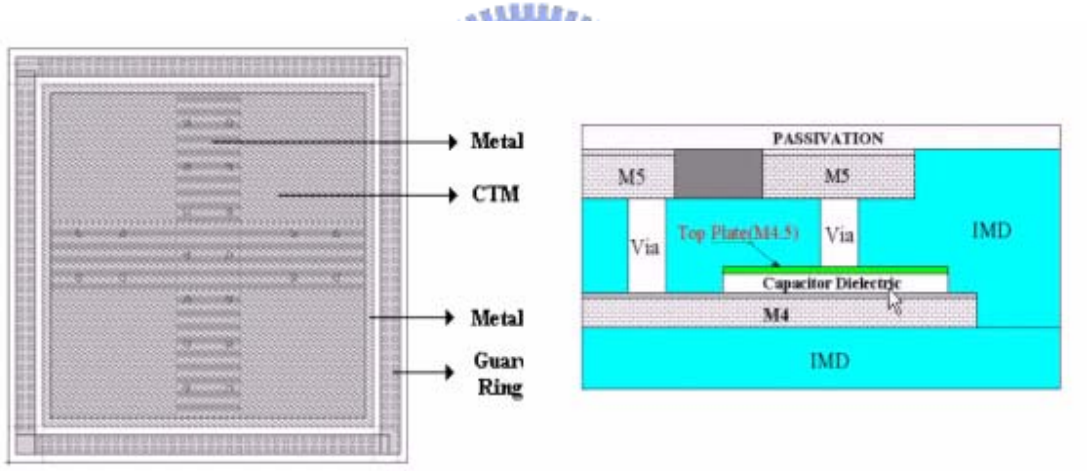


Fig. 2.3.2 (a) Layout top view (b) Cross section view of MIM capacitor

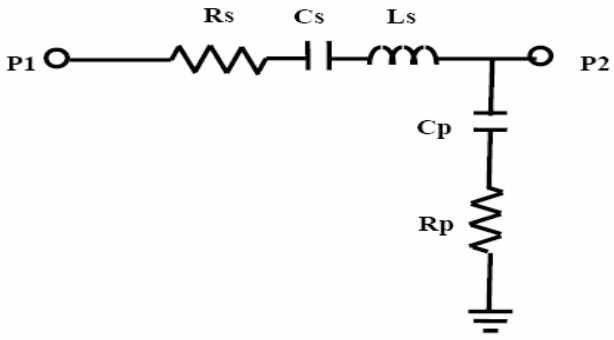


Fig. 2.3.3 Equivalent circuit model of MIM capacitor

2.3.3 Spiral Inductors

From the view point of RF circuits, the lack of a good inductor is by far the most conspicuous shortcoming of standard IC processes. In general, three types of inductors, including active inductor, bond wire inductor, and spiral inductor, have been used for RF IC applications. Although active circuits can sometimes synthesize the equivalent of an inductor, they always have higher noise, distortion, and power consumption than real passive inductors made with some number of turns of wire. However, although bond wire inductors permit a high quality factor to be achieved, their inductance values are constrained and can be rather sensitive to production fluctuations. Typically, the inductance of bond wire inductor is about 1nH per 1mm length and Q of it is about 60 near GHz frequency. Furthermore, the only widely used on-chip inductor is spiral inductor, a square version of which is shown in Fig. 2.3.4. One thing must be noticed that any device underneath inductor was forbidden due to magnetic flux penetrate into the silicon substrate. It will affect the device behavior when the device is under spiral inductor. In addition, on-chip spiral inductor has become one of the critical components and plays a significant role for implementing modern low-cost and high-integration RF ICs such as a low-noise amplifier, a voltage-controlled oscillator, and an impedance matching network etc.

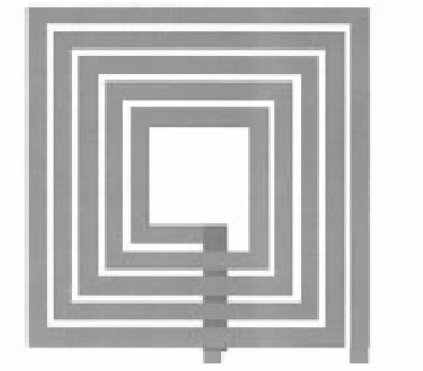


Fig. 2.3.4 Square planar spiral inductor

The values of inductance (L), quality factor (Q), and self-resonant frequency (SRF) are three major indexes for the design of a spiral inductor. A good spiral inductor must provide desired accurate inductance value, high quality factor, and high SRF with acceptable area. One of the most important parameters is the quality factor, which is mainly limited by the loss due to inductor metal resistance, substrate resistance, and that associated with induced eddy current below the inductor metal trace. For the CMOS RF IC applications, the realization of high Q spiral inductors is an important task to be solved imperatively, but this task is confronted with the challenge of high frequency performance degradation due to higher silicon substrate losses and thickness limitations of metal lines.

Recently, considerable efforts have gone into the design and modeling of spiral inductor implementations. A simple equivalent circuit model for spiral inductor is shown in Fig. 2.3.5. In this model, Ls represents the major spiral inductance, Rs is the series parasitic resistance which represents the energy losses due to the skin effect in the spiral interconnect structure and the induced eddy current in any conductive media close to the inductor, Cs represents the parasitic capacitance overlapped between the spiral and the center-tap underpass, Cox represents the oxide capacitance between the spiral and the substrate, Rsi represents the ohmic loss which signifies the energy dissipation in the silicon substrate, and Csi represents parasitic capacitance in the silicon substrate. While a lot of methods have been developed to estimate for the inductance of spiral inductor, one of the most useful expressions is analytical formulas for the inductance calculation proposed in [12]. The Q value of spiral inductor is defined as:

$$Q \equiv 2\pi \cdot \frac{Peak\_magnetic\_energy - Peak\_electric\_energy}{Energy\_loss\_in\_one\_oscillation\_sycle}$$

The single-ended Q value can be simply derived form the image part over the real part

of the input impedance while port 2 is short to ground, that is:

$$Q = \frac{\mathrm{Im}[Zin]}{\mathrm{Re}[Zin]} = \frac{X}{R}$$

Typically, the Q value of spiral inductor is about in the range of 4 to10 with the appropriate design of geometrical sizes.

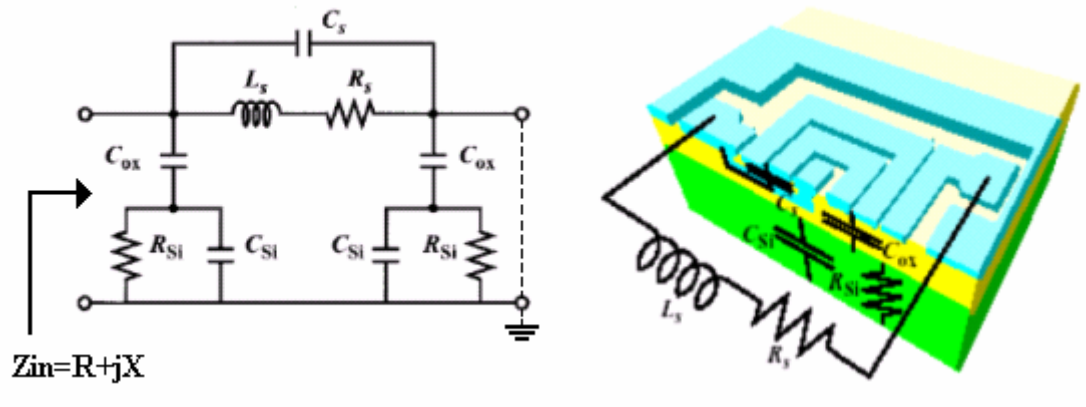
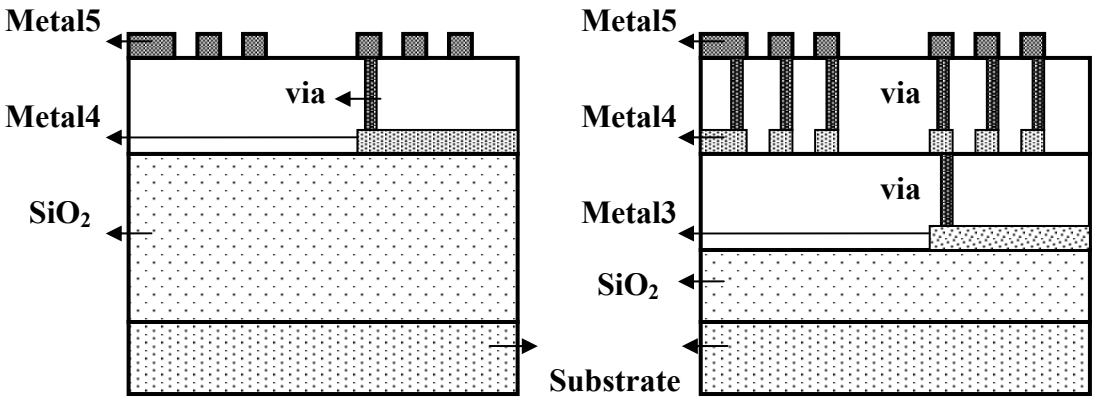


Fig. 2.3.5 Equivalent circuit model for spiral inductor

There are a lot of methods that can be used to improve the Q value of spiral inductors. Since the Q value depends on the real part of input impedance, so we can improve the Q value by reducing the resistance. Although increasing metal width (W) will reduce the resistance and thus increase the Q value in the lower frequency range, it will lower the self-resonance frequency. Another simple useful method is to take advantage of double metal layers in parallel to decrease the real part of input impedance and thus improve the Q value. Fig. 2.3.6 shows the simplified diagram of the single metal layer and double metal layer inductor structures in 1P5M 0.25-μm CMOS technology.

Throughout this thesis, in addition to square spiral inductors, we also take advantage of double metal layer circular spiral inductors, one case of them as shown in Fig. 2.3.7. In general, circular spiral inductors have the advantage of higher quality factor than other geometries with the same inductance value. Besides, it can also be realized with smaller inductance suitable for higher frequency applications.



(a) **(b)**

Figure 2.3.6 (a) Cross section view of a single metal layer spiral inductor

(b) Cross section view of a double metal layer spiral inductor

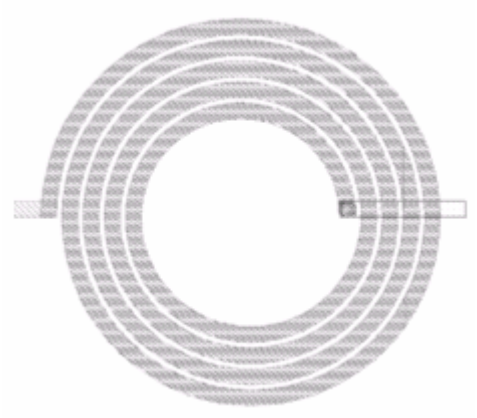


Fig. 2.3.7 Circular spiral inductor

Chapter 3

Concurrent Triple-Band CMOS LNA Design and Implementation

3.1 Architecture of Concurrent Multi-Band Receiver

Standard receiver architectures, such as super-heterodyne or zero-IF receivers, achieve high selectivity and sensitivity by narrow-band operation at a single input frequency. [13] Such operation modes always limit available bandwidth and robustness to channel variation and functionality of system. On the other hand, general wideband operations are more sensitive to out-of-band unwanted signals due to nonlinearity of transistors, even for new generation of ultra wideband system (UWB). These out-of-band blockers can severely degrade receiver's sensitivity. [14] However, modern wireless applications necessitate communication systems with more wideband, functionality and flexibility. Besides, for low cost and high integration consideration, the CMOS process has become one of the most popular technologies to provide excellent integration with other base-band blocks. Therefore, multi-standard RF receiver systems which integrated using CMOS technology are predicted to play a critical role in the future wireless communication system. Recently, multi-band receivers have been introduced to achieve these goals by switching between multiple bands to receive one band at a time [15-17], such as a simplified block diagram of the conventional dual-band WLAN receiver for IEEE802.11a/b/g shown in Fig. 3.1.1. Although it improves the receiver's versatility, it is not sufficient in the case of a multi-functionality receiver where more than one band needs to be received simultaneously. Besides, using conventional receiver architectures, simultaneous

operation at different frequency bands can only be achieved by building multiple independent signal paths with an inevitable increase in the cost, footprint, and power dissipation.

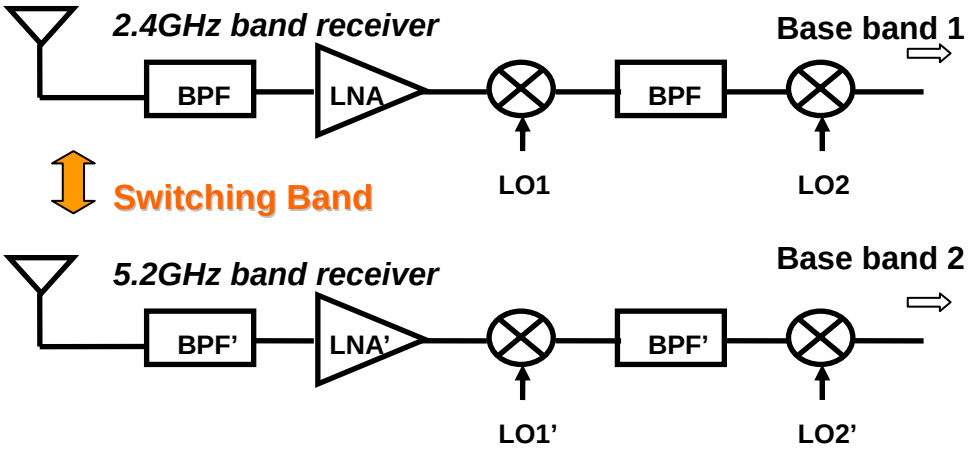


Fig. 3.1.1 Conventional dual-band receiver architecture

If we can combine two or more single-path RF receivers into one that is capable of simultaneous operation at different frequencies without dissipating as much power or a significant increase in cost and footprint, it will much reduce cost & power dissipation and improve integration in advanced. This observation leads to a compact and efficient front-end for a concurrent multi-band receiver, such as a simplified block diagram of the concurrent dual-band receiver shown in Fig. 3.1.2, which consists of a dual-band antenna, a monolithic dual-band filter, and a concurrent dual-band low noise amplifier (LNA) that provides simultaneous gain and matching at two bands. [2] It should be noted that the concurrent multi-band receiver does not need any multi-band switch or diplexer, because simultaneous reception at both bands is desired. However, a suitable LNA must be designed and realized before implementing a multi-standard receiver. This kind of novel LNA called concurrent multi-band band LNA [1] have to provide simultaneous narrow-band input matching and gain at multiple frequency bands, while maintaining low noise. A detailed approach to the design of such a multi-band LNA will be described in the subsequent sections.

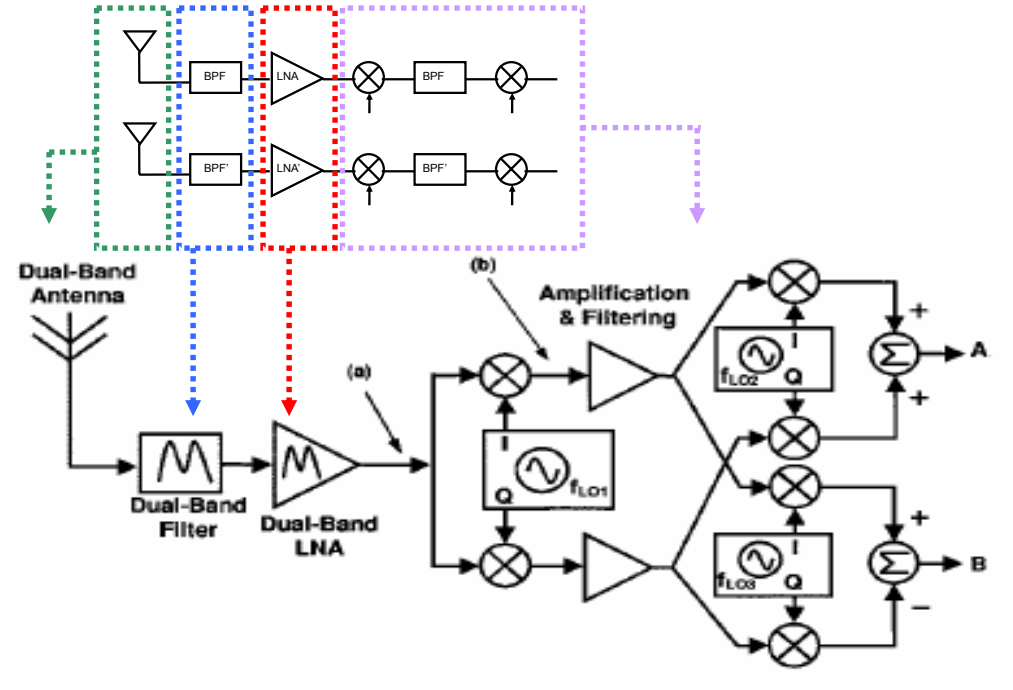


Fig. 3.1.2 Concurrent dual-band receiver architecture

3.2 Review of Concurrent Dual-Band LNA Architecture

As the wireless communication system becomes mature and widespread, the requirement of a LNA for the system has become a lot more sophisticated. Besides, LNA is one of the most critical building blocks in modern integrated RF transceivers for wireless communications. Recently, many researches about dual-band LNA have been studied and reported. [2-5] However, the concurrent triple-band LNA is rarely cited and studied. In this work, a new fully integrated high linearity concurrent triple-band CMOS LNA is first proposed that is capable of simultaneous operation at all three different frequency bands (1.8GHz, 2.45GHz, and 5.25GHz) without dissipating triple as much power or a significant increase in cost and footprint.

To provide some background and knowledge, before explaining the design details of concurrent triple-band LNA, it is helpful to review some basic design guidance and architecture of concurrent dual-band LNA. Similar to the single-band LNA, being the first active element of the receiver chain, the noise figure (NF) of a

dual-band LNA also plays a significant role in the overall NF of the dual-band receiver. Fig. 3.2.1 (a) shows the general model for transistor amplifier in common source configuration with arbitrary gate impedance (Z_g), source impedance (Z_s), load impedance (Z_L), gate-source impedance (Z_{gs}), and gate-drain impedance (Z_{gd}). Fig. 3.2.1(b) also shows its equivalent circuit that includes the inherent reactance components (C_{gs} & C_{gd}) of the transistor. We can use this equivalent model to achieve simultaneous power and noise matching in a concurrent multi-band LNA. Assume that Z_{gd} is much larger than the other impedances and the effects of C_{gd} and its associated Miller effect can be neglected, the input impedance can be simplified as:

$$Z_{in} = Z_g + Z_{gs} + Z_s\left(1 + g_m Z_{gs}\right)$$

This expression can be used to design multi-band input matching network with optimized NF at multi-band frequencies of interest if the real part of $Z_g + Z_{gs} + Z_s$ is minimized. The desired transconductance (g_m) of the transistor is calculated based on power dissipation, gain consideration and noise figure. We can select minimum channel length and smaller C_{gs} to improve NF. A very important observation is found that the transconductance of the transistor is inherently wide-band and can be used to provide gain and noise matching at other frequencies without any penalty in the power dissipation. [1]

The typical structure of the concurrent dual-band LNA is shown in Fig. 3.2.2. [2] In a common source configuration, inductive degeneration is used to easily generate the real part of input impedance which can make the input of LNA match to the preceding antenna or filter. Inductive degeneration can also enhance the output signal-to-noise ratio (SNR) of the receiver. The inductive feedback moves the source

impedance for optimum NF toward the optimum power match with only a minor increase in the minimum NF. Cascode configuration can be used to enhance gain, frequency response, stability, reverse isolation of the amplifier, and also reduce Miller effect. [5][18] The input parallel LC tank (L_a & C_a) is designed to resonate with $Z_g + Z_{gs} + Z_s$ at both frequency bands. The drain load network (the series LC branch in parallel with the parallel LC tank) exhibits high impedance only at desired frequencies and offers an extra image rejection at series LC resonant frequency between dual-band frequencies.

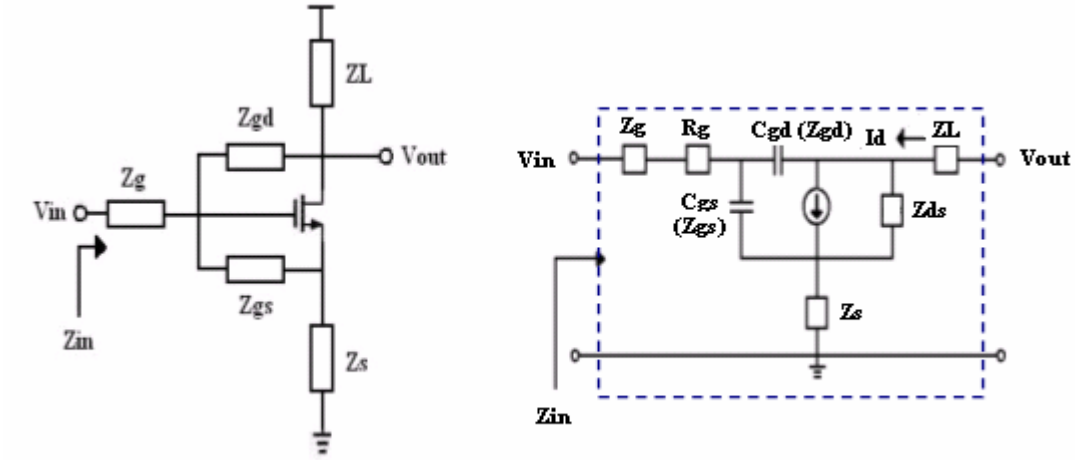


Fig. 3.2.1 (a) General model for a common-source amplifier
(b) Equivalent circuit for a common-source amplifier

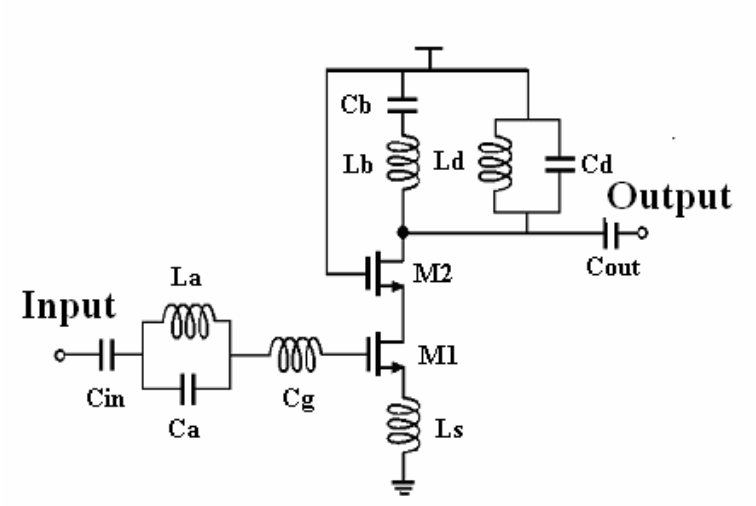


Fig. 3.2.2 Concurrent Dual-band LNA

3.3 Architecture of Concurrent Triple-Band Receiver and LNA

In this section, we will describe the concept of a single path concurrent triple-band receiver topology and propose a new concurrent triple-band LNA architecture based on dual-band LNA we discussed previously. Fig. 3.3.1 shows a simplified diagram of the concurrent triple-band receiver architecture that can be fully integrated on a chip. If we can combine three independent received paths into single path, it will not only maximize the power usage but also reduce the cost and chip area a lot, leading to an efficient concurrent triple-band receiver.

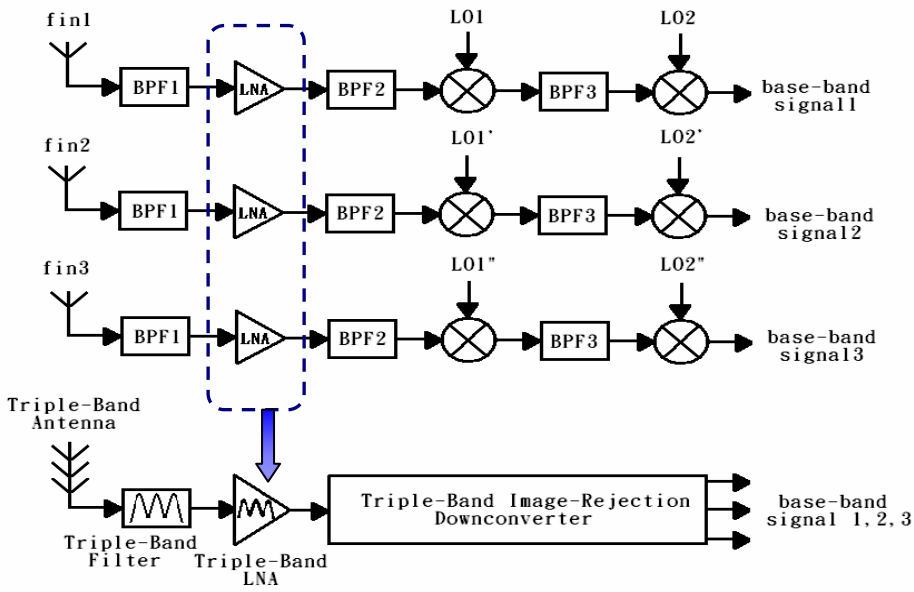


Fig. 3.3.1 Architecture of Concurrent Triple-Band Receiver

As shown in Fig. 3.3.2, we develop and propose a new concurrent triple-band LNA architecture that is fully integrated. A two-stage topology with bias-current reuse technique has been used to simultaneously achieve high gain and good matching without large amount of power consumption at all three desired band. [7][19] The first stage consisted of M1 and M2 is similar to dual-band LNA architecture, which adopts a source inductive degeneration cascode configuration. The second stage (M3) is

isolated from the first one via bypass capacitor (Cb) and RF signals are fed into the second stage through coupling capacitor (Cc). Based on the characteristics of series LC tank resonance (short circuit) and parallel LC tank resonance (open circuit), we can simultaneously design and realize input and output networks matched to about 50ohm source impedance. Similar to dual-band LNA, output matching network will provide two zeros between each band. Large image rejection in excess of that of the single-sideband receiver is achieved through diligent frequency planning and proper usage of stop-band attenuation. In particular, we introduce some feedback and coupling capacitors to adjust bandwidth of desired bands and spacing between each band. In the subsequent sections, we will demonstrate that this newly proposed circuit topology could meet our design ideas by using these design considerations through SPICE post simulation and measurement results.

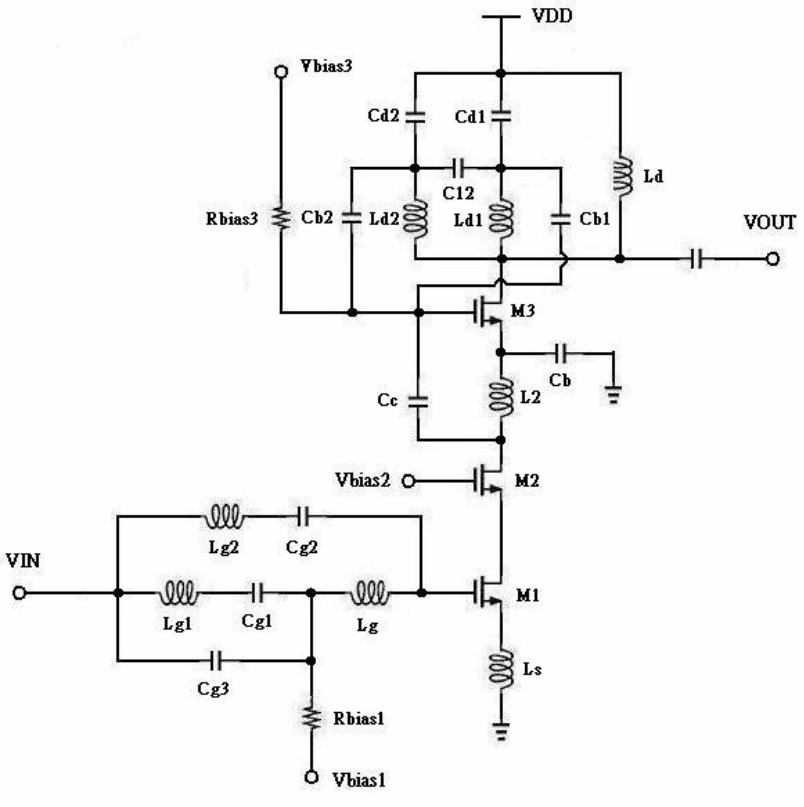


Fig. 3.3.2 Concurrent Triple-Band CMOS LNA (Fully-integrated)

3.4 Design and Analysis of Concurrent Triple-Band LNA

In this section, we will develop the design and analysis of concurrent triple-band LNA step by step. The most important thing in design and analysis the LNA is to pick up the appropriate device width and bias point to optimize noise performance in given specific objectives for gain and power dissipation. [20][21] For the triple-band LNA, it will degrade the noise performance at higher frequency band inherently. So we will choose the MOS transistor M1 size by optimizing noise performance at the highest frequency band (5.25GHz).

To select the width of transistor M1, we recall the noise factor expression (shown in below) that includes the effect of induced gate noise for an amplifier. [18]

$$F = 1 + \frac{\gamma \omega_0 L}{3 v_{sat}} P(\rho, P_D)$$

where

$$P(\rho, P_D) \approx \frac{\frac{P_D}{P_0}(1 + \frac{\delta}{5\gamma}) + 2|c|\sqrt{\frac{\delta}{5\gamma}}\rho^2 + \frac{P_0}{P_D}\frac{\delta}{5\gamma}\rho^4}{\rho^3}$$

$$P_0 = \frac{3}{2}\frac{V_{dd} v_{sat} \varepsilon_{sat}}{\omega_0 R_s} \quad \& \quad \rho = \frac{V_{od}}{L\varepsilon_{sat}}$$

γ : Coefficient of channel thermal noise δ : Coefficient of gate noise

ω_0 : Resonance frequency v_{sat} : Saturation velocity

ε_{sat} : Velocity saturation field strength c : Noise correlation coefficient

The relation between Noise Factor and MOS size is as follows:

$$Q_L = \frac{\omega_0 (L_s + L_g)}{R_s} = \frac{1}{\omega_0 R_s C_{gs}} \quad \text{.....(1)}$$

$$P_D = V_{dd} I_d = V_{dd} W C_{ox} v_{sat} \frac{V_{od}^2}{V_{od} + L\varepsilon_{sat}} \quad \text{.....(2)}$$

$$C_{gs} = \frac{2}{3} W L C_{ox} \quad \text{.....(3)}$$

$$Q_L = \frac{P_o}{P_D} \frac{\rho^2}{1+\rho} \quad \text{.....(4)}$$

We have calculated and solved these above equations through MATLAB program and also generated the result as shown in Fig. 3.4.1, that is "Fixed power (P_D=40mW) Noise Figure vs. Q_L". From this result, we can choose Q_L=1.5 as P_D=40mW to minimize the Noise Figure at the highest frequency band (5.25GHz). Finally, substitute them into equation shown below:

$$W_{m1,opt,PD} = \left[\frac{2}{3} \omega_0 L C_{ox} R_s Q_{L,opt,PD} \right]^{-1} \quad \text{.....(5)}$$

We can derive the optimized width of M1 for 5.25GHz, which is about 480um if minimum channel length of 0.25um is chosen. And the width of transistor M2 is approximately selected as half of M1 according the experience in [22].

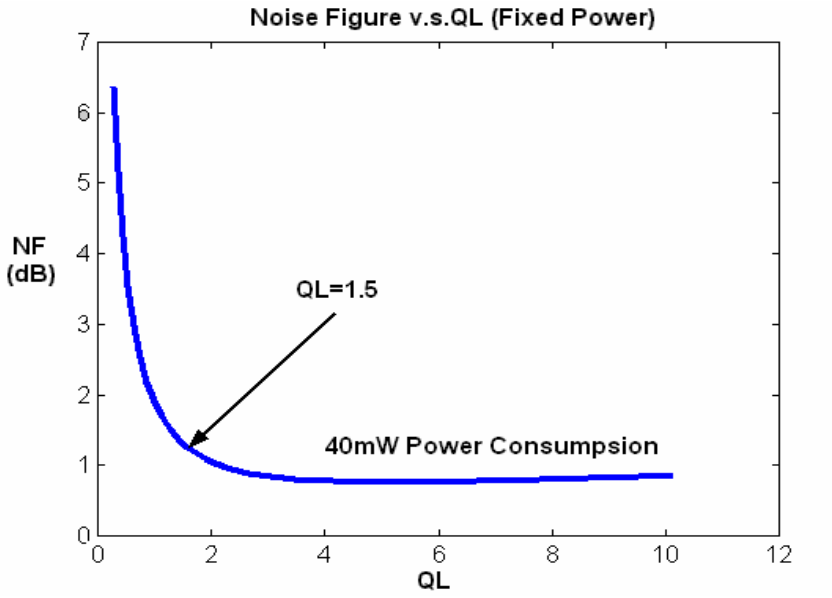


Fig. 3.4.1 Noise Figure vs. QL with fixed power

3.5 Simulation and Measurement of Concurrent Triple-Band LNA

3.5.1 Layout and Simulation Results

A fully integrated high linearity concurrent triple-band LNA shown in Fig. 3.3.2 is designed and optimized through SPICE simulator. The final layout of it is shown in Fig. 3.5.1 and all elements are fully integrated on a chip including spiral inductors, metal-insulator-metal (MIM) capacitors, multi-finger RF NMOS transistors, poly resistors, and decouple MOS capacitors. The total chip size including pads is about 1200umx1400um. It has been fabricated using TSMC 0.25-um mixed-signal CMOS process through CIC. At high frequencies, the drain and source of a MOSFET, pads, inductors, and other elements on the silicon substrate have resistive components due to lossy silicon substrate. These parasitic resistances consume signal power, generate thermal noise, and thus gain & noise performances of the LNA are degraded a lot. To avoid these effects from pads, we also take advantage of the shielded signal PAD as shown in Fig. 3.5.2 to reduce noise coupling from the noisy silicon substrate. [23]

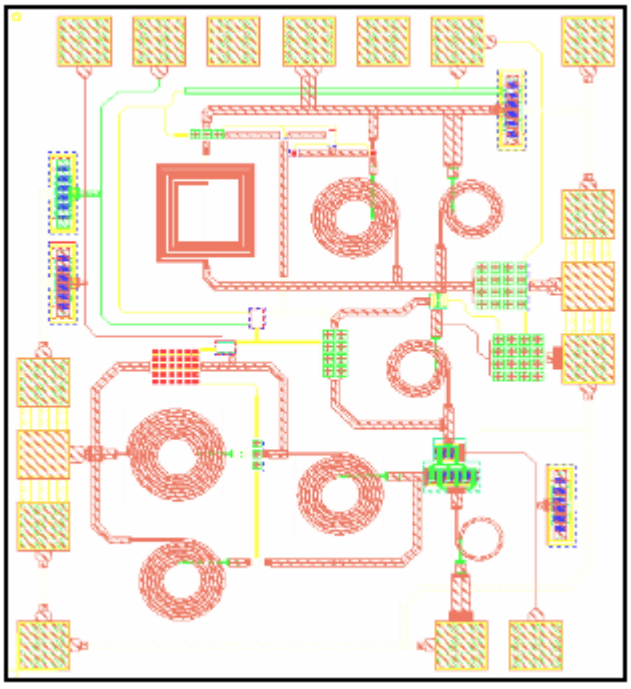


Fig. 3.5.1 Layout of Concurrent Triple-Band LNA

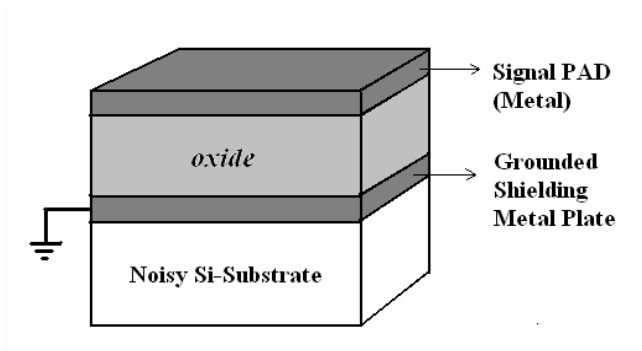


Fig. 3.5.2 The shielded signal PAD structure

The SPICE post simulation performances including all extracted parasitic are shown in Fig. 3.5.3 to Fig. 3.5.5. Fig. 3.5.3 shows the S-parameter of input matching (S_{11}) and power gain (S_{21}). Fig. 3.5.4 shows the S-parameter of output matching (S_{22}) and reverse isolation (S_{12}). Fig. 3.5.5 shows the NF performance. The LNA exhibits input matching to 50ohm with S_{11} of -10.6dB at 1.8GHz, -10.4dB at 2.45GHz, and -19.9dB at 5.25GHz, as well as output matching to 50ohm with S_{22} of -15.5dB, -12.5dB, and -12.0dB respectively. And it provides forward gain of 10.1dB, 10.8dB, and 11.8dB as well as reverse isolation of –67.0dB, -62.5dB, and –54.5dB with Noise Figure of 3.7dB, 4.8dB, and 6.4dB respectively. The simulation results of two-tone test IIP_3 (Input 3rd order intercept point) are 1.7dBm, 0dBm and 4.5dBm. And the P_{1dB} (Input 1dB compression point) is simulated to be -7.8dBm, -9.8dBm and -6.9dBm respectively. The circuit draws dc current of 15.7mA from a 2.5V supply voltage. The performances at three desired frequency bands are summarized in Table 3.5.1.

According to above results, we can find that this circuit design actually provides similar good performances in input/output matching, forward gain, reverse isolation, linearity, and dynamic range at all desired three bands. However, the noise performance seems not as good as that of the conventional single-band LNA. There are two major factors to cause it. First, unlike single-band LNA, the noise performance of concurrent multi-band LNA is intrinsically restricted by its inherently

complicated architecture. Furthermore, to achieve concurrent multi-band matching, the circuit must involve more passive devices. It will thus cause worse noise performance than simple single-band architecture with less passive devices. Second, for easy integration in the future, all passive devices what we used here are fully on-chip elements and it will also cause worse noise performance than that with outside-chip elements due to their lower quality factor, especially for low Q spiral inductors at higher frequency.

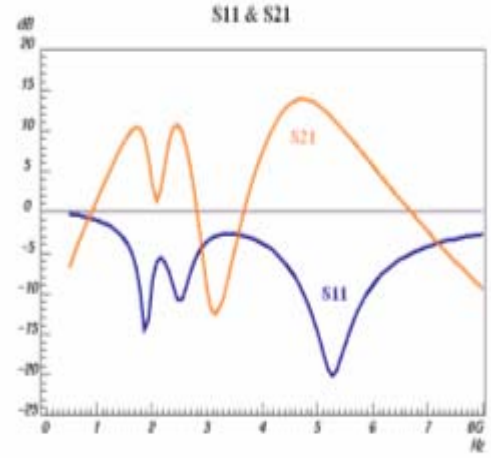


Fig. 3.5.3 Input Matching & Power Gain

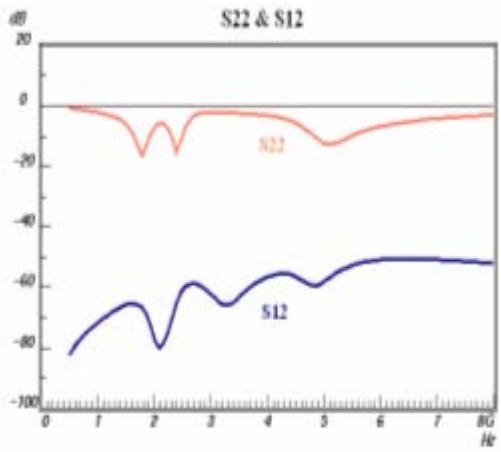


Fig.3.5.4 Output Matching Reverse Isolation

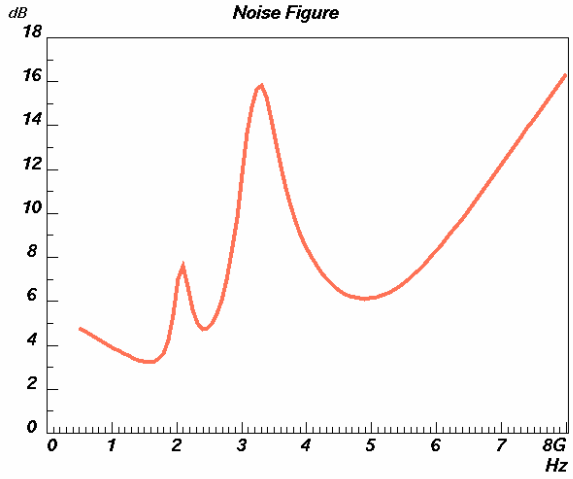


Fig. 3.5.5 Noise Figure

Specification	@1.8GHz	@2.45GHz	@5.25GHz
S11 (dB)	-10.6	-10.4	-19.9
S21 (dB)	10.1	10.8	11.8
S22 (dB)	-15.5	-12.5	-12
S12 (dB)	-67	-62.5	-54.5
NF (dB)	3.7	4.8	6.4
P1dB (dBm)	-7.8	-9.8	-6.9
IIP3 (dBm)	1.7	0	4.5
Supply voltage: 2.5V Power dissipation: 39.1mW			

Table 3.5.1 Post Simulation Performance Summary

3.5.2 Measurement Consideration

The measurement arrangement for our design of the concurrent triple-band LNA is shown in Fig. 3.5.6. Because we take advantage of on-wafer testing on our design, the chip layout allocation must meet the specification of the NDL probe station layout rule as shown in Fig. 3.5.7. We use one 6-pin dc probe card, two single-pin dc probes, and two GSG RF probes on NDL probe station as shown in Fig. 3.5.8 conjunction with the RFIC parameter measurement system as shown in Fig. 3.5.9. The die photograph is also shown in Fig. 3.5.10.

There are some RF parameters of LNA or other front-end circuits that we have to measure through on-wafer testing. These parameters include the high frequency S-parameters, Noise Figure, P_{1dB}, and two-tone IIP_3 linearity test. We use RFIC measurement system in NDL to finish these parameter measurements. The measurement setups and instruments for each parameter are shown in Fig. 3.5.11.

The concurrent triple-band LNA is designed for the 50Ω measurement system. All of the matching devices are integrated as on-chip components and then we can make the on-wafer measurements directly without extra matching circuits. Since we

have finished the measurements from NDL, we will compare and discuss the simulation and measurement results in subsequent section.

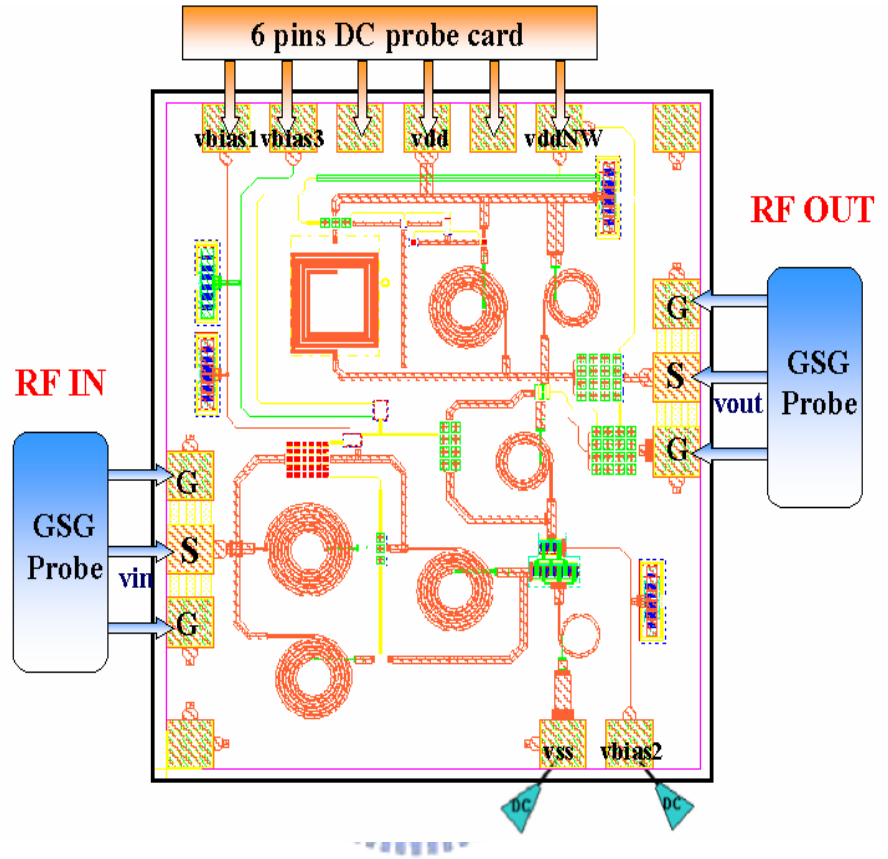


Fig. 3.5.6 Measurement Arrangement

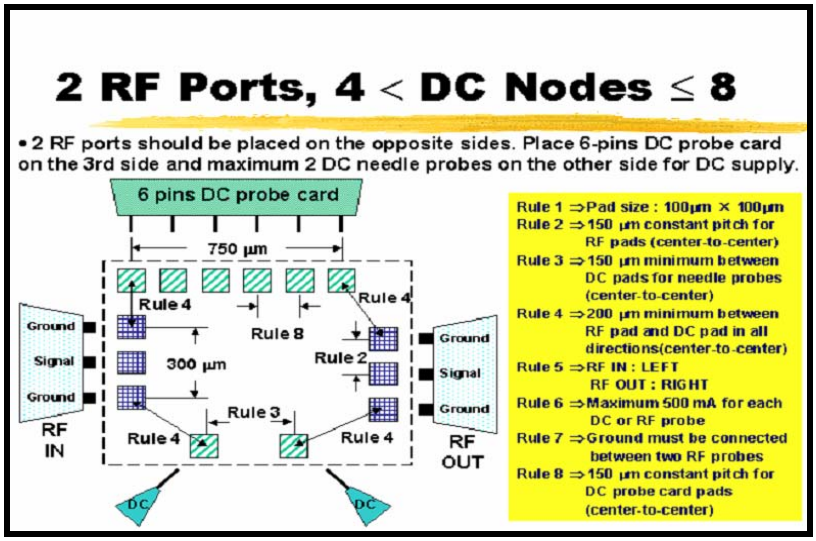


Fig. 3.5.7 NDL Probe Station Layout Rule

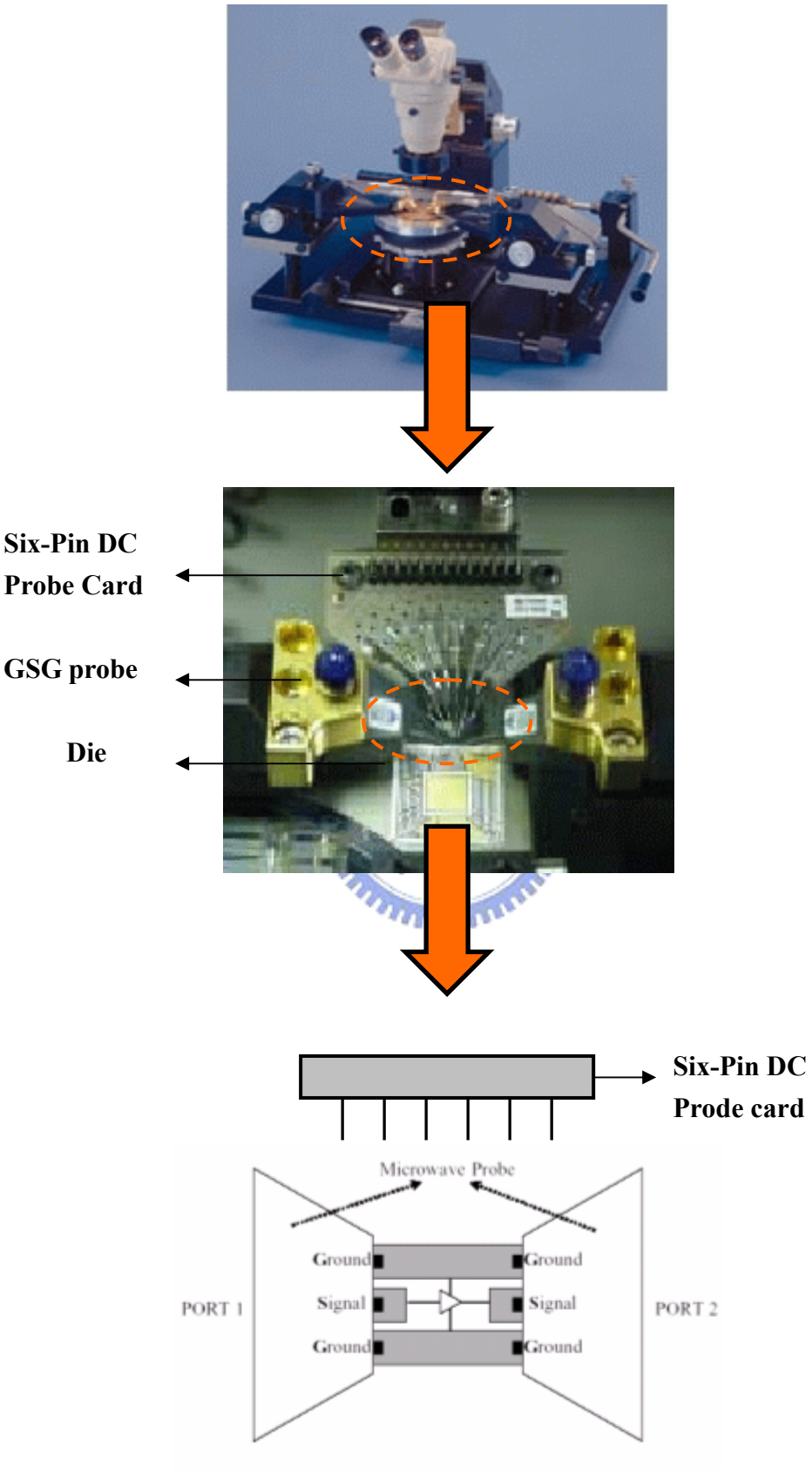


Fig. 3.5.8 Probe Station and on-wafer GSG Probe testing setup

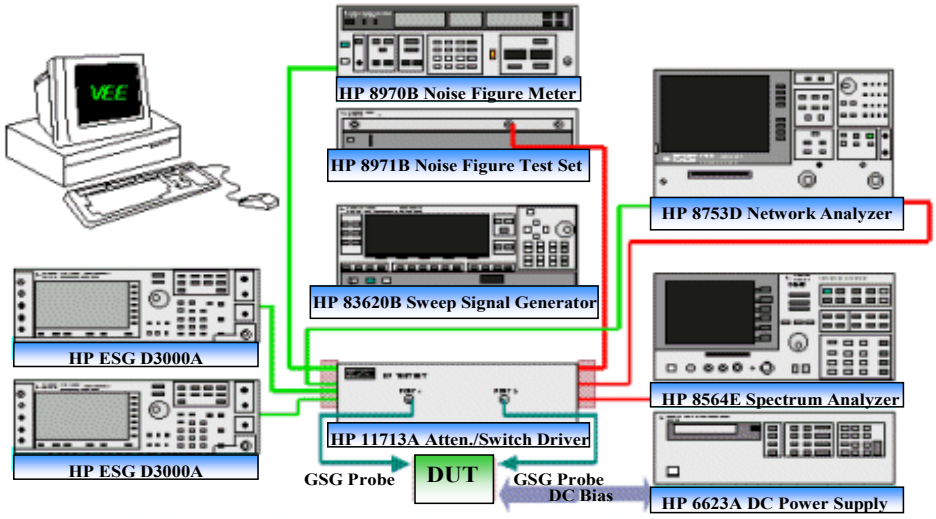


Fig. 3.5.9 RFIC Parameter Measurement System

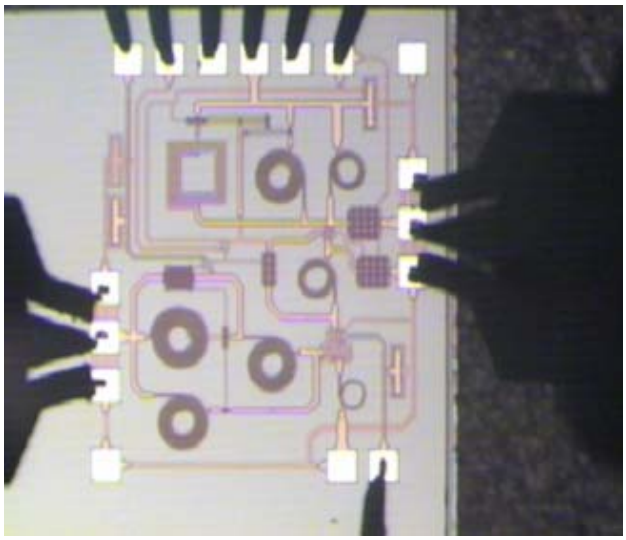
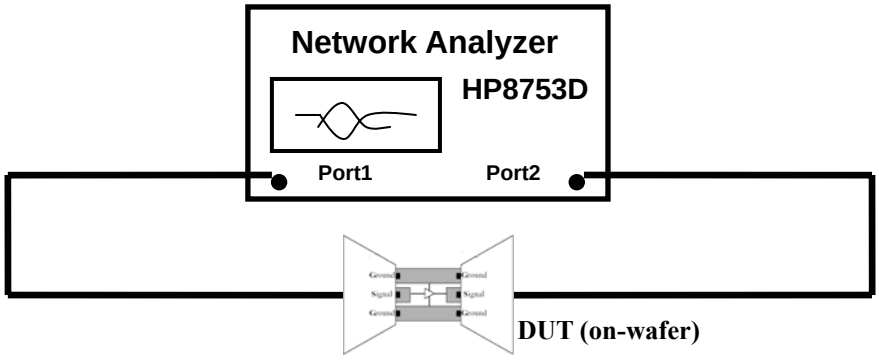
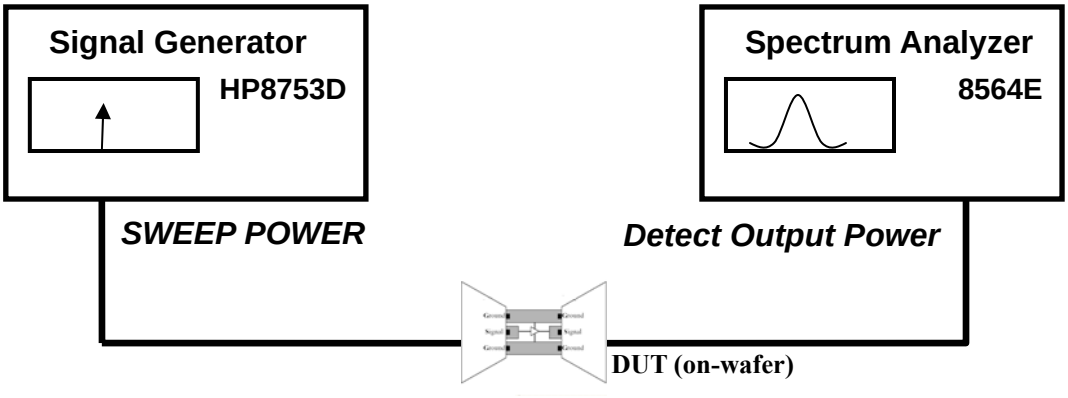


Fig. 3.5.10 Die Photograph of Triple-Band LNA



(a)



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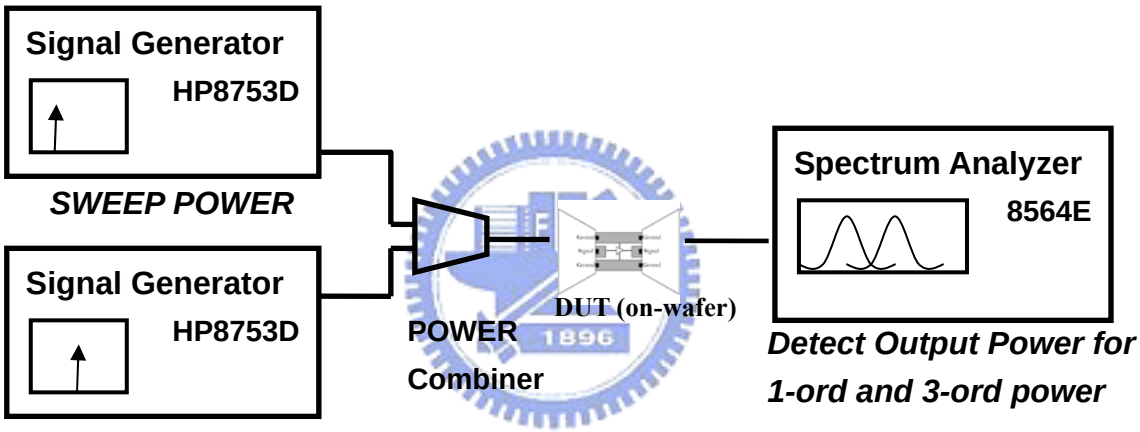

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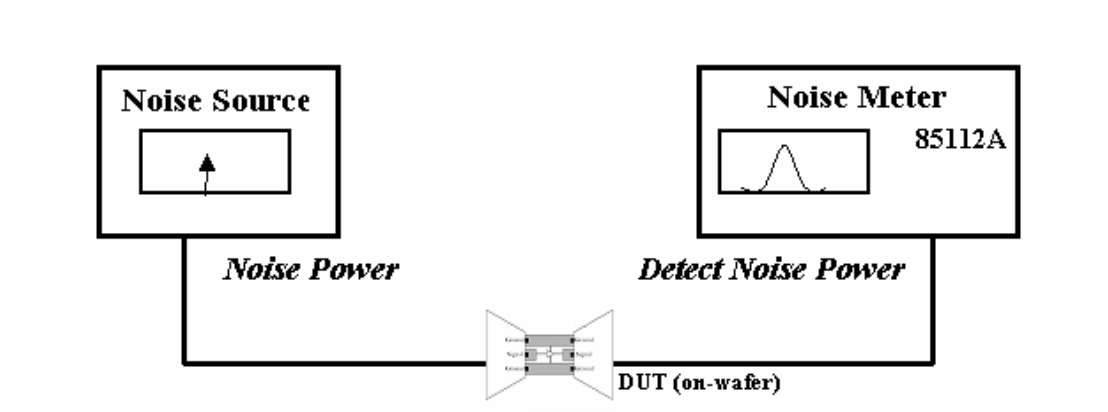


(d)

Fig. 3.5.11 Measurement Setups for (a) S-parameters

(b) P_{1dB} (c) Two-tone IIP_3 test (d) Noise Figure

3.5.3 Measurement Results

Upon previous measurement consideration and arrangement, we have made on-wafer testing for our novel LNA in NDL. Fig. 3.5.12 shows the simulated and measured input matching (S11) and forward gain (S21). Fig. 3.4.13 shows the simulated and measured output matching (S22) and reverse isolation (S12). The simulation and measurement result of noise figure is shown in Fig. 3.5.14. The output power gain versus input power sweep is shown in Fig. 3.5.15. The two-tone test measurement result is shown in Fig. 3.5.16. The LNA exhibits input matching of –23.9dB at 1.8GHz, -10.9dB at 2.45GHz, and –25.7dB at 4.5GHz, as well as output matching of –6.9dB, -4.3dB, and –6.7dB respectively. And it provides forward gain of 5.8dB, 4.1dB, and 2.7dB as well as reverse isolation of -35.0dB, -30.7dB, and –47.9dB with NF of 6.0dB, 7.6dB, and 10.3dB respectively. The measurement results of IIP_3 are 4.9dBm, 3.9dBm, and 11.9dBm respectively. And the measurement results of P_{1dB} are –5.0dBm, -6.2dBm, and 0dBm respectively. The LNA actually exhibits very high linearity and wide dynamic range from above measurement data. The simulation and measurement performances are summarized in Table 3.5.2. The circuit drains dc current of 15.7mA from a 2.5V power supply voltage that is very close to that in TT-corner simulation result.

3.5.4 Comparison and Discussion

Although the measured performances in S-parameters and noise figure are not as good as those in simulation results, we actually have demonstrated our novel circuit design concepts for concurrent triple-band LNA that is first proposed. From the simulation and measurement comparison results of the S-parameters, we can observe that the input matching for lower dual frequency bands is nearly falling at desired

frequencies and LNA achieves better input matching than that of simulation, -23.3dB at 1.8GHz and -10.9dB at 2.45GHz respectively. But the input matching for higher frequency band (5.25GHz) is obviously shifted to lower frequency at 4.5GHz, -25.7dB. The major reason is that the parasitic inductances are not considered and included in our design procedure, especially for such a complicated and large area chip layout at higher frequency. It can be demonstrated easily through the post simulation extracted these extra parasitic inductances. We can also find that the output matching is nearly broadband matching but still has the trend of concurrent triple-band matching. This is because the original additive feedback capacitors are chosen too small to control exactly and have great deviations after fabrications. Lager feedback capacitances have made the output port become broadband matching.

Besides, although the two-stage cascode topology can achieve better isolation, the power gain and noise figure performances do not meet our anticipation in this architecture. There are three major factors. First, the parasitic resistances are also not considered and neglected in our design procedure. These will largely reduce the forward gain and increase output noise, especially at higher frequency. It can also be demonstrated easily through the post simulation extracted these extra parasitic resistances. Second, the quality factor Q value of the LC tank is not good enough due to increasing parasitic resistances. We can see if we substitute these tanks with high Q or off-chip ones, it will largely improve these performances. The third factor is unacceptable output matching (S22). Furthermore, this LNA design can achieve better dynamic range and linearity of P_{1dB} and IIP_3 parameters in measurement than those in simulation due to lower gain performances.

In fact, the models of the spiral inductors applied at higher frequency (5.25GHz) are not as accurate as those applied at lower frequency because all models we have involved are designed for optimum operation at lower frequency (2.4GHz). So that

they will also cause mismatches between simulation and measurement results. In summary, to design a concurrent multi-band LNA or even other RF circuits with better performances, not only the parasitic effects have to be considered more carefully but the more accurate models designed and optimized for all desired frequencies must be involved, especially for complicated and large chip area circuits at higher frequency.

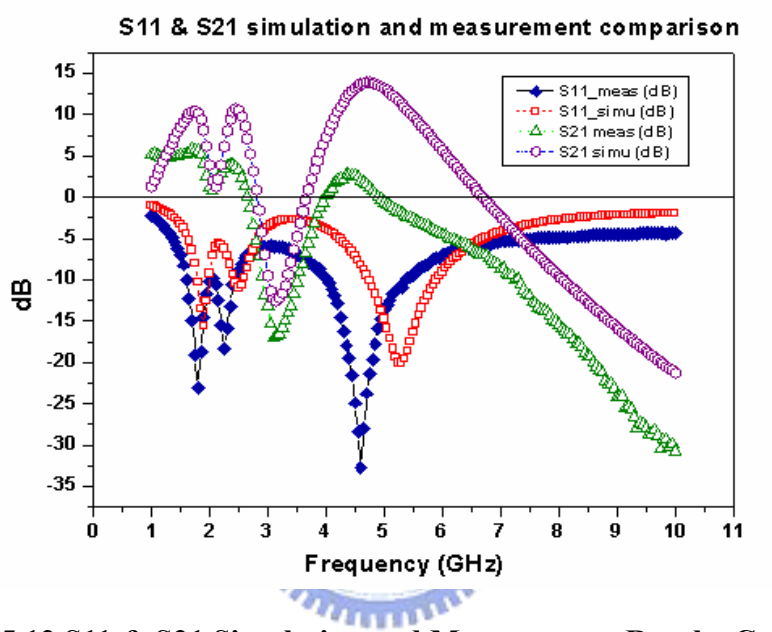


Fig. 3.5.12 S11 & S21 Simulation and Measurement Results Comparison

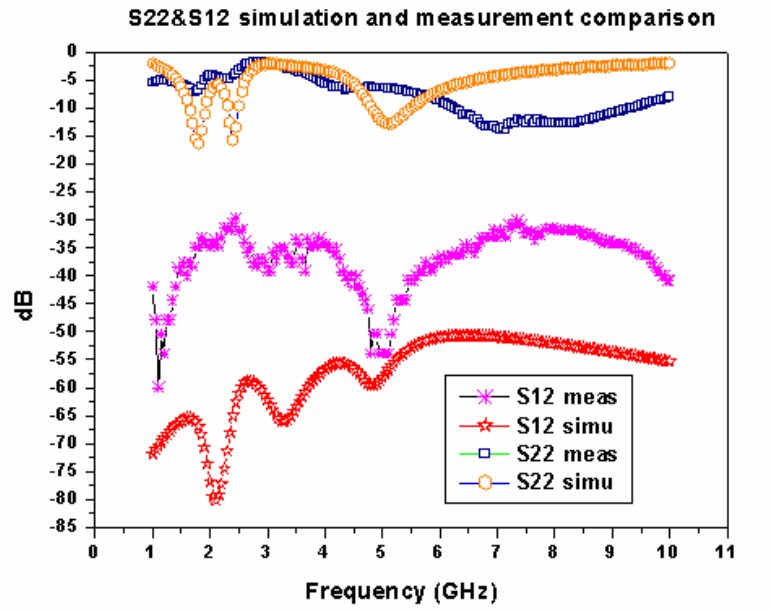


Fig. 3.5.13 S22 & S12 Simulation and Measurement Results Comparison

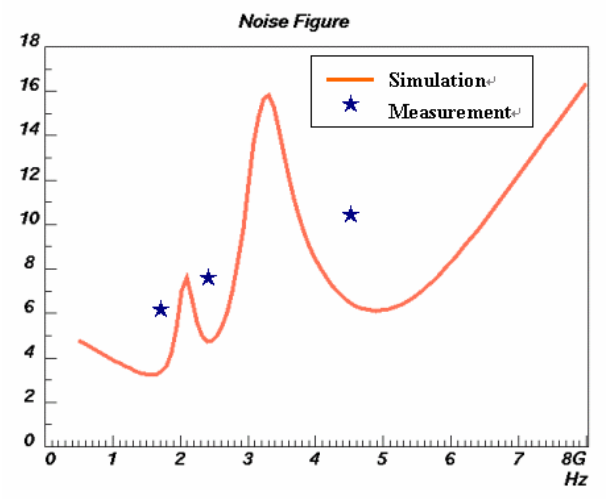
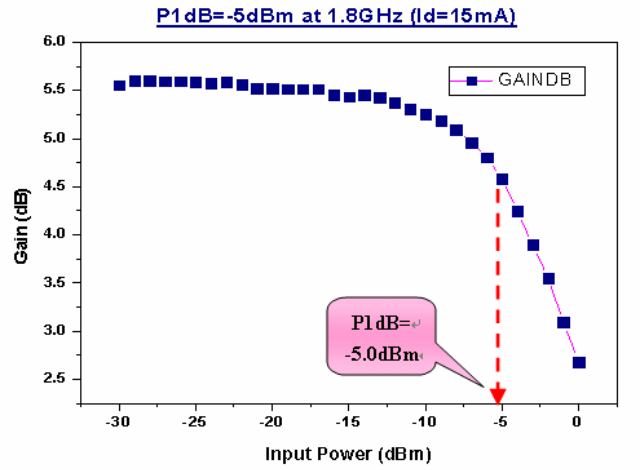


Fig. 3.5.14 NF Simulation and Measurement Results Comparison



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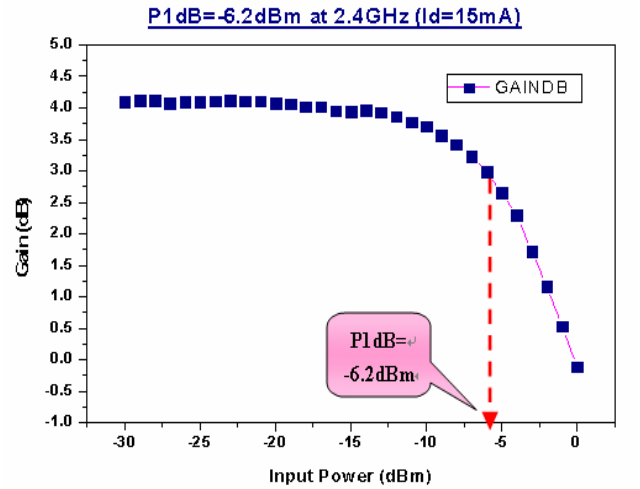

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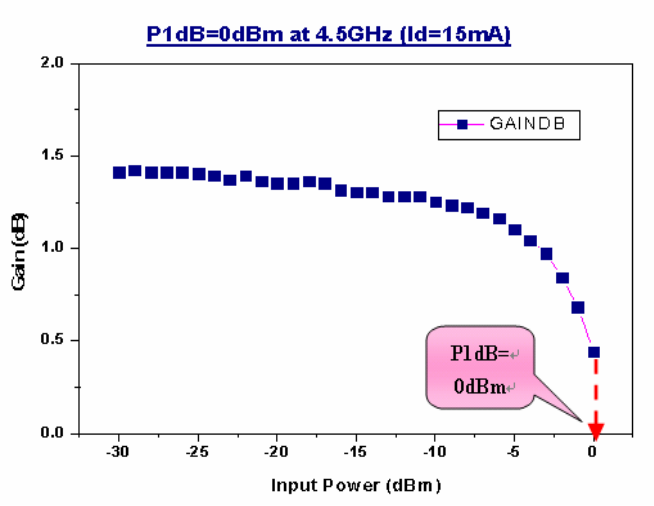
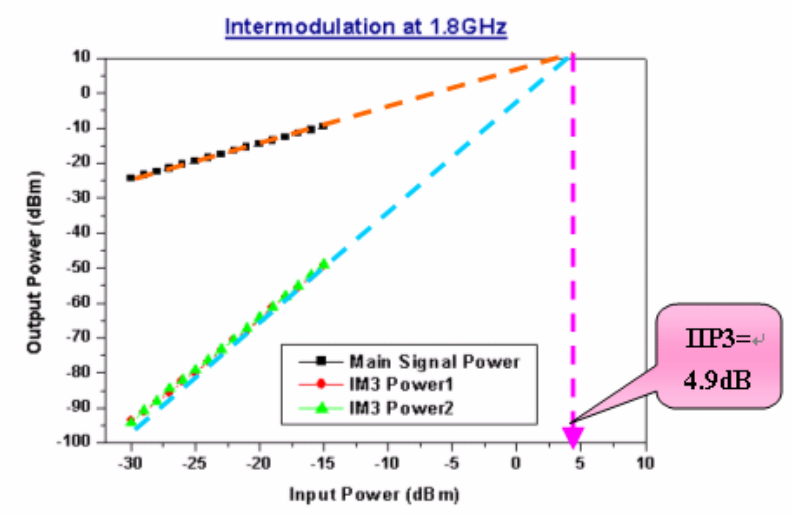
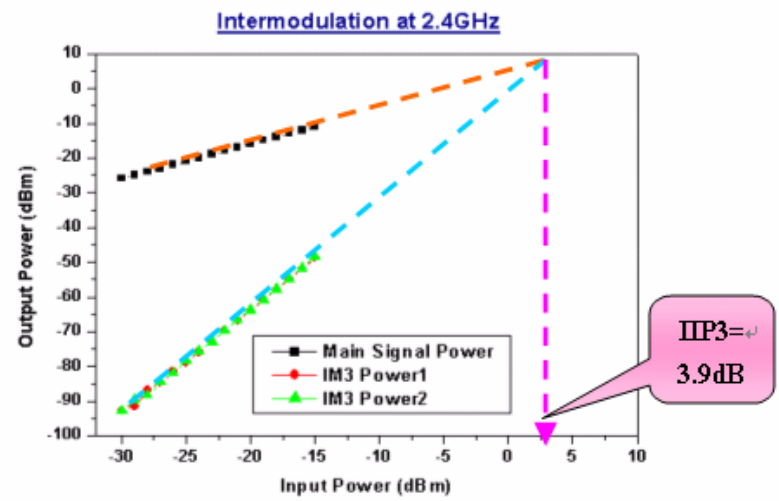


(c)

Fig. 3.5.15 Power Gain vs. Input Power Measurement Results



(a)



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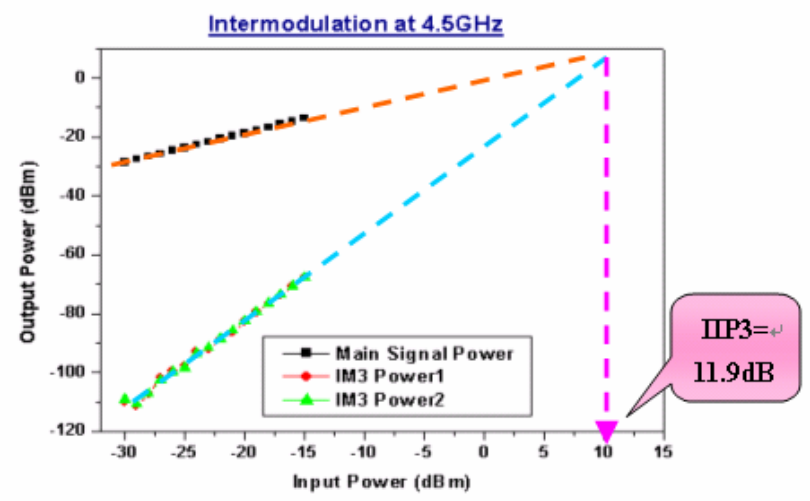


(c)

Fig. 3.5.16 Two-tone Test Measurement Results

Specification	Simulated at 1.8GHz	Measured at 1.8GHz	Simulated at 2.45GHz	Measure at 2.45GHz	Simulated at 5.25GHz	Measured at 4.5GHz
S11 (dB)	-10.2	-23.3	-9.4	-10.9	-19.4	-25.7
S21 (dB)	10.2	5.8	10.5	4.1	11.9	2.7
S22 (dB)	-16.3	-6.9	-15.6	-4.3	-12.4	-6.7
S12 (dB)	-67.1	-35.0	-65.1	-30.7	-55.4	-47.9
NF (dB)	3.7	6.0	4.8	7.6	6.4	10.3
P_{1dB} (dBm)	-7.8	-5.0	-9.8	-6.2	-6.9	0
IIP_3 (dBm)	1.7	4.9	0	3.9	4.5	11.9
Power & Current	Simulated	Id=15.6mA Power consumption=39.1mW				
	Measured	Id=15.5mA Power consumption=38.8mW				

Table 3.5.2 Simulation and Measurement Performance Summary

Chapter 4

CMOS Double-Balance Mixer Merged LNA Design and Implementation

4.1 Review of Double-Balanced Gilbert Mixer

Being the indispensable element of the receiver chain, the mixer always plays an important role as a frequency-translation device in the communication system. It is also one of the most critical building blocks in modern integrated radio frequency transceivers for wireless communications. It can perform frequency translation to a higher frequency (up-conversion) or to a lower frequency (down-conversion). Such mixers are nonlinear devices no matter which are made of diodes or transistors, so we can use trigonometric identities:

$$A\cos(\omega_{RF}t)B\cos(\omega_{LO}t)=\frac{AB}{2}[\cos(\omega_{RF}+\omega_{LO})t+\cos(\omega_{RF}-\omega_{LO})t]\text{------Eq. (1)}$$

$$A\cos(\omega_{RF}t)B\sin(\omega_{LO}t)=\frac{AB}{2}[\sin(\omega_{RF}+\omega_{LO})t-\sin(\omega_{RF}-\omega_{LO})t]\text{-------Eq. (2)}$$

to obtain the up-converted and down-converted frequencies $\omega_{RF}\pm\omega_{LO}$. This multiplier relies on the square law of voltage-current relationship to achieve the frequency-translation. In addition, there are several important parameters for determining the performance of Gilbert mixer. These include conversion gain, noise figure, linearity, isolation, and power consumption etc. However, among all of these parameters, conversion gain and linearity are especially important for active or Gilbert mixer. Therefore, it is helpful to realize the detailed definition of these two parameters first before formally introducing our design in the subsequent sections.

4.1.1 Conversion Gain

The simplified diagram of ideal Gilbert Mixer is illustrated in Fig. 4.1.1. [24] The lower stage is operated as an ideal transconductance amplifier that magnifies RF signals with transconductance (g_m). Then, the output current of the transconductance amplifier can be expressed as:

$$I = g_m V_{RF}(t)$$

Suppose that upper stage is worked as a perfect LO switch function as shown in Fig.4.1.2. It can be expressed as a square function of $T(t) = T_1(t) + T_2(t)$ and can be represented by Fourier series as follows:

$$T_1(t) = \frac{1}{2} + \frac{2}{\pi}\left[\sin(\omega_{LO}t) + \frac{1}{3}\sin(3\omega_{LO}t) + \ldots\right]$$

$$T_2(t) = -\frac{1}{2} + \frac{2}{\pi}\left[\sin(\omega_{LO}t) + \frac{1}{3}\sin(3\omega_{LO}t) + \ldots\right]$$

The square wave only includes odd-order LO harmonics in spectrum. Finally, the IF output is:

$$V_{IF}(t) = g_m R_L T(t) V_{RF}(t) = AT(t) V_{RF}(t)$$

The even-order LO harmonics and DC offset have been canceled out of the LO spectrum due to the symmetry of doubled-balanced structure. There will be LO harmonics appearing at $3\omega_{LO}$ and $5\omega_{Lo}$ etc. These will also mix with all RF input signals to produce spurious signals at IF outputs. If LO signal is multiplied by a single frequency cosine at ω_{RF}, the desired sum and difference outputs $V_{IF}(t)$ are:

$$V_{IF}(t) = AV_{RF}\cos(\omega_{RF}t)\cdot\frac{4}{\pi}\left[\sin(\omega_{LO}t) + \frac{1}{3}\sin(3\omega_{LO}t) + \frac{1}{5}\sin(5\omega_{LO}t) + \ldots\right]$$

Then, using trigonometric identity (2), we have second-order IF output:

$$V_{IF(2nd-order)}(t) = AV_{RF}\cos(\omega_{RF}t)\cdot\frac{4}{\pi}\sin(\omega_{LO}t)$$

$$= \frac{2AV_{RF}}{\pi}\left[\sin(\omega_{RF} + \omega_{LO})t - \sin(\omega_{RF} - \omega_{LO})t\right]$$

at $\omega_{RF} \pm \omega_{LO}$, that are the desired up-converted and down-converted products from the MOSFET Gilbert mixer. Therefore, conversion gain can be obtained as following definition and above derivation. [24]

$$Conversion\_Gain \equiv \frac{Desired\_IF\_Output\_Power}{RF\_Input\_Power} \approx \frac{2g_m R_L}{\pi}$$

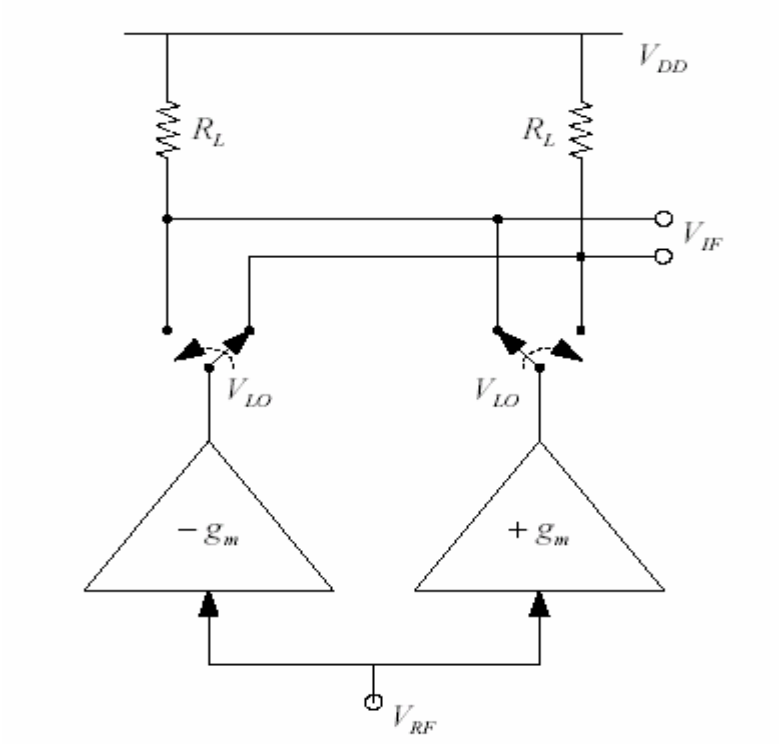


Fig. 4.1.1 Simplified diagram of ideal Gilbert Mixer

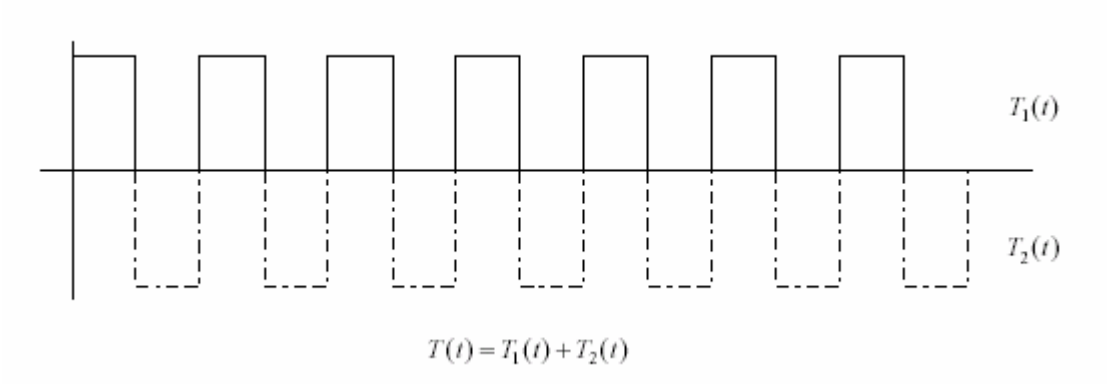


Fig. 4.1.2 LO switch function

4.1.2 Two-tone Linearity

Before the discussion of two-tone intermodulation performance, a basic IIP_3 mathematic derivation for nonlinear system must be introduced first. For a memoryless nonlinear system as shown in Fig.4.1.3, the input-output relationship can be approximated with a polynomial:

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t)$$

Here, we have neglected dc and higher-order components. If a two-tone sinusoid signal is applied to a nonlinear system, it will leads to the intermodulation. Assume $x(t) = A_1 \cos\omega_1 t + A_2 \cos\omega_2 t$. Thus,

$$y(t) \approx \alpha_1 (A_1 \cos\omega_1 t + A_2 \cos\omega_2 t) + \alpha_2 (A_1 \cos\omega_1 t + A_2 \cos\omega_2 t)^2$$
$$+ \alpha_3 (A_1 \cos\omega_1 t + A_2 \cos\omega_2 t)^3$$

Expanding and discarding dc terms and harmonics, we can obtain the following intermoedulation products:

$$\omega = \omega_1 \pm \omega_2 \rightarrow \alpha_2 A_1 A_2 \cos(\omega_1 + \omega_2)t + \alpha_2 A_1 A_2 \cos(\omega_1 - \omega_2)t$$
$$= 2\omega_1 \pm \omega_2 \rightarrow \frac{3\alpha_3 {A_1}^2 A_2}{4} \cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 {A_1}^2 A_2}{4} \cos(2\omega_1 - \omega_2)t$$
$$= 2\omega_2 \pm \omega_1 \rightarrow \frac{3\alpha_3 {A_2}^2 A_1}{4} \cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 {A_2}^2 A_1}{4} \cos(2\omega_2 - \omega_1)t$$

and these fundamental components:

$$\omega = \omega_1, \omega_2 \rightarrow \left(\alpha_1 A_1 + \frac{3}{4}\alpha_3 {A_1}^3 + \frac{3}{2}\alpha_3 A_1 {A_2}^2\right)\cos\omega_1 t$$
$$+ \left(\alpha_1 A_2 + \frac{3}{4}\alpha_3 {A_2}^3 + \frac{3}{2}\alpha_3 A_2 {A_1}^2\right)\cos\omega_2 t$$

For two equal-amplitude tone of signals $A_1 = A_2 \equiv A$, then:

$$y(t) \approx \left(\alpha_1 + \frac{9}{4}\alpha_3 A^2\right) A\cos\omega_1 t + \left(\alpha_1 + \frac{9}{4}\alpha_3 A^2\right) A\cos\omega_2 t$$
$$+ \frac{3}{4}\alpha_3 A^3 \cos(2\omega_1 - \omega_2)t + \frac{3}{4}\alpha_3 A^3 \cos(2\omega_2 - \omega_1)t$$

If $\alpha_1 >> 9\alpha_3 A^2/4$, the input level for which the output components at ω_1 and ω_2 have the same amplitude as those at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ is given by:

$$|\alpha_1| A_{IP3} = \frac{3}{4}|\alpha_3| A_{IP3}^3$$

Thus, the input IP_3 is:

$$A_{IP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \quad \text{----- Eq. (3)}$$

and the output IP_3 is equal to $\alpha_1 A_{IP3}$.

Let us denote the input level of at each frequency by A_{in}, the amplitude of the output components at ω_1 and ω_2 by $A_{\omega 1,\omega 2}$, and the amplitude of the IM_3 products by A_{IM3}. Then, we have

$$\frac{A_{\omega 1,\omega 2}}{A_{IM3}} \approx \frac{|\alpha_1| A_{in}}{3|\alpha_3| A_{in}^3/4} = \frac{4|\alpha_1|}{3|\alpha_3|}\frac{1}{A_{in}^2}$$

which, in conjunction with Eq. (3), reduce to

$$\frac{A_{\omega 1,\omega 2}}{A_{IM3}} = \frac{A_{IP3}^2}{A_{in}^2}$$

Consequently,

$$20\log A_{\omega 1,\omega 2} - 20\log A_{IM3} = 20\log A_{IP3}^2 - 20\log A_{in}^2$$

and

$$20\log A_{IP3} = \frac{1}{2}\left(20\log A_{\omega 1,\omega 2} - 20\log A_{IM3}\right) + 20\log A_{in} \quad \text{----- Eq. (4)}$$

or

$$IIP_3(dBm) = \frac{1}{2}\left[P_{\omega 1,\omega 2}(dBm) - P_{IM3}(dBm)\right] + P_{in}(dBm)$$

$$= \frac{1}{2}\Delta P(dB) + P_{in}(dBm)$$

As shown in Fig. 4.1.4, it is a quick method of measuring the IIP_3. In Fig.4.1.4 (a), if all the signal levels are expressed in dBm, the input third intercept point is equal

to half the difference between the magnitudes of the fundamentals and the IM_3 products at the output plus the corresponding input level. The key point here is that IP_3 can be measured with only one input level, obviating the need for extrapolation.

Shown in Fig. 4.1.4 (b) is a geometric interpretation of the above relationship. Since Line L_1 has a slope equal to unity and line L_2 a slope equal to 3, an input increment $\Delta P/2$ yields an equal increment in L_1 and an increment equal to $3\Delta P/2$ in L_2, reducing the difference between the two lines to zero.

The above approach provides an estimation of IP_3 in initial phases of the design characterization. The actual value of IP_3, however, must still be obtained through accurate extrapolation to ensure that all nonlinear and frequency-dependent effects are taken into account. [25]

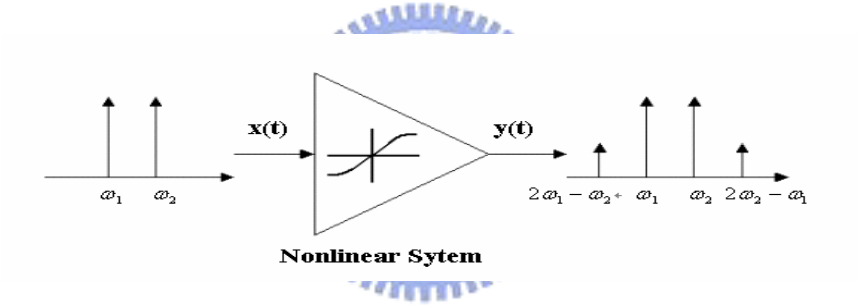
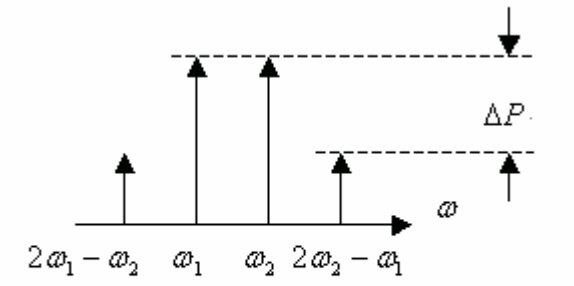


Fig. 4.1.3 Memoryless Nonlinear system with Two-tone Test



$$IIP_3(dBm) = \frac{\Delta P(dB)}{2} + P_{in}(dBm)$$

Fig. 4.1.4 (a) Calculation of IP_3 without extrapolation

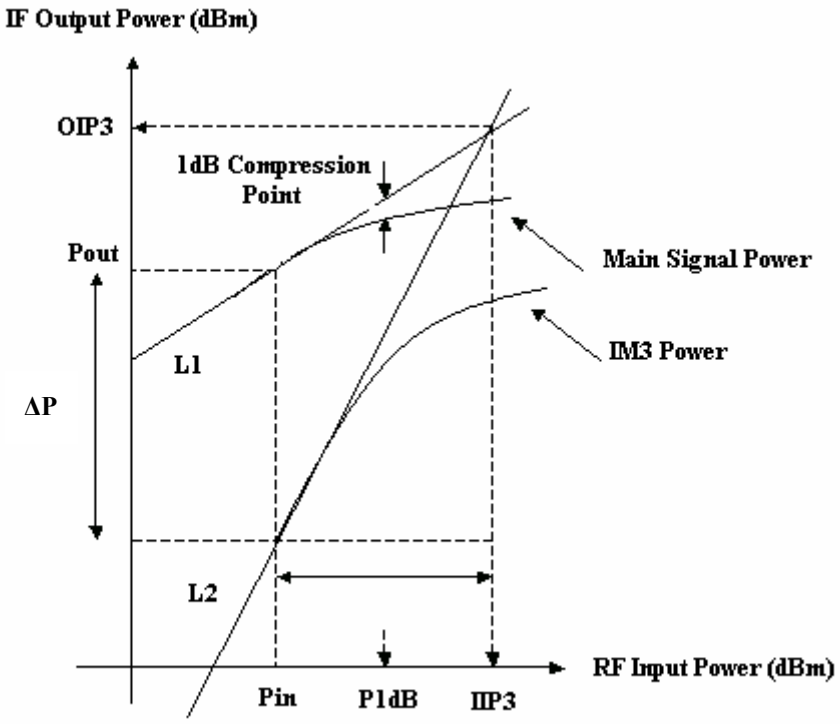


Fig. 4.1.4 (b) Graphical interpretation of Two-tone Test IIP_3

The Gilbert mixer is fully differential that means any common mode noise from the LO, RF ports or even substrate will be suppressed at the IF output. Besides, such double-balanced mixer is expected to have very good RF-to-IF and LO-to-IF isolation performance. In addition, all even-order harmonics at the two IF output ports are canceled by the differential output. Note that such good performances greatly depend on the switching behavior and transistors working region.

For low cost and high integration consideration, CMOS process has become one of the most popular technologies to provide excellent integration with other base-band blocks. For many years, CMOS Gilbert mixer as shown in Fig. 4.1.5 has been favored in many integrated circuit applications for its linearity, noise performance, high bandwidth, and port-to-port isolation. [8][26] Similar to Fig. 4.1.1, transistors M1p & M1n form the input transconductors, which convert input RF voltage signals into current signals. Then current signals are delivered to different commutating switches

branches, transistors M2p,n and M3p,n, which are turned on and off current signals by the local oscillator signal accordingly. Finally, such switching activities perform multiplication of the RF current signals with the local oscillator signals. In practice, the switching voltages at transistor bases are not ideal square waves and even have rather large rise and fall times. This multiplication relies on the square law of voltage-current relationship to achieve the frequency-translation. In the low-If frequency, using the resistors as loads can reduce the flicker noise and the differential IF signal is then output from these two loads.

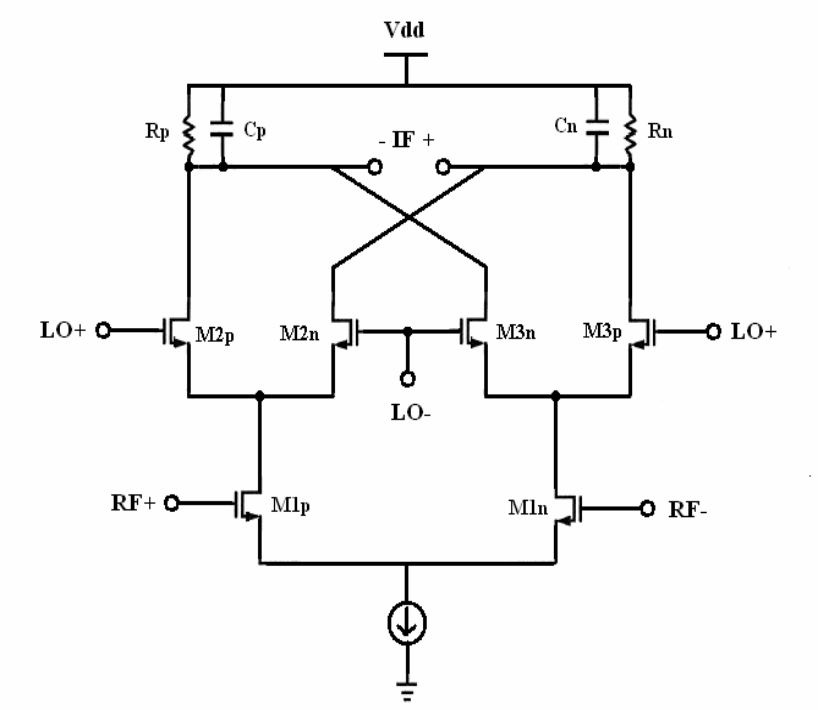


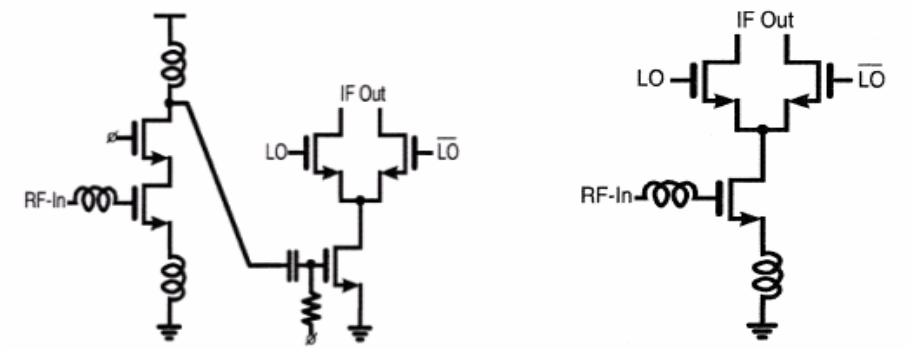
Fig. 4.1.5 CMOS Gilbert Mixer

4.2 Architecture of Double-Balanced Mixer Merged LNA

4.2.1 Comparison Between Conventional and Merged LNA & Mixer

RF designs are increasing taking advantage of advanced CMOS technology that is capable of integration for whole communications system. The use of CMOS

technologies for implementation of the front-end circuits is therefore attractive because of the promise of integrating whole chip system on a single chip. However, a more linear RF CMOS front-end circuit is indeed necessary to be implemented in modern wireless communications, such as WCDMA receiver front-end. [27] Before introducing the merged LNA and Mixer, let us start with the shortcomings of the cascade of a conventional LNA and mixer as shown in Fig. 4.2.1(a). The single-ended NMOS LNA should be an inductive source degeneration cascode topology and its output should be tuned to the band of interest using an inductor. The LNA could be coupled into an NMOS single-balanced mixer through a coupling capacitor. The LNA input transistors convert the incoming signal into current, which then translate to voltage across the inductor load. This voltage drives the transconductance input of the mixer, which converts the signal into current once again. Finally, the mixer differential pairs commutate this current and translate it into IF signal, to be read off at the mixer output as voltage.



(a) **(b)**

Fig. 4.2.1 (a) Conventional Cascade LNA and Mixer

(b) LNA Merged into Commutating Mixer pair

Large signal swing interferer may exist in a strong adjacent channel and drive the LNA cascode FET or the mixer input FET into the triode region. Furthermore, this interferer will force the mixer into compression at the intermediate node where the

LNA feeds. If we can eliminate this node, it will remove the associated bottleneck to linearity. Instead of cascading the LNA and Mixer in voltage, the commutating differential pair of the mixer may be cascaded in current as shown in Fig. 4.2.1(b). The lower FET is now a transconductor designed for low input noise and good input matching simultaneously. It amplifies the input signal into current and feeds it directly into the commutating differential pairs comprising the mixer. We can consider this circuit as a current-mode cascade of LNA and mixer, or simply as a low-noise mixer whose input impedance is optimized good noise matching at RF frequency. [6]

In the same way, we can then develop a modified version of the current-mode cascade topology in advanced. A doubled-balance mixer merged the differential LNA is shown in Fig. 4.2.2. [6] This circuit is realized with a differential LNA coupled into the tail of the commutating differential mixer pair. Although the intermediate node is eliminated, the linearity of this circuit is still limited at two different points. At the input port, it is limited by the bias $V_{GS} - V_t$ of the input FETs and the voltage gain in the matching circuit. At the output port, too large a negative voltage swing across the load resistor might force LNA drain into triode. However, we can optimize the linearity performance by carefully setting these bias points.

Since the circuit is intended for low-IF application, flicker noise at the mixer output is of concern [28]. An inductor resonating with parasitic capacitances at the tails of the mixer differential pairs will lower the effect of mixer flicker noise. [6] This will be also explained in the subsequent section. Besides, since the resistive loads are, of course, free of flicker noise, we can choose the resistors as mixer loads instead of the active PMOS loads to improve the noise performance. Finally, in addition to improving linearity, since two power-hungry blocks, LNA and Mixer, are merged into one, such stacking cascode architecture will also reduce power consumption and save area or cost as compared to the fundamental cascade LNA and Mixer.

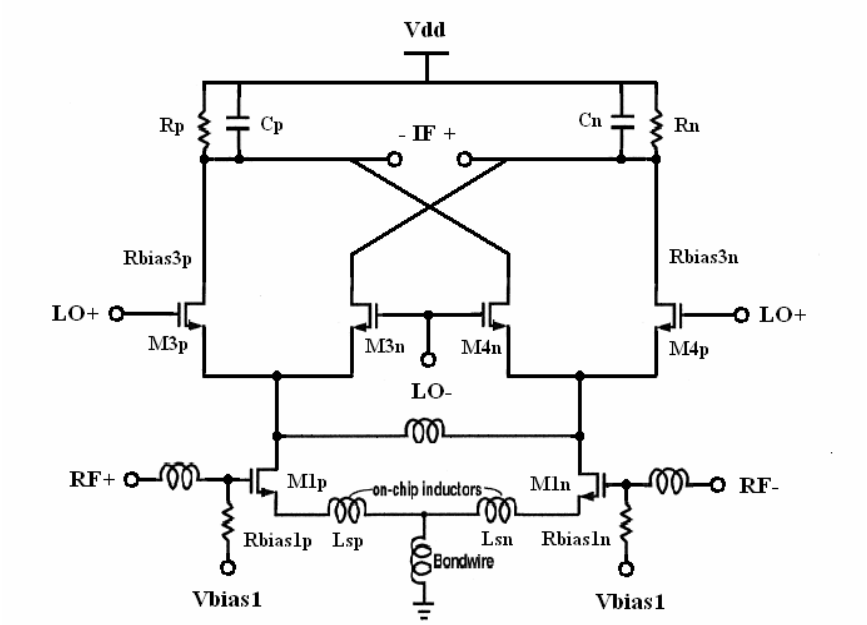


Fig. 4.2.2 Conventional Doubled-Balanced Mixer Merged LNA

4.2.2 Architecture of Proposed Modified Merged LNA & Mixer

In this section, we propose a modified merged LNA and Mixer circuit as shown in Fig. 4.2.3 based on above architecture. [6] Two kinds of improving mechanisms are included in this circuit. First, in a conventional LNA and mixer, the unilateral nature of the mixer's input FET and cascode FET in the LNA substantially isolates the mixer LO port from the LNA input port. While these FETs are not present in the merged LNA and mixer, the LO input signal strongly couple to the LNA input. So that two common-gate NMOS transistors (M2p & M2n) are added between common-source LNA and the tail of commutating mixer pair to improve LO-to-RF Isolation. These two additive transistors also make the original LNA become the common-source cascode LNA. This cascode configuration can be used to enhance gain, frequency response, stability, reverse isolation, and also reduce Miller effect. [18] Second, two PMOS transistors (Mb1 & Mb2) are also introduced to original circuit. These two transistors simultaneously act as not only bleeding current sources to improve

linearity, noise figure, gain, and LO isolation [29-30] but small signal common-source amplifiers to achieve higher gain through two coupling capacitors (Cc1 & Cc2). [30] The detail analysis will be described in subsequent section.

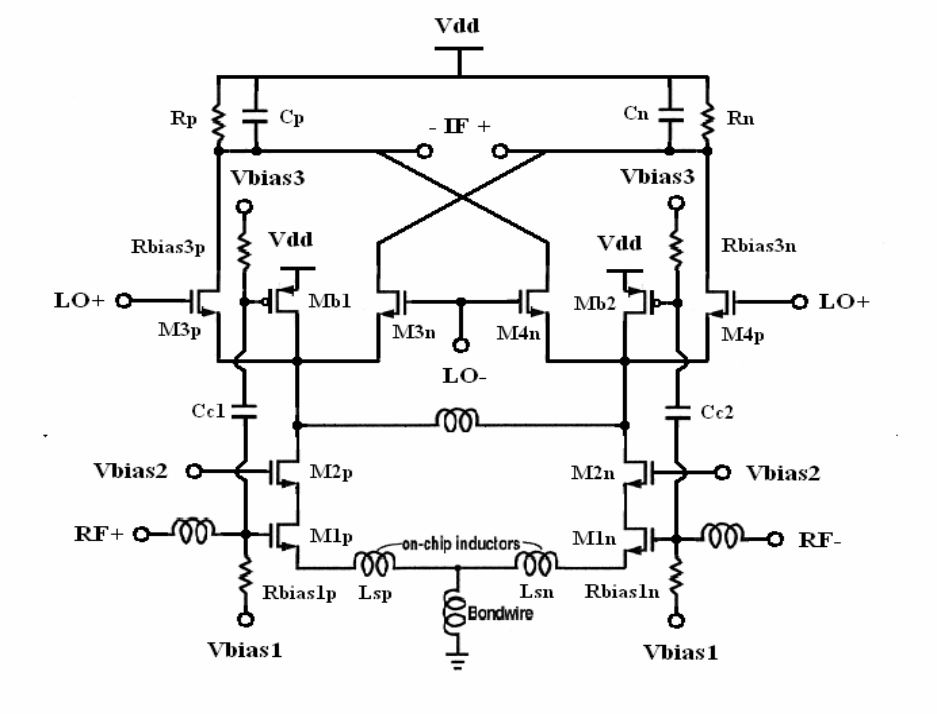


Fig. 4.2.3 The Modified Merged LNA and Mixer Circuit

Besides, capacitors (Cp & Cn) and resistive loads (Rp & Rn) across the mixer loads act as low-pass filters to filter out undesired signals and strong feedthrough from LO. In this circuit design, since low-IF frequency is chosen as 10MHz, so we have set the capacitors of filters as 6.4 pF and the resistors as 736Ω. Such setups will result in a cutoff frequency of 34MHz as desired. For measurement purpose, we also have connected an on-chip common-drain output buffer as shown in Fig.4.2.4 to simultaneously achieve IF port output matching to 50Ωand increase output driving capability. Finally, we take advantage of π-matching circuits and coupling capacitors as shown in Fig. 4.2.5 to achieve good LO input matching to 50Ω and be able to provide the mixer enough LO power from outside signal generator. In the subsequent sections, we will demonstrate that this proposed modified circuit topology could meet our design ideas through SPICE post simulation and measurement results.

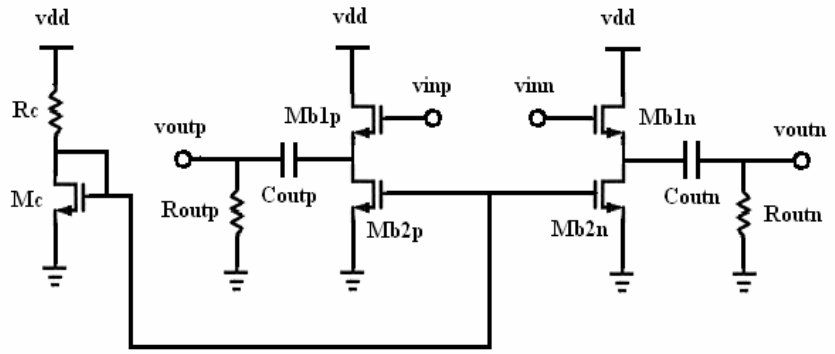


Fig. 4.2.4 Common-Drain Output Buffer

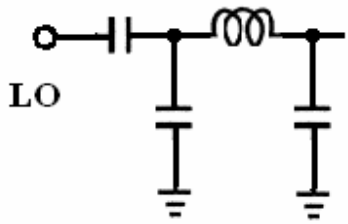


Fig. 4.2.5 π-matching circuit and coupling capacitor

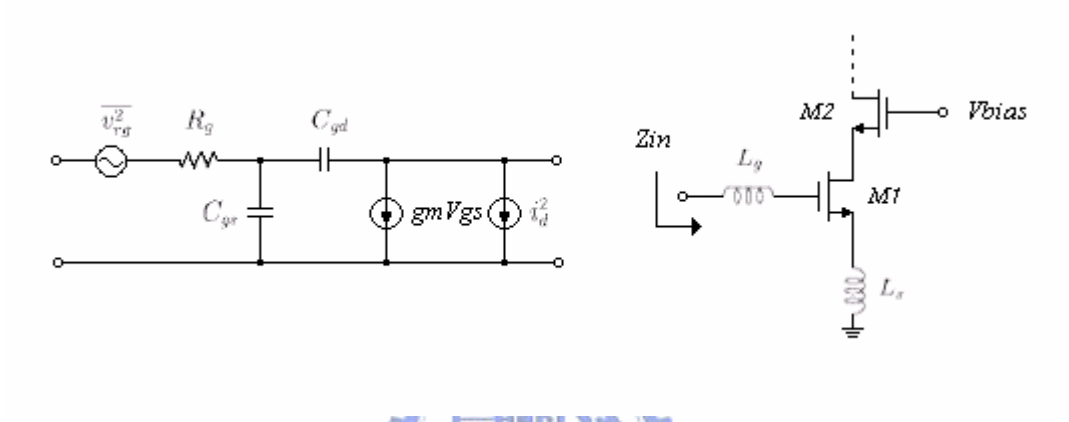
4.3 Design and Analysis of Double-Balanced Mixer Merged LNA

4.3.1 Design and Analysis of LNA Part

The design and analysis of double-balanced mixer merged LNA can be separated into two parts. In the design of the LNA part, we can follow the original inductive source degeneration LNA design guidance. [18] There are several common goals in the design of LNA. These includes minimizing the noise figure, providing high gain with sufficient linearity to overcome the noise of subsequent circuits, a stable 50Ω good input matching, and low power consumption etc. Fig. 4.3.1 illustrates the standard CMOS noise model and common-source input stage of LNA. A simple analysis of the input impedance shows that:

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \left(\frac{g_{m1}}{C_{gs}}\right)L_s \approx \omega_T L_s \quad \text{(at resonance)}$$

At the serious resonance of the input circuit, the impedance is purely real and proportional to L_s. To pick up appropriate value of L_s, this real term can be matched to 50Ω. The gate inductance L_g is used to set the resonance frequency once L_s is chosen to satisfy the criterion of a 50Ω input impedance.



(a) **(b)**

Fig. 4.3.1 (a) Standard CMOS noise model (b) The input stage of LNA

One of the most important things in the design of LNA is to pick up the appropriate device width and bias point to optimize noise performance and to obtain the largest dynamic range and linearity in given specific objectives for gain and power dissipation. Because the detailed analysis procedure has been made in Section 3.4 (design and analysis of concurrent triple-band LNA), we have omitted the redundant analysis here. As in any LNA, the higher the transit frequency f_T of transistor is the better performance of LNA is. So the channel length of MOS is selected as the minimum value (0.25μm) here. Accordingly, the optimum width of FET in LNA is selected as 240μm. Choosing the appropriate bias value of $V_{GS} - V_t$ for the desired IIP_3 will lead to a dc current drawing of about 7mA per one side. [31] With these MOS width and bias point, we can now decide the source degeneration and gate

inductance to obtain a narrow-band input matching to 50Ω. It should be noted that the relatively small inductance of L_s is less than the inductance of a bond-wire and a package lead. Since the circuit is differential, the source degeneration inductors are integrated as small on-chip spirals and then center tapped to ground through the bond-wire and package lead. As only the common-mode dc and even harmonics flow to ground, the bond-wire and lead inductance do not affect the differential input impedance of LNA.

4.3.2 Design and Analysis of Mixer Part

In the mixer part, the design and analysis of the commutating mixer differential pair is similar to that of double-balanced Gilbert mixer described in Section 4.1. The mixer here also takes advantage of resistively loads. Although the series load resistors consume valuable dc voltage headroom, they are free of flicker noise, occupy less area, and are more suitable for low-IF output. For example, a differential load with active PMOS pull-up current sources or passive spiral inductors can operate with lower headroom, but the former suffers from large flicker noise. However, the latter occupies great area and can't operate in such a low frequency with high Q value.

The FETs in the commutating differential pair also contribute noise as it passes through the balance point. Signal-dependent current division in the differential pair also creates nonlinearity. Sharp LO transitions can alleviate both mixer noise and nonlinearity. The time for the pair to transition through its active region is inversely proportional to the LO amplitude and proportional to the gate overdrive of the pair's FETs biased at balance. Although the larger amplitude of the LO can reduce this transition time, it will force the switch FETs into deep triode, shorting the LNA drains to the resistor loads and worsening overall linearity. [6] Besides, the large LO swing is not practical in realized integrated on-chip VCO.

4.3.3 Design and Analysis of Merged LNA & Mixer Circuit

The linearity and conversion gain of whole merged LNA & Mixer circuit are proportional to the square root of LNA drive stage bias current. For the requirements of high linearity, gain, and low noise in the LNA part, the bias current of each branch is quite large and it will force the reduction of load resistors and conversion gain. Therefore, we have taken advantage of the bleeding current sources to resolve these problems. [29][30] The bleeding current sources can allow a higher conversion gain through the higher load resistors because part of the driver stage current is being steering from the switching transistors. Furthermore, the gate overdrive $V_{GS} - V_t$ can also be lowered by such reducing bias current of each switch FET even for smaller transistor size. In either case, for a given level of LO signal, bleeding helps to improve the conversion efficiency as lower charges are necessary to turn them on and off the switch FETs of mixer pair. In addition, the bleeding current sources are also used as part of the driving stage amplifiers to improve the gain performance and reduce the noise figure. Moreover, the higher overall transconductance reduces the noise figure and nonlinearity. [32][33] The major disadvantage is the addition of noise signals due to the present of the bleeding active devices.

Slowly varying flicker noise at the gate of mixer FETs appears as flicker noise at the mixer output through two mechanisms. [28] First, a direct mechanism, it modulates the instants of zero crossing of the tail current. Second, an indirect mechanism, it induces current in the tail capacitance that is commutated to the output. Large LO amplitude lowers the direct mechanism. A floating on-chip inductor between the two mixer RF inputs tunes out the tail capacitance at the LO frequency to suppress the indirect mechanism [28], thus, greatly lowering the mean square flicker noise at the mixer output.

4.4 Simulation and Measurement of Proposed Merged LNA & Mixer

4.4.1 Layout and Simulation Results

A modified double-balanced mixer merged LNA by previous architecture is designed and optimized using TSMC 0.25 μm CMOS technology. The final layout of it is shown in Fig. 4.4.1. All elements are fully integrated on a chip including spiral inductors, MIM capacitors, multi-finger RF MOS transistors, poly resistors, and decouple MOS capacitors. The total chip size including the pads is about 1300umx1400um. It has been fabricated using TSMC 0.25 μm mixed-signal CMOS process. Similarly, we also take advantage of shielded signal PAD as described in Section 3.4.1 to reduce coupling noise from the noisy Silicon substrate. We will show its final simulation and measurement performances latter.

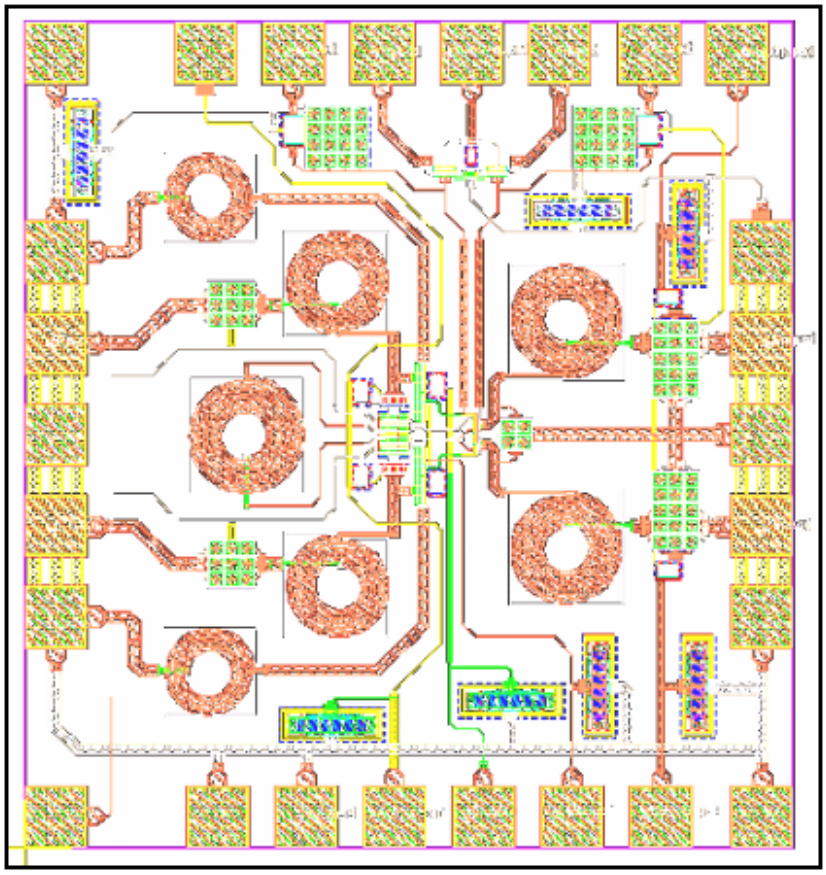


Fig. 4.4.1 Layout of Proposed Double-Balanced Mixer Merged LNA

The RF and LO signal frequencies are designated at 2.1GHz and 2.11GHz, respectively. The output mixing IF signal thus falls at 10MHz. Because this work is designed for PCB on-board testing, the parasitic effects of bond-wires and bond-pads will greatly affect the impedance matching of all ports. For all outside 50Ω instruments, only input power of generators can be delivered into the chip or circuit output power can be received by measurement instruments more efficiently with good input or output impedance matching. Therefore, these parasitic effects must be included and considered throughout all simulation procedure very carefully. Typically, the inductance of bond wire is about 1nH per 1mm length and the parasitic capacitance of a 100umx100um bond-pad is approximate 200fF to the ground.

The SPICE post simulation performances including all parasitic effects are shown in Fig. 4.4.2-9. Fig. 4.4.2 shows RF port input matching to 50ohm with input return loss of 10.9dB at 2.1GHz and Fig. 4.4.3 shows the LO port input matching to 50ohm with input return loss of 25.9dB at 2.11Hz, while LO input power is –7dBm and RF input power is –35dBm. Fig. 4.4.4 shows voltage gain vs. RF input power swept from -70dBm to 0dBm with -7dBm LO input power and 1MΩ load. It exhibits high voltage gain of 20.3dB and V_{1dB} of -13.7dBm. Fig. 4.4.5 shows voltage gain vs. LO input power swept from -20dBm to 10dBm with -35dBm RF input power and 1MΩ load. We can see that the maximum voltage gain is obtained while LO input power is –7dBm. Fig. 4.4.6 shows power gain vs. RF input power swept from -70dBm to 0dBm with -7dBm LO input power and 50Ω load. It also exhibits high power gain of 10.5dB and P_{1dB} of -26.0dBm. Fig. 4.4.7 shows power gain vs. LO input power sweep from -20dBm to 10dBm with -35dBm RF input power and 50Ω load. The maximum power gain is also obtained while input LO power is close to –7dBm. Fig. 4.4.8 presents its NF performance of 6dB. Finally, Fig. 4.4.9 shows the two-tone test IIP_3 simulation result of –4.6dBm.

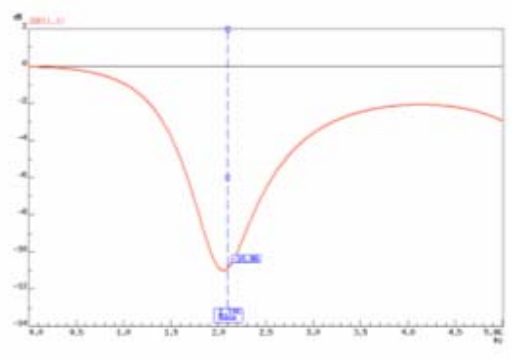


Fig. 4.4.2 RF Port Input Matching

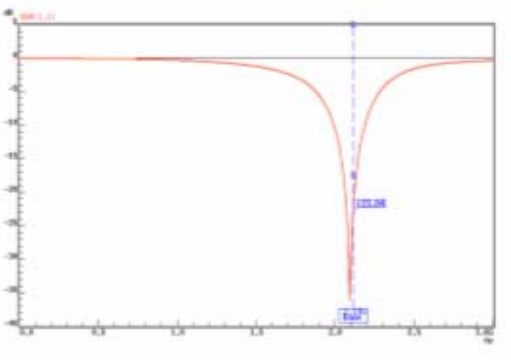


Fig. 4.4.3 LO Port Input Matching

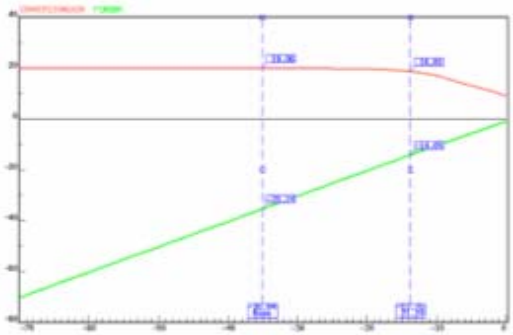


Fig. 4.4.4 Voltage Gain vs. RF Power

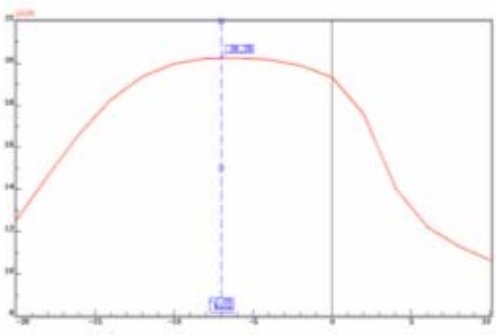


Fig. 4.4.5 Voltage Gain vs. LO Power

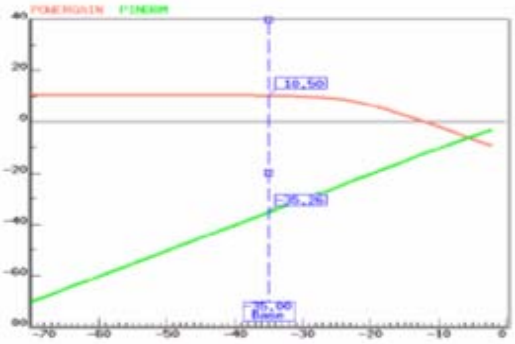


Fig. 4.4.6 Power Gain vs. RF Power

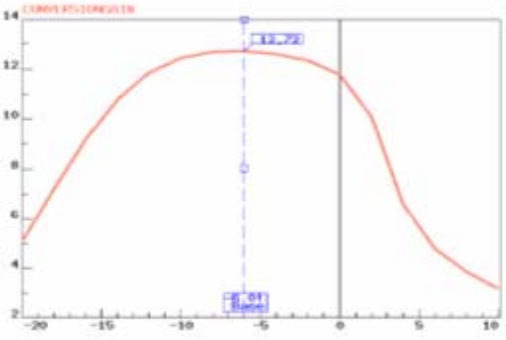


Fig. 4.4.7 Power Gain vs. LO Power

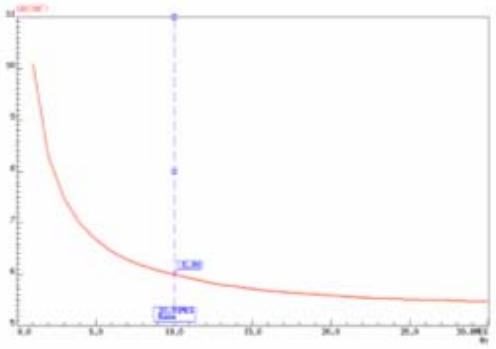


Fig. 4.4.8 Noise Figure

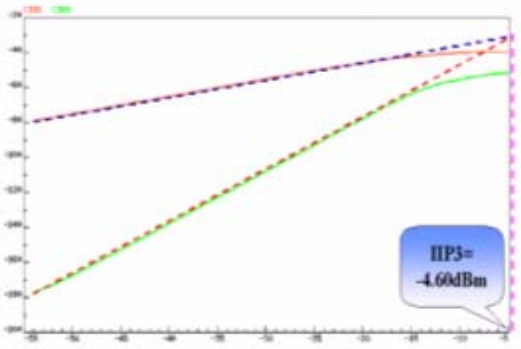


Fig. 4.4.9 Two-tone Intermodulation

These noise and linearity performances are quite good as compared to the conventional cascade LNA and mixer. And it will lead to quite a wide dynamic range. The simulation performances including corner affections are summarized in Table 4.4.1. The proposed merged LNA and mixer circuit dissipates power of 14.4mW (not including power dissipation of output buffer, 6.4mW) from a 2.5V power supply voltage. According to above results, we can conclude that the proposed modified circuit actually exhibits much higher gain, lower noise, higher linearity, better isolation, and wider dynamic range with acceptable low power consumption than the conventional one in CMOS technology.

Specification	TT	FF	SS
RF Input Return Loss (dB)	-10.9	-9.6	-10.5
LO Input Return Loss (dB)	-25.9	-41.4	-20.8
IF Output Return Loss (dB)	-16.2	-18.6	-14.4
Voltage Gain (dB)	20.3	23.2	16.2
Power Gain (dB)	10.5	13.3	7.4
Noise Figure (dB)	6.00	5.1	7.5
V1dB (dBm)	-13.7	-15.0	-12.6
P1dB (dBm)	-26.0	-27.5	-24.0
IIP3 (dBm)	-4.6	-7.97	-4.2
LO-to-RF Isolation (dB)	-81.8	-81.0	-81.8
Power Consumption (mW)	Buffer: 6.4 Core: 14.4 Total: 20.8	Buffer: 6.6 Core: 22.1 Total: 28.7	Buffer: 6.3 Core: 9.4 Total: 15.7

Table 4.4.1 Post Simulation Performance Summary

4.4.2 Measurement Consideration

The simplified block diagram of the PCB on-board testing for our design is illustrated in Fig. 4.4.10. Because of fully differential input/output structures, two extra Baluns are required to transform differential pairs into single-ended port for common single-ended measurement systems. Here, we take advantage of two rat-races (180^0 ring hybrids) as shown in Fig. 4.4.11 to act as such Baluns. The ideal S-parameter of rat-race is as follows:

$$\begin{bmatrix} 0 & 0.707 & 0.707 & 0 \\ 0.707 & 0 & 0 & 0.707 \\ 0.707 & 0 & 0 & -0.707 \\ 0 & 0.707 & -0.707 & 0 \end{bmatrix}$$

It can split the input power from port 4 into output port 2 and port 3 with equal half power and 180^0-phase difference. However, the real S-parameter of rat-race we have designed and implemented is as follows:

$$\begin{bmatrix} 0.046\angle 156.6° & 0.684\angle 105.4° & 0.661\angle 106.3° & 0.018\angle 31.2° \\ 0.692\angle 103.3° & 0.077\angle -99.3° & 0.039\angle 59.1° & 0.676\angle -83.0° \\ 0.676\angle 104.4° & 0.040\angle 55.8° & 0.046\angle -89.1° & 0.700\angle 97.7° \\ 0.017\angle 33.1° & 0.668\angle -81.8° & 0.684\angle 99.3° & 0.093\angle 88.3° \end{bmatrix}$$

Although this experimental result still has little error, it is very close to that of ideal case and satisfied for our requirement.

PCB (printed circuit board) layout and practical FR4 PCB circuit conjunction with SMA connectors for this work are shown in Fig. 4.4.12 and Fig. 4.4.13, respectively. One important thing must be taken care in the design of PCB layout, the width of RF and LO signal paths must be drawn as 50Ω-line width for impedance matching. Besides, we have reserved extra space in the RF signal path for π-matching circuits to prevent and tune back mismatching due to bond-wire length variation. The chip is adhered to PCB first and all I/O pads on this chip are then bonded to PCB via bond-wires. The die photograph of this chip including bond wires

is also shown in Fig. 4.4.14. Throughout all measurement procedures, we still require extra three signal generators, one spectrum analyzer, one network analyzer, and other auxiliary devices, such as cables, 50Ω terminals ,and power combiners. Since we have finished the prior preparations of PCB on-board testing, the measurements can now be proceeding according to arrangements in Fig.4.4.10. It should be noted that the losses of cable, Baluns, SMA connectors, and PCB board itself must be taken account for calibration and calculation in measurement results.

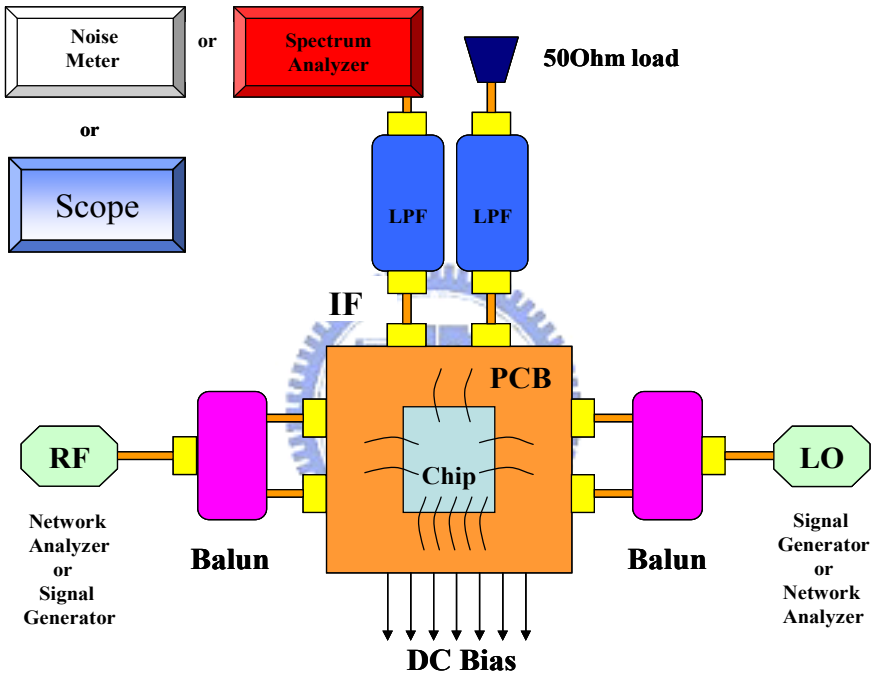
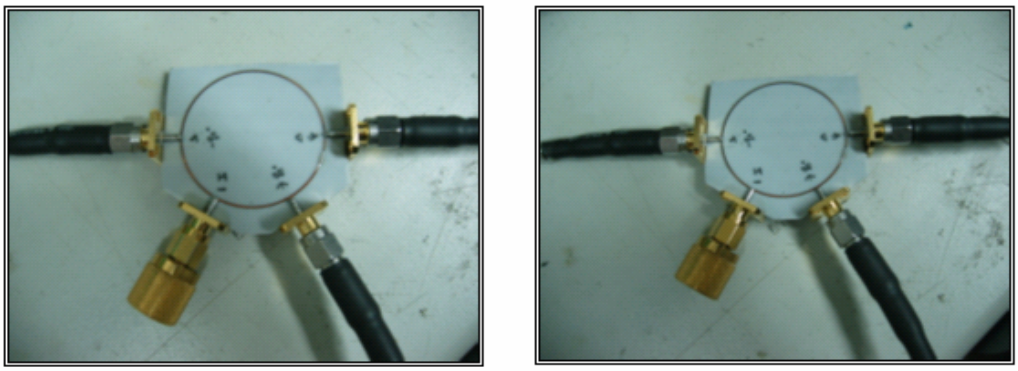


Fig. 4.4.10 Simplified Block Diagram of PCB on-board Testing



(a) **(b)**

Fig. 4.4.11 Photograph of (a) RF Port Rat-race (b) LO Port Rat-race

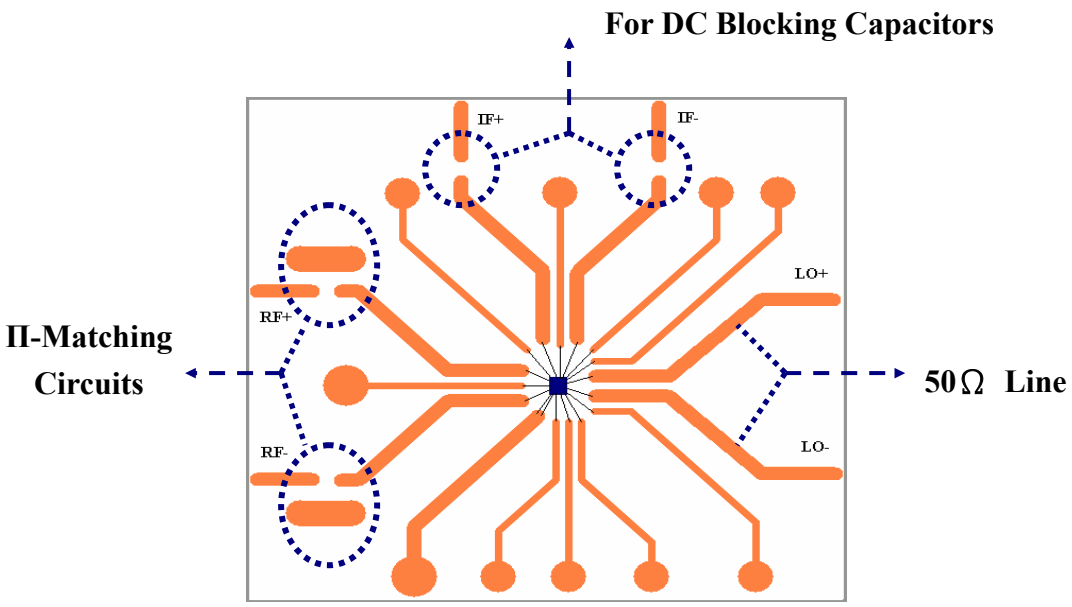


Fig. 4.4.12 PCB Layout

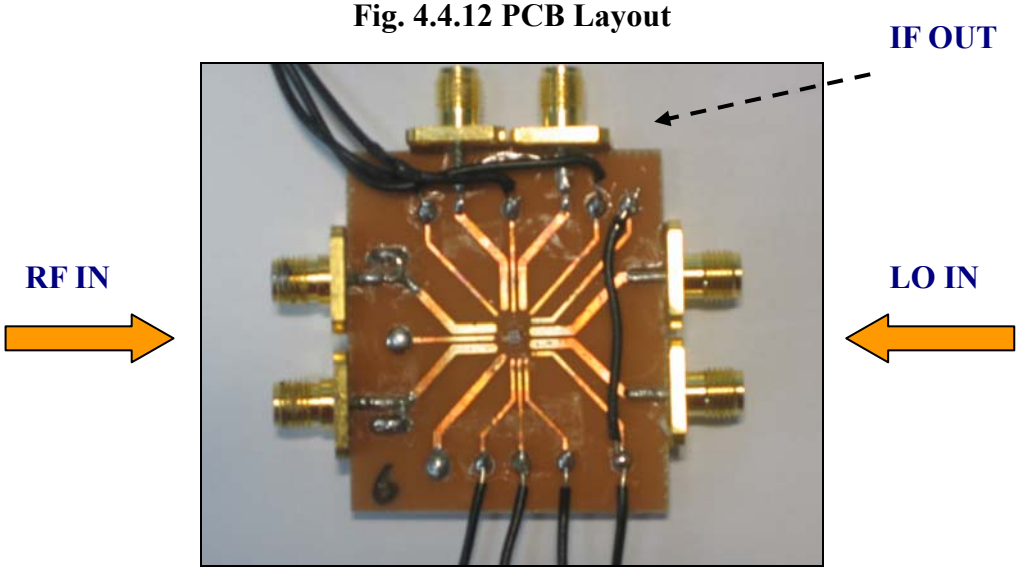


Fig. 4.4.13 Photograph of Practical FR4 PCB circuit

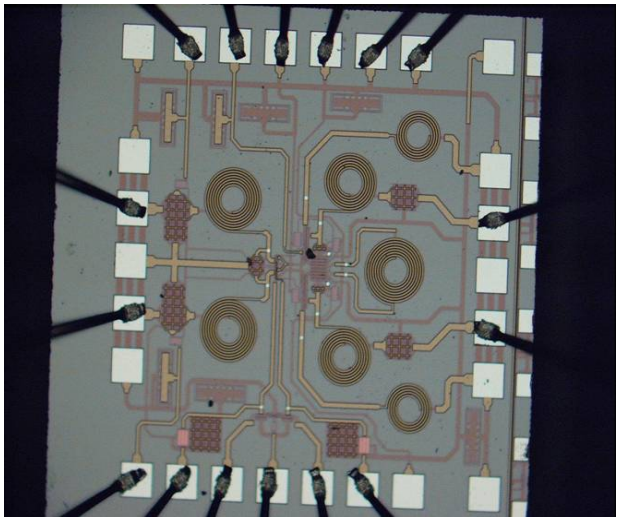
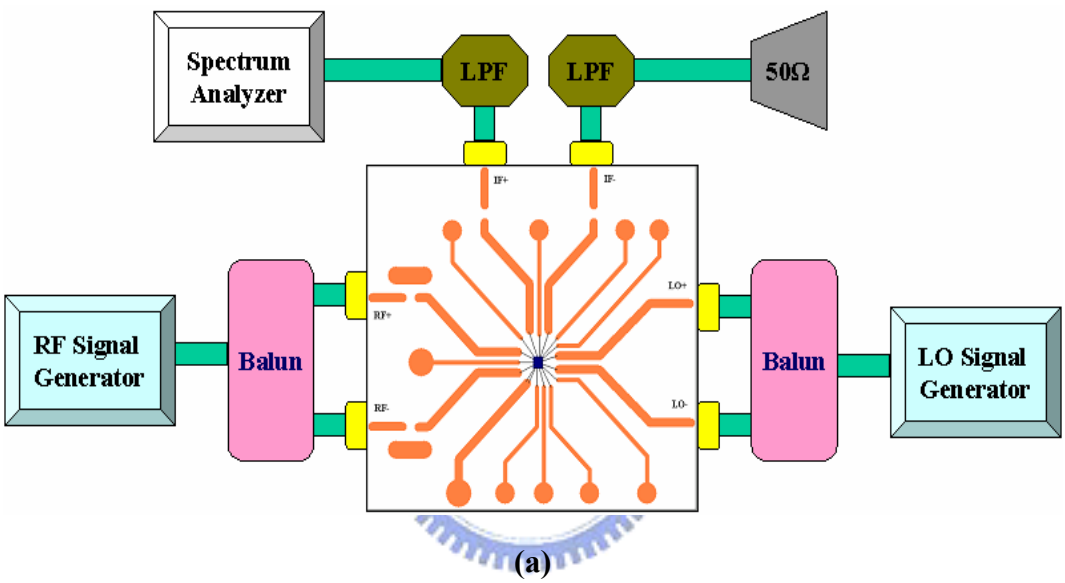
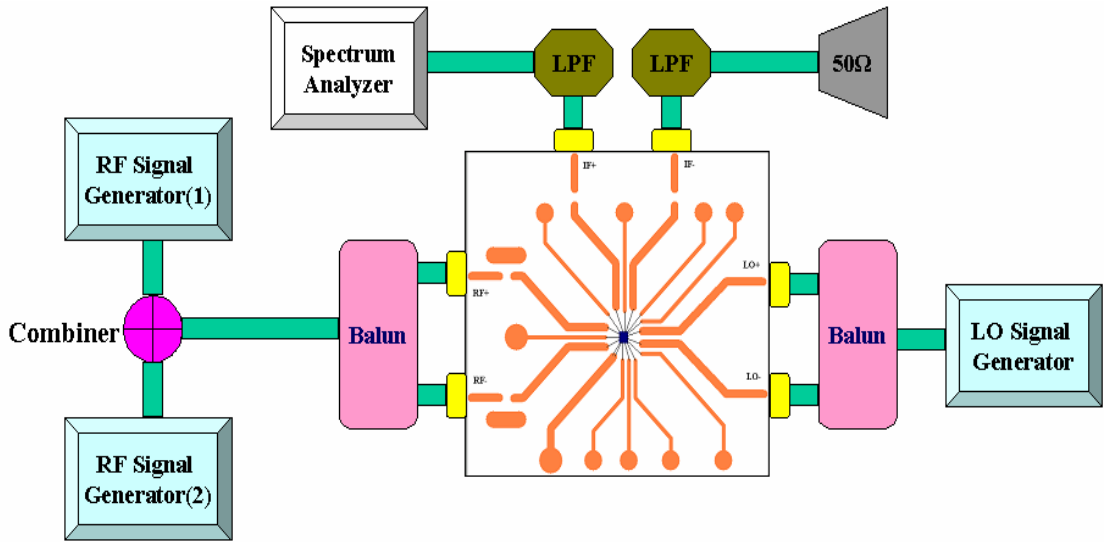


Fig. 4.4.14 Die Photograph of Merged LNA and Mixer

There are some RF parameters that we have to measure in our front-end circuit design of modified double-balanced mixer merged LNA. These parameters include RF & LO input return loss, conversion gain, input one-dB compression point (P_{1dB}), and two-tone linearity test of IIP_3. We have used RFIC measurement systems in CIC and our laboratory to finish these parameter measurements. The simplified block diagrams of each measurement setup for each parameter are illustrated in Fig. 4.4.15.



(a)



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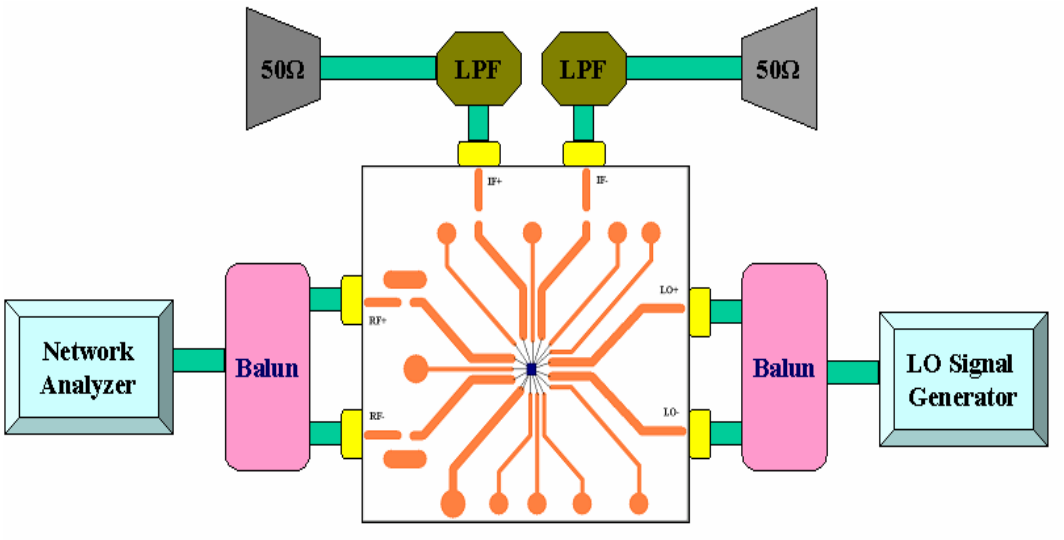


(c)

Fig. 4.4.15 Simplified Block Diagram of Each Measurement Setup for (a) Conversion Gain (b) Two-tone IIP3 Test (c) Input Return Loss

In addition, we also have designed an extra voltage-division circuit that is consisted of variable resistors, OP amplifiers, and batteries as shown in Fig. 4.4.16 for measurements. The purpose of variable-resistors and batteries is to achieve the desired dc bias voltage according to the principle of resistor voltage-division. Furthermore, OP amplifiers act as unit-gain buffers to avoid destruction of the principle of resistor voltage-division. In such a way, in addition to its convenience for our circuit design with so many dc bias points, it also can stable the dc bias supply voltage and measurement results.

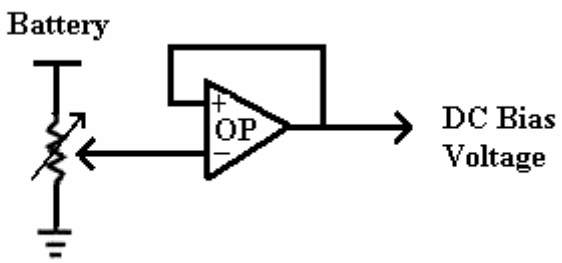


Fig. 4.4.16 Voltage-Division Circuit

4.4.3 Measurement Results

Upon previous measurement considerations and arrangements, we have made all PCB on-board tests for our design in CIC and our Laboratory. In 50Ω measurement system, Fig. 4.4.17 shows the measured RF port input matching including additional effect of π-matching circuit and Fig. 4.4.18 shows the measured LO port input matching from 0.5GHz to 5GHz. It exhibits both good RF port input return loss (RL) of 13.7dB at 2.1GHz and good LO port input RL of 15.3dB at 2.11GHz. The measurement and TT-corner simulation results of power gain versus LO input power are compared and shown in Fig. 4.4.19 where RF input power is fixed with –35dBm. We can see that the maximum measured power gain of 8.3dB can be obtained while LO input power is 0.5dBm. The measurement and TT-corner simulation results of power gain vs. RF input power swept from -50dBm to -12dBm are compared and shown in Fig. 4.4.20 where LO input power is fixed with 0.5dBm in measurement and -7dBm in simulation. It exhibits high measured power gain of 9dB and P_{1dB} of -19dBm. Finally, Fig. 4.4.21 shows the measurement result of two-tone test IIP_3 that is –4.8dBm. It also exhibits high linearity and wide dynamic range. All TT-corner simulation and measurement performances are summarized in Table 4.4.2.

The proposed double-balance mixer merged LNA circuit dissipates total power of 25.1mW, including 18.8mW in core circuit and 6.3mW in output buffer, from a 2.5V power supply voltage. We can see that power dissipation of measurement is a little more than that of TT-corner simulation result in the part of core circuit. However, power dissipation of measurement is very close to that of TT-corner simulation result in the part of output buffer. In fact, the process condition is falling between TT and SF-corner according to WAT data provide by foundry. However, we have made fine tuning for bias condition to optimize measurement results.

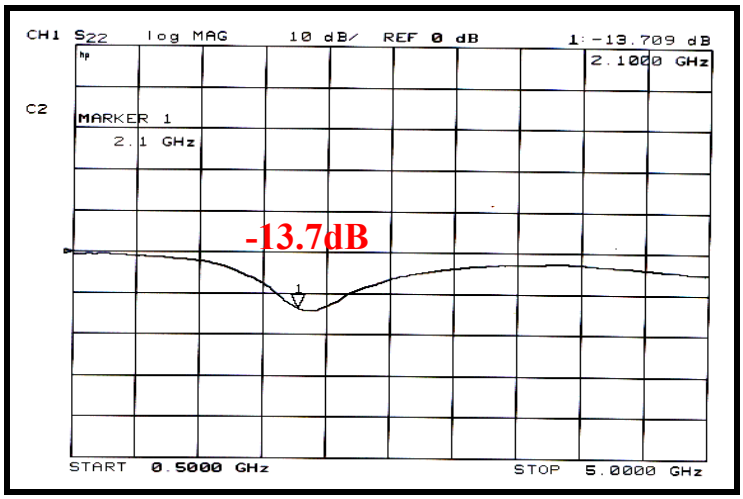


Fig. 4.4.17 Measured RF Port Input Matching

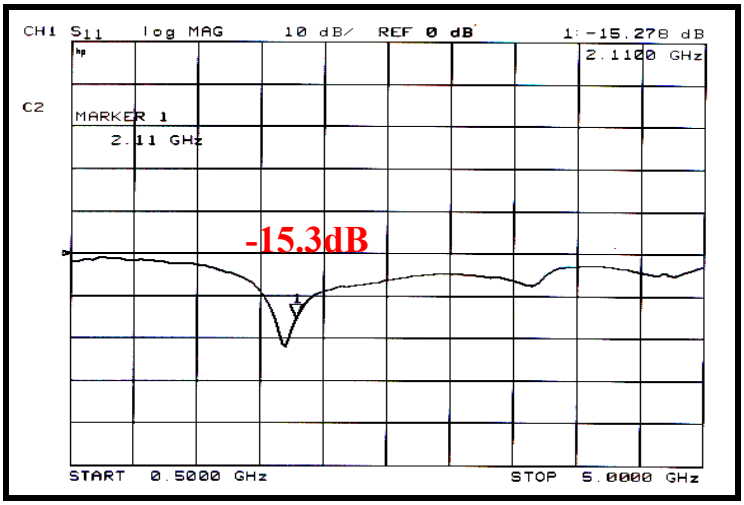


Fig. 4.4.18 Measured LO Port Input Matching

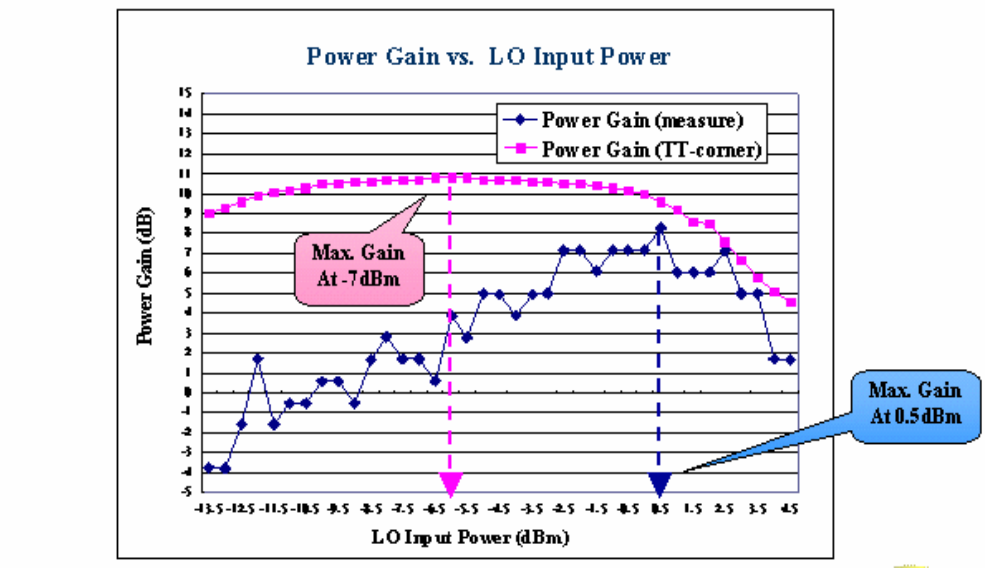


Fig. 4.4.19 Power Gain vs. LO Input Power Comparison

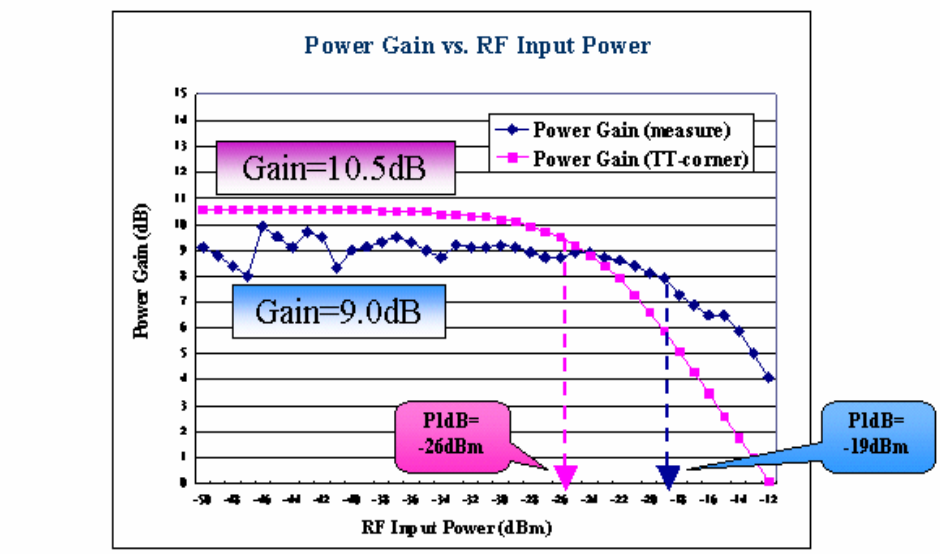


Fig. 4.4.20 Power Gain vs. RF Input Power Comparison

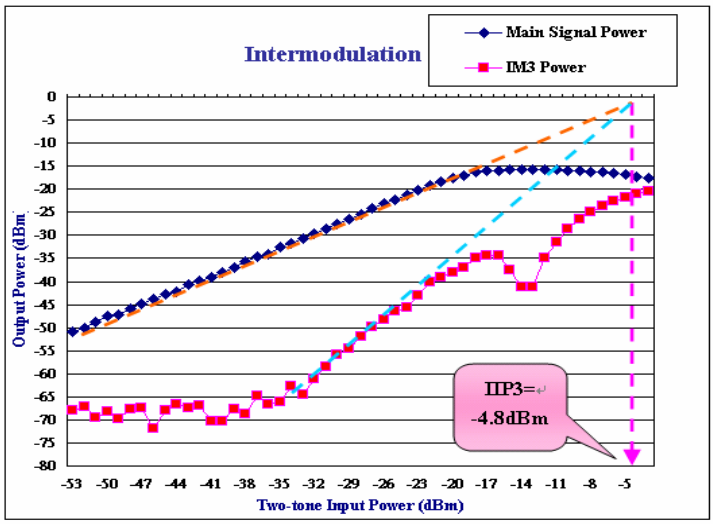


Fig. 4.4.21 Two-tone Test Measurement Result

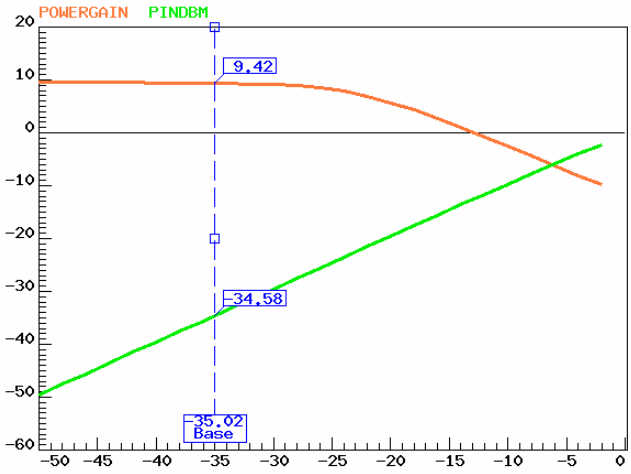


Fig. 4.4.22 Simulated Power Gain vs. RF Power including mismatch effects

Specification	Simulation (TT)	Measurement
RF Port Input RL (dB)	10.9	13.7
LO Port Input RL (dB)	25.9	15.3
IF Port Output RL (dB)	16.2	N/A
Power Gain (dB)	10.5	9.0
Voltage Gain (dB)	20.3	18.2
NF (dB)	6.0	N/A
P1dB (dBm)	-26.0	-19.0
IIP3 (dBm)	-4.6	-4.8
LO-to-RF Isolation (dB)	-81.8	-48.4
Power Consumption (mW) & Current Drawing @ Supply voltage: 2.5V	Buffer: 6.4 (2.6mA) Core: 14.4 (5.8mA) Total: 20.8 (8.4mA)	Buffer: 6.3 (2.5mA) Core: 18.8 (7.5mA) Total: 25.1 (10mA)

Table 4.4.2 Simulation and Measurement Performance Summary

4.4.4 Comparison and Discussion

According to performance comparison result shown in Fig. 4.4.20, we can see that power gain of measurement is about 1.5dB lower than that of TT-corner simulation. There are two major factors to cause it. First, the practical non-ideal rat-race circuits generate deviations of non-equal power and non-180^0-phase difference. In other words, non-ideal differential signal is delivered into RF or LO differential port and this will lower the efficiency of input power from signal generator. Second, there is a little mismatch in original balanced circuit and this will cause asynchronous amplification and mixing of signals. Fig. 4.4.22 shows the simulated power gain vs. RF input power if these effects of mismatch are considered in this work. Just as we expected, this simulation result of 9.4dB power gain is almost equal to the measurement one.

In addition, we can also find in Fig. 4.4.19 that the maximum measured power gain occurs at higher LO input power than TT-corner simulation result. There are also

two major factors to cause it. First, the gate overdrive $V_{GS} - V_t$ of commutating NMOS pair is increasing due to more drain current drawing. As described in Section 4.3.2, the time for the pair to transition through its active region is inversely proportional to the LO amplitude and proportional to the gate overdrive of the pair's FETs biased at balance. So this will cause the requirement of higher LO input swing to achieve the same switching transition time. Second, the non-ideal rat-race circuit will also cause the requirement of higher LO input power.

From comparison results in Table 4.4.2, the linearity performance of two-tone test IIP_3 is very close to the simulation result and the measured P_{1dB} is better than the TT-corner simulated one. In general, lower gain allows higher upper limit of RF input signal swing before transistors enter into triode region and thus leads to a wider dynamic range, so does P_{1dB}. Finally, although LO-to-RF isolation is much lower than the overestimated simulation result, it works very well and meets the requirements for practical circuit application. This also demonstrates that the additional cascode common-gate NMOS transistors are contributive to the improvement of isolation.

In summary, although some performances are a little degraded as compared to the simulation results, we can still conclude that our proposed modified merged LNA & Mixer circuit actually works very well and exhibits much higher gain, higher linearity, better isolation, and wider dynamic range with acceptable low power consumption than the conventional cascade LNA & Mixer architecture in CMOS technology.

Chapter 5

New RF CMOS MICROMIXER Design and Implementation

5.1 Review of Basic MICROMIXER Architecture

Mixers have for decades played an indispensable role in communications systems as frequency-translation devices. System integrated monolithic mixers often use a topology called Gilbert mixer, especially in CMOS technology. However, its RF input stage, usually a simple differential pair or sometimes using source degeneration, sets fundamental limits to the attainable dynamic range. [1] The small-signal linearity of this input stage, and thus the third-order intercept point, can be greatly improved using several techniques, notably, source degeneration, the multi-tanh doublet and triplet [34]. However, the 1-dB gain compression point still falls short of what may be required in handling large input signals without significant intermodulation. Being the indispensable element of the receiver chain, the linearity and dynamic range of mixers play a significant role in the overall linearity and dynamic range of the receiver. Further, these RF stages do not provide an accurate match to the source, even when using various types of impedance-transformation methods. Accordingly, in this section we describe a basic topology, dubbed MICROMIXER for reference purposes [35-36]. Besides, before introducing our proposed modified topology called new RF CMOS MICROMIXER, it is helpful to review some design guidance and architecture of the basic MICROMIXER.

As shown in Fig.5.1.1, the basic MICROMIXER [8] in CMOS form adopts a quite different approach to improve dynamic range. It follows the general form of

Gilbert mixer, except for the use of a bisymmetric Class-AB RF stage. We can see that its mixer core is identical to that of standard Gilbert mixer. The only difference lies on the RF stage that is replaced by a bisymmetric Class-AB topology based on translinear principles. This provides well-defined matching impedance and much lower input related nonlinearity. Although it does not have inherent gain compression in RF stage, the 1-dB compression point of MICROMIXER will often be determined by limitations on the output IF signal amplitude, rather than by the RF stage. The lower reaches of the dynamic range are constrained by the input-referred wideband noise, usually expressed in terms of noise figure. Although the noise figure in MICROMIXER depends on design details and is generally not as low as in standard mixers specially optimized for noise performance, it is acceptable for many receiver applications.

In Fig. 5.1.1, Ma can be viewed as a gate-grounded stage. It delivers its output I_1 to the mixer pair M1-M2 in-phase. It can, in principle, handle unlimited amounts of current during large negative excursion of V_{GEN}. On the other hand, the current-mirror sub-cell Mb-Mc can handle essentially unlimited amounts of current during positive excursion of V_{GEN} both at its input node and at its inverted-phase current output I_3, which drives the mixer pair M3-M4. Acting together, these two sub-cells provide an overall transfer characteristic which is symmetric to both positive and negative inputs, and which is in principle not limited by the choice of bias level. The differential current output I_1-I_3 is linear with I_{RF}, although the individual currents are quite nonlinear. [8]

For simplifying, assume ideal transistors and neglecting parasitic effects, we can derive two simple expressions for low-frequency small-signal input resistance and voltage gain. The low frequency small-signal input resistance of RF input stage is approximately:

$$R_{IN} = \mathrm{Re}(Z_{in}) = \frac{1}{2g_m}$$

Unlike standard Gilbert Mixer, this characteristic of MICROMIXER RF input stage will facilitate the design of good RF input matching to 50Ω as long as we choose appropriate bias current. Assume perfect impedance matching to 50Ω, the low frequency small-signal voltage gain is approximately:

$$G_V \equiv \frac{V_{IF}}{V_{RF}} \approx \frac{1}{2} \cdot g_m \cdot \frac{2}{\pi} \cdot 2R_L = \frac{2}{\pi} \cdot g_m R_L \text{ ------ Eq. (1)}$$

In general, the topology of basic MICROMIXER performs very well in BTJ technology. However, in the next section, we will demonstrate that the conversion gain of basic MICORMIXER in CMOS technology is not high enough to meet our desired specification due to lower transconductance as compared to that in BJT technology. That may be the major reason why MICROMIXER in BJT form is generally studied and reported, but that in CMOS form is almost not investigated and presented up to now. Therefore, in the subsequent sections, we will propose and study a modified topology based on this basic MICROMIXER to eliminate this bottleneck in CMOS technology.

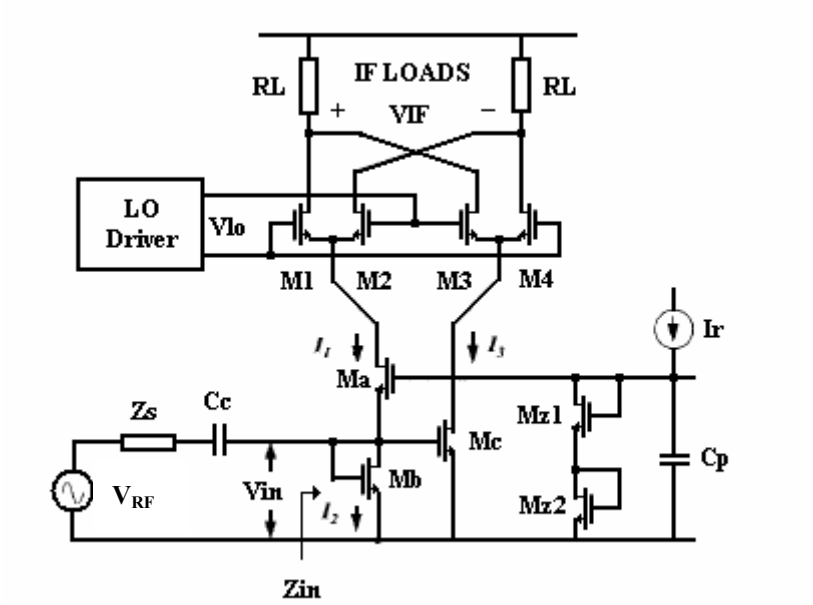


Fig. 5.1.1 Basic CMOS MICROMIXER

5.2 The Proposed New RF CMOS MICROMIXER

Radio frequency designs are increasingly taking advantage of technology advances in CMOS that make possible the integration of complete communication systems. However, due to poor performances of basic MICROMIXER in CMOS technology, the standard form of Gilbert mixer is still prefer to the topology of MICROMIXER, even though it has the advantage of easily matching and wide dynamic range. The design of CMOS MICROMIXER is always restricted by the trade-off of gain, noise figure, and power dissipation. To overcome this bottleneck, a modified architecture of CMOS MICROMIXER as shown in Fig. 5.2.1 is first proposed that is fully integrated and capable of operation at 2.45GHz band with higher gain, lower noise, higher linearity, and lower power dissipation than those of basic one. The simulation results compared between basic and proposed new architecture of CMOS MICROMIXER are shown in Table 5.3.1 and we can see these disadvantages (low gain, high noise figure and power dissipation) and design difficulties of basic MICROMIXER in CMOS technology obviously. Furthermore, we also have demonstrated these superior performances of new CMOS MICROMIXER. We will present the design and analysis of such a new MICROMIXER in advanced.

The modified architecture of new MICROMIXER is based on that of basic MICROMIXER. We still reserve the original topology of bisymmetric Class-AB RF drive stage because it not only can transform single-ended RF input to differential pair signals but also can obtain good impedance matching and wide dynamic range. This is quite an important characteristic and advantage in RF input stage of MICROMIXER. Neglecting large blocking capacitor (C_c), the input admittance of RF drive stage is approximately:

$$Y_{in} \approx 2g_m + j\omega(3C_{gs})$$

The real part of input impedance in this circuit is still about $1/2g_m$. We can choose appropriate size of transistors (M1, M2, and M3) to make it close to 50Ω. If we use the inductors series in input node to achieve matching, it will break this advantage of 50Ω input resistance and will be hard to achieve good matching. So we take advantage of a serial LC tank (L_{rf} & C_{rf}) in parallel with input node to resonate and eliminate the image part of input impedance. Thus the input admittance of RF drive stage is:

$$Y_{in} \approx 2g_m + j\omega(3C_{gs}) - j\frac{1}{\omega L_{rf} - \frac{1}{\omega C_{rf}}} \approx 2g_m$$

This method will achieve good input impedance matching very easily.

In addition, two pairs of parallel LC tanks (L1, C1 & L3, C3) are added to resonate at desired frequency (2.45GHz) to provide high impedance looking into the mixer core (M4p, M4n & M5p, M5n). The differential currents generated by RF input stage (M1-M3) are obstructed and unable to directly couple into the mixer core and then converted to high differential voltages. These high voltages are then separately fed into a pair of bleeding-current NMOS transistors (Mb1 & Mb2) via a pair of large bypass capacitors (Cc1 & Cc2). This pair of transistors is added to simultaneously act as not only bleeding-current sources to improve linearity, gain, and noise figure [29-30] but common-drain source followers which constitute a mechanism of high frequency current amplifiers to achieve higher gain. This method is similar to that of bias-current reuse technique widely used recently. [7][30] It can achieve much higher gain without large amount of power consumption. As derived in previous section, assume perfect impedance matching to 50Ω is done, the low frequency small-signal voltage gain is then approximately:

$$G_V \equiv \frac{V_{IF}}{V_{RF}} \approx \frac{1}{2} \cdot g_{m1} \cdot \left\| 1 + \frac{g_{mb1}}{SC_{gsb1}} \right\| \cdot \frac{2}{\pi} \cdot 2R_L = \frac{2}{\pi} \cdot g_{m1} R_L \cdot \left\| 1 + \frac{g_{mb1}}{SC_{gsb1}} \right\|$$

For convenient in our circuit design, we have chosen the transistor size of Mb1 and Mb2 to make that:

$$\left\| 1 + \frac{g_{mb1}}{SC_{gsb1}} \right\| \approx g_{m1} R_L$$

hold and thus voltage gain is approximately:

$$G_V \equiv \frac{V_{IF}}{V_{RF}} \approx \frac{2}{\pi} \cdot g_{m1} R_L \cdot \left\| 1 + \frac{g_{mb1}}{SC_{gsb1}} \right\| \approx \frac{2}{\pi} \cdot g_{m1}^2 R_L^2 \text{ ------ Eq. (2)}$$

To compare Eq. (2) with Eq. (1), we can see that the voltage gain of new proposed MICROMIXER is proportional to square of the transconductance (g_m^2) and it can achieve much higher gain, one of the major purposes of our modification, than that of basic one, that is only proportional to single transconductance (g_m).

As explained in Section 4.3, a floating inductor (L_{pn}) is added to resonate with parasitic capacitances at the tails of the mixer core and to lower the effect of mixer flicker noise. [6] Besides, capacitors (Cp & Cn) and resistive loads (Rp & Rn) across the mixer output act as low-pass filters to filter out the undesired signals and feedthrough at the LO frequency. In this circuit design, we choose low-IF frequency as 10MHz. So we have set the filter capacitors as 6.4 pF and the resistors as 800Ω. Such setups will result in a cutoff frequency of 31MHz as desired. For measurement purpose, we connect an on-chip common-drain output buffer as shown in Fig.5.2.2 to simultaneously achieve IF port output matching to 50ohm and increase output driving capability. Finally, we take advantage of π-matching circuits and coupling capacitors as shown in Fig. 5.2.3 to achieve good LO input matching to 50Ω and be able to provide the mixer enough LO power from outside signal generator. In the subsequent sections, we will demonstrate that this proposed modified circuit topology could meet our design ideas through SPICE post simulation and measurement results.

Specification	Basic MICROMIXER	New MICROMIXER
RF Port Input RL (dB)	11.7	23.5
LO Port Input RL (dB)	12.9	19.3
Voltage Gain (dB)	-1.5	10.4
Noise Figure (dB)	20.1	11.4
P1dB (dBm)	-11.5	-10.1
IIP3 (dBm)	-1.5	-0.7
Power Consumption (mW)	15.0	3.7

Table 5.2.1 Simulation Comparison Between Basic and New MICROMIXER

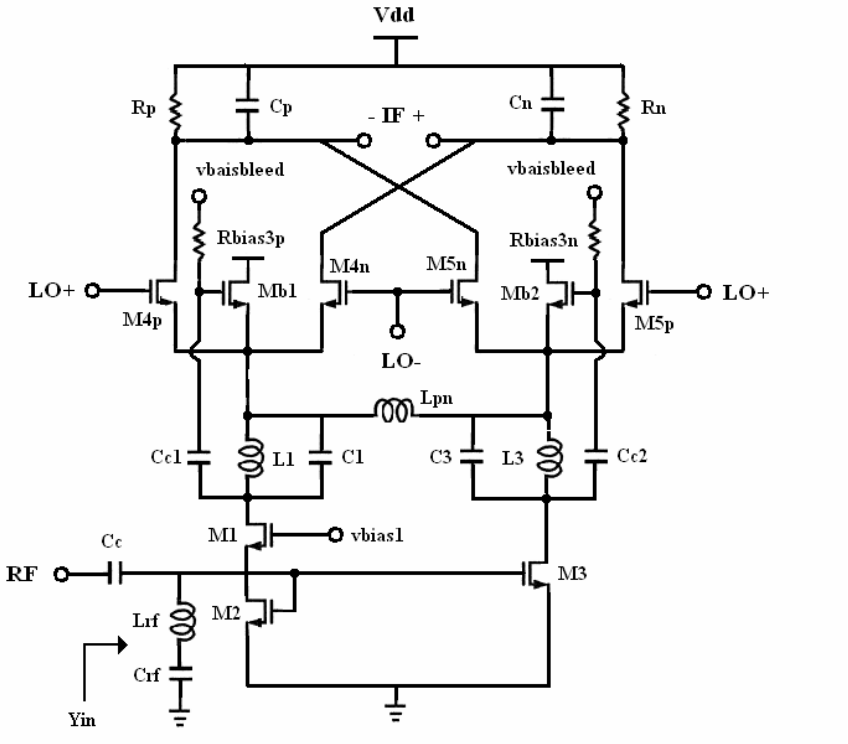


Fig. 5.2.1 New RF CMOS MICROMIXER

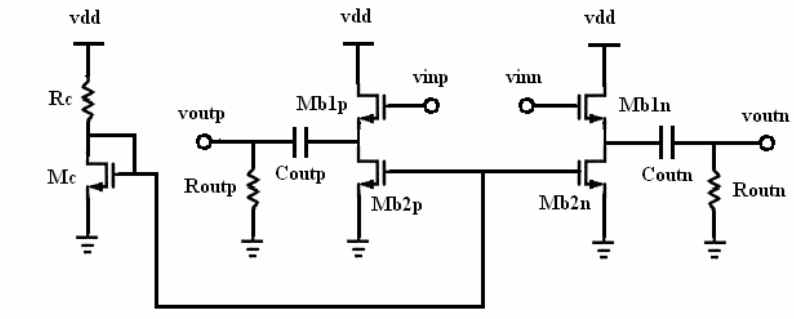


Fig. 5.2.2 Common-Drain Output Buffer

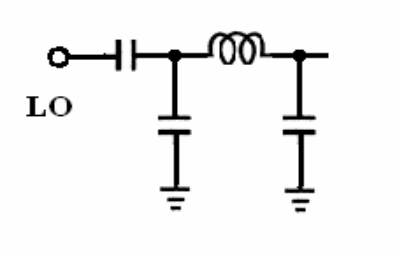


Fig. 5.2.3 π-matching circuit and coupling capacitor

5.3 Simulation and Measurement of New CMOS MICROMIXER

5.3.1 Layout and Simulation Results

A new RF CMOS MICROMIXER by previous architecture is designed and optimized using 0.25 μm CMOS technology. The final layout of it is shown in Fig. 5.3.1. All elements are fully integrated on a chip including spiral inductors, MIM capacitors, multi-finger RF NMOS transistors, poly resistors, and decouple MOS capacitors. The total chip size including the pads is about 1150umx1400um. It has been fabricated using TSMC 0.25 μm mixed-signal CMOS process. Similarly, we also take advantage of shielded signal PAD as described in Section 3.4.1 to reduce coupling noise from the noisy Silicon substrate. We will show its final simulation and measurement performances latter.

The RF and LO signal frequencies are designed at 2.45GHz and 2.44GHz, respectively. The fact that LO frequency is lower than the center of desired band is called “low-side injection“. To minimize LO frequency will facilitate the design of oscillator. The output mixing IF signal thus falls at 10MHz. Because this work is designed for PCB on-board testing, the parasitic effects of bond-wires and bond-pads will greatly influence the impedance matching of all ports. For all outside 50Ω instruments, only input power of generators can be delivered into the chip or output power of the circuit can be received by measurement instruments more efficiently

with good input or output impedance matching. Therefore, these parasitic effects must be included and considered throughout all simulation procedure very carefully.

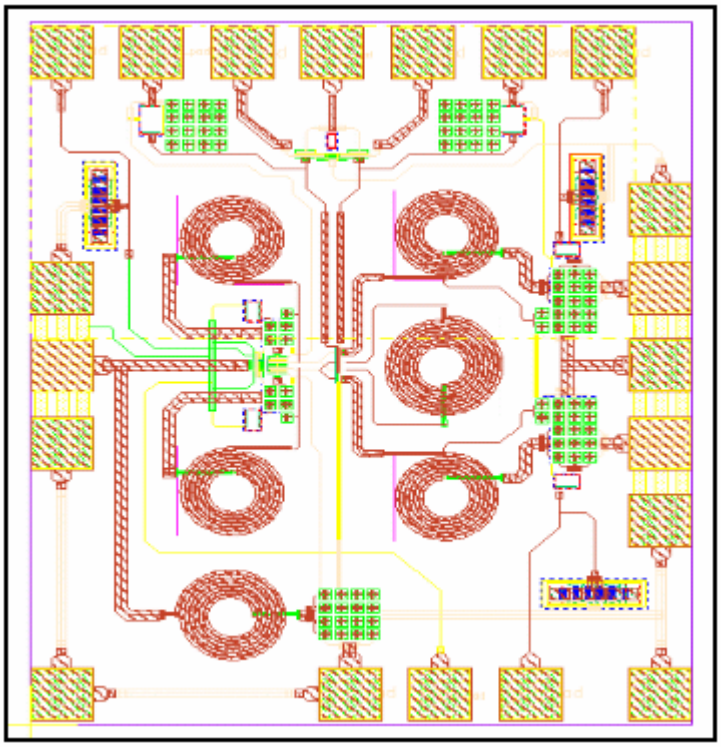


Fig. 5.3.1 Layout of Proposed New MICROMIXER

The SPICE post simulation performances including all parasitic effects are shown in Fig. 5.3.2-9. Fig. 5.3.2 shows RF port input matching to 50ohm with input return loss of 17.5dB at 2.45GHz and Fig. 5.3.3 shows LO port input matching to 50ohm with input return loss of 14.1dB at 2.44Hz, while LO input power is –11dBm and RF input power is –35dBm. Fig. 5.3.4 shows voltage gain vs. RF input power swept from -50dBm to 0dBm with -11dBm LO input power and 1MΩ load. It exhibits high voltage gain of 11.0dB and V_{1dB} of –10.0dBm. Fig. 5.3.5 shows voltage gain vs. LO input power swept from -30dBm to 0dBm with -35dBm RF input power and 1MΩ load. We can see that the maximum voltage gain is obtained while LO input power is –11dBm. Fig. 5.3.6 shows power gain vs. RF input power swept from -50dBm to 0dBm with -11dBm LO input power and 50Ω load. It exhibits power gain

of 1.6dB and P_{1dB} of -20.0dBm. Fig. 5.3.7 shows power gain vs. LO input power sweep from -20dBm to 0dBm with -35dBm RF input power and 50Ω load. The maximum power gain is also obtained while input LO power is close to –11dBm. Fig. 5.3.8 presents its NF performance of 11.6dB. Finally, Fig. 5.3.9 shows two-tone test IIP_3 simulation result of +1.1dBm and it exhibits quite good linearity of this circuit. Besides, above results will also lead to quite a wide dynamic range. The simulation performances including corner affections are summarized in Table 5.3.1.

The proposed new MIXROMIXER not only dissipates very low power of 3.7mW (not including power dissipation of output buffer, 4.7mW) from a 2.5V power supply voltage but also provides very good performance. According to above results, we can conclude that the proposed modified circuit actually exhibits much higher gain, lower noise, higher linearity, wider dynamic range, and lower power consumption than the conventional basic one in CMOS technology.

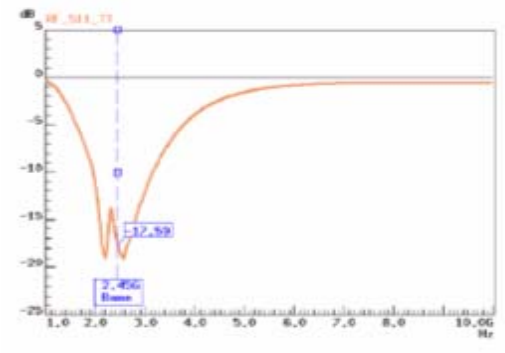


Fig. 5.3.2 RF Port Input Matching

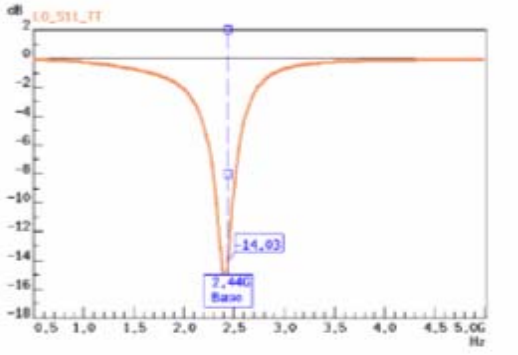


Fig. 5.3.3 LO Port Input Matching

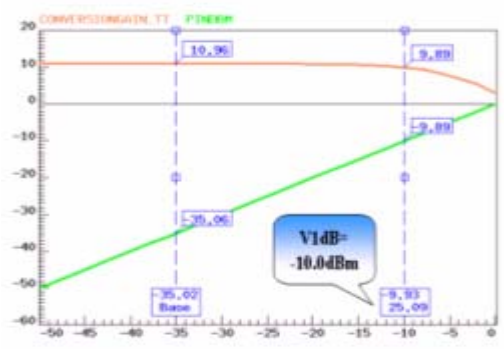


Fig. 5.3.4 Voltage Gain vs. RF Power

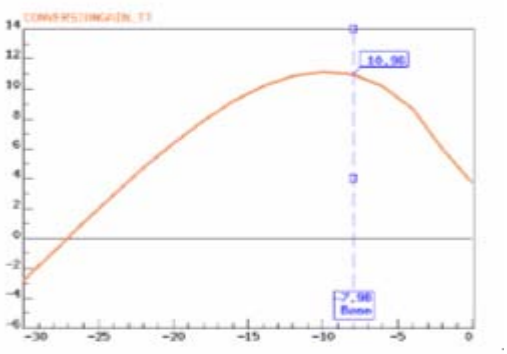


Fig. 5.3.5 Voltage Gain vs. LO Power

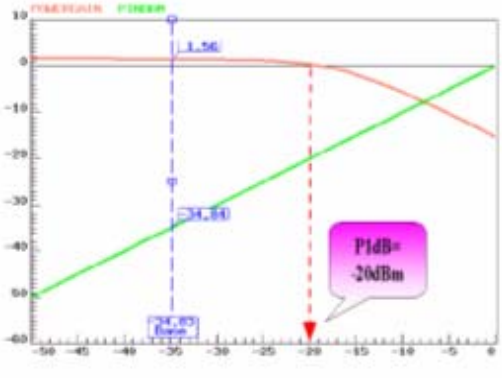


Fig. 5.3.6 Power Gain vs. RF Power

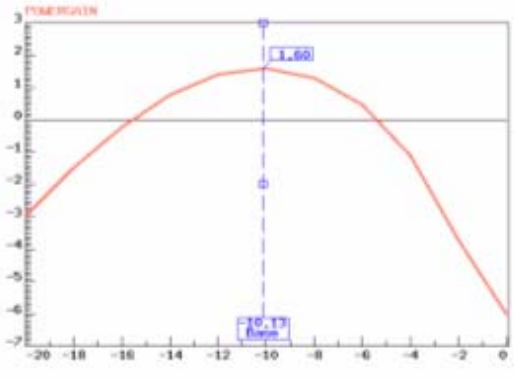


Fig. 5.3.7 Power Gain vs. LO Power

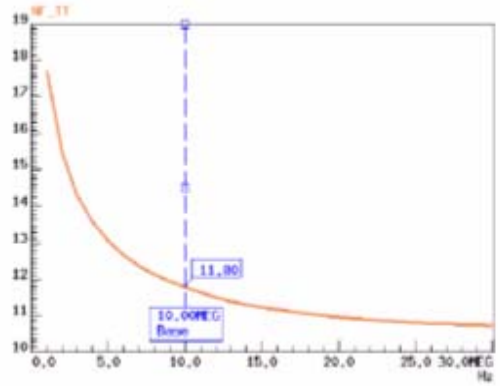


Fig. 5.3.8 Noise Figure

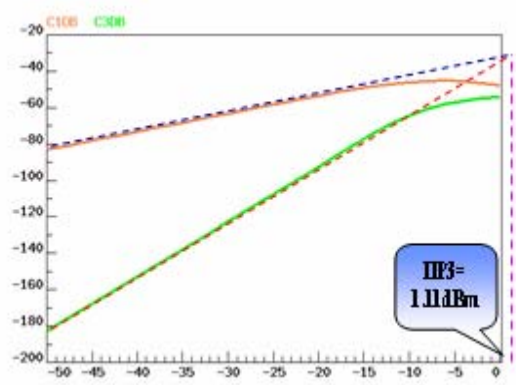


Fig. 5.3.9 Two-tone Intermodulation

Specification	TT	FF	SS
RF Input RL (dB)	17.5	16.1	17.5
LO Input RL (dB)	14.1	14.6	13.0
IF Output RL (dB)	11.6	12.9	10.5
Power Gain (dB)	1.6	5.4	-1.7
Voltage Gain (dB)	11.0	14.1	8.1
NF (dB)	11.8	10.6	13.0
P1dB (dBm)	-20.0	-24.0	-17.5
V1dB (dBm)	-10.0	-13.4	-7.1
IIP3 (dBm)	+1.1	-3.7	+5.7
LO-to-RF Isolation (dB)	> 50	>50	>50
Power Consumption (mW)	Buffer: 4.7 Core: 3.7 Total: 8.4	Buffer: 5.0 Core: 4.4 Total: 9.4	Buffer: 4.4 Core: 3.3 Total: 7.7

Table 5.3.1 Post Simulation Performance Summary

5.3.2 Measurement Consideration

The simplified block diagram of the PCB on-board testing for our design is illustrated in Fig. 5.3.10. Because of differential LO input structure, one extra Balun is required to transform differential pair into single-ended port for common single-ended measurement systems. Here, we take advantage of one rat-race (180^0 ring hybrid) as shown in Fig. 5.3.11 to act as such a Balun. The ideal S-parameter of rat-race is shown as follows:

$$\begin{bmatrix} 0 & 0.707 & 0.707 & 0 \\ 0.707 & 0 & 0 & 0.707 \\ 0.707 & 0 & 0 & -0.707 \\ 0 & 0.707 & -0.707 & 0 \end{bmatrix}$$

It can split the input power from port 4 into output port 2 and port 3 with equal half power and 180^0-phase difference. However, the real S-parameter of rat-race we have designed and implemented is as follows:

$$\begin{bmatrix} 0.170\angle 78.1° & 0.661\angle 74.7° & 0.661\angle 73.5° & 0.017\angle 32.8° \\ 0.676\angle 72.2° & 0.180\angle -113.8° & 0.002\angle 7.2° & 0.684\angle -109.1° \\ 0.684\angle 70.8° & 0.002\angle 5.3° & 0.170\angle -108.7° & 0.684\angle 69.6° \\ 0.017\angle 30.7° & 0.661\angle -106.2° & 0.661\angle 72.2° & 0.170\angle 71.3° \end{bmatrix}$$

Although this experimental result still has little error, it is very close to that of ideal case and satisfied for our requirement.

PCB layout and practical FR4 PCB circuit conjunction with SMA connectors for this work are shown in Fig. 5.3.12 and Fig. 5.3.13, respectively. One important thing must be taken care in the design of PCB layout, the width of RF and LO signal paths must be drawn as 50Ω-line width for impedance matching. This chip is adhered to PCB first and all I/O pads on this chip are then bonded to PCB via bond-wires. The die photograph of this chip including bond wires is shown in Fig. 5.3.14. Throughout all measurement procedures, we still require extra three signal generators, one spectrum analyzer, one network analyzer, one oscilloscope and other auxiliary devices,

such as cables, 50Ω terminals ,and power combiners. Since we have finished the prior preparations for PCB on-board testing, the measurements can now be proceeding according to arrangements in Fig.5.3.10. It should be noted that the losses of cable, Balun, Combiner, SMA connectors, and PCB board itself must be taken account for calibration and measurements.

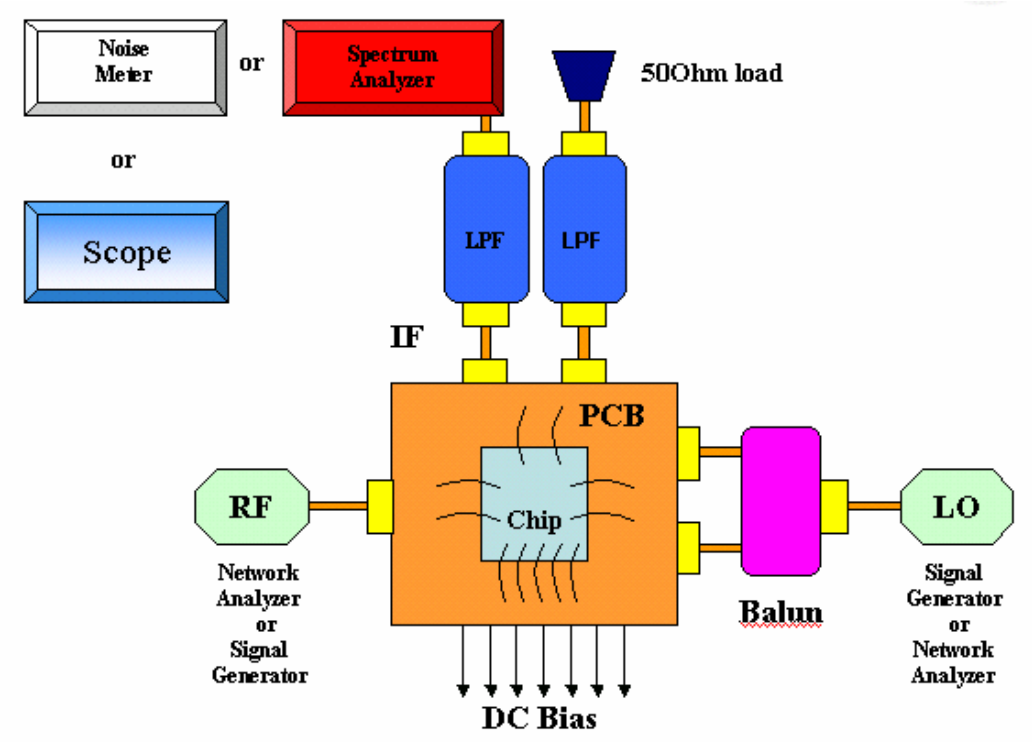


Fig. 5.3.10 Simplified Block Diagram of PCB on-board Testing

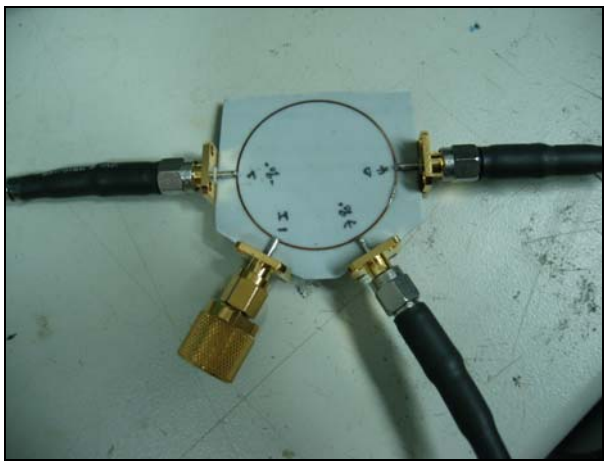


Fig. 5.3.11 The Photograph of LO Port Rat-race

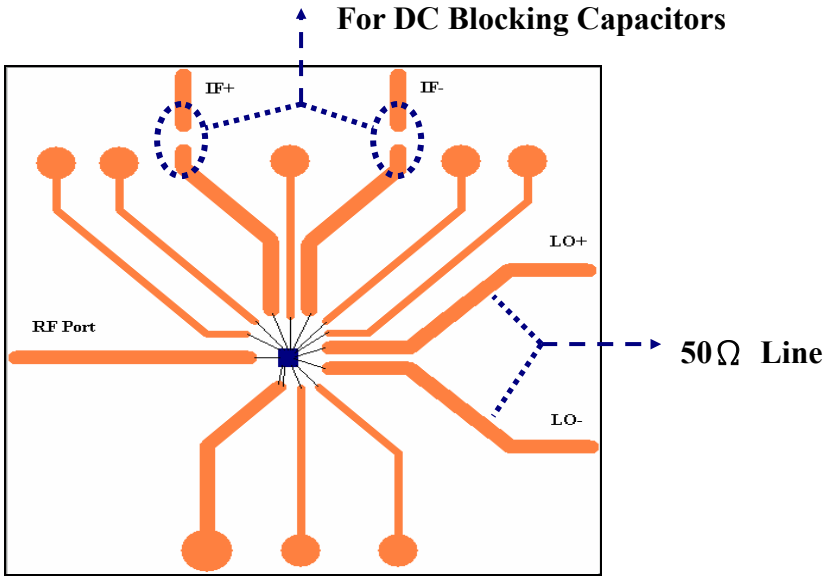


Fig. 5.3.12 PCB Layout

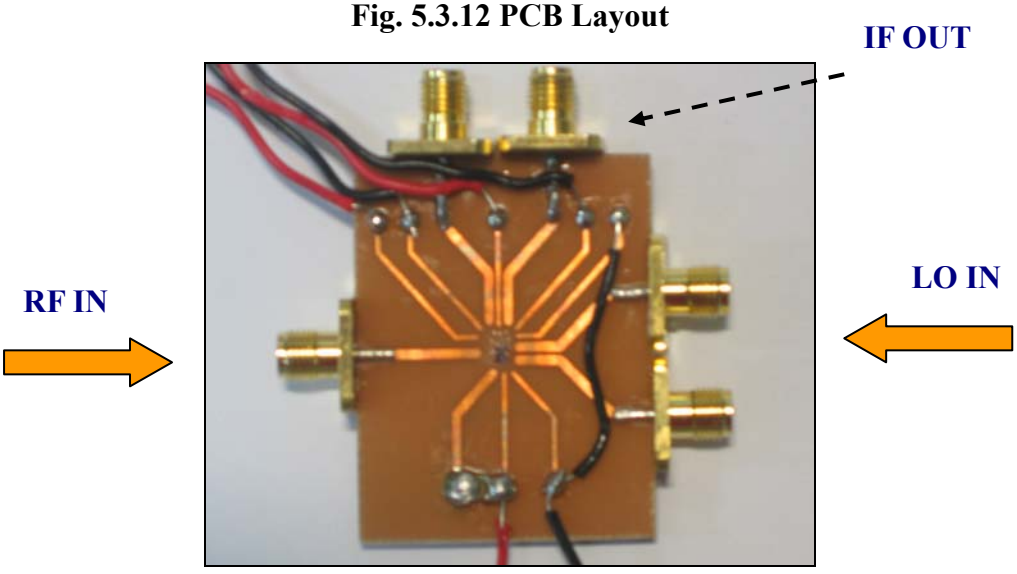


Fig. 5.3.13 Photograph of Practical FR4 PCB circuit

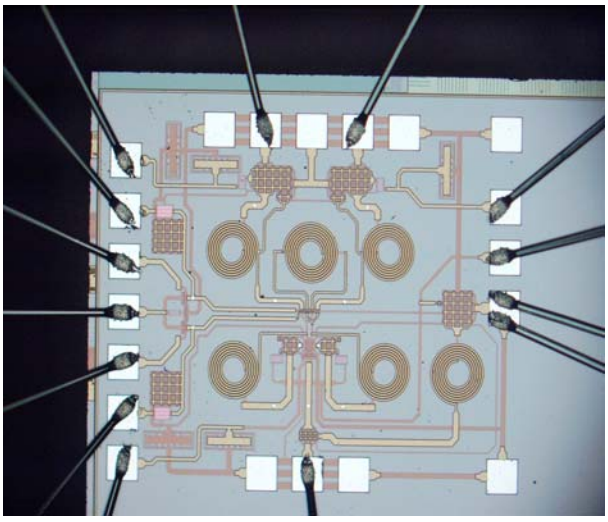
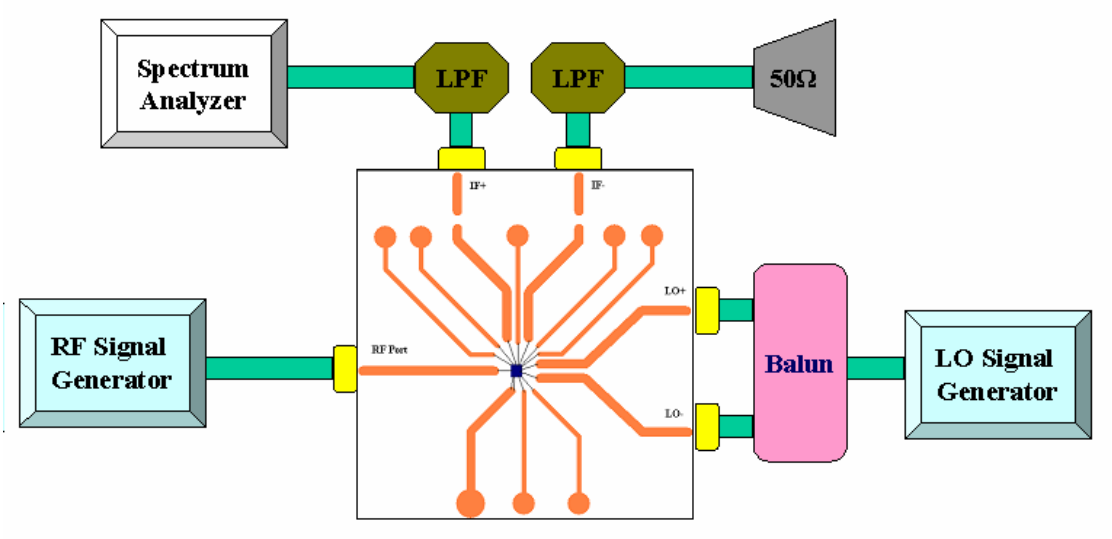
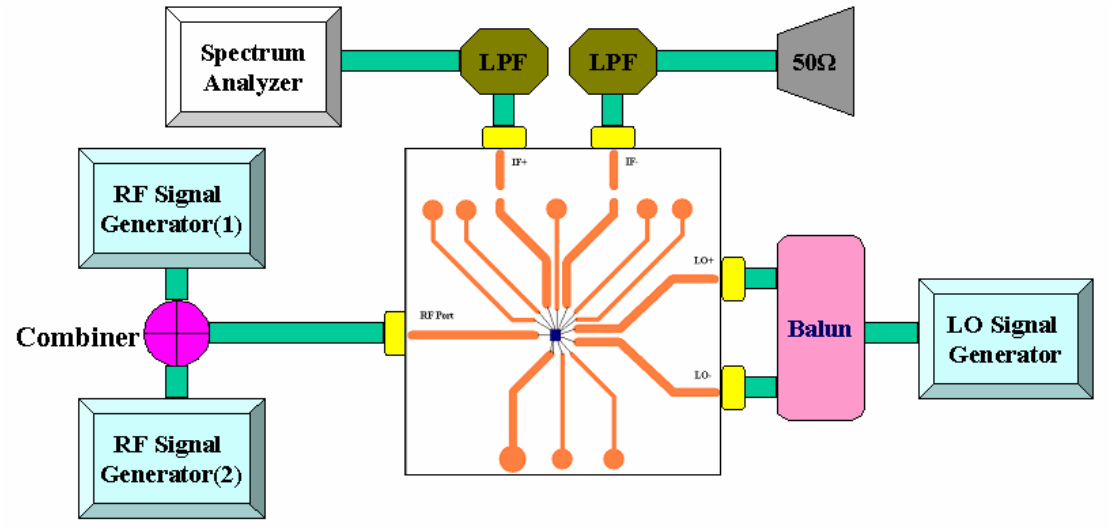


Fig. 5.3.14 Die Photograph of New CMOS MICROMIXER

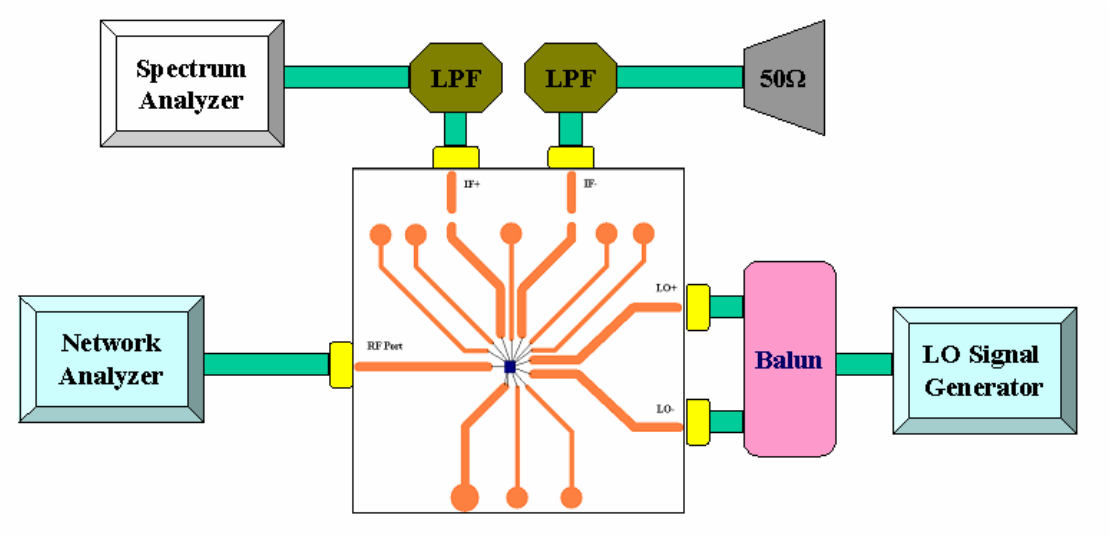
There are some RF parameters that we have to measure in our design of new RF CMOS MICROMIXER. These parameters include RF & LO input return loss, conversion gain, P_{1dB}, and two-tone linearity test of IIP_3. We have used RFIC measurement systems in CIC and our laboratory to finish these parameter measurements. The simplified block diagrams of each measurement setup for each parameter are illustrated in Fig. 5.3.15. In addition, an extra voltage-division circuit as described in Section 4.4.2 is also used to provide the desired stable dc bias voltages for these measurements.



(a)



(b)



(c)

Fig. 5.3.15 Simplified Block Diagram of Each Measurement Setup for (a) Conversion Gain (b) Two-tone IIP3 Test (c) Input Return Loss

5.3.3 Measurement Results

Upon previous measurement considerations and arrangements, we have made all PCB on-board tests for our design in CIC and our Laboratory. In 50Ω measurement system, Fig. 5.3.16 shows the measured RF port input matching and Fig. 5.3.17 shows the measured LO port input matching from 0.5GHz to 5GHz. It exhibits both good RF port input return loss (RL) of 15.4dB at 2.45GHz and good LO port input RL of 16.1dB at 2.44GHz. The measurement and FF-corner simulation results of power gain versus LO input power swept from -20dBm to 0dBm are compared and shown in Fig. 5.3.18, where RF input power is fixed with –35dBm. We can see that the maximum measured power gain of 6.8dB can be obtained while LO input power is -11dBm. The measurement and FF-corner simulation results of power gain vs. RF input power swept from -40dBm to -8dBm are compared and shown in Fig. 5.3.19 where LO input power is fixed with -11dBm both in measurement and FF-corner simulation. It exhibits high measured power gain of 6.8dB and P_{1dB} of -15dBm. Fig. 5.3.20 shows

the measurement result of two-tone test IIP_3 that is -1.0dBm. It also exhibits much high linearity and wide dynamic range. Finally, IF output waveform is also measured by oscilloscope (1MΩ equivalent load), instead of spectrum analyzer (50Ω equivalent load). Fig. 5.3.21 shows that the measured peak-to-peak voltage of IF output waveform is about 60.6mV while RF and LO input power is –35dBm and –11dBm, respectively. Through simple mathematics transformation, this circuit actually performs quite high voltage gain of 14.6dB. All simulation and measurement performances are summarized in Table 5.3.2.

This proposed new RF CMOS MICROMIXER dissipates total power of 10.5mW, including 5.5mW in mixer core and 5.0mW in output buffer, from a 2.5V power supply voltage. Power dissipation of measurement is more than that of TT-corner simulation result in the part of core circuit but close to that of FF-corner simulation. However, power dissipation of measurement almost coincides with that of simulation result in the part of output buffer. This means that the process condition is now falling at the vicinity of FF-corner. Since the process condition is falling at the vicinity of FF-corner, Table 5.3.2 also contains the simulation results of FF-corner and we will make any comparison and discussion based on above measurements and FF-corner simulations in next section.

5.3.4 Comparison and Discussion

According to performance comparison result shown in Fig. 5.3.19, we can see that power gain of measurement is 1.4dB better than that of FF-corner simulation. This is, in fact, because of more current drawing in mixer core circuit as compared to FF-corner simulation. As derived in Section 5.2, we know that IF port output voltage is proportional to square of the transconductance of NMOS transistors in the RF input drive stage of MICROMIXER core. Besides, in the same 50Ω input source resistor

and output load, power gain is also equal to square of voltage gain. An approximation is derived to explain above result as follows:

(1) $g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_D}$ and

$$V_{out} \propto g_m{}^2 \propto \mu_n C_{ox} I_D$$

(2) With the same RF input power, we know that:

$$\Delta P_{out}(dB) = P_{measured}(dB) - P_{FF-corner}(dB) = 20\log\left(\frac{V_{measured}}{V_{FF-corner}}\right)$$

(3) According to (1), we can obtain that:

$$\frac{V_{measured}}{V_{FF-corner}} = \frac{g_{m\_measured}{}^2}{g_{m\_FF-corner}{}^2} = \frac{(\mu_n C_{ox})_{measured}}{(\mu_n C_{ox})_{FF-corner}} \cdot \frac{I_{D\_measured}}{I_{D\_FF-corner}}$$

(4) To simplify, since process condition is at vicinity of FF-corner and we just estimate it approximately, so that we assume the variation ratio of process parameters is close to unity. Thus,

$\frac{(\mu_n C_{ox})_{measured}}{(\mu_n C_{ox})_{FF-corner}} \approx 1$ and then:

$$\frac{V_{measured}}{V_{FF-corner}} \approx \frac{I_{D\_measured}}{I_{D\_FF-corner}} = \frac{P_{DC\_measured}}{P_{DC\_FF-corner}}$$

(5) Finally, the deviation of power gain in dB unit is obtained as follows:

$$\Delta G_P = \Delta P_{out} \approx 20\log\left(\frac{P_{DC\_measured}}{P_{DC\_FF-corner}}\right) = 1.9dB$$

Above final result is very close to experimental deviation of power gain, 1.4dB. In fact, process parameters variation ratio is a little more than unity. However, above approximation is actually a very useful estimation and explanation and it has

demonstrated the root cause of this incremental power gain reasonably and obviously. In addition, the P_{1dB} value of measurement is much better than that of FF-corner simulation. Although the simulator underestimated the performance of dynamic range for our proposed new RF CMOS MICROMIXER, this result actually has demonstrated the good characteristic of wide dynamic range in a bisymmetric Class-AB RF stage topology.

From comparison results in Table 5.3.2, we can see that its good linearity performance of measured IIP_3 is close to that of simulation result. However, although LO-to-RF isolation is much lower than the overestimated simulation result, it works very well and meets the requirements for practical circuit application. Besides, from Fig. 5.3.18, we can also find that the measured maximum power gain occurs at almost the same LO input power as simulation result. It also has demonstrated that the modified new MICROMIXER we proposed is indeed required only very low LO input power to drive the commutating pairs. Furthermore, it will facilitate the design of on-chip oscillator for the integration in the future.

In summary, although process condition is deviated from TT-corner and it causes a little more power consumption than what we expected, all of measurement performances are almost coincided with those of FF-corner simulation, even better. In other words, we actually reach the major purposes of our modification in original MICROMIXER architecture, to achieve high gain with acceptable low power and still maintain good linearity. Finally, we can conclude that our proposed modified new RF CMOS MICROMIXER actually works very well and exhibits much higher gain, higher linearity, better isolation, and wider dynamic range with acceptable low power consumption than the conventional basic MICROMIXER architecture in CMOS technology.

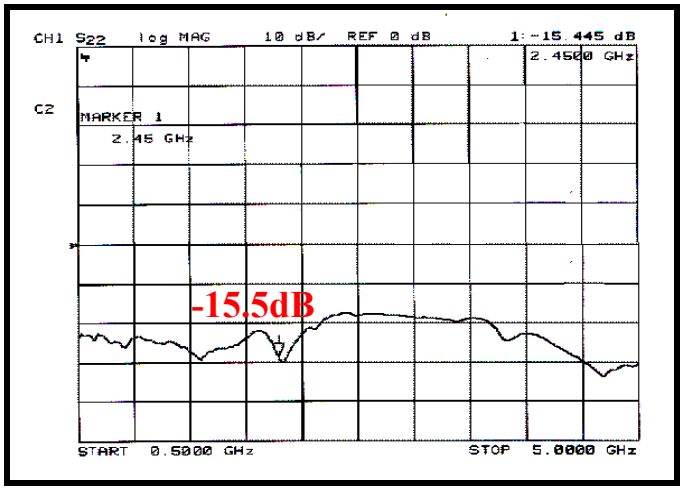


Fig. 5.3.16 Measured RF Port Input Matching

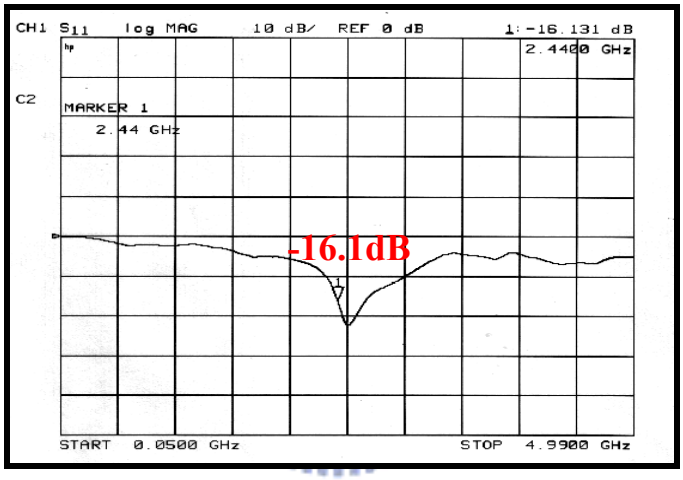


Fig. 5.3.17 Measured LO Port Input Matching

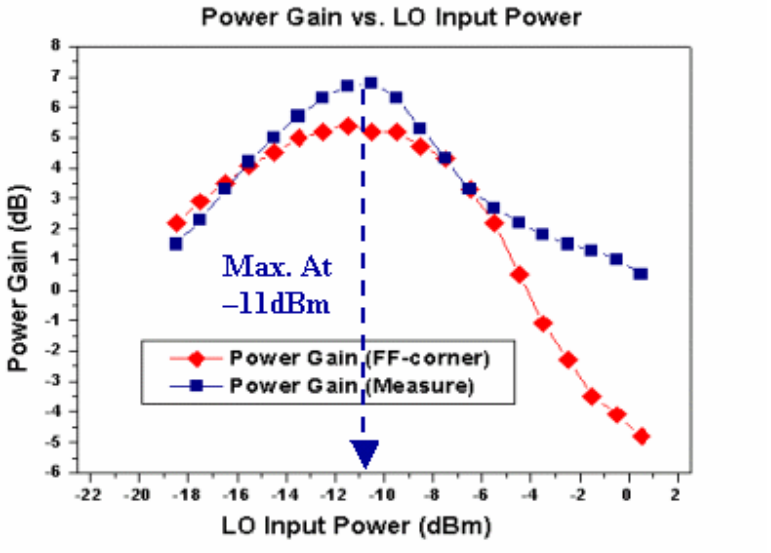


Fig. 5.3.18 Power Gain vs. LO Input Power Comparison

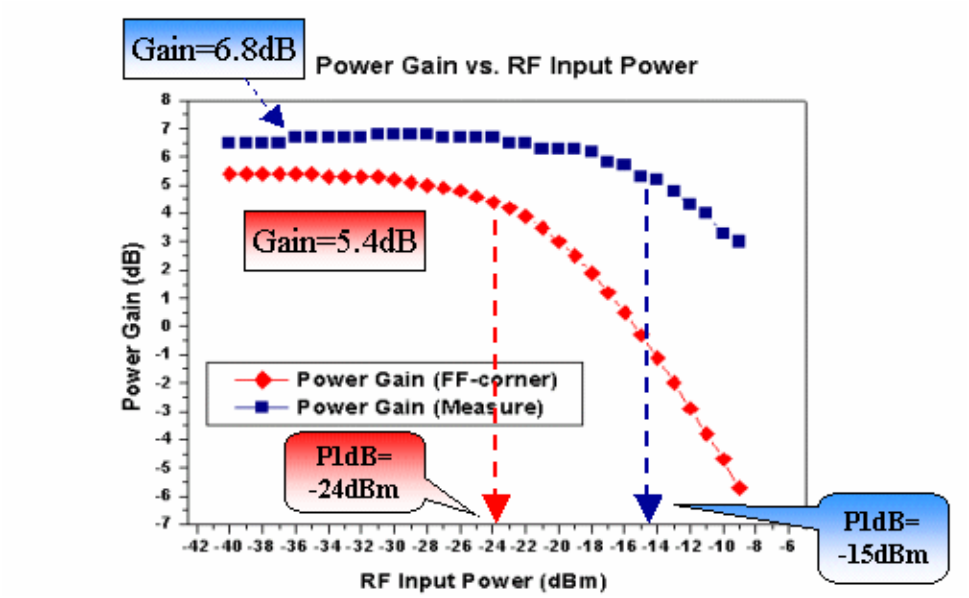


Fig. 5.3.19 Power Gain vs. RF Input Power Comparison

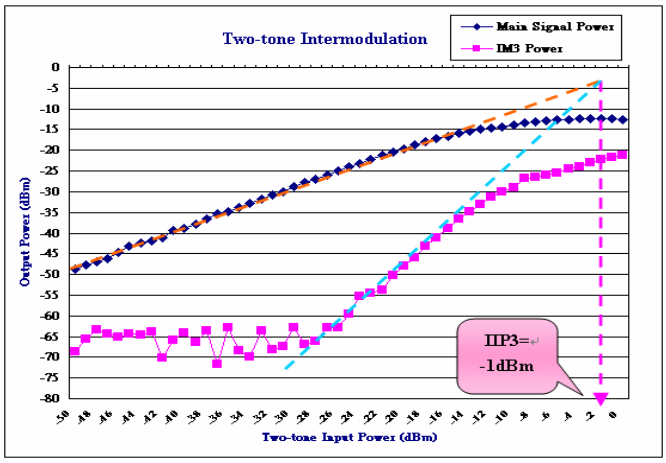


Fig. 5.3.20 Two-tone Test Measurement Result

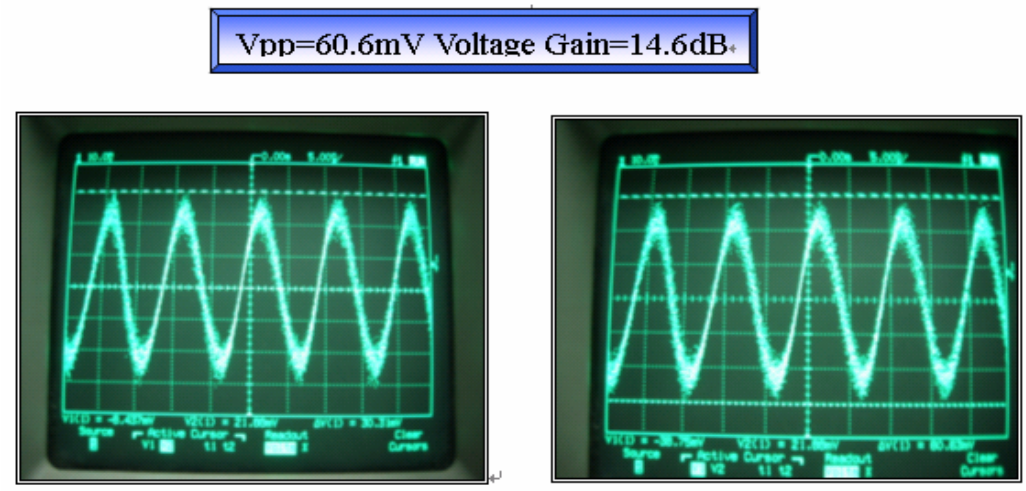


Fig. 5.3.21 IF Output Waveform Measured by Oscilloscope

Specification	Simulation (TT)	Simulation (FF)	Measurement
RF Input RL (dB)	17.5	16.1	15.4
LO Input RL (dB)	14.1	14.6	16.1
IF Output RL (dB)	11.6	12.9	NA
Power Gain (dB)	1.6	5.4	6.8
Voltage Gain (dB)	11.0	14.1	14.6
NF (dB)	11.8	10.6	NA
P1dB (dBm)	-10	-13.4	-15
IIP3 (dBm)	+1.1	-3.7	-1.0
LO-to-RF Isolation (dB)	> 50	> 50	32
Power Consumption (mW)	Buffer: 4.7 (1.9mA) Core: 3.7 (1.5mA) Total: 8.4 (3.4mA)	Buffer: 5.0 (2.0mA) Core: 4.4 (1.8mA) Total: 9.4 (3.8mA)	Buffer: 5.0 (2.0mA) Core: 5.5 (2.2mA) Total: 10.5 (4.2mA)

Table 5.3.2 Simulation and Measurement Performance Summary

Chapter 6

Conclusion and Future Work

6.1 Conclusion

This thesis contents three works. The first work is a novel fully integrated concurrent triple-band CMOS LNA for 1.8GHz, 2.45GHz, and 5.25GHz. The second work is a modified CMOS double-balance mixer merged LNA for WCDMA. The last work is a new RF CMOS MICROMIXER for 2.45GHz. All of the simulation performances were finished through Eldo-RF simulator. These three ICs all have been fabricated using TSMC 0.25-μm CMOS process through CIC. In this thesis, we have presented the design concepts, simulation results, experimental results, and advanced comparisons & discussions for these three works.

6.1.1 Concurrent Triple-Band CMOS LNA

A novel fully integrated concurrent triple-band CMOS LNA has been designed and presented in this thesis. All measurements were finished through on-wafer testing at NDL. The measured input matching for lower dual frequency bands (1.8GHz and 2.45GHz) is nearly falling at desired frequencies and achieves better matching than simulation. But the input matching for higher frequency band (5.25GHz) is shifted to lower frequency at 4.5GHz. The major reason is that the parasitic inductances are not considered and included in our design procedure. The measured output matching is nearly broadband matching but still has the trend of concurrent triple-band matching. This is because the original additive feedback capacitors are chosen too small to control exactly and have great deviations after fabrications. Besides, the power gain and noise figure performances do not meet our anticipation in this architecture. Three

major factors also have been explained in Section 3.5.4. However, this LNA design can achieve better dynamic range and linearity of P_{1dB} and IIP_3 parameters in measurement than those in simulation.

In fact, the models of the spiral inductors applied at higher frequency (5.25GHz) are not as accurate as those applied at lower frequency. So that they will also cause mismatches between simulation and measurement results. In summary, to design a concurrent multi-band LNA or even other RF circuits with better performances, not only the parasitic effects have to be considered more carefully but the more accurate models designed and optimized for all desired frequencies must be involved, especially for complicated and large chip area circuits at higher frequency.

Although the measured performances in S-parameters and noise figure are not as good as that in simulation results, we actually have demonstrated our novel circuit design concepts of the concurrent triple-band LNA that is first proposed.

6.1.2 CMOS Double-Balanced Mixer Merged LNA

A modified CMOS double-balanced merged LNA has been design and presented in this thesis. All measurements were finished through PCB on-board testing at CIC and our laboratory. The process condition has been shifted between TT and SF-corner. The power gain of measurement is about 1.5dB lower than that of TT-corner simulation. And the maximum measured power gain occurs at higher LO input power than TT-corner simulation result. Besides, the linearity performance of the two-tone test IIP_3 is very close to the simulation result and the measured P_{1dB} is better than the TT-corner simulated one. All factors to cause these measurement results have been explained in Section 4.4.4. Finally, although LO-to-RF isolation is much lower than the overestimated simulation result, it works very well and meets the requirements for practical circuit application.

In summary, although some performances are a little degraded as compared to the simulation results, our proposed modified merged LNA & Mixer circuit actually works very well and exhibits much higher gain, higher linearity, better isolation, and wider dynamic range with acceptable low power consumption than the conventional cascade LNA & Mixer architecture in CMOS technology.

6.1.3 New RF CMOS MICROMIXER

A modified New RF CMOS MICROMIXER has been designed and presented in this thesis. All measurements were also finished through PCB on-board testing at CIC and our laboratory. The process condition has been moved toward FF-corner. The power gain of measurement is about 1.4dB better than that of FF-corner simulation. This is because of more current drawing in mixer core circuit as compared to FF-corner simulation. The root cause of this incremental power gain has been demonstrated and explained through a very useful approximate estimation. In addition, the P_{1dB} value of measurement is much better than that of FF-corner simulation. This result actually has demonstrated the good characteristic of wide dynamic range in a bisymmetric Class-AB RF stage topology.

Besides, the circuit performs good linearity of high measured IIP_3 that is close to that of simulation result. However, although LO-to-RF isolation is much lower than the overestimated simulation result, it works very well and meets the requirements for practical circuit application. We can also find that the measured maximum power gain occurs at almost the same low LO input power as simulation result. It will facilitate the design of on-chip oscillator for the integration in the future.

In summary, although process condition is deviated from TT-corner and it causes a little more power consumption than what we expected, we actually reach the major

purposes of our modification in original MICROMIXER architecture, to achieve high gain with acceptable low power and still maintain good linearity. Finally, we have demonstrated that our proposed modified new RF CMOS MICROMIXER actually works very well and exhibits much higher gain, higher linearity, better isolation, and wider dynamic range with acceptable low power consumption than the conventional basic MICROMIXER architecture in CMOS technology.

6.2 Future Work

Some future works are made up as follows:

1. For higher frequency applications, more accurate RF CMOS models must be built up in advanced, especially spiral inductor models for exact matching.
2. All parasitic effects, not only parasitic capacitance but also parasitic resistance and inductance, must be considered and included more carefully, especially for complicated and large chip area circuits at higher frequency. A more accurate procedure or EDA tool for extracting these parasitic effects is greatly urgency.
3. Because lack of mature noise measurement system and accurate calibration procedure, the noise performances of mixers have not been done in this thesis. Therefore, to set up an accurate noise measurement system with correct calibration procedure for mixers will be also a greatly urgent work.
4. Since all circuits we have designed in this thesis can be integrated with other blocks on a single chip, on-chip bias networks and on-chip gain control mechanisms have to be designed and integrated for future SOC implementations.
5. As rapidly growth in CMOS technology with thinner gate oxide, ESD (Electrostatic discharge) protection circuits must be designed and involved in the RF IC.
6. The SPICE circuit simulator conjunction with 3-D simulator will make more precise predictions of circuit performances for future SOC total solutions.

Reference

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