全金屬矽化物互補式金氧半奈米晶片之

靜電放電防護電路設計與實現

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摘要

隨著互補式金氧半製程的持續發展並微縮至奈米等級，閘極氧化層變得愈來愈薄且擴散區的接面深度變得愈來愈淺，這些製程上的發展導致金氧半場效電晶體的閘極氧化層崩潰電壓下降以及金氧半場效電晶體的閘極漏電流增加。閘極氧化層崩潰電壓的下降會使得金氧半場效電晶體更容易受到靜電放電(Electrostatic Discharge, ESD)的轟擊而受損，因為靜電放電的本質並未隨著金氧半製程的發展而微縮，閘極漏電流的增加會使得靜電放電防護電路裡的金氧半場效電晶體在靜電放電事件與正常電路操作的情況下發生電性功能失常的問題。在可靠度(Reliability)領域中，靜電放電已成為積體電路產品在量產過程中最為重要的問題，對於所有的電子產品在設計階段時就必須謹慎地將靜電放電等問題納入考慮以符合可靠度的各種規範。為了達到全晶片靜電放電防護設計，所有的銲墊(Pad)，包括輸入/輸出(input/output)銲墊以及電源/接地(VDD/VSS)銲墊，皆必須具有靜電放電防護電路以提供有效的靜電放電防護予積體電路。介於輸入/輸出銲墊以及電源/接地銲墊的靜電放電防護元件無可避免地會對射頻(Radio Frequency, RF)與高速電路的訊號路徑產生寄生效應，而這些電路對於寄生效應是非常敏感的，因為過大的寄生效應會造成射頻與高速電路的電路性能嚴重衰減，因此對於應用在射頻與高速電路的靜電放電防護元件之挑戰則是靜電放電防護元件能夠承受最大的靜電放電耐受度並且達到其寄生效應的最小化。此外，介於電源/接地銲墊之間的靜電放電防護電路則可在電源軌線間提供有效的靜電放電防護，雖然電源軌線間靜電放電箝制電路的寄生效應對於內部電路毫無影響，但是金氧半場效電晶體閘極氧化層崩潰電壓的下降以及閘極漏電流的增加仍然大幅提高了靜電放電防護設計上的困難度。另外，積體電路的單位面積製作成本隨著互補式金氧半製程的持續微縮而快速地增加，因此，在佈局面積上具有高度效益的電源軌線間靜電放電箝制電路也是另一個設計上的挑戰。基於以上所提及之設計挑戰，本論文的研究主題包括：(1)適用於射頻與高速輸入/輸出電路的靜電放電防護二極體、(2)不需電容元件之電源軌線間靜電放電箝制電路、(3)具有等效靜電放電偵

測機制的電源軌線間靜電放電箝制電路、(4)具有閘極漏電流與閘極氧化層可靠度之設計考量的電源軌線間靜電放電箝制電路、(5)不需電阻元件之電源軌線間靜電放電箝制電路。

本論文第二章提出可適用於射頻前端與高速輸入/輸出銲墊的新型靜電放電防護二極體元件，其佈局型式分為八角形、四方中空形、八角中空形、多重四方形、以及多重四方中空形。在 90 奈米互補式金氧半製程的實驗結果顯示，相較於長條形與四方形佈局型式的二極體元件在相同的靜電放電耐受度之下可以達到較小的寄生電容，因此射頻前端與高速輸入/輸出電路的訊號衰減程度可以被降低。

在本論文第三章中，不需使用電容元件的新型靜電放電偵測電路已被提出並且驗證在 65 奈米 1.2 伏特的互補式金氧半製程。相較於傳統的 *RC*-based 靜電放電偵測電路，新型設計的佈局面積可縮小超過 54%，具有可調整維持電壓的新型設計在快速電源啟動以及暫態雜訊干擾的情形下擁有非常好的抗誤觸發與抗暫態引起的閂鎖效應之能力。

本論文第四章提出一個以大通道電晶體作為靜電放電箝制元件並且利用大通道電晶體的寄生二極體之電源軌線間靜電放電箝制電路，並且驗證在 65 奈米 1.2 伏特的互補式金氧半製程。利用二極體連接方式的電晶體作為等效電阻以及利用大通道電晶體寄生逆偏二極體作為等效電容，新型的電容耦合以及 *RC*-based 靜電放電偵測機制可不使用實際的電阻與電容元件就能達成，並且相較於傳統的 *RC*-based 靜電放電偵測電路，可顯著地縮小所需之佈局面積達 82%。

本論文第五章提出一個僅使用薄閘極氧化層元件以及使用矽控整流器(Silicon-Controlled Rectifier, SCR)作為靜電放電箝制元件的電源軌線間靜電放電箝制電路，並且驗證在 65 奈米 1 伏特的互補式金氧半製程。藉由降低在靜電放電偵測電路中元件閘極氧化層的跨壓，提出的電源軌線間靜電放電箝制電路可具有低漏電流，此外，藉由佈局的方式還可以將靜電放電偵測電路完全嵌入至矽控整流器元件中。在本章中，一個可操作在 2 倍 VDD 的電源軌線間靜電放電箝制電路也被提出，並且驗證在相同的製程。根據實驗結果，提出的電源軌線間靜電放電箝制電路搭配 50 微米寬的矽控整流器元件在偏壓 1 伏特的正常電路操作與室溫的情形下僅消耗 34.1 奈安培的漏電流。

本論文第六章提出一個僅使用薄閘極氧化層元件、使用矽控整流器作為靜電放電箝制元件、以及不需使用電阻元件的電源軌線間靜電放電箝制電路，並且驗證在 65 奈米 1 伏特的互補式金氧半製程。技巧性地使用閘極漏電流以實現等效電阻，*RC*-based 靜電放電偵測機制可不使用實際的電阻元件就能達成並且顯著地縮小所需之佈局面積。不需電阻元件的電源軌線間靜電放電箝制電路搭配 45 微米寬的矽控整流器在偏壓 1 伏特的正常電路操作與室溫的情形下僅消耗 1.43 奈安培的極低漏電流。

第七章總結本論文的研究成果，並提出數個接續本論文研究方向的研究題目。本論文所提出的各項新型設計，皆已經由實驗晶片進行驗證。本論文已有數篇國際期刊與國際研討會論文發表。

DESIGN AND IMPLEMENTATION OF ESD PROTECTION CIRCUITS IN NANOSCALE FULLY SILICIDED CMOS TECHNOLOGY

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Abstract

As CMOS technology is continuously scaled down to nanoscale, the gate oxide becomes thinner and the diffusion junction depth becomes shallower. These lead to the reduced gate oxide breakdown voltage and increased gate leakage current of MOS transistor. The reduced gate oxide breakdown voltage makes the MOS transistor more vulnerable to electrostatic discharge (ESD) because ESD is not scaled down with the CMOS technology. The gate leakage current makes the MOS transistors in ESD protection circuit malfunction during ESD stresses and normal circuit operating condition. ESD is one of the most important reliability issues for the integrated circuit (IC) during mass production. It must be taken into consideration during the design phase to meet the reliability specifications for all microelectronic products. For whole-chip ESD protection design, all pads, including the input/output (I/O) pads and VDD/VSS pads, are necessary to be implemented with ESD protection circuits to provide effective ESD protection for the IC. The ESD protection devices between the I/O pads and VDD/VSS pads inevitably cause parasitic effects on the signal path of RF front-end and high-speed circuits, which are very sensitive to those parasitic effects. The challenge of ESD protection devices for RF front-end and high-speed circuits is to sustain the highest ESD level and to achieve the smallest parasitic effects. Moreover, the ESD protection circuits between the VDD/VSS pads are necessary to provide ESD protection between the power rails. Although the parasitic effects of power-rail ESD clamp circuit have no impact on the internal circuits, the reduced gate oxide breakdown voltage and increased gate leakage current of MOS transistor greatly increase the difficulty of ESD protection design. In addition, the fabricated cost per unit area of the IC is dramatically increased with the continuously scaled-down CMOS technology. Therefore, the power-rail ESD clamp circuit with high efficiency of layout area is another design challenge. The research topics

based on aforementioned design challenges in this dissertation including: (1) ESD protection diode for RF and high-speed I/O applications, (2) capacitor-less power-rail ESD clamp circuit, (3) power-rail ESD clamp circuit with equivalent ESD-transient detection mechanism, (4) power-rail ESD clamp circuit with considerations of gate leakage current and gate oxide reliability, and (5) resistor-less power-rail ESD clamp circuit.

In Chapter 2, new ESD protection diodes drawn in the octagon, waffle-hollow, octagon-hollow, multi-waffle, and multi-waffle-hollow layout styles are presented in a 90nm CMOS process. The experimental results confirmed that they can achieve smaller parasitic capacitance under the same ESD robustness level as compared to the stripe and waffle diodes. Therefore, the signal degradation of RF and high-speed transmission can be reduced.

In Chapter 3, a new ESD-transient detection circuit without using the capacitor has been proposed and verified in a 65nm 1.2V CMOS process. The layout area of the new ESD-transient detection circuit can be greatly reduced by more than 54%, as compared to the traditional *RC*-based one. The new ESD-transient detection circuit with adjustable holding voltage has better immunity against mis-trigger and transient-induced latch-on event under the fast power-on and transient noise conditions.

In Chapter 4, a power-rail ESD clamp circuit realized with ESD clamp device drawn in the layout style of BigFET, and with parasitic diode of BigFET, is proposed and verified in a 65nm 1.2V CMOS process. Utilizing the diode-connected MOS transistor as the equivalent large resistor and parasitic reverse-biased diodes of BigFET as the equivalent capacitors, the new *RC*-based and capacitance-coupling ESD-transient detection mechanism can be achieved without using an actual resistor and capacitor to significantly reduce the layout area by ~82%, as compared to the traditional *RC*-based ESD-transient detection circuit.

In Chapter 5, a power-rail ESD clamp circuit realized with only thin gate oxide devices and with SCR as main ESD clamp device has been proposed and verified in a 65nm 1V CMOS process. By reducing the voltage difference across the gate oxide of the devices in the ESD-transient detection circuit, the proposed design can achieve a low standby leakage current. In addition, the ESD-transient detection circuit can be totally embedded in the SCR device by modifying the layout structure. In this chapter, a 2×VDD-tolerant power-rail ESD clamp circuit has also been proposed and verified in the same CMOS process. The proposed design with SCR width of 50μm can achieve a low standby leakage current of 34.1nA at room temperature under the normal circuit operating condition with 1.8V bias.

In Chapter 6, a resistor-less power-rail ESD clamp circuit realized with only thin gate oxide devices, and with SCR as main ESD clamp device, has been proposed and verified in a 65nm 1V CMOS process. Skillfully utilizing the gate leakage current to realize the equivalent resistor, the RC-based ESD-transient detection mechanism can be achieved without using an actual resistor. The resistor-less power-rail ESD clamp circuit with SCR width of 45μm can achieve an ultra-low standby leakage current of 1.43nA at room temperature under the normal circuit operating condition with 1V bias.

In this dissertation, several novel designs have been proposed in the aforementioned research topics. Measured results of the fabricated test chips have demonstrated the performance improvement. The innovative designs and achievements of this dissertation have been published or submitted to several international journals and conferences.

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首先我要感謝我的指導教授柯明道教授三年多來的耐心指導與鼓勵，使我能夠順利完成博士學業。在指導教授循序漸進的教誨下，讓我得以在積體電路靜電放電防護設計的領域中，由入門到能夠獨立解決問題。此外，指導教授認真的研究態度與嚴謹的處事原則，也讓我學習到挑戰困難與解決問題的正確態度與方法。雖然在過程中倍感艱辛，也經歷了不少挫折，然而卻讓我獲益良多。指導教授為研究群同學爭取的許多福利，更讓人感念在心。

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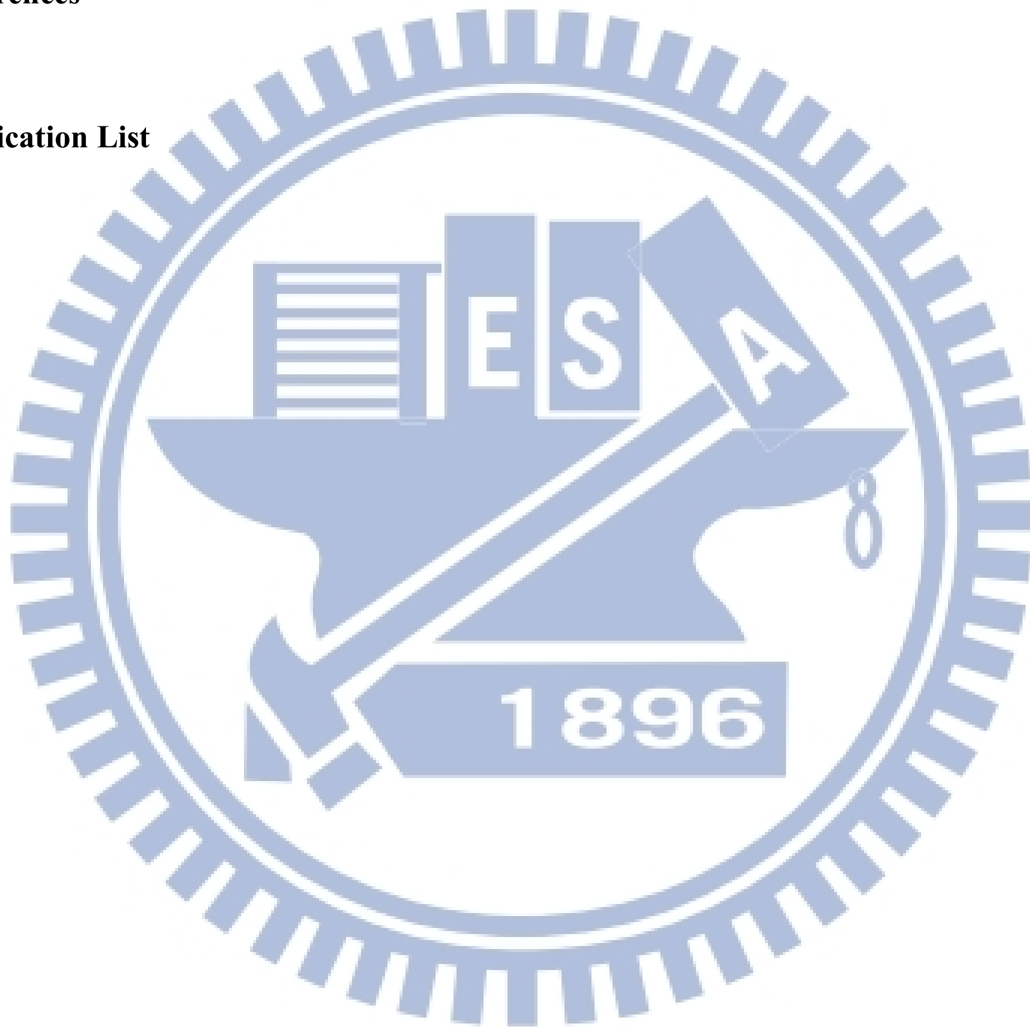

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