國立交通大學

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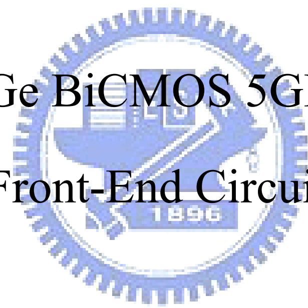
碩 士 論 文

SiGe BiCMOS 5GHz 射頻接收器前端電路



Design of SiGe BiCMOS 5GHz RF Receiver

Front-End Circuits

研究生：劉炳宏

指導教授：周復芳　博士

中 華 民 國 九 十 三 年 六 月

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碩　士　論　文

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中文摘要

在這篇論文研究中，我們首先會討論到積體電路製程的發展，SiGe BiCMOS 發展的進況及這個製程和 Si CMOS 的不同處，並比較其電路特性的優缺點。接著會探討兩個實做的電路主題；第一個主題爲操作在高頻 5.25GHz 的低雜訊放大器，電路完全未採用晶片外元件做爲匹配的設計以便日後和其他電路整合，在 2.5 伏特的的電壓下有 7.5mW 的消耗功率，並有 S_{11}8.3dB，功率增益爲 4.6dB，S_{22}10.9dB 及 IIP3 有 3dBm，雜訊指數則爲 9.3dB。因爲實測操作頻率往低頻移動，造成增益及雜訊的阻抗匹配點接有所變動，所以實測的電路特性並不如模擬預期，我們對這方面做了探討。第二個主題是 5GHz 的低功率共電流低雜訊放大器及降頻混頻器，將 Gilbert Cell 混頻器疊接在差動的低雜訊放大器之上以達到共用電流的目的，設計成射頻訊號爲 5GHz 及中頻訊號爲 10megHz 以方便量測，利用電路板量測，並已預估到電路板的打線等所產生的高頻寄生效應，有-1dB 的轉換功率增益及-5dBm 的 IIP3，電路操作在 2.5 伏特的的電壓下有 5mW 的消耗功率，且此量測結果和模擬結果有稍爲的差距，我們針對了輸入轉導值及輸出端阻抗做了探討。以上兩組晶片皆以台積電 SiGe BiCMOS 0.35-μm 的製程實現並完成量測和模擬比較討論。

Design of SiGe BiCMOS 5GHz RF Receiver Front-End Circuits

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Abstract

This thesis contents two works. First of all, we discuss the development of SiGe BiCMOS technology and the comparison between the SiGe and Si technologies. The first circuit, we implement a fully integrated 5.25GHz RF low noise amplifier, this circuit has a 8.3dB S_{11}, a 4.6dB power gain, a 10.9dB S_{22}, a 3dBm IIP3 and a 9.3dB noise figure, under the 7.5mw power consumption with a 2.5 V supply voltage. Because the operating frequency shift to lower frequency, the gain and noise impedance matching point are changed, the measurement performance is not as good as simulation. Furthermore, we have completed a low-power concurrent low noise amplifier and down-converter. A Gilbert Cell is stacked on the top of differential LNA to achieve the re-use of DC current. We choose The RF signal is at 5GHz and IF signal is at 10megHz for measurement conveniently. The circuit is on-board testing and all the effect of parasitic and bonding wires is being taken account. The conversion gain is -1dB and IIP3 is -5dBm under the 5mw power consumption with a 2.5 V supply voltage. We would find out the difference reasons between simulation and measurement. These two IC have fabricated in a TSMC SiGe BiCMOS 0.35-μm technology. Moreover, the measurement and comparison with simulation had been done.

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還有要感謝實驗室的學長姐邦瑞、朝安、先成、佳民、美蒨，及我的同學盈蒼、政良、汪揚、馥榕，學弟家良、偉誠、欽賢、政宏、柏達、俊賢，在這兩年來在實驗室渡過一起討論一起生活的研究過程，帶給我一個美好、難忘、也最充實的時光。

最後我要感謝我最愛的父母親和家人，在我想走的路上，一路給我最大的支持和自由，讓我能順利地完成碩士學業。

Contents

Chinese Abstract………………..……………..……….……………..…...I

English Abstract……….…………………………….………………II

Acknowledgement…………………………………………………III

Contents……………………………………………………………IV

Tables Captions…………………………………..…………………VI

Figures Captions………………………………..…..………………VII

CHAP 1. Introduction……………………………………………....………1

1.1 Motivation…………………………………………..…………………………1

1.1.1 Communication ICs Develop ………………………………………………1

1.1.2 Designed Circuits Introduction ……………………………………..…..2

1.2 Thesis Organization ………………………………………………………..……6

CHAP 2. SiGe Technology Applications to RF Integrated Circuit...........7

2.1 SiGe BiCMOS Technology Evolution………………………………………7

2.2 Active Device and RF Model ………………………….………………..……10

2.2.1 RF CMOS Model 10

2.2.2 SiGe Bipolar Model ………………………………………………………12

2.3 Passive Device and RF Model………………………………………………...14

2.3.1 MIM Capacitors…………………..……………………….……….……14

2.3.2 Spiral Inductors ……………………………………………………….....15

CHAP 3. A 0.35-μm SiGe BiCMOS 5.25 GHz LNA ……………………..18

Design and Implementation………………..…………………18

3.1 Architecture and Design Concept of LNA…...18

3.1.1 Architecture of LNA …………………………………………………18

3.1.2 Design of Common-Source with Inductive Degeneration LNA ……..21

3.2 Measurement Consideration …...24

3.3 Simulation and Measurement results comparison ……………………….....27

CHAP 4. A 0.35-μm SiGe Concurrent LNA and Mixer ………………..34

Design and Implementation…………………………….………34

4.1 Architecture and Design Concept of Concurrent LNA and Mixer…………34

4.1.1 Architecture of Mixer ……………………………………………….....34

4.12 LNA and Mixer Circuits Design ……………………………………...…38

4.2 Measurement Consideration……………………………………….….……43

4.3 Simulation and Measurement results comparison……………………….…47

CHAP 5. Conclusion……………………………………………………....56

5.1 Conclusion …………………………………………………..……….56

5.2 Future Progress……………………………………………………….....58

Reference………………………………………………………………..59

1896

Tables Captions

Table1.1.1 Comparison of cascade LNA ……………………………………….……4

Table1.1.2 Comparison of concurrent LNA and mixer………………………………5

Table2.1.1 Transport properties of buck silicon germanium at 300K ………………..8

Table3.3.1 Performance summary ……………………………………..…….31

Table3.3.2 Comparison of recently LNA paper ……………………………………..32

Table4.3.1 The bias voltage versus the current …………………………….………..51

Table4.3.2 Comparison between simulation and measurement of R_{out}……………...52

Table4.3.3 The summary of performance ……………………………………………53

Table4.3.4 Comparison of recently papers...55

Figures Captions

Figure 1.1.1 (a) Effective mobility is enhanced by 70% over the control and universal mobility even at a very high vertical field of >1.0MV/cm

(b) Mobility enhancement is depending on Ge content in the relaxed SiGe layer ……………………………………………………….…….2

Figure 1.1.2 The 5GHz Front-End Cascode block diagram …………………….………3

Figure 1.1.3 The schematic of works ……………………………………………..…….3

Figure 2.1.1 Atom spacing comparisons ……………………………………..……8

Figure 2.1.2 Mobility enhancement factor ……………………………………………9

Figure 2.1.3 Cross section view of Si/SiGe PMOS and HBT ………………………..…9

Figure 2.2.1 MOSFET cross section view …………………………………………..……10

Figure 2.2.2 Illustration of the sub-circuit of the RF MOSFET model …………..…10

Figure 2.2.3 The Layout top view of RF MOSFET ………………………………………11

Figure 2.2.4 The MOSFET equivalent circuit includes the noise source ………..….12

Figure 2.2.5 Cross section view of vertical NPN …………………………..……12

Figure 2.2.6 The full Mextram equivalent circuit for the vertical ………………...…13

Figure 2.2.7 The layout top view of NPN ……………………………….……..13

Figure 2.3.1 The sample of MIM capacitor ……………………………………....15

Figure 2.3.2 The equivalent circuit of a MIM capacitor …………………………....15

Figure 2.3.3 The equivalent sub-circuit of an spiral inductor …………………..…..16

Figure 2.3.4 The Q factor of spiral inductor ……………………………….…..16

Figure 2.3.5 Layout top view of inductor ……………………………….…..17

Figure 3.1.1 The architectures of LNA ……………………………………………...19

Figure 3.1.2 (a) Noise modeling of BJT (b) Impedance matching network ………...20

Figure 3.1.3 The schematic of cascode LNA with degeneration inductor …………22
Figure 3.1.4 GSG pad structure ……………………………………………………..23
Figure 3.2.1 On wafer measurement instrument; probe station and on-wafer GSG testing layout …………………………………………………………..24
Figure 3.2.2 The testing setup of (a) S-parameters (b) Output Power (c) Two-tone test (d) Noise Figure ……………………………………………………....26
Figure 3.3.1 Comparison between simulation and measurement of S11 …………....27
Figure 3.3.2 Comparison between simulation and measurement of S21 ……………28
Figure 3.3.3 Comparison between simulation and measurement of S22 ……………29
Figure 3.3.4 Comparison between simulation and measurement of gain …………...29
Figure 3.3.5 Comparison between simulation and measurement of two-tone test…..30
Figure 3.3.6 Comparison between simulation and measurement of noise figure …...31
Figure 3.3.7 The layout and test plan of LNA 33
Figure 3.3.8 The die photo of LNA..33
Figure 4.1.1 A switching simple and switching mixer circuit 35
Figure 4.1.2 The Gilbert cell 37
Figure 4.1.3 (a) A conceptually figure of stacking the LNA in the top of the mixer (b) Transistor implementation 38
Figure 4.1.4 The schematic of cascode structure 39
Figure 4.1.5 The schematic of buffer 40
Figure 4.1.6 The parasitic effect of bond-wire 40
Figure4.1.7 Simulation of the bond-wire inductance variation range (3nH, 3.5nH and 4nH), the input return loss are both high than 15dB (a)RF input port (b) LO input port 41
Figure 4.1.7 Layout and test plan of this circuit 42
Figure 4.1.8 Die photo with bond-wire 42

Figure 4.2.1 PCB layout 43

Figure 4.2.2 Reality PCB circuit 43

Figure 4.2.3 Measurement setup of (a) Conversion Gain (b) Two-tone IIP3 testing

(c) Input return loss testing …………………………………………..45

Figure 4.2.4 Measurement picture 45

Figure 4.2.5 Loss testing board 46

Figure 4.2.6 The measurement results of loss; about 0.3dB 46

Figure 4.3.1 Comparison between simulation and measurement ………………….…47

Figure 4.3.2 The bonding wire ……………………………………………….…..…48

Figure 4.3.3 RF power =-35dBm @5GHz, LO power = 0dBm@ 4.99GHz, F=10MHz

………………………………………………………………..………48

Figure 4.3.4 Conversion gain versus the LO input power 49

Figure 4.3.5 Conversion gain versus the RF input power 49

Figure 4.3.6 Comparison between simulation and measurement of IIP3 ……………50

Figure 4.3.7 A simplified circuits; Vbias means lowest layer device bias voltage (bias current is domain by lowest layer active device; BJT), Gm means the total transconductor of core circuits, 50Ω is the instrument impedance

……………………………………………………………………..50

Figure 4.3.8 The characteristic of bias voltage versus the current …………………..51

Figure 4.3.9 The buffer output impedance consideration; $R_{out} = {}^{1}\!/_{gm}$ 52

Figure 4.3.10 A diagram of Rout and 50ohm load ……………………………….…53

Figure 4.3.11 The bonding wires effect ……………………………………………...54

Figure 5.2.1 A merged LNA and mixer ……………………………………..…58

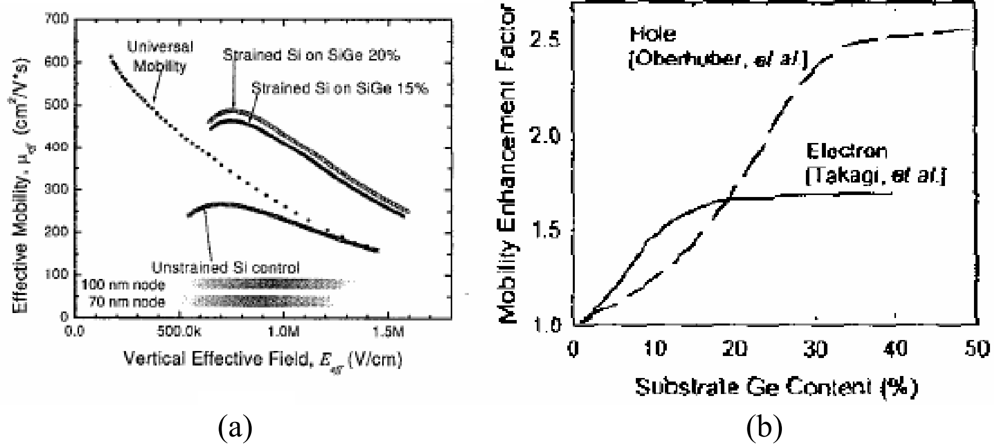
Chapter 1

Introduction

1.1 Motivation

1.1.1 Communication ICs Develop

The low-cost, low-power and highly integration have become the tread for the communication ICs. Silicon integrated circuit technology is a ubiquitous feature of modern electronics industry, because silicon has numerous practical advantages as a semiconductor material, including (1) ease of growth of large, low-cost; (2) availability of a stable high-quality dielectric, SiO_2; (3) ease doping and fabrication of ohmic contacts; and (4) excellent mechanical properties is including strength and high thermal conductivity. However the comparative low intrinsic speed of electronic in silicon, which is related to their effective mass and saturated drift velocity, was inferior to competing Ⅲ-Ⅴtechnologies of GaAs and InP, but the well-known limitations of Ⅲ-Ⅴtechnologies including higher defect densities, poor thermal conductivity, and lack of a passivating native oxide. One of the important advances in silicon technology has been the addition of alloy of silicon and germanium (Ge) to the base of a bipolar transistor, resulting in the Si/SiGe HBT. The device emerged from a variety of industrial and university research laboratories in the early 1990s and is now in commercial production for wide range of high-frequency communication applications. Si/SiGe technology promises to satisfy the simultaneous requirements of outstanding high-frequency performance and low-cost silicon manufacturing. [1] Fig 1.1.1 points out the advantage of SiGe technology; enhancing the effective mobility. [2] [3]



(a) (b)

Fig 1.1.1 (a) Effective mobility is enhanced by 70% over the control and universal mobility even at a very high vertical field of >1.0MV/cm

(b) Mobility enhancement is depending on Ge content in the relaxed SiGe layer

Because of the growing demands of personal communication and notebook market, higher data rate wireless local area network (WLAN) system has been announced. As shown in Fig 1.1.1, the IEEE802.11a standard operates in 5GHz unlicensed national information infrastructure (UNII) band, which is base on the orthogonal frequency division multiplexing (OFDM) modulation. It can provide the data rate up to 54Mb/s in each 20 MHz channel and this is five times data rate as the currently used IEEE802.11b 2.4GHz-ISM-Band operation.[4] [5]

1.1.2 Designed Circuits Introduction

Now we design a low noise amplifier (LNA) circuit up to the higher 5GHz band operation. First work presents a full integrated RF SiGe a common-source with inductive degeneration single stage LNA for the access of 5.25GHz-band. We integrated the front-end circuits of LNA and down conversion in the topology of cascode at second stage. In this circuit, two power-hungry front-end blocks are merged; a Gilbert cell down-mixer is stacking on the top of differential

common-source with inductive degeneration LNA (Figure 1.1.2). This structure could be concurrent biasing to save power and improve the problem of interface matching simultaneously; the supply voltage is set at 2.5V. This circuit could integrate with other RF circuits easily. [6] The schematic of two works are illustrated in Fig 1.1.3.

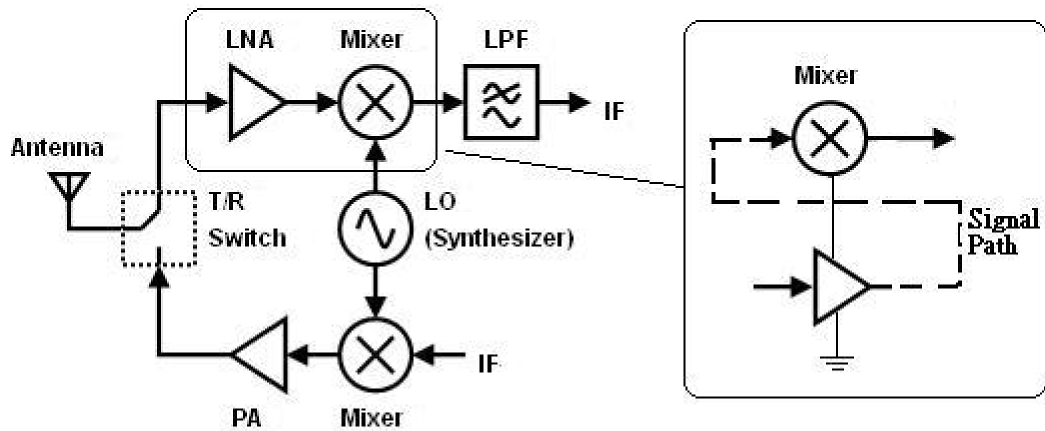
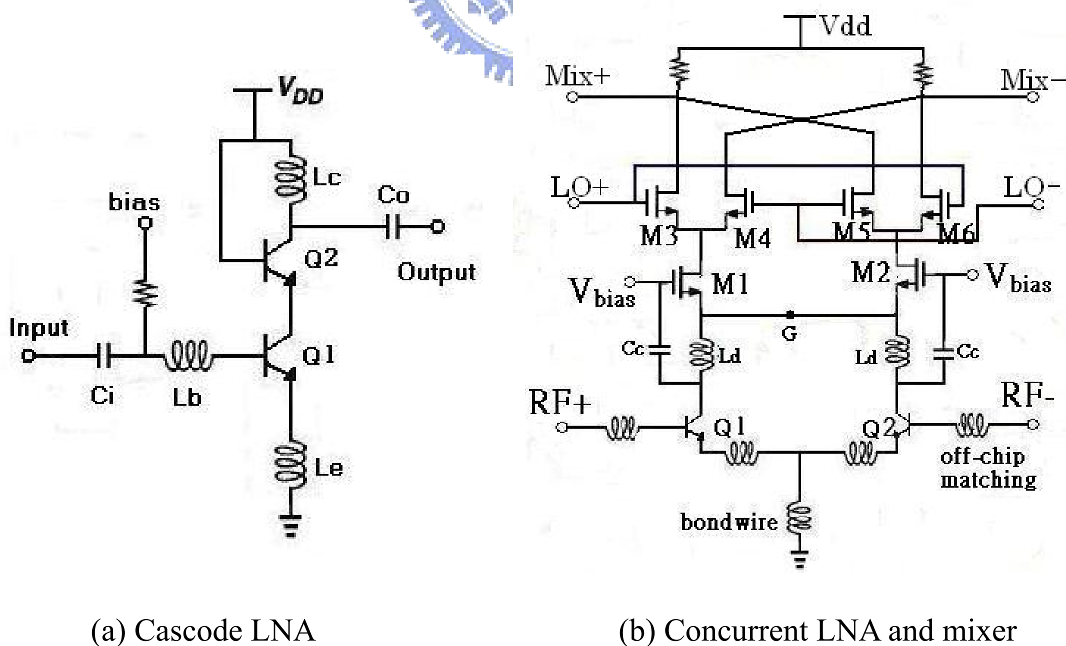


Figure 1.1.2 The 5GHz Front-End Cascode block diagram



(a) Cascode LNA

(b) Concurrent LNA and mixer

Fig 1.1.3 The schematic of works

All the simulation and measurement results of the two works is shown in Table 1.1.1 (Cascode LNA) and Table 1.1.2 (Concurrent LNA and mixer), respectively.

Comparison between this work and recently papers are listed in table. The differentia between simulation and measurement and performance comparison with other papers would be discussed in detail in section 3.3 and section 4.3.

REF	[19] 2002	[20] 2003	[21] 2002	[22] 2002	[23] 2002	This work 2003.08	
Frequency (GHz)	5	4.4-5	5.8	5.8	6	5.2	3.2
Power (mW)	31	24	20	16	13	11	7.5
NF (dB)	1.7	2.2	3.2	4.4	2.3	2.9	9.3
Gain (dB)	18.3	14.1	7.2	11	17	14.9	4.6
S11 (dB)	-25	-13.8	-11	-20	---	-24.1	-8.3
S22 (dB)	-27.3	-8.5	-17	-12	---	-23.5	-10.9
IIP3 (dBm)	-4.0	-6.2	6.7	-2	-7	-3.2	3
P_{1dBin} (dBm)	-12.3	11.6	-3.7	-10.4	-18	-15.3	-6.5
Process	SiGe 0.5um	SiGe 0.25um	CMOS 0.35um	SiGe 0.35um	SiGe 0.35um	SiGe 0.35um	SiGe 0.35um
Condition	Sim.	Sim.	Meas.	Meas.	Meas.	Sim.	Meas.

Table 1.1.1 Comparison of cascode LNA

REF	1[22] 2002	2[26] 2003	3[6] 2003	This work 2003.10	
				Sim.	Meas.
Frequency (GHz)	5.8	2.1	2.4	5	5
Power (mW)	48	21.6	6.3	5.1	5
Gain (dB)	20.2	23	29	6.3	-0.9
NF (dB)	9.9	3.4	3	6.8	---
IIP3 (dBm)	-6.8	-3	-16	-15	-5
P_{1dBin} (dBm)	-14	---	---	-25.1	-16
IF (Hz)	0	0	---	10Meg	10Meg
Process	SiGe 0.35um	CMOS 0.35um	CMOS 0.25um	SiGe 0.35um	SiGe 0.35um
Architecture	Two-stage LNA+ Micromixer	Concurrent LNA+ Mixer	Concurrent LNA+ Mixer	Concurrent LNA+ Mixer	Concurrent LNA+ Mixer

Table 1.1.2 Comparison of concurrent LNA and mixer

The front-end circuit is simulated by the harmonic balance tools Eldo-RF. This two IC has been fabricated using TSMC 0.35-μm SiGe BiCMOS foundry through Chip Implementation Center (CIC). The on-wafer testing measurements results have been fulfilled at National Nano Device Laboratories (NDL) and PCB layout measurement results have been accomplished at Chip Implementation Center (CIC).

1.2 Thesis Organization

This work discusses about the front-end circuits design and implementation for WLAN frequency bands. The contents consist of two major topics: "A 0.35μm SiGe BiCMOS 5.25GHz LNA" and "A 0.35μm SiGe low power concurrent LNA and mixer", respectively in Chapter 3 and Chapter 4. We will present the design flow and experimental results. Moreover, we will discuss the reasons of differences between simulation and measurement results.

In Chapter 2, we introduce the base SiGe technology application to RF integrated circuits. We will discuss the components such as: BJTs, MOSs, capacitors, inductors, application to the RF front-ends.

In Chapter 3, section 3.1 will start from the 5.25GHz LNA architecture and design consideration. The next, we will bring up the design concepts and consideration of this circuit. We will also show the on-wafer testing methods application to this work in 3.2. The section 3.3 will compare the simulation and measurement results.

Chapter 4 presents the design and implementation of concurrent LNA and mixer. We will introduce the design theories in section 4.1 and measurement method in 4.2, respectively. The simulation and measurement results comparison is in section 4.3.

Finally, the conclusions and future progress are drawn in chapter 5.

Chapter 2

SiGe Technology Applications to RF Integrated Circuit

2.1 SiGe BiCMOS Technology Evolution

Because of the explosive growth in wireless personal communication market, the demand for the balance in performance, cost, and power consumption becomes a remarkable design consideration than in the past. The silicon-based technology, Si/SiGe, exhibit performance compatible with the demand of the low-power wireless communications marketplace, and it retain the low cost than Ⅲ-Ⅴ technologies of its silicon pedigree. Although the SiGe and bipolar device can provide the highest performance for the RF ICs, the conventional digital CMOS device still have the low cost, superior linearity, and dynamic range per power than that of bipolar devices. Furthermore, another noticeable advantage over the CMOS technology is that it can be easily integrated with the base-band digital or mixed-signal partition, because it is also the logic process. Therefore, we can realize that the Si/SiGe BiCMOS RF IC is the key point for system-on-chip (SOC). This technology wills also provide for a straightforward path for integration of standard radio-frequency functions along with analog-to-digital conversion and digital signal processing onto a signal high-performance integrated circuit. The 0.35um SiGe processing provided by TSMC has been specifically designed to be as compatible with existing CMOS technology as possible.

The low mobility of electrons and holes in silicon limits the CMOS application

to relatively frequency. Because silicon has smaller lattice constant (atom spacing) than Germanium, when silicon is grown in SiGe, silicon might be stretched, form a strained layer, as shown in Fig 2.1.1. [7]

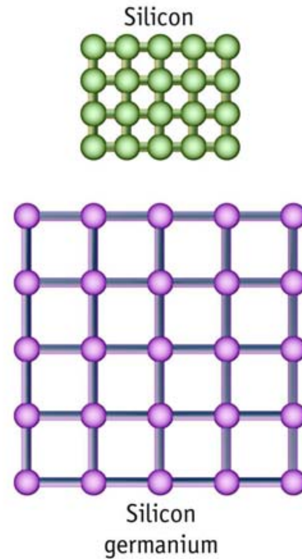


Fig 2.1.1 Atom spacing comparisons

Table 2.1.1 shows the important properties of Silicon and Germanium. From the table, we know bulk Germanium's hole mobility is even greater than the electron mobility of bulk silicon. Mobility enhancement can vary depending in Ge content in the relaxed SiGe layer a well as temperature. As shown in Fig2.1.2, mobility enhancement increases linearity with Ge content up to certain point, 20% Ge content for electron and 40% Ge content for hole, and then saturate afterward. [3] Since lower Ge content can achieve higher material quality in general, technology incentive is toward 20% than higher percent Ge.

	Effective Mass of electron	Effective Mass of hole	Electron Mobility (cm^2/ Vs)	Hole Mobility (cm^2/ Vs)	Band Gap (eV)	Dielectric constant
Ge	0.22	0.29	3900	1900	0.7	16
Si	0.33	0.55	1500	450	1.1	12

Table 2.1.1 Transport properties of bulk silicon germanium at 300K

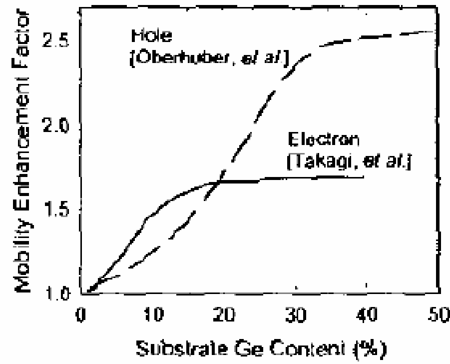


Fig 2.1.2 Mobility enhancement factor

In order to apply the higher mobility of SiGe to microelectronics technology, researchers have proposed many structures. In 1982, IBM developed UHV-CVD [8] and in 1987, SiGe base HBT was fabricated. Low base resistance, high gain and high early voltage make the SiGe HBTs ideal foe analog and mixed-signal applications SiGe HBTs has been incorporated into CMOS to get good performance of BiCMOS. [9] A basic structure of SiGe PMOS and HBT are shown in Fig 2.1.3. [10] [11]

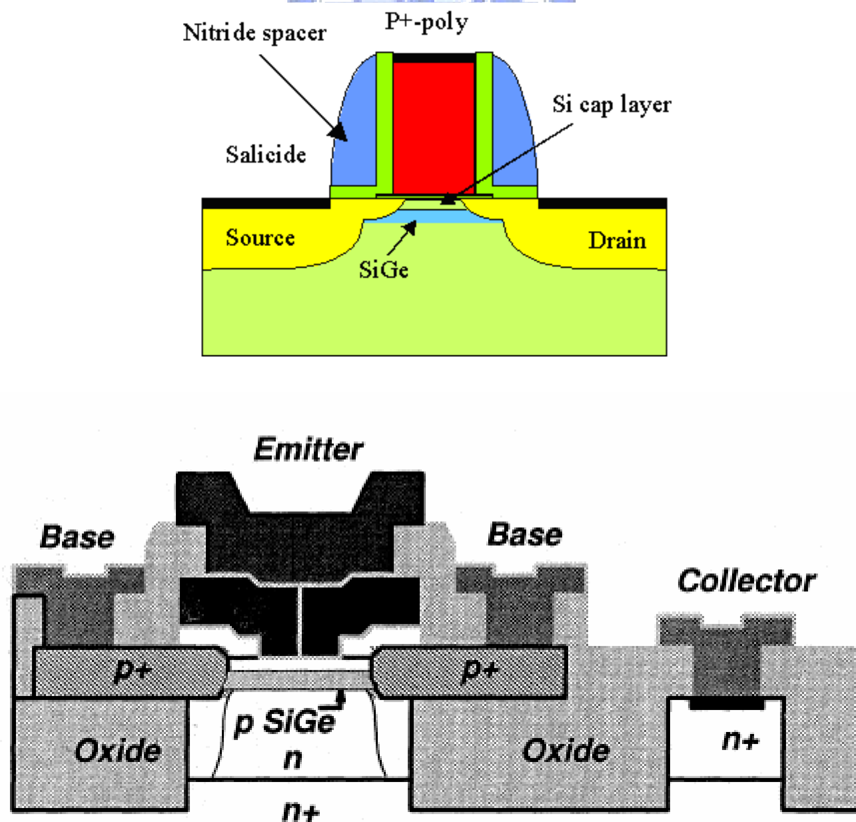


Fig 2.1.3 Cross section view of Si/SiGe PMOS and HBT

2.2 Active Device and RF Model

2.2.1 RF CMOS Model

CMOS transistor physical model is shown in Fig 2.2.1. [12] An RF small signal model based on the sub-circuit approach is given in Figure 2.2.2. It includes the parasitic components at the gate, source, drain and substrate. The core intrinsic model is base on the spice model BSIM3v3, which can be used to model the MOSFET nonlinear characteristics at radio frequency operation.

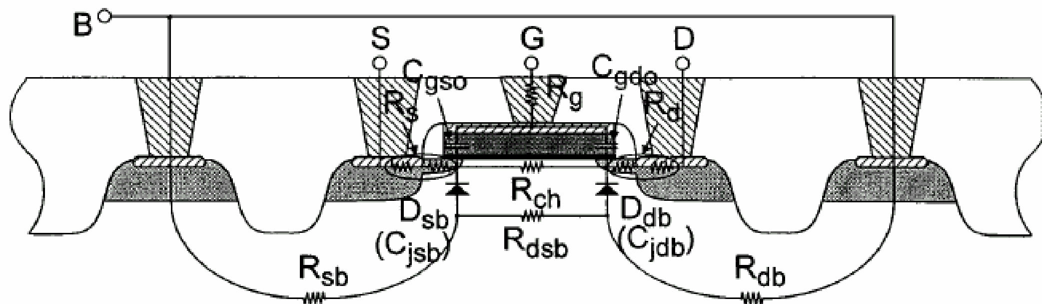


Figure 2.2.1 MOSFET cross section view

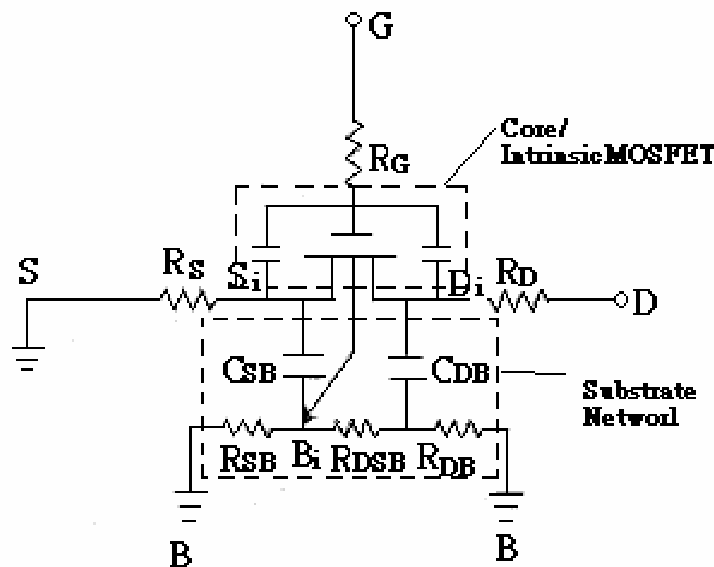
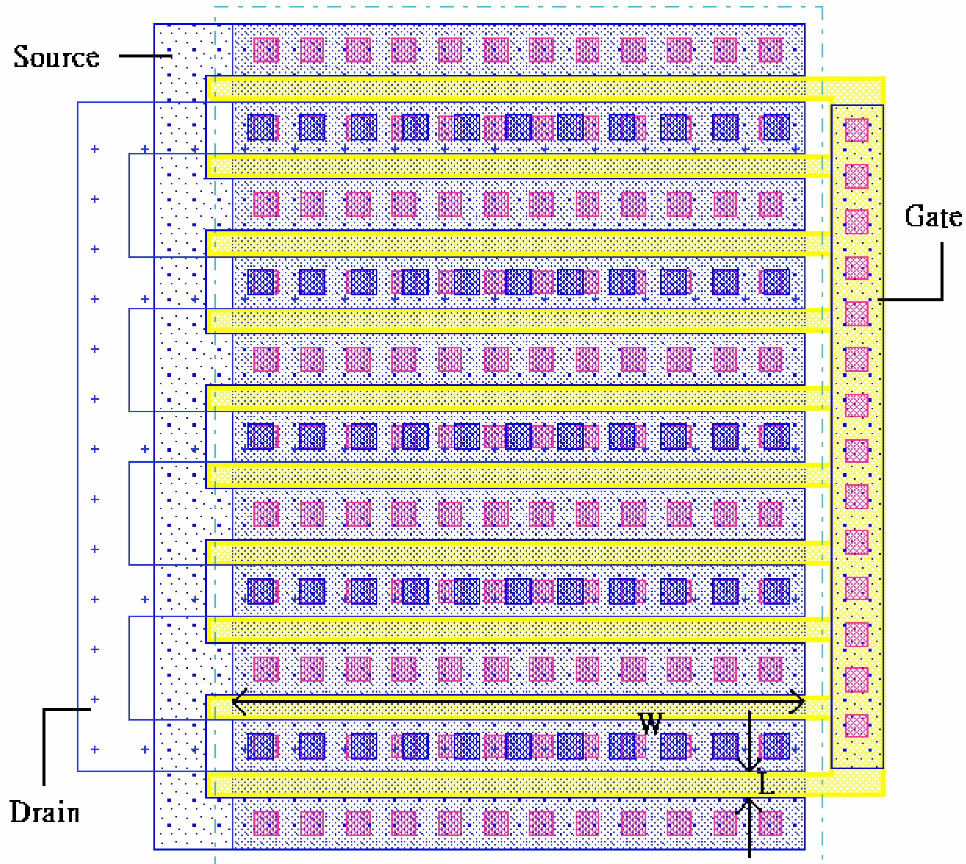


Figure 2.2.2 Illustration of the sub-circuit of the RF MOSFET model

Besides of the modeling, the physical layout consideration is a great influence to really high frequency performance. A standard physical layout corresponding to a modeled sub1circuit provided by TSMC is shown in Fig2.2.3. [13] Furthermore, when we layout a real circuit we must consider with many issues such as current endurance, relationship with other components, and ac signal coupling etc.



Total Gate width (W_g) = W * N

Figure 2.2.3 The Layout top view of RF MOSFET

In the BSIM3v3, it has built-in thermal noise characteristics in the core sub-circuit shown in figure 2.2.4. [12] Unfortunately, nowadays the BSIM3v3 model does not provide an accurate noise model for RF range so that the noise parameter simulation is not completely convinced.

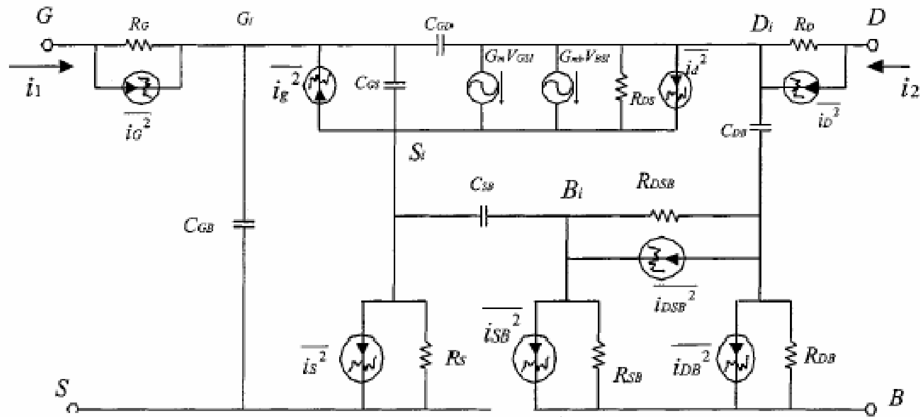


Figure 2.2.4 The MOSFET equivalent circuit includes the noise source.

2.2.2 SiGe Bipolar Model

Bipolar transistor cross section view is shown in Fig 2.2.5.The RF small signal model is provided for each vertical NPN transistor based on Mextran 504 model (shown in Fig 2.2.6). It contains description for the effects of bias-dependent Early effect, low-level non-ideal base current, velocity saturation effects on the resistance of the epi-layer, thermal noise, shot noise and 1/f noise, etc. [13]

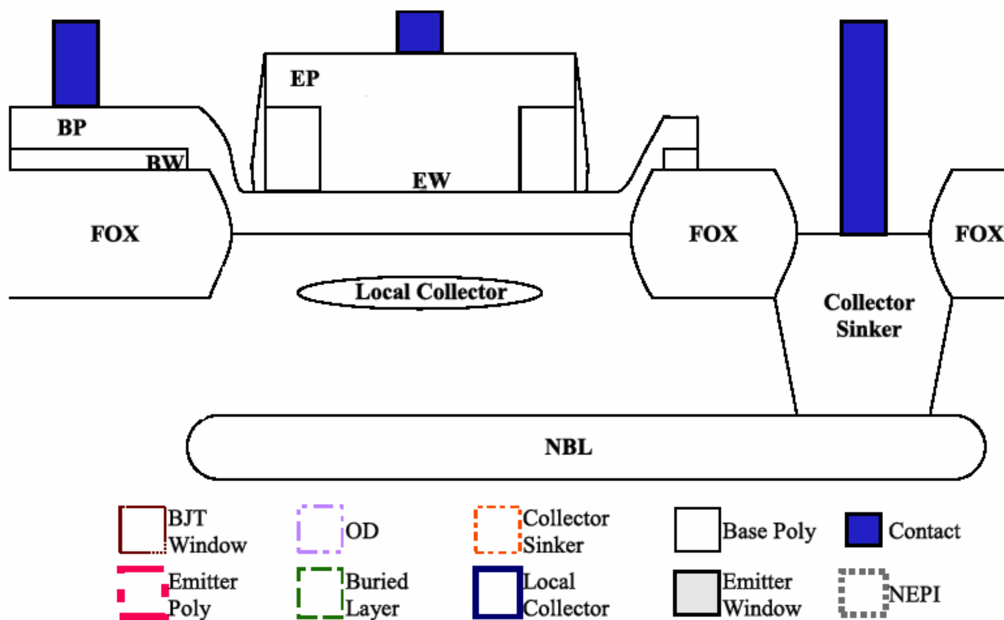


Fig 2.2.5 Cross section view of vertical NPN

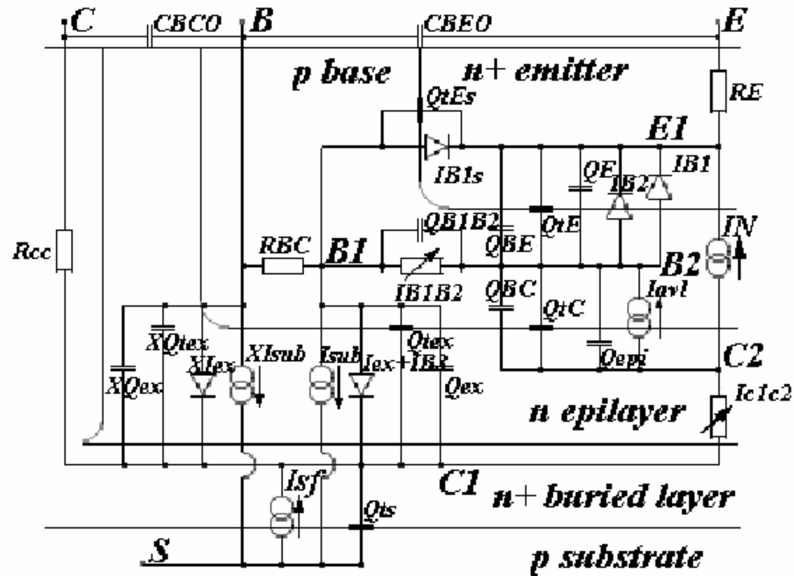


Fig 2.2.6 The full Mextram equivalent circuit for the vertical

The foundry provides three NPN transistor types; a high voltage NPN, a standard NPN and a high speed NPN. We select the high speed NPN which peak Ft is around 67GHz at Vce = 1V as RF active components used with circuits that supply voltage 2.5V. A standard layout cell is shown in Fig 2.2.7.

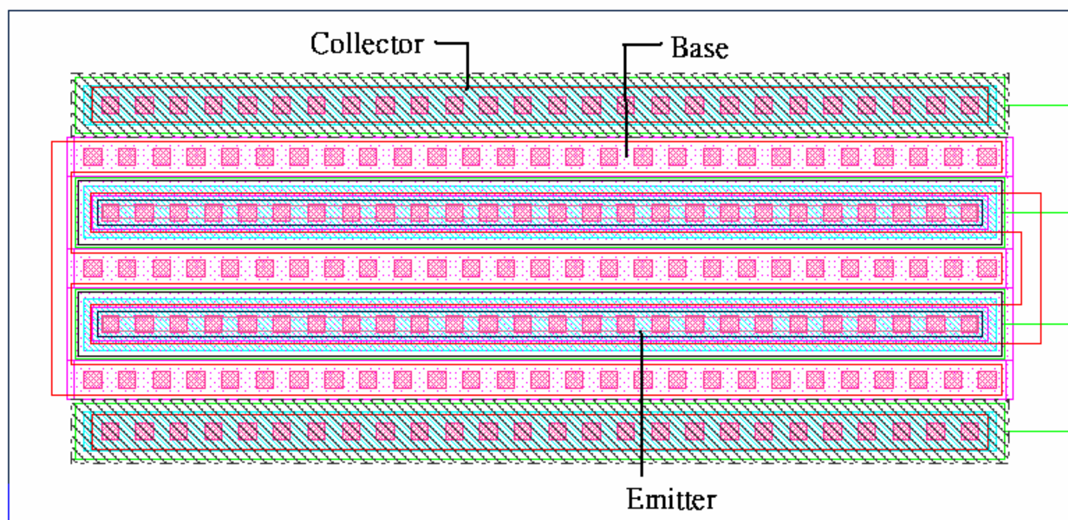


Fig 2.2.7 The layout top view of NPN

2.3 Passive Device and RF Model

For the analog mixed-mode or RF circuits design, the passive components such as the resisters, capacitors, and inductors are the significant effect toward circuit performance. The passive involved with biasing condition, DC/AC blocking and matching impedances. Therefore the passive devices, MIM capacitor, varactor, spiral inductor and poly resistor, modeling and improvement are the inevitable work to RF circuits design.

2.3.1 MIM Capacitors

The most linear on-chip capacitors are metal-insulator-metal (MIM) structures as shown in figure2.3.1. The MIM capacitors has high Q-factor, low loss and stable capacitance which apply the principle of parallel plate capacitors that the capacitance can be calculated from the formula

$$C \approx \varepsilon \frac{A}{H} = \varepsilon \frac{W \cdot L}{H} \tag{2.1}$$

which ε is the dielectrically constant; A is plate area can be calculate by W*L; H is two plate distance[14]. Designed can change the width and length of the top MIM cap plate (CTM) to get the expected capacitance value; unit capacitance is $1fF/um^2$. The MIM capacitors use an additional layer (CTM) as top plate between matal2 and metal3. Additionally, a sub-circuit and component description of MIM capacitor which performs the non-ideal effect from the lossy si-substrate and some parasitic resistance, inductance, and capacitance shows in figure2.3.2. Generally, the Q value of MIM capacitors can reach to 30~80 and depends on the width and operation frequency of capacitors.

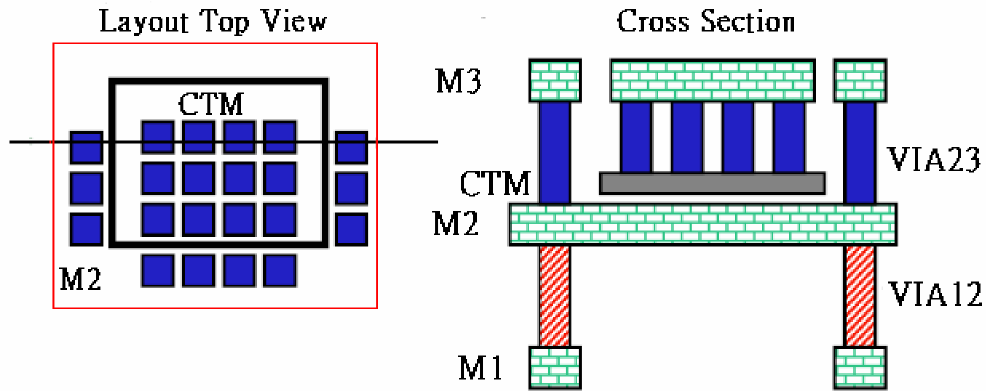


Fig 2.3.1 The sample of MIM capacitor

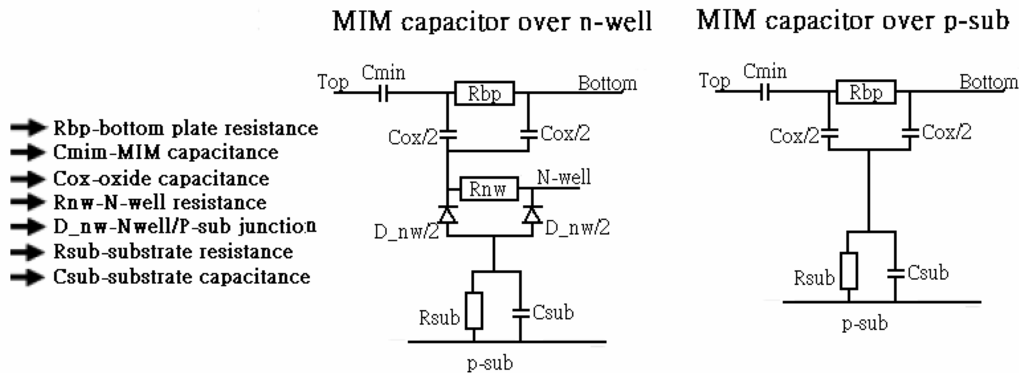


Figure 2.3.2 The equivalent circuit of a MIM capacitor

2.3.2 Spiral Inductors

The on-chip spiral inductors are nowadays the highly critical structures for RFIC. The accurate at inductance is favorable for impedance matching. The most useful advantage of spiral inductors is analytical formulas for inductance [15]. Figure 2.3.3 shows the equivalent sub-circuit model of an inductor. We set the input impedance is **Zin = R + jX,** then the inductance (L) is defined that the image part from port 1 to port 2 over the operating angular frequency (ω) and the Q value is defined that the image part over the real part of the input impedance, respectively.

$$Q = \frac{X}{R} \quad , \quad L = \frac{X}{\omega} \tag{2.2}$$

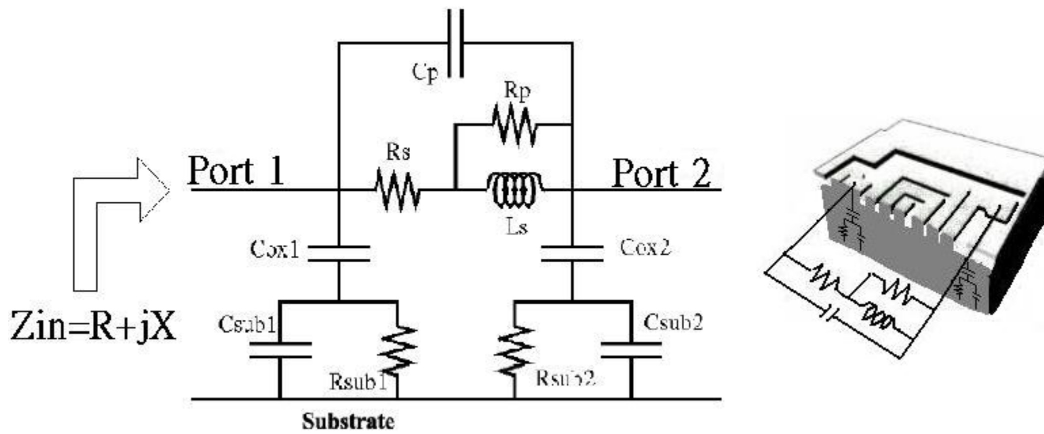


Figure 2.3.3 The equivalent sub-circuit of an spiral inductor

Generally speaking, an on-chip spiral inductor's Q value is 4~10 with the appropriate design of geometrical sizes and the self-resonance-frequency (SRF) is depend on the inductance; the SRF is must higher than the operating frequency.

Because of the Q value depends on the real part of input impedance, so we can determine the Q value by the effective resistance and inductance. Figure 2.3.4 shows the comparison of measure and model parameters offered by foundry. [13] This inductor is a 4 turns and measurement results shown that it is applicable at the high frequency operation beyond 5GHz.Only signal layer inductors provided by this process, because three metal layers in technology. The layout top view and the key layout parameters of spiral inductor are shown in Fig 2.3.5

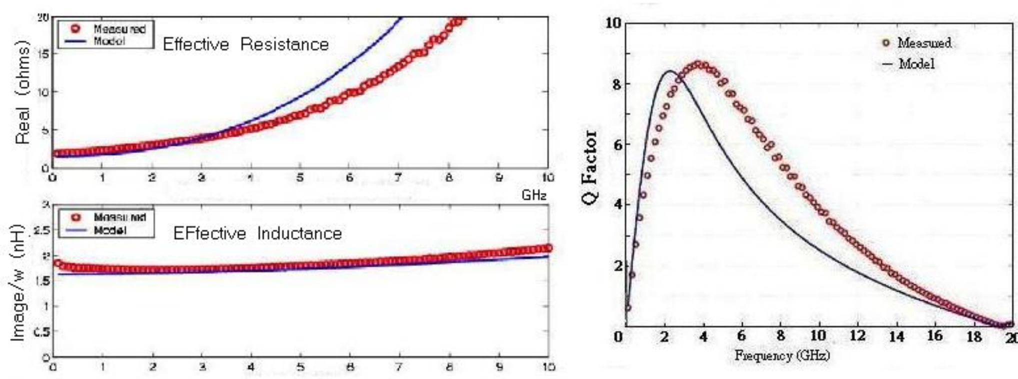
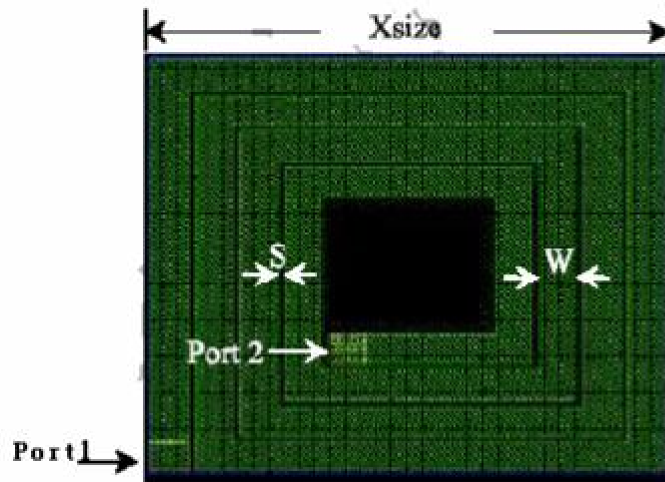


Fig 2.3.4 The Q factor of spiral inductor



N: Number turns

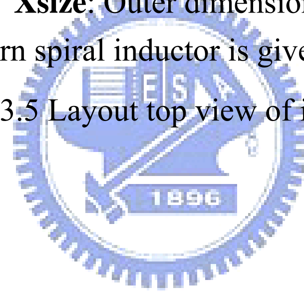
W: Metal width of top metal

S: Metal space of top metal

Xsize: Outer dimension

A typical 4-turn spiral inductor is given in this figure.

Fig 2.3.5 Layout top view of inductor



Chapter 3

A 0.35-µm SiGe BiCMOS 5.25G LNA Design and Implementation

3.1 Architecture and Design Concept of LNA

LNA are one of the key performance bottlenecks in an RF system. The low noise amplifier is required to contend with a variety of signals from the antenna and both low noise and high linearity are simultaneously required. But these requirements are often at odds with an additional requirement of low power consumption. As the case stand, the key design point is the noise and the trade off between power consumption and noise consideration. The accurate noise behavior is unknown at present, but we can use rough noise formula, noise equivalent model and the topology of LNA to determine how to reduce the noise figure. The SiGe BiCMOS process could execute higher performance than CMOS proved by several research papers. The SiGe HBTs has a significant improvement over standard Si BJT performance. We select the SiGe Bipolar to act as the noise low amplifier in this thesis.   .

3.1.1 Architecture of LNA

To design a LNA, the minimum noise figure and maximum power gain are the most important consideration. In fact, the noise performance is depending on the LNA experimental results and appropriate architectures. Two architectures of LNA for the design goal are shown in Fig 3.1.1; common-emitter stage and common-base stage. [16]   .

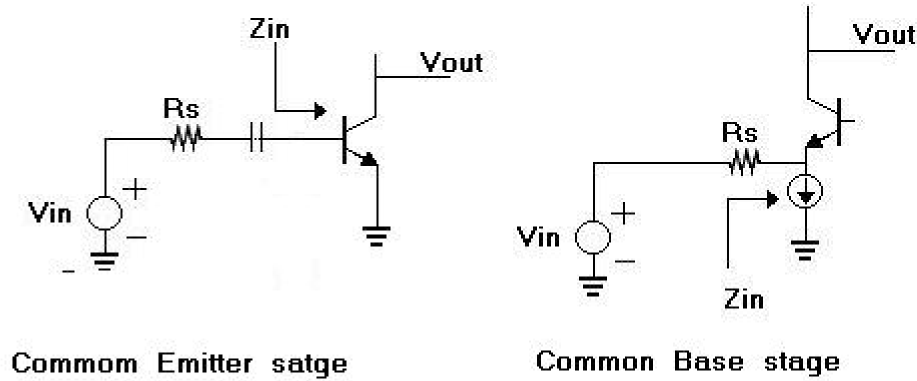


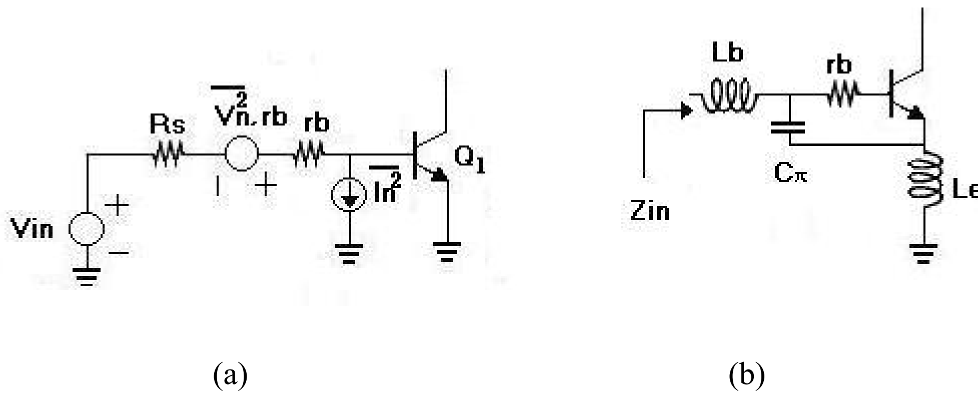
Figure 3.1.1 The architectures of LNA

In a common-base circuit, the source resistance, Rs, linearizes the input-output characteristic by smoothing down the excursions from emitter current. This effect results the source resistance experience only the base current variations. To exhibit an input resistance Rs = $(g_m + g_{mb})^{-1}$ = 50 Ω, the transconductance of the input transistor cannot be arbitrarily high (g_m simulation about 30 $\frac{1}{\Omega}$ in this process), thus imposing a lower bound on the noise figure and the input capacitance may be canceled by means of an external inductor. This topology exhibits a high reverse isolation if the bias is properly bypassed, but the primary drawback is relatively high noise figure.

The common-emitter stage with the inductive degeneration is the most prevalent method used for low noise amplifier .Since the input-referred noise voltage per unit bandwidth (noise modeling is shown in Fig 3.1.2(a)) is given by

$$\overline{V_n^2} = 4kT(r_b + \frac{1}{g_m}) = 4kT(r_b + \frac{V_T}{2I_C}) \qquad (3.1.)$$

where Ic is the collector current. To lower the noise, Q_1 must be relatively large and biased at a high current. However, large device size leads to higher input capacitance. Larger collector-base and collector-substrate capacitance lowers the voltage gain, and increasing the bias current results in base shot noise. For the overall reason, the noise figure reaches a minimum for a particular choice of the size and bias current.



(a) (b)

Fig 3.1.2 (a) Noise modeling of BJT (b) Impedance matching network

We add the base shot noise as a current source to (3.1)

$$\overline{I_n^2} = 4kT\frac{I_c/\beta}{2V_T} \tag{3.2}$$

So, for a source resistance of Rs**,** the total input-refereed noise voltage is given by

$$\overline{V_{total}^2} = 4kT(R_s + r_b + \frac{1}{g_m} + \frac{g_m R_s^2}{2\beta}) \tag{3.3}$$

The noise figure is therefore equal to

$$NF = \frac{V_{total}^2}{4kTR_s} = 1 + \frac{r_b}{Rs} + \frac{1}{2g_m R_s} + \frac{g_m R_s}{2\beta} \tag{3.4}$$

Rs is a independent variable, the

$$R_{s,opt} = \sqrt{\frac{\beta(1+2g_m r_b)}{g_m}} \tag{3.5}$$

The noise figure reaches a minimum of NF_{min}

$$NF_{min} = 1 + \sqrt{\frac{(1+2g_m r_b)}{\beta}} \tag{3.6}$$

This equation does not take the effect of parasitic capacitance in account and a reasonable high-frequency is simplifying β at the operating frequency. The accurate NF must obtain from simulation.

$$|\beta| \approx \frac{f_T}{f} \tag{3.7}$$

Therefore, the rough value of g_m, r_b and f_T could be given in model files when the power consumption is asked, we can get a optimum value of Rs. It has been found out that NF_{mim} is a weak function of device size but primarily a function of the bias current density. [17] The small noise figure can be found more easily through the above expression but the impedance matching condition must be taken into account.

To null the input capacitance and achieve the input matching, a prevalent series-connect two-element matching network is adopted in LNA design. It consists of base and emitter degeneration inductors L_b and L_e, respectively. Inductor L_e plays two roles in the circuits; it both allows the conjugate matching and linearizes the circuit. Neglecting the effect of C_μ and r_π, the input impedance is as

$$Z_{in}(real) \cong r_b + R_{Lb} + R_{Le} + \frac{g_m}{C_\pi} Le \tag{3.8}$$

$$Z_{in}(imageinary) \cong sLb + sLe + \frac{1}{sC_\pi} \tag{3.9}$$

where R_{Lb} and R_{Le} are the parasitic series resistors of Lb and Le, respectively. C_π is the base-emitter capacitor of NPN device. To achieve the matching condition of 50-Ohm input resistance, the value of components must set as follow:

$$R_s \cong r_b + R_{Lb} + R_{Le} + \frac{g_m}{C_\pi} Le \tag{3.10}$$

$$\omega^2 C_\pi (Lb + Le) = 1 \tag{3.11}$$

where ω is the center frequency in radians/s. Le is used to match the real part of source impedance, while Lb is used to cancel the reactance duo to the capacitance of input port.

3.1.2 Design of Common-Source with Inductive Degeneration LNA

The on-chip spiral inductors are realizing to achieve 50-Ohm input and output matching. The transistors are bilateral devices, through collector-base junction

capacitor C_μ, which couples the two ports of base and collector. Therefore, a signal stage amplifier must face the severe effect of input and output port coupling. As a consequence, we use cascode topology in this work to avoid the signal coupling, there by favoring higher isolation and solving the problem of Miller effect (shown in Fig 3.1.3).

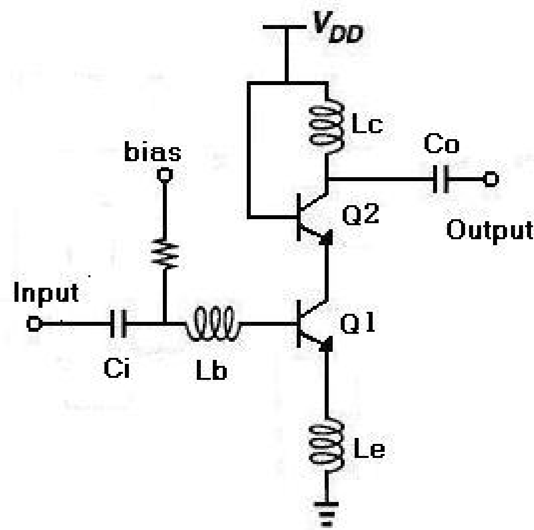


Fig 3.1.3 The schematic of cascode LNA with degeneration inductor

We utility the above-mentioned method to decide the components and devices size, and the ratio of Lc and Le determines the voltage gain of amplifier, in order to obtain maximum power gain, the values of Lc and Co must be select to match up at operating frequency. Because the output matches to 50 Ohm system, the voltage gain and the power gain is the same in this work. Because no suitable inductor model is offered, the emitter inductor Le is replaced by a transmission line; width and length decided by simulator, IE3D.

Pad effects of RF port are critical. Since this LNA is designed for on-wafer measurement, layout is set in uni-directional mode. The RF input and the RF output are placed on opposite sides of the layout to avoid the high frequency signals coupling, and GSG (Ground – Signal – Ground) pad structures are used in both RF input

and output ports. A low resistance material, metal-1 layers, is placed between P-substrate and RF signals layer (metal-3), and the other space was filled by oxide to minimize the effect of inducing noise and extra substrate loss, which from the parasitic resistance between the metal plate and substrate. To reduce parasitic capacitor, the metal-3 (top metal layer of this process) is used as signal pad. A shielded signal GSG pad structure is shown in figure3.1.4, to shield the undesired effects cause by the noisy substrate. [18]

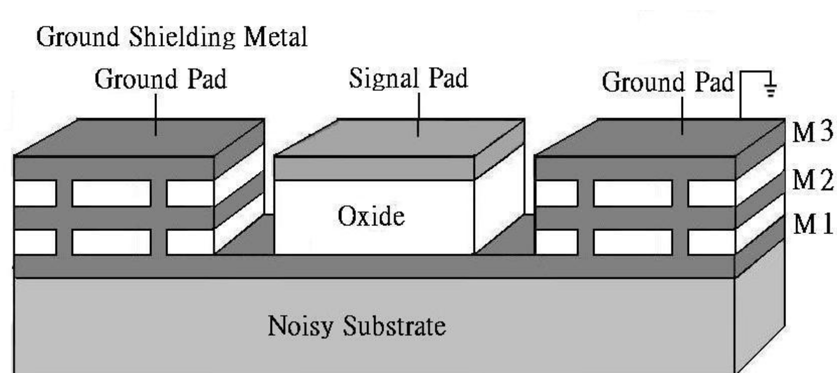


Fig 3.1.4 GSG pad structure

3.2 Measurement Consideration

This LNA circuit is designed for on-wafer testing; the layout allocation must fit the requirement of the NDL's probe station testing rule. This work uses 6-pin DC card and two GSG probes and measurement instrument is shown in Fig3.2.1

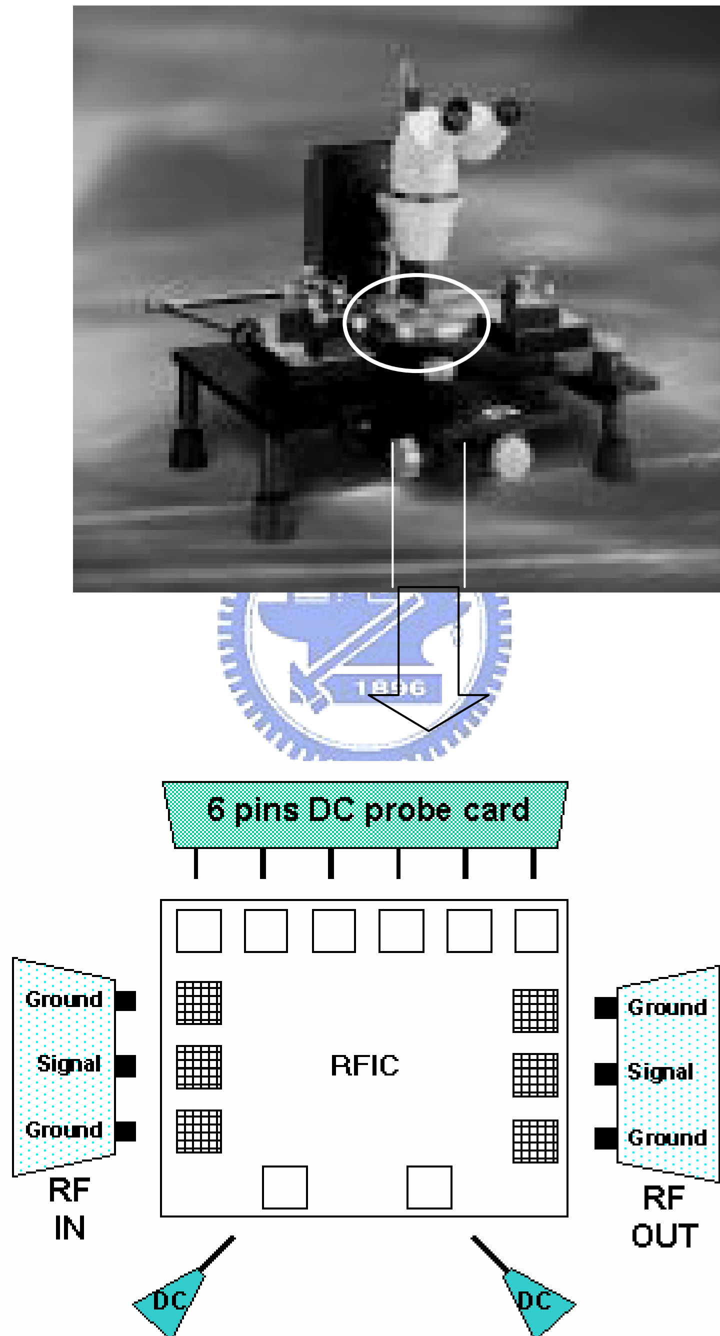
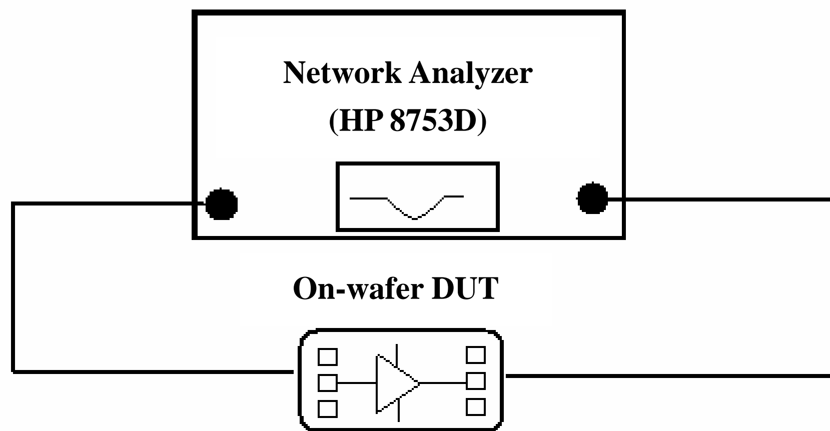
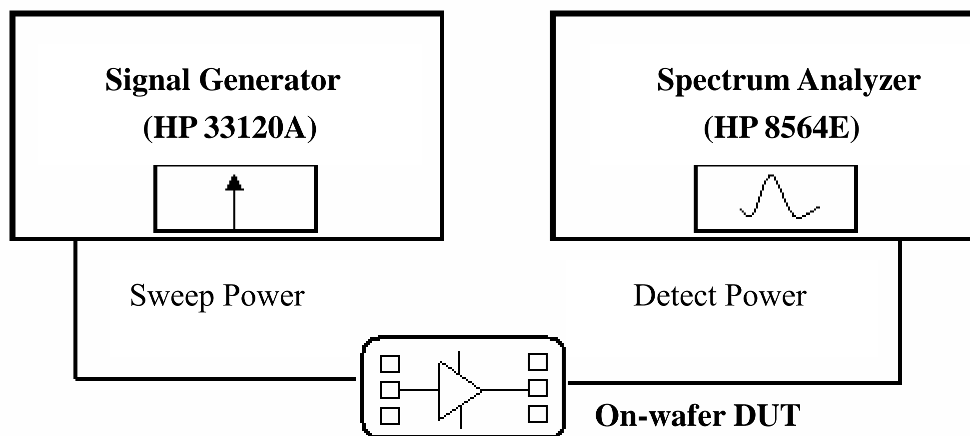


Fig 3.2.1 On wafer measurement instrument;

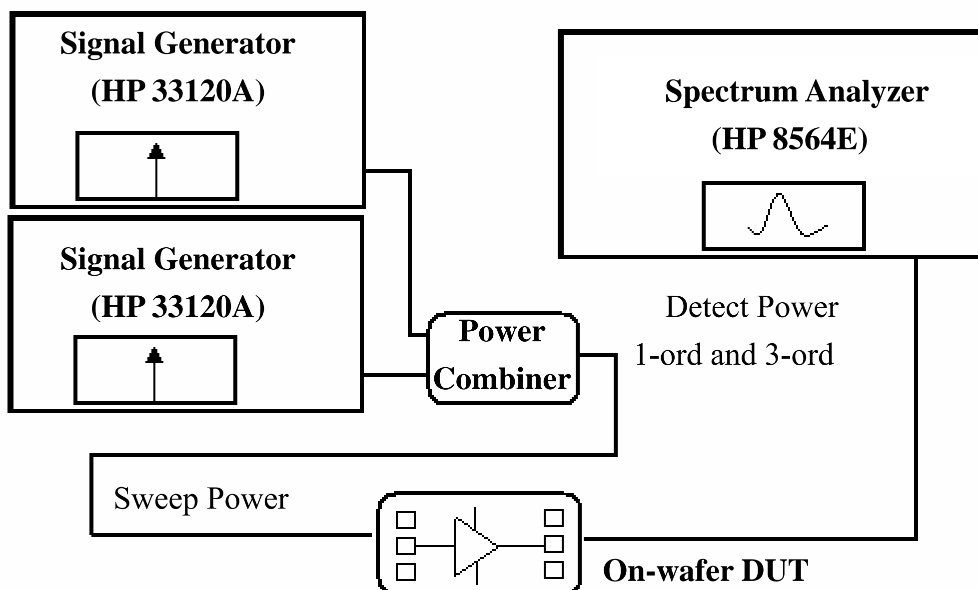
probe station and on-wafer GSG testing layout



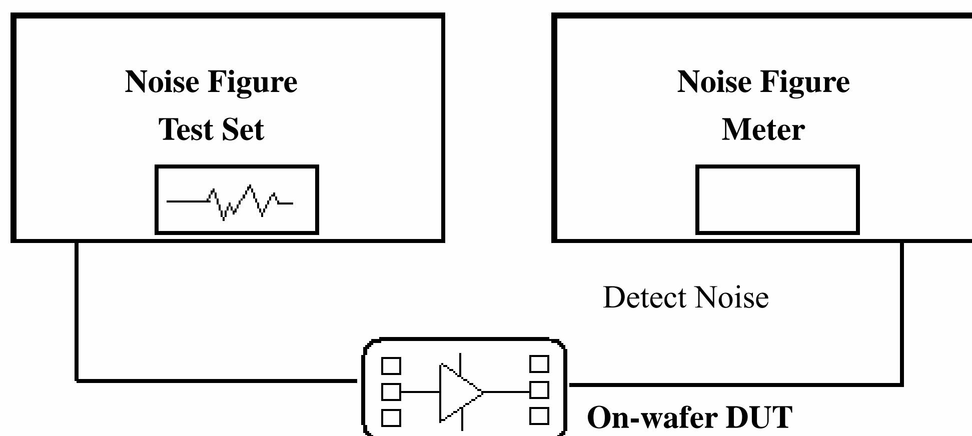
(a)



(b)



(c)



(d)

Fig 3.2.2 The testing setup of (a) S-parameters (b) Output Power

(c) Two-tone test (d) Noise Figure

Each measurement setup is shown in figure 3.2.2. They are high frequency S-parameter, output power, noise figure and linearity two-tone testing. We use RFIC measurement system in NDL to complete. This circuit is designed a front-end in 50Ω system for the measurement system. All of the matching devices are on-chip components and then we can easily integrate the other front-end circuit such as mixer and synthesizer in future work. We will discuss the experimental and testing results of this circuit in following sections.

3.3 Simulation and Measurement results comparison

Fig3.3.1 shows illustrated the simulation and measurement results of S-parameter (S11).

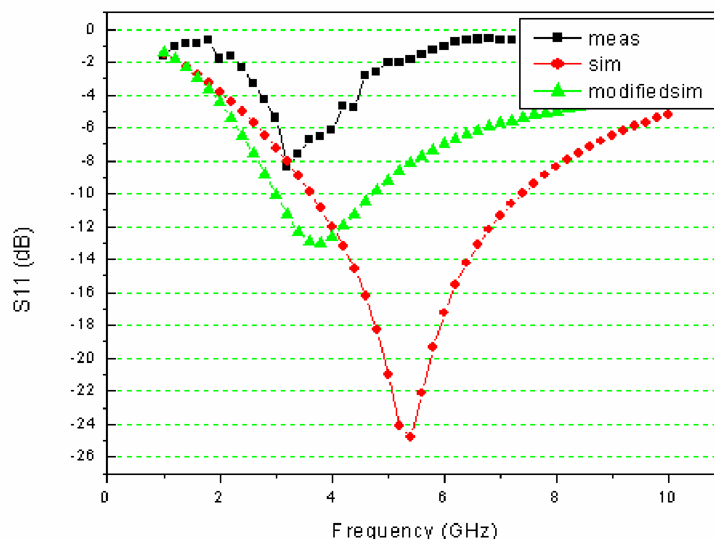


Fig3.3.1 Comparison between simulation and measurement of S11

We could observe the measurement results in the foregoing illustrates. The central frequency shifts from 5.2GHz to 3.2GHz obviously. The simulation and experimental results are different. To find out the critical problem, we redo the simulation to fit the measurement results. Adding the modified simulation results in above-mentioned figure is for comparison easily. Since the sub-circuit component models are physical, the corner models are determined directly from process variation. In on-wafer testing, we find that the DC current of this chip is smaller than the simulation results; this condition is meaning process approach to SS corner model and the data of process variation (W.A.T data attached) is also shown the same results. To realize the influence of the process variation, the re-simulation is done and shown in above. The size of active devices, NPN transistor, is not change, but the SS corner model is adopted to redo the simulation. We use the variation range of ±10% to simulate the value variation of passive components. Furthermore, the metal lines to

substrate parasitic capacitances can not ignore in practical IC. Although through the layout parasitic extraction (LPE), we still can not predict the hundred percent parasitic effects when the high frequency operation.

The follow pictures are s-parameter of S21 and S22, matching peak point is shift to about 3.2GHz in measurement condition and 3-4GHz in re-simulation results. This simulation could verify that the parasitic capacitances of active device in practical IC is large the simulation modeling, from the input matching equations (3.10) to ((3.11)

$$R_s \cong r_b + R_{Lb} + R_{Le} + \frac{g_m}{C_\pi} Le \tag{3.10}$$

$$\omega^2 C_\pi (Lb + Le) = 1 \tag{3.11}$$

we find if the value of Cπ is increasing , the operating frequency ω is required to decreasing to satisfy the equation (3.11) . And in equation (3.10), if Cπ is larger than the expected value, the input resistance of this circuit is lower than anticipated value, 50 Ω. These are possible reasons that cause the port 1 matching shifting. The port 2 matching is sensitive to capacitance in this kind of LNA architecture, the gain (S21) maximum point variation would be related with the minimum S22 point shift. The output DC de-coupling MIM capacitor and other parasitic capacitance are significant reason of variations.

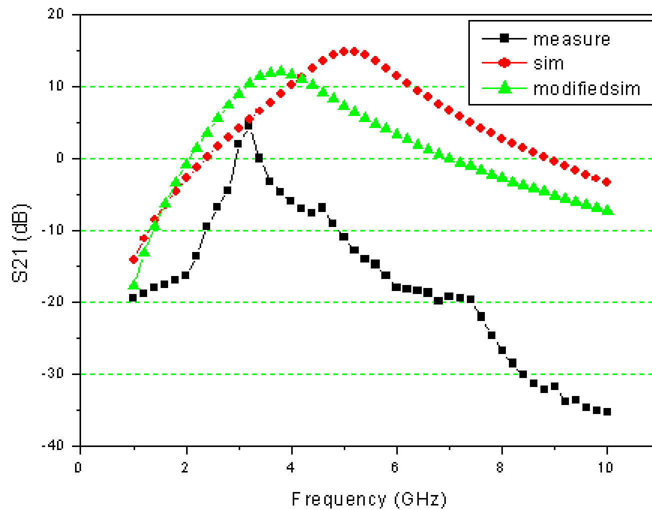


Fig3.3.2 Comparison between simulation and measurement of S21

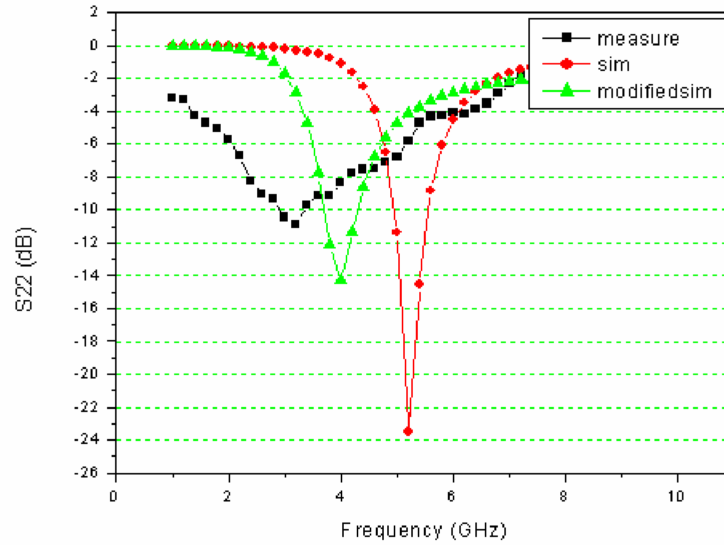


Fig3.3.3 Comparison between simulation and measurement of S22

The power parameters and two-tone test are showing in figure 3.3.4 and figure3.3.5, respectively. Input signal of simulation results is at 5.2GHz and the 1dB compression points (P1dB) and input third intercept point (IIP3) are testing in 3.2GHz frequency band. The input power of modified simulation results are setup at 3.2GHz.

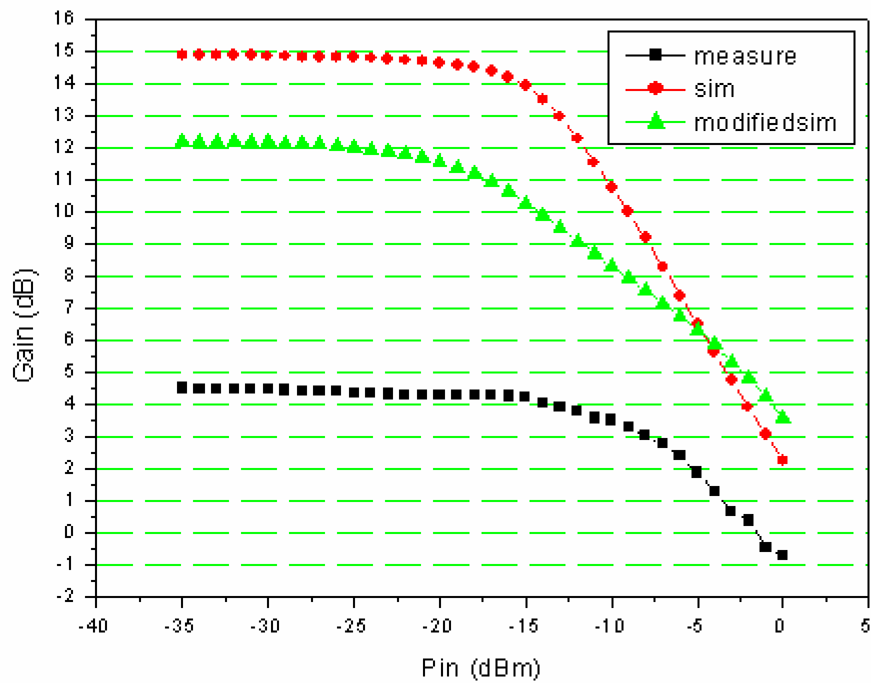


Fig 3.3.4 Comparison between simulation and measurement of gain

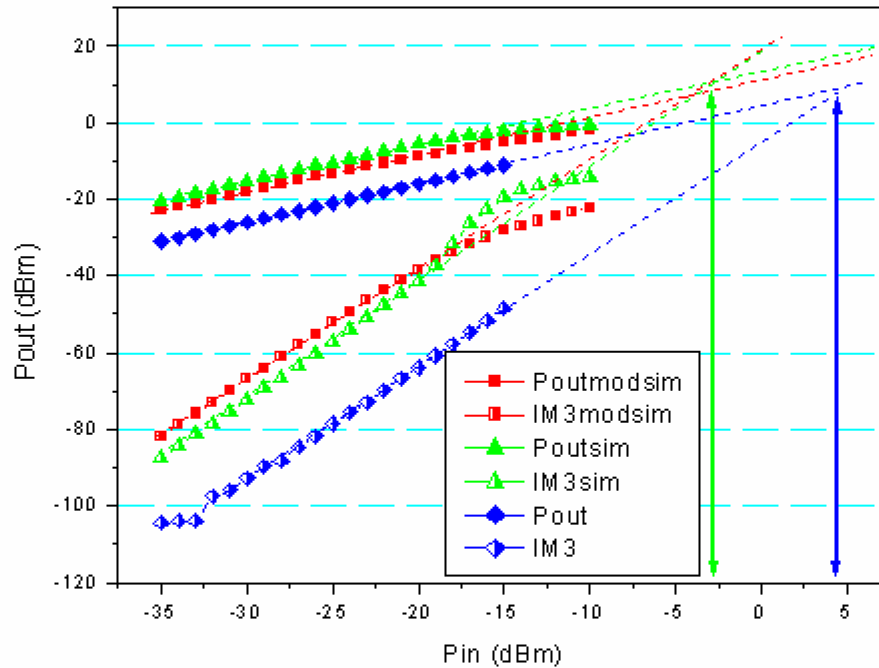


Fig 3.3.5 Comparison between simulation and measurement of two-tone test

The experimental 1dB point and IIP3 are greater than the simulation. The trade-off between power gain and the linearity under fixed biasing condition is the criterion for LNA design. Because the gain of measurement is lower than the expected, the performance of linearity is greater than expected one. The experimental maximum gain point shifts to 3.2GHz, the two-tone testing and output power testing are selected at 3.2GHz to measure the performance.

And Figure 3.3.6 is noise figure results. The noise figure is testing cover the 3GHz to 6GHz. The noise figure is not as good as the simulation. We have to first know there is no accurate model for our simulation, therefore, there could be many noise sources from the inside outside the chip and we do not know clearly. And the performance of s-parameter is shifting from the design operating frequency, optimization noise figure point also shifts. From the re-simulation, we know under this situation that the noise figure would rise to 7.5dB. The measurement result is 9.3dB at 3.2GHz. The process variation is important reason to lead the unexpected performance of this LNA.

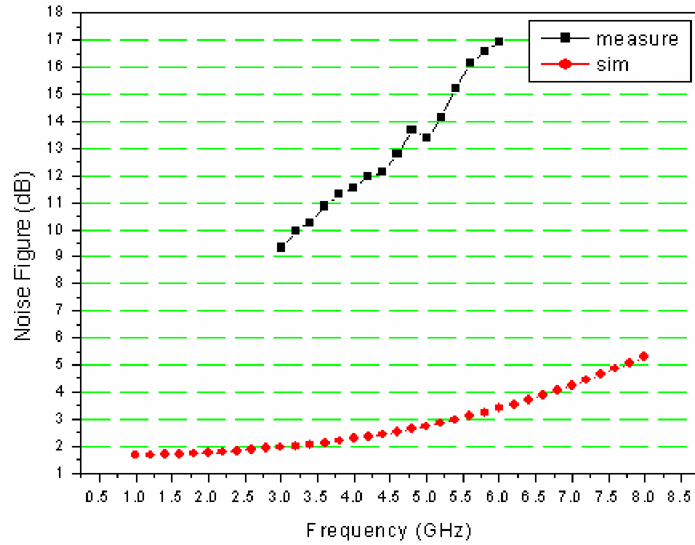


Fig 3.3.6 Comparison between simulation and measurement of noise figure

The Table3.3.1 is the summary performance result of this SiGe LNA.

Specification	Simulation		Measurement	
	5.2GHz	3.6GHz	5.2GHz	3.2GHz
Noise Figure (dB)	2.86	7.45	14.1	9.3
S21 (dB)	14.87	12.0	-12.8	4.6
S11 (dB)	-24.14	-12.9	-2.0	-8.3
S22 (dB)	-23.52	-7.8	5.8	-10.9
S12 (dB)	-40.7	-42.8	-22	-17
Pin-1dB (dBm)	-15.3	-17.8	N/A	-6.5
IIP3 (dBm)	-3.2	-5.3	N/A	3
Supply Voltage (v)	2.5	2.5	2.5	2.5
Power consumption (mW)	11.2	6.7	7.5	

Table 3.3.1 Performance summary (Center frequency of measurement shifts to 3.2GHz; we change the corner model to re-simulate the performance.)

REF	[19] 2002	[20] 2003	[21] 2002	[22] 2002	[23] 2002	This work 2003.08	
Frequency (GHz)	5	4.4-5	5.8	5.8	6	5.2	3.2
Power (mW)	31	24	20	16	13	11	7.5
NF (dB)	1.7	2.2	3.2	4.4	2.3	2.9	9.3
Gain (dB)	18.3	14.1	7.2	11	17	14.9	4.6
S11 (dB)	-25	-13.8	-11	-20	---	-24.1	-8.3
S22 (dB)	-27.3	-8.5	-17	-12	---	-23.5	-10.9
IIP3 (dBm)	-4.0	-6.2	6.7	-2	-7	-3.2	3
P_{1dBin} (dBm)	-12.3	11.6	-3.7	-10.4	-18	-15.3	-6.5
Process	SiGe 0.5um	SiGe 0.25um	CMOS 0.35um	SiGe 0.35um	SiGe 0.35um	SiGe 0.35um	SiGe 0.35um
Condition	Sim.	Sim.	Meas.	Meas.	Meas.	Sim.	Meas.

Table 3.3.2 Comparison of recently LNA paper

Table3.3.2 shows the comparison of this work and recently LNA paper. Because the difference between measurement and simulation results; both data are showed. According to the simulation parameter, power dissipation of this work circuit is less than all other circuits; the linearity is lower than others. We must base on accurate circuits models and careful simulation to make the measurement closed to the simulation in future work.

The layout and test plan are shown as figure 3.3.7. We endeavor to shorten the RF signal path and consider the current distribution to decide the top metal (metal-3) width for DC current path. The SiGe LNA chip area is 900-μm x 900-μm. The die photo is shown in Fig3.3.8.

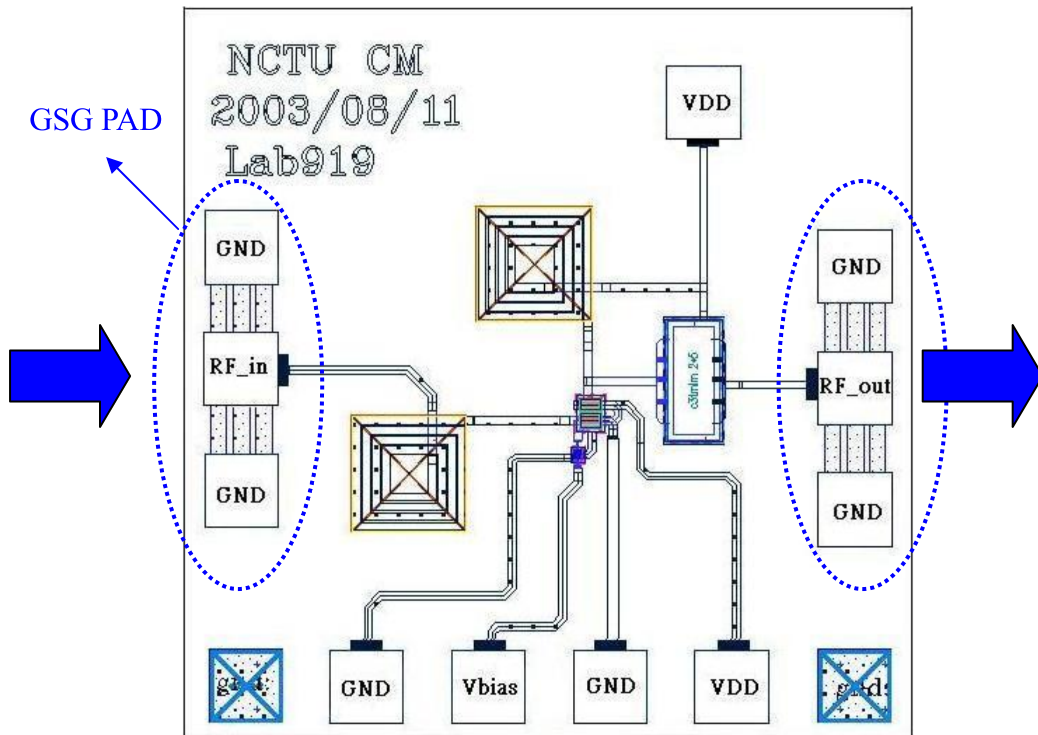


Fig 3.3.7 The layout and test plan of LNA

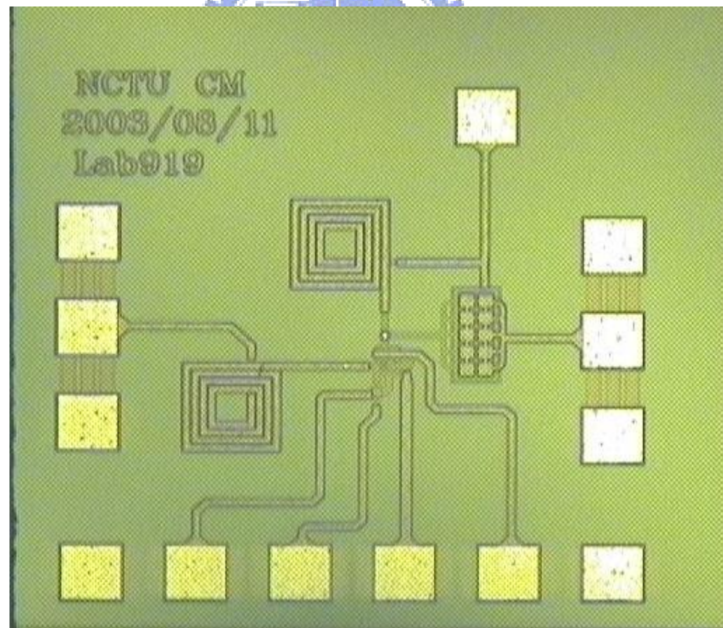


Fig 3.3.8 The die photo of LNA

Chapter 4

A 0.35-µm SiGe 5GHz Concurrent LNA And Mixer Design and Implementation

4.1 Architecture and Design Concept of Concurrent LNA and Mixer

4.1.1 Architecture of Mixer

Mixers perform frequency translation by multiplying two signals. Downconversion mixer employed in receive path have two distinctly different inputs; RF port and LO port. The RF port senses the signal to be downconverted and the LO port senses the periodic waveform generated by the local oscillator. When a device (a diode, a MOS and a BJT) is in operating region, it could perform to multiply the signals. The characteristic curve of current versus voltage in operating region is as follow

Diode,

$$i_D = I_S (e^{\frac{v_D}{\eta V_t}} - 1) \tag{4.1}$$

MOS,

$$i_{DS} = \frac{1}{2}\mu_n c_{ox} (\frac{W}{L})(v_{GS} - v_t)^2 \tag{4.2}$$

BJT,

$$i_C = I_S e^{\frac{v_{BE}}{V_t}} \tag{4.3}$$

we take the BJT for example, the power series representation of characteristic curve is

$$i_C = I_S e^{\frac{v_{BE}}{V_t}} = I_S e^{\frac{V_{BE}}{V_t}} e^{\frac{v_{be}}{V_t}} = I_S e^{\frac{V_{BE}}{V_t}} (1 + \frac{v_{be}}{V_t} + \frac{(\frac{v_{be}}{V_t})^2}{2} + \frac{(\frac{v_{be}}{V_t})^3}{6} + \cdots) \tag{4.4}$$

where $i_C = I_C + i_c$; $v_{BE} = V_{BE} + v_{be}$; $I_C = I_S e^{\frac{V_{BE}}{V_t}}$

the term, $v_{be}{}^2$, could mix desired signal, if we set $v_{be} = \cos\omega_{rf}t + \cos\omega_{lo}t$

then $v_{be}{}^2$

$$= \cos^2\omega_{rf}t + 2\cos\omega_{rf}t \cdot \cos\omega_{lo}t + \cos^2\omega_{lo}t$$

$$= \frac{1+\cos 2\omega_{rf}t}{2} + \frac{1+\cos 2\omega_{lo}t}{2} + (\cos(w_{rf} - \omega_{lo}) + \cos(\omega_{rf} + \omega_{lo}))$$

the $\cos 2\omega_{rf}t$, $\cos 2w_{lo}t$ and $\cos(\omega_{rf} + \omega_{lo})$ can be filter out for down conversion by LPF and $\cos(\omega_{rf} - \omega_{lo})$ is desired signal.

The most popular mixer circuits for RF are mixers based on ideal multipliers and mixers based on switching. [24]

The switching performs a multiplication between the RF signal and local oscillator signal ideally represented by a square wave switching between +1 and -1. The output spectrum contain not only the desired difference frequency term but also components corresponding to all odd harmonics of the local oscillator signal, that is at offsets found at the Fourier decomposition of the square wave. Provided a perfectly balanced design and perfectly symmetric local oscillator signal is used, the mixer does not generate even order components or a DC component. A switching simple and switching mixer circuit is illustrated as follow. In terms of implementation in CMOS switching mixer has the advantage that CMOS transistor is a fairly close approximation to an ideal switch.

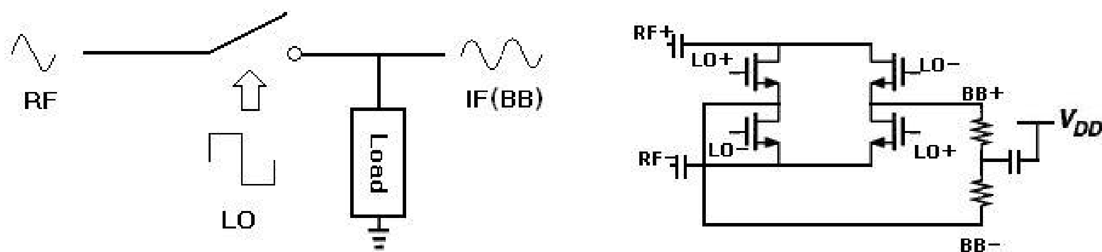


Fig 4.1.1 A switching simple and switching mixer circuit

$$V_{IF} = V_{RF}\cos(\omega_{RF}t)\cdot\delta_{LO}$$

where δ_{LO} = Fourier series of a square wave, with amplitude A= $\frac{\pi}{2}$

$$= \cos(\omega_{LO}t) + \frac{1}{3}\cos(3\omega_{LO}t) + \text{ higher odd harmonics}$$

since

$$\cos A\cdot\cos B = \frac{1}{2}\left[\cos(A+B)+\cos(A-B)\right] \quad (4.5)$$

The output terms contain frequencies such as $\omega_{RF}-\omega_{LO}$, $\omega_{RF}+\omega_{LO}$, $3\omega_{LO}-\omega_{RF}$, $3\omega_{LO}+\omega_{RF}$, and we could get the desired IF frequency, $\omega_{RF}-\omega_{LO}$.

The multiplying mixer directly implements a multiplication between the RF signal and the local oscillator signal, both represented by sine wave, i.e. the function

$$\cos(\omega_{RF}t)\cos(\omega_{LO}t) = \frac{1}{2}\left[\cos(\omega_{RF}t+\omega_{LO}t)+\cos(\omega_{RF}t-\omega_{LO}t)\right] \quad (4.6)$$

thus, ideally the output spectrum from the mixer contains only the desired difference frequency and the sum frequency which is easily filtered out. With bipolar transistors the multiplier is easily implemented using a Gilbert cell for the multiplier [25]. In CMOS the Gilbert cell has to be modified in order to cancel the quadratic terms originating from the basic MOS device equations. [24]

Shown in Fig 4.1.2 is the commonly used bipolar Gilbert mixer. Transistors Q1-Q2 forms the input transconductors, which convert input RF voltage signal into current signal. Transistors Q3-Q6 is commutating switches, which are turned on and off by the local oscillator signal, accordingly, current signals from the transconductors are delivered to different branches. The net effect of the switching activities is that the RF current signals are multiplied with the local oscillator signal. In practice, the switching voltage at transistor bases are not ideal square waves but it can be shown that even rather large rise and fall times of the switching waveforms. [25]The resistors serve as loads. The differential IF output signal is gotten from these two loads.

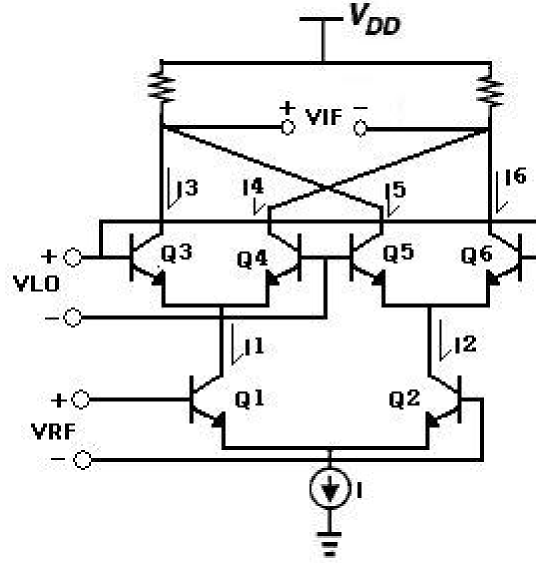


Fig 4.1.2 The Gilbert cell

The bipolar Gilbert mixer operates with both differential LO and RF inputs, then it is called" double balanced," this topology perform a multiplication and output is the desired frequency.

$$I_1 = I_S e^{\frac{VRF}{V_T}} \quad , \quad I_2 = I_S e^{\frac{-VRF}{V_T}} \tag{4.7}$$

$$I_1 + I_2 = I \tag{4.8}$$

use equation (4.7) and (4.8), we got

$$I_1 = I \frac{e^{\frac{VRF}{V_T}}}{e^{\frac{VRF}{V_T}} + e^{\frac{-VRF}{V_T}}} \quad , \quad I_2 = I \frac{e^{\frac{-VRF}{V_T}}}{e^{\frac{VRF}{V_T}} + e^{\frac{-VRF}{V_T}}} \tag{4.9}$$

$$I_2 - I_1 = I \frac{e^{\frac{VRF}{V_T}} - e^{\frac{-VRF}{V_T}}}{e^{\frac{VRF}{V_T}} + e^{\frac{-VRF}{V_T}}} = I \tanh(\frac{VRF}{V_T}) \tag{4.10}$$

then using the results of equation (4.10), VIF as follow

$$VIF = R[(I_3 + I_5) - (I_4 + I_6)] = R[(I_3 - I_4) - (I_6 - I_5)]$$

$$= R\left[I_1 \tanh(\frac{VLO}{V_T}) - I_2 \tanh(\frac{VLO}{V_T}) \right] = R(I_1 - I_2) \tanh(\frac{VLO}{V_T})$$

$$= RI \tanh(\frac{VRF}{V_T}) \tanh(\frac{VLO}{V_T}) \tag{4.11}$$

The multiplying Gilbert cell mixer directly implements a multiplication between current signals of the RF and the local oscillator. This mixer is double balance, any common mode high frequency signals from the LO and RF ports will be reduced at the output. The mixer is expected to have very good RF-to-IF and LO-to-IF isolation performance. In addition, any second order harmonic at the two IF output ports are canceled by the differential output. Note that such quality greatly depends on the switching behavior and transistors working region.

4.1.2 LNA and Mixer Circuits Design

In order to save power, the supply voltage can be lowered but the minimum is dictated by headroom issues in the baseband section and the prescaler in the synthesizer as well as the tuning range required of the VCO. For this reason, the supply is set at suitable value and stacking techniques are employed to reuse the bias currents. [6]

As conceptually illustrated in Fig 4.1.3 (a), the down mixer is stacked on the top of the LNA, with the schematic in Fig4.1.3 (b).

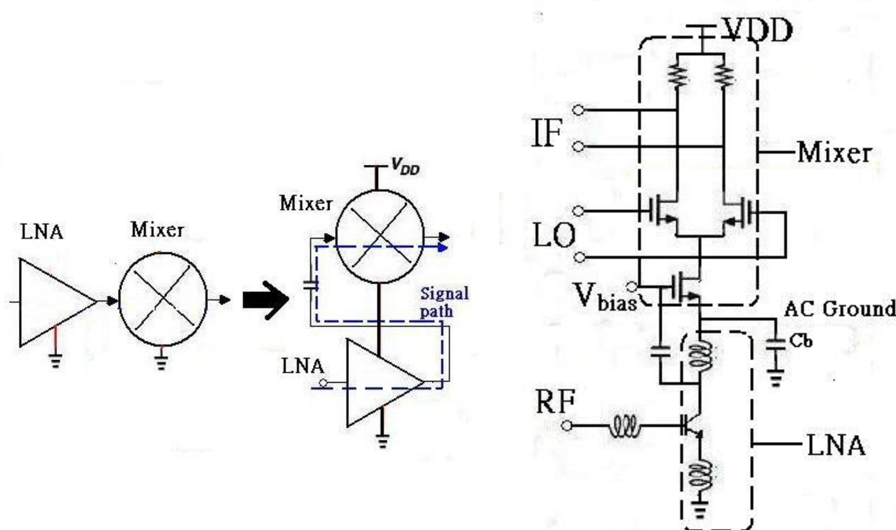


Fig 4.1.3 (a) A conceptually figure of stacking the LNA in the top of the mixer

(b) Transistor implementation

Usually, the differential pair can lower the coupling effect and common-mode noise from a power line, and minimize even-order non-linear effect. A Gilbert cell would a good choice to provide good isolation. To achieve the goal of low-power, high isolation and good stability, the cascode differential structure is shown in Fig4.1.4.

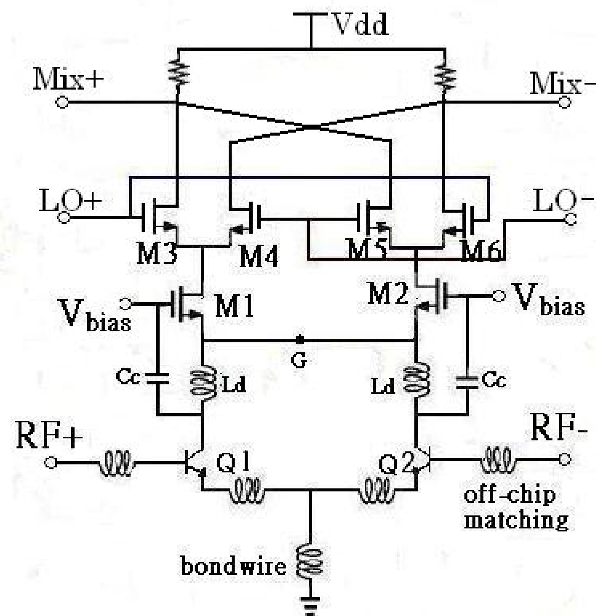


Fig 4.1.4 The schematic of cascode structure

From Fig4.1.4, Q1 and Q2 are signal stage low noise amplifiers which provide the major gain of this circuits, the matching network is composed of two inductors. Because the variation of base inductance would affect the matching performance, the several strips bond wires off-chip inductor is adopted. And the active device is SiGe high speed NPN. The high frequency signal is delivered by coupling capacitor to the gate of M1 and M2 which is the input of mixer. The point G is virtual ground because of the differential circuit structure; the stacked mixer could be operating exactly. The DC current is reused and the RF signal is bypass via capacitors.

The RF and LO signal are 5GHz and 4.99GHz, respectively. LO frequency is lower than the center of desired band is called "low-side injection. " Minimizing the LO frequency facilitate the design of the oscillator. [16] The mixing IF signal is 10MHz. The

M1 and M2 are the main gain stage of the mixer; M3-M6 is switching function which is controlled by the local oscillator power, the passive load is resistor which device size is smaller than an inductor. We add on-chip buffer for testing conveniently. The buffer is illustrated in Fig4.1.5. M7-M9 is current mirror and M10-M11 is common-drain voltage buffer. The output impedance is designed to 50 Ω for instrument. This chip is designed for on board testing; low pass filter or de-coupling capacitor would be used at the output of buffer.

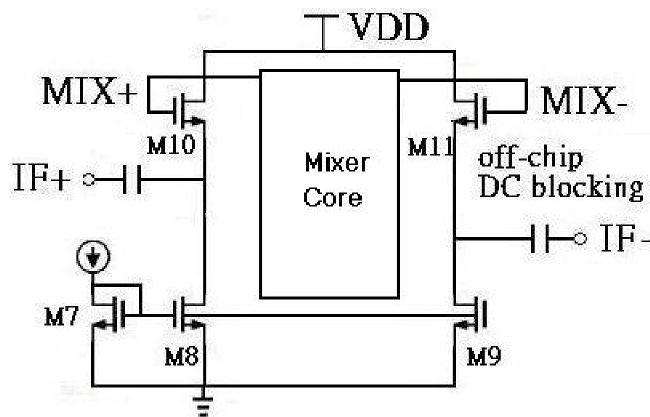


Fig 4.1.5 The schematic of buffer

Because of the on board testing, the input impedance matching is important. For the circuit operating regularly, input power must be delivered into the chip. Fig4.1.6 shows the parasitic effect of the bond-wire, the experience in bond-wire inductance is about 1nH/1mm and the parasitic capacitance is about 200fF to the ground.

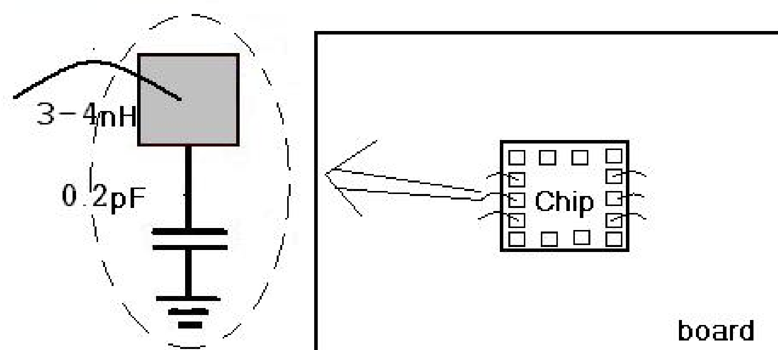
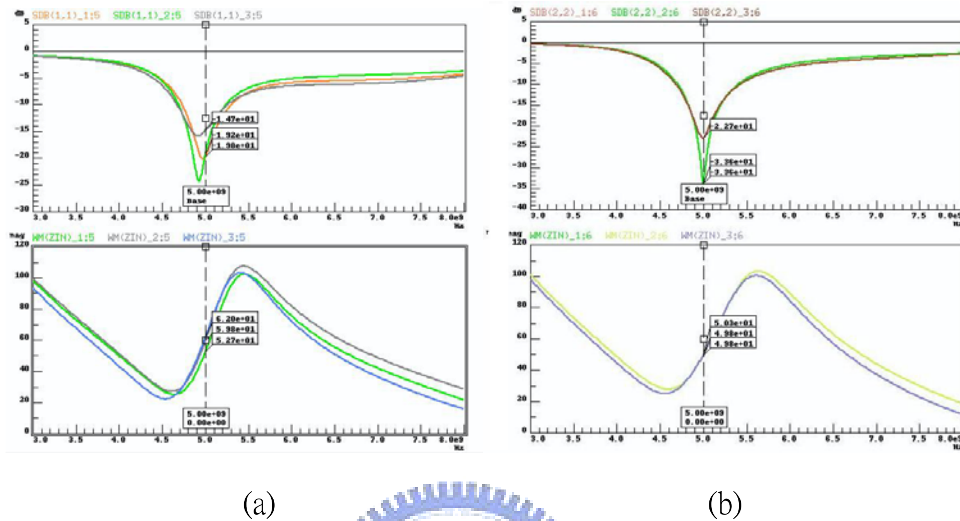


Fig 4.1.6 The parasitic effect of bond-wire

To reduce the variation of RF port and LO port matching network, we add 3 bond wires and 2 bond wires on the RF and LO matching network, respectively. And simulation the variation of a bond-wire length to confirm the result does not affect the matching performance. Fig4.1.7 shows the simulation results.



(a) (b)

Fig4.1.7 Simulation of the bond-wire inductance variation range (3nH, 3.5nH and 4nH), the input return loss are both high than 15dB

(a)RF input port (b) LO input port

The major gain stage is Q1 and Q2; we could decide the device size form a fixed bias condition and trade-off design of the power, linearity, and noise. The Gilbert cell physical size could be determined after the LNA size under the same bias current. Finally, the passive components and matching network would be accomplished. The layout and test plan are shown as figure 4.1.7. The circuit chip area is 1300-μm ＊ 950-μm. The die photo is shown in Fig4.1.8.

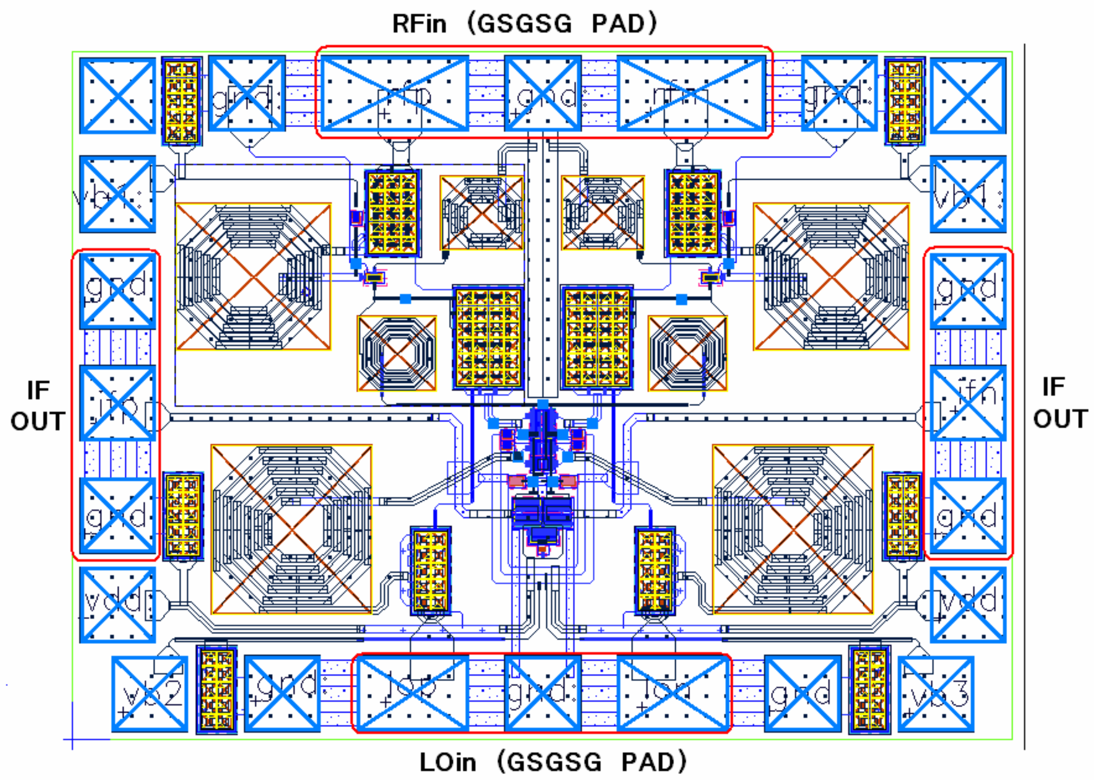


Fig4.1.7 Layout and test plan of this circuit

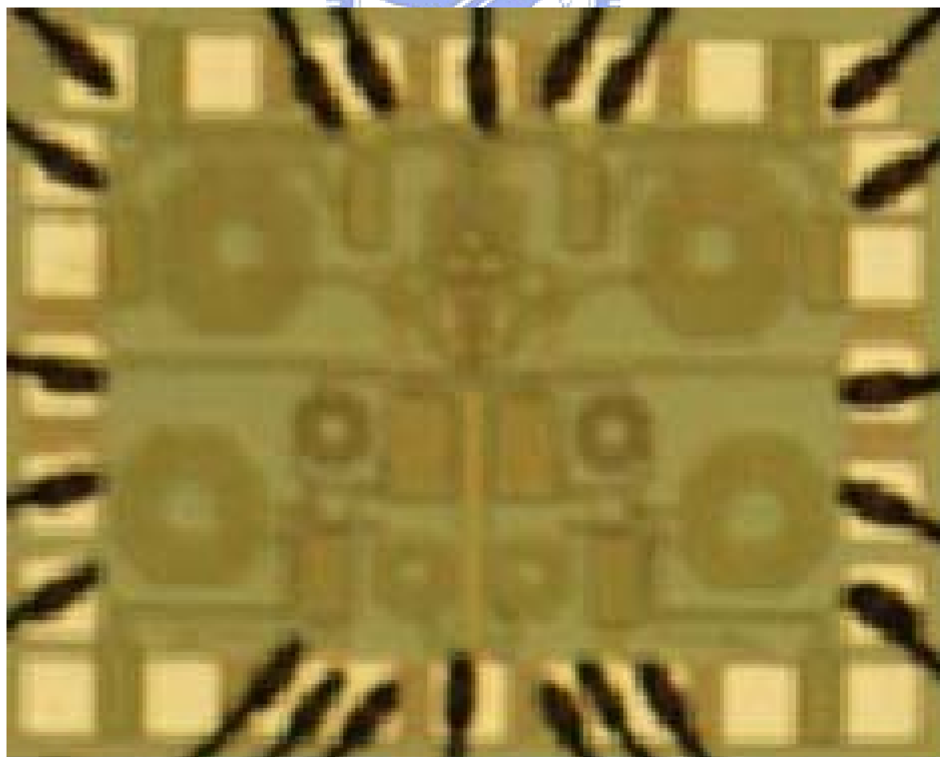


Fig4.1.8 Die photo with bond-wire

4.2 Measurement Consideration

The network analyzer only could execute 2 port measurements. Measurement condition must connect the Balun and transfer two differential ports to one port for differential mixer testing. This chip is bonded wires to microwave circuit board for testing. The Balun blocks split the input power to differential signal and the loss of cable, Balun, SMA connector and board must be taken account. Layout of PCB and reality PCB circuit with SMA connectors are shown as Fig4.2.1 and Fig4.2.2.

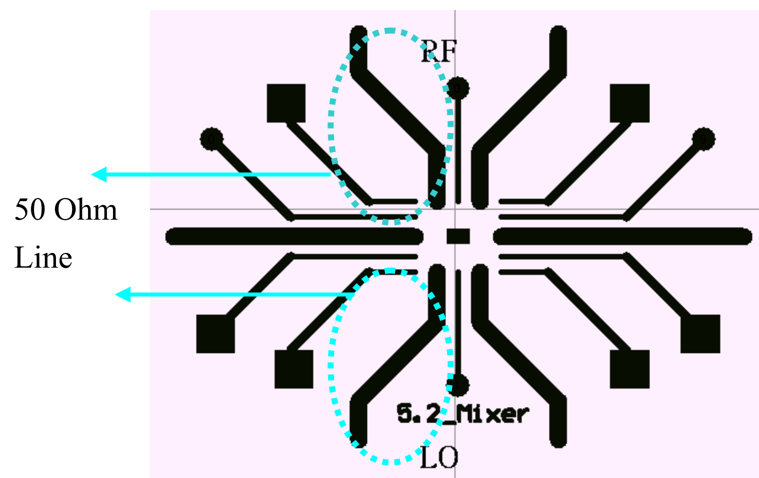


Fig 4.2.1 PCB layout

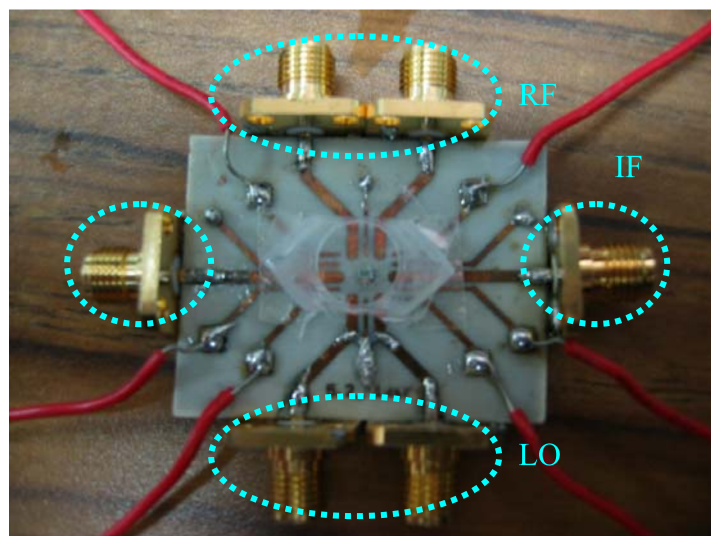
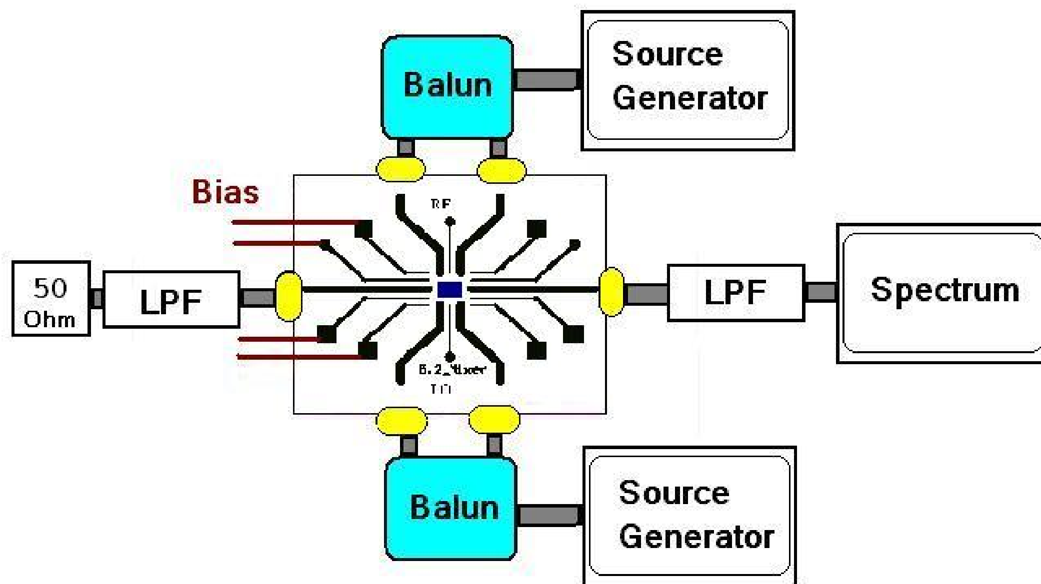
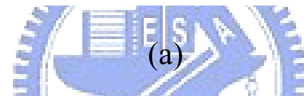


Fig4.2.2 Reality PCB circuit

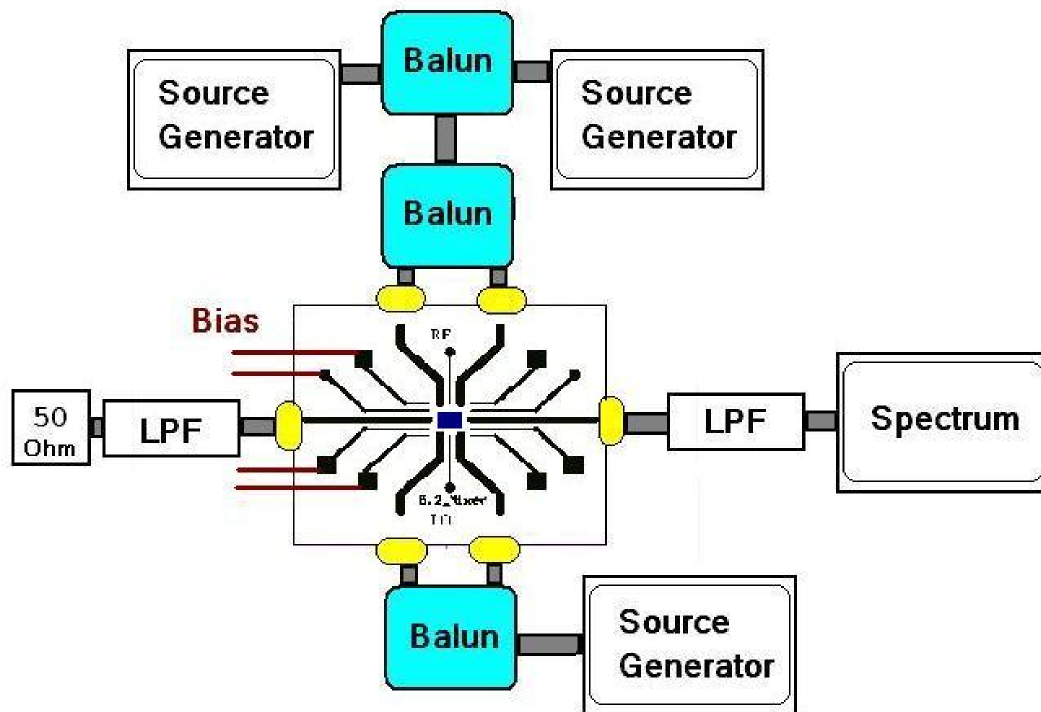
Each measurement setup is shown in figure 4.2.3. They are output power; linearity two-tone testing and high frequency input return loss of RF and LO ports.

We use RFIC measurement system in CIC to complete. The wide band Balun blocking (4GHz-8GHz) is provided by CIC.

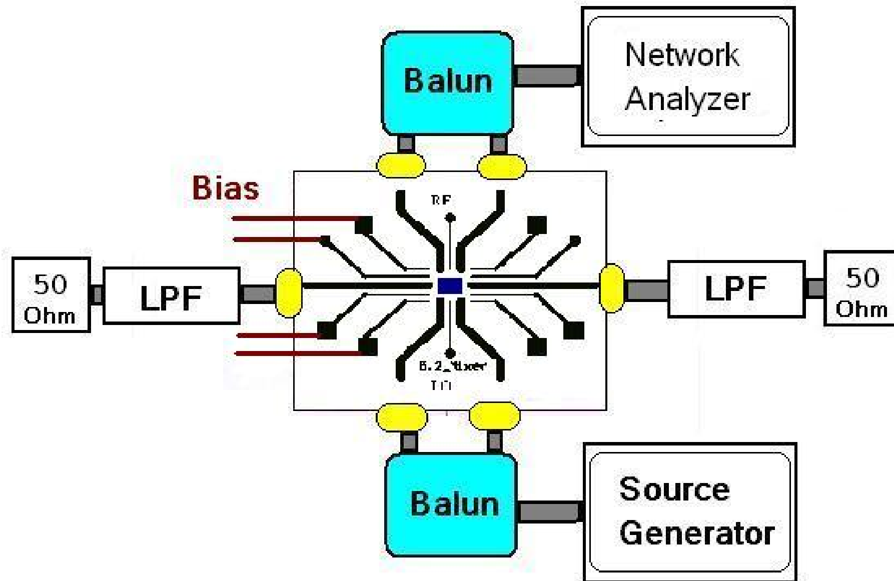




(a)



(b)



(c)

Fig 4.2.3 Measurement setup of (a) Conversion Gain (b) Two-tone IIP3 testing

(c) Input return loss testing

The reality measurement picture is shown in Fig 4.2.4 which include of the mixer, PCB, Balun and cables.

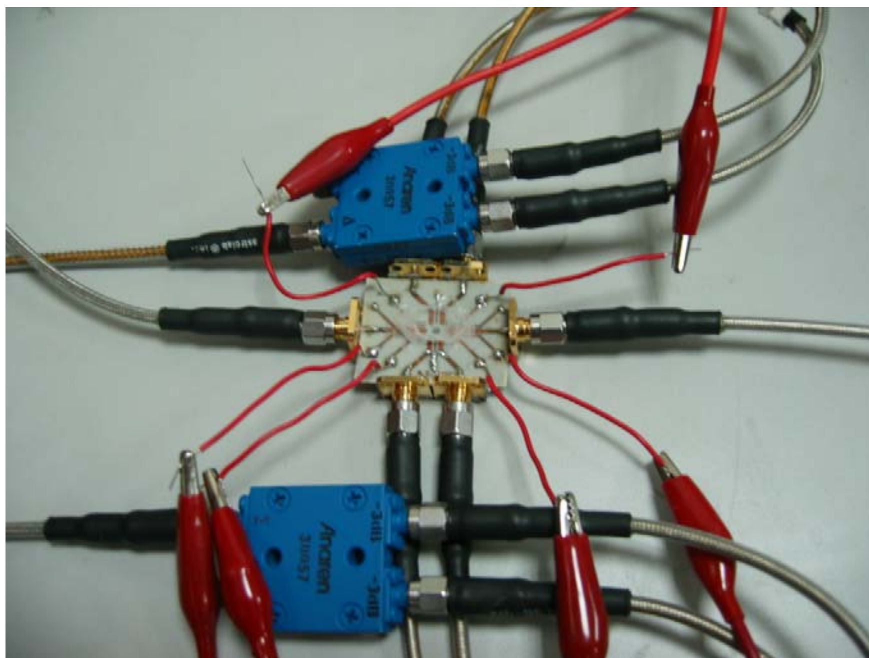


Fig 4.2.4 Measurement picture

To find out the loss of each component, and confirm if the loss would affect the circuit performance, we utilize the 50 Ω line testing board to do the loss testing. The loss of board and SMA connectors are about 0.3dB. The reality picture and measurement result are shown in Fig4.2.5 and Fig 4.2.6, respectively. Furthermore, the cable and Balun loss data could be sum up in CIC RFIC measurement system.

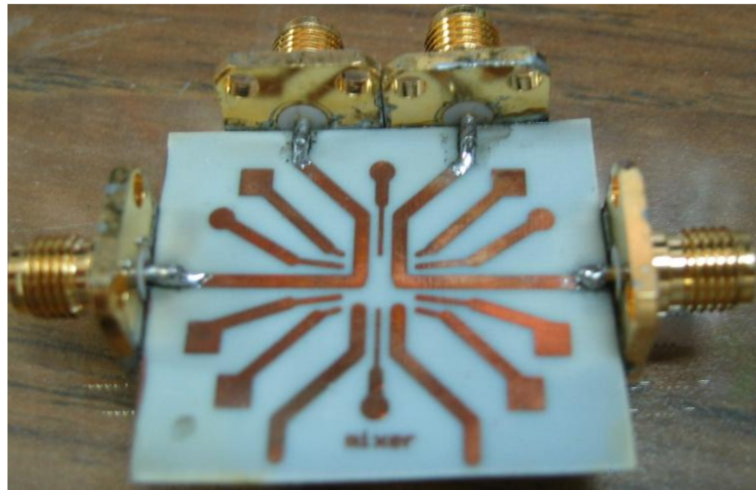


Fig4.2.5 Loss testing board

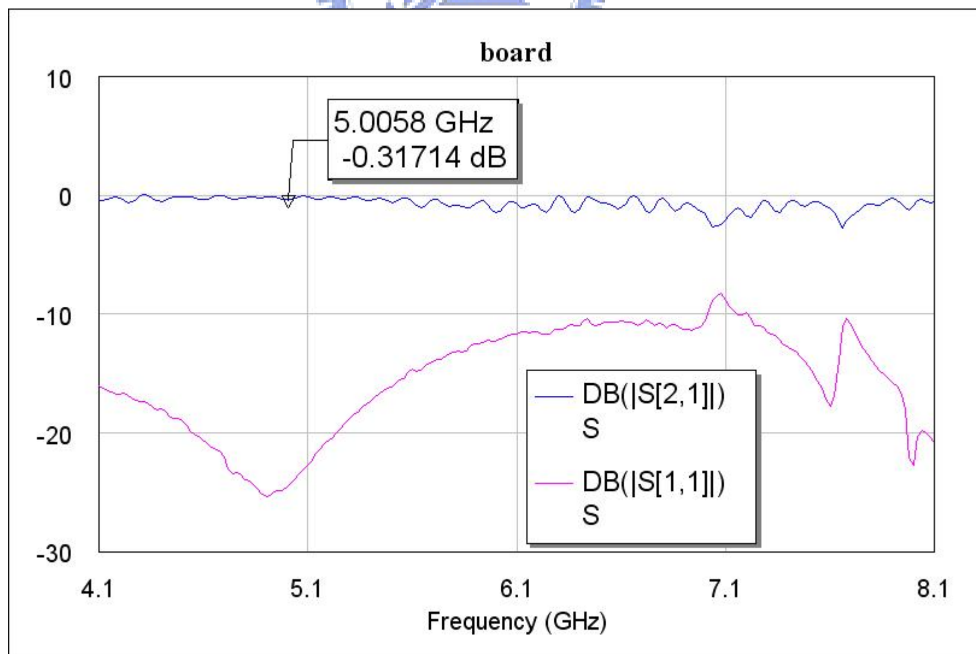
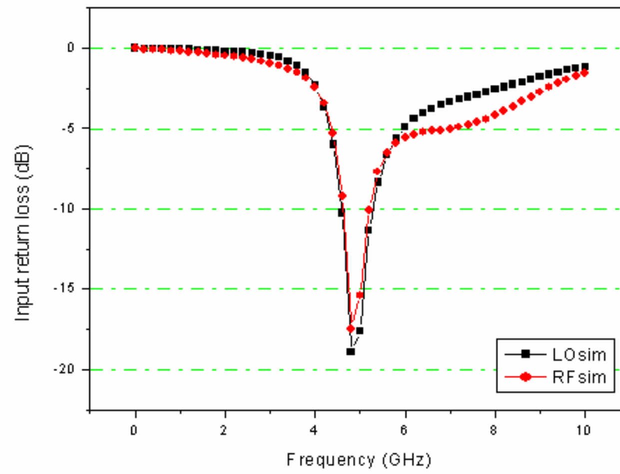


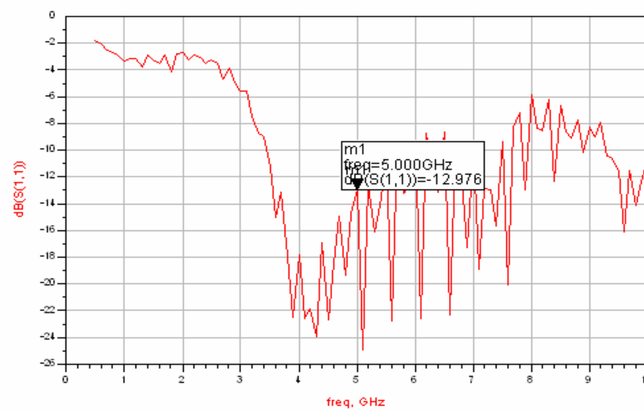
Fig 4.2.6 The measurement results of loss; about 0.3dB

4.3 Simulation and Measurement results comparison

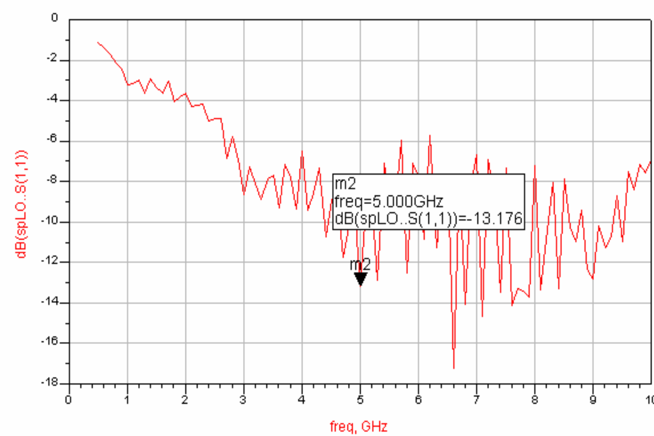
Fig4.3.1 is showed the simulation and measurement results of input return loss.



(a) The simulation of input returns loss



(b) The measurement of RF port input returns loss



(c) The measurement of LO port input returns loss

Fig 4.3.1 Comparison between simulation and measurement

The measurement input return loss of the RF port and LO port are 12.9dB and 13.1 dB, which are closed to the simulation result; 15.4dB and 17.6dB, respectively. One of an important reason should that we use several bonding wires to reduce the variation of the inductance, the impedance of matching network does not have obvious shift, Fig 4.3.2 is illustrated the bonding wires.

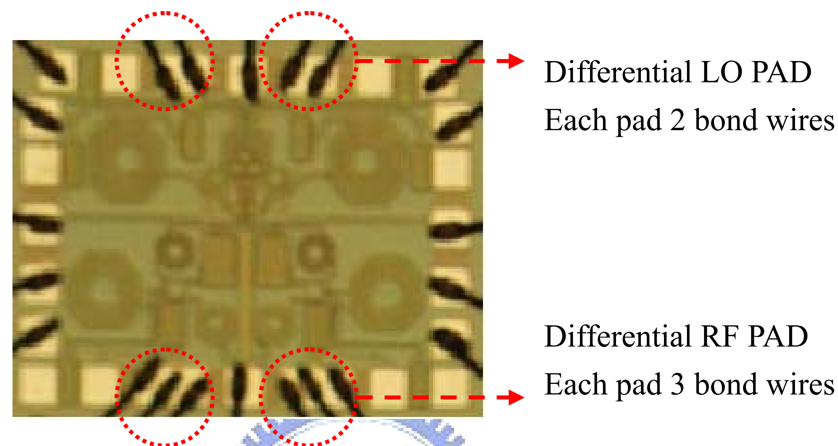


Fig 4.3.2 The bonding wire

And the mixing test is showed as Fig 4.3.3.

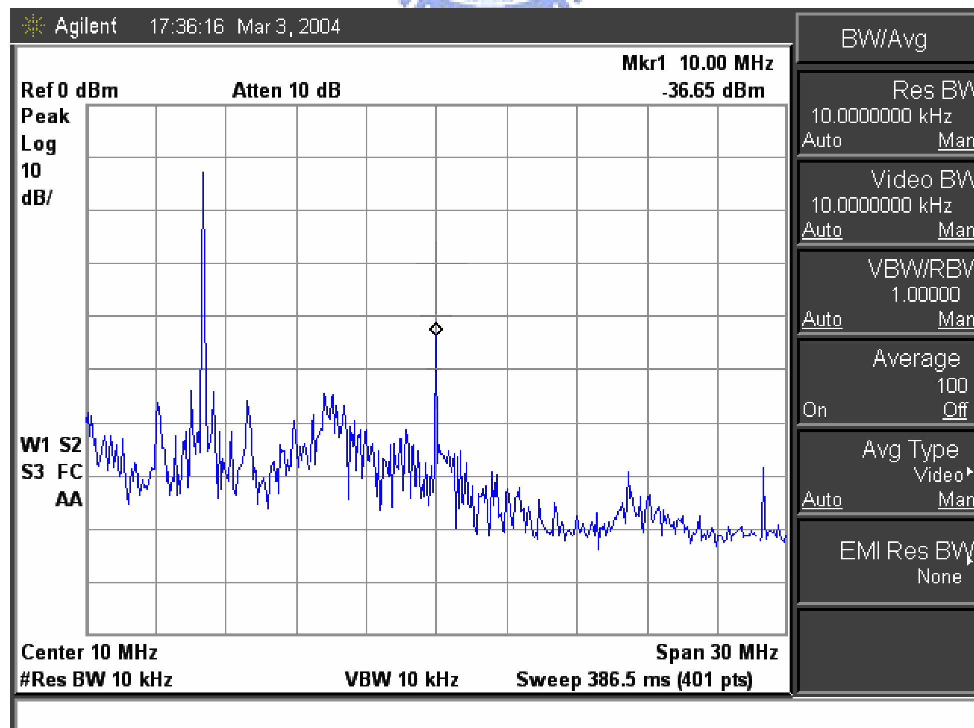


Fig 4.3.3 RF power =-35dBm @5GHz, LO power = 0dBm@ 4.99GHz, IF=10MHz

Fig 4.3.4 and Fig 4.3.5 are illustrated the conversion gain versus the LO input power and the conversion gain versus the RF input power, respectively.

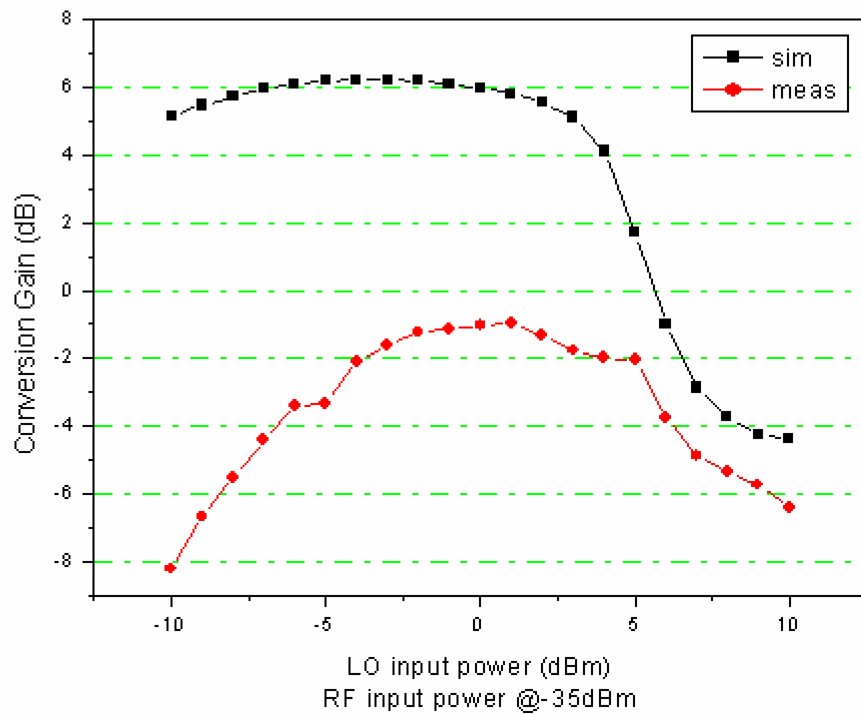


Fig 4.3.4 Conversion gain versus the LO input power

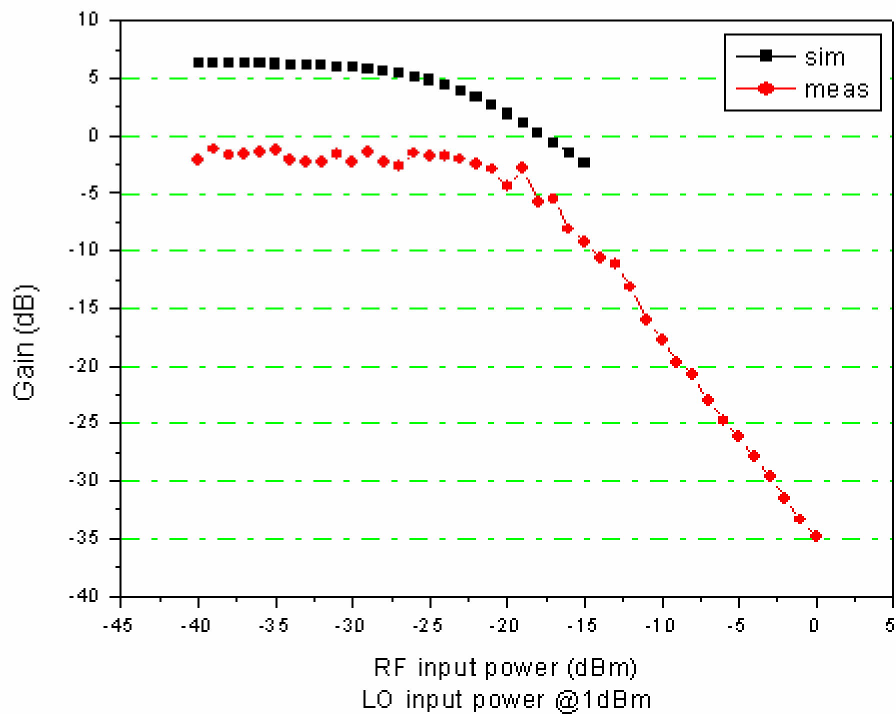


Fig 4.3.5 Conversion gain versus the RF input power

Fig 4.3.6 is shown the two-tone testing (5.001GHz and 5GHz) and IIP3.

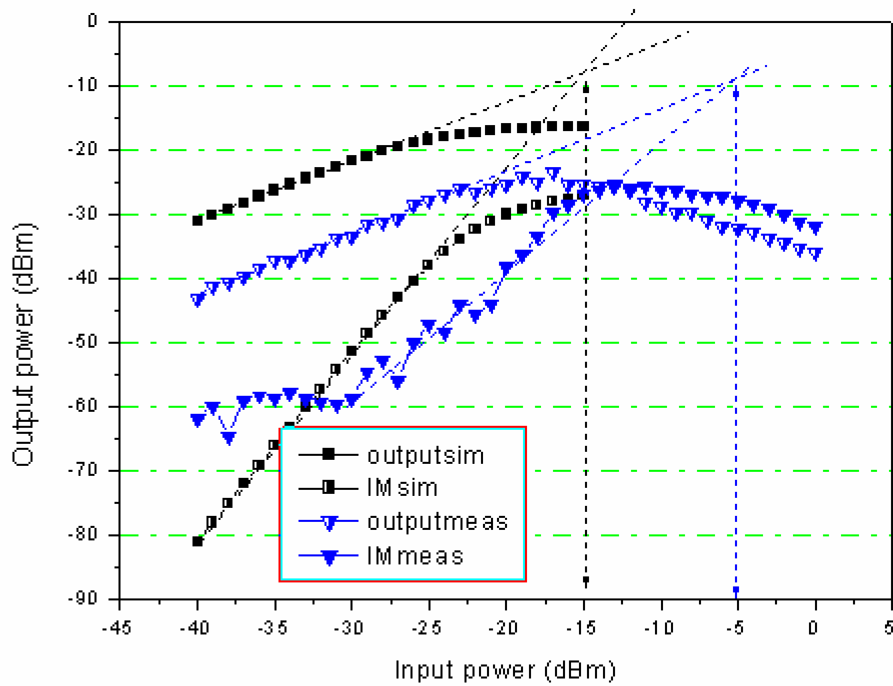


Fig 4.3.6 Comparison between simulation and measurement of IIP3

The measurement performance of conversion gain is not good as simulation. The difference is about 7dB, we take the analyses into two parts; Gm and output impedance matching. A simplified amplifier circuit is illustrated as Fig4.3.7.

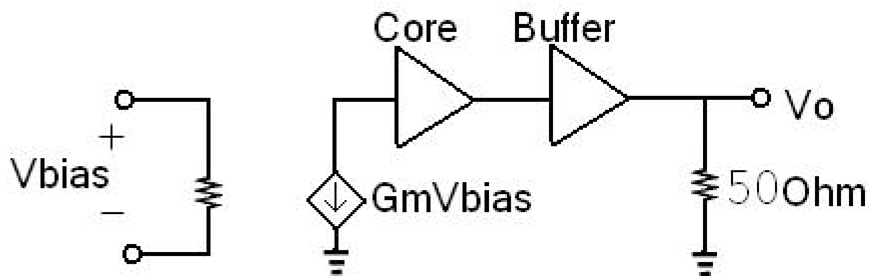


Fig 4.3.7 A simplified circuits; Vbias means lowest layer device bias voltage (bias current is domain by lowest layer active device; BJT), Gm means the total transconductor of core circuits, 50Ω is the instrument impedance.

Fig 4.3.8 and Table 4.3.1 are shown the characteristic of bias voltage versus the current; we could obtain the Gm value.

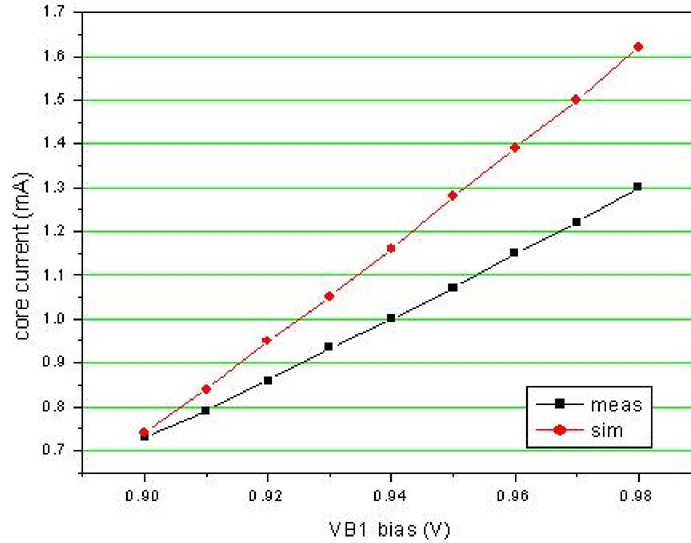


Fig 4.3.8 The characteristic of bias voltage versus the current

Bias Voltage (v)	Simulation Current (mA)	Measurement current (mA)
0.9	0.73	0.74
0.92	0.87	0.95
0.94	1	1.16
0.96	1.14	1.39

Simulation Gm = (1.39-0.74) (mA)/ (0.96-0.9) (V) = 10.83 m (1/Ω)

Measurement Gm = (1.14-0.73) (mA)/ (0.96-0.9) (V) = 6.83 m (1/Ω)

Table 4.3.1 The bias voltage versus the current

This transconductor effect would attenuate about 4dB conversion gain performance.

$$A_v = 20 \cdot \log(\frac{6.83}{10.83}) = -4.0dB \qquad (4.12)$$

Subsequently, we would discuss the output matching. If the output impedance is not equal to 50Ω, even larger than 50Ω, the output power could not deliver to load efficiently. Fig 4.3.9 is shown the consideration of output impedance.

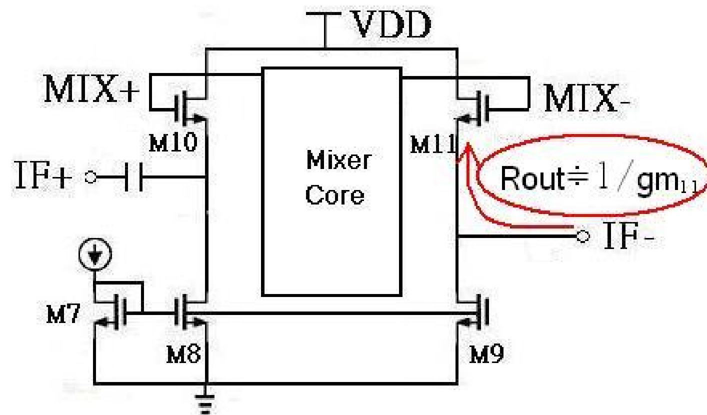


Fig 4.3.9 The buffer output impedance consideration; $R_{out} = {}^{1}/_{gm}$

The simulation value and measurement is as follow table 4.3.2, and we obtain process parameter; $K = \mu_n C_{ox} \frac{W}{L}$ from the equation.

$$gm = \sqrt{2 I_D K} \qquad (4.13)$$

Parameters	Simulation	Measurement
I_{D11} (mA)	0.81	0.6
gm_{11} ($\frac{1}{\Omega}$)	0.012956	0.01115
K ($\frac{A}{V^2}$)	0.1036	
R_{out} (Ω)	77	90

Table 4.3.2 Comparison between simulation and measurement of R_{out}

The impedance of instrument is about 50 Ω; the larger output impedance would affect the power deliver (A diagram in Fig4.3.10). From the equation, this mismatch would attenuate about 0.9dB conversion gain performance.

$$A_v = 20 \cdot \log\left(\frac{\frac{50}{90+50}}{\frac{50}{77+50}}\right) = -0.85dB \qquad (4.13)$$

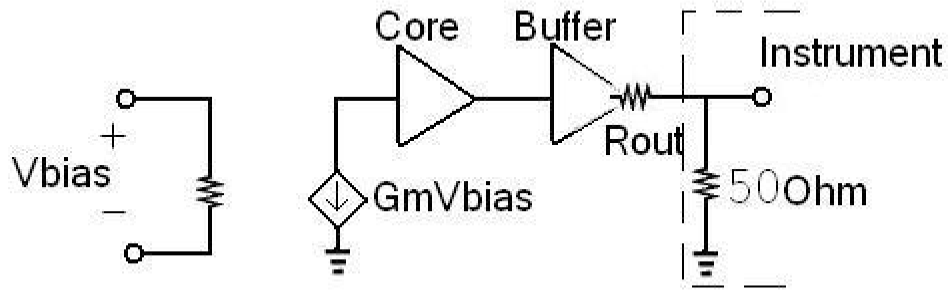


Fig 4.3.10 A diagram of Rout and 50ohm load

Table 4.3.1 is the summary of the performance of this circuit.

Specifications		Simulation	Measurement
Supply Voltage (V)		2.5	2.5
Power Consumption (mA/mW)	core	2.04mA / 5.1mW	2mA / 5mW
	buffer	2.42mA / 6mW	1.9mA / 4.8mW
	total	11.1mW	9.8mW
DSB_NF (dB)		6.8	N/A
RF Input Power (dBm)		-35	-35
LO Input Power (dBm)		-3	1
Conversion Gain (dB)	1MΩ Load	18	N/A
	50Ω Load	6.3	-0.9
RF Input Return Loss(dB)		15.4	12.9
LO Input Return Loss(dB)		17.6	13.1
IF Input Return Loss(dB)		14.6	N/A
P1dB (dBm)		-25.1	-16
IIP3 (dBm)		-15	-5
LO-RF Leakage		-70	<-30

Table 4.3.3 The summary of performance

The loss of cable, connector and Balun would be account in CIC RFIC measurement system. From the above discuss of transconductor and output matching impedance, we could find out the reasons between the different of simulation and measurement results.

6.3dB (simulation conversion gain) – 4dB (transconductor effect)

– 0.9dB (output matching impedance) – 0.3dB (loss of board and connectors)

= 1.1dB ≒ -0.9 dB (measurement conversion gain)

There are a little different from the above equation, because we could not consider the 50Ω high frequency signal impedance matching of bonding wires effect, illustrated in fig4.3.11.

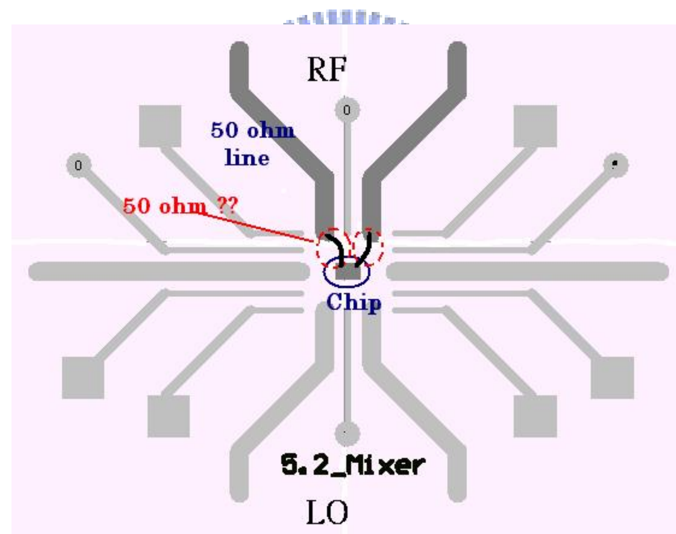


Fig4.3.11 The bonding wires effect

Besides, the experimental 1dB point and IIP3 are greater than the simulation. The trade-off between power gain and the linearity under fixed biasing condition is the criterion for amplifier design. Because the gain of measurement is lower than the expected, the performance of linearity is greater than expected one. The simulation P1dB and IIP3 are -25dBm and -15dBm, respectively, and measurement results are -16dBm and -5dBm.

The follow table 4.3.4 shows the comparison of recently papers.

REF	1[22] 2002	2[26] 2003	3[6] 2003	This work 2003.10	
				Sim.	Meas.
Frequency (GHz)	5.8	2.1	2.4	5	5
Power (mW)	48	21.6	6.3	5.1	5
Gain (dB)	20.2	23	29	6.3	-0.9
NF (dB)	9.9	3.4	3	6.8	---
IIP3 (dBm)	-6.8	-3	-16	-15	-5
P_{1dBin} (dBm)	-14	---	---	-25.1	-16
IF (Hz)	0	0	---	10Meg	10Meg
Process	SiGe 0.35um	CMOS 0.35um	CMOS 0.25um	SiGe 0.35um	SiGe 0.35um
Architecture	Two-stage LNA+ Micromixer	Concurrent LNA+ Mixer	Concurrent LNA+ Mixer	Concurrent LNA+ Mixer	Concurrent LNA+ Mixer

Table 4.3.4 Comparison of recently papers

The performance of gain is not as good as recently reports, because the output load of this work is 50 Ω, the others are not; the circuits connect with other stage, load is larger than 50 Ω. This work is a directly down conversion topology, and we set the IF is 10MHz for conveniently measurement.

Chapter 5

Conclusion

5.1 Conclusion

This thesis contents two works. The first work is a SiGe 0.35um 5.25GHz cascode LNA. The second work presents a SiGe concurrent 5GHz LNA and mixer. In this thesis, we have presented the design concepts and simulation verse experimental comparison results.

Nowadays, there are several papers provide the RF front-end circuits around the 2.4GHz and even up to 5GHz band. We try to upgrade the RF front-end circuits to 5GHz band and prove that it works at high frequency well. The difficult key points of this circuit are high frequency operation and the integration. However, we have faced these difficulties and design a signal stage LNA and concurrent front-end circuits in this work. We can see this fact in the simulation and measurement comparison results in chapter3. Although the performance does not meet our expectation, we can improve it by modeling the passive components or replacing by off-chip elements.

The full-integrated single chip LNA circuit consists: 7.5mW power consumption, a 4.6dB power gain, a 9.3dB NF, a 3.8dBm IIP3, -6.5dBm $P_{out-1dB}$, an 8.3dB input return loss and 10.9dB output return loss. The LNA design concepts and experimental results are proposed here. Besides, we also discuss the reasons about the differences between simulation and measurement results in each circuit. All of the performance was simulated by Eldo-RF at 5.25GHz. This IC has been fabricated using TSMC 0.35-µm BiCMOS SiGe foundry through CIC. And the measurement was done using on-wafer testing at RF probe station at NDL.

A concurrent SiGe LNA and mixer with low power are presented at 5GHz. It designed with off-chip inductors to approach measurement conveniently. The circuits has a -0.9dB gain, a -5dBm IIP3, a -16dBm $P_{out-1dB}$, a 12.9dB RF input return loss, a 13.1dB LO input return loss and about 10mW power consumption.

We can compare the simulation and experimental results and we can find its differentia and the reasons. Simulation results present better performances than measurement results. It may because buffer output matching impedance and the transconductor effect to cause the variations. This IC has been fabricated using TSMC 0.35-μm BiCMOS SiGe foundry through CIC and measurement is done by on-board testing at CIC.

5.2 Future Progress

At 5GHz high frequency application, we must build up more RF BiCMOS components' models such as the large capacitance MIM capacitors, spiral inductors and different inductance spiral inductors for exactly matching in future design. We would try to improve the differentia between the simulations and measurement results by more accurate components models. And we will integrate the 5.25GHz front-end with other RF or Mixed-signal parts such as filters, switch, and synthesizer of the receiver to make progress to SOC target.

In the second work, concurrent LNA and mixer, the performance is not as good as simulation. To implement large inductance and capacitance values, the multi-layers stacked spiral inductors and MOS varactor capacitors are employed. [6] We could increase the passive components models to forward the circuits performance. And we could change the architecture to reduce a number of passive large value components such as inductors and capacitors [26] (shown in Fig 5.2.1).In the original topology, the bypass large capacitor is coupling the RF output voltage signal to mixer. The LNA stage transfers input RF voltage signal to current and mix with LO signal without more passive components in proposal architecture. This one could redeem the insufficient passive models to achieve better performance.

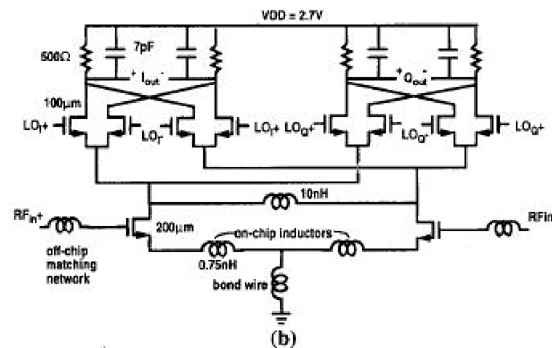


Fig 5.2.1 A merged LNA and mixer

Reference

[1] Tatsuo Itoh, George Haddad and James Harvey," RF TECHNOLOGIES FOR LOW POWER WIRELESS COMMUNICATIONS," A John Wiley & Sons, 2001

[2] K. Rim, et al., "Strained Si NMOSFETs for high performance CMOS technology," 2001 Symposium on VLSI Technology Digest of Technical papers, pp. 59-60, 2001

[3] K. Rim," Strained Si surface channel MOSFETs for high-performance CMOS technology," IEEE International Solid-State Circuits Conference, Digest Technical of Paper, pp 116-117, 2001

[4] M. Zargari, et al., "A 5-GHz CMOS Transceiver for IEEE 802.11a Wireless LAN systems," IEEE Journal Solid-State Circuits, vol. 37, pp.1688-1694, Dec 2002

[5] T. P. Liu and E. Westerwick, "5-GHz CMOS Radio Transceiver Front-End Chipset," IEEE Journal Solid-State Circuits, vol. 35, pp.1927-1933,Dec 2000.

[6] Alireza Zolfaghari and Behzad Razavi," A Low-Power 2.4-GHz Transmitter/ Receiver CMOS IC,"IEEE Journal Solid-State Circuits, vol.38, pp.176-183, Feb.2003

[7] IBM news, http://www.research.ibm.com/resources/press/strainedsilicon

[8] D. L. Harame and B.S. Meyerson," The early history of IBM's SiGe mixed signal technology," Electron Devices, IEEE Transactions on, vol. 48, issue 11, pp2555-2567, Nov, 2001

[9] D. L. Harame, et. al.," Current status and future trends of SiGe BiCMOS Technology," Electron Devices, IEEE Transactions on, vol. 48, issue 11, pp2575-2594, Nov, 2001

[10] Intrauniversity microelectronics center web page,

http://www.imec.be/wwwinter/processing/asd/activities/strained.shtml

[11]Lawrence E. Larson," Silicon Technology Tradeoffs for Radio-Frequency /Mixed-Signal 'System-on-a-chip'," Electron Devices, IEEE Transactions on, vol. 50, issue 3, pp683-6994, Mar, 2003

[12]Yuhua Cheng, Chih-Hung Chen, M. Matloubian and M. J. Deen," High-frequency small signal AC and noise modeling of MOSFETs for RF IC design," Electron Devices, IEEE Transactions on, vol. 49, issue 3, pp400-408, Mar, 2002

[13] TSMC," TSMC 0.35um SiGe BiCMOS 3P3M 3.3V Design Rule," 2002

[14] Thomas H. Lee, "The Design of CMOS Radio Frequency Integrated Circuits", 1998

[15] Thomas H. Lee and Simon Wong, "CMOS RF integrated circuit at 5GHz and beyond," Proceedings of the IEEE, vol. 88 issue 10, pp1560-1571, October 2000

[16] B. Razavi," RF Microelectronic," Prentice Hall, 1998

[17] Y. C. Xiaojuen, et al.," Demonstration of SiGe RF LNA Design using IBM Design Kits in 0.18um SiGe BiCMOS Technology," Design, Automation and Test in Europe Conference and Exhibition, 2004. DATE'04, Vol. 3,pp. 22-27, 16-20 Feb, 2004

[18] Jou C.F., Kuo-Hua Cheng, Pang-Ruci Huang and Mei-Chien Chen," Design of a fully integrated high linearity dual-band CMOS LNA," Electronics, Circuits and Systems, 2003. ICECS 2003, Vol. 3, pp. 978-981, 14-17 Dec. 2003

[19] H.R. Kim and S.G. Lee," A 5-GHz LNA for wireless LAN Application based on 0.5um SiGe BiCMOS, " ICMMT 2002, pp. 50-53, Aug 2002

[20] P. Crippa, S. Orcioni, F. Ricciardi and C. Turchetti," DESIGN OF A 4.4 TO 5 GHz LNA IN 0.25-um SiGe BiCMOS TECHNOLOGY," ISCAS03, vol. 1, May 2003

[21] R.C. Liu, C.R. Lee, H. Wang and C.K. Wang," A 5.8-GHz Two-Stage High-Linearity Low-Voltage Low Noise Amplifier in a 0.35-um CMOS

Technology," IEEE RFIC symposium, pp. 221-224, 2002

[22] S. Chakraborty, S.K. Reynolds, T. Beukema, H. Ainspan and J. Laskar ," Architectural Trade-offs for SiGe BiCMOS Direct Conversion Receiver Front-ends for IEEE802.11a," IEEE GaAs symposium, pp 120-123, Oct. 2002.

[23] J. Sadowy et al.," Low Noise, high linearity, wide bandwidth Amplifier using a 0.35um SiGe BiCMOS for WLAN applications," IEEE RFIC symposium, pp. 217-220, 2002

[24] J. Pihl, K. T. Christensen and E. Bruun," DIRECT DOWNCONVERSION WITH SWITCHING CMOS MIXER," Circuits and Systems, 2001 ISCAS2001. vol.1, pp. 117-120, 6-9 May 2001

[25] B. Gilbert," A Precise Four-Quadrant Multiplier with Sub-nanosecond Response," IEEE Journal Solid-State Circuits, vol. 3, pp. 365-373, Dec. 1968.

[26] H. Sjohand, et al.," A Merged CMOS LNA and Mixer for a WCDMA Receiver," IEEE Journal Solid-State Circuits, vol. 38, pp. 1045-1050, Jun 2003.