# 國立交通大學

## 電控工程研究所

碩士論文

# 具虛擬斜坡電流平衡技術之電壓模式多相位降壓轉換器

# Pseudo-Ramp Current Balance (PRCB) Technique for Voltage-Mode Multiphase Buck Converter

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## 摘　　要

在現今科技發展不斷進步的社會中，體積小且多功能的可攜式產品越來越受到歡迎,例如智慧型手機、MP3 及平板電腦等設備。除了功能選項多能吸引消費者，這些可攜式產品的操作時間是一個重要的考量；越長的操作時間表示系統越省電越不需要多次充電，具有很大的方便性.為了設計出省電的系統，如何使電源系統具備高效率、低損耗的特點是一項考驗，特別是需在可攜式產品有限的空間中設計。另外，在某些系統中，常常會需要電源管理電路可以提供大電流、低電壓漣波等要求，如 CPU 的電源規格.在這樣的情況下，多相位電源轉換器是一個很好的選擇。透過多相位的方式，並聯多組降壓或升壓等電壓轉換 cell 以提供大電流到輸出端。但當相位越多，也就是並聯的組數越多，就需要越多的控制器來對應多相位的控制。

為了解決多相位造成的多控制器之電源消耗與面積無法縮小問題，本論文提出一具虛擬斜坡電流平衡技術應用於電壓模式多相位直流-直流降壓轉換器，只需使用一組控制器即可達到多相位控制。在本論文中，將會依序介紹虛擬斜坡技術與對應的時間多功電流平衡機制、系統穩定度分析、電路實現方法、電路量測結果與結論。

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## ABSTRACT

A pseudo-ramp current balance (PRCB) technique is proposed to achieve the time-multiplexing (TM) current balance in voltage-mode multiphase DC-DC buck converter with only one modulation controller. Thus, compared to the conventional multiphase converter, the N-1 controllers can be removed when the PRCB technique is implemented in the monolithic N-phase DC-DC buck converters for largely decreasing the silicon area and power consumption. In addition, the TM current balance scheme can further enhance the current sharing accuracy since the mismatches between different controllers does not exist. Particularly, an explicit model of multiphase converter with the PRCB technique is derived for system stability analysis. Both of the voltage loop and the current balance loops with non-ideal effect are taken into consideration. Experimental results show that the current difference between each phase can be decreased by over 83 % at both heavy load and light load conditions.

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玉萍 于 桂月

國立交通大學

中華民國一百年九月

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# Chapter 1

# INTRODUCTION

## 1.1 Background of Power Management System and Voltage Regulators

Nowadays, portable devices such as smart phone, media player, tablet PC, are accepted widely due to the small size and versatile application. Besides the multiple functions, the operation time of these portable devices is one of the major issues of a successful product. To obtain a long operation time, the power management design of the whole system is crucial for achieving high efficiency, which means low power consumption, with limited board area inside the portable devices. To achieve a low-cost, high-efficiency and high-performance voltage regulator, there are many different kinds of power management architectures, as shown in Fig. 1, could be used such as buck converter, boost converter and charge pump, etc.

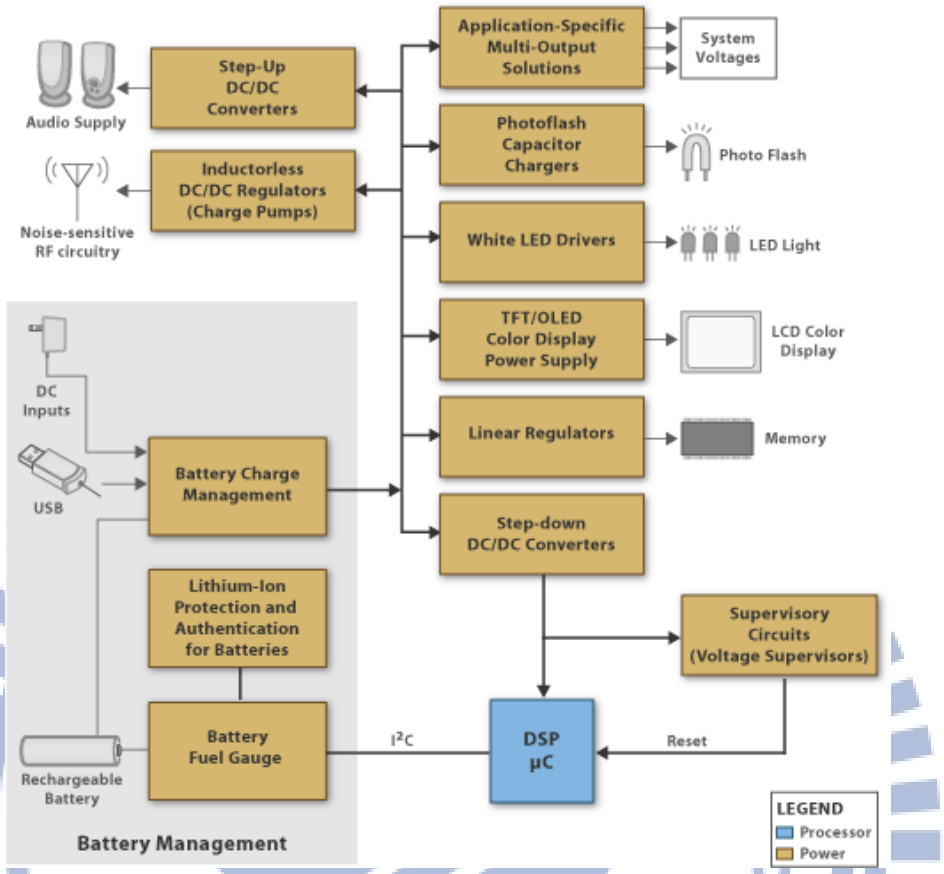



Fig. 1. Power management system.

# 1.2 Classification of Voltage Regulators

In this section, Power management circuits can be classified into three different techniques in function-works: linear regulators, switching capacitor regulators, and switching regulators. These structures are briefly introduced and described at the following subsections. Finally, a brief comparison will be given about these three types of voltage regulators.

## 1.2.1 Linear Regulator

The linear regulator (or low-dropout regulator, LDO) is usually used for light load current condition. It has simple structure, better transient performance and the output voltage is ripple-free compared to the other types of power management IC's [1]-[4]. The LDO also has

smaller chip size, printed circuit board (PCB) area. High efficiency is guaranteed by the low drop-out voltage with the input supply voltage ($V_{in}$) and regulated output voltage ($V_{OUT}$). The efficiency formula is shown in (1), where $I_Q$ is the quiescent current of the LDO and the $I_{Load}$ is the output load current.

$$\eta = \frac{V_{OUT} I_{Load}}{V_{in}(I_Q + I_{Load})} \approx \frac{V_{OUT}}{V_{in}} \tag{1}$$

As illustrated in Fig. 2, it shows the schematic of a linear regulator. The linear regulator uses a pass device ($M_P$) between the input supply voltage and the regulated output voltage. The error amplifier (EA) is the control circuit of the linear regulator. The gate voltage of the pass transistor is controlled by the output voltage of EA generated by the difference between the feedback voltage ($V_{FB}$, in a ratio of the desired output voltage ($V_{OUT}$)) and reference voltage ($V_{REF}$). The linear regulator is constructed in a negative feedback configuration to maintain the output voltage irrespective of load current and input voltage variation. Under the above description, a linear regulator operates linearly to regulate the output voltage according to the reference voltage.

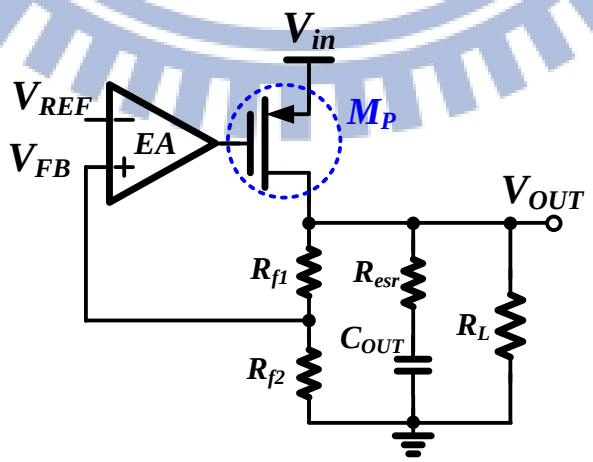



Fig. 2. The schematic of a low drop-out regulator.

## 1.2.2 Switching Capacitor Regulator

The switching capacitor regulator is usually used to obtain a DC voltage inverting or higher than the supply voltage in low load-current applications [5]-[8]. As shown in Fig. 3, this is a conventional switching capacitor regulator. There is no magnetic component, such as inductor, required comparing with the switching regulators. In the $\Phi_1$ phase period, the input voltage charges $C_f$ until the voltage $V_{Cf}$ is equal to input voltage. During $\Phi_2$ phase, the output equals to input voltage plus voltage $V_{Cf}$ and gets twice input voltage. An error amplifier decides the error signal from the difference between feedback voltage and reference voltage to adjust the operation frequency of $\Phi_1$ and $\Phi_2$ through the controller circuit. Thus, the output voltage can be regulated at desired output voltage. The controller circuit is more compact than that of switching regulators, but more complex than linear regulators. Due to switching clock, switching capacitor regulator suffers from the EMI and noise problems. But these problems are slighter than that of switching regulators, resulting from smaller operating frequency in the range of hundreds of Kilo-Hertz. The supply load ability of switching capacitor regulator is weak because it depends on the capacitor size and the switching frequency.

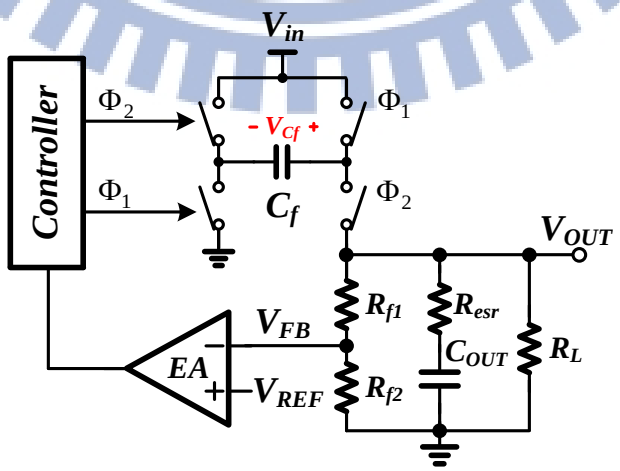



Fig. 3. The schematic of a switching capacitor regulator.

## 1.2.3 Switching Regulators

Switching regulators are widely used in power management IC because it has many excellent properties such as high power efficiency, high conversion ratio and programmable ability [9]-[18]. In Fig. 4, a simple architecture of voltage-mode buck converter, they are mixed-signal circuits which have both analog and digital blocks in the feedback loop. An analog signal, which is an error signal, is fed back to produce a digital signal at a certain frequency rate which calls duty cycle. The duty cycle is used to control the on/off state of the switches $M_{P1}$ and $M_{N1}$ to regulate the output voltage ($V_{OUT}$).

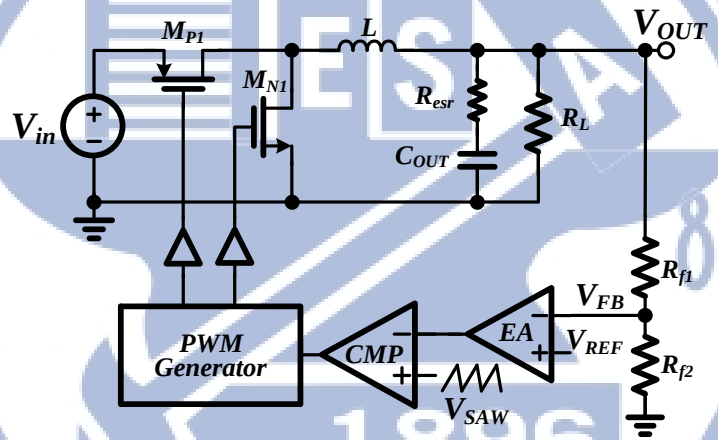


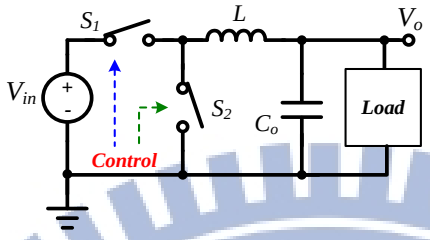
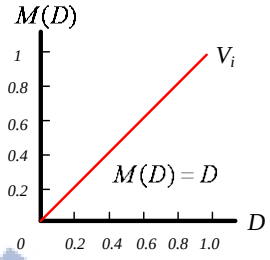
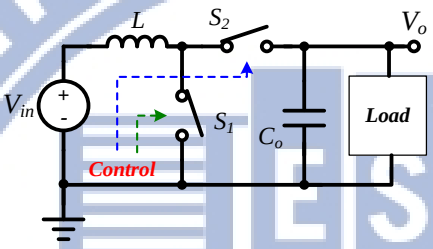
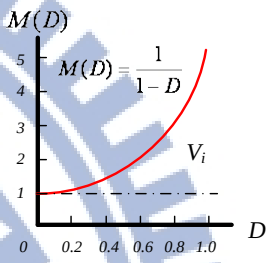

Fig. 4. The simple architecture of buck converter.

Due to dual storage components, inductor and capacitor, the switching converter can be operated in buck or boost operation. Generally speaking, the efficiency can be achieved above 90% under heavy load condition. Meanwhile, with higher switching frequency in the range from hundreds of Kilo-Hertz to several Mega-Hertz, the storage components can be designed smaller to save the cost. But the EMI and noise problems become critical. Depended on efficiency requirement, the control circuit is much larger than the other two regulators and the cost is the highest. However, the supply load ability is the largest in the range from about hundreds of milliamps to several amps.

Therefore, the switching regulators can easily be classified into two topologies in

functional-works, buck and boost converters, listed in Table I,

Table I. Two structures of switching regulators

| | Architecture | Conversion Curve |
|---|---|---|
| **Buck** |  |  |
| **Boost** |  |  |

The first regulator is called as buck converter because of its property that steping down the input voltage with respect to output node. The conversion ratio *M(D)* of buck converter is written as $M(D) = D$. The second regulator is called as boost converter because of its property that steping up the input voltage with respect to output node. The conversion ratio *M(D)* is written as $M(D) = \frac{1}{1-D}$.

There are many advantages of switching regulators compare with the linear regulators and switching capacitor regulators. Switching regulators have high current efficiency because they use power MOSFETs as switches and inductors, capacitors as energy storing elements. When the switched transistors operate in the cutoff region, it has no power dissipation. When the switched transistors operate in the triode region, it is nearly a short circuit with little voltage drop across it and has little power dissipation. Hence, most of the power dissipation is spent in the output node. A high power efficiency performance can be achieved numerically in the range 80% to 90%.

Switching regulators also have disadvantages. There are larger complexity in circuit design of switching regulators than that of the linear regulators and also require discrete components such as inductors and capacitors. Furthermore, the transition response time and output noise are much larger than that of the linear regulators.

A comparison table between linear regulators, switching capacitor regulators and switching regulators are listed in Table II.

Table II: Comparisons of the different voltage regulators.

| | **Linear Regulators** | **Switching Capacitor regulators** | **Switching Regulators** |
|---|---|---|---|
| **Regulation Type** | buck | buck/boost | buck/boost/buck-boost |
| **Efficiency** | Low | Medium | High |
| **Complexity** | Low | Medium | High |
| **Load ability** | Medium | Low | High |
| **Chip Area** | Compact | Moderate | Large |
| **EMI/Noise** | Low | Medium | High |
| **Cost** | Low | Medium | High |

# 1.3 Design Motivation

For switching regulators, operation mode switching between pulse-width modulator (PWM), pulse-frequency modulator (PFM) and pulse-skipping modulator are widely used to enhance the efficiency over the wide load range [19]-[24]. Besides, transient response is greatly improved by prior arts [25]-[30], such as Adaptive Pole-Zero Position (APZP) technique and dual-current pump. Moreover, in high-performance microprocessors applications, multiphase DC-DC converters are essential owing to its high current driving capability, small output voltage ripples and thermal management improvement [31]-[36].

Conventional PWM controller with a constant switching frequency is a suitable candidate for multiphase DC-DC converters. Nevertheless, the demand of complicated compensation

network, especially for the voltage-mode control, causes the vast increase of printed circuit board (PCB). Several methods make efforts on minimizing the area of the compensation elements [37]-[39]. Besides, to improve the load transient recovery time, the hysteresis-control DC-DC converters become an adequate solution to exhibit fast load transient response without the need of compensation components [42]. However, it suffers from synchronizing problem in multiphase applications. Although the delay-locked loop (DLL) controller can achieve synchronization between different phases with accurate duty cycle and large voltage conversion range [43], the power consumption and area occupation are substantially large.

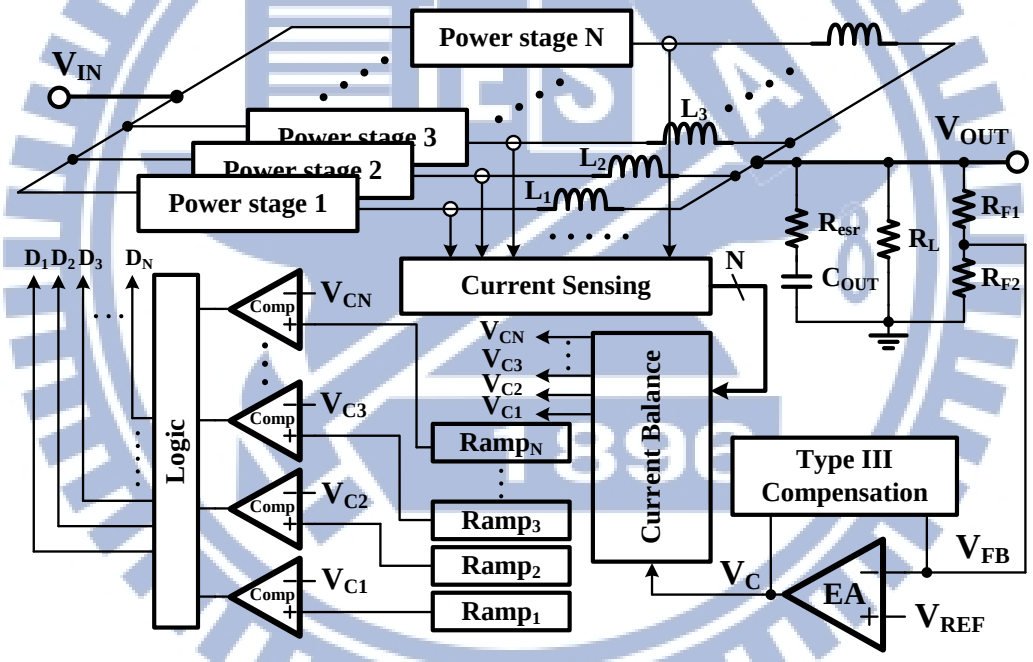



Fig. 5. Conventional structure of the N-phase voltage-mode DC-DC buck converter.

Conventional N-phase architecture as shown in Fig. 5 has high current driving capability as well as low output voltage ripple. N buck converter cells are implemented parallel in a voltage regulator module (VRM) to provide energy to the load simultaneously. In common with conventional voltage-mode DC-DC buck converter, each buck converter cell is controlled by one of the N independent controllers. In each controller, there contains a ramp generator, a comparator and a control logic circuit. Owing to the multiphase operation, N

interleaving ramp signals, $Ramp_1$-$Ramp_N$, are needed to compare with the error signals ($V_{C1}$ - $V_{CN}$) carried out from the error amplifier for generating N interleaving duty cycles, $D_1$ - $D_N$, for each phase. Obviously, the replicas of the controller derive large area and power dissipation.

## 1.4 Thesis Organization

In this thesis, the PRCB technique (Pseudo-Ramp Current Balance) is proposed to improve the performance and reduce circuit complexity in voltage-mode controlled multiphase DC-DC buck converter. The PRCB technique simply uses one controller to make multiphase operation and achieve high precision current balance comparing with the prior arts. The proposed PRCB technique are majorly divided into two parts, the pseudo-ramp technique and time-multiplexing current balance. Their description is given in the first part of Chapter 2. Besides the design concept, the system stability analysis is discussed and illustrated in the second part of Chapter 2. Detailed circuit implementations are presented in Chapter 3. Experimental results are shown in Chapter 4. Finally, a conclusion and future work are made in Chapter 5.

# Chapter 2

# PROPOSED MULTIPHASE STRUCTURE AND THE PRCB OPERATION PRINCIPLE

## 2.1 System Operation

Fig. 6 shows the proposed structure of N-phase DC-DC buck converter with the proposed PRCB technique. The N-phase power stages can simultaneously deliver energy to the output to improve the driving capability, and are controlled by a single controller to achieve an area-efficient operation. The power stage contains one P-type and one N-type power MOSFET. A dead-time control is used in the driver to prevent the short-through current problem. The voltage divider is composed of $R_{F1}$ and $R_{F2}$ to feed the information of output voltage to the controller.

The main control scheme of the proposed multiphase converter is the voltage-mode operation [31], [34] and [40]-[42]. Thus, the Type III compensation is implemented to extend the system bandwidth and to obtain an adequate system phase margin. Particularly, there are only one saw-tooth signal and one comparator in the proposed design to control the N-phase power stages. In other words, the N-phase converter can be achieved with the elimination of the N-1 controllers in the proposed PRCB technique.

The pseudo-ramp operation and the current balance mechanism constitute the PRCB technique. The pseudo-ramp generator circuit can generate the fixed-frequency system clock $V_{clk}$ to realize the pulse-width modulation (PWM). The multiphase clocks, $V_{ck1}$-$V_{ckN}$, are also

generated to ensure synchronization. Besides, the saw-tooth signal $V_{SAW}$ can be used to determine the control signal $V_{PWM}$ through the comparison with the error signals $V_C$, which is carried out by the error amplifier (EA). Here, the proposed pseudo-ramp operation uses only one physical saw-tooth signal to obtain the multiple duty cycles ($D_1$-$D_N$) for multiphase operation.

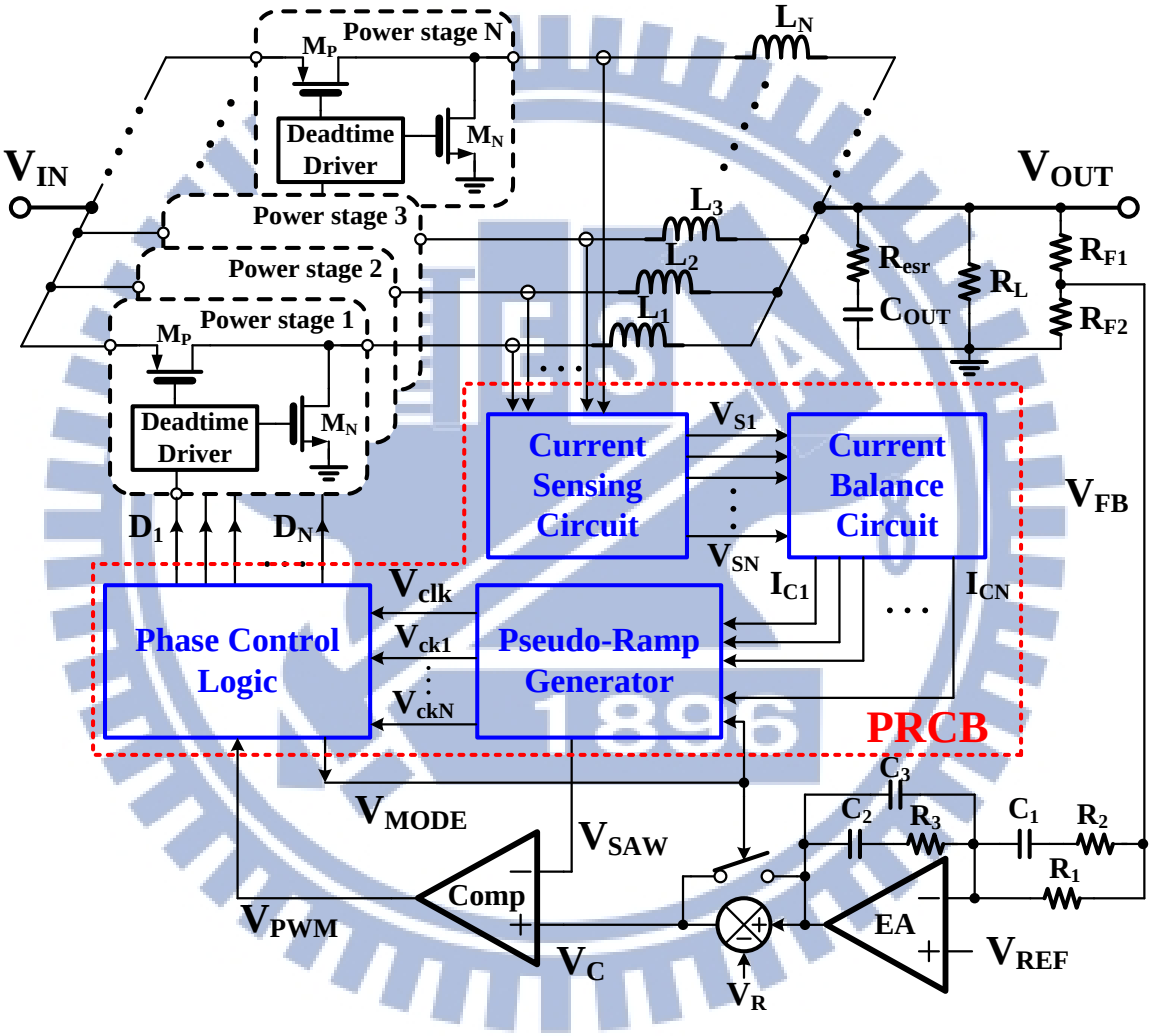



Fig. 6. Structure of the N-phase DC-DC buck converter with proposed PRCB technique.

The phase control logic can realize the duty cycles, $D_1$-$D_N$, for the N-phase power stages according to the multiphase clocks, $V_{ck1}$-$V_{ckN}$, and the signal $V_{PWM}$. Moreover, mode control signal $V_{MODE}$ is used to determine the operation modes of the pseudo-ramp operation under the different duty cycles. Specially, the auxiliary reference voltage $V_R$ is utilized to ensure the smooth mode transition operation.

On the other hand, the current balance mechanism is composed of the current sensing circuit and the current balance circuit. To ensure equal energy distribution in each of phases, the current sensing circuit can be used to sense the inductor current information during each phase. The sensed inductor current information, $V_{S1}$-$V_{SN}$, will be sent to the current balance circuit, which can generate the signals, $I_{C1}$-$I_{CN}$, to adjust the duty cycles for each phase. Therefore, the energy delivered by each of phases will be matched regardless of the mismatch problem derived between the N-phase power stages.

### 2.1.1 Pseudo-Ramp Operation

Fig. 7 shows the illustration of pseudo-ramp operation. Dual-phase topology is adopted to verify the proposed PRCB technique in this paper. The PRCB operation can be divided into two modes. It depends on the duty cycle smaller than 50 % or larger than 50 %, for Mode I or Mode II, respectively. Two clock periods, $2*V_{clk}$, will constitute one complete switching cycle, $T_s$, for two phases. That is, one pseudo-ramp is composed of two physical ramps in one switching period.

In Mode I operation, the duty cycles $D_1$ and $D_2$ of the phase 1 and the phase 2, respectively, are smaller than 50%. When the signal $V_{MODE}$ is high, as shown in the left-side of Fig. 7, the duty cycle $D_1$ of the phase 1 is determined by the intersection of the odd physical ramps, which are part of the signal $V_{SAW}$, and the error signal $V_C$. Since the duty cycle is smaller than 50 %, the $D_1$ can be determined within $T_S/2$. That is in a physical ramp. On the other hand, the duty cycle $D_2$ of the phase 2 is decided by the even physical ramps of the signal $V_{SAW}$. That means the duty cycles $D_1$ and $D_2$ are carried out by the odd and even physical ramps, respectively. In other words, the even physical ramps in the period of $T_S/2$ to $T_S$ joins the determination of the $D_2$ and has no effect on the determination of the $D_1$. In Mode I operation, only one saw-tooth signal $V_{SAW}$ with a fixed frequency is used to realize the $D_1$ and the $D_2$ for

the dual-phase buck converter operation.

Once the duty cycle is larger than 50 %, the proposed PRCB technique will enter to the Mode II operation by setting the $V_{MODE}$ low. At the right-side of Fig. 7, it shows the characteristic of the PRCB technique that can break through the limitation of 50 % duty cycle in dual-phase operation. Under Mode II control, alternatively, the $D_1$ is determined by the even physical ramps of the $V_{SAW}$ signal, and in consequence the $D_2$ is decides by the odd physical ramps. $D_1$ is high (on state) during the odd physical ramps until the intersection of $Vc$ and the even physical ramps. When the view point is changed from the odd/even physical ramp into a continuous process, it is easy to find out the determination of $D_1$ can be realised with the black extended datted-line as show in Fig. 7. The idea of Pseudo-Ramp is carried out from here. Namely, two solid-line ramps constitute one datted-line pseudo-ramp, which has the switching period $T_S$. The intersection of $V_C$ and pseudo-ramp can be extended from less 50% of $T_S$ to more than 50% of $T_S$. Thus, the duty cycle $D_1$ of amount larger than 50% can be made. Similarly, the duty cycle $D_2$ can be larger than 50%.

In the PRCB technique, two pseudo-ramps determine the dual-phase operation. Both $D_1$ and $D_2$ can be well-interleaved regardless the value of duty cycle. Most importantly, there is only one physical ramp to determine the two interleaving duty cycles.

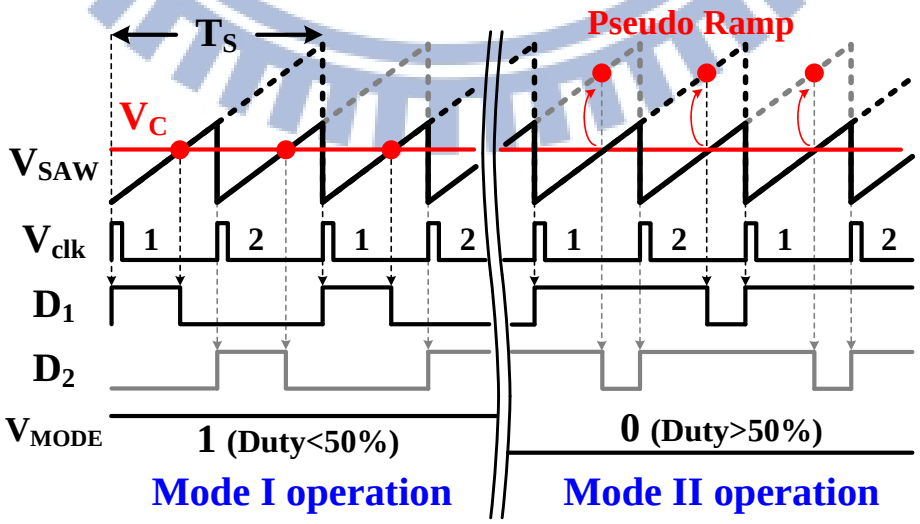



Fig. 7. The illustration of the PRCB technique in the Mode I and the Mode II.

However, the unstable scenario may happen when the duty cycle is exactly equal to 50% due to the discontinuous $V_{SAW}$. In other words, the transition will induce a step increase in the $V_C$. To solve the transition between Mode I and Mode II, the deduction of the auxiliary reference voltage $V_R$ from the EA's output is activated for rapid response in the $V_C$. As illustrated in Fig. 8, the $V_R$ helps overcome the discontinuous duty cycle determination when the duty cycle is close to 50 %. In addition, the duty blocking period (DBP) is also utilized in Mode II operation to avoid the duty cycle determination into the undistinguishable region. The DBP results in the phase shift of duty cycle in Mode II operation for stable operation because the proper duty cycle can be carried out. That is, the DBP helps define a hysteretic region to avoid the abnormal mode transitions triggered by switching noise.

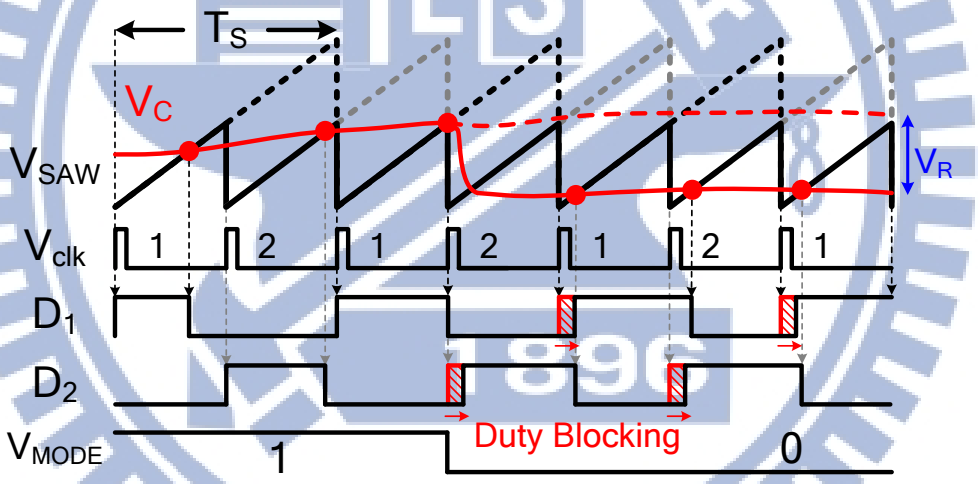



Fig. 8. The timing diagrams when the DBP is utilized.

Moreover, the mode transition operation contributes the enhancement of transient response. In case of a sudden load current increase, the voltage drop induces a rapid variation at the $V_C$ by the EA. Large increase in the $V_C$ will lead to the mode transition from Mode I to Mode II if the $V_C$ exceeds the amplitude of physical ramps. Thus, a resultant increase in the duty cycle will provide extra energy to compensate the insufficient driving capability so as to enhance the load transient response. The similar operation would occur when a large decrease of load happens.

## 2.1.2 Time-Multiplexing Current Balance Mechanism

Ideally, if each of the individual phases derives the identical duty cycles, $D_1=D_2=\ldots D_N$, the inductor current in each individual phase will be theoretically equal in the multiphase operation. However, the inevitable mismatches existing among the N power stages and PCB boards will cause enormously unbalanced current distribution. Thus, the current balance mechanism is demanded to compensate the unbalanced scenario by automatically adjusting the duty cycles by $\hat{d}_i(t)$ (where *i=1, 2, 3…* and *N*). Thus, the adjusted duty cycle of each phase becomes $d_i(t) = D_i + \hat{d}_i(t)$ (where *i=1, 2, 3…* and *N*) to achieve current balance. Fig. 9 shows the implemented current balance mechanism in the proposed PRCB technique.

If one of the two phases has large driving current, the duty cycle, which causes large driving current, needs to decrease. Contrarily, the other duty cycle is required to increase. Owing to the voltage-mode operation in the monolithic control scheme, the duty cycles are determined through the comparison of the $V_{SAW}$ and the $V_C$. [40]-[42] However, in the PRCB technique, it is improbable to adjust the $V_C$ for current balance since the change in the $V_C$ will lead both duty cycles to increase or decrease simultaneously. Alternatively, the modulation in the $V_{SAW}$ is used to achieve the dual-phase current balance in the PRCB technique [44].

The time-multiplexing current balance mechanism is activated in the PRCB technique according to the distinct operation modes. In the Mode I, the ramp adjustments for the $d_1(t)$ and $d_2(t)$ act on the odd and even ramps, respectively. If the inductor current $I_{L1}$ in phase 1 is larger than the $I_{L2}$ in phase 2, the increase of the odd ramp slopes will lead the decrease of the $d_1(t)$ to reduce the current driving capability in phase 1. Besides, the increase of $d_2(t)$ in phase 2 will enhance its current driving capability by decreasing the even ramp slopes. Similarly, in case of large $I_{L2}$ and small $I_{L1}$, the current balance can also be ensured in the Mode I.

On the other hand, when the duty cycle is larger than 50 % in the Mode II, the ramp

adjustment will work in an alternative way to fit the pseudo-ramp operation. The odd ramp slopes are decreased while the even ramp slopes are increased to reduce the $d_1(t)$ and to enlarge the $d_2(t)$ when the $I_{L1}$ is larger than the $I_{L2}$. The similar operation is achieved when the $I_{L1}$ is smaller than the $I_{L2}$ in the Mode II. Therefore, the current balance mechanism can be realized by adjusting the ramp signals both in the Mode I and the Mode II. In other words, current balance is achieved under the whole duty cycle range.

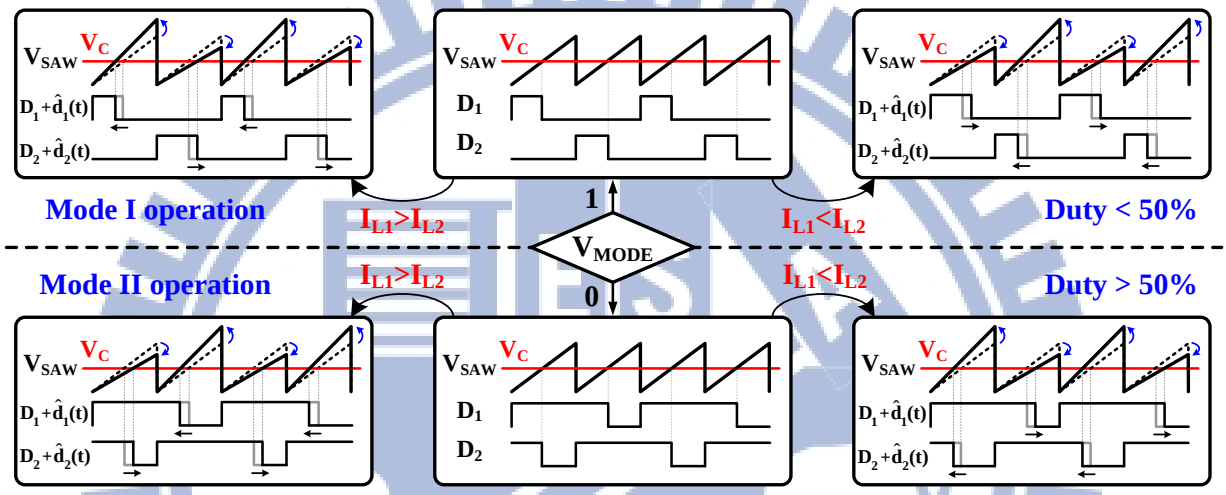



Fig. 9. Current balance mechanism implemented with pseudo-ramp operation in the proposed dual-phase DC-DC buck converter.

## 2.2 Stability Analysis of the Multiphase Converter with the PRCB Technique

To ensure the system stability, not only the proposed PRCB technique but also the TM current balance technique should be modeled accurately. In this work, a dual-phase converter is modeled to verify the system stability.

## 2.2.1 The Model of the Pseudo-Ramp Technique

Equivalent model of the two-phase converter with the pseudo ramp technique is shown in Fig. 10 [45]. In frequency domain, the duty cycle can be expressed as (2).

$$d_i(s) = D_i + \hat{d}_i(s) \text{ where } i = 1 \text{ or } 2 \tag{2}$$

$\hat{d}_i(s)$ is the duty cycle variation caused by the TM current balance technique. $D_i$ is the duty cycle without the current balance function. Theoretically, $D_1$ and $D_2$ are equal to the average duty cycle as shown in (3).

$$D = \frac{d_1(s) + d_2(s)}{2} \text{ where } i = 1 \text{ or } 2 \tag{3}$$

The feedback voltage $V_{FB}(s)$ is acquired by the voltage divider with the gain of $H(s)$. The difference of the $V_{ref}$ and the $V_{FB}(s)$ is amplified by the error amplifier to produce the error signal $V_C(s)$. The modulator compares the $V_C(s)$ with the ramp signal to generate the duty cycles, $d_1(s)$ and $d_2(s)$, for phase 1 and phase 2, respectively.

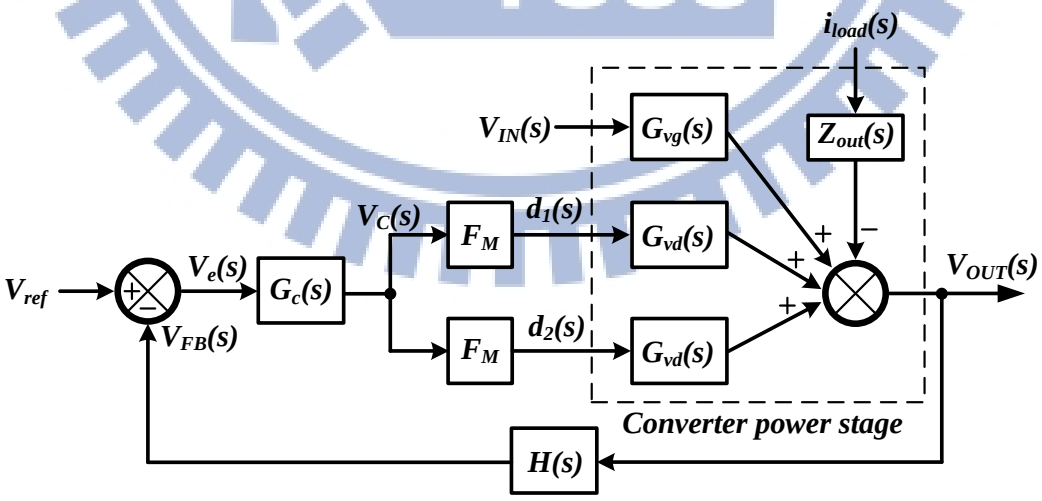



Fig. 10. Equivalent model of the two-phase converter with the pseudo-ramp technique.

The open-loop output impedance $Z_{out}(s)$, the line-to-output transfer function $G_{vg}(s)$, and the control-to-output transfer function $G_{vd}(s)$ are expressed in (4), (5), and, (6), respectively.

$$Z_{out}(s) = \frac{sL}{1 + s\frac{L}{R_L} + s^2 LC} \tag{4}$$

$$G_{vg}(s) = D \cdot \frac{1}{1 + s\frac{L}{R_L} + s^2 LC} \tag{5}$$

$$G_{vd}(s) = \frac{V_{OUT}}{D} \cdot \frac{1}{1 + s\frac{L}{R_L} + s^2 LC} \tag{6}$$

$L$, $C$, and $R_L$ are the filter inductor, capacitor, and equivalent load resistance, respectively.

In the pseudo-ramp control, all phases share the same ramp. Similar to the conventional architecture of multiple controllers, it is convenient to model separately the modulator of each phase. The effective magnitude of pseudo-ramp is twice of the physical ramp amplitude $V_M$. Thus, the modulator gain, $F_M$, can be written as (7).

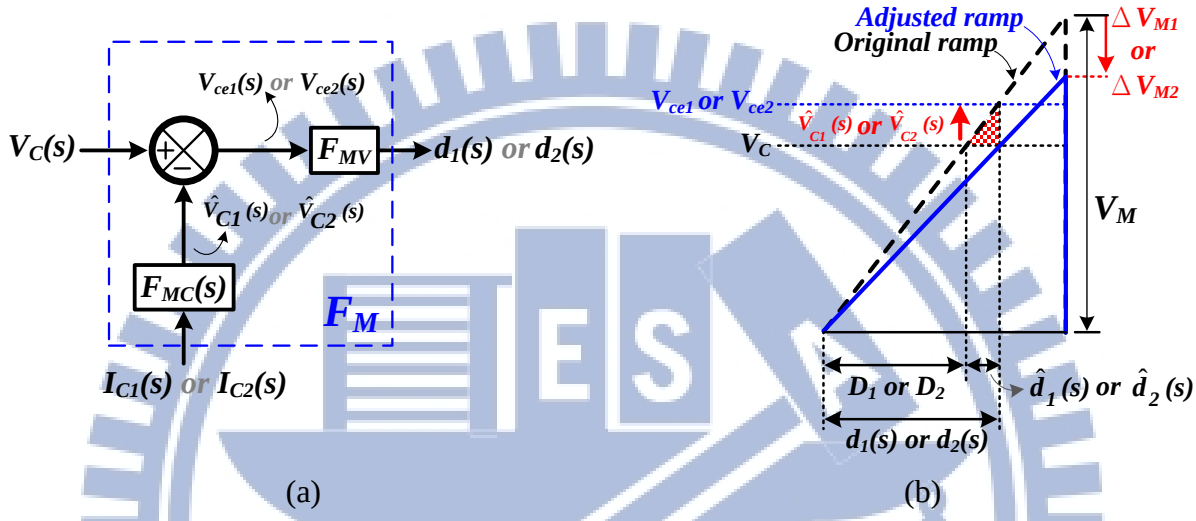
$$F_M = \frac{1}{2V_M} \tag{7}$$

Considering the stability problem, Type III compensation is adopted to compensate the complex poles caused by the $L$, $C$. Fortunately, only one set of Type III compensator is required since the PRCB technique has single controller. Besides, the design of the Type III compensation is simply the same as single phase operation.

## 2.2.2 TM Current Balance Model

TM current balance can be achieved by comparing the adjusted ramp with the error signal $V_C(s)$. To fit the characteristic of the adjusted ramp, the model of the pulse-width modulator needs to be modified as shown in Fig. 11(a). The difference of the current sensing signals, $V_{S1}$ and $V_{S2}$ in Fig. 6, which derived from the current sensing circuit, will be amplified to generate

the current-balance control signals $I_{C1}(s)$ and $I_{C2}(s)$. The $I_{C1}(s)$ and $I_{C2}(s)$ are injected to the ramp signal capacitor $C_{ramp}$ to adjust the amplitude by $\Delta V_{Mi}$ ($i$=1 or 2) as depicted in Fig. 11(b). The equivalent variation in the duty cycle is equal to $\hat{d}_1(s)$ (or $\hat{d}_2(s)$), which causes the duty varies from $D_1$ (or $D_2$) to $D_1 \pm \hat{d}_1(s)$ (or $D_2 \pm \hat{d}_2(s)$). Thus, the modified duty cycles $d_1(s)$ and $d_2(s)$ can achieve good current balance.




(a) (b)

Fig. 11. (a) Equivalent model of the pulse-width modulator with the current balance. (b) The relationship between the duty cycle and the adjusted ramp.

Without the current balance function, the duty cycle is obtained by comparing the error signal $V_c(s)$ with the original ramp. For the two phases, the original duty cycles are $D_1$ and $D_2$ as shown in (8).

$$D_i(s) = \frac{V_C(s)}{2V_M} \quad (i = 1 \text{ or } 2) \tag{8}$$

Here, the $\Delta V_{Mi}$, which can be either a positive or a negative value, contributed by the current balance circuit compensates current unbalance circumstance to adjust the ramp amplitude $V_M+\Delta V_{Mi}$ ($i$=1 or 2). Comparing the adjusted ramp with the $V_c(s)$, the duty cycle $d_i(s)$ ($i$=1 or 2) with the current balance can be expressed in (9).

$$d_i(s) = \frac{V_C(s)}{2(V_M + \Delta V_{Mi})} \quad (i = 1 \text{ or } 2) \tag{9}$$

Since the $\Delta V_{Mi}$ is produced by injecting the current-balance control signal $I_{C1}(s)$ (or $I_{C2}(s)$) into the ramp capacitor $C_{ramp}$ during the period of $T_s/2$ for each phase, the $\Delta V_{Mi}$ can be derived as (10).

$$\Delta V_{Mi} = I_{Ci}(s) \cdot \frac{T_s}{2} \cdot \frac{1}{C_{ramp}} \text{ (where } i = 1 \text{ or } 2) \tag{10}$$

According to (8), (9) and (10), the duty cycle variation is given by (11).

$$\begin{aligned} \hat{d}_i(s) = d_i(s) - D_i &= -\frac{V_C(s)}{2} \cdot \frac{\Delta V_{Mi}}{V_M (V_M + \Delta V_{Mi})} \\ &\approx -D\frac{\Delta V_{Mi}}{V_M} = -\frac{DI_{Ci}(s)T_s}{2V_M C_{ramp}} \ (i = 1 \text{ or } 2) \end{aligned} \tag{11}$$

As a result, the adjusted-current-to-duty transfer function can be derived as shown in (12).

$$\frac{\hat{d}_i(s)}{I_{Ci}(s)} \approx \frac{DT_s}{2V_M C_{ramp}} \tag{12}$$

The model of the PRCB technique with the current balance is complicated since the duty cycle is determined by many factors. To simplify the model, the duty cycle variation $\hat{d}_1(s)$ (or $\hat{d}_2(s)$) is transferred to the error signal variation $\hat{V}_{C1}(s)$ (or $\hat{V}_{C2}(s)$). Thus, the pseudo-ramp modulator can be divided in to two blocks, the voltage modulator $F_{MV}$ and the current modulator $F_{MC}(s)$. With the TM current balance technique, the error signal variation $\hat{V}_{C1}(s)$ (or $\hat{V}_{C2}(s)$) is subtracted from the original error signal $V_C(s)$ to generate the effective error signal $V_{ce1}(s)$ (or $V_{ce2}(s)$). Comparing the $V_{ce1}(s)$ (or $V_{ce2}(s)$) with the original ramp signal is able to obtain the duty cycle $d_1(s)$ (or $d_2(s)$), which is equal to the comparison of the error signal $V_C(s)$ and the adjusted ramp signal. Here, the voltage modulator $F_{MV}$ in (13) remains the same as (7).

$$F_{MV} = F_M = \frac{1}{2V_M} \tag{13}$$

Besides, the current modulator $F_{MC}(s)$ is derived as (14). Here shows a fact that the current balance effect is in relation with the magnitude of the average duty cycle. As *D* becames larger, the effect of $F_{MC}(s)$ is greater because of capacitor integration.

$$F_{MC}(s)=\frac{\hat{V}_{Ci}(s)}{I_{Ci}(s)}=\frac{\hat{V}_{Ci}(s)}{\hat{d}_i(s)}\cdot\frac{\hat{d}_i(s)}{I_{Ci}(s)}$$
$$=2V_M\cdot\frac{DT_s}{2V_M C_{ramp}}=\frac{DT_s}{C_{ramp}}(i=1 \text{ or } 2) \quad (14)$$

## 2.2.3 System Stability Analysis

In spite of the disturbance of input voltage and load current, eventually, the equivalent model of the PRCB technique with the TM current balance is depicted in Fig. 12. Except for the voltage loop, the TM current balance loop as well as the cross coupling loop are also included. The voltage loop is defined as (15).

$$T_v(s)=G_c(s)F_{MV}G_{vd}(s)H(s) \quad (15)$$

In the current balance loop, the two-phase inductor currents are sensed by the $R_i$ and hold by the sample-and-hold circuits to generate the signals, $V_{SH1}(s)$ and $V_{SH2}(s)$. The sensing and sampling effect will introduce a pair of complex RHP zeros at half of the switching frequency [28]. The transform function can be expressed as (16).

$$H_e(s)\approx\frac{s^2}{\omega_n^2}+\frac{s}{\omega_n Q_n}+1 \text{ where } Q_n=-\frac{2}{\pi} \text{ and } \omega_n=\frac{\pi}{T_s} \quad (16)$$

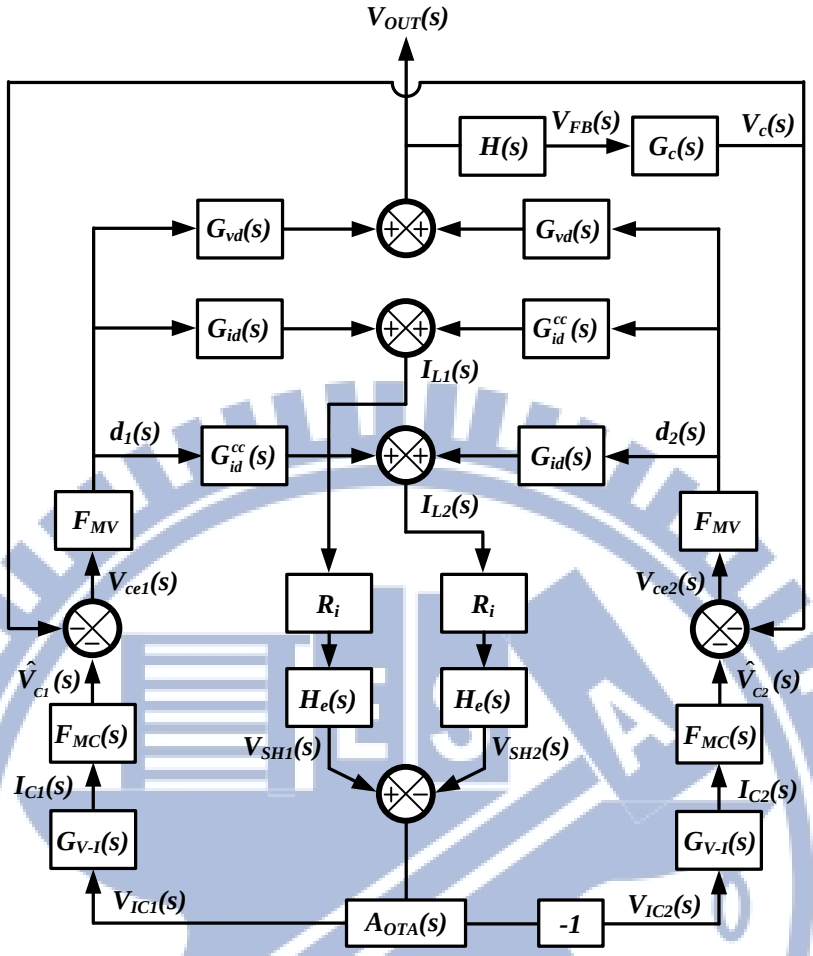



Fig. 12. Equivalent model of dual-phase buck converter with the PRCB technique and the TM current balance.

The difference of the $V_{SH1}(s)$ and the $V_{SH2}(s)$ will be amplified by operational transconductance amplifier $A_{OTA}(s)$ to obtain the current balance control voltages, $V_{IC1}(s)$ and $V_{IC2}(s)$. The V-to-I converter $G_{V\text{-}I}(s)$ converts the $V_{IC1}(s)$ and the $V_{IC2}(s)$ to the current balance control currents, the $I_{C1}(s)$ and the $I_{C2}(s)$, respectively, which can adjust the $d_1(s)$ and the $d_2(s)$, respectively. The duty-to-current transform function is derived in (17) for each phase.

$$G_{id}(s) = \frac{V_{OUT}}{D} \frac{1 + sC\left(R_L + R_{esr}\right)}{s^2 LCR_1 + s\omega_0 Q_0 + R_{DCR} + R_L}$$
$$\text{where } \omega_0 Q_0 = L + C\left[R_L\left(R_{DCR} + R_{esr}\right)\right] + R_{DCR}R_{esr} \quad (17)$$
$$\text{and } R_1 = R_L + R_{esr}$$

The characteristic of current loop is the crucial of the TM current balance technique. Ideally, a stable current loop will not have influence on the output voltage. Furthermore, the

operation of current balance loop is independent of load current but relies on the difference of the dual-phase inductor currents. Therefore, the output can be regarded as shorted ground. The duty-to-current transform function is modified as (18).

$$G_{id}(s)\big|_{\hat{V}_{OUT}=0} = \frac{V_{OUT}}{D} \cdot \frac{1}{sL + R_{DCR}} \tag{18}$$

Since the TM current balance scheme is based on the average current balance control, the small signals in two phases are the same in magnitude and opposite in phase [34]. That is, $\hat{V}_{SH1} = -\hat{V}_{SH2}$, $\hat{V}_{IC1} = -\hat{V}_{IC2}$, $\hat{I}_{C1} = -\hat{I}_{C2}$, $\hat{d}_1 = -\hat{d}_2$, and $\hat{I}_{L1} = -\hat{I}_{L2}$. Consequently, the two loops in dual-phase operation become symmetric and thus are added as shown in Fig. 13. Thus, the TM current balance loop gain is derived as (19).

$$T_{cb}(s) = 2A_{OTA}(s)G_{V-I}(s)F_{MC}(s)F_{MV}G_{id}(s)\big|_{shorted} R_i H_e(s) \tag{19}$$

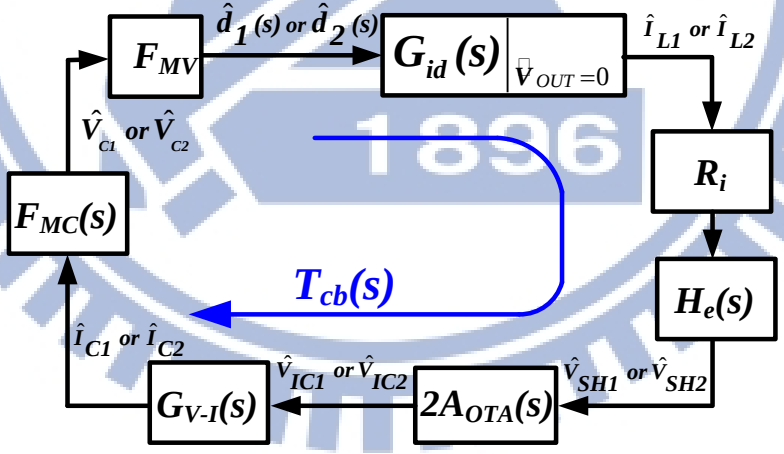



Fig. 13. Small signal model of the TM current balance loop.

Ideally, the inductor current is controlled by its own current balance control signal. However, the inductor current in one phase will be affected by the change in duty cycle of another phase inevitably [47]. Therefore, the cross coupling effect has to be taken into consideration in system stability analysis. The cross coupling duty-to-current transform function can be derived as (20).

$$G_{id}^{cc}(s) = -\frac{V_{OUT}}{D}\frac{R_L(1+sCR_{esr})}{(sL+R_{DCR})}\frac{1}{s^2LCR_1 + s\omega_{cc}Q_{cc} + R_{DCR} + 2R_L}$$
$$\text{where } \omega_{cc}Q_{cc} = L + C\left[R_L(R_{DCR}+2R_{esr})\right] + R_{DCR}R_{esr} \quad (20)$$
$$\text{and } R_1 = R_L + R_{esr}$$

And the cross coupling loop can be defined as (21).

$$T_{cc}(s) = -A_{OTA}(s)G_{V-I}(s)F_{MC}(s)F_{MV}G_{id}^{cc}(s)R_iH_e(s) \quad (21)$$

In the proposed structure, a compensation capacitor is located at the output of the operational transconductance amplifier. The added compensation pole not only ensures the stability of current balance loop $T_{cb}(s)$ but also compensates the cross coupling loop $T_{cc}(s)$. The bode plot of loops $T_v(s)$, $T_{cb}(s)$ and $T_{cc}(s)$ is shown in Fig. 14. The DC gain and the phase margin of the $T_v(s)$ are 91.9 dB and 51° while the DC gains and the phase margins of the $T_{cb}(s)$ and the $T_{cc}(s)$ are (24.7 dB, 52°) and (12.2dB, 86°), respectively. With the stabilized loops, the system stability is assured.

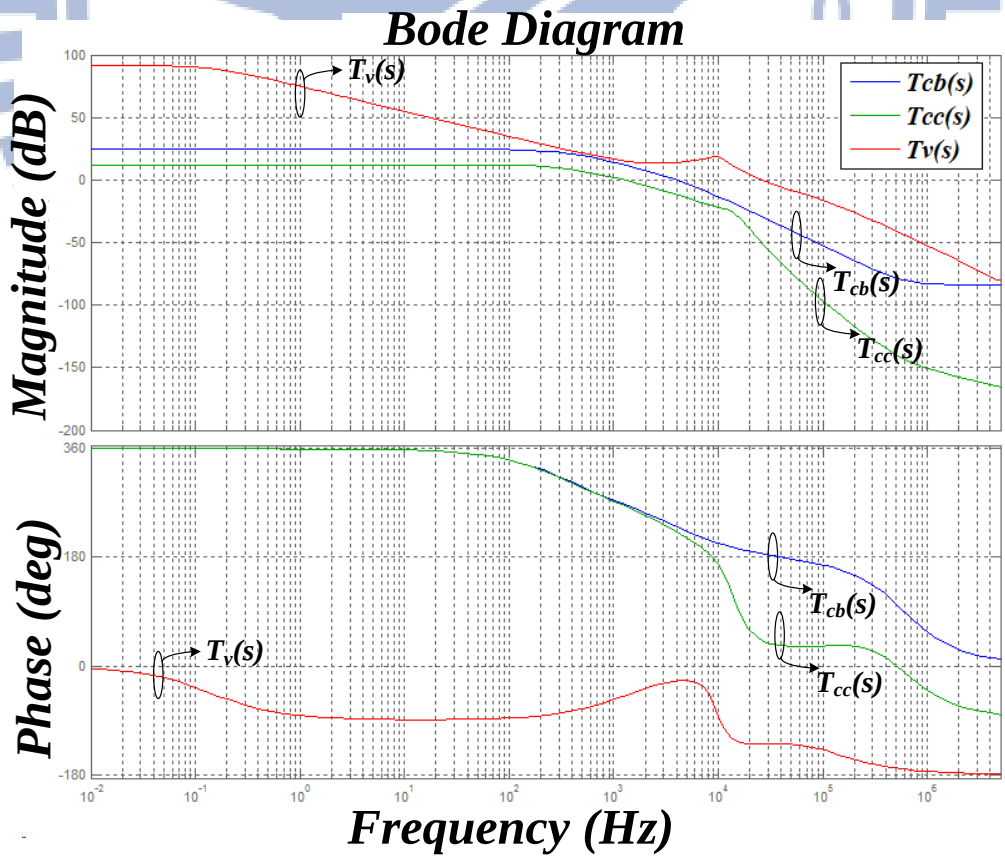



Fig. 14. The frequency response of the $T_v(s)$, the $T_{cb}(s)$ and the $T_{cc}(s)$.

Moreover, the voltage loop dominates the operation of the whole multi-phase system. In other words, the voltage loop gain is designed to be higher the current balance loop gain. Bandwidths of both loops are desired as large as possible in general design to accelerate the transient response. However, the enlarged bandwidth of the current balance loop would slow down load transient response due to the lack of rapidly increasing inductor current. For instance, in case of light-to-heavy load variation, one of the phases must suddenly prolong the on-time to cope with the lack of energy. Consequently, it causes current unbalance inevitably. Simultaneous, the current balance loop will start to pull down the unbalance inductor current. Owing to the enlarged bandwidth, the suppression of energy provided to output will be reduced by the fast current balance loop. More switching cycles are needed to regulate output voltage. As a result, loop gain and bandwidth of the two loops have to be carefully designed to meet the specification.

# Chapter 3

# CIRCUIT IMPLEMENTATION

## 3.1 Current Sensing Circuit

For current balance, the inductor current information of each phase needs to be detected to modulate the individual duty cycles. The simplest way to achieve current sensing is to implement an auxiliary resistor in series with the power switch. It induces large power dissipation so as to deteriorate the power conversion efficiency [47]-[48]. Therefore, Fig. 15 shows the utilized current sensing circuit with the replica current flowing through the sensing switch [10]. The power transistor $M_P$ conducts the inductor current during its turn-on period. The common-gate amplifier, which is composed of $M_2$-$M_5$, can ensure the near source-to-drain voltages between the $M_P$ and the sensing MOSFET $M_{S1}$. Thus, the sensing current $I_{sen}$ as the replica of the inductor current depends on the aspect ratio between the $M_P$ and the $M_{S1}$.

The $I_{sen}$ flows through the $M_6$ and the sensing resistor $R_S$ to carry out the current sensing signal $V_S$. Besides, to enhance the current sensing accuracy, the $M_7$, which has the same aspect ratio as the current mirror structure, the $M_2$ and the $M_3$, is added to provide a compensative current, $I_B$. Moreover, the sensing speed of the proposed current sensing circuit can be improved since the common-gate gain stage derives large operation bandwidth since no compensation component is demanded in this structure [49].

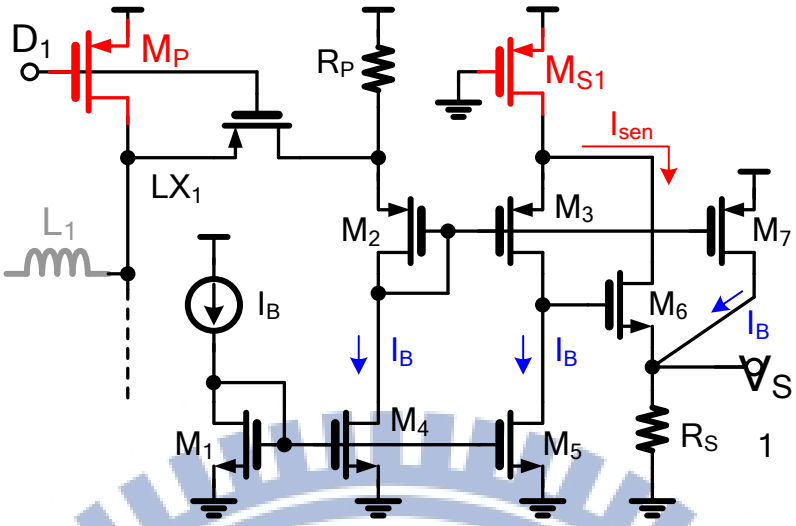



Fig. 15. The current sensing circuit.

## 3.2 Current Balance Circuit

Current balance mechanism in the multiphase structure can ensure equivalent current driven capability of each phase. As shown in Fig. 16, the proposed current balance circuit, which contains the current matching unit and the voltage averaging element, is used to adjust the saw-tooth signal generated by the pseudo-ramp generator circuit, as well as the duty cycles for matched inductor current levels. The sensing signals, $V_{S1}$ and $V_{S2}$, derived from the current sensing circuits will be sent into the current matching unit. The sample-and-hold (SH) circuit is activated to obtain the voltages, $V_{SH1}$ and $V_{SH2}$, for representing the average inductor current level of each phase.

To get an accurate current balance, the voltage averaging element is used to derive the average value $V_{avg}$ for the phase current distribution. That is, a high-gain operational transconductance amplifier (OTA) is realized to reflect the current difference between the average value and each of the phases. The voltage difference will be amplified to generate the current balance control signals, $V_{IC1}$ and $V_{IC2}$**.** $V_{IC1}$ and $V_{IC2}$ are converted to the difference injection currents $I_{C1}$ and $I_{C2}$, respectively, which are injected into the pseudo-ramp generator for current balance. Since the high-gain OTA is chosen to enhance the current balance

accuracy, the capacitor $C_c$ is used to stabilize the current-loop operation. As a result, both of the on-chip and off-chip mismatch issues will be well compensated through the current balance control scheme. Only one controller is utilized to achieve high accuracy and area and conversion efficiency in the proposed PRCB technique.

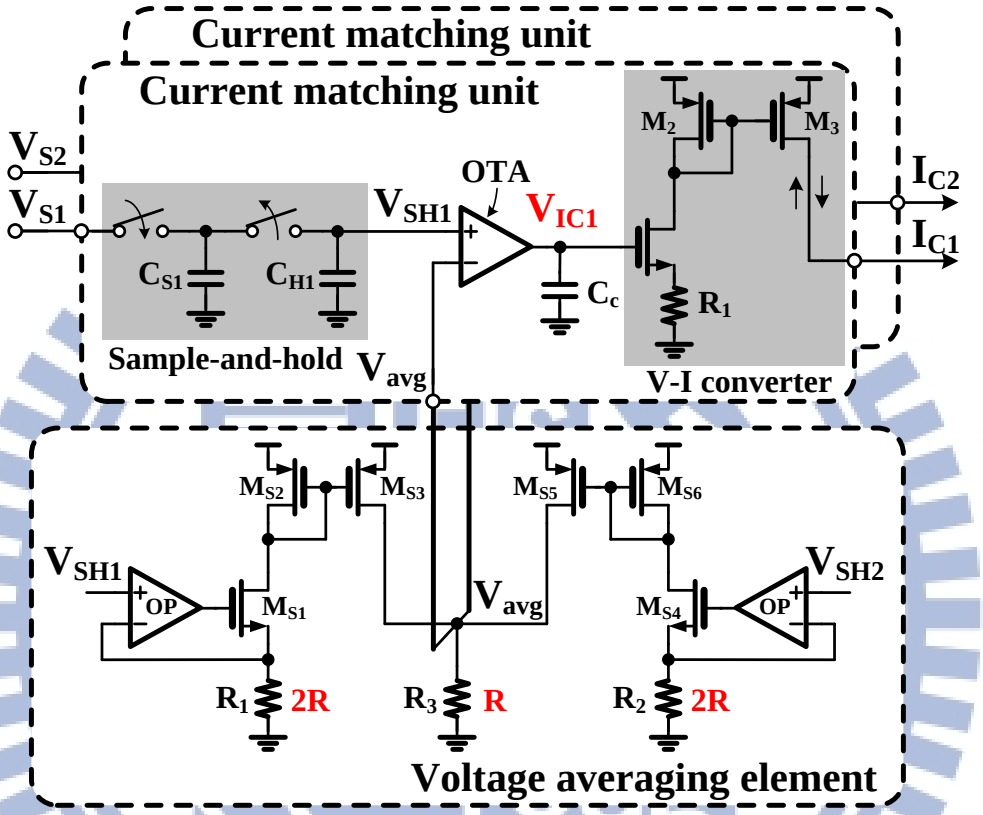



Fig. 16. Current balance circuit.

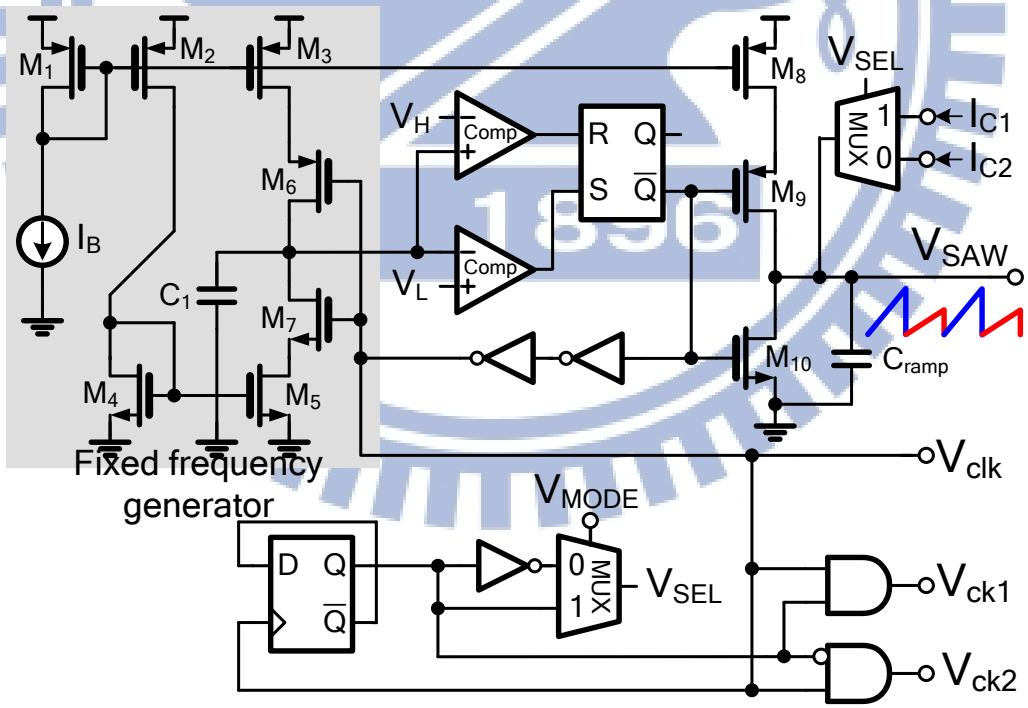
# 3.3 Pseudo-Ramp Generator

Fig. 17(a) shows the schematic of the pseudo-ramp generator. A fixed frequency signal $V_{clk}$ is derived through the fixed frequency generator composed of $M_1$-$M_7$ and the capacitor $C_1$. The reference voltages $V_H$ and $V_L$ are derived from the bandgap circuit to determine the frequency of $V_{clk}$ with the bias current $I_B$. Thus, the $V_{clk}$ can be used to control the switches, $M_9$ and $M_{10}$, to generate the saw-tooth signal $V_{SAW}$ through the charging and discharging of $C_{ramp}$ for achieving the PRCB technique.

Suppose the dual-phase inductor currents are well balanced, the $I_{C1}$ and the $I_{C2}$ must be

equal. That is, each of the ramps of $V_{SAW}$ is identical so as to realize the same duty cycle for the dual-phase operation. However, once the current unbalance operation occurs, the current balance circuit will detect the current difference between the two phases to modulate the $I_{C1}$ and the $I_{C2}$ and thus to modify the $V_{SAW}$. By alternatively injecting the $I_{C1}$ and the $I_{C2}$, the odd and even ramps in the $V_{SAW}$ will be changed to adaptively adjust the duty cycles as well as the dual-phase inductor currents. The compensated current injection is also controlled by the signal $V_{MODE}$ to properly generate the pseudo-ramp signal for different operation modes.

The timing diagram of the pseudo-ramp generator circuit is depicted in Fig. 17(b). Moreover, a frequency divider is implemented to carry out the two phase clocks, $V_{ck1}$ and $V_{ck2}$, for the dual-phase operation. The $V_{ck1}$ and the $V_{ck2}$, indicate the beginning of the switching cycle of phase 1 and phase 2, respectively. Consequently, the phase control logic can produce individual duty cycle for each power stage.




(a)

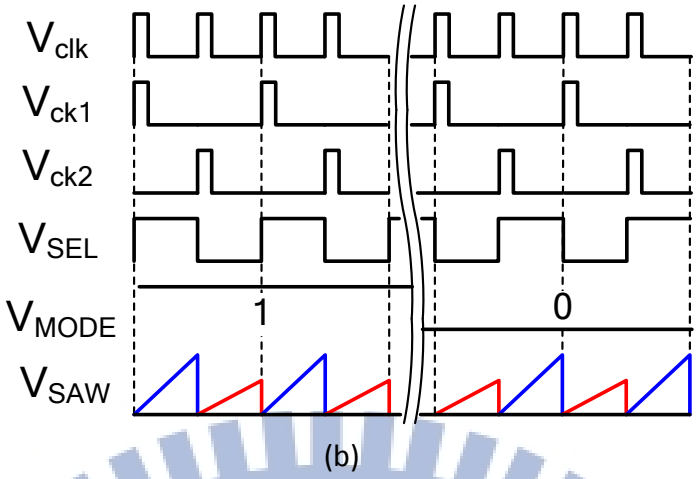


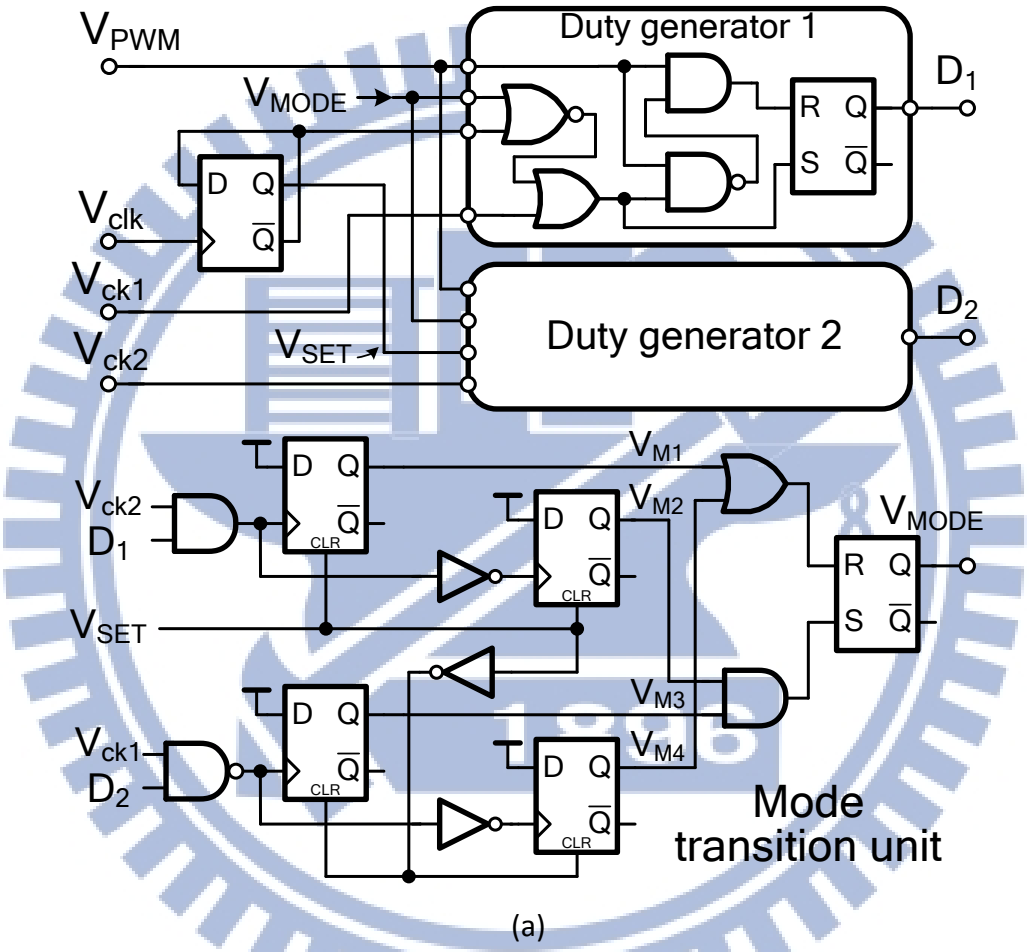

Fig. 17. The pseudo-ramp generator. (a) Schematic (b) Time diagrams

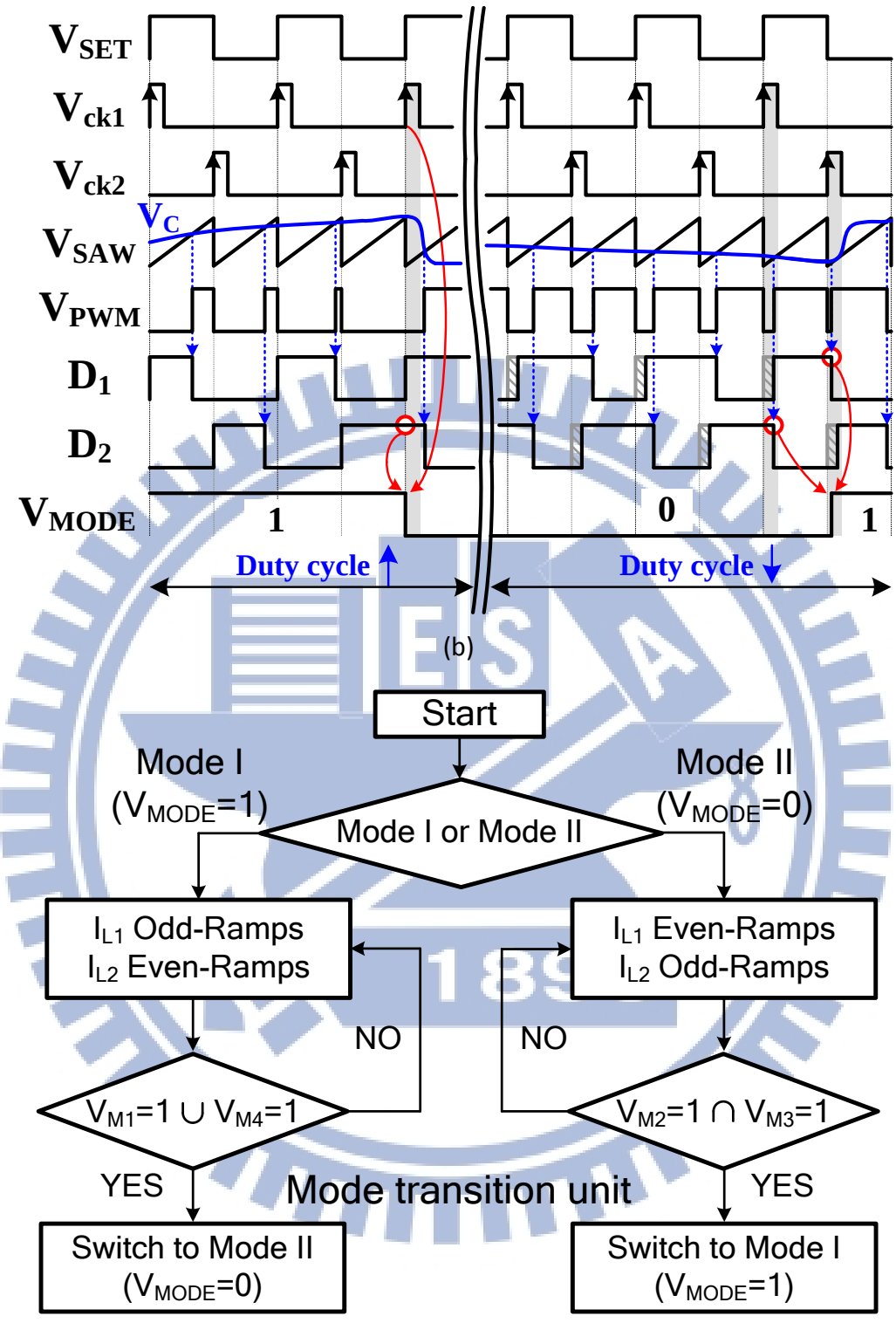
# 3.4 Phase Control Logic

Fig. 18 shows the implementation and the operation of phase control logic. Fig.18(a) shows the schematic of phase control logic, which is composed of the duty generator unit and the mode transition unit. The signals $V_{clk}$, $V_{ck1}$, and $V_{ck2}$ are generated from the pseudo-ramp generator. The $V_{ck1}$ and the $V_{ck2}$ are used to indicate phase 1 and phase 2, respectively, because there is only one saw-tooth signal to determine the duty cycle. The $V_{PWM}$ is the resultant duty determination derived from the comparison of the $V_{SAW}$ and the $V_C$ in the proposed pseudo-ramp operation. The $V_{ck1}$ and the $V_{ck2}$ can activate the $D_1$ and the $D_2$, respectively. In the meanwhile, the rising edge of the $V_{PWM}$ is used to reset the duty cycles and thus wait for the next triggering. The operation time diagram is depicted in Fig. 18(b).

The mode transition unit is used to decide the operation mode according to the duty cycle. With a continuously increasing duty cycle in the Mode I, the $D_1$ or the $D_2$ would overlap with the $V_{ck2}$ or the $V_{ck1}$, respectively. Thus, the $V_{M1}$ or the $V_{M4}$ will indicate the exceeding duty cycle of 50 %. The overlapping of the $D_1$ and the $V_{ck2}$ (or that of the $D_2$ and the $V_{ck1}$) represents that the duty cycle in the Mode I has taken over the full period of one physical ramp in the $V_{SAW}$. Once it occurs, the operation mode will transit from the Mode I to the Mode II in order to obtain the sufficient duty cycles in the PRCB technique.

On the other hand, if the duty cycle is continuously decreasing in the Mode II, it would enter the boundary region of duty determination. When both the $D_1$ and the $D_2$ do not cover the entire period of the $V_{ck2}$ and the $V_{ck1}$, respectively, the duty cycle is smaller than 50 %. To ensure the proper pseudo-ramp operation, the operation mode will change from the Mode II to the Mode I. Detailed flow chart of the mode transition operation is shown in Fig. 18(c).






(c)

Fig. 18. (a) Implementation of the phase control logic. (b) Time diagram of the phase control logic. (c) Flow chart of the mode transient operation.

# Chapter 4

# EXPERIMENTAL RESULTS

## 4.1 Chip Micrograph and Design Specification

The proposed multiphase DC-DC buck converter with the PRCB technique was fabricated in 0.25 μm CMOS process. Dual power stages are embedded in the test chip for verification. The utilization of off-chip inductors and capacitors are 4.7 μH and 47 μF, respectively. The chip micrograph is shown in Fig. 19 with an active silicon area of 3.91 $mm^2$. Power stages of phase 1 and phase 2 are placed closed to bond pads. The single controller is implemented in the middle of the chip so as to minimize the mismatches issues for both power stages. The key design specifications are listed in Table III.

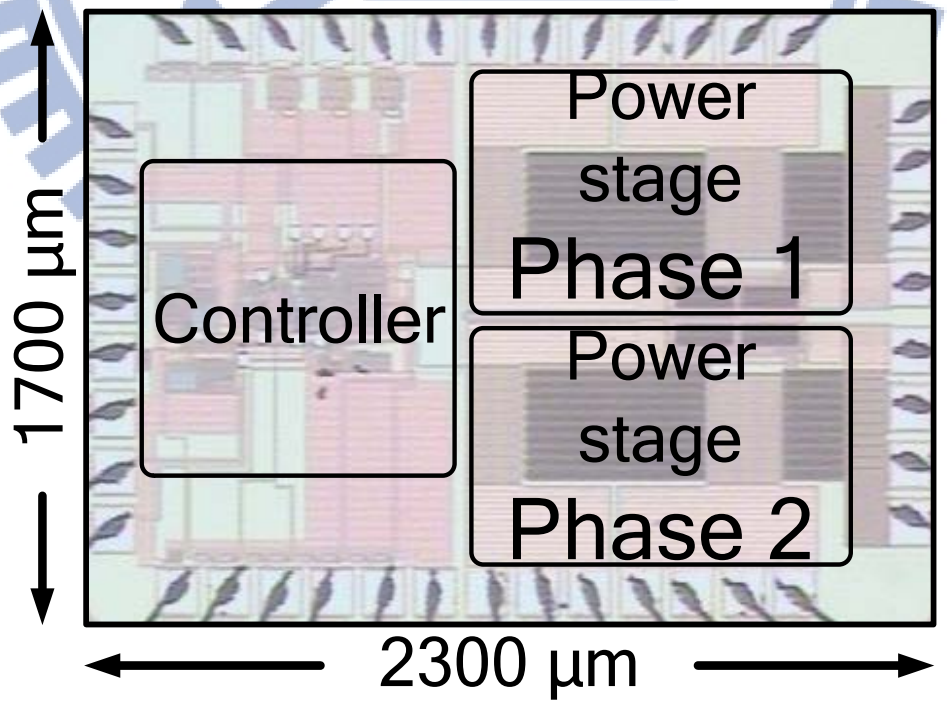



Fig. 19. Chip micrograph.

TABLE III: Design specification of the PRCB multiphase voltage buck converter

| | |
|---|---|
| Technology | 0.25m μm CMOS process |
| Inductor / DCR | 4.7 μH/ 100 mΩ (nominal) |
| Capacitor /ESR | 47 μF/ 50 mΩ (nominal) |
| Switching Frequency | 600 kHz |
| Input Voltage ($V_{IN}$) | 3.3 V – 5 V |
| Output Voltage range ($V_{OUT}$) | 0.8 V – 3 V ($V_{IN}$ = 3.3 V) |
| Load Current range ($I_{Load}$) | 0 mA – 2000mA |
| Current balance improvement (%) | Min. 83% |
| Power conversion efficiency | Max. 88 % |
| Chip size | 3.91 $mm^2$ |

## 4.2 Steady-State Operation Results

Fig. 20 shows the measured steady-state operation. With the input voltage $V_{IN}$ of 3.3 V, the nominal output voltage $V_{OUT}$ is 2 V. The switching frequency is 600 kHz. The mismatch from the size of power MOSFETs and the DCR of inductors between each phase results in current unbalance. The proposed pseudo-ramp operation can generate the proper duty cycles for the dual-phase operation with a 12 mV output voltage ripple. Besides, the current balance mechanism achieves the current matching. Fig. 21 shows the measured steady-state operation with the load current of 500 mA. The pseudo ramp can decide the correct duty cycles so as to guarantee the output voltage regulation. The current difference between the dual phases is reduced to 1.9 mA, which can verify the operation of the proposed current balance mechanism in the PRCB technique.

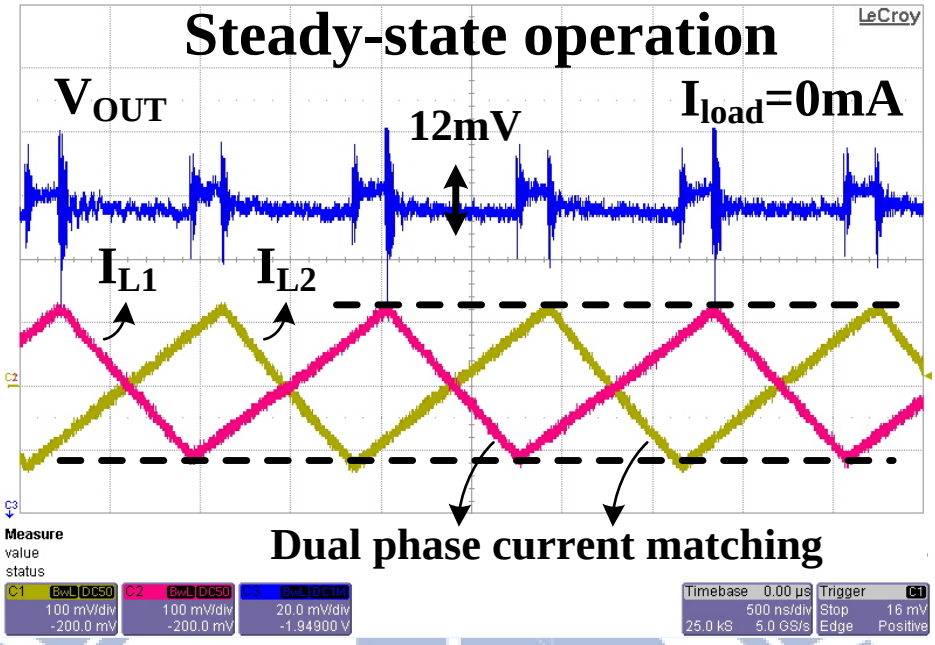



Fig. 20. Measured steady-state operation result with the $V_{IN}$ of 3.3 V.

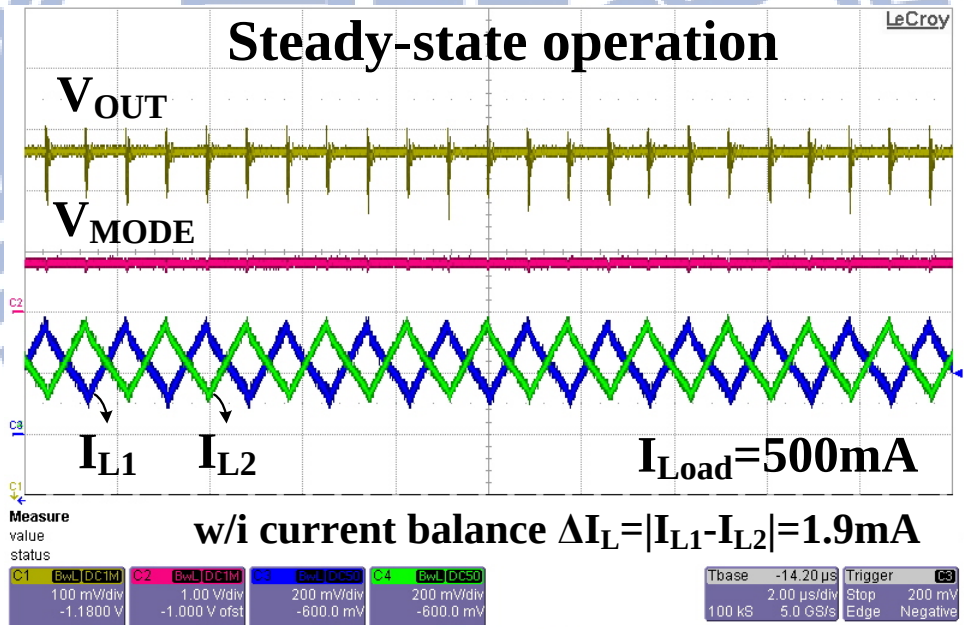



Fig. 21. Measured steady-state operation result with $I_{Load}$ of 500mA.

# 4.3 Load Transient Response

Fig. 22 shows the measured load transient response with the load changes between 0 mA and 550 mA. The voltage drop and overshoot are about 70 mV and 40 mV, respectively. The current balance mechanism is achieved in the period of load transient response as well.

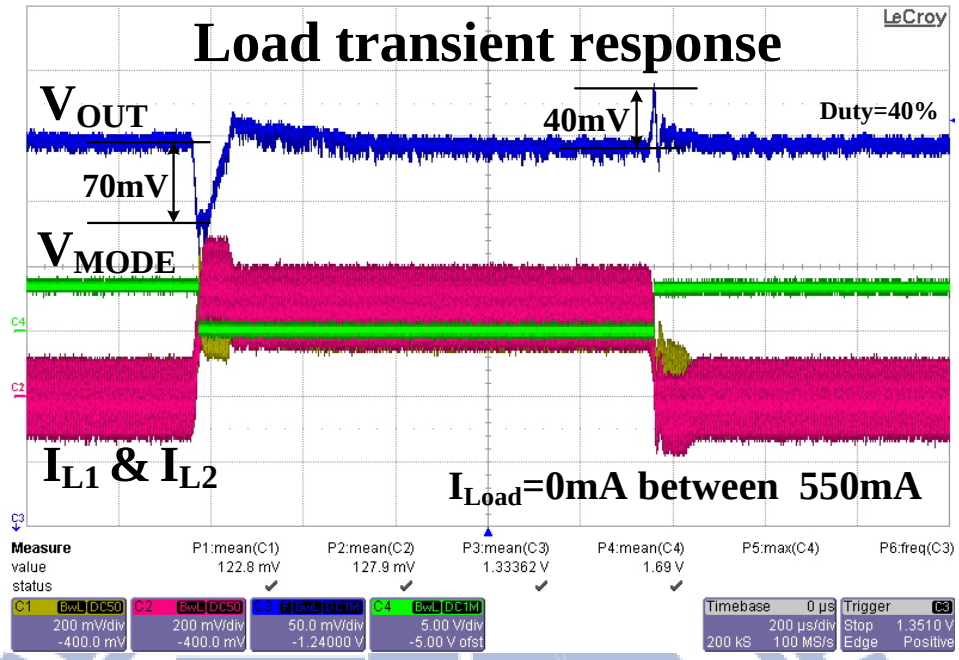



Fig. 22. Measured load transient response with the current balance mechanism.

The mode transition operation is shown in Fig. 23 The operation mode would be changed from the Mode I to the Mode II during the load transient period so as to enlarge the duty cycles to derive extra energy. In Fig. 23(a), the load current steps from 0 mA to 550mA and the recovery time is long since the mode transition function is closed for comparison. The second experiment result as shown in Fig. 23(b), which shows a shorter recovery time, is taken to examine the load transient improvement with the mode transition function opened. Thus, as shown in the experimental results, the mode transition operation can help minimize the voltage drop and shorten the transient response time to enhance the load transient operation. The operation mode may be switched back to the Mode I once the load transient period is terminated. However, the DBP mechanism helps define a hysteretic region to avoid the abnormal mode transitions triggered by switching noise. Therefore, the converter will keep operating in the Mode II until the surplus energy is detected at the output.

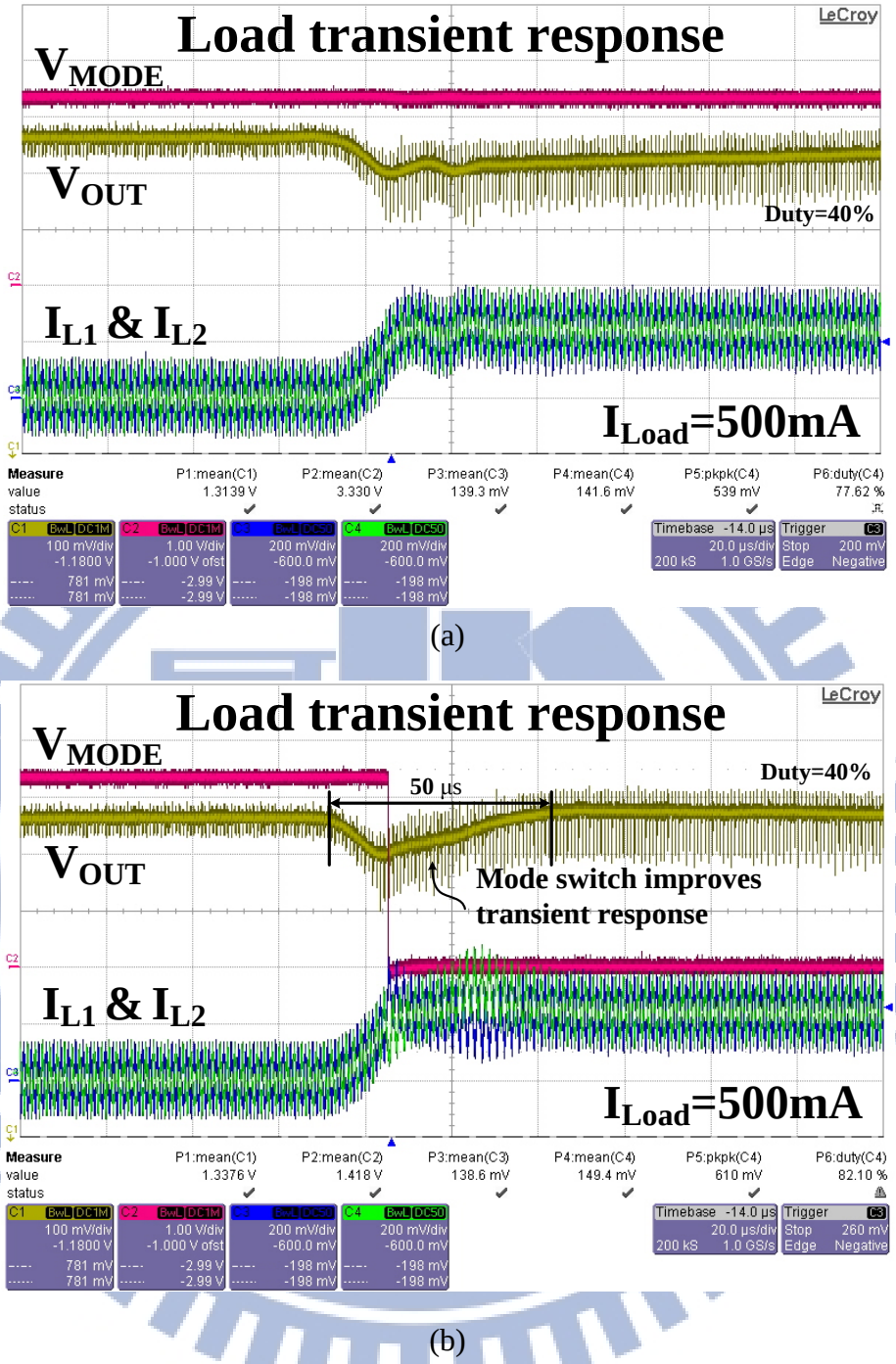



Fig. 23. Experimental results of load transient response (a) without mode switching strategy and (b) with the mode switching strategy.

# 4.4 Line Transient Response

As described in the foregoing sections, Mode I and Mode II are used for duty cycle smaller and larger than 50%, respectively. To show the relation between the variations of duty cycle, caused by the input voltage, with the mode transition operation, the line transient response of

the proposed circuit has been taken. Fig. 24 presents the experimental result of the line transient response. While input voltage is changing between 2V and 2.5V, for getting the same output voltage, the mode transient operation will change the mode signal $V_{MODE}$ to cooperate with the variations of input voltage. For instance, to keep the output voltage of 1.1V, the duty cycle is 55% when the input voltage is 2V. At this time, $V_{MODE}$ is high for the operation of mode II. When the input voltage changes to 2.5V, the duty cycle of 44% makes $V_{MODE}$ to be low for the operation of mode I.

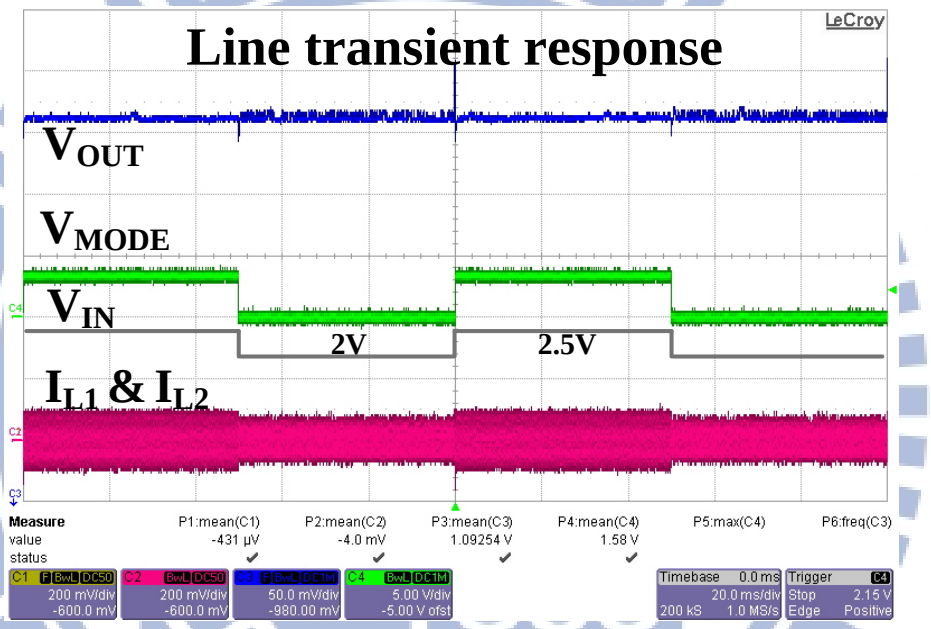
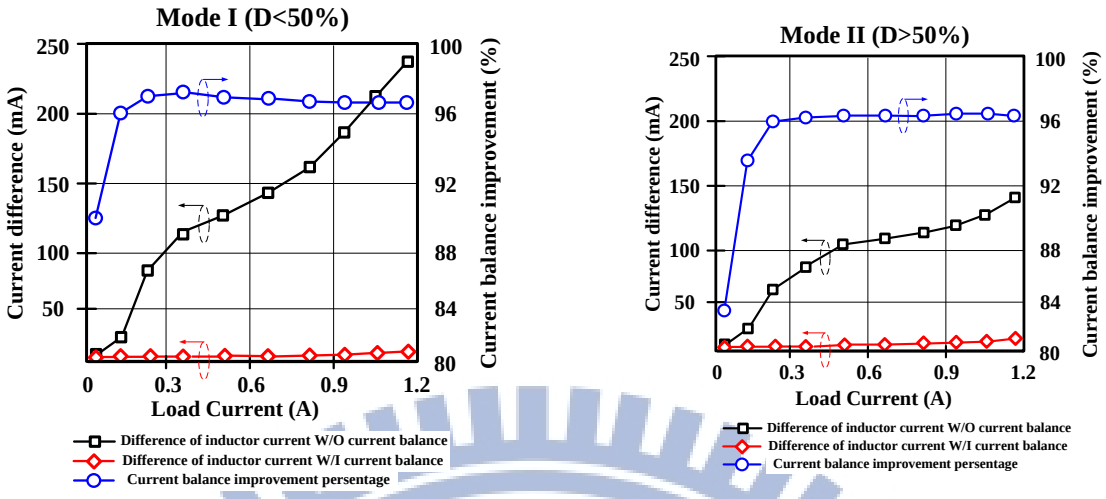



Fig. 24. Measured line transient response

# 4.5 Current Balance Performance Analysis

The statistic summaries of the current balance performance of the Mode I and the Mode II are reported in Fig. 25 (a) and (b), respectively. Owing to mismatch, the difference inductor current of two phases increases dramatically as the increment of load current. With the PRCB technique, the current difference is kept smaller than 10 mA over the whole load range. The current balance improvement percentage, which is the decrement percentage of the difference of inductor current, is over 95% at mostly load conditions. However, the worst case is about 83% at very light load since the offset voltage existing at the input of the OTAs in Fig. 16.




(a) (b)

Fig. 25. Statistic summary of the current balance mechanism in the proposed PRCB technique. (a) Operating in the Mode I. (b) Operating in the Mode II.

# 4.6 Power Conversion Efficiency

Fig. 26 shows the power conversion efficiency. If the load current is smaller than 30mA, the processor can change the converter to the single-phase operation for high efficiency. The efficiency improvement can be 5%. However, the converter with the dual-phase operation has better efficiency at heavy loads. A peak efficiency of 88 % is derived with the load of 1150 mA. Improved efficiencies are 5% and 10% compared to dual-phase operation without current balance function and single-phase operation, respectively.

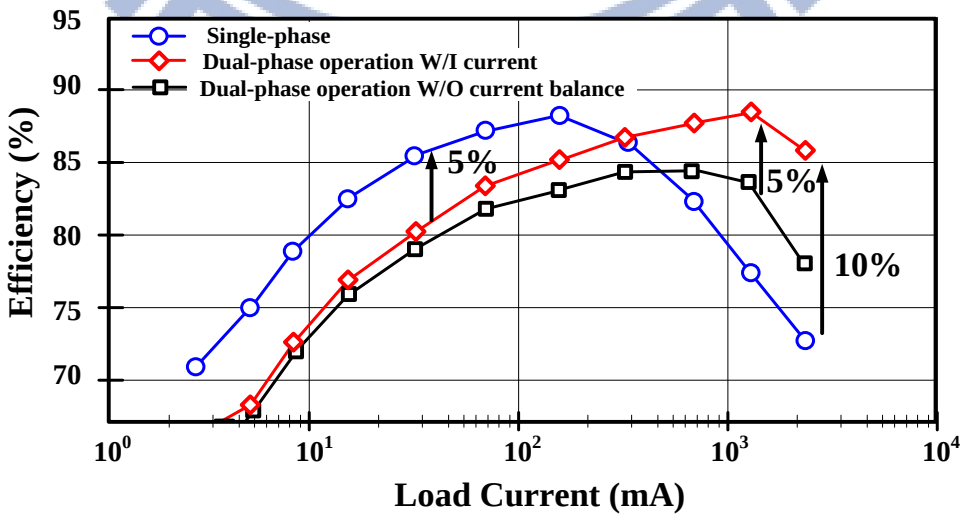



Fig. 26. Power conversion efficiency.

# Chapter 5

# CONCLUSION AND FUTURE WORK

## 5.1 Conclusion

The proposed PRCB technique for the voltage-mode multiphase DC-DC buck converter is presented with single controller to achieve the area-efficient solution. The pseudo-ramp operation can use only one physical saw-tooth to generate two individual control duties for the dual-phase operation. In addition, the current balance mechanism also forms a current-loop, which can dynamically adjust each of duty cycles, to ensure the identical driving capability in the multiphase structure. Moreover, the mode transition operation is activated when the point of duty cycle determination is around 50 % so as to prevent the unwilling mode transitions and help enhance the load transient response. Experimental results demonstrate the different mode operation with the distinct duty cycles. The current in each phase is well balanced under both light load and heavy load conditions with an improvement of 83 % in current balance.

## 5.2 Future Work

This thesis proposes a pseudo-ramp current balance technique to achieve single controller for multiphase operation in voltage-mode DC-DC buck converter. In this work, the operation of dual-phase is unchangeable under light load and heavy load conditions. To get the best efficiency solution under different load current, the number of the operating phase should be decided by the controller. For instance, while the load current is light, only one phase is used. On the other hand, when the load current is large, more phases should be used to cope with. Furthermore, since the current balance tends to slow down the load transient response for accurate current balance, how to improve the transient response with proper current balance performance is good topic of research.

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