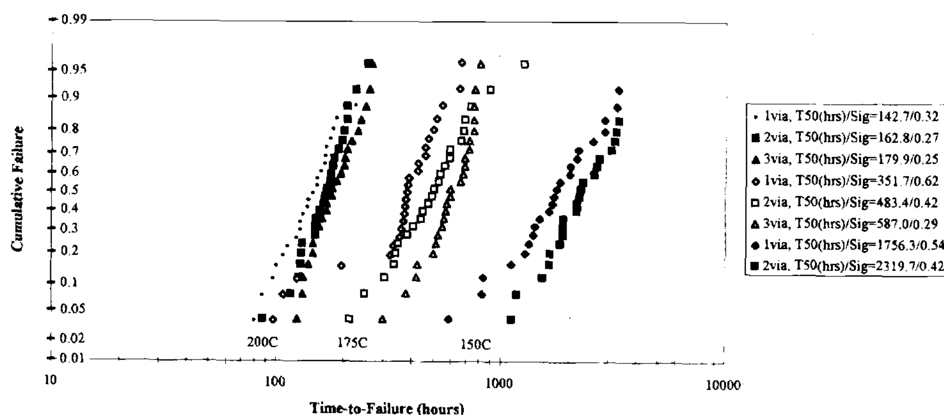



**Fig. 6.** Log normal time-to-failure distribution of set No. 3 test structures with one, two, and three vias. EM performance is a weak function of the number of feeding vias in this case.

REFERENCES

1. L. Ting and C. Graas, in *Proceedings of IEEE International. Reliability Physics Symposium,* p. 326, IEEE (1995).
2. H. S. Rathore, R. G. Filippi, R. A. Wachnik, J. J. Estabil, and T. Kwok, in *Stress-Induced Phenomena in Metallization*, Proceedings of 2nd International Workshop, P. Ho, C. Y. Li, and P. Totta, Editors, p. 165, Am. Inst. Phys., New York (1994).
3. H. A. Le, K. Banerjee, and J. W. McPherson, *Semicond. Sci. Technol.,* **11,** 858 (1996).
4. J. W. McPherson, in *Electronic Materials Handbook,* Vol. 1, p. 887, ASM International, Materials Park, OH (1989).
5. C. K. Hu, R. Rosenberg, and K. N. Tu, in *Stress-Induced Phenomena in Metallization,* in Proceedings of 2nd International Workshop, P. Ho, C. Y. Li, and P. Totta, Editors, p. 195, Am. Inst. Phys., New York (1994).
6. H. B. Huntington and A. R. Grone, *J. Phys. Chem. Solids,* **20,** 76 (1961).
7. V. Vlack, *Elements of Materials Science and Engineering,* p. 135, Addison-Wesley Pub. Co., Reading, MA (1980).

# Plasma Charging Damage and Water-Related Hot-Carrier Reliability in the Deposition of Plasma-Enhanced Tetraethylorthosilicate Oxide

**Y. M. Lin,[a] S. M. Jang,[b] C. H. Yu,[b] T. F. Lei,[a] and J. Y. Chen[b]**

[a]*Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsin-Chu, Taiwan*
[b]*Taiwan Semiconductor Manufacturing Company, Research and Development, Hsin-Chu, Taiwan*

ABSTRACT

This paper presents plasma-enhanced tetraethylorthosilicate oxide process (PETEOS) induced hot-carrier reliability associated with an intermetallic dielectric formed by depositing oxide films from PETEOS, ozone-TEOS, and spin-on glass (SOG), where a single or dual-frequency PETEOS film is deposited as an underlayer followed by an ozone-TEOS deposition for gap filling and a SOG coating for planarization. The impact of PETEOS process conditions such as low- and high-frequency plasma power and PETEOS film thickness on hot-carrier reliability are studied. It is observed that increasing the low- and/ or high-frequency plasma power can improve the film quality and moisture-related hot carrier immunity, but at the expense of plasma charging damage. This plasma charging damage accumulates gradually and finally saturates as the deposition of oxide from PETEOS proceeds. In general, a thick PETEOS layer is desired for improving the moisture-related hot carrier immunity. As a result, there is a trade-off between the plasma charging damage and the moisture-related hot carrier immunity. The plasma charging damage is dominant in large devices and the moisture-related hot-carrier immunity is dominant in small devices.

## Introduction

Plasma-enhanced tetraethylorthosilicate (PETEOS) based oxide films are extensively used as intermetallic dielectrics (IMDs) due to their good step coverages as well as good electrical and mechanical properties.[1] Ozone-TEOS oxide has been a promising IMD candidate for sub-0.5 μm processes. However, owing to substrate dependency, moisture absorption, and cracking tendency of ozone-TEOS oxide, a compressive PETEOS is usually deposited prior to ozone-TEOS deposition. Recently, it is reported that moisture resistance of PETEOS films is improved by increasing the low frequency power but plasma damage is increased.[2]

In very large scale integrated (VLSI) fabrication, the gate oxide is often degraded due to the charge collected at the gate electrode during plasma processing such as polysilicon reactive ion etching (RIE) etch, plasma resist stripping, and plasma etching of aluminum.[3-5] However, little has been reported with regard to charging damage from PETEOS deposition.[6-8] Recently, we reported the improvement of device reliability in single- and dual-frequency PETEOS processes.[5] In this paper, we investigate the impact of PETEOS process conditions such as plasma frequency, plasma power, and PETEOS oxide film thickness on gate oxide integrity as well as hot-carrier aging.

## Experimental

The PECVD-TEOS and subatmospheric CVD (SACVD) $O_3$-TEOS reactor used in this study is implemented in a multichamber single-wafer tool which was described in

Downloaded on 2014-04-28 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

Ref. 19. These PETEOS films are generated by a single (13.56 MHz), or dual (13.56 MHz and 350 KHz), radio frequency (RF) supply. TEOS and oxygen were used as reactants and the deposition temperature was set at 400°C. PETEOS oxide film was deposited to 0.1~0.3 μm, followed by an ozone-TEOS deposition at 400°C without plasma enhancement. Spin-on-glass (SOG) was then applied for planarization. Finally, a plasma-enhanced silane oxide is deposited to terminate the IMD process. Gate oxide thickness is 14.6 or 10 nm. A 0.5 μm complementary metal oxide semiconductor (CMOS) process was used for device fabrication. A complete list of experimental parameters is shown in Table I.

To characterize gate oxide damage from PETEOS oxide deposition, the lifetime of n- and p-MOSFETs with and/or without antenna structure were tested by HP4145B. Large area capacitors were also tested using time dependent dielectric breakdown (TDDB). TDDB characteristics were examined by applying a constant current stress. The total current passing through the oxide is integrated to yield the charge-to-breakdown value, $Q_{bd}$. All measurements were performed at room temperature.

## Results and Discussion

*Comparison of device reliability between single- and dual-frequency PETEOS oxide film.*—The advantages of dual-frequency PECVD for the deposition of IMD films has been reported.[9,10] But the role of plasma on device damage and reliability is not well understood. In this paper, we first compare the device reliability with a PETEOS oxide film deposited by single- and dual-frequency PECVD. The key experimental parameters are described in Table I (rows 1 and 2). The stress of single- and dual-frequency PETEOS films are all $1 \times 10^9$ dyn/cm$^2$. Figure 1 compiles the Weibull plot of charge to breakdown ($Q_{bd}$) for single- and dual-frequency PETEOS IMD capacitor structures. The capacitor area is 0.01 cm$^2$; 30 capacitors were stressed for each of the oxide. The measurement was made using a constant current stress of −6.7 mA/cm$^2$. The lower charge (~0-6 C/cm$^2$) sections of the curves in Fig. 1 refer to the defect-related components and the higher charge sections of the curves represent the intrinsic breakdown strength of the oxides. The devices with dual-frequency PETEOS oxide layers have smaller intrinsic $Q_{bd}$ and more defects than that of single-frequency PETEOS oxide layers. However, our wet etch rate test results show the quality of dual frequency PETEOS oxide films are better than that of single-frequency PETEOS oxide films. The moisture resistance of PETEOS oxides are improved by using dual-frequency PECVD.

In order to investigate the charge trapping characteristics, the Fowler-Nordheim tunneling current stress test was also performed with constant current of −6.7 mA/cm$^2$ for 200 s. n-Channel transistors with gate electrodes 0.7 μm long and 50 μm wide were measured. As shown in Fig. 2, initially all devices show very tight $V_t$ distributions. After constant current stress, devices with dual-frequency PETEOS oxide show more highly scattered $V_t$s than devices with single-frequency PETEOS oxide. Note that

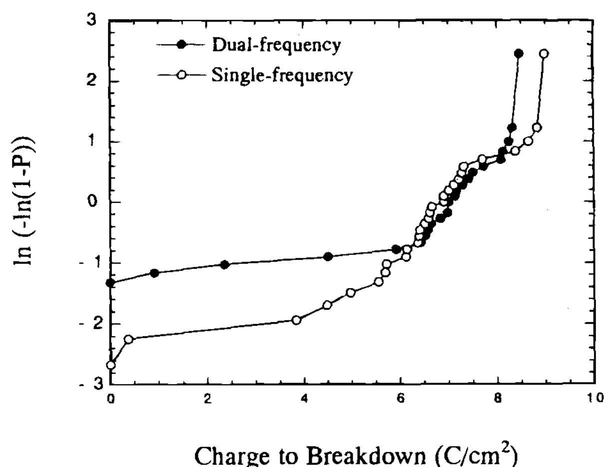



**Fig. 1. Weibull plot of charge to breakdown ($Q_{bd}$) for single- and dual-frequency PETEOS IMD oxide film stressed at a current density of −6.7 mA/cm$^2$.**

after constant current stress, the difference of average mean $V_t$ between single and dual frequency exceeds 1 V.

The importance of an IMD in controlling hot-carrier performance has been reported previously.[11] In this work, we examine the impact of single- and dual-frequency PETEOS oxide layers on the n-MOSFETs hot carrier immunity. Figure 3 compiles device lifetime *vs.* the substrate current per unit gate width for devices with single or dual frequency PETEOS oxidelayers. n-MOSFETs with gate electrode 0.5 μm long and 20 μm wide were stressed at selected $V_{gs}$ and $V_{ds}$ to give maximum substrate current. Device lifetime was determined using a criterion of 10% transconductance (gm) decrease during the stress. The n-MOSFETs with dual frequency PETEOS oxide layers have less hot-carrier immunity.

The moisture resistance of PETEOS oxide layers and their device hot-carrier reliability are inversely affected by processing. Recently, it was reported that charging damage results from PETEOS deposition.[2,4] In this work, we study the transconductance (gm) and saturation current ($Id_{sat}$) degradation in antenna attached to n- and p-MOSFETs stressed at peak substrate current ($I_{sub}$) and gate current ($I_g$), respectively. The antenna structure used in this study is shown in Fig. 4. Figure 5 shows the changes in transconductance and saturation current with stress time. Dual-frequency PETEOS leading enhanced gm and $Id_{sat}$ degradation compared to single-frequency process shows the enhanced interface trap generation and electron

**Table I. List of key experimental parameters.**

| No. | Gate oxide thickness (nm) | Underlayer thickness (μm) | Low-frequency (350 kHz) power | High-frequency (13.56 MHz) power |
|---|---|---|---|---|
| 1 | 14.6 | 0.2 | | H |
| 2 | 14.6 | 0.2 | L | L |
| 3 | 14.6 | 0.15 | M | L |
| 4 | 10 | 0.1 | | L |
| 5 | 10 | 0.1 | | M |
| 6 | 10 | 0.1 | | H |
| 7 | 10 | 0.2 | | H |
| 8 | 10 | 0.3 | | H |

Note: H: high; M: medium; L: low.

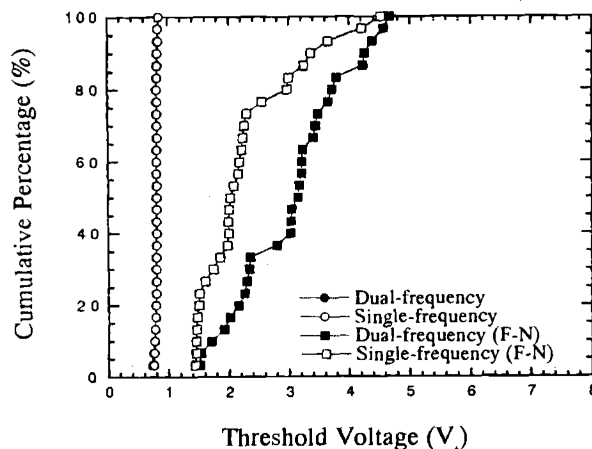



**Fig. 2. Cumulative distribution of threshold voltage before and after constant current (−6.7 mA/cm$^2$) stress.**

Downloaded on 2014-04-28 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

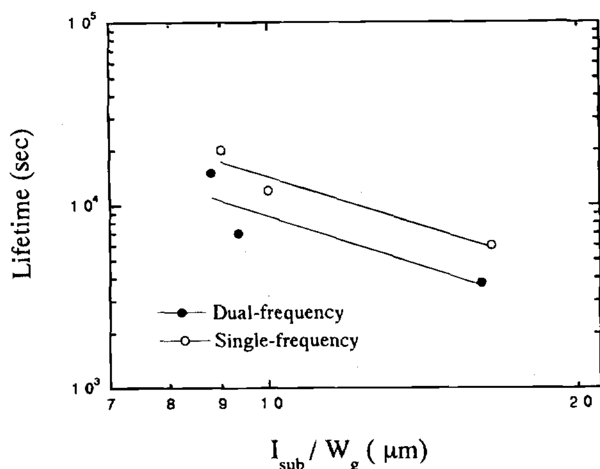
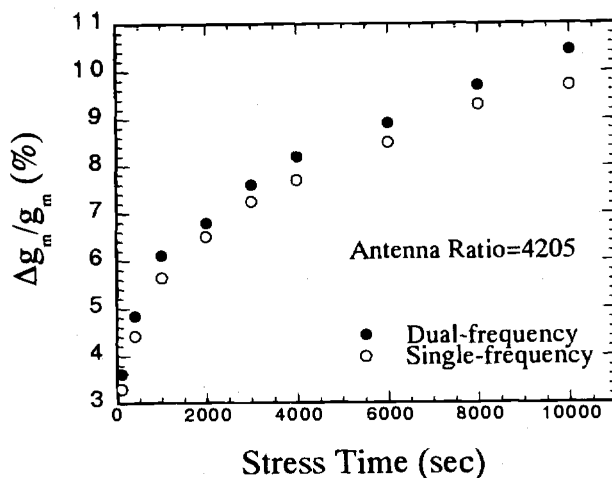



Fig. 3. n-Channel transistor hot-carrier lifetime *vs.* substrate current per unite gate width for single- and dual-frequency PETEOS oxide layer. Each data point is an average of several measurements.

trapping in the dual-frequency process. The addition of RF power at 350 kHz increases low frequency ion bombardment which reduces hydrogen content and improves film density, quality, and moisture resistance.[10] The degraded device hot carrier reliability associated with dual-frequency PETEOS underlayer may be due to the more pronounced plasma damage.

*Low-frequency plasma power effect.*—In the dual-frequency (350 kHz and 13.56 MHz) PECVD, the low-frequency plasma power provides ion bombardment/implantation to densify the film and render an intrinsic compressive stress.[9] We improve the moisture resistance of an PETEOS oxide layer , the charge to breakdown ($Q_{bd}$) of gate oxide and n-MOSFETs hot carrier immunity by increasing the low-frequency power to get the high compressive stress PETEOS oxide film.[2] It was reported that $3 \times 10^9$ dyn/cm$^2$ TEOS-$N_2O$ oxides contain more Si-H bonding at 2260 to 2100 cm$^{-1}$ then $1 \times 10^9$ TEOS-$N_2O$ oxide film.[20] The presence of Si-H bonding in the high stress oxide can enhance the moisture resistance.[21] However, increasing the low frequency plasma power increases the plasma charging damage. Figure 6 shows the cumulative distribution of p-MOSFETs hot-carrier lifetime defined as a 5% increase in saturation current ($Id_{sat}$) with antenna ratio 1051 ~ 4205. PETEOS underlayers were deposited by dual frequency PECVD with varied low-frequency plasma powers set to ~1:2 for comparison. The key experimental parameters are described in Table I



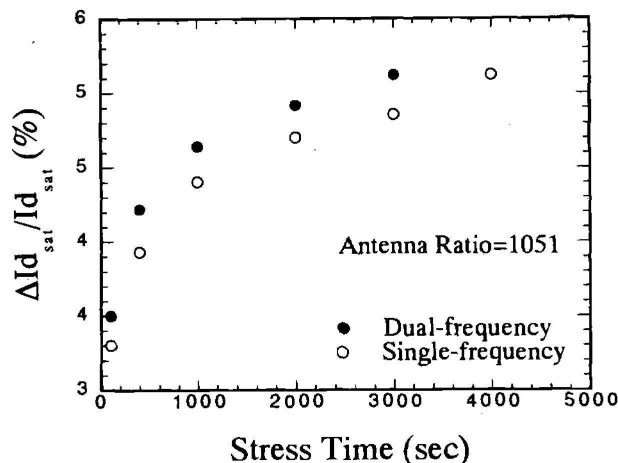




Fig. 5. (a, top) The degradation of transconductance in n-MOSFETs for single- and dual-frequency PETEOS oxide layer. (b, bottom) The degradation of saturation current in p-MOSFETs for single- and dual-frequency PETEOS oxide layer.

(rows 2 and 3). p-MOSFETs with a gate electrode 1.0 μm long and 20 μm wide were stressed at selected $V_{ds}$ and $V_{gs}$ to give the maximum gate current. It is reported that under condition where bulk electron trapping is the dominant hot carrier degradation mechanism (p-MOSFETs stressed at peak $I_g$) the hot-carrier induced failure times depend strongly on antenna ratio.[12] As shown in Fig. 6, a dependence of device lifetime on antenna ratio increases is

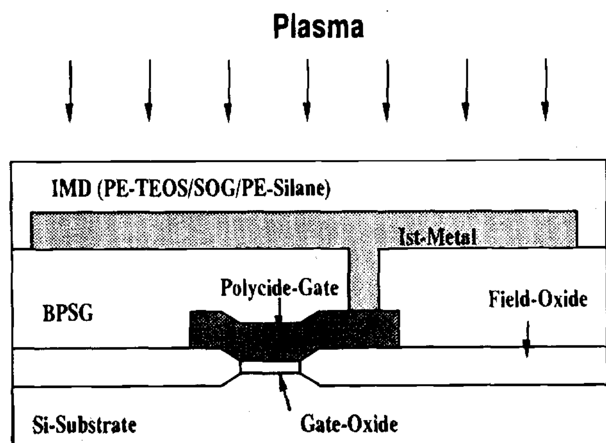



Fig. 4. The cross section of the test structure with a large charge collecting antenna.

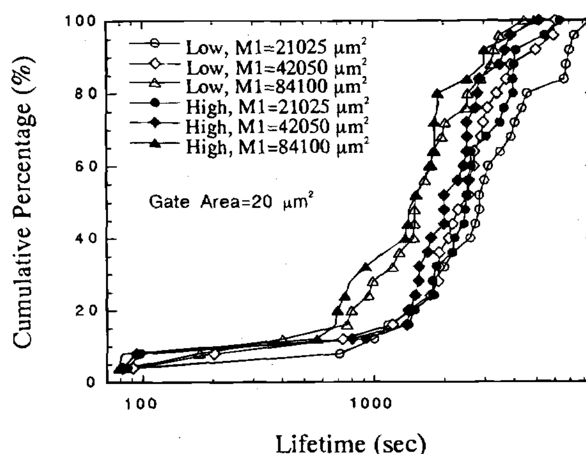



Fig. 6. Cumulative distribution of hot-carrier lifetime of p-MOSFETs without protection diode for single- and dual-frequency PETEOS oxide layer and various antenna areas.

Downloaded on 2014-04-28 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

indicative of plasma charging damage. In all cases, the wafer center suffers more damage than the wafer edge, suggesting nonuniform plasma distribution across the wafer. However, the lifetime of p-MOSFETs without an antenna structure connected is all the same.[2] Clearly, PETEOS deposition has induced plasma damage on devices as manifested by antenna.

Before IMD deposition, the first metal is divided into many small individual conductors and is similar to the overetched poly-gate during RIE poly etching. When the plasma is nonuniform, a spatially nonuniform plasma potential $V_p$ exists and the potential of the floating wafer surface $V_f$ tracks the plasma potential $V_p$.[13] The primary concern with the charging lies in the dc spatial nonuniformity that exists in $V_p$ which is forced to be dropped across the wafer oxide. The reason the voltage changes for different frequencies is that the capacitive reactance of oxide goes like 1/fC. For the ac charging, effect peak to peak voltage swing $V$ across the gate-oxide due to ac charging is[13]

$$V = \left[0.6n\sqrt{\frac{KT}{M}}d_e/(2.2\times10^6)f\right]\left[(1+R_A)/\left(1+\frac{R_A}{R_d}\right)\right] \quad [1]$$

where $n$, $T$, $M$, $d_e$, and $f$ are plasma density, electron temperature, electron mass, gate-oxide thickness, and bias-frequency. $R_A = A_f/A_t$ and $R_d = d_f/d_e$ denote the antenna ratio and thickness ratio, respectively. $A_f$, $A_t$, $d_f$, and $d_e$ are field oxide area, gate oxide area, field oxide thickness, and gate oxide thickness, respectively. An interesting prediction of Eq. 1 is the bias-frequency dependence of ac antenna effect. For a given plasma density, the longer the RF period, the more ions the surface per cycle collects.[13] Consequently, the lower the frequency, the higher the gate oxide degradation from ac charging. Obviously, the plasma charging damage of dual-frequency PECVD is larger than that of single-frequency PECVD.

Hot-carrier reliability degradation caused by plasma charging damage can be simulated as a Fowler-Nordheim type $J \cdot t$ stress that generates interface traps and bulk electron traps.[8] These interface traps can be passivated by moisture-related components during the IMD deposition. At the same time, the bulk traps would be emptied but not removed.[12] As-processed devices (before any stress) show no symptoms of current flow-induced damage. But the latent defects give rise to more defect-related early breakdown in devices with dual frequency PETEOS oxide layers as shown in Fig. 1. As shown in Fig. 2 and 3 harmful effects may be initiated by F-N stressing and hot-carrier stressing which cause electrons to be trapped at the damaged sites and cause degraded hot-carrier immunity, respectively.

*High-frequency plasma power effect.*—PECVD films with improved integrity, *i.e.*, lower porosity and improved bulk density could be deposited by raising high-frequency (13.56 MHz) plasma power.[14] Increased RF (13.56 MHz) power density yielded oxides which were structurally more relaxed and homogeneous. In this work, the impact of high-frequency plasma power on the device reliability is reported for the first time. Single-frequency PETEOS oxide layers were deposited with varied high-frequency plasma power. The key experimental parameters are described in Table I (rows 4, 5, and 6), respectively. Characteristics of charge to breakdown ($Q_{bd}$) shown in Fig. 7 indicates $Q_{bd}$ can be improved by increasing high-frequency plasma power from 325 to 500 W and finally saturates with 675 W. The $Q_{bd}$ measurements were made with a Fowler-Nordheim injection current level of $-5$ mA/cm$^2$ over a gate oxide capacitor of $10^{-4}$ cm$^2$. To characterize the PETEOS quality, thermal desorption spectroscopy (TDS) was used to determine the amount of $H_2O$ in the films. Our TDS data (not shown) shows the $H_2O$ in the films can be lessened by increasing high-frequency plasma power. Table II lists the normalized n-MOSFETs hot-carrier lifetime for varied high-frequency plasma power and PETEOS oxide layer thickness. For every

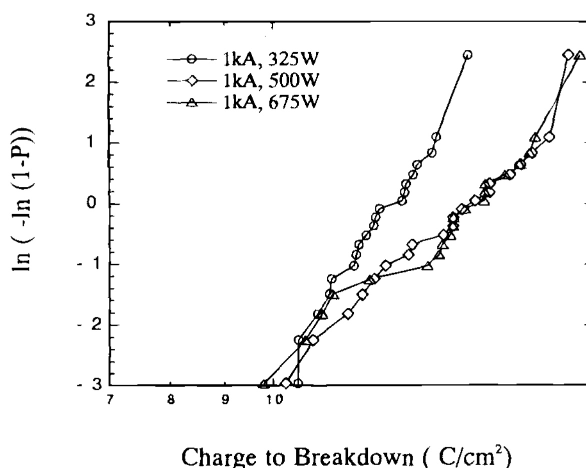



**Fig. 7. Weibull plot of charge to breakdown ($Q_{bd}$) of capacitors with varied high-frequency power single-frequency PETEOS IMD oxide layer.**

process condition, 20 devices were stressed at selected $V_{gs}$ and $V_{ds}$ which give maximum substrate current. Compared with devices with high-frequency plasma power of 350 and 500 W, the hot-carrier lifetime can be prolonged by increasing the high-frequency plasma power. When the power is raised to 625 W, the hot-carrier lifetimes are degraded. According to previous discussions and Ref. 14, it is speculated that plasma charging damage exists and moisture resistance of the films is degraded if high-frequency plasma power is increased over some critical value. Figure 8 compiles the hot-carrier lifetime of p-MOSFETs with an antenna ratio of about 1810 across the wafer for different high-frequency plasma power. p-MOSFETs with gate electrodes 0.5 μm long and 9.0 μm wide were stressed at $V_{ds} \sim -5.9$ V and $V_{gs} \sim -1.4$ V giving the peak gate current. For the devices sited at wafer edge, the trend of p-MOSFET is opposite to that of n-MOSFETs of Table II, which is consistent with Ref. 2. This phenomenon may suggest the moisture resistance of 675 W PETEOS oxide layer are degraded. Especially only p-MOSFETs with 675 W PETEOS show the typical nonuniform radial dependence of antenna effect. Clearly, increasing high-frequency plasma power has induced plasma charging damage. According to Eq. 1, the peak to peak voltage swing $V$ across the gate oxide is proportional to the plasma density $n$. The high-frequency plasma power gives a stable discharge, generates part of the reactive species, and assures effective coupling to the substrate.[9] Consequently, raising

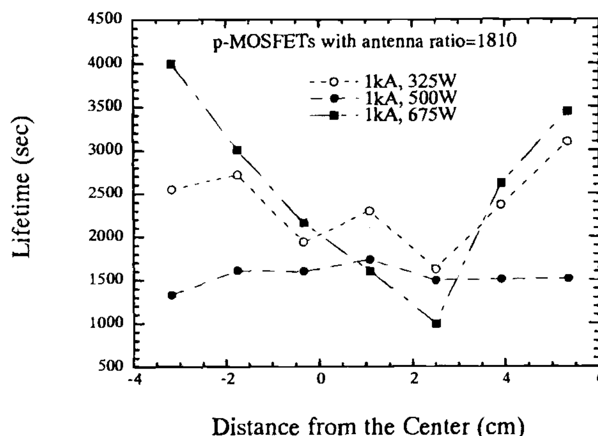



**Fig. 8. Radial dependence of p-MOSFETs hot-carrier lifetime with antenna ratio 1810 for varied high-frequency plasma power.**

Downloaded on 2014-04-28 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

the high-frequency plasma power can increase the plasma density to induce higher plasma damage.

*PETEOS oxide thickness effect.*—Conventional plasma charging damage is generated at the beginning of IMD deposition and is prevented by the as-deposited underlayer quickly. However as the deposition of PETEOS underlayer proceeds, another plasma charging mechanism resulted from photoconduction occurs and dominates. The equation for photoconduction of vacuum ultraviolet (VUV) photons is[4,15]

$$I = qF\mu\tau V/L^2 \qquad [2]$$

where $q$ is the electron charge, $F$ is the intercepted photon flux, $\mu$ is the electron mobility, $\tau$ is the electron lifetime, $V$ is the applied voltage, and $L$ is the distance between the electrodes. This equation predicts that the plasma charging damage will saturate as the deposition of PETEOS underlayer proceeds. To confirm this new plasma damage mechanism, we also characterized the radial dependence of p-MOSFETs lifetime for varied thickness of PETEOS oxide. The key experimental parameters are described in Table I (rows 6, 7, and 8). p-MOSFETs with gate electrodes 0.5 μm long and 9.0 μm wide and with antenna ratio ~1810 were stressed at $V_{gs}\sim -1.4$ V and $V_{ds}\sim -5.9$ V to give the peak gate current where bulk electron trapping is the dominant hot-carrier degradation machanism.

The hot-carrier reliability of p-MOSFETS are significantly degraded by plasma charging damage.[12,16] The higher the plasma charging damage, the shorter the lifetime of p-MOSFET. As shown in Fig. 9, the plasma charging damage resulting from nonuniform plasma distribution is the worst at the wafer center. In the meanwhile, the accumulated plasma charging damage increases gradually and saturates finally as the deposition of PETEOS underlayer proceeds.

There are two competitive mechanisms during the deposition of PETEOS oxide. In general, in order to improve the water-related reliability, the thickness of PETEOS underlayer are as thick as possible. However, as the deposited thickness of PETEOS increases, the accumulated plasma charging damage is higher. Consequently, in order to determine which mechanism dominates, n-MOSFET without antenna structure are also stressed at selected $V_{gs}$ and $V_{ds}$ to give maximum substrate current. Twenty devices are stressed for every condition. The key experimental parameter are described in Table I (rows 6, 7, and 8). Results are listed in Table II. As shown in Table II, the thicker the thickness of PETEOS, the more robust is the n-MOSFET hot-carrier reliability. Clearly, in n-MOSFETs the improvement of water-related hot-carrier reliability is the dominant mechanism. It may be attributed to: (*i*) n-MOSFETs hot-carrier reliability is hardly affected by the plasma charging effect,[12] and (*ii*) IMD affects the short channel device more strongly.[17]

**Table II. List of normalized n-MOSFETs lifetime.**

| Underlayer thickness (μm) | High-frequency (13.56 MHz) power | Normalized n-MOSFETs lifetime |
|---|---|---|
| 0.1 | L | 1 |
| 0.1 | M | 1.405 |
| 0.1 | H | 0.8 |
| 0.2 | H | 1.126 |
| 0.3 | H | 1.829 |

Note: H: high; M: medium; L: low.

To check the previous assumption, $Q_{bd}$ was measured by the time-dependent dielectric breakdown (TDDB) technique using constant-current stress of −5 mA/cm². The area of the capacitor with varied thickness of PETEOS underlayer is 0.01 cm². The key experimental parameters are described in Table I (rows 6, 7, and 8). Figure 10 shows the $Q_{bd}$ for capacitors with varied thickness of PETEOS oxide. The trend of Fig. 10 is very different from that of Fig. 9. As the deposition of PETEOS oxide proceeds, the $Q_{bd}$ is degraded at first and eventually is partially recovered. When the thickness of PETEOS oxide increases by 0.1 to 0.2 μm, the plasma charging damage degrades the $Q_{bd}$ although the water-related hot-carrier reliability is improved by increasing the thickness of the PETEOS oxide. As shown in Fig. 9, the plasma charging damage of 0.2 and 0.3 μm thick PETEOS oxide are nearly the same or larger than that of 0.1 μm thick PETEOS oxide. Hence, the $Q_{bd}$ is improved when the thickness of PETEOS oxide increases by 0.1 to 0.3 μm. However, the degraded $Q_{bd}$ of 0.2 and 0.3 μm compared to that of 0.1 μm thick PETEOS underlayer shows the plasma charging damage is the dominant mechanism in large area devices.

Figure 11 compiles the radial dependence of $Q_{bd}$ for 0.3 μm thick PETEOS oxide showing, which plasma charging damage is worst. As shown in Fig. 11, nonuniform the radial dependence of $Q_{bd}$ shows that a nonuniform plasma exists. It shows that for large area devices, plasma charging damage is still severe even though devices are attached to no antenna structures.

Figure 12 shows the shift of gate voltage ($\Delta V_g$) under the constant current (−5 mA/cm²) stress for varied thickness of PETEOS underlayer. It is seen that the higher the plasma charging damage, the larger the electron trapping rate. As a result, more bulk electron traps lead to smaller $Q_{bd}$, which is consistant with the physical damage model.[18]

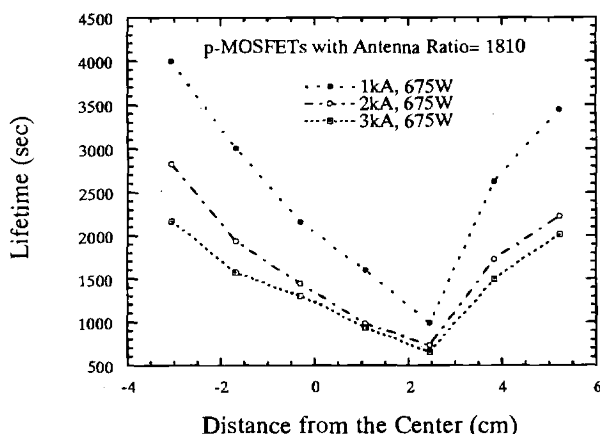



**Fig. 9. Radial dependence of p-MOSFETs hot-carrier lifetime with antenna ratio 1810 for varied single-frequency PETEOS oxide film thickness.**

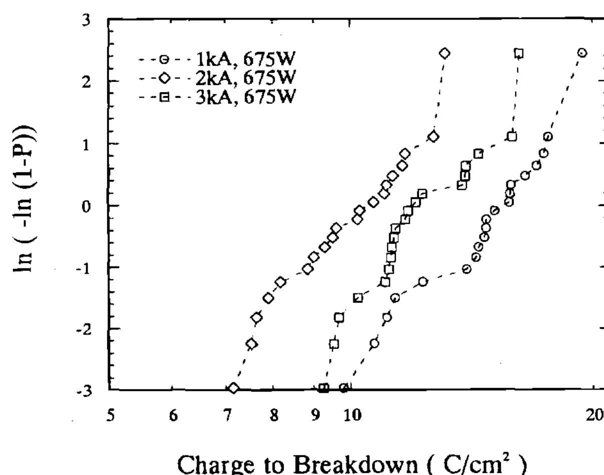



**Fig. 10. Radial dependence of charge to breakdown ($Q_{bd}$) for varied single-frequency PETEOS oxide layer film thickness.**

Downloaded on 2014-04-28 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

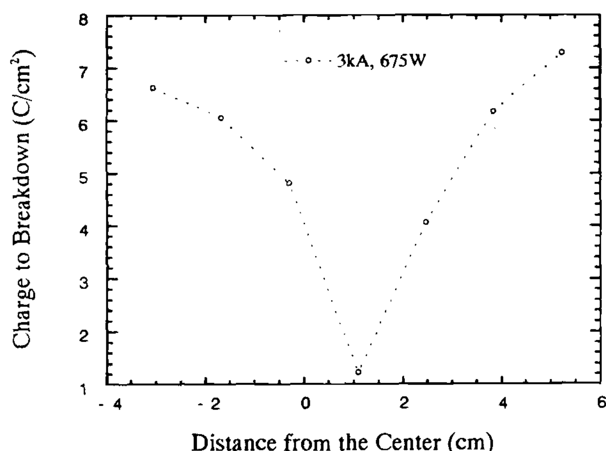



**Fig. 11. Radial dependence of charge to breakdown ($Q_{bd}$) for 0.3 μm 625 W single-frequency PETEOS oxide layer.**

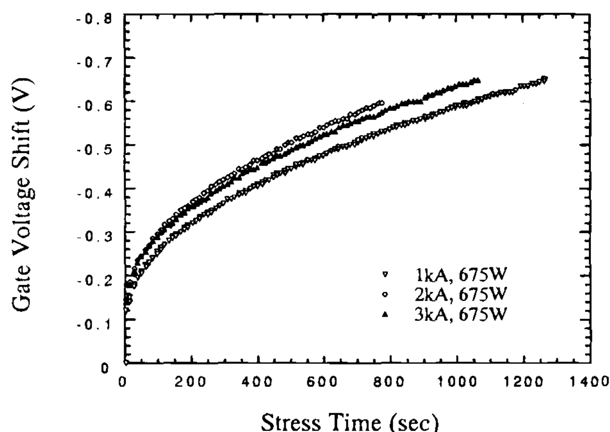



**Fig. 12. Gate voltage shift ($\Delta V_g$) under the constant current (−5 mA/cm²) stress for varied PETEOS oxide film thickness.**

## Conclusions

We have studied the impact of elements of PETEOS processes factors such as plasma frequency, plasma power, and the thickness of the PETEOS films on device reliability. Increasing the high-frequency power can yield oxides which are structurally relaxed and homogeneous with improved oxide quality and n-MOSFETs water-related hot-carrier immunity at the expense of plasma charging damage. Compared with increasing high-frequency power, increasing the low-frequency plasma power can increase stress to more effectively improve the film quality and n-MOSFETs water-related hot carrier immunity. However, increasing low- and/or high-frequency also induces plasma charging damage. This plasma charging damage will accumulate gradually and finally saturates as the deposition of PETEOS proceeds. However, in general a thick PETEOS underlayer is desired to improve the n-MOSFETs water-related hot-carrier immunity. As a result, there is a trade-off between the plasma charging damage and the water-related hot-carrier immunity. At the same time, the plasma charging damage is dominant in large devices and the water-related hot-carrier immunity is dominant in small devices.

## Acknowlegment

This research was supported in part by the Republic of China National Science Council (ROC NSC) under contract No. NSC-86-2215-E009-041.

Manuscript submitted Aug. 13, 1996; revised manuscript received April 14, 1997.

*National Chiao Tung University assisted in meeting the publication costs of this article.*

REFERENCES

1. G. W. Hills, A. S. Harrus, and M. J. Thomas, *Solid State Technol.*, **127** (1990).
2. Y. M. Lin, S. M. Jang, C. H. Yu, and T. F. Lei, *This Journal*, **144** (Aug., 1997).
3. W. M. Greene and C. K. Lau, *ibid.*, **139**, 2948 (1992).
4. S. Fang and J. P. Mcvittie, *IEEE Trans. Electron Devices*, **ED-41**, 1034 (1994).
5. H. Shin, C.-C. King, T. Horiuchi, and C. Hu, *IEEE Electron Device Lett.*, **EDL-12**, 404 (1991).
6. S. Hirao, T. Sugiyama, T. Yoshida, K.Yano, and N. Nomura, in *Proceedings of International Conference on Solid State Devices and Materials*, p. 826 (1993).
7. K. P. Cheung and C.-S. Pai, *IEEE Electron Device Lett.*, **EDL-16**, 220 (1995).
8. S. M. Jang, Y. M. Lin, L. Chen, C. L.Chang, C. H. Yu, and T. F. Lei, in *Proceedings of Second International Dielectric for ULSI Multilevel Interconnection Conference (DUMIC)*, p. 167 (1996).
9. E. P. van de Ven, I.-W. Connick, and A. S. Harrus, in *Proceedings of IEEE 11th International VLSI Multilevel Intrerconnection Conference (VMIC)*, p. 194, IEEE (1990).
10. P. Lee, B. Pang, J. Huang, C. Ngai, and D. Cheng, *ibid.*, p. 299 (1994).
11. N. Shimoyama, K. Machida, J. Takahashi, K. Murase, K. Minegishi, and T. Tsuchiya, *IEEE Trans. Electron Devices*, **ED-40**, 1682 (1993).
12. K. R. Mistry, B. J. Fishbein, and B. S. Doyle, in *Proceedings of the 28th IEEE International Reliability Physics Symposium*, p. 42, IEEE (1994).
13. K. P. Cheung and C. P. Chang, *J. Appl. Phys.*, **75**, 4415 (1994).
14. J. D. Chapple-Sokol, W. A. Pliskin, and R. A. Conti, *This Journal*, **138**, 3723 (1991).
15. S. M. Sze, *Physics of Semiconductor Devices*, p. 746, John Wiley & Sons, Inc., New York (1981).
16. Y. -H. Lee, L. Yau, R. Chau, E. Hansen, B. Sabi, S. Hui, P. Moon, and G. Vandentop, in *Tech. Dig. Int. Electron Devices Meet.*, 65 (1992).
17. C. Jiang, C. Hu, C. H. Chen, and P. N. Tseng, in *Proceedings of the 30th IEEE International Reliability Physics Symposium*, p. 122 (1992).
18. P. P. Apte and K. C. Saraswat, *IEEE Trans. Electron Devices*, **ED-41**, 1595 (1994).
19. S. M. Jang, Y. M. Lin, P. Lee, L. M. Liu, C. H. Yu, T. F. Lei, and M. S. Lin, in *SPIE Proc. Vol.*, **2636**, p. 307 (1995), SPIE-Int. Soc. Opt. Eng.
20. S. Robles, E. Yieh, and B. C. Nguyen, *This Journal*, **142**, 580 (1995).
21. K. Machida, N. Shimoyama, J. Takahashi, E. Arai, and N. Yabumoto, in *Proceedings of the 10th International IEEE VLSI Multilevel Interconection Conference (VMIC)*, p. 103, IEEE (1993).

Downloaded on 2014-04-28 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).