

# 新型微小高 Q 值電感之分析、設計及模型建立

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## 摘要

本論文因應無線通訊射頻電路對高品質電感的需求，提出有別於傳統架構，極具創意之高 Q 值，小面積電感。當今 CMOS VLSI 0.18um technology 提供 6 層金屬和一層多晶矽，使得電感設計有更多發揮的空間，想要設計出 Q 值高，面積小之電感不再是夢想。Q 值、L 值及面積是電感之重要參數，一般由晶圓廠提供之電感 Q 值不高又佔面積，以 TSMC 0.18um 1P6M technology 為例提供的是方形電感， $Q < 8$ ， $\text{Area} > 0.0467\text{mm}^2$ ，UMC 0.18um 1P6M 提供的是圓形電感， $Q < 19.41$ ， $\text{Area} > 0.06\text{mm}^2$ 。下線實作部分 (tapeout)，TSMC 及 UMC 都有實作經驗，但以 UMC 為主，最後有做本案設計之電感與 UMC 電感之比較。另外，本文亦提供相當準確之電感模型，並與量測結果做比較，以利電路設計者參考使用。

# Analysis, Design and Modeling of Novel Miniature High Quality Factor Inductors for 0.18 $\mu$ m RF CMOS Technology

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## Abstract

Several innovative RF CMOS on-chip inductor structures are proposed in this thesis. We take advantage of modern VLSI technology with multi-metal layers utilization, for example, TSMC 0.18 $\mu$ m 1P6M process supports one polysilicon and six metal layers, where the metal consists of aluminum alloy. Rather than the typical inductors, our designing inductors that achieve much higher quality factor with smaller area at the equal inductance level can be easily integrated with other RF IC devices. The thesis also offers accurate inductor pi models that are comparable with the measurement results. These accurate inductor models can be applied to the broadband circuit design.

## Acknowledgements

First and foremost I would like to thank my advisor, Prof. Yu De Lin, for giving me the opportunity of researching such an interesting subject. I have learned so much knowledge about the concept of VLSI circuit design and fabrication by devotion to this project. I also have to appreciate to the Ansoft engineer, Nilson Yu, who taught me how to easily and correctly simulate monolithic RF inductors by Ansoft HFSS.

Last, certainly but not least, I am gratefully indebted to my parents and family for their spiritual support and everlasting love.

I have done the best of my limited ability. I wish there is some contribution to the semiconductor industry and academia from my hard working effort.



# Contents

摘要	i
Abstract	ii
Acknowledgements	iii
Contents	iv
<b>Chapter 1 Introduction</b>	<b>1</b>
1.1 Overview	1
1.2 Thesis Organization	2
<b>Chapter 2. Inductor Design and Characterizations</b>	<b>3</b>
2.1 Introduction	3
2.2 Design Method	9
2.3 Measurement Results	16
2.4 Summary	26
<b>Chapter 3 Substrate Effect Decoupling</b>	<b>28</b>
3.1 Introduction	28
3.2 Novel Ideas Presentation	31
3.3 Measurement Results	34
3.4 Summary	37
<b>Chapter 4 Inductor Modeling</b>	<b>38</b>
4.1 Introduction	38
4.2 Modeling In Contrast to Measurement Results	41



<b>Chapter 5 Application --- A 5.2GHz Oscillator</b>	<b>49</b>
5.1 Oscillation Theory	49
5.2 Differential Stimulation to Enhance Inductor Quality	52
5.3 Circuit Performance Demonstration	53
<b>Chapter 6. Conclusions &amp; Future Work</b>	<b>56</b>
<b>References</b>	<b>57</b>



# Figure Captions

## Chap 2

Figure 2.1-1 Cross-sectional view of metal and polysilicon layers in a typical IC process. ....	3
Figure 2.1-2 TSMC inductor structure. ....	4
Figure 2.1-3 UMC inductor structure. ....	4
Figure 2.1-4 (a) All of the inductor loss and coupling, (b) lumped element circuit model of single turn (see Long [7]), (c) simplified PI model. ....	5
Figure 2.1-5 (a) Electric coupling between adjacent metal wires, (b) magnetic coupling between two adjacent metal wires, (c) substrate noise coupling effect, (d) magnetic coupling between inductor and substrate is equivalent to a transformer action, (e) right angle bends can be mitered to minimize the discontinuities, (f) most current flow is confined to the conductor surface at giga hertz frequency. ....	6
Figure 2.2-1 The signal flow diagram of a (a) single ended, (b) differentially driven inductor. ....	9
Figure 2.2-2 (a) Asymmetrical inductor, (b) capacitance distribution along the path, x represents distance, (c) symmetrical inductor, (d) capacitance distribution, x represents both distance and voltage. ....	10
Figure 2.2-3 (a) Symmetrical inductor including interwinding capacitance, (b) circuit model of inductor, (c) voltage profile through the inductor. ....	11
Figure 2.2-4 Stacked inductor and its model. ....	11
Figure 2.2-5 (a) Layout description, (b) 3D view, (c) top view, (d) lateral view. ....	12
Figure 2.2-6 (a) Layout description, (b) 3D view, (c) top view, (d) lateral view. ....	13
Figure 2.2-7 (a) Layout description, (b) 3D view, (c) top view, (d) lateral view. ....	14
Figure 2.2-8 Comparison of inductor quality between with and without overlapping types. ....	15
Figure 2.2-9 (a) 3D view, (b) lateral view. ....	15

Figure 2.3-1 The de-embedding procedure as well as the extraction of Q and L. ....	16
Figure 2.3-2 Electric coupling (a) stacked metal type, (b) non-overlapping type. ....	22

### Chap 3

Figure 3.1-1 Substrate coupling in a mixed signal SOC. ....	28
Figure 3.1-2 (a) Circuit model for illustrating the effects of negative magnetic coupling between a spiral inductor and solid ground shield, (b) closed photo of the patterned ground shield. ....	29
Figure 3.1-3 Inserting a patterned ground shield beneath an inductor makes capacitive coupling more severe, (a) without a PGS, (b) with a PGS. ....	30
Figure 3.1-4 Inductor quality improved by inserting a PGS. ....	31
Figure 3.2-1 Schematic representation of substrate effects. Eddy currents are induced magnetically, and displacement currents are injected from the conductors to the substrate by capacitive coupling. ....	31
Figure 3.2-2 (a) Physical layout, (b) enlargement of the magnetic decoupler...	32
Figure 3.2-3 (a) Simplified pattern of a magnetic decoupler for simulation, (b) current distribution in substrate without a magnetic decoupler, (c) current distribution in substrate with a magnetic decoupler. ....	32
Figure 3.2-4 Performance improvements, where blue lines signify that a magnetic decoupler is added, (a) the quality factor, (b) the inductance value. ....	33

### Chap 4

Figure 4.1-1 (a) The trend of inductor quality factor can be divided into three sections, such as linear, saturation and degradation regions, (b) the inductance value varies with frequency. ....	39
Figure 4.1-2 RL series model. ....	39

## Chap 5

Figure 5.1-1 A closed loop form of oscillatory circuits: a small noise signal $a_n$ is generated in the loop externally or internally. Letter ‘a’ signifies incident waves, and letter ‘b’ signifies reflective waves. ....	49
Figure 5.1-2 Negative resistance realization: (a) topology, (b) equivalent small signal model, (c) Smith chart test. ....	49
Figure 5.1-3 An ideal resonator is realized by a parallel LC tank, (a) schematic view, (b) S- parameter frequency response, where the extremely small return loss and the large attenuation are obtained at resonance. ....	51
Figure 5.2-1 Quality factors of single ended and differentially driven inductor tapeout in TSMC: (a) sym_od210um_3m2t, (b)sym_od210um_3m3t, (c)sym_od210um_3m4t, (d) sym_od180um_3d3t_nol. ....	52
Figure 5.2-2 Quality factors of single ended and differentially driven inductor tapeout in UMC: (a) sym_od210um_3m3t, (b)sym_od210um_3m4t. ....	53
Figure 5.3-1 A 5.2 GHz Oscillator schematic view, (a) common configuration, (b) two inductors in series are replaced by only one of the symmetrical type. ....	54
Figure 5.3-2 A 5.2 GHz Oscillator, (a) transient response (single ended), (b) transient response (differential mode), (c) spectrum analysis (differential mode), (d) phase noise. ....	55



# Table Captions

## Chap 2

Table 2.3-1 Measurement data of the inductors taped out in TSMC 0.18um 1P6M process. ....	21
Table 2.3-2 Measurement data of the inductors taped out in UMC 0.18um 1P6M process. ....	26
Table 2.4-1 Comparison with UMC's inductors. ....	27

## Chap 3

Table 3.4-1 Measurement data of the inductors taped out in UMC 1P6M Process. ....	37
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## Chap 4

Table 4.1-1 The guide of inductor model tuning. ....	40
Table 4.2-1 The component values of the inductor compact PI model (by TSMC 0.18um 1P6M process). ....	45
Table 4.2-2 The component values of the inductor compact PI model (by UMC 0.18um 1P6M process). ....	48

