Chapter 1 Introduction

1.1 Overview

The topics related to system-on-chip (SOC) have surged with the growing demand for radio frequency integrated circuits (RF IC's) recently. Modern Complementary Metal Oxide Semiconductor (CMOS) technology prevails for low cost over any other compound semiconductor process (GaAs, SiGe). However, implementing RF circuits on lossy silicon substrate integrated with other baseband circuits is such a tough work. Substrate noise i.e. substrate coupling is a serious problem due to the low resistivity of silicon. Eddy current induced by the magnetic coupling, ohmic and displacement current induced by the electrical coupling, degrade the quality factor and produce redundant power dissipation. Isolating or decoupling the inductor from the substrate can enhance the overall performance and simplify modeling. Yue and Wong [1] inserted a pattern ground shield underneath inductors as a typical approach of decoupling. Meanwhile, the stray capacitance also increases to diminish the self-resonance frequency. Some unprecedented concepts are proposed to remove the substrate effect in this thesis.

Moreover, the enormous demand of handheld wireless communication ICs is stringent in terms of low cost, low supply voltage, low power consumption, low noise, high frequency of operation and low distortion. In addition, consumers prefer the portable equipment as lighter and smaller as possible. RF inductors provided by foundries, either conventional rectangular or circular structure, occupy extremely large chip area than any other passive or active devices, but with a poor quality factor. Designing a small and high Q

inductor has become a very popular topic today. Danesh and Long et al [2][3] proposed symmetrical property that can improve Q because of the equal distribution of stray capacitance from both the entrance orientations. Zolfaghari et al [4] and Tang et al [5] suggested that three-dimension design with multi-metal layers utilization can save much area. Some extraordinary inductor structures are presented that maintains symmetry and three-dimension characteristic.

Accurate inductor models desired by circuit designers can characterize each coupling effect for wide band application. Nevertheless, more accuracy needs more CPU run time. J. Gil and H. Shin [6] proposed a modified PI model to elevate accuracy. Actually, compact PI model can match the measurement curve appropriately by proper tuning, thus the modification maybe not necessary.

1.2 Thesis Organization

The rest of the thesis is organized as: Chapter 2 researches and analyzes the loss and coupling effects introduced into the inductors. The novel inductor structures design with respect to suppressing the unwanted factors is illustrated at this chapter. Our inductor performance is compared with those of UMC at the ending. Chapter 3 describes the substrate effects in detail and what can be done to remove them as possible at all. Chapter 4 depicts the accurate PI models in contrast to the measurement data. Chapter 5 displays a LC tank oscillator with excellent phase noise performance for an application of high Q inductor by circuit simulation. The conclusions of the work are finally drawn in Chapter 6.

Chapter 2 Inductor Design and Characterizations

2.1 Introduction

Figure 2.1-1 shows a profile of metal and polysilicon layers in a customary IC process. Typical Inductors provided by foundries are either rectangular or circular and only use the top metal. Next page displays the information about inductors supplied by Taiwan Semiconductor Manufacturing Corporation (TSMC) and United Manufacturing Corporation (UMC), respectively.

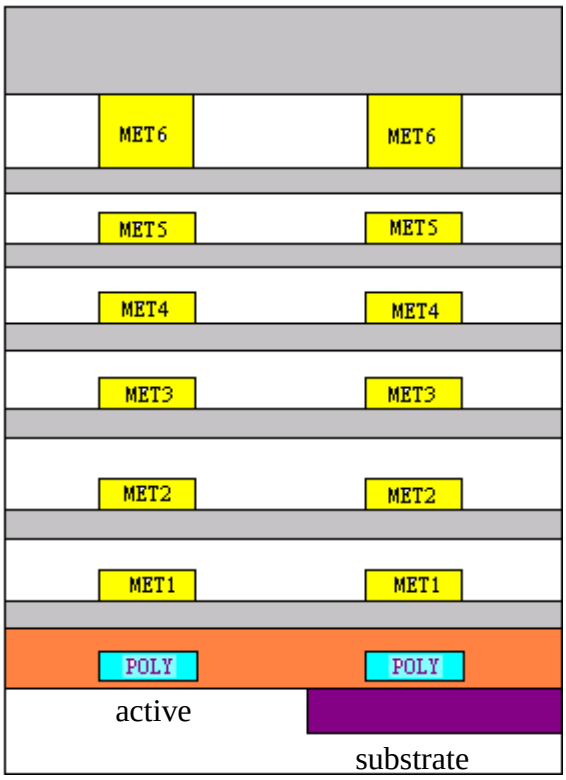
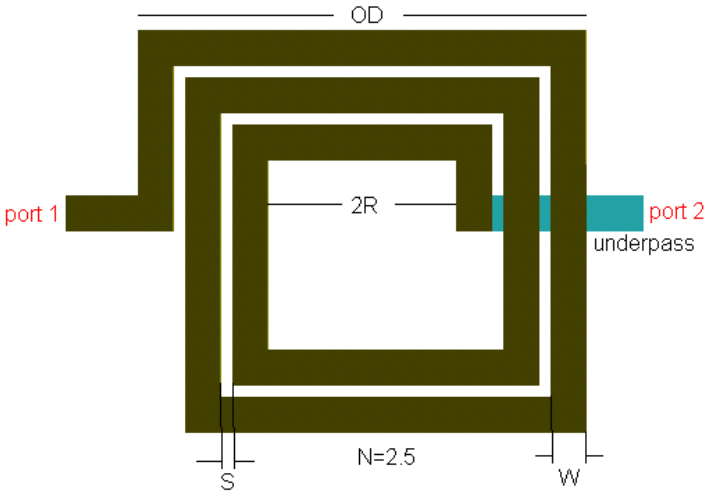


Figure 2.1-1 Cross-sectional view of metal and polysilicon layers in a typical IC process.

TSMC 0.18um 1P6M technology:



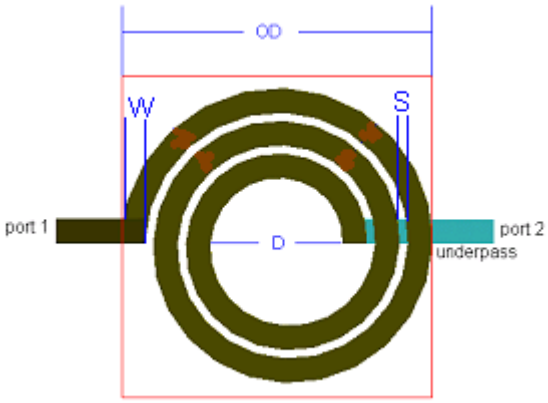
OD: outer diameter
N: number of coil turns
W: metal width of top metal
S: metal space of top metal
R: radius inside inner coil.
Port 1: input port
Port 2: output port

Figure 2.1-2 TSMC inductor structure.

Effective Area $A_{eff} = (OD)^2 = \{2 \times [R + W \times (N + 0.5) + S \times (N - 0.5)]\}^2$

Where R=60um W=15um S=1.5um, Q is lower than 8.5, L ranges from 2 to 18 nH, the area is larger than 0.0467mm^2.

UMC 0.18um 1P6M technology

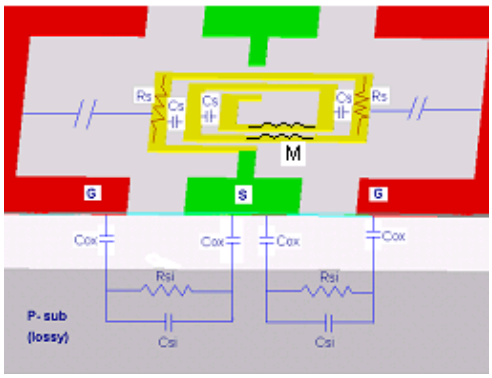


OD: outer diameter
N: number of coil turns
W: metal width of top metal
S: metal space of top metal
D: inner diameter
Port 1: input port
Port 2: output port

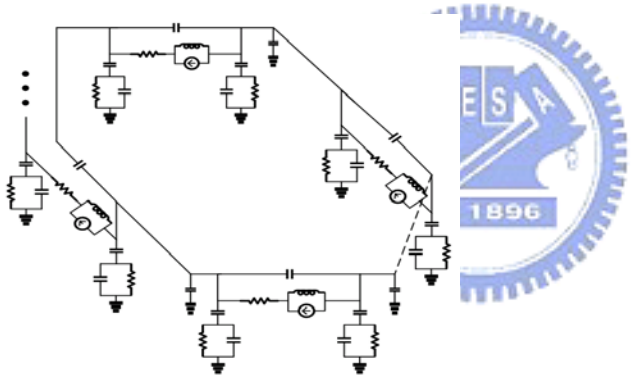
Figure 2.1-3 UMC inductor structure.

Effective Area $A_{eff} = (OD)^2 = \{D + 2 \times [W \times (N + 0.5) + S \times (N - 0.5)]\}^2$

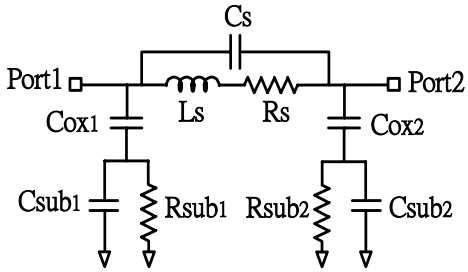
Where W≦25um, S=2um, Q is lower than 19.4, L ranges from 0.98 to 10.51nH, the area is larger than 0.06mm^2. Although the inductors of UMC have higher quality, they are substantially cumbersome.



(a)



(b)



(c)

Figure 2.1-4 (a) All of the inductor loss and coupling, (b) lumped element circuit model of single turn (see Long [7]), (c) simplified PI model.

Figure 2.1-4 illustrates the entire inductor loss and coupling mechanism (see Long [7]). The following explains each of them in detail.

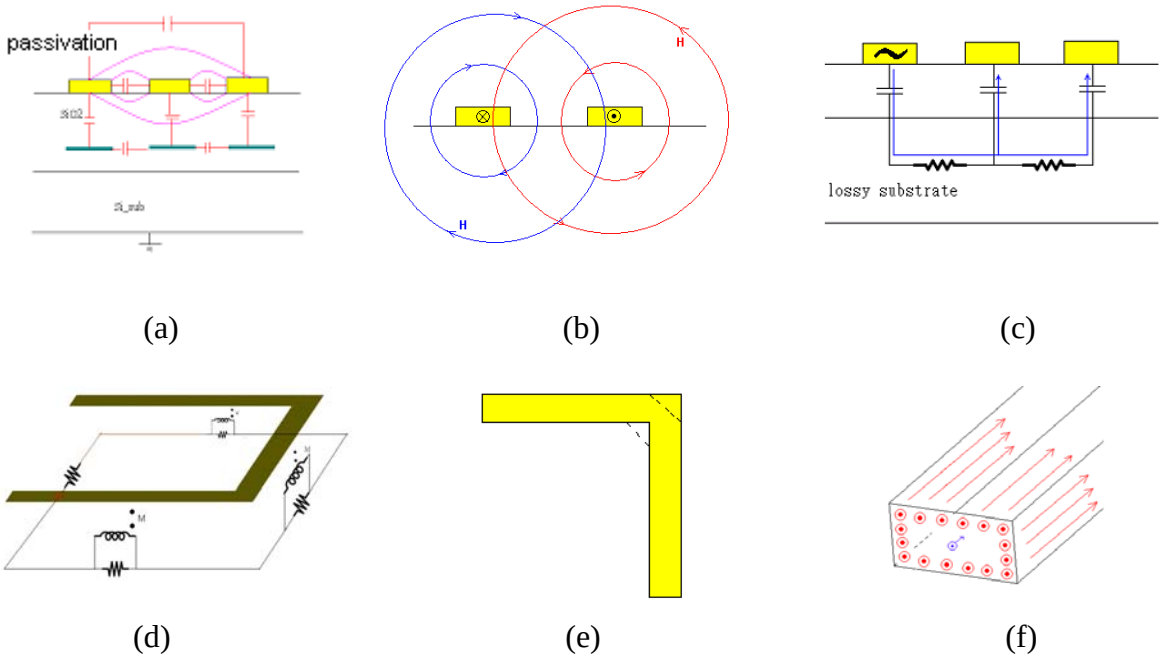


Figure 2.1-5 (a) Electric coupling between adjacent metal wires, (b) magnetic coupling between two adjacent metal wires, (c) substrate noise coupling effect, (d) magnetic coupling between inductor and substrate is equivalent to a transformer action, (e) right angle bends can be mitered to minimize the discontinuities, (f) most current flow is confined to the conductor surface at giga hertz frequency.

(a) The electric coupling among adjacent metal lines

As shown in Fig. 2.1-5 (a), three top metal layers (drawn in yellow) and three lower metal layers (drawn in green) parallel and reside closely to each other, where the blue lines denote the electric fields. The high dielectric constant ε of insulators e.g. passivation or silicon dioxide degrades the self-resonance frequency by parasitic capacitance. Widening metal line only raises the parasitic capacitance between upper and lower metal layers since currents concentrate on the edges of conductors at high frequency. By simulation and optimization, the spacing and the metal line width kept as 5um and 10um for all inductors are distinguished from those of foundries'. This effect is characterized by Cs in Fig. 2.1-4 (c).

(b) The magnetic coupling between two adjacent metal lines

Two parallel metal lines lie nearly on the substrate. The current flow is oriented out of the paper on the left one and reversed on the right one, respectively. The magnetic fields interact and resist to each other thereby the equivalent resistance is produced and introduced into the conductors. This so-called proximity effect can be ignored as long as the central area or inner diameter of inductors is large sufficiently.

(c) Substrate noise coupling (substrate effect)

Silicon semiconductor is a lossy material with finite resistivity. Figure 2.1-5 (c) schemes signals on one conductor coupled to lossy substrates through silicon dioxide might disturb the ones on other conductors. Furthermore, as shown in Fig. 2.1-4 (a), the behavior of where signals coupled to substrate carry on coupling to ground degrades the quality of inductors. Widening metal line makes capacitive couple more severe. The coupling path would generate redundant power dissipation and noise owing to the conductive substrate. In the simplified PI model of Fig. 2.1-4 (c), Cox, Csub and Rsub characterize the substrate effect.

(d) Eddy current in substrate

Inductors generate time-varying magnetic fields during alternative current operation. Lenz's law states that reversely oriented magnetic fields would be generated to oppose the variation of the preceding fields and eddy currents is induced in the substrate, as shown in Fig. 2.1-5 (d). The reduction of inductance as well as the redundant power dissipation occurs. This effect modeling resembles to the previous one, characterized by Csub and Rsub as

well.

(e) Inductor structure defects

Rectangular inductors have a trivial drawback that exists at the all right angle bends. Electrical charges accumulate and radiate EM waves at sharp angles. UMC provides circular inductors to prevent charges accumulation and radiation. However, chip area is consumed more to trade off higher quality. Actually, repairing this contradiction for inductor design just needs a trick shown in Fig. 2.1-5 (e).

(f) Conductor loss

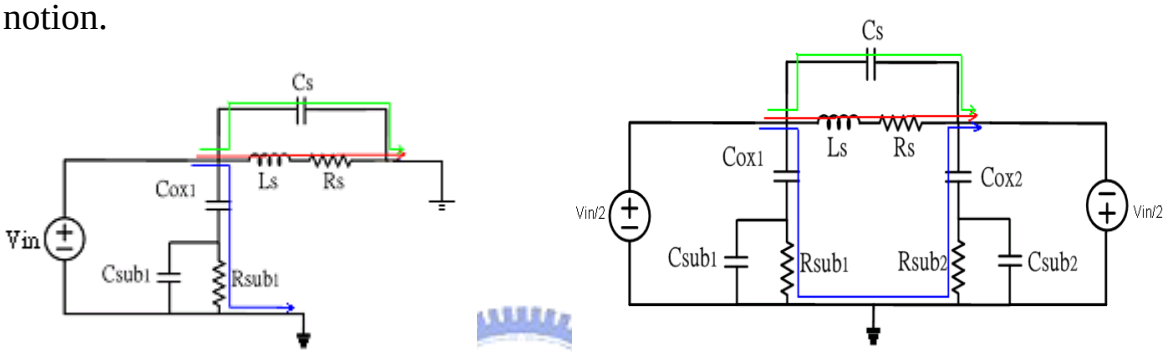
Metal layers comprise aluminum alloy in modern VLSI 0.18um 1P6M technology. Generally, the conductivity of the metal ranges from 1.4x10^7 S/m to 2.4x10^7 S/m, and the top layer is much thicker for inductor design. Current flow concentrates on the surface or the edges of conductors at high frequency, this is called skin effect. The skin depth is defined as

$$\delta = \frac{1}{\sqrt{\sigma \pi \mu f}} \qquad \text{Eq. (2.1-1)}$$

Where $\sigma = 2 \times 10^7\ S/m$, $\mu = 4\pi \times 10^{-7}\ H/m$, skin depth $\delta \approx 2.52\ \mu m$ at 2GHz. This means 63.2 % of currents concentrates into 2.52um thickness of metal. Therefore, imperfection of conductors and skin effect cause the parasitic resistance at high frequency; excessive width of metal wires is not meaningful at all.

2.2 Design Method

Nowadays, Some distinct inductors are proposed. 3D stacked and symmetrical structures are the representative examples. 3D stacked structures can minimize the inductor area; symmetrical structures can distribute the capacitance uniformly from the two oriented signal entries (port1 to port2 or port2 to port1), as mentioned at Chap 1, respectively. Figure 2.2-1 illustrates the notion.



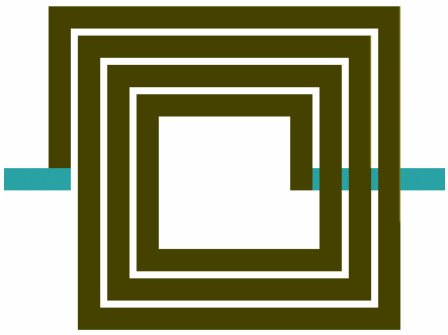
(a) (b)

Figure 2.2-1 The signal flow diagram of a (a) single ended, (b) differentially driven inductor.

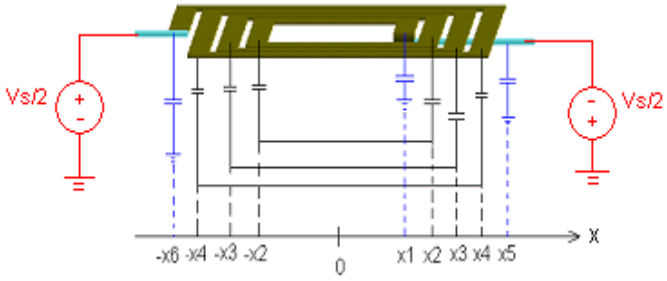
The blue line denotes the capacitive coupling path through the substrate. The capacitance is divided as well as the substrate resistance is doubled while the inductor is differentially stimulated. The impedance for the blue line can be expressed as:

$$Z_{blue\ line} = \frac{1}{j\omega C_{ox1}} + \frac{1}{G_{sub1} + j\omega C_{sub1}} + \frac{1}{j\omega C_{ox2}} + \frac{1}{G_{sub2} + j\omega C_{sub2}} \qquad \text{Eq. (2.2-1)}$$

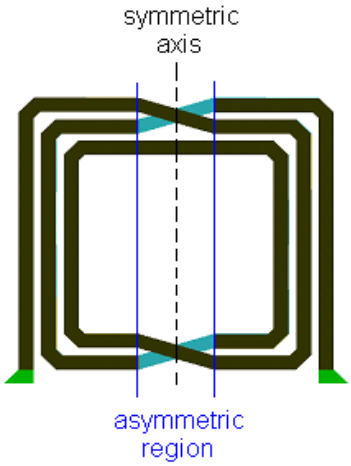
If the capacitance of two sides is equal, the total becomes half and minimum. Hence, either the quality factor or the self-resonance frequency is elevated. Figure 2.2-2 sketches the capacitance distribution of symmetrical and asymmetrical inductors as they are differentially driven, respectively.



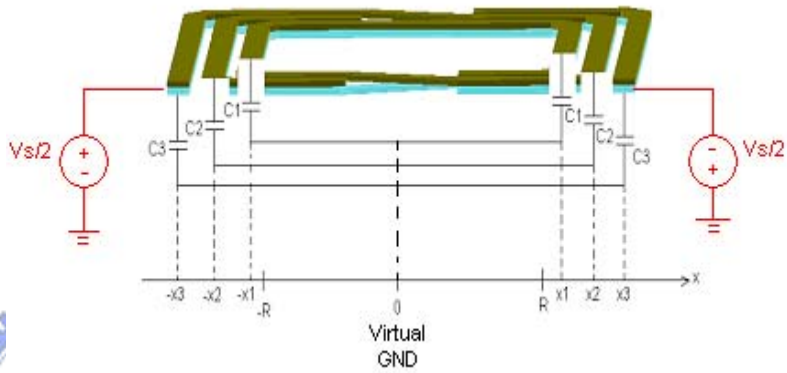
(a)



(b)



(c)



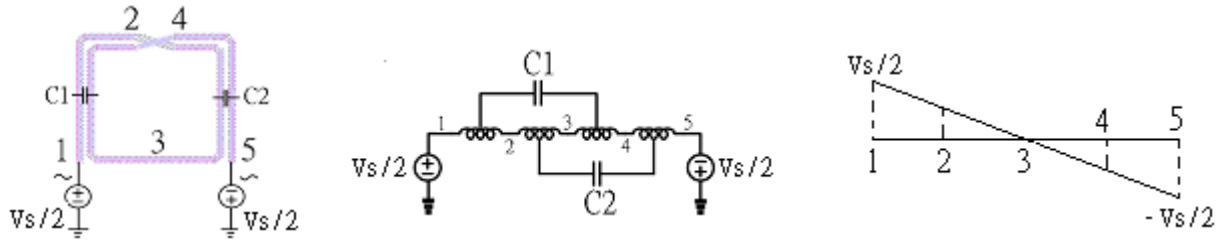
(d)

Figure 2.2-2 (a) Asymmetrical inductor, (b) capacitance distribution along the path, x represents distance, (c) symmetrical inductor, (d) capacitance distribution, x represents both distance and voltage.

Some asymmetry still exists at the cross over region in a symmetrical inductor as depicted in Fig. 2.2-2 (c). Figure 2.2-2 (d) demonstrates that each stray capacitor under a symmetrical inductor can correlate to its image on the opposition except at the cross sections. Furthermore, x represents distance and voltage simultaneously since the geometry and voltage distribution are balanced.

In symmetrical inductors, the interwinding (fringe) capacitance becomes significant [8]. Consider the structure shown in Fig. 2.2-3 (a), where the spiral is excited differentially and viewed as four segments in series. Modeling each segment and including the fringe capacitance between the segments, we arrive

at the equivalent circuit in Fig. 2.2-3 (b). Note that symmetry creates a virtual ground at node 3. This model reveals that C1 and C2 sustain large voltages, e.g., as much as Vin/2 if we assume a linear voltage profile from node 1 to node 5 [Figure 2.2-3(c)].



(a) (b) (c)

Figure 2.2-3 (a) Symmetrical inductor including interwinding capacitance, (b) circuit model of inductor, (c) voltage profile through the inductor.

Consequently, the line-to-line spacing may be chosen several times the minimum allowable value.

Circuits requiring large inductance values can incorporate “stacked” structures to save substantial area [4]. Depicted in Fig. 2.2-3 is an example, where two stacked spirals are placed

Figure 2.2-4 Stacked inductor and its model.

in series, yielding a total inductance equal to

$$L_{tot} = L_1 + L_2 + 2M, \qquad M = k\sqrt{L_1 L_2} \qquad \text{Eq. (2.2-2)}$$

Synthesizing the both merits of symmetrical and stacked structures as well as avoiding the nonidealities studied at last section is able to propose three inductor types: 3D symmetrical inductors, 3D non-overlapping symmetrical inductors and symmetrical multi-metal layers connected inductors.

I. 3D symmetrical inductor

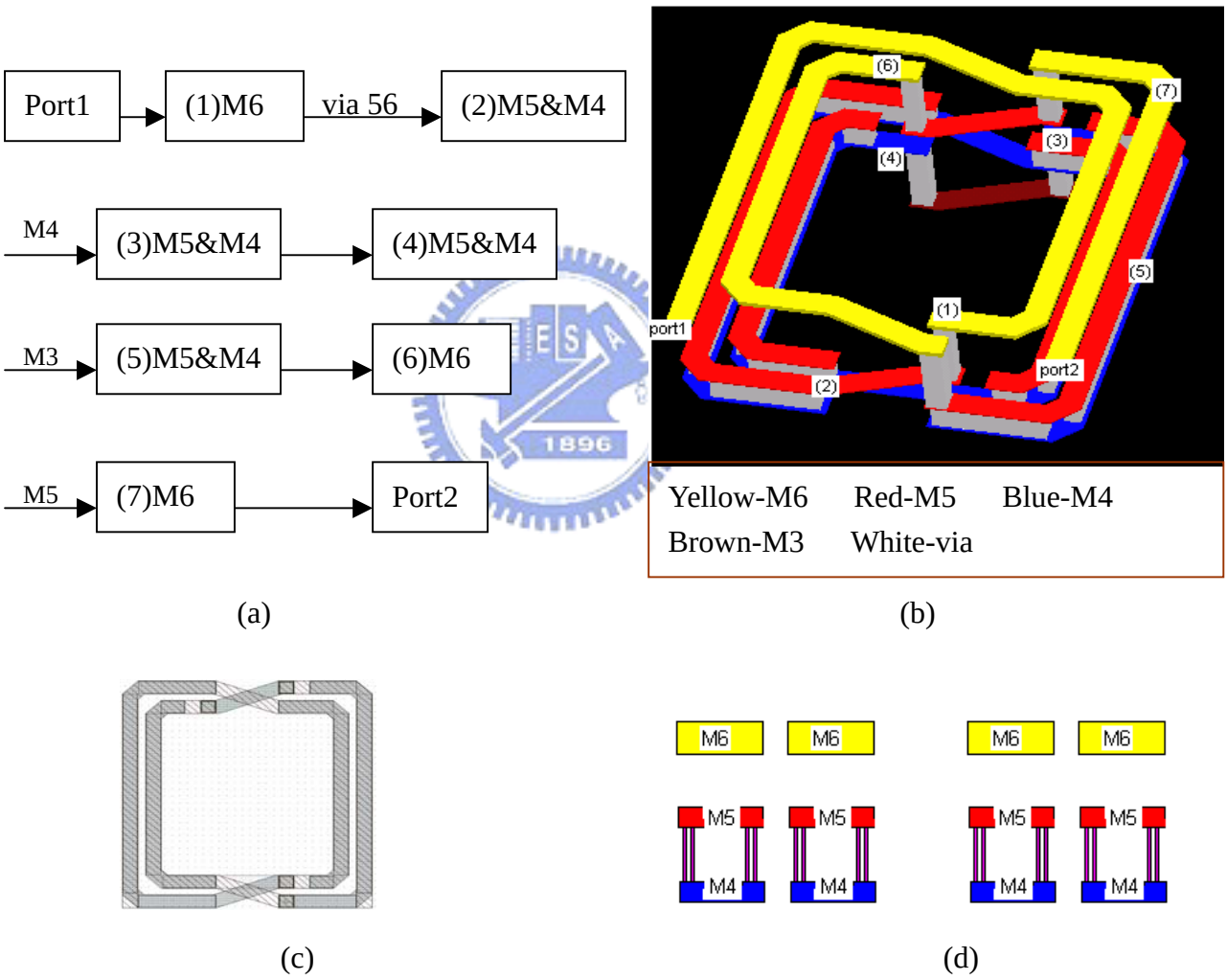


Figure 2.2-5 (a) Layout description, (b) 3D view, (c) top view, (d) lateral view.

Metal 5 and metal 4 are connected by vias since the lower metal layers are thinner, to diminish conductor resistance. The equivalent turn number is four.

The 3D symmetrical structure can be developed and extended to six turns, as depicted in Fig. 2.2-6.

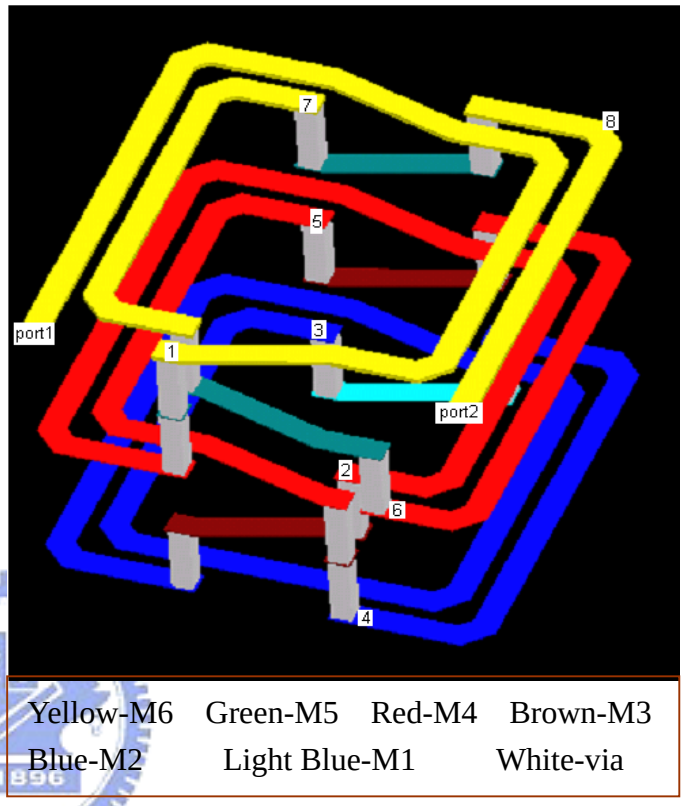
port1 → (1) M6 → (2) M4

→ (3) M2 → (4) M2

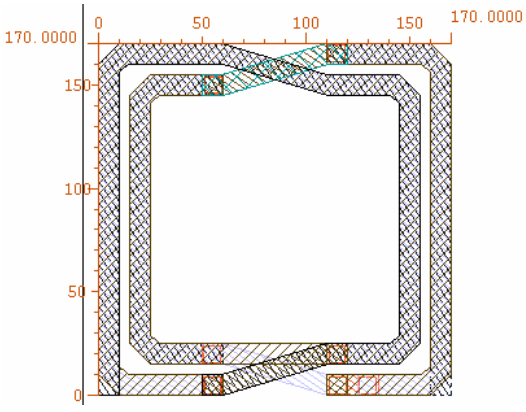
→ (5) M4 → (6) M4

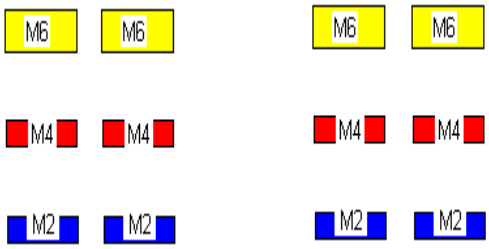
→ (7) M6 → (8) M6

→ port2



(a) (b)

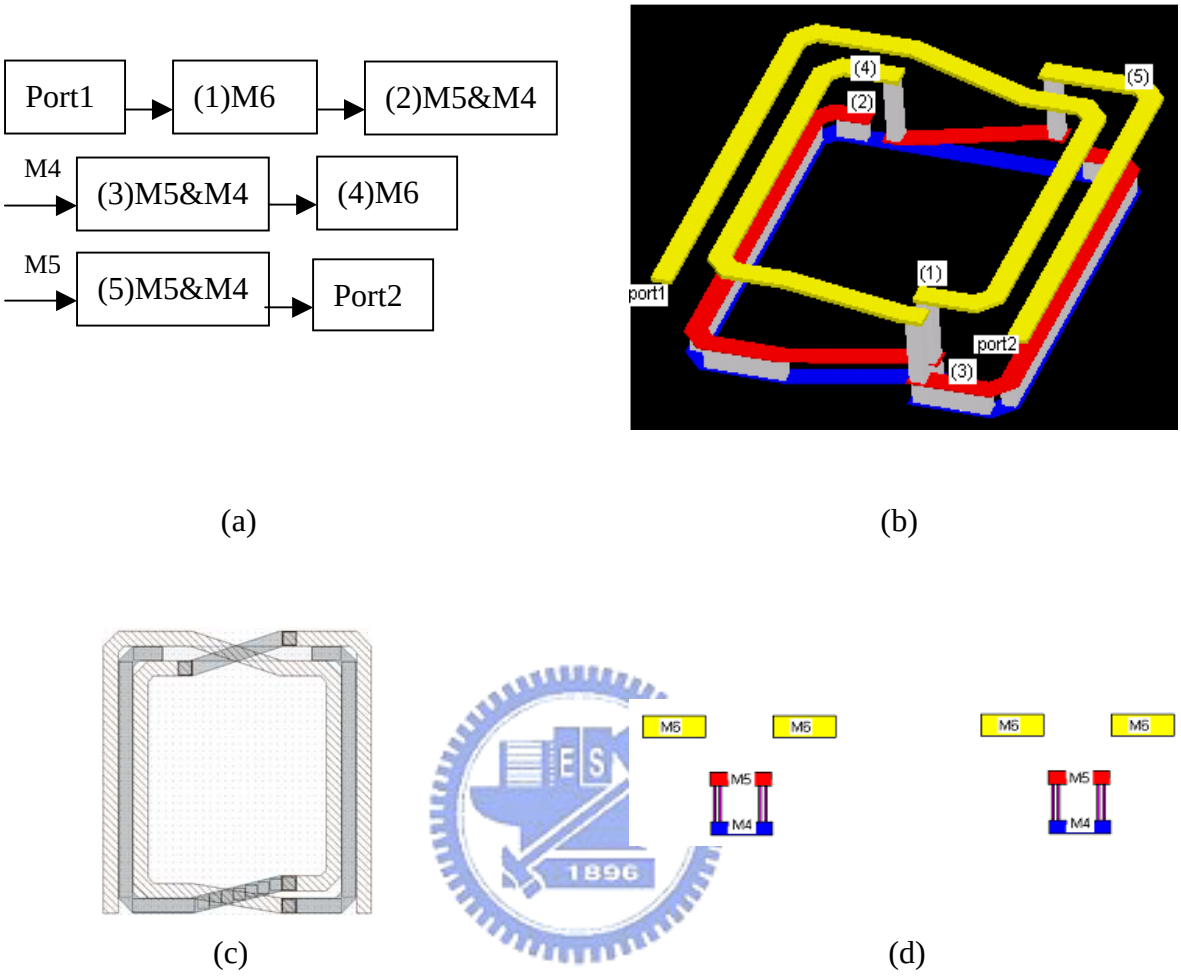




(c) (d)

Figure 2.2-6 (a) Layout description, (b) 3D view, (c) top view, (d) lateral view.

II. 3D non-overlapping symmetrical inductor



(a) (b)

(c) (d)

Figure 2.2-7 (a) Layout description, (b) 3D view, (c) top view, (d) lateral view.

The coupling capacitance between the stacked metal might distort the inductor quality, thus the non-overlapping type is presented. The simulation result somewhat coincides with this statement as depicted in Fig. 2.2-8. The equivalent turn number is three.

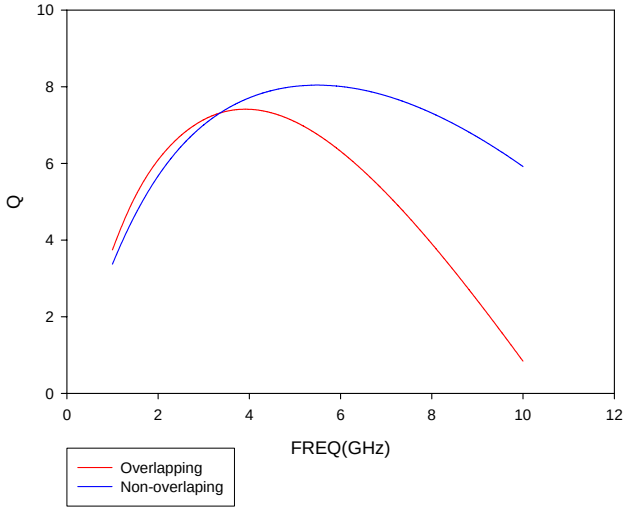
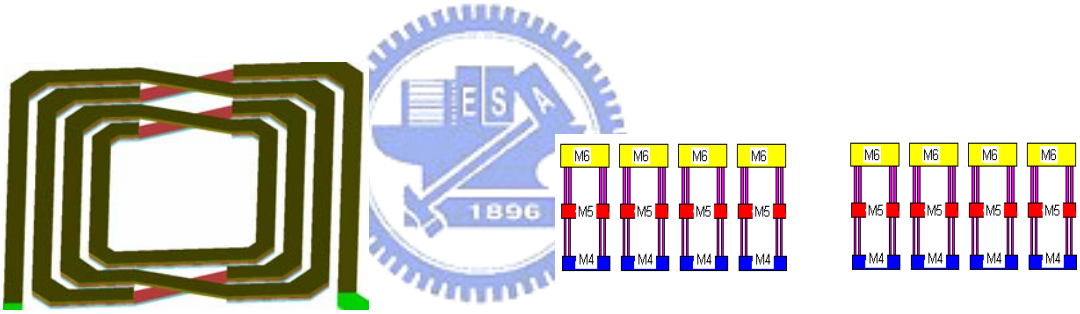


Figure 2.2-8 Comparison of inductor quality between with and without overlapping types.

III. Symmetrical multi-metal layers connected inductor



(a) (b)

Figure 2.2-9 (a) 3D view, (b) lateral view.

This is a coplanar structure that differs from those introduced before, where metal 6, metal 5 and metal 4 are connected by vias to reduce the parasitic resistance. The equivalent turn number is four.

2.3 Measurement Results

The pad effect must be discarded by de-embedding process to own the real characterization of devices. An open dummy pad is added in layout for de-embedding process. The y-parameter of the open pad $[Y]_{pad}$ is subtracted from the y-parameter of the inductor including the pad [Y]. Next, the de-embeded y parameter $[Y]_{de}$ is obtained and it can be transformed to S or Z-parameter. Q and L are extracted by the formulas eventually. Figure 2.3-1 depicts the procedure in detail.

$= [Y]_{de}$

$\Rightarrow$ $[Y]_{de}$ transforms to $[S]_{de}$ or $[Z]_{de}$

$$\begin{cases} V_1 = Z_{11}I_1 + Z_{12}I_2 \\ V_2 = Z_{21}I_1 + Z_{22}I_2 \end{cases}$$

$$Z_{in} = \frac{V_1}{I_1}\Big|_{V_2=0} \quad , \quad I_1 = -\frac{Z_{21}}{Z_{22}}I_1 \quad \Rightarrow \quad Z_{in} = Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22}}$$

Q=Im(Zin)/Re(Zin), L=Im(Zin)/(2 π f)

Figure 2.3-1 The de-embedding procedure as well as the extraction of Q and L.

The design is implemented on the 0.18um 1P6M technology of both TSMC and UMC. It is informed that UMC's process provides higher metal conductivity and low loss substrate by investigating the data books or documents.

I. TSMC 0.18um 1P6M technology

(i) 3D symmetrical inductor

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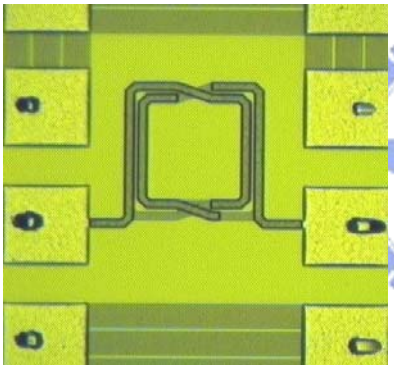
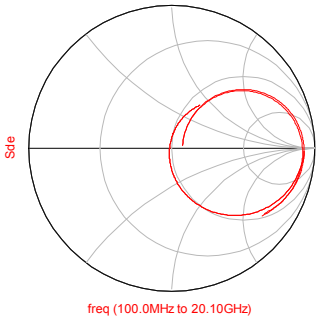
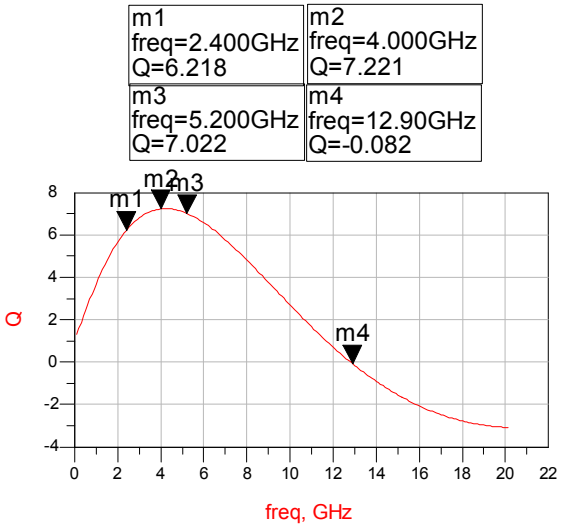
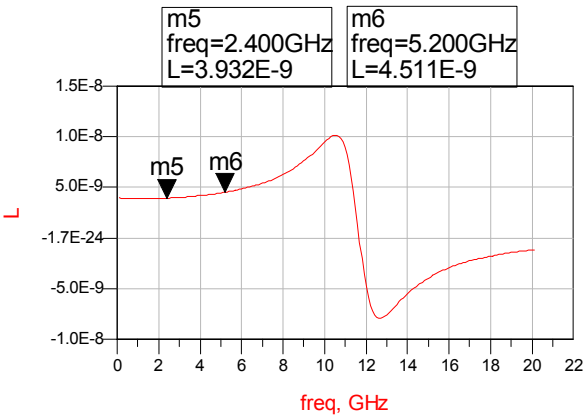
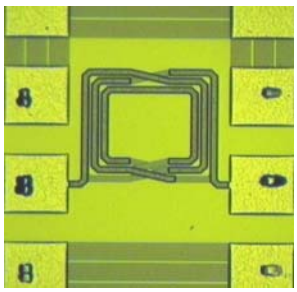


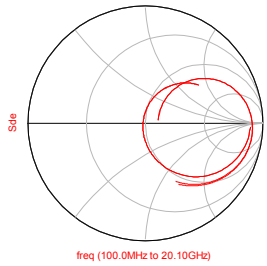


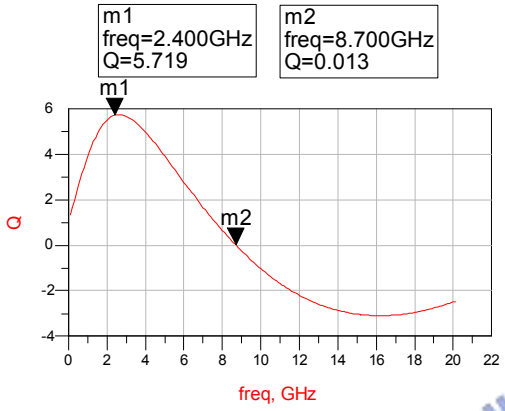


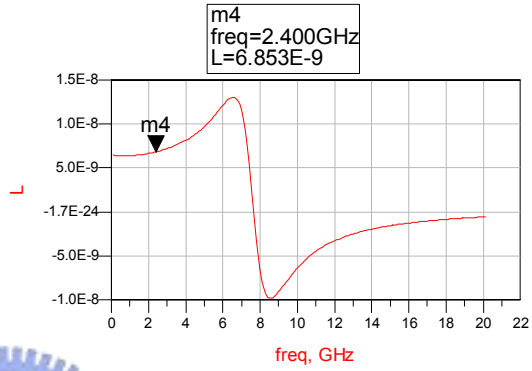


No. sym_od210um_3d5t Area=0.21mm*0.19mm=0.0399 mm^2



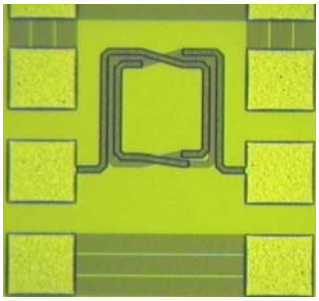


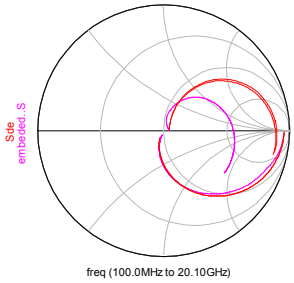


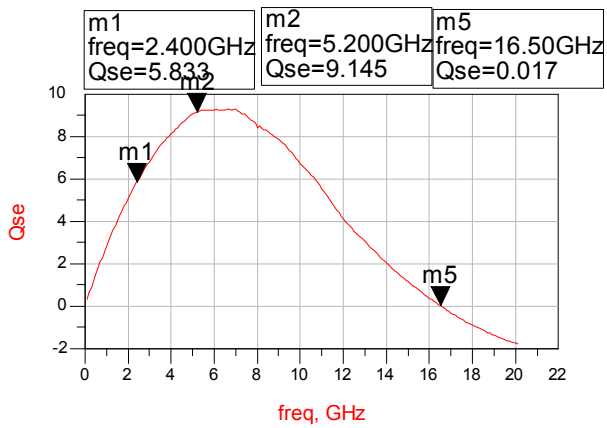


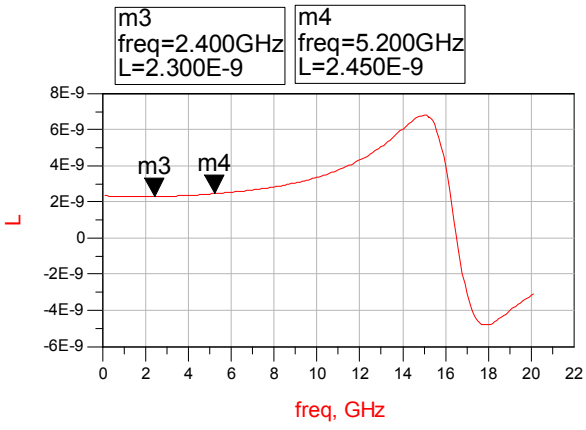
(ii) 3D non-overlapping symmetrical inductor

No. sym_od180um_3d3t_nol Area=0.18mm*0.19mm=0.0342 mm^2

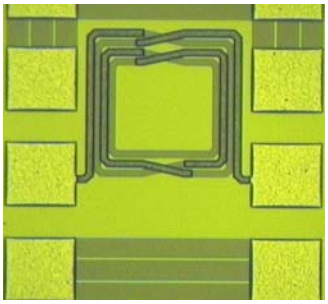


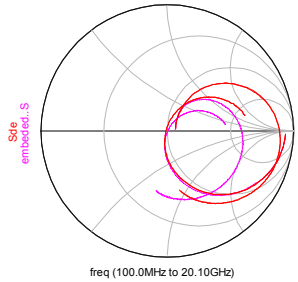


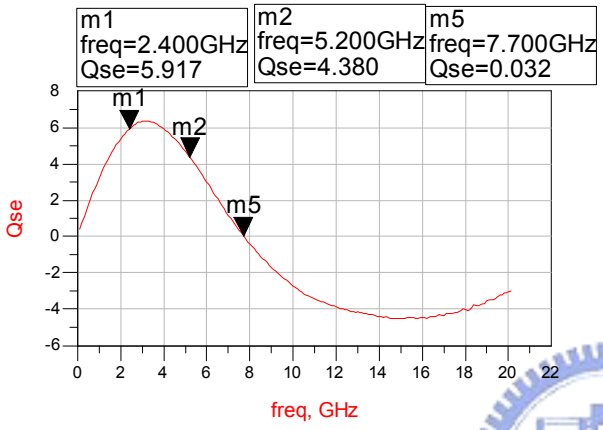


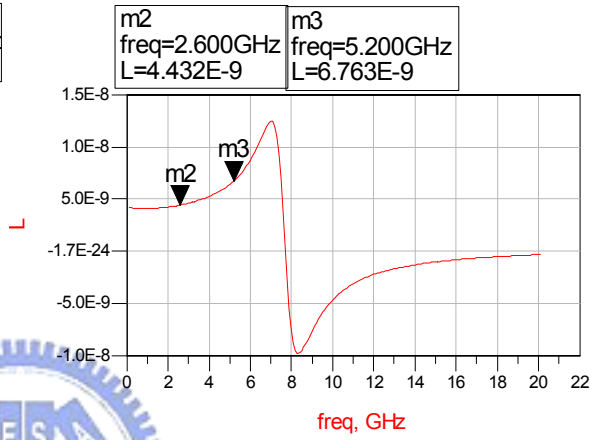


No. sym_od210um_3d4t_nol Area=0.21mm*0.19mm=0.0399mm^2

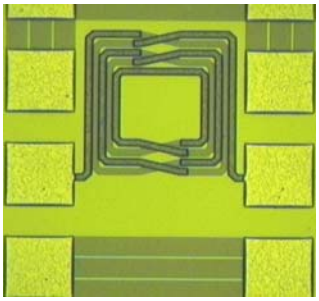


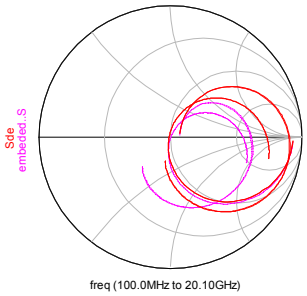


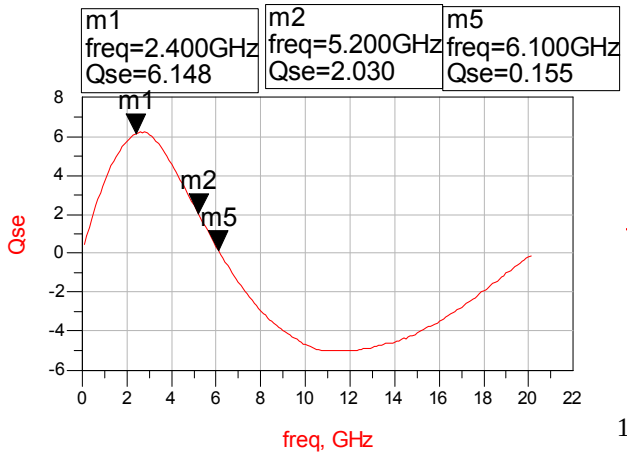


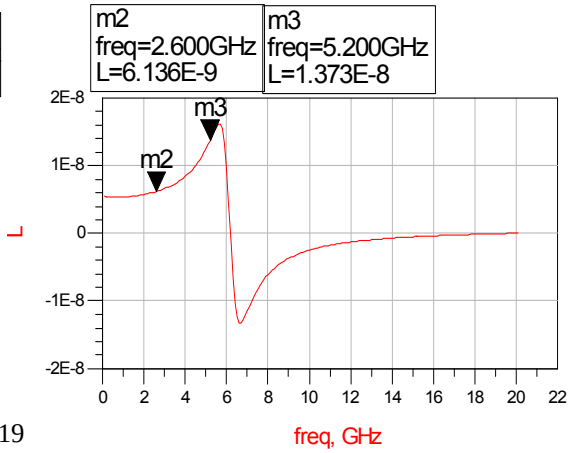


No. sym_od210um_3d5t_nol Area=0.21mm*0.19mm=0.0399mm^2



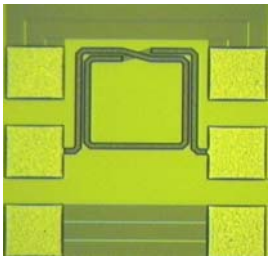


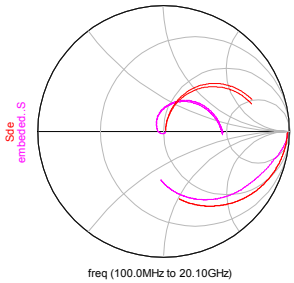


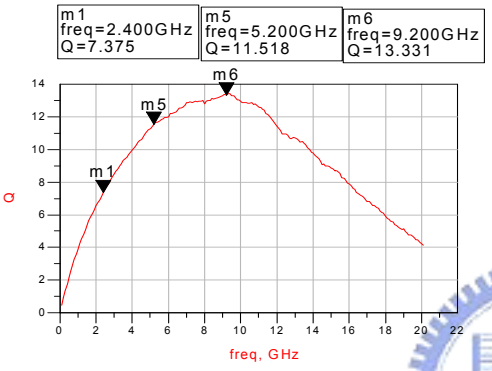


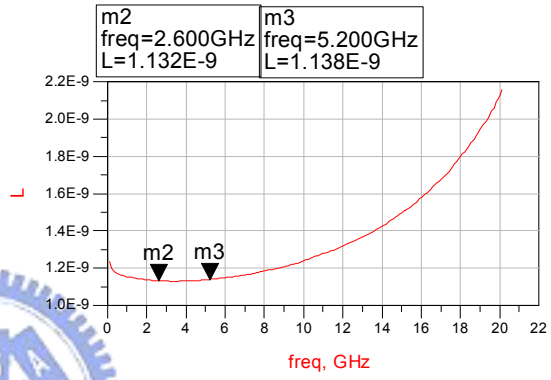
(iii) Symmetrical multi-metal layers connected inductor

No.sym_od210um_3m2t Area=0.21mm*0.19mm=0.0399mm^2

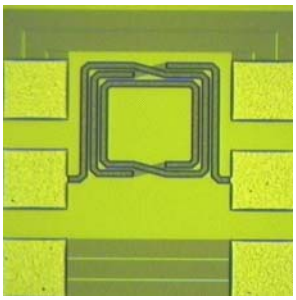


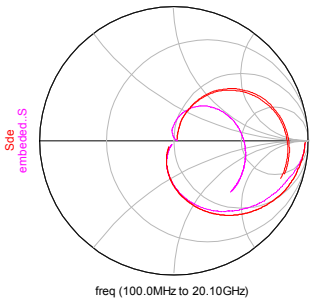


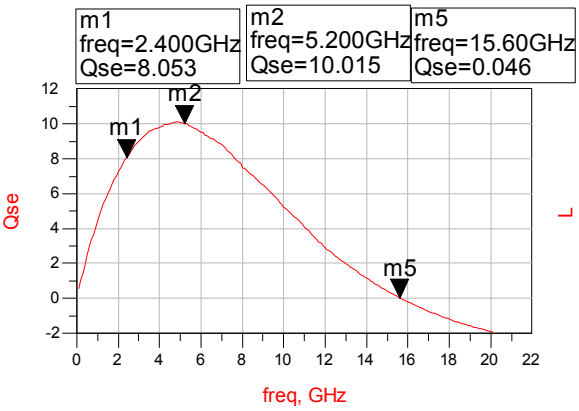


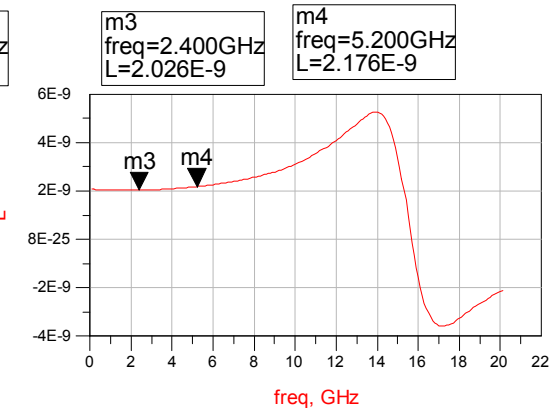


No. sym_od210um_3m3t Area=0.21mm*0.19mm=0.0399mm^2

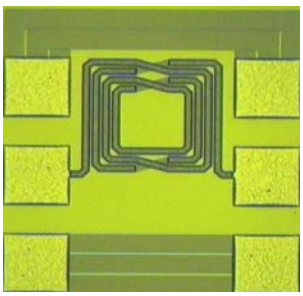


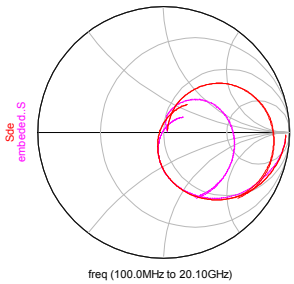


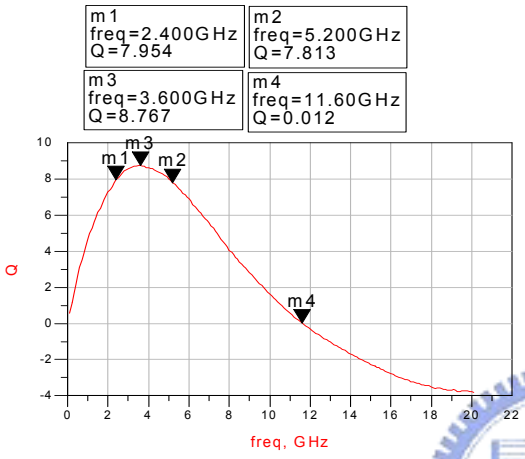


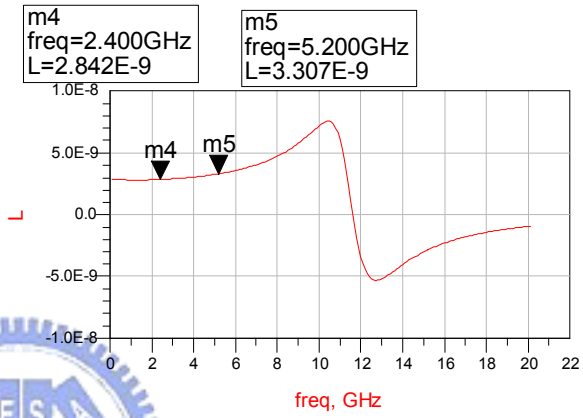


No. sym_od210um_3m4t Area= 0.21mm*0.19mm=0.0399mm^2





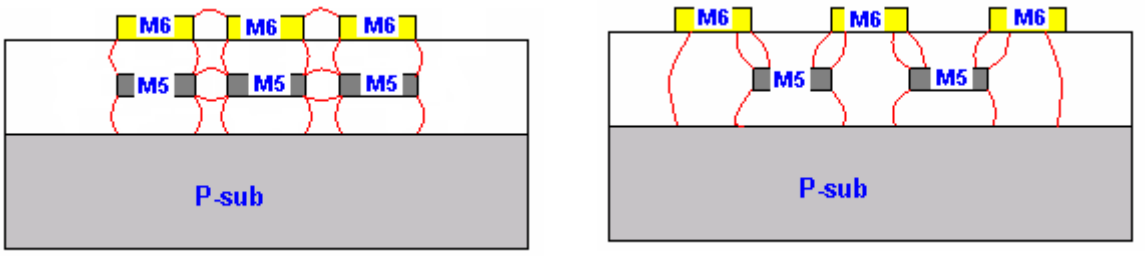




No.	sym_ od160um_ 3d4t	sym_ od210um_ 3d5t	sym_ od180um_ 3d3t_nol	sym_ od210um_ 3d4t_nol	sym_ od210um_ 3d5t_nol	sym od210um 3m2t	sym od210um 3m3t	sym od210um 3m4t
Qmax	7.2	5.72	9.15	6.2	6.15	13.4	10.015	8.766
Q@ 2.4GHz	6.22	5.72	5.833	5.92	6.15	7.345	8.053	7.954
Q@ 5.2GHz	7		9.145	4.38	2.03	11.518	10.015	7.813
L(nH)@ 2.4GHz	3.93	6.85	2.3	4.36	5.96	1.133	2.026	2.842
L(nH)@ 5.2GHz	4.51		2.45	6.76		1.138	2.176	3.307
fsr(GHz)	12.9	8.7	16.5	7.7	6.1	>20	15.6	11.6
Area(mm^2)	0.028	0.0399	0.0342	0.0399	0.0399	0.0399	0.0399	0.0399

Table 2.3-1 Measurement data of the inductors taped out in TSMC 0.18um 1P6M process.

According to the measurement results, non-overlapping type has neither a better quality nor a broader bandwidth than metal-stacked type at a high inductance level. The reasons probably are that the fringe effect still exists although the metal layers are staggered as well as the substrate coupling acts more severely. Consider the affairs depicted in Fig. 2.3-2, where red lines denote the electric fields.



(a) (b)

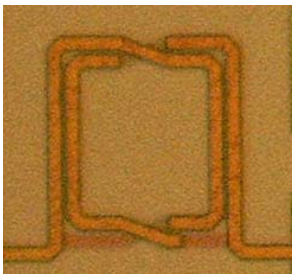
Figure 2.3-2 Electric coupling (a) stacked metal type, (b) non-overlapping type.

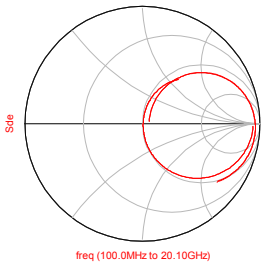
The identical inductor structures are implemented in UMC as well. The measurement results are displayed in the following.

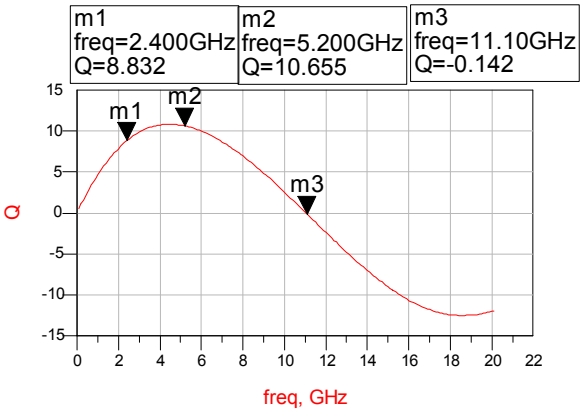
II. UMC 0.18um 1P6M technology

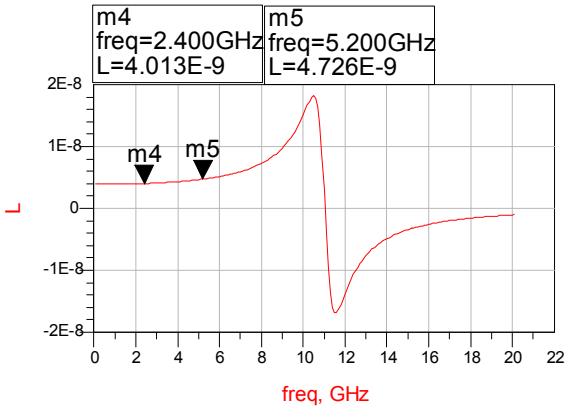
(i) 3D symmetrical inductor

No. sym_od160um_3d4t Area=0.16mm*0.175mm=0.028 mm^2

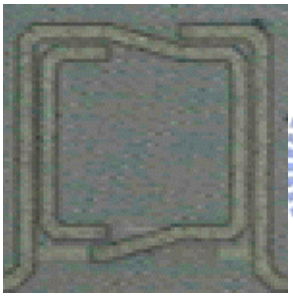


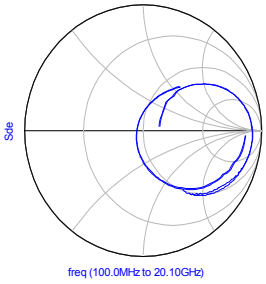


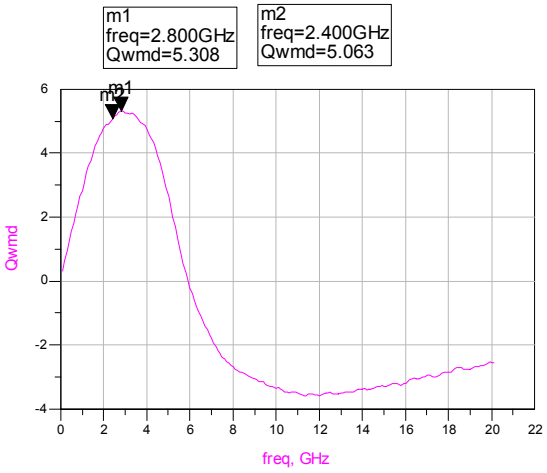


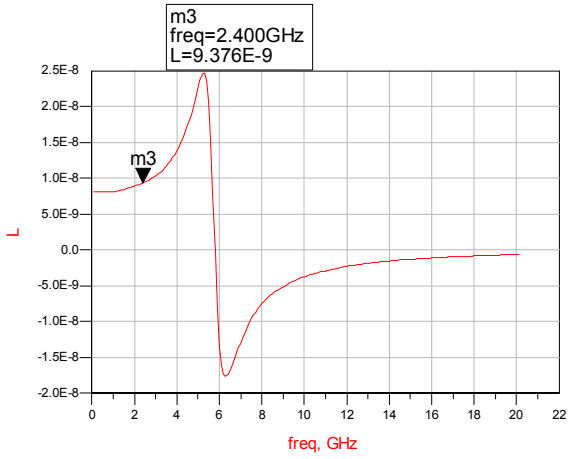


No. sym_od170um_3d6t Area=0.17mm*0.17mm=0.0289 mm^2



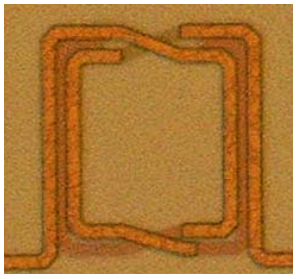


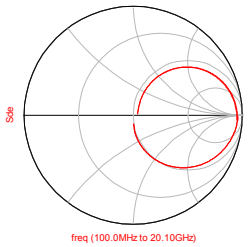


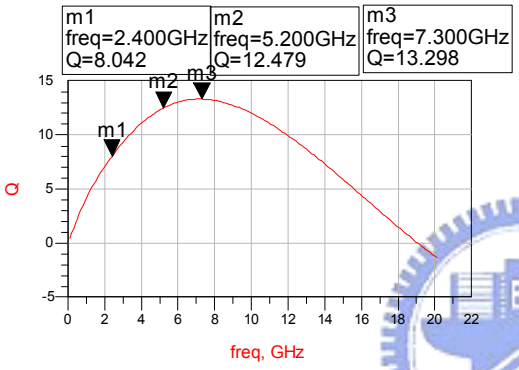


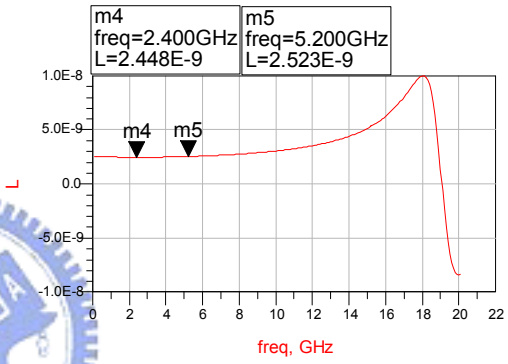
(ii) 3D non-overlapping symmetrical inductor

No. sym_od180um_3d3t_nol Area=0.18mm*0.19mm=0.0342 mm^2



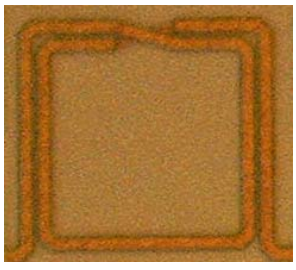


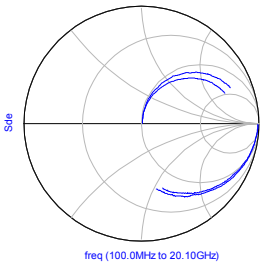


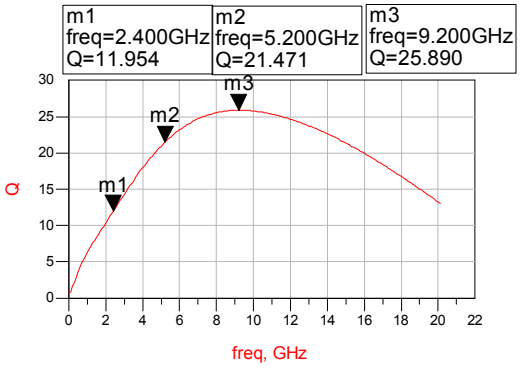


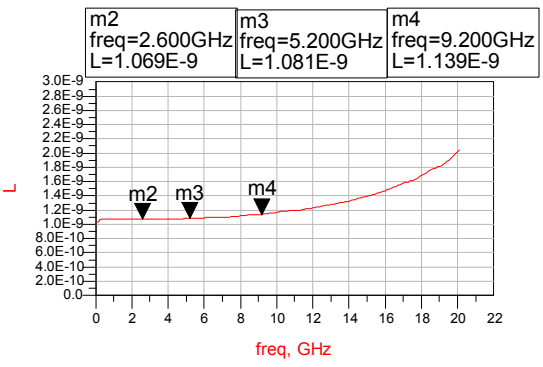
(iii) Symmetrical multi-metal layers connected inductor

No. sym_od210um_3m2t Area=0.21mm*0.19mm=0.0399mm^2

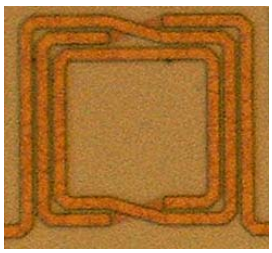


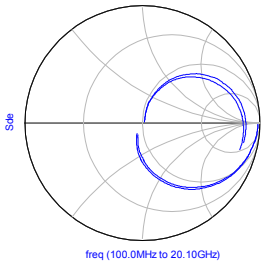


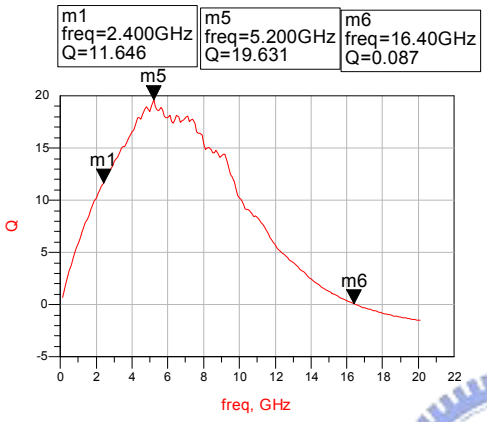


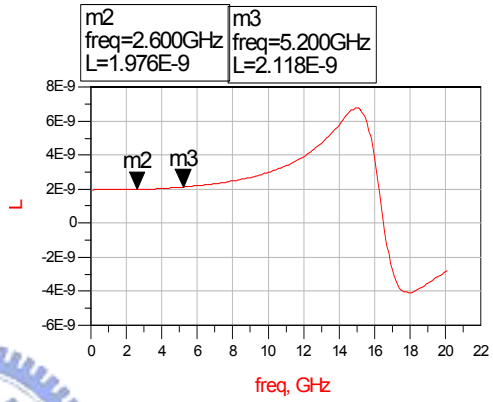


No. sym_od210um_3m3t Area=0.21mm*0.19mm=0.0399mm^2

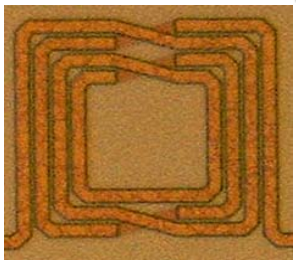


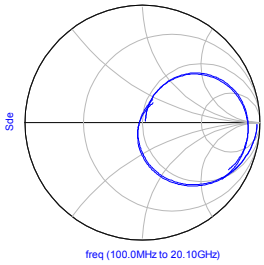


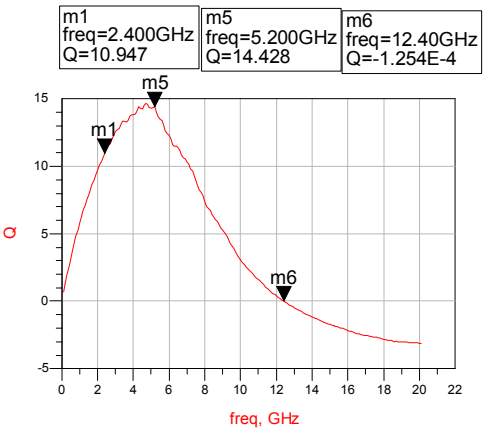


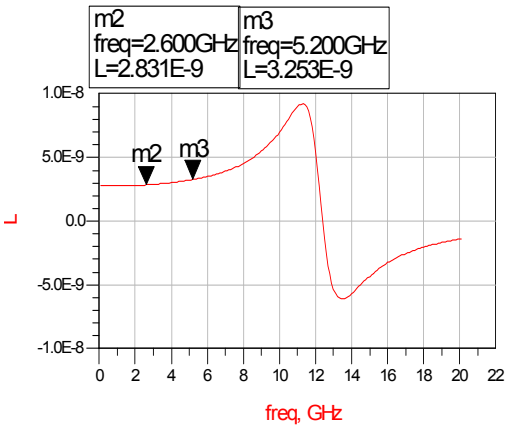


No. sym_od210um_3m4t Area=0.21mm*0.19mm=0.0399mm^2









No.	Sym Od160m 3d4t	Sym Od170um 3d6t	Sym Od180um 3d3t_nol	Sym Od210um 3m2t	Sym Od210um 3m3t	Sym Od210um 3m4t
Qmax	10.655	5.308	13.3	25.89	19.631	14.428
Q@ 2.4GHz	8.832	5.063	8.042	11.954	11.646	10.947
Q@ 5.2GHz	10.655		12.479	21.471	19.631	14.428
L@ 2.4GHz	4.013	9.376	2.45	1.069	1.976	2.831
L@ 5.2GHz	4.726		2.523	1.081	2.118	3.253
Fsr(GHz)	11.1	5.8	19	>20	16.4	12.4
Area(mm^2)	0.028	0.0289	0.0342	0.0399	0.0399	0.0399

Table 2.3-2 .Measurement data of the inductors taped out in UMC 0.18um1P6M process.

As anticipated, the inductors fabricated by UMC perform much better than those by TSMC, because of the higher metal conductivity and lower substrate loss.

2.4 Summary

The Qmax and area of our inductors are compared with those of UMCs, as listed in the table below.

No.	Sym_ Od210um_ 3m2t	IND_C1
L(nH)	1.07	0.98
Qmax	25.98	19.41
Area(mm^2)	0.0399	0.075076

No.	Sym_ Od210um_ 3m3t	IND_C3
L(nH)	2	1.9
Qmax	19.631	12.96
Area(mm^2)	0.0399	0.076176

No.	Sym_ Od210um_ 3m4t	IND_C5
L(nH)	3	2.9
Qmax	14.428	11.6
Area(mm^2)	0.0399	0.092416

No.	Sym_ Od180um_ 3d3t_nol	IND_C4
L(nH)	2.5	2.37
Qmax	13.3	12.4
Area(mm^2)	0.0342	0.082944

No.	Sym_ Od160um_ 3d4t	IND_C8
L(nH)	4.3	4.37
Qmax	10.655	10.2
Area(mm^2)	0.028	0.068644

Table 2.4-1 Comparison with UMC's inductors.

Consequently, our inductors have marvelous quality with much smaller area. The reasons can be summarized as:

1. Highly symmetrical geometry can distribute the stray capacitance uniformly along the path.
2. Multi-metal layers connected in parallel by vias reduce parasitic resistance effectively.
3. The right angle bends are mitered to minimize the discontinuities without sacrificing any area.
4. Metal line width and spacing are maintained as 10um and 5um to minimize the capacitive coupling.

Chapter 3 Substrate Effect Decoupling

3.1 Introduction

Figure 3.1-1 illustrates the various substrate-coupling mechanisms present in a CMOS IC environment (see Niknejad [9]). Currents are injected into the substrate through different ways. Physically large passive devices such as inductors, capacitors, transformers, interconnect and bonding pads inject displacement current in the substrate. As inductors occupy substantial chip area, they tend to be the source or receptor of detrimental noise coupling. Furthermore, the physical phenomena behind the substrate effects are complicated to characterize. Hence, the device performance and modeling simplification relies on substrate isolation.

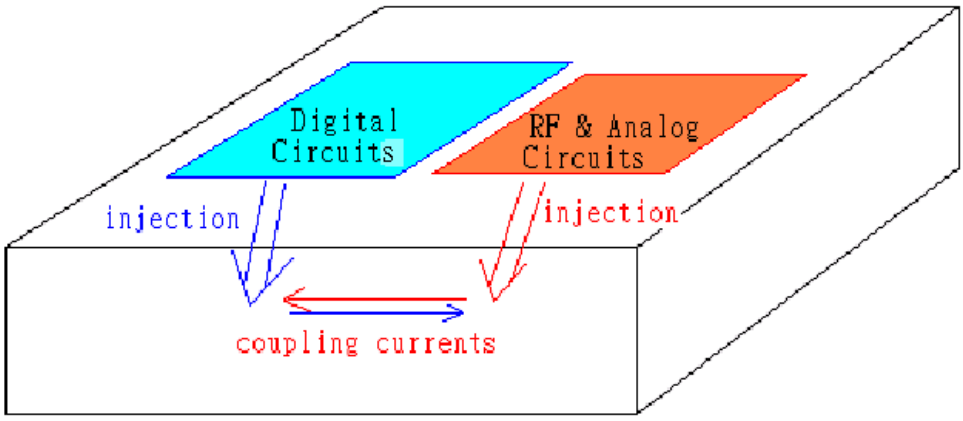
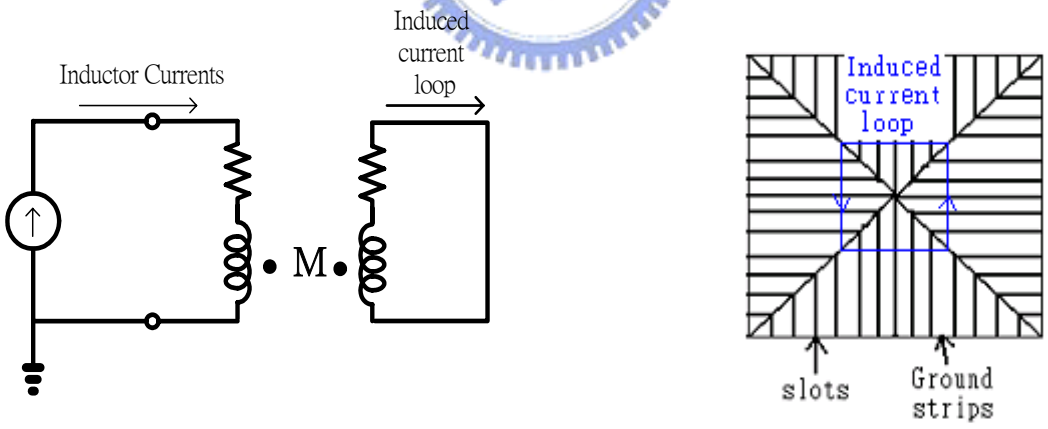


Figure 3.1-1 Substrate coupling in a mixed signal SOC.

Some approaches have been proposed to address the substrate issues; however, they are associated with some drawbacks. Ashby [10] suggested to use high-resistivity (150–200Ω-cm) silicon substrate to mimic the low-loss semi-insulating GaAs substrate, but this is an uncommon option for current silicon technologies. Chang [11] demonstrated that etching a cavity in the silicon substrate under the inductors could remove the substrate effects. However, the etch adds extra processing cost, and is not readily available. Moreover, it raises reliability concerns such as packaging yield and long-term mechanical stability. For low-cost integration of inductors, the solution to substrate problems should avoid increasing process complexity.

C. Patrick Yue and S. Simon Wong [4] presented a patterned ground shield, which is compatible with standard silicon technologies, to reduce unwanted substrate effects.



(a) (b)

Figure 3.1-2 (a) Circuit model for illustrating the effects of negative magnetic coupling between a spiral inductor and solid ground shield, (b) closed photo of the patterned ground shield.

To conserve electric energy isolated away from the lossy substrate, inductors should be shielded and the electric fields are terminated theoretically. However, the reversed oriented loop current is induced on the shielding plane to oppose the alternative magnetic fields of inductors. This is called negative magnetic coupling effect characterized by the equivalent circuit shown in Fig. 3.1-2 (a). Hence, the solid ground shield must be slotted or stripped to suppress the loop current. Unfortunately, the energy leaks out to the substrate through the slots. On the other hand, the capacitive coupling acts more severely as plotted in Fig. 3.1-3, where C’ > Cox.

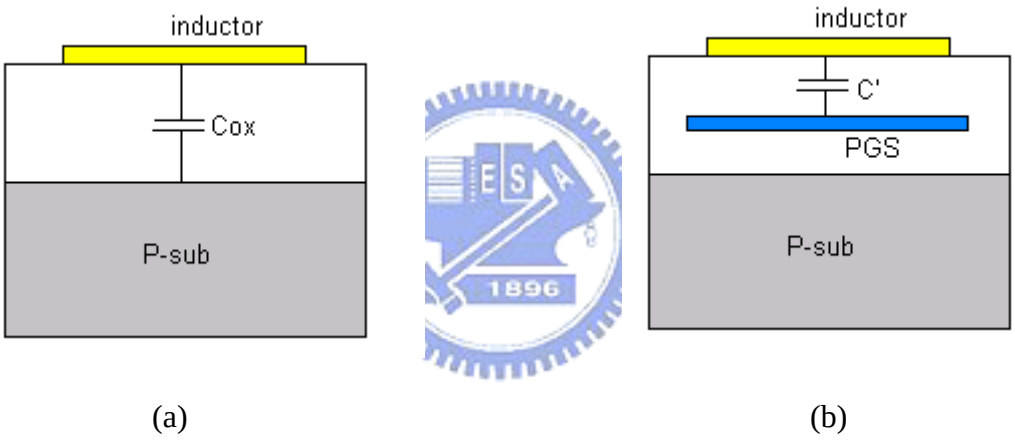


Figure 3.1-3 Inserting a patterned ground shield beneath an inductor makes capacitive coupling more severe, (a) without a PGS, (b) with a PGS.

Moreover, patterned ground shield composed of either polysilicon or metal can not keep equal potential to ground with finite conductivity thereby ground shielding doesn’t work. The measurement result verify our inference.

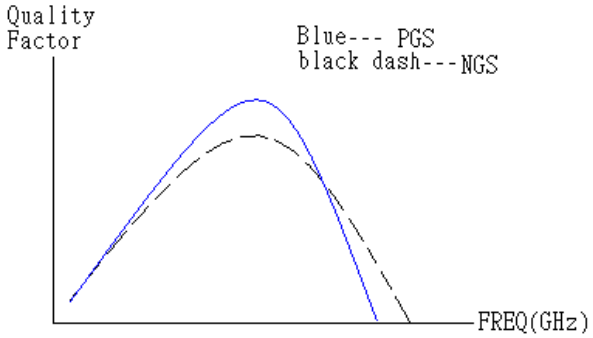


Figure 3.1-4 Inductor quality improved by inserting a PGS.

As plotted in Figure 3.1-4, there is a trade off between Q peak value and self-resonance frequency.

3.2 Novel Ideas Presentation

The concept related to patterned ground shielding is eliminating the electric coupling effect or the displacement currents in the substrate as plotted in Figure 3.2-1. Eddy currents magnetically induced by impressed device currents also impact inductor performance harmfully.

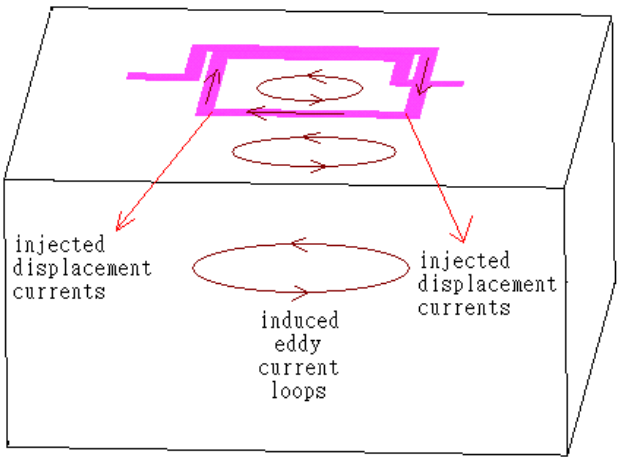


Figure 3.2-1 Schematic representation of substrate effects. Eddy currents are induced magnetically, and displacement currents are injected from the conductors to the substrate by capacitive coupling.

To prohibit the event depicted in Figure 3.1-3, it is suggested to insert a magnetic decoupler at the center of an inductor and only eddy currents are reduced.

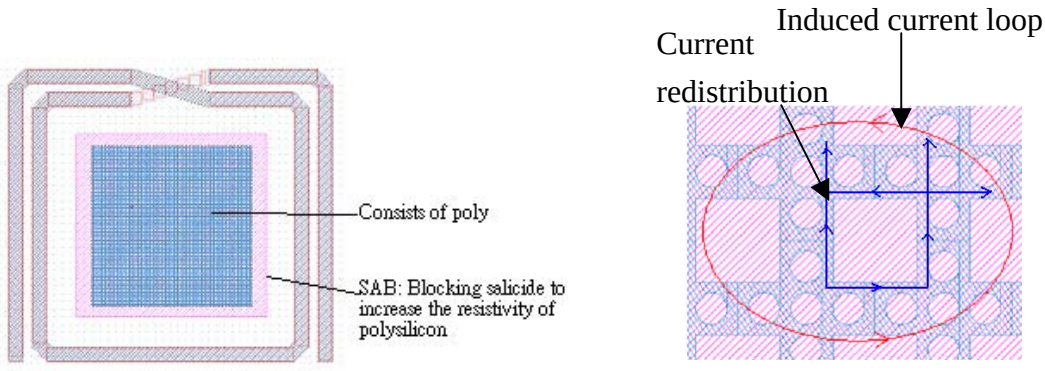


Figure 3.2-2 (a) Physical layout, (b) enlargement of the magnetic decoupler.

Figure 3.2-2 (b) indicates that the magnetic decoupler disturbs and redistributes the orientation of induced current loop divergently. Induced currents collide with themselves to each other. Consequently, most of eddy currents disappear. The key concept is that eddy currents must be induced primarily then be neutralized. Otherwise, a decoupler doesn't differ from an insulator.

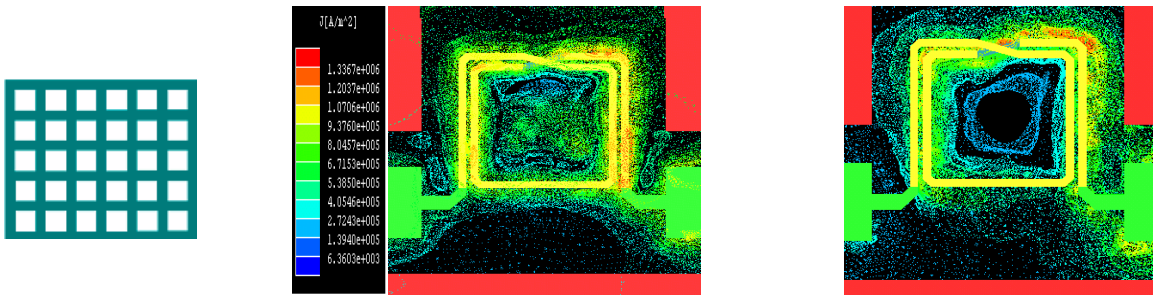


Figure 3.2-3 (a) Simplified pattern of a magnetic decoupler for simulation, (b) current distribution in substrate without a magnetic decoupler , (c) current distribution in substrate with a magnetic decoupler.

Figure 3.2-3 reveals the current distribution in substrate with and without a magnetic decoupler inserted at the inductor core. The pattern of magnetic decoupler must be simplified for simulation, like the one shown in (a). Figure 3.2-3 (b) plots that the substrate currents consist of displace currents at the periphery and eddy currents at the kernel. Figure 3.2-3 (c) demonstrates that a magnetic decoupler reduces the eddy current apparently.

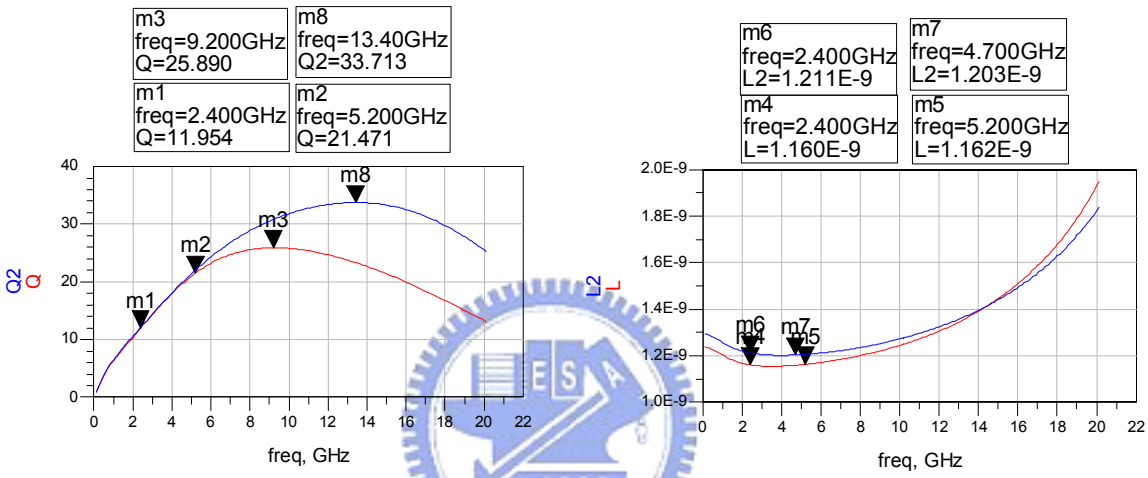


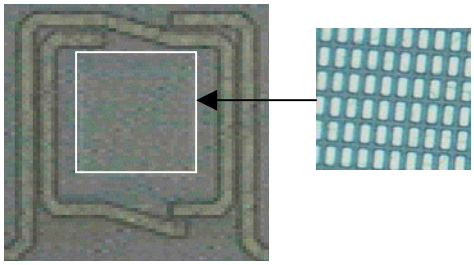
Figure 3.2-4 Performance improvements, where blue lines signify that a magnetic decoupler is added, (a) the quality factor, (b) the inductance value.

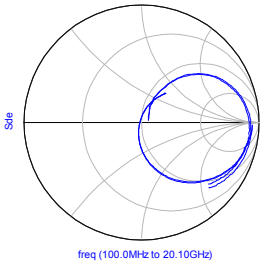
As a result of simulation, it is notable that the performance is enhanced particularly on the quality factor. The inductance value becomes a little bit higher at low frequency as well.

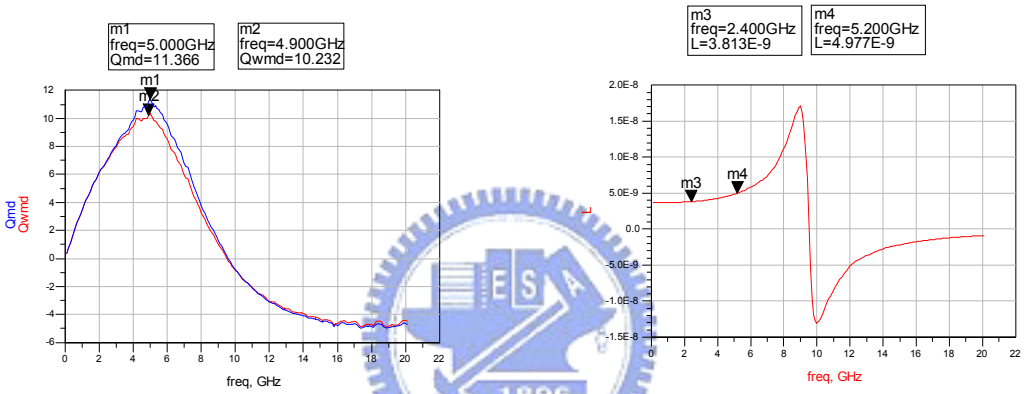
3.3 Measurement Results

(i) 3D symmetrical inductor

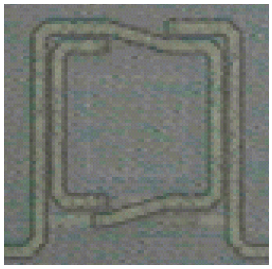
No. sym_od170um_3d4t_md

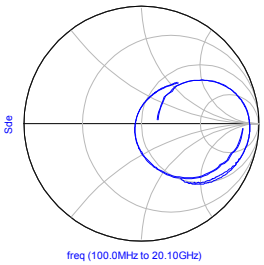


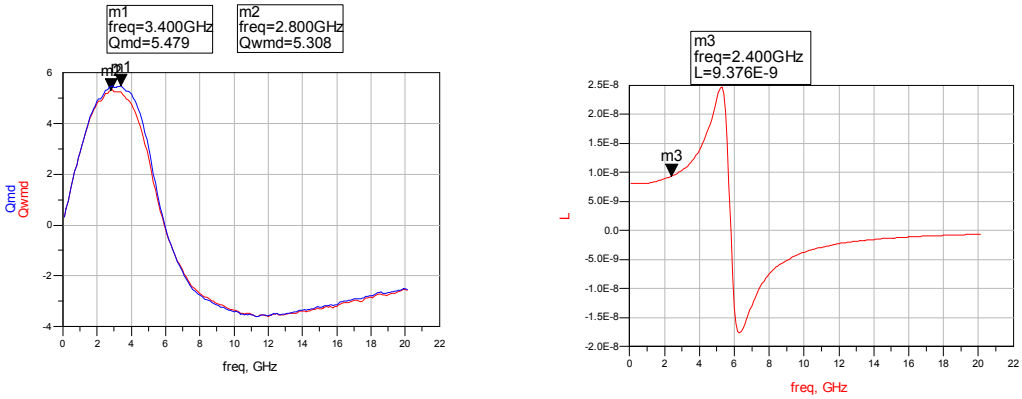




No. sym_od170um_3d6t_md

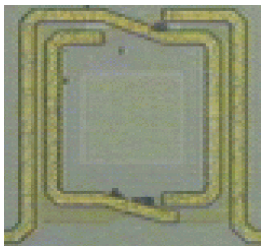


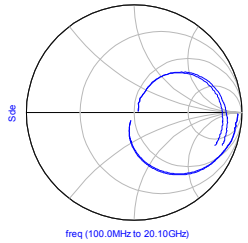


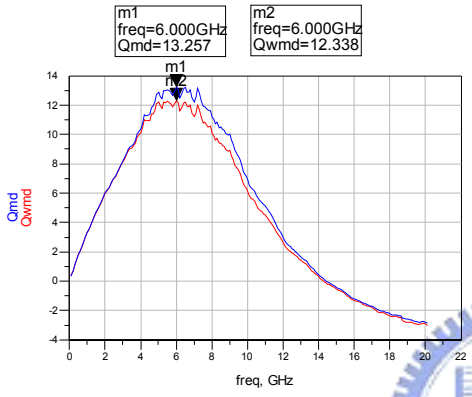


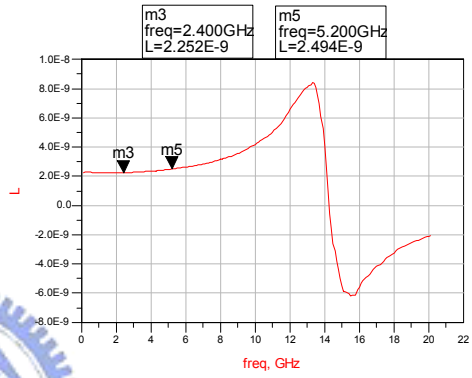
(ii) 3D non-overlapping symmetrical inductor

No. sym_od180um_3d3t_nol_md



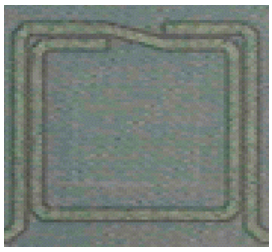


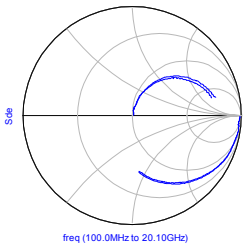


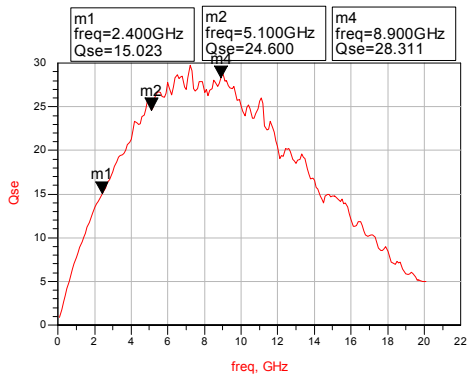


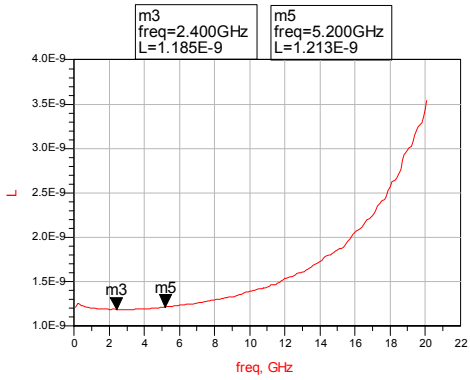
(iii) Symmetrical multi-metal layers connected inductor

No. sym_od210um_3m2t_md









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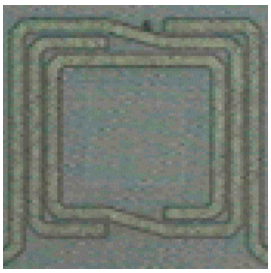

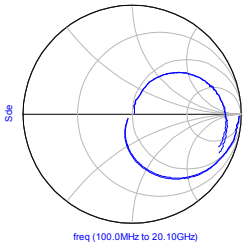

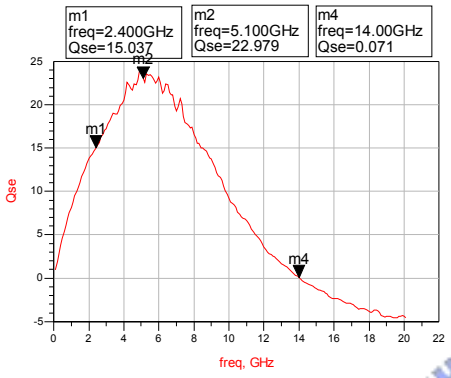

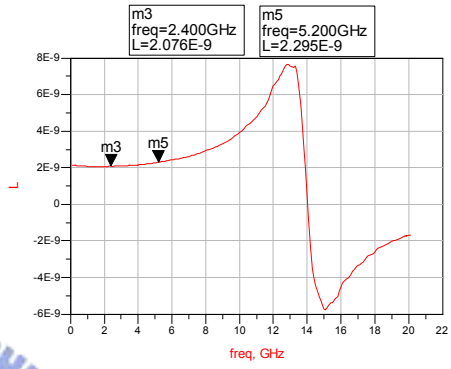

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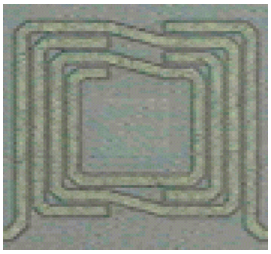
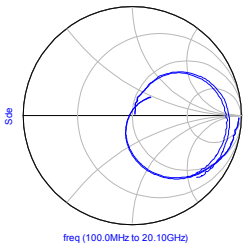
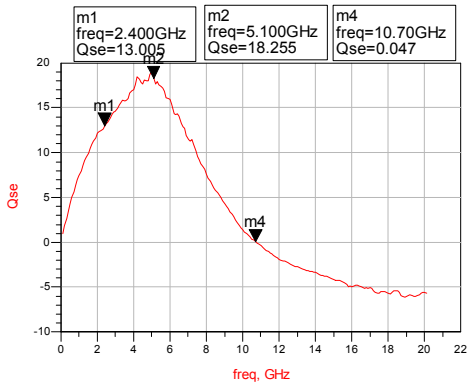
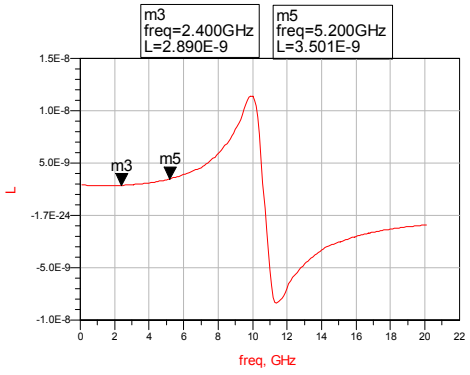








3.4 Summary

The enhancement of inductor quality contributed by inserting a magnetic decoupler at inductor core can be observed due to the measurement results, as listed in table 3.4-1.

No.	Sym Od210um 3m2t	Sym Od210um 3m2t_md	Sym Od210um 3m3t	Sym Od210um 3m3t_md	Sym Od210um 3m4t	Sym Od210um 3m4t_md
Qmax	25.89	28.311	19.631	22.979	14.428	18.255
Q@ 2.4GHz	11.954	15.023	11.646	15.037	10.947	13
Q@ 5.2GHz	21.471	24.6	19.631	22.5	14.428	18
L@ 2.4GHz	1.069	1.185	1.976	2.076	2.831	2.89
L@ 5.2GHz	1.081	1.213	2.118	2.295	3.253	3.5
fsr(GHz)	>20	>20	16.4	14	12.4	10.7
Area(mm^2)	0.0399	0.0399	0.0399	0.0399	0.0399	0.0399

No.	Sym Od170um 3d4t	Sym Od170um 3d4t_md	Sym Od170um 3d6t	Sym Od170um 3d6t_md	Sym Od180um 3d3t_nol	Sym Od180um 3d3t_nol_ md
Qmax	10.13	11.132	5.308	5.479	10.721	11.223
Q@ 2.4GHz	6.85	6.91	4.774	4.871	6.67	6.705
Q@ 5.2GHz	10.13	11.13			10.7	11
L@ 2.4GHz	3.813	3.81	9.376	9.355	2.257	2.261
L@ 5.2GHz	4.977	4.94			2.514	2.508
fsr(GHz)	9.5	9.5	5.8	5.8	14.3	14.1
Area(mm^2)	0.0289	0.0289	0.0289	0.0289	0.0324	0.0324

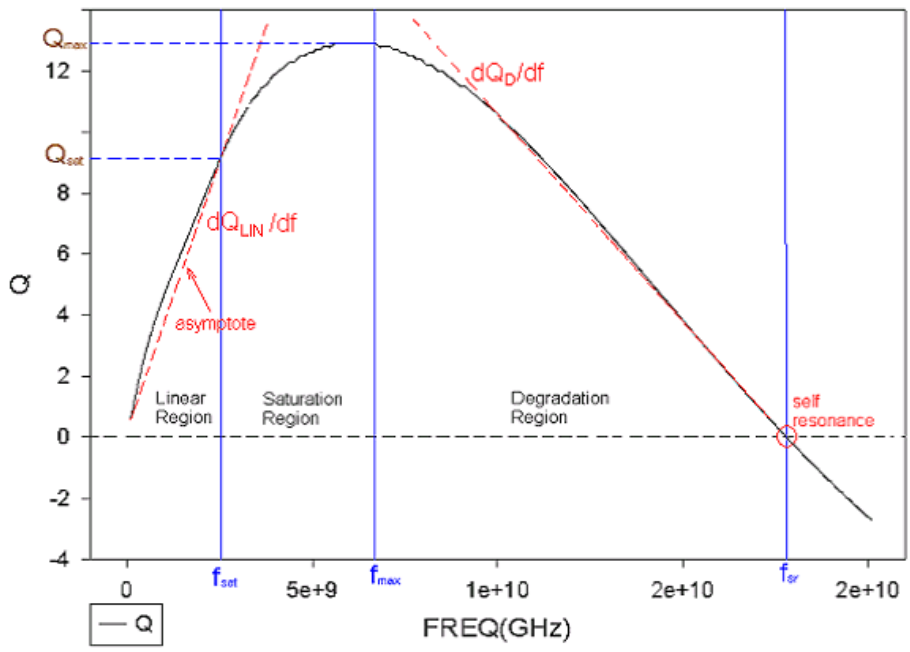
Table 3.4-1 Measurement data of the inductors taped out in UMC 0.18um 1P6M process.

The quality elevation is limited intuitively as only the eddy currents are reduced since not only the substrate loss but also the capacitive coupling distorts the inductor quality.

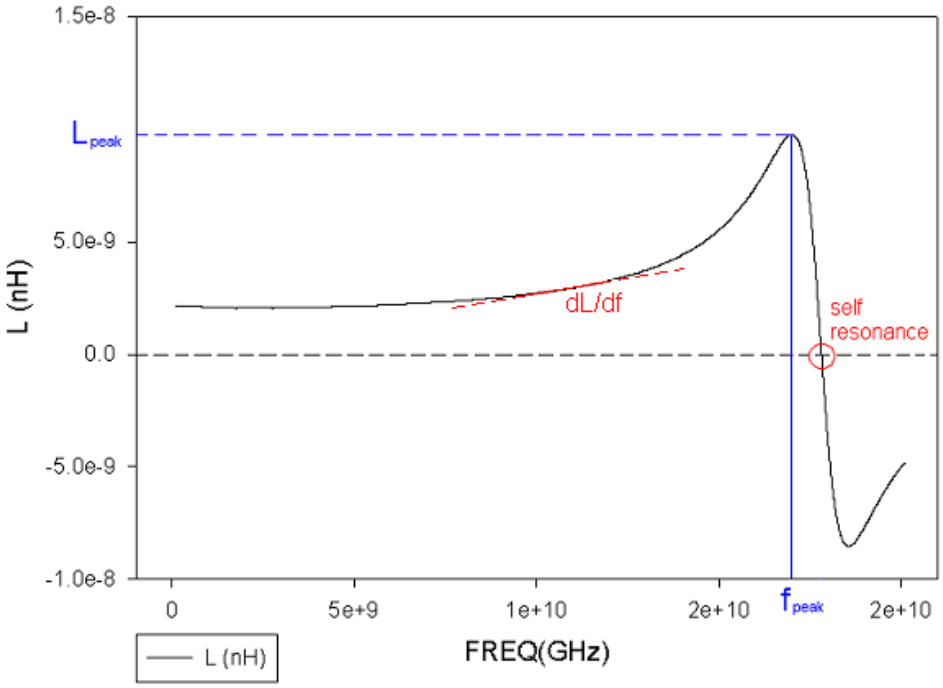
Chapter 4 Inductor Modeling

4.1 Introduction

Several RF circuit researchers promote complicated inductor models for broadband circuit application. Horng [12] suggested a modified T equivalent circuit for modeling LTCC inductors. Nevertheless, more accuracy needs more computation resource. For most circuits, Q implies the insertion loss or the noise performance; L implies the matching or resonance frequency, and narrow band model suffices. That means we just ought to make the curve fitting of Q and L from modeling to measurement results. Figure 4.1-1 demonstrates that the trend of inductor quality factor depends on frequency variation. According to the physical analysis, it can be divided into three sections, such as linear, saturation and degradation regions.



(a)



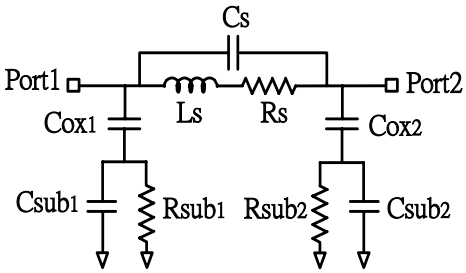
(b)

Figure 4.1-1 (a) The trend of inductor quality factor can be divided into three sections, such as linear, saturation and degradation regions, (b) the inductance value varies with frequency.

The simple model composed of a resistor in series with an inductor dominates at low frequency, as shown in Figure 4.1-2. The linearity can be approximated by an asymptote. The slope of Q_{LIN} as well as even the successive Q_{max} is determined by the ratio of inductance and resistance (see Razavi [8]).

Figure 4.1-2 RL series model.

When the frequency ascends to f_{sat}, the corresponding Q tends to saturate. Either electric or magnetic coupling effect appears to distort the linearity of Q. After arising to Q_{max}, it declines until the self-resonance. According to the experience of model tuning, the dependence of performance on each component is realized and the relationship among them is organized in Table 4.1-1.



Parameter / Influence / Component	Q_{sat}	Q_{max}	f_{sat}	f_{max}	f_{sr}	L_{peak}	f_{peak}	$\frac{dQ_{LIN}}{df}$	$\lvert\frac{dQ_D}{df}\rvert$	$\frac{dL}{df}$
C_{ox} ↑	↓	↓	↓	↓	↓	↓	↓			↑
C_{sub} ↑		↑		↑	↓	↑	↓		↑	↑
R_{sub} ↑		↑		↑	↑	↑			↓	↓
C_s ↑		↓		↓	↓		↓		↑	↑
L_s ↑	↑	↑	↑	↓	↓		↓	↑		↑
R_s ↑	↓	↓		↓				↓	↓	

Table 4.1-1 The guide of inductor model tunning.

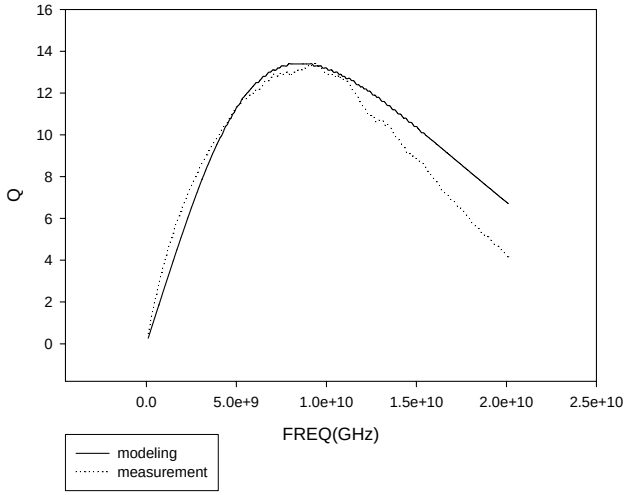
Comment: The all parameters come from Figure 4.1-1.

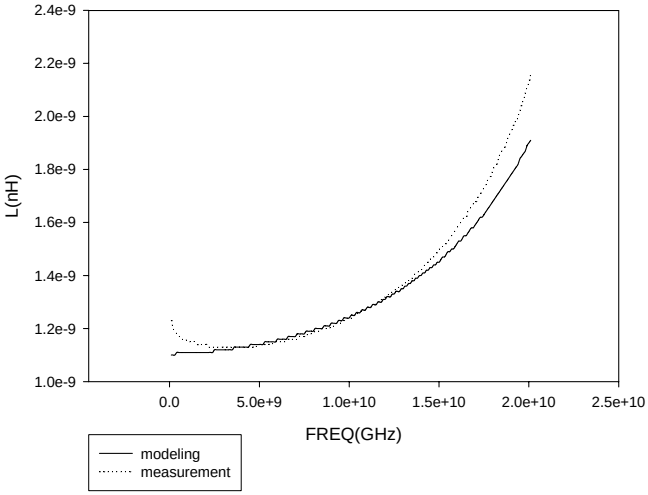
4.2 Modeling In Contrast to Measurement Results

The high accuracy of our inductor models can be proven in contrast to the measurement results by put them together. Even for the broadband circuit application, the models are appropriate.

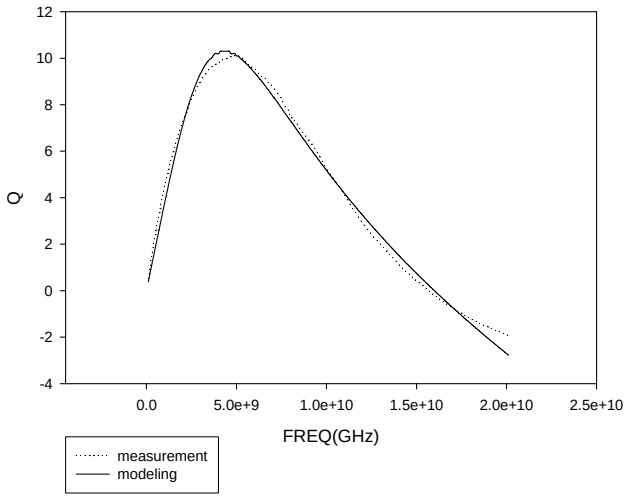
TSMC 0.18um 1P6M:

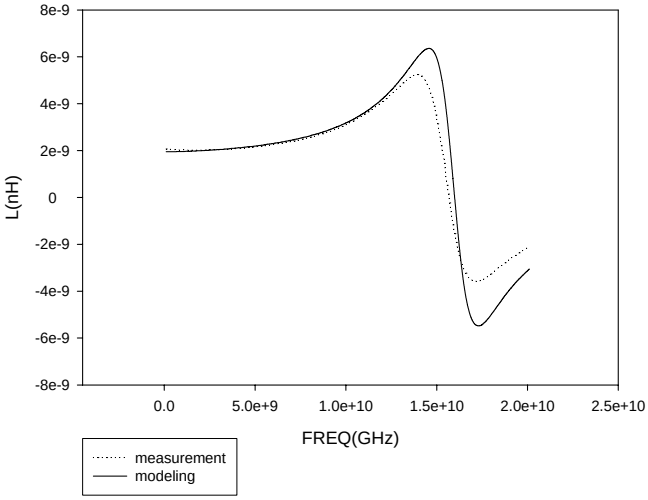
sym_od210um_3m2t





sym_od210um_3m3t





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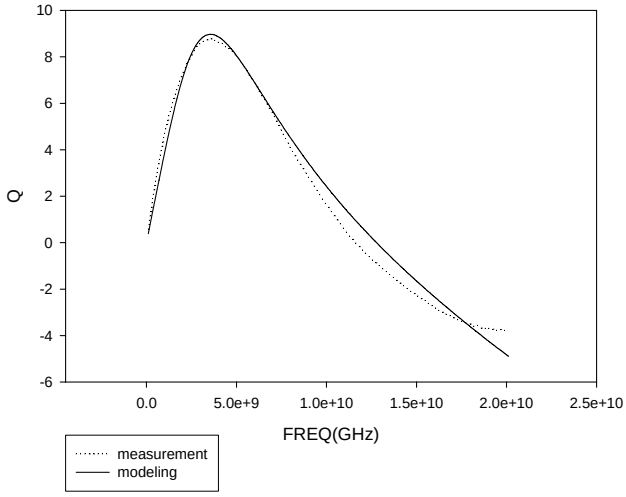
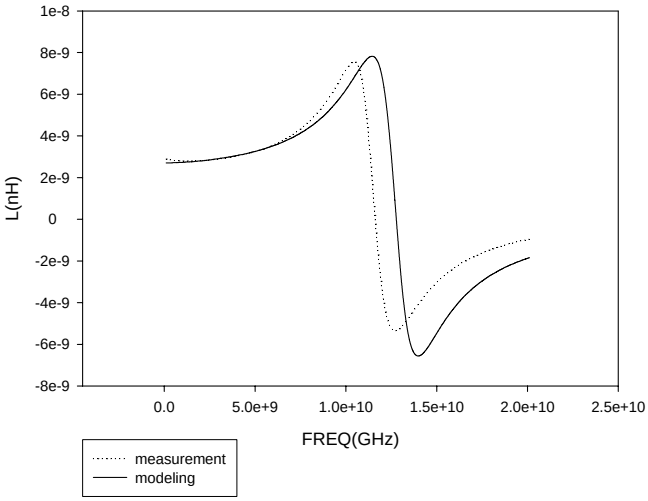
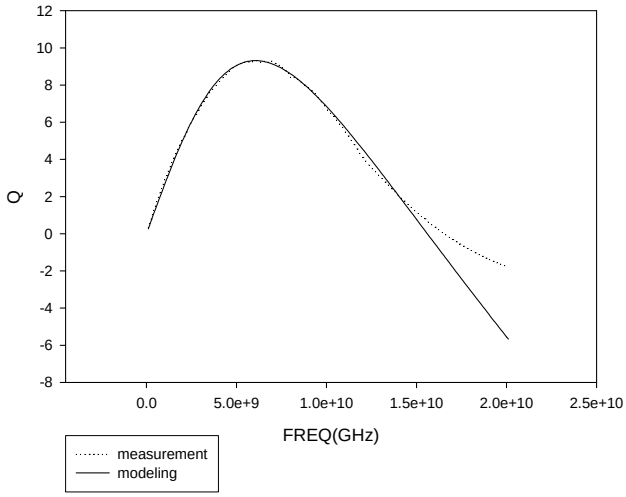
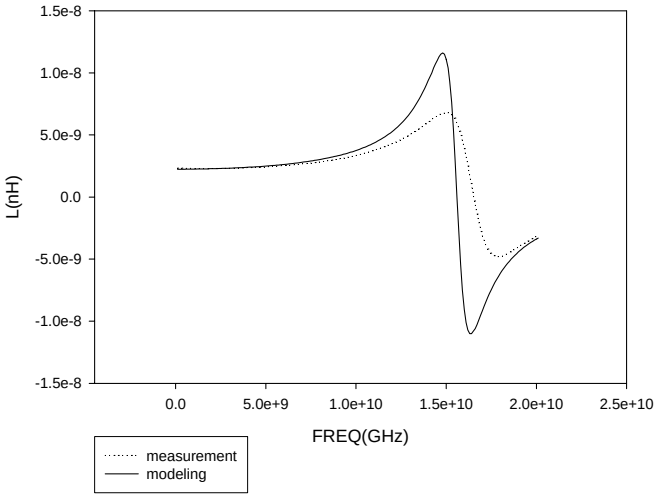


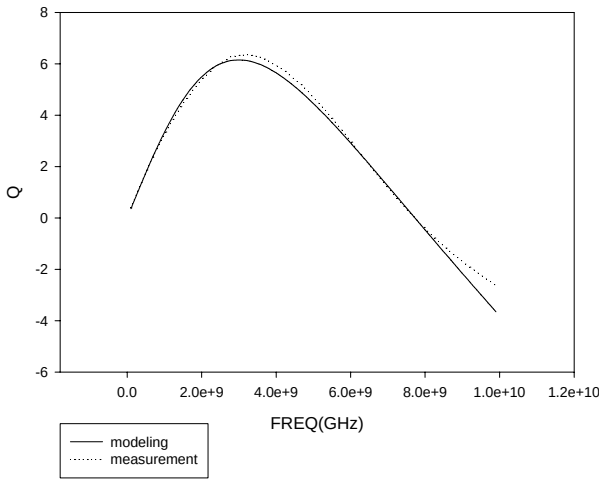


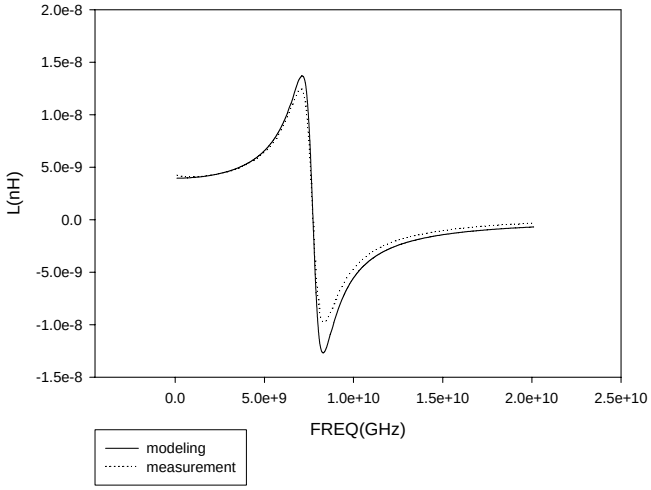
sym_od180um_3d3t_nol



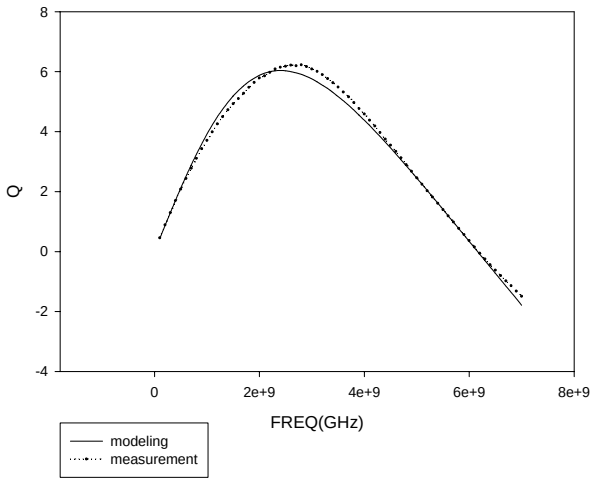


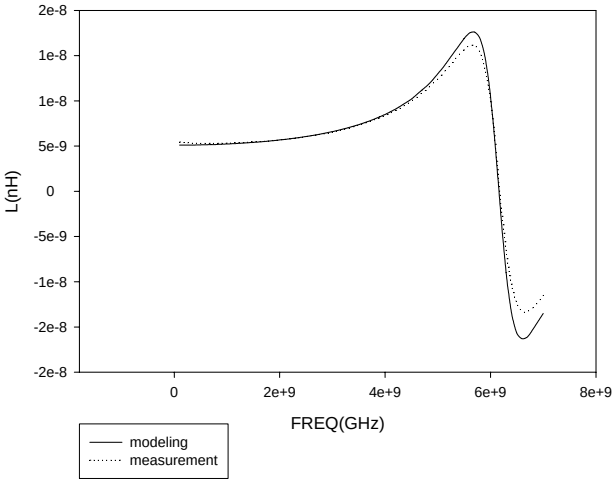
sym_od210um_3d4t_nol





sym_od210um_3d5t_nol





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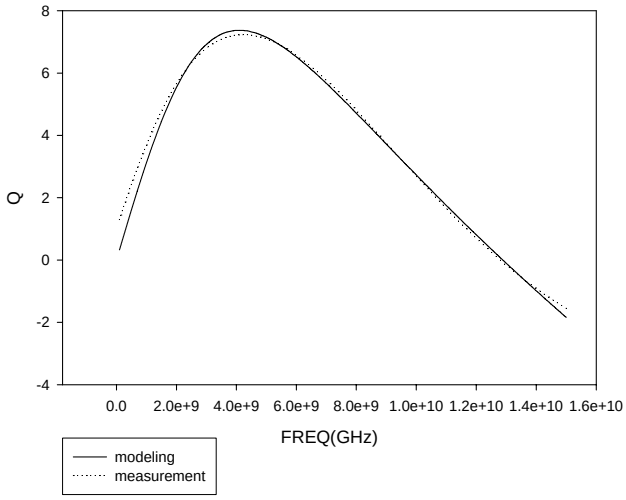

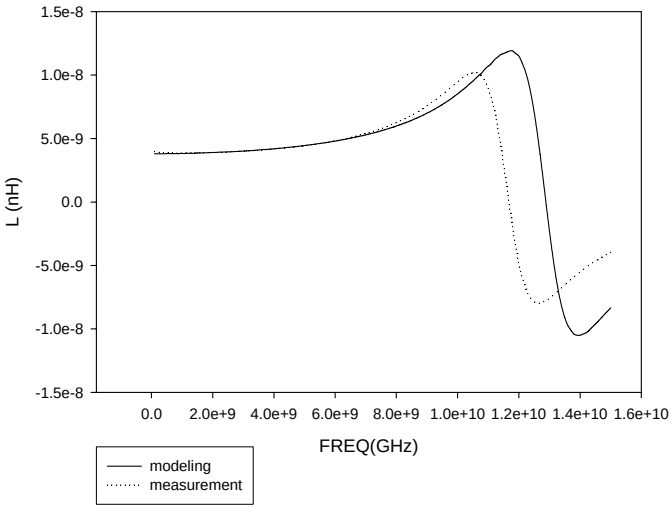

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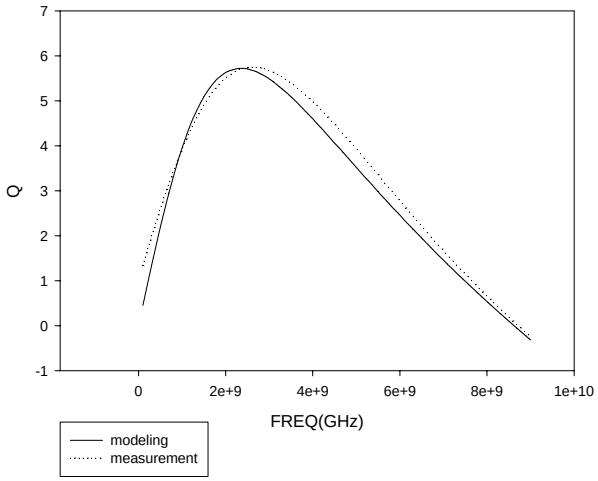
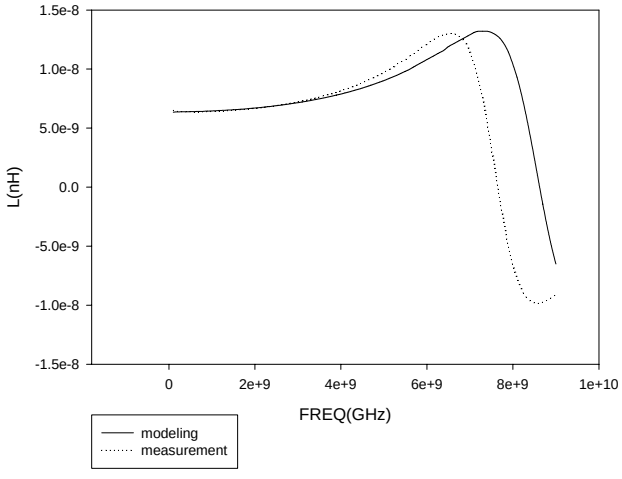
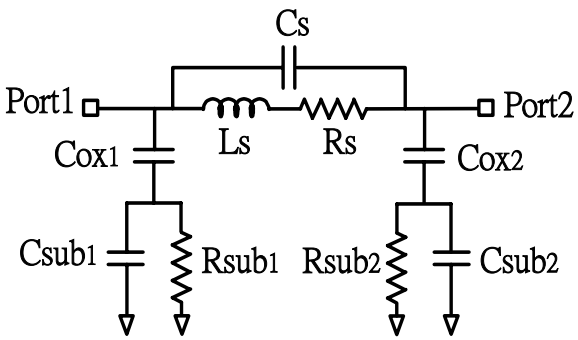




The value of each device is listed in Table 4.2-1



No.	sym_ od160um_ 3d4t	sym_ od210um_ 3d5t	sym_ od180um_ 3d3t_nol	sym_ od210um_ 3d4t_nol
Cs(pF)	0.012	0.024	0	0.089
Rs(Ohm)	7.37	8.877	5.27	6.29
Ls(nH)	3.805	6.45	2.25	3.995
Cox1(pF)	0.134	3.14	0.36	1.5
Cox2(pF)	0.13	3.2	0.4	1.3
Csub1(pF)	0.035	0.029	0.053	0.017
Csub2(pF)	0.03	0.03	0.05	0.0158
Rsub1(Ohm)	1317	1379	2212	1261
Rsub2(Ohm)	1300	1360	2000	1200

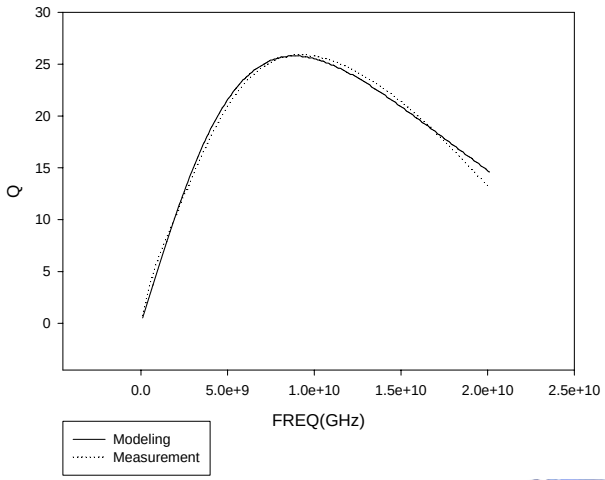
No.	sym_ od210um_ 3d5t_nol	sym_ od210um_ 3m2t	sym_ od210um_ 3m3t	sym_ od210um_ 3m4t
Cs(pF)	0.06	0	0.0135	0.01825
Rs(Ohm)	6.8	2.592	3.24	4.363
Ls(nH)	5.15	1.105	1.95	2.711
Cox1(pF)	1.845	0.045	0.075	0.0786
Cox2(pF)	1.8	0.05	0.07	0.0744
Csub1(pF)	0.069	0.051	0.0684	0.0684
Csub2(pF)	0.07	0.0504	0.05	0.0504
Rsub1(Ohm)	1460	449	345.6	345.6
Rsub2(Ohm)	1450	440	360	360

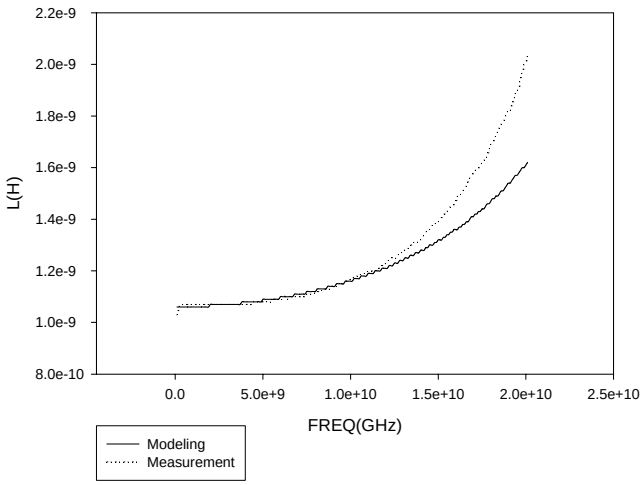
Table 4.2-1 The component values of the inductor compact PI model

(by TSMC 0.18um 1P6M process).

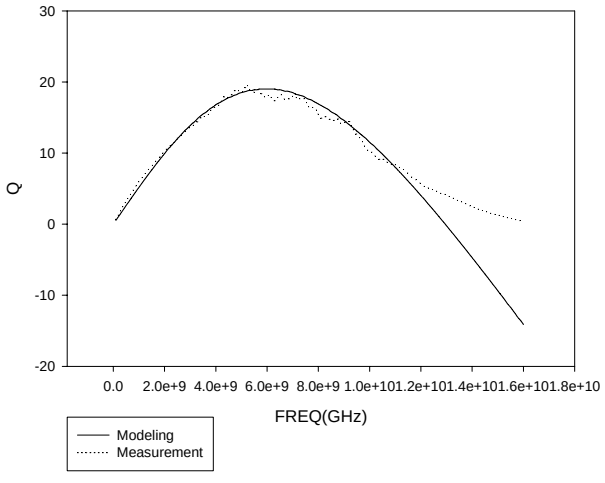
UMC 0.18um 1P6M:

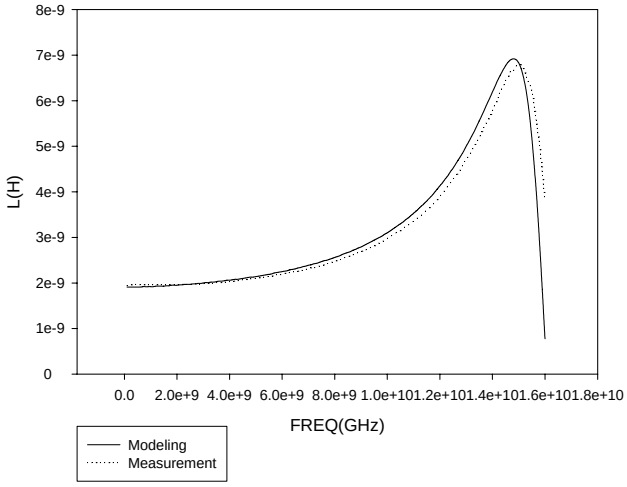
sym_od210um_3m2t



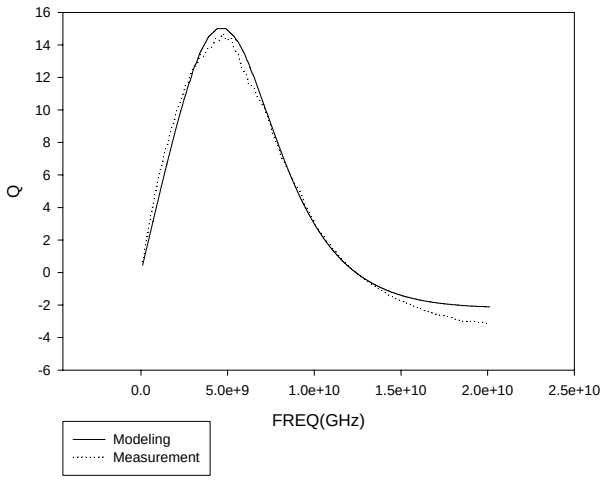


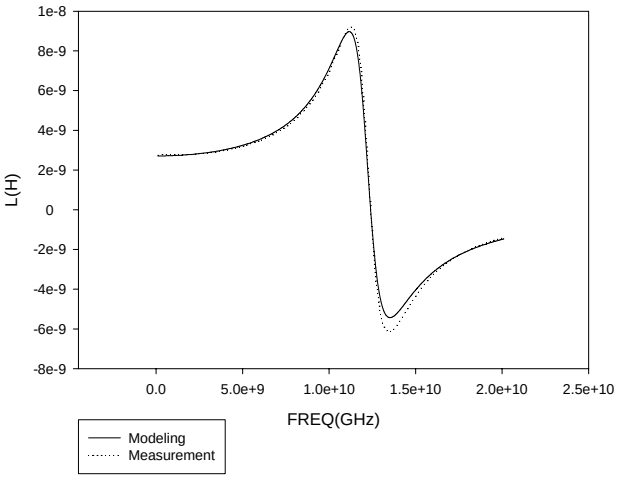
sym_od210um_3m3t



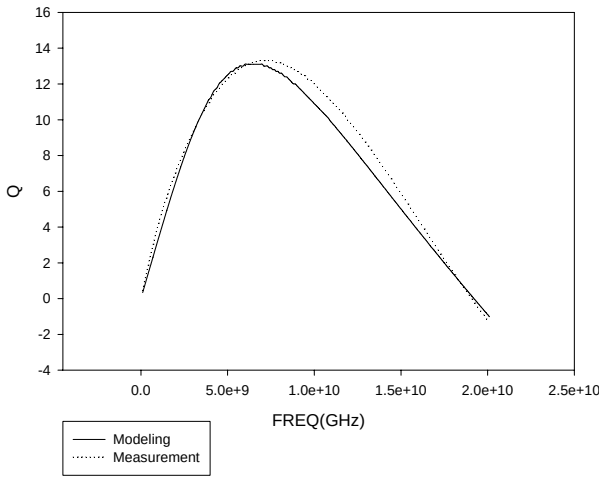


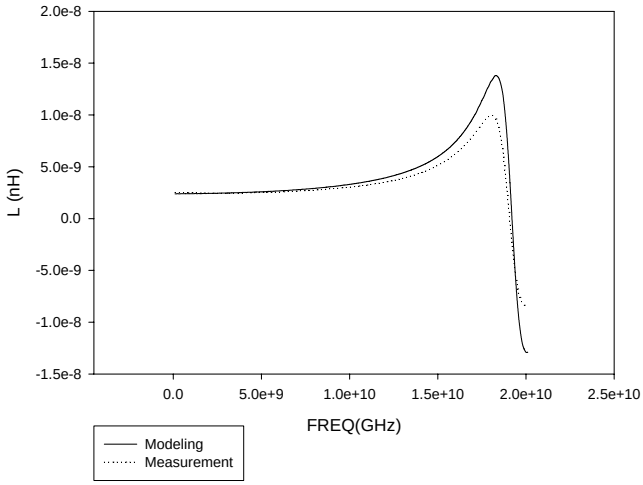
sym_od210um_3m4t



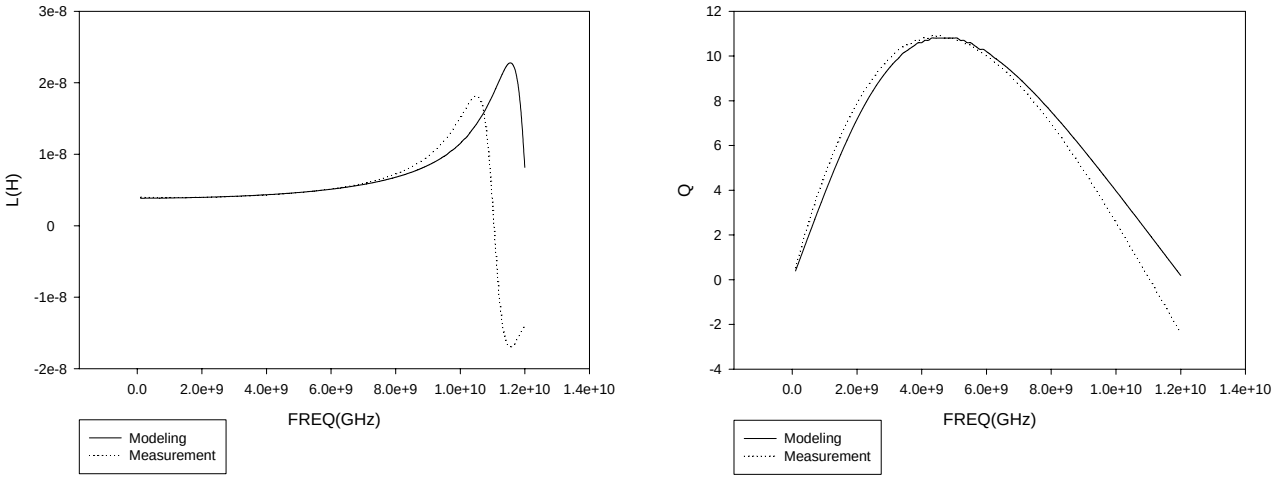


sym_od180um_3d3t_nol

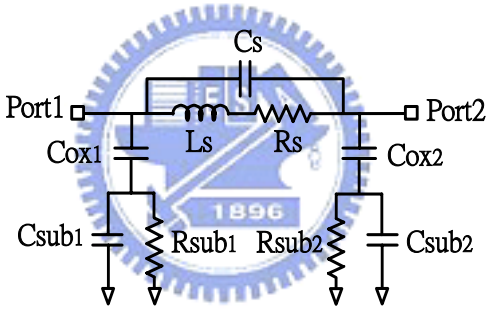




sym_od160um_3d4t



The value of each device is listed in Table 4.2-2



No.	Sym_ od210um_ 3m2t	Sym_ od210um_ 3m3t	sym_ od210um_ 3m4t	sym_ od180um_ 3d3t_nol	sym_ od160um_ 3d4t
Cs(pF)	0.0008	0.0183	0.0022	0	0.0044
Rs(Ohm)	1.2472	2.2744	3.75276	4.5	6.17746
Ls(nH)	1.06	1.9	2.71	2.394	3.845
Cox1(pF)	0.03608	0.108	0.06048	0.0413	0.064
Cox2(pF)	0.03	0.1	0.06	0.05	0.04
Csub1(pF)	0.00996	0.141	0	0.09	0.108
Csub2(pF)	0.00996	0.14	0	0.1	0.095
Rsub1(Ohm)	2120	1413	38.26	374	612
Rsub2(Ohm)	2000	1441	40	370	600

Table 4.2-2 The component values of the inductor compact PI model

(by UMC 0.18um 1P6M process).

Chapter 5 Application --- A 5.2GHz Oscillator

Inductors with high quality and accurate model have been developed by our design methodology. The inductor numbered as sym_od210um_3m3t taped out in UMC, where the corresponding maximum quality factor Q_{max} is 19.6, inductance value is 2.12nH at 5.2 GHz, is incorporated to embody a 5.2 GHz oscillator. Oscillators are the most sensitive to inductor quality than any other circuits, i.e. the quality of LC tank directly responds to the phase noise performance (see Leeson [13] and Razavi [14]). The circuit architecture comprises a negative resistance and a LC tank as well as provides differential output configuration (see Gonzalez [15]).

5.1 Oscillation Theory

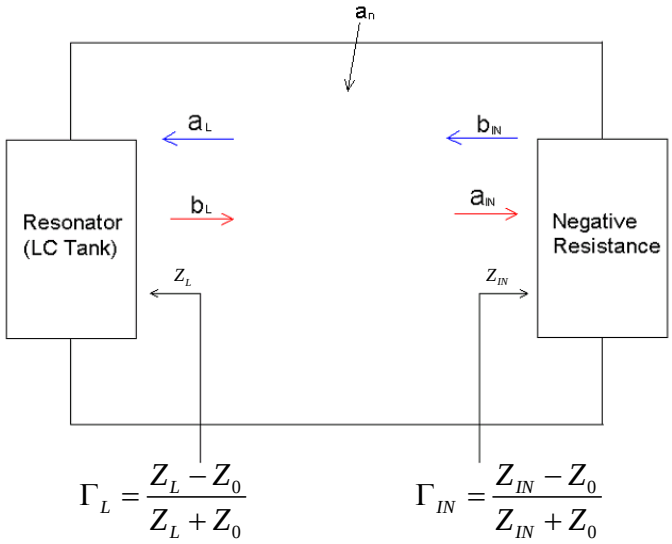
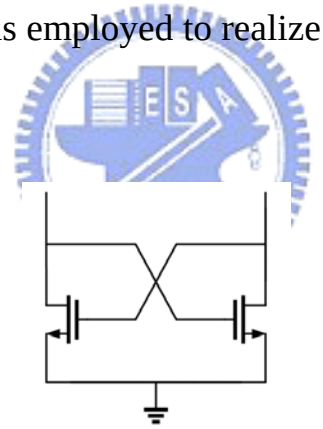


Figure 5.1-1 A closed loop form of oscillatory circuits: a small noise signal a_n is generated in the loop externally or internally. Letter 'a' signifies incident waves, and letter 'b' signifies reflective waves.

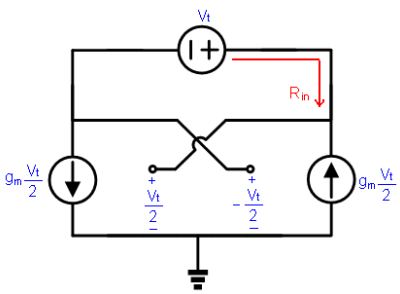
An oscillator is a one-port configuration circuit, where the input and the output are the same. Oscillation is usually initiated by any noisy signal. Consider the closed loop form [3] shown in Fig. 5.1-1, a small noise a_n is generated externally or internally. When it propagates toward the negative resistance, the power more than itself reflects since $|b_i|=|a_i||\Gamma_{IN}|$, $|\Gamma_{IN}|>1$. Furthermore, the growing wave power keeps going on and it is absorbed or consumed except at the resonance frequency. Therefore, only the signal of resonance frequency remains and recycles periodically in the closed loop.

I. Negative Resistance

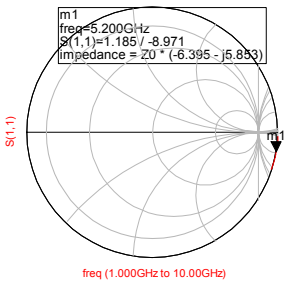
A NMOS cross couple is employed to realize the negative resistance.



(a)



(b)



(c)

Figure 5.1-2 Negative resistance realization:
(a) topology, (b) equivalent small signal model, (c) Smith chart test.

According to the small signal circuit model plotted in Fig. 5.1-2 (b), the current returns when apply a voltage to a NMOS cross couple, thus a negative resistor is obtained.

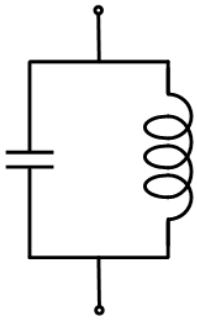
$$R_{in} = -\frac{V_t}{\frac{1}{2} g_m V_t} = -\frac{2}{g_m} \qquad \text{Eq. (5.1-1)}$$

$$g_m = k_n'(\frac{W}{L})(V_{GS} - V_t) = \sqrt{2k_n'(\frac{W}{L})I_D} \qquad \text{Eq. (5.1-2)}$$

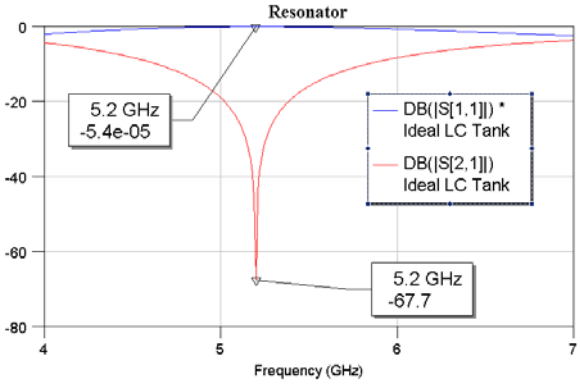
The above equations imply that the absolute value of negative resistance is inversely proportional to the root of NMOS bias current I_D as well as indicate that large voltage swing degrades oscillator output power.

II. Resonator

An ideal resonator realized by a LC tank (in parallel) can be viewed as a band reject filter, that is, it impedes infinitely (open circuit) and totally reflects incident signal power at resonance.



(a)



(b)

Figure 5.1-3 An ideal resonator is realized by a parallel LC tank, (a) schematic view, (b) S- parameter frequency response, where the extremely small return loss and the large attenuation are obtained at resonance.

5.2 Differential Stimulation to Enhance Inductor Quality

It has been mentioned previously that differential-driven can minimize coupling effect of inductors thereby Q should be raised, as demonstrated in Fig. 5.2-1 and Fig. 5.2-2.

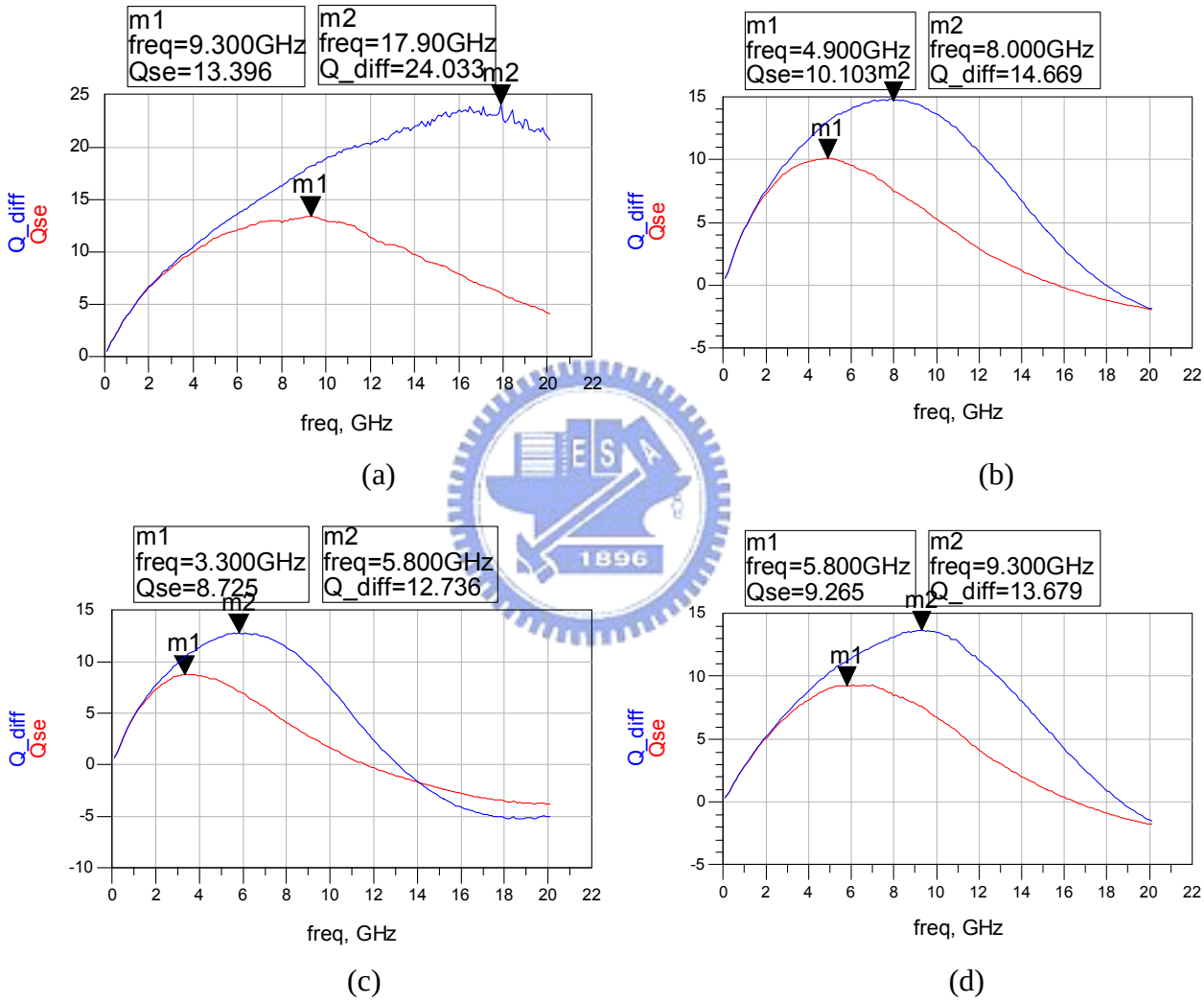
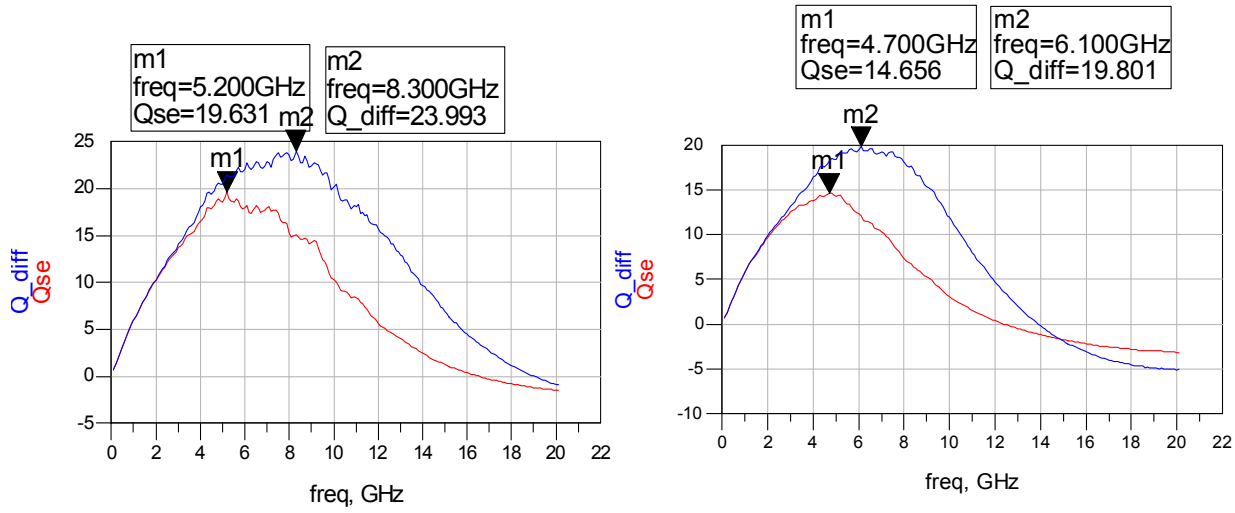


Figure 5.2-1 Quality factors of single ended and differentially driven inductor tapeout in TSMC: (a) sym_od210um_3m2t, (b)sym_od210um_3m3t, (c)sym_od210um_3m4t, (d) sym_od180um_3d3t_nol.



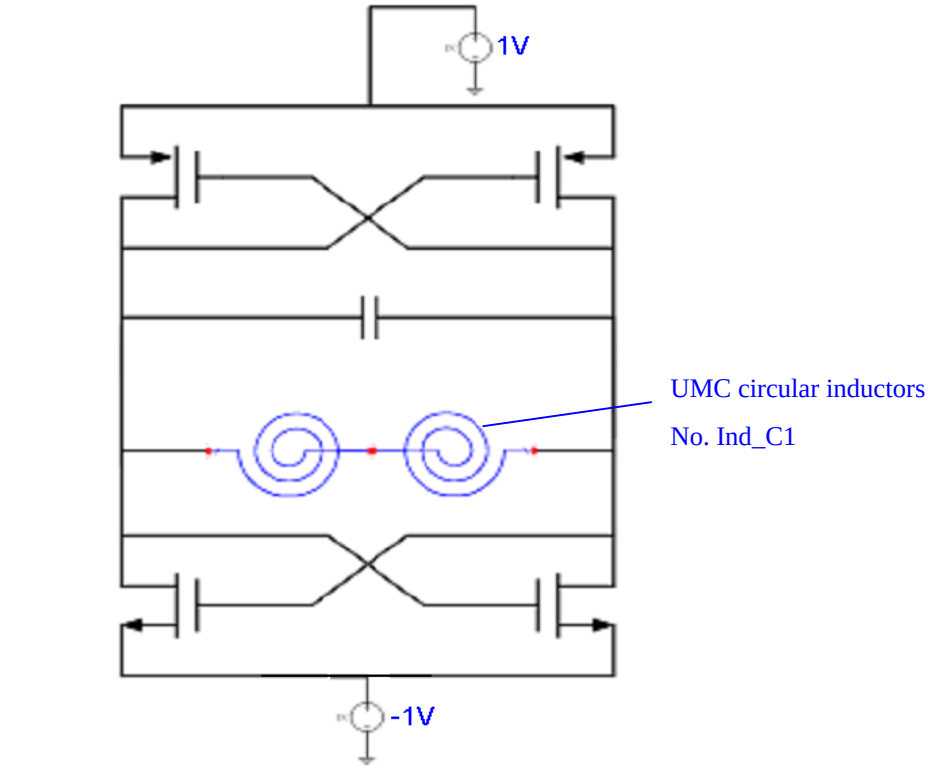
(a) (b)

Figure 5.2-2 Quality factors of single ended and differentially driven inductor tapeout in UMC: (a) sym_od210um_3m3t, (b)sym_od210um_3m4t.

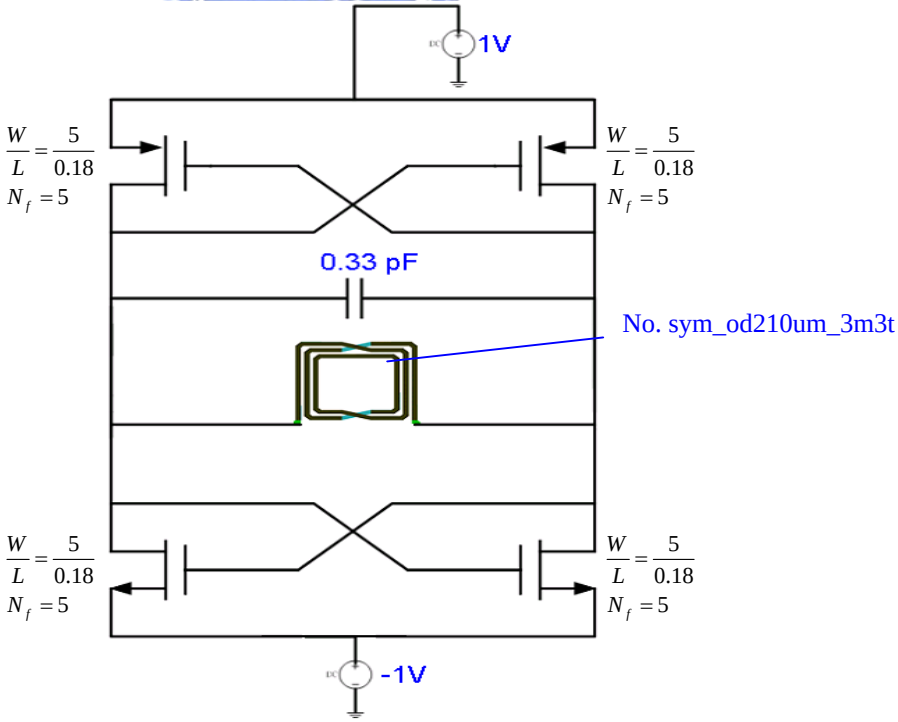
As anticipated, differential-driven improves the linearity and postpones the distortion. The quality factors are certainly elevated case by case. Meanwhile, the corresponding f_{max} to Q_{max} shifts to high frequency.

5.3 Circuit Performance Demonstration

The circuit simulation of a 5.2GHz oscillator that incorporates the equivalent inductor model of No. sym_od210um_3m3t is displayed at this section. Phang [16] set up two opposing connected inductors instead of one for balance, e.g. inductance of 2nH is divided into half, so the two 1nH inductors are connected in series, as depicted in Fig. 5.3-1(a).



(a)



(b)

Figure 5.3-1 A 5.2 GHz Oscillator schematic view, (a) common configuration, (b) two inductors in series are replaced by only one of the symmetrical type.

The phase noise performance of oscillators incorporate UMC inductors is not available since foundries don't release the accurate models for free as usual, but anyhow the inductors incorporate symmetrical design can save three times the chip area more at least. The transistor size is chosen to be the minimal allowable value such as $\frac{W}{L}=\frac{5}{0.18}$, $N_f=5$, to guarantee circuit oscillation, where N_f is the finger number.

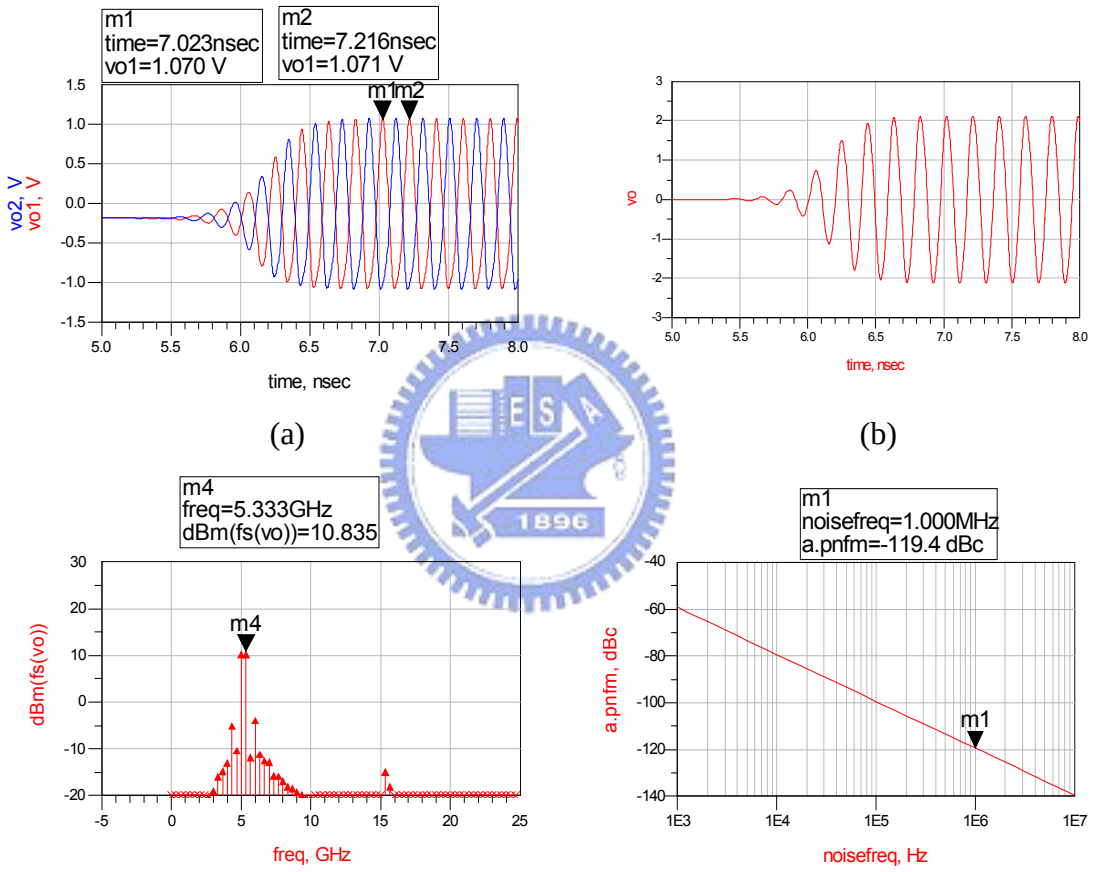


Figure 5.3-2 A 5.2 GHz Oscillator, (a) transient response (single ended), (b) transient response (differential mode), (c) spectrum analysis (differential mode), (d) phase noise.

Therefore, an oscillator is acquired that output swings $\pm 2\,V$ and outputs power 10.835dBm for differential operation; the phase noise approaches -120 dBc/Hz for 1MHz offset, at 5.2GHz.

Chapter 6. Conclusions & Future Work

The feature of balanced geometry and three-dimensional structure has achieved the design goal of high quality and small area inductors successfully. The novel concept related to substrate effect decoupling is proposed in the thesis. Whatever the approaches to resolve the problematic coupling effects, an issue concerned with the corresponding f_{max} to Q_{max} shifts to high frequency must be addressed. A loss is acquired more than gain if we try to move f_{max} downward because the metal sheet resistance dominates the quality at low frequency. Conventional CMOS RF IC's suffer from the various parasitic effects caused by insulators, conductors and lossy substrates. Advanced semiconductor technology provides cupper and low k dielectric process, which is more compatible with RF circuit design. Magnetic decouplers only can reduce eddy currents; displacement currents still remain in substrates. A low loss or high isolation substrate must be developed; maybe floating N-well array in P-substrate is a great choice.

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