A Fast Algorithm for the Analysis of Meander Delay Line

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Abstract

In high-speed digital system, in order to synchronize the logic gates, use of delay line in board level interconnection is usually required. A popular delay line design is the meander delay line.

In this thesis, we develop an equivalent circuit approach to analyze the stripline type of meander delay line. The all structure is composed by one or more unit cells, and each unit cell can be constructed from three types of building block.The full wave analysis program-HFSS is first used to determined the S parameters of each building block, which are then, it can be transformed into the two-port Z parameters for the extraction of T-type equivalent circuit parameters. These circuits are them cascaded to from the equivalent circuits of a single unit cell and the complete delay line structure. SPICE simulation is then performed to evaluate delay lines transmission characteristics. For a fixed coupled-line spacing, the ability to analyze structures with different numbers of unit cell and/or lengths of coupled line are the two main advantagesof the proposed method of analysis..

In the application, we discuss the two common phenomenon of the meander delay line: (1) speed-up of the signal due to inductive/capacitive

coupling between coupled lines and(2) the ladder wave distortion. From the results obtained, it’s found that: (1) if the total length is fixed, using less number of unit cells which results in longer coupled line length, ladder wave becomes serious, especially for the narrower coupled line spacing. (2) On the contrary, increasing the number of unit cells, the effects of bends increase, but ladder wave distortion is redused, especially when coupled line spacing gets wider. (3)Although wider coupled line spacing can improve the signal transmission, it consumes more board areas.