國 立 交 通 大 學

電信工程研究所

碩 士 論 文

使用開放式精簡指令集處理器

應用於即時偵測失神性癲癇動物模型之軟硬體共同實現

Software-hardware Co-implementation for Real-time Epileptic Seizure Detection Using OpenRISC Processor Core on Absence Animal Models

研究生：張舜婷

指導教授：闕河鳴

中 華 民 國 一 百 年 十 二 月


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研究生：張舜婷　　Student: Shun-Ting Chang

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中 華 民 國 一 百 年 十 二 月

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摘要

癲癇是一種最常見的神經系統失調疾病之一，全球有 1%的人罹患癲癇，25%的癲癇病患無法完全被治癒。在過去幾年，開迴路的癲癇控制器已經被提出，如迷走神經刺激和腦深部刺激，但連續性或間歇性的電刺激會導致高功率消耗以及神經細胞損害的可能性。相反的，近年來閉迴路的硬體和生理訊號處理器已經被提出。但這些研究中，在癲癇發作 5 秒後才會偵測到癲癇或者是沒有提及偵測時間。此外，大部分的研究通常是利用片段的腦電圖驗證癲癇演算法，無法全然地證實演算法的健全性。因此，在過去我們提出一套無線可攜式即時癲癇偵測與抑制系統，並使用連續性的腦電圖長時間偵測癲癇。

在本篇論文中，改進上述所提出的即時癲癇偵測閉迴路系統的決定參數方式，提出一個快速決定參數方法，使這些參數最適合每個老鼠的模型。這個快速決定參數方法比先前決定參數的方法快了 416×10^6 倍，同時也可達到 92-99%的高偵測率以及可以在 0.63-0.79 秒偵測到癲癇。此外，使用精簡指令集的技術實現一個低功耗的生理訊號處理器，將偵測癲癇演算法實現在生理訊號處理器上可達到即時處理生理訊號以及只消耗 6 mW。與先前提出的系統比較，可以降低 93.8%的功率消耗。本篇所提出的癲癇偵測器可應用於即時偵測系統中，以及在未來可以與類比前端電路和後端刺激器整合成一個積體化的閉迴路偵測系統。

Software-hardware Co-implementation for Real-time Epileptic Seizure Detection Using OpenRISC Processor Core on Absence Animal Models

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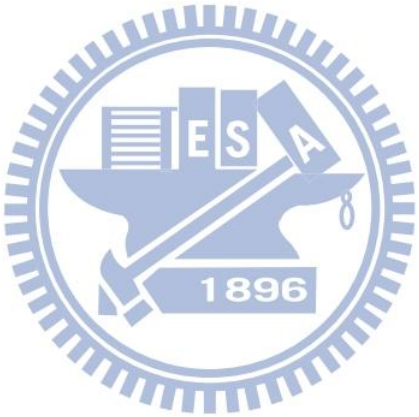
Abstract

Epilepsy is one of the most common neurological disorders. Approximately 1% of people in the world suffer from epilepsy, and 25% of epilepsy patients cannot be healed by today's available treatments. In past years, open-loop seizure controllers have been proposed, such us vagus nerve stimulation and deep brain stimulation devices; however, the device drives a stimulator continuously or intermittently that causes high power consumption and the likelihood of neuronal damage. In contrast, the closed-loop implementation of hardware prototypes or biomedical signal processors has been proposed recently. Nevertheless, the average of seizure detection delay is either longer than 5 seconds or often not mentioned in these works, and it is insufficient to validate the robustness of detection algorithm. Moreover, most of studies often use the discontinuous electroencephalogram (EEG) signal fragments to validate seizure detection algorithm. As a result, a portable wireless online closed-loop seizure controller in freely moving rats was proposed, which validated seizure detection algorithm by using continuous online EEG signals.

In this thesis, the fast parameter determination method, which determines a fitting model for each rat, is proposed to improve our previous work. The proposed parameter determination method is 416×10^6 times faster than our previous work, and it can attain the same detection accuracy (92-99%) and detection delay (0.63-0.79 s). Additionally, a low-power biomedical signal processor which bases on reduced instruction set computer (RISC) technology consumes only 6 mW for real-time epileptic seizure detection algorithm. Compared with our previous prototype, the measurement results show that the implemented processor can reduce 93.8% power consumption. The developed seizure detector can be applied to monitor the online EEG signals and integrate with analog front-end circuitries and an electrical stimulator to perform a closed-loop seizure controller in the future.



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經過了兩年半，終於實現了生日願望。這兩年半，曾經很茫然，不知道要做什麼，要休學要放棄的念頭出現過好幾百回，最後還是膽小地不敢放棄。到如今可以拿到碩士學位，首先，我要感謝我的老師闕河鳴，您讓我學習到思考要有邏輯，做事情要有效率以及口語表達的能力，讓我在可以進入社會前，可以有一個紮實的訓練。

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舜婷

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Chapter 1 Introduction

Epilepsy is one of the most common neurological disorders. Approximately 1% of people in the world suffer from epilepsy, and 25% of epilepsy patients cannot be healed by today's available treatments [1, 2]. If seizures cannot be well controlled, the patients experience major limitations in family, social, educational, and vocational activities.

1.1 Motivation

Recently, numerous alternative techniques have been proposed, such us vagus nerve and deep brain stimulation devices [1, 2]. Most of the devices utilize open-loop controller to suppress the seizure. However, an open-loop controller drives a stimulator continuously or intermittently that causes high power consumption and the likelihood of neuronal damage. In contract, a closed-loop device combines a stimulator and seizure detector. Recently, one closed-loop epilepsy control system developed by NeuroPace called Responsive Neurostimulator (RNS®) System is in U.S. FDA clinical trials [2]. A closed-loop device can increase stimulus efficacy and reduce tissue damage over the long term. A closed-loop seizure controller drives a stimulator when a closed-loop device detects the seizure [2-4]. Despite additional hardware, a closed-loop device can increase stimulus efficacy and reduce tissue damage over the long term. As a result, compared with open-loop devices, closed-loop devices is more effective and attractive. In general, a robust on-line seizure detection method, which can drive antiepileptic device to suppress the seizure as early as possible when a seizure happens, is required for the development of a closed-loop seizure controller.

Recently, the implementation of hardware prototypes and biomedical signal processors has been proposed [5-19]. Among these projects, wavelet analysis, spectral analysis, entropy analysis, and variance analysis are applied to detect seizure events. Some closed-loop seizure controllers utilized analog to extract seizure features so epileptic seizure detection accuracy was high [15, 18]. Some seizure detection algorithm relied on powerful processing platform keeping real-time seizure detection and high detection accuracy [9-11, 13, 17]. However, the average response time for seizure detection is either longer than 5 seconds or often not mentioned in these works. Moreover, most of studies often use the discontinuous electroencephalogram (EEG) signal fragments to validate seizure detection algorithm; nevertheless, it is deficient in validating the robustness of detection algorithm. As a result, a portable wireless online closed-loop seizure controller in freely moving rats was proposed [20-23], which validated seizure detection algorithm by using continuous online EEG signals. Furthermore, the detection delay is shorter than 1 second. To summarize, an open-loop seizure controller with periodic stimulation is inaccurate and inefficient as shown in Fig. 1.1 (a). A closed-loop seizure controller with responsive stimulation which is proposed by other groups as mentioned above is more accurate and efficient; however, the detection delay is longer than 5 seconds as shown in Fig. 1.1 (b). Fig. 1.1 (c) shows that a closed-loop seizure controller with responsive stimulation is proposed by our group. When a seizure occurs, the responsive stimulator starts to suppress the seizure, and the detection delay is shorter than 1 second.

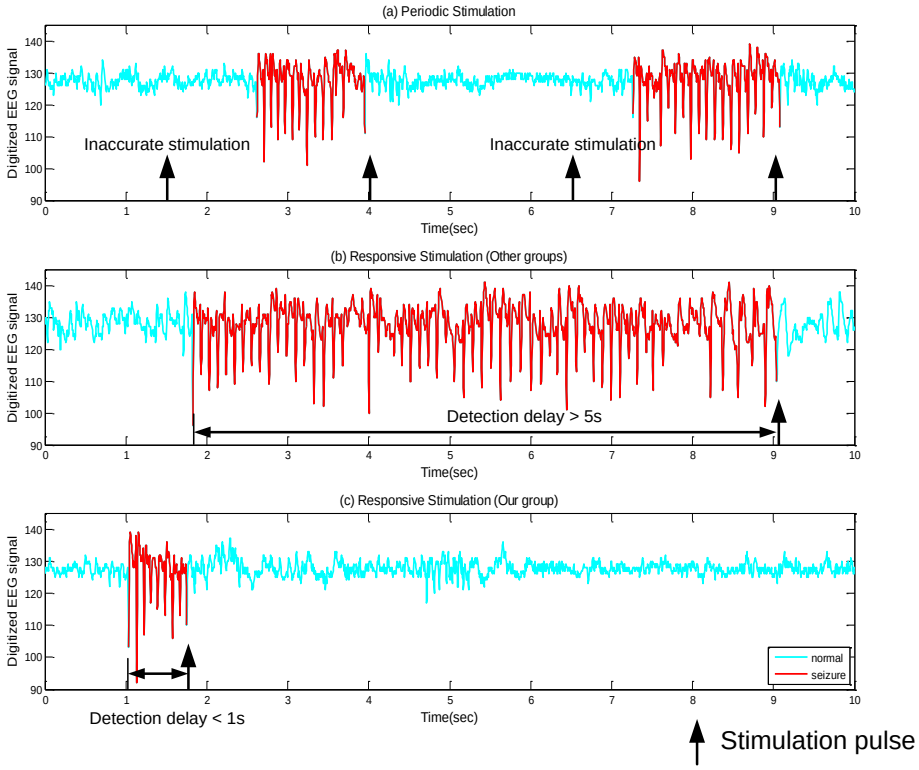


Fig. 1.1 A diagram of (a) periodic stimulation,

(b) responsive stimulation (other groups), and (c) responsive stimulation (our group).

1.2 Study Objective

In our previous work, using implied approximate entropy and 64-point fast Fourier transform, which contained large portion of digital processing, increased detection rate. In order to decrease complex calculation and hardware area, a liner least squares (LLS) was classifier in this project. Furthermore, it was observed that most of false detections occurred in slow-wave sleep (SWS) state, so adaptive thresholds were utilized to switch the threshold of the LLS for decreasing false detection rate. However, adaptive thresholds were obtained by using exhaustive key search in training phase; as a result, this method wasted a lot of time on training phase. In addition, implementation based on 8051-like microcontroller [24] consumed more than 117mW to perform the real-time seizure detection.

In this study, it is proposed that using the mean and standard deviation of EEG training data searches adaptive thresholds rapidly. The new parameter determination method is faster than our previous work, and it can attain same performance. Moreover, the seizure detection algorithm in previous work is implemented in a RISC-like processor to suppress seizures. The flexibility, simplicity, and fixed instruction format of RISC [25] is feasible implementation with high processing performance. Although more complicate hardware architecture is used to realize real-time seizure detection, the RISC-like processor does not run algorithm at full speed in processing biomedical signals. As a result, a slower clock rate is applied to reduce the power and energy consumption of the proposed system. The continuous EEG signals of four Long-Evens rats are applied to the proposed biomedical signal processor. The results show the embedded processor is robustly processing 24 hours long-term and uninterrupted EEG sequence. In the future, the development of proposed processor will integrate analog front-end and antiepileptic circuitries into system-on-a-chip design for neural prosthesis applications.

1.3 Thesis Organization

The content of this thesis is organized as follows. Chapter 1 introduces the motivation and objective of this work. Chapter 2 describes the preparation of animal models and recorded EEG training data. In Chapter 3, the system architecture of proposed biomedical signal processor is described. Chapter 4 presents the epileptic seizure detection algorithm and the proposed parameter determination method. Chapter 5 demonstrates the hardware and firmware implementation. In Chapter 6, the evaluation procedure and measurement results are presented. Finally the conclusion and future work are made in Chapter 7.

Chapter 2 EEG Data Acquisition

In this thesis, we use EEG signals of absence animal models to validate our seizure detection algorithm. As a result, first, we introduce what absence seizure is, how we prepare general animals, and how we define four state of continuous EEG recording.

2.1 Absence Seizure

Absence seizures are one of several kinds of seizures. These seizures are sometimes referred to as petit mal seizures. People may appear to be staring into space blankly. These periods last for seconds, or even tens of seconds. Sometimes, those experiencing absence seizures move from one location to another without any purpose. In normal circumstances thalamo-cortical oscillations maintain normal consciousness of an individual. However, in abnormal circumstances the normal pattern may be disrupted; as a result, people are led to an episode of absence [26].

The spike-wave discharge (SWD) is the archetype electroencephalographic characteristic of non-convulsive epilepsy. SWDs can be found in various types of absence epilepsy, including childhood absence epilepsy, juvenile absence epilepsy, juvenile myoclonic epilepsy, myoclonic absence epilepsy, eyelid myoclonia with absence epilepsy, and generalized tonic-clonic seizures in some patients.

Nowadays, genetic rodent models, such as GAERS and WAG/Rij rats, are most commonly used for studying new antiepileptic drugs, basic mechanisms of seizures and seizure related neurophysiological and neurochemical activities and processes. The frequency of the discharges in genetic rodent strains is 7-10 Hz [27, 28].

2.2 General Animal Preparation

Adult Long-Evans rats with spontaneous spike-and-wave discharge (SWD) are used in the thesis. There are two seizure types of Long-Evans rats in previous work, including absence seizures and pentylenetetrazol (PTZ) induced seizures. The genetic defect of Long-Evans rats causes spontaneous SWD. The EEG characteristic of spontaneous SWD is much closer to epileptic patients' EEG than PTZ induced SWD in the clinical aspect.

In this thesis, Long-Evans rats were 4-6 months old, and their weight was 500-700 grams. The rats were placed in a room under a 12:12-hour light-dark cycle with food and water provided ad libitum. All surgical and experimental procedures were reviewed and approved by the Institutional Animal Care and Use Committee of the National Cheng Kung University. The rats were anesthetized with sodium pentobarbital (50 mg/kg, i.p.). Subsequently, it was placed in a standard stereotaxic apparatus. Screw electrodes were bilaterally implanted over the area of the frontal barrel cortex (anterior 2.0 mm, lateral 2.0 mm with regard to the bregma). A four-microwire bundle, which was made of Teflon-insulated stainless steel microwires (#7079, A-M Systems), was used to stimulate the right-side zona incerta (ZI) (posterior 4.0 mm, lateral 2.5 mm, and depth 6.7-7.2 mm). A ground electrode was implanted 2 mm caudal to the lambda. Dental cement was applied to fasten the connection socket to the surface of the skull. Following suturing to complete the surgery, animals were given antibiotics and housed individually in cages for recovery.

Two weeks after the surgery, each animal was placed in the recording environment at least two times (1 hour/day) prior to testing to allow rats to habituate to the experimental apparatus. In this procedure, about 90% of Long-Evans rats showed spontaneous SWD, which were used for continuous EEG recording. Continuous EEG recording from 5 hours to 24 hours (contained one circadian cycle) were recorded and analyzed to assess our seizure detector in this thesis.

2.3 Continuous EEG Recording

In order to validate the robust of seizure detection algorithm, EEG recording must be continuous and uninterrupted for monitoring and analyzing. Fig. 2.1 shows an example of EEG recording corresponding to various behavioral states, including wakefulness (WK), spike-wave discharge (SWD), slow-wave sleep (SWS), and movement artifact in continuous recording of Long-Evans rats.

In this thesis, two essential processing phases of EEG data were performed in Long-Evans, including a training phase and a testing phase. In the training phase, continuous EEG data of each rat were recorded for feature extraction without enabling electrical stimulation. Then, marking recorded EEG data corresponds to seizures (SWD) and non-seizures (WK, SWS, and artifact) by specialist. After four states (SWD, WK, SWS, and artifact) of EEG data were used to train the seizure program off-line, the parameters of a seizure detection model were determined. In the testing phase, after applying the especial parameters to each rat, we proceeding to on-line closed-loop seizure detection. The details of training and testing methods describe in Chapter 4.

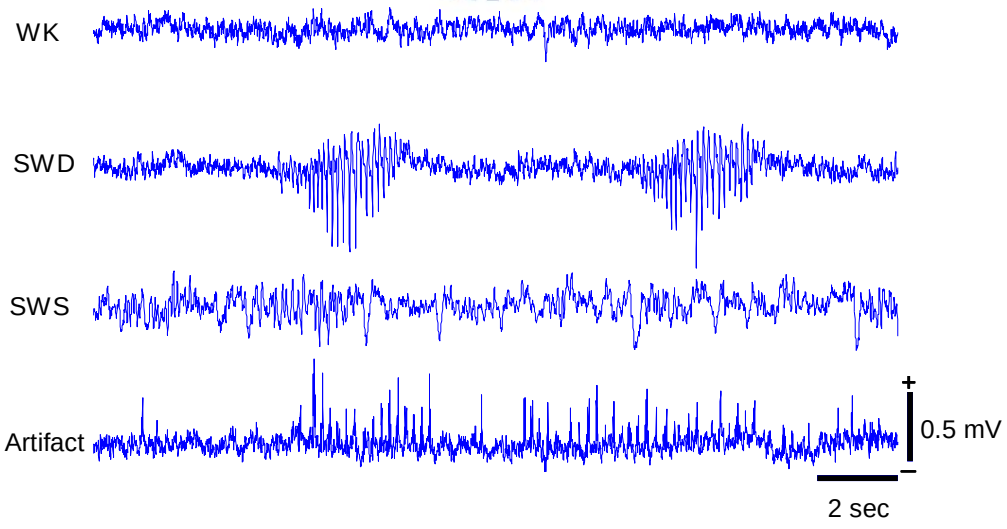


Fig. 2.1 EEG examples during the wakefulness (WK), spike-wave discharge (SWD), slow-wave sleep (SWS), and movement artifact.

Chapter 3 System Architecture

This chapter describes system architecture of closed-loop epileptic seizure control system. The detail of epileptic seizure controller is also introduced. In previous work, a seizure controller has been implemented based on an enhanced 8051 microcontroller. In this thesis, in order to achieve high performance, the seizure controller is implemented by OpenRISC processor.

3.1 Closed-Loop Epileptic Seizure Control System

The closed-loop epileptic seizure control system is composed of three modules: 1) an analog front end (AFE); 2) a biomedical signal processor; and 3) a stimulator. The functional block diagram of the closed-loop epileptic seizure control system is illustrated in Fig. 3.1. The AFE transforms EEG signals into digitized EEG signals. The BSP processes digitized EEG signals. When the BSP detects seizures, it generates enable signals to stimulator. Then, the stimulator generates electric current to suppress seizures.

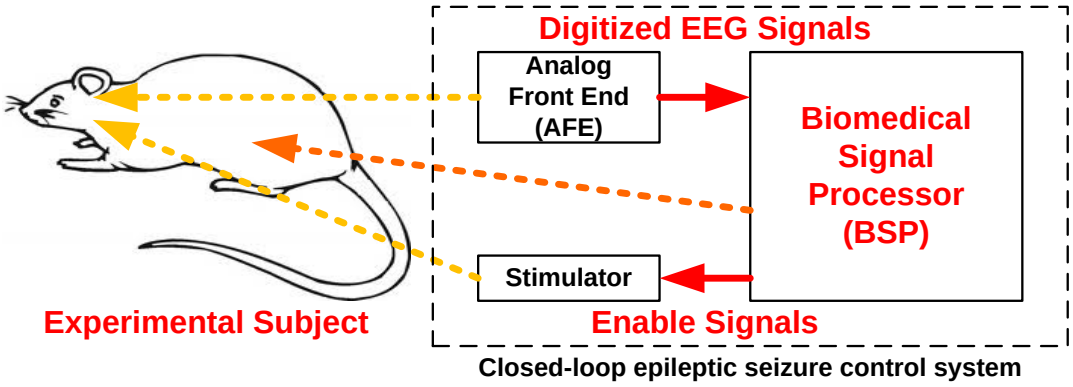


Fig. 3.1 Closed-loop epileptic seizure control system

In this thesis, the seizure detection scheme is based on a large proportion of digital signal processing. Much technology have the high capability of processing digital signals, such as field-programmable gate array (FPGA), DSP, application-specific integrated circuit (ASIC), and RISC processor. Modern high-density FPGA can incorporate embedded processor with custom hardware accelerator to attain high performance; nonetheless, it consumes high static power (tens of milliwatts to hundreds of milliwatts) because of its advanced fabrication technology. ASIC is an integrated circuit, which is highly specialized for particular scenarios or applications. This solution is highly optimized in terms of area, power, and speed to perform its designated task, but it is lack of flexibility. DSP also has high processing capability, but it consumes power consumption highly because of other dedicated hardware accelerators which are not required in our algorithm. Hence, a general purpose processor is chosen in this research.

3.2 General Purpose Processor

3.2.1 Enhanced 8051 Microcontroller

In our previous work [20-23], a seizure controller has been implemented based on an enhanced 8051 microcontroller in freely moving rats. The seizure controller was comprised of a signal conditioning circuit, a microcontroller, and a stimulator. As shown in Fig. 3.2, a closed-loop seizure controller was carried by an experimental subject, and a host computer monitored spontaneous brain activities, which were communicated based on a wireless ZigBee protocol. The EEG signals were amplified and band-pass filtered by the signal conditioning block. Based on a single-channel, 200-Hz sampling rate, and 10-bit ADC resolution, the microcontroller and the signal conditioning circuit consumed 117.66 mW. The power consumption of biomedical implementation is significant for implantable devices.

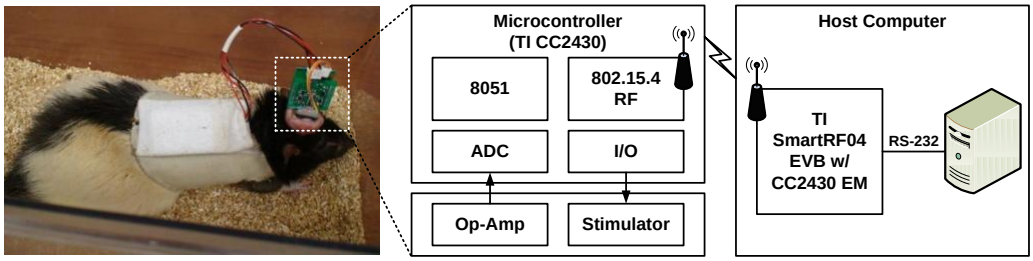


Fig. 3.2 Closed-loop epileptic seizure control system based on enhanced 8051 microcontroller.

3.2.2 OpenRISC Processor

Modern 32-bit RISC processors deliver better energy efficiency than traditional 8-bit microcontrollers. Therefore, a powerful 32-bit processor which is OpenRISC 1200 (OR1200) [29] is modified and implemented for real-time and low-power epileptic seizure detection. In addition, it provides over one dhrystone 2.1 MIPS (DMIPS) per MHz and one DSP MAC 32×32 operations per MHz, and the speed of OpenRISC 1200 is up to 10 times faster than an enhanced 8051 microprocessor's (about 0.1 DMIPS/MHz [30], [31]). In biomedical application, energy efficiency is an important characteristic of biomedical implant, so how low power and energy is the central concern in this work. Our experimental results show the energy per seizure event determination is about 1.15 mJ for OpenRISC and 18.8 mJ for enhanced 8051 microprocessor. The details of evaluation results are described in Chapter 6. The characteristic of OpenRISC is energy efficiency and flexibility; as a result, it can be applied to not only epileptic seizure detection but also other biomedical applications.

Chapter 4 Epileptic Seizure Detection Algorithm

This chapter describes the overall procedure and the seizure detection algorithm [32, 33] in our closed-loop epileptic seizure control system. Briefly speaking, two essential stages of EEG signal processing are performed in Long-Evans rats in this thesis as illustrated in Fig. 4.1. The overall procedure consists of the off-line training phase and the on-line testing phase.

In training phase, continuous EEG signals of each rat are recorded for marking and training. After recorded, EEG signals which correspond to seizures (SWD) and non-seizures (WK, SWS, and artifact) are marked by specialist. The marked events as mentioned above are used to extract complexity measurement (CM) and fast Fourier transform (FFT) values, train linear least square (LLS) classifier and search the finest thresholds (T1 for WK, T2 for SWS, TL_{SWS}, and TH_{SWS}) in our closed-loop seizure control system.

In testing phase, while the parameters of a seizure detection model, which include 4-coefficient of LLS classifier and 4-threshold of seizure determination, are determined, the parameters are downloaded to our processor. Finally, on-line seizure detection testing is performed in OpenRISC.

The following are the details of feature extraction and classifier. Moreover, the details of proposed training flow and testing flow are also described in 4.3.

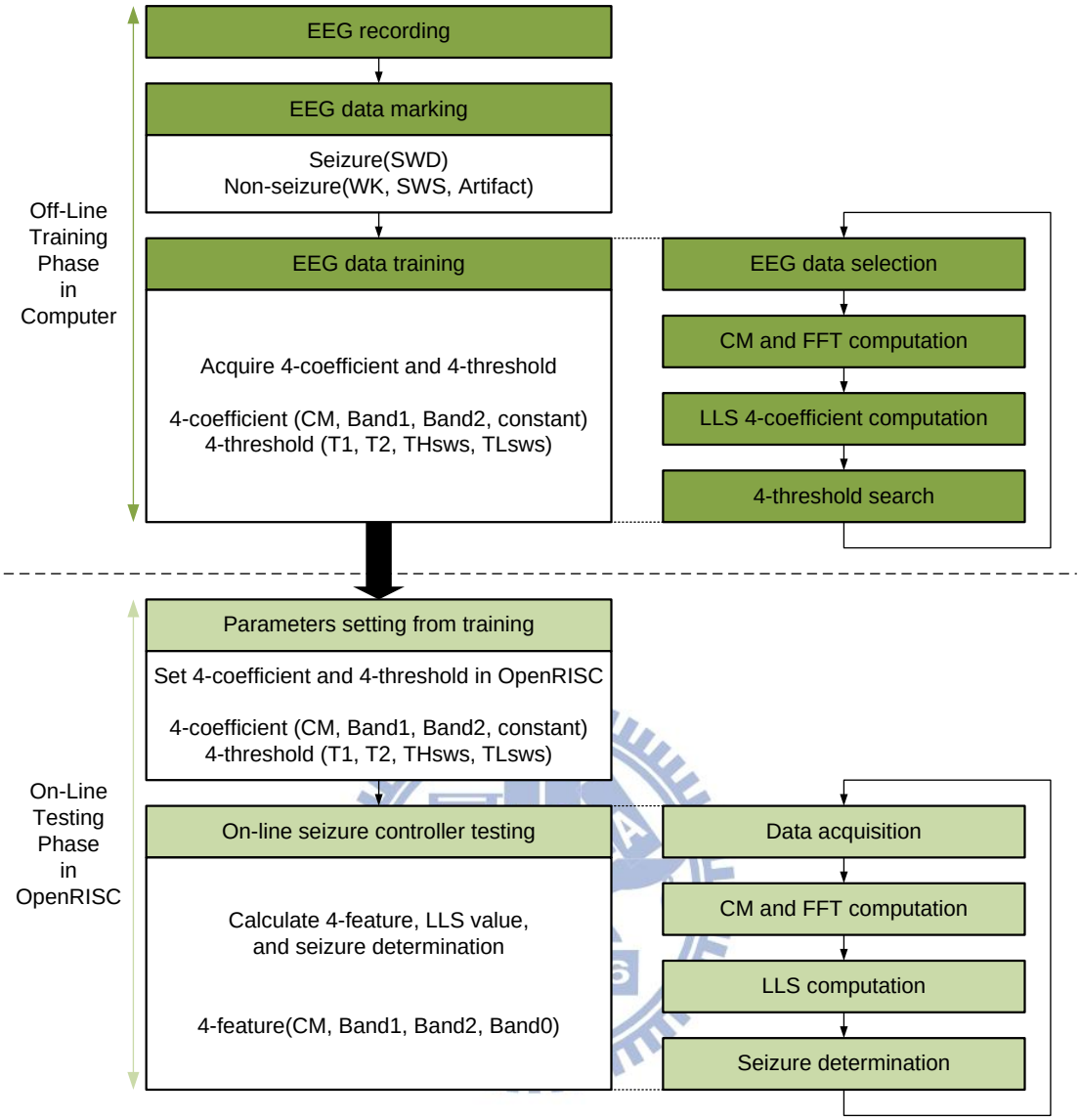


Fig. 4.1 Overall procedure in closed-loop seizure detection system.

4.1 Feature Extraction

Fig. 4.2 shows that 64 points of EEG data are packed with 32 points overlap from previous 64 points of EEG data. In this thesis, combining chaotic and frequency domain analysis can attain high detection accuracy and low computational cost. Complexity analysis such as entropy can distinguish between WK and SWD [34]. The frequency bands of power changes correlate closely with SWD. Spectral analysis can perform as the complementary features of entropy to reduce false detection during SWS or movement artifact.

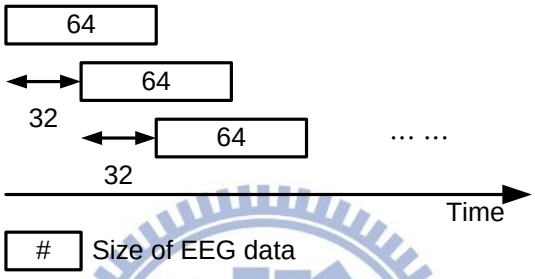


Fig. 4.2 Window size and window shift are applied to feature extraction.

4.1.1 Complexity Analysis

The EEG signals of a seizure are more ordered than those in normal state; as a result, entropy has been used to analyze and detect the seizure. In order to reduce computational cost, simplified entropy which is approximate entropy (ApEn) has been proposed for real-time processing [34]. The value of the ApEn is determined as shown in the following.

1) Give an *N*-point time-series of data, which is formed the same space in time. *X* is represented to be

$$X = \left[x(1), x(2), \ldots, x(N) \right] \quad (1)$$

2) Let $\boldsymbol{x}(i)$ be a subsequence of *X*; that is,

$$\boldsymbol{x}(i) = \left[x(i), x(i+1), \ldots, x(i+m-1) \right], \text{for } 1 \le i \le N-m+1 \quad (2)$$

where *m* is the number of samples used for the comparison.

3) Define $d[\boldsymbol{x}(i), \boldsymbol{x}(j)]$, which is the maximum difference of the relative elements in vectors $\boldsymbol{x}(i)$ and $\boldsymbol{x}(j)$ as follows:

$$d\left[\boldsymbol{x}(i), \boldsymbol{x}(j)\right] = \max\left[\left|x(i+k) - x(j+k)\right|\right], \text{for } k = 0,1,\ldots,(m-1) \quad (3)$$

4) $C_i^m(r)$ and $C_i^{m+1}(r)$ is calculated below:

$$C_i^m(r) = \frac{\sum_{i=1}^{N-m+1} \omega_j}{N-m+1} \quad (4)$$

and

$$C_i^{m+1}(r) = \frac{\sum_{i=1}^{N-m+1} \omega_j}{N-m+1} \quad (5)$$

where

$$\omega_j = \begin{cases} 1, \text{if } d\left[\boldsymbol{x}(i), \boldsymbol{x}(j)\right] \le r \\ 0, \quad \text{else} \end{cases} \quad (6)$$

5) We define $\Phi^m(r)$ and $\Phi^{m+1}(r)$ as follows:

$$\Phi^m(r) = \frac{\sum_{i=1}^{N-m+1} \ln\left(C_i^m(r)\right)}{N-m+1} \quad (7)$$

and

$$\Phi^{m+1}(r) = \frac{\sum_{i=1}^{N-m+1} \ln\left(C_i^{m+1}(r)\right)}{N-m+1} \quad (8)$$

6) ApEn(m, r, N) is calculated in the following way:

$$\mathrm{ApEn}(m, r, N) = \Phi^m(r) - \Phi^{m+1}(r) \quad (9)$$

$$= \frac{\sum_{i=1}^{N-m+1} \ln\left(C_i^m(r)\right)}{N-m+1} - \frac{\sum_{i=1}^{N-m+1} \ln\left(C_i^{m+1}(r)\right)}{N-m+1} \quad (10)$$

$$= \frac{1}{N-m+1}\left[\sum_{i=1}^{N-m+1} \ln\left(C_i^m(r)\right) - \sum_{i=1}^{N-m+1} \ln\left(C_i^{m+1}(r)\right)\right] \quad (11)$$

$$= \frac{1}{N-m+1}\left[\sum_{i=1}^{N-m+1} \ln\left(\frac{C_i^m(r)}{C_i^{m+1}(r)}\right)\right] \quad (12)$$

In order to reduce computational complexity, we modify Eq. (12) by eliminating logarithmic calculation. As a result, we define complexity measurement (CM) as follows:

$$\mathrm{CM}^m = \frac{S^{m+1}}{S^m} \quad (13)$$

where

$$S^m = \frac{\sum_{i=1}^{N-m+1} C_i^m(r)}{N-m+1} \quad (14)$$

and

$$S^{m+1} = \frac{\sum_{i=1}^{N-m+1} C_i^{m+1}(r)}{N-m+1} \quad (15)$$

In this thesis, the setting of parameters is m=1, N=16, and r which differs from one another. The calculation of CM in this work is schematically represented below. First, the 64-point of EEG data is divided into 4-vector for computing CM as shown in Fig. 4.3. Second, to take an example from $X(1)$, we calculate ω_j of each square in Fig. 4.4 and Fig. 4.5. Third, each ω_j is summed up in the S^1 in Fig. 4.4, and S^2 is calculate in the same way in Fig. 4.5. Fourth, using Eq. (13) compute the sub-CM of each vector. Finally, we sum up sub-CM into CM, and the results are depicted in four states as shown in Fig. 4.6. As a result, it is observed that CM can quantify the regularity or complexity of a time series of signals. Because periodic signal components of seizures reduce complexity levels, CM is utilized to analyze the complexity of EEG signals. However, SWS and artifact also show rhythmic patterns, so discrimination ability of CM is reduced. Therefore, to improve the performance of epileptic

seizure detection, it is required to combine complementary features to CM analysis. Spectral analysis is recruited for this purpose.

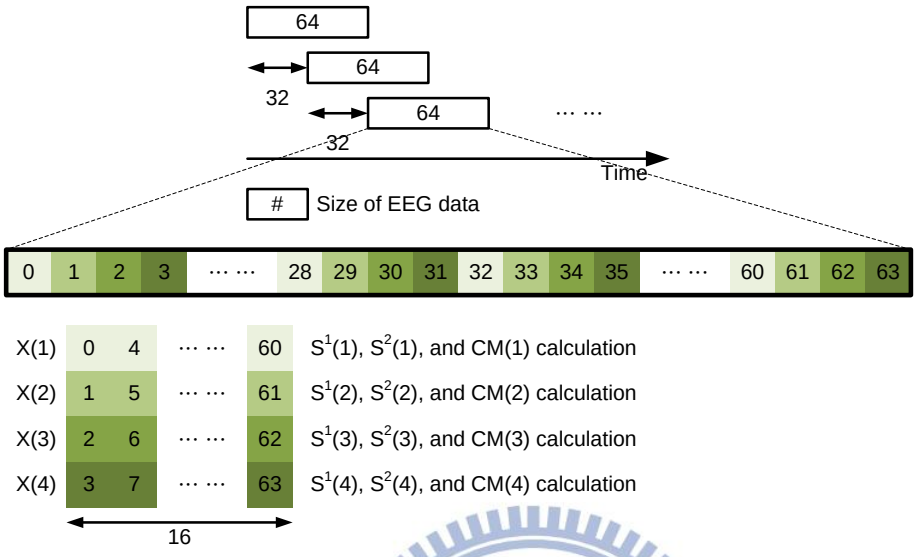


Fig. 4.3 Data size of EEG signals for CM calculation.

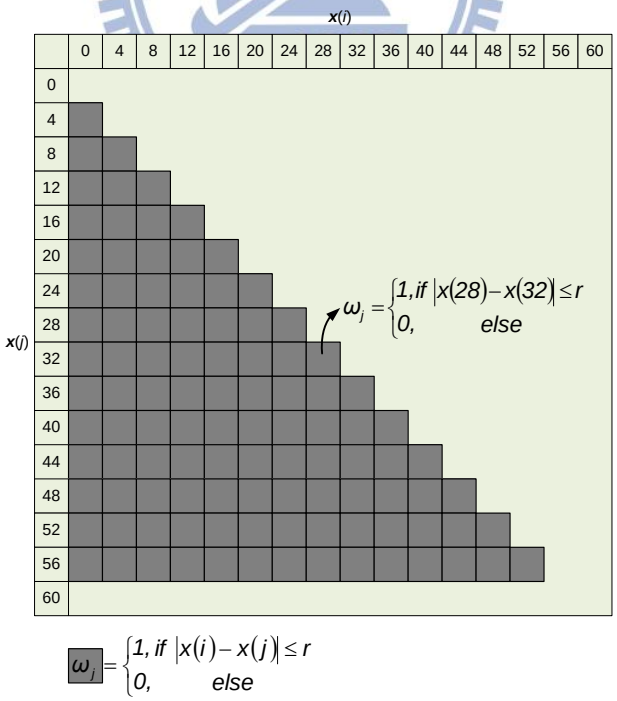


Fig. 4.4 Computation of the S^1 value.

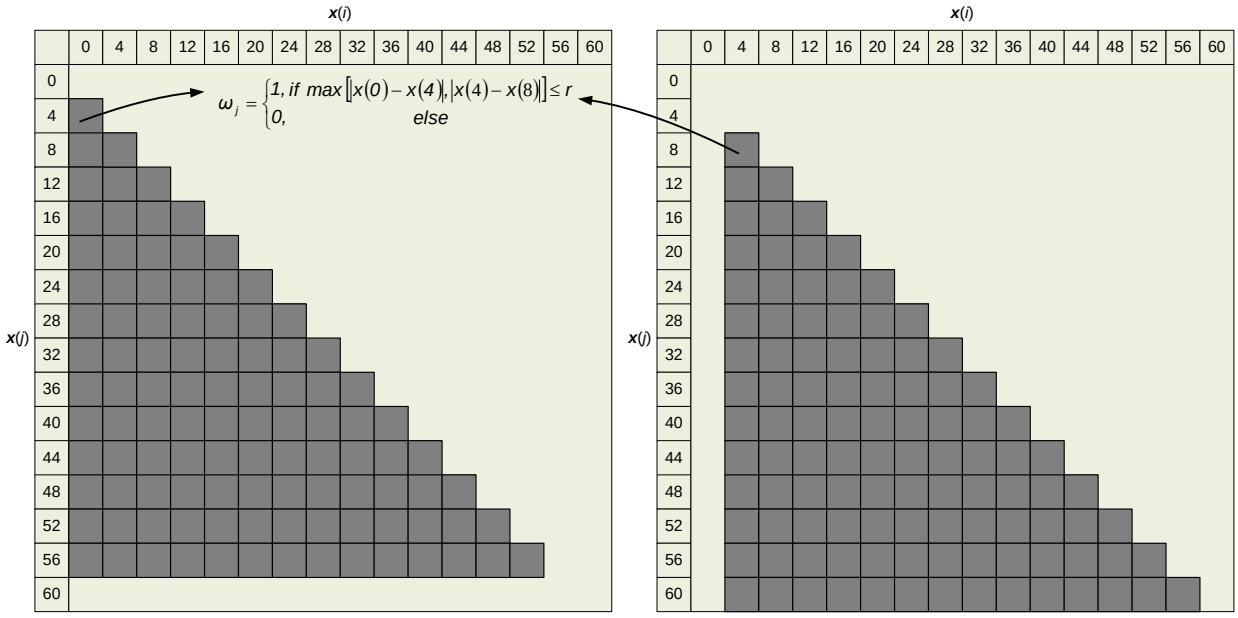


Fig. 4.5 Computation of the S^2 value.

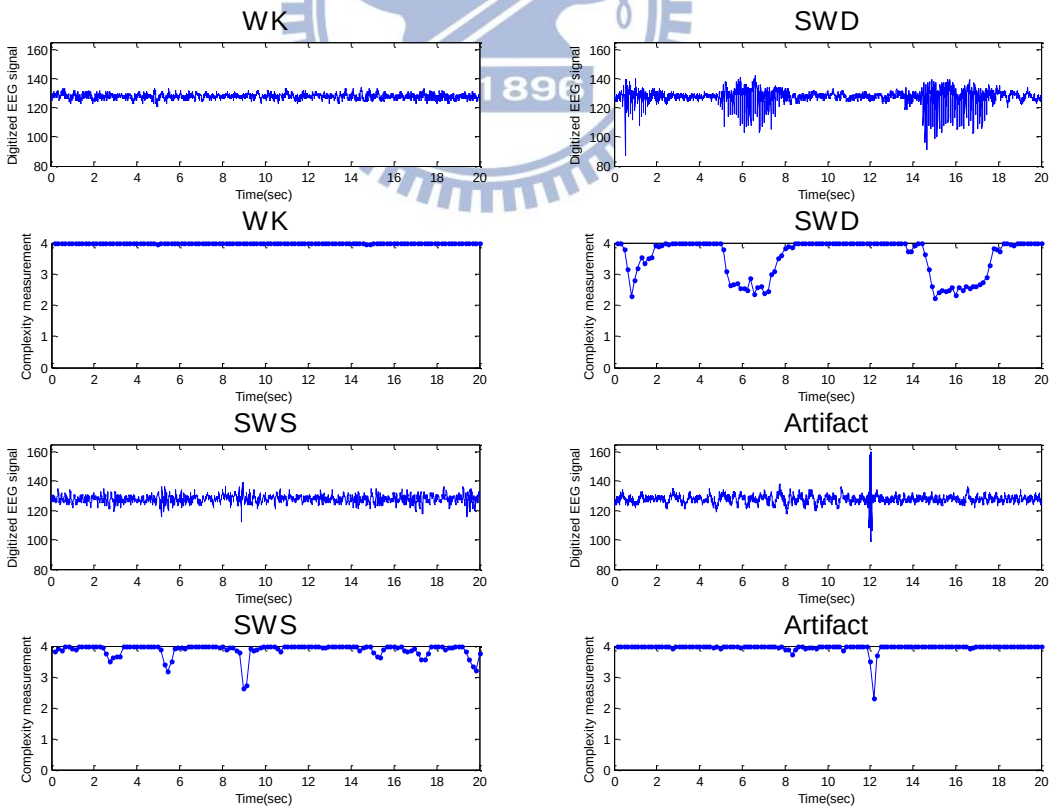


Fig. 4.6 Complexity measurement in four behavioral states.

4.1.2 Spectral Analysis

In this thesis, short-term Fourier transform is used to analyze spectral power distribution. It is observed that enormous power of the absence seizure is at the fundamental frequency (Band1 at 7-9 Hz) and at the second harmonic (Band2 at 14-18 Hz) as seen in Fig. 4.7. SWS state contains delta rhythms (Band0) as well as some oscillations at higher frequencies. Artifact state has high power at low and some high frequency bands. Therefore, EEG band powers are combined with CM to improve the performance of epileptic seizure detection.

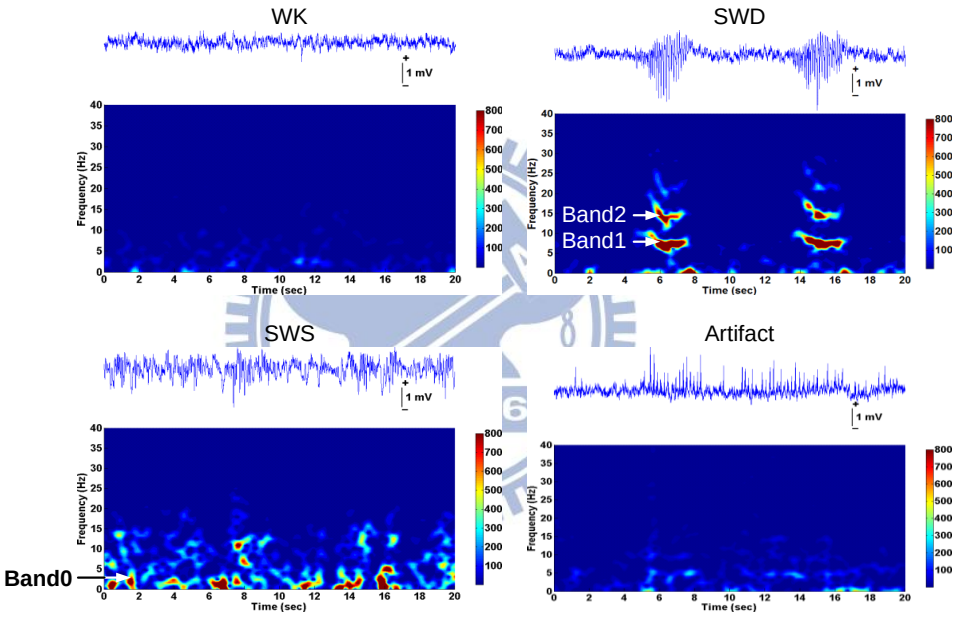


Fig. 4.7 Spectral analysis in four behavioral states.

The 64-point fast Fourier transform (FFT) is used to calculate the power of two frequency bands (Band1 and Band2) of spontaneous brain waves because of its well-established implementation in various microprocessors. Fig. 4.7 displays the highest correlations between the power of two frequency bands (Band1 and Band2) and SWDs; therefore, Band1 and Band2 are selected as spectral indexes. To determine spectral indexes to extract an SWD feature adequately, a seizure event (denominated as “1”) is correlated with

the power of several specific frequency bands by using Pearson's product-moment correlation coefficient. Fig. 4.8 shows that using correlation analysis between seizure event and a specific frequency band identifies effective spectral indexes for seizure detection.

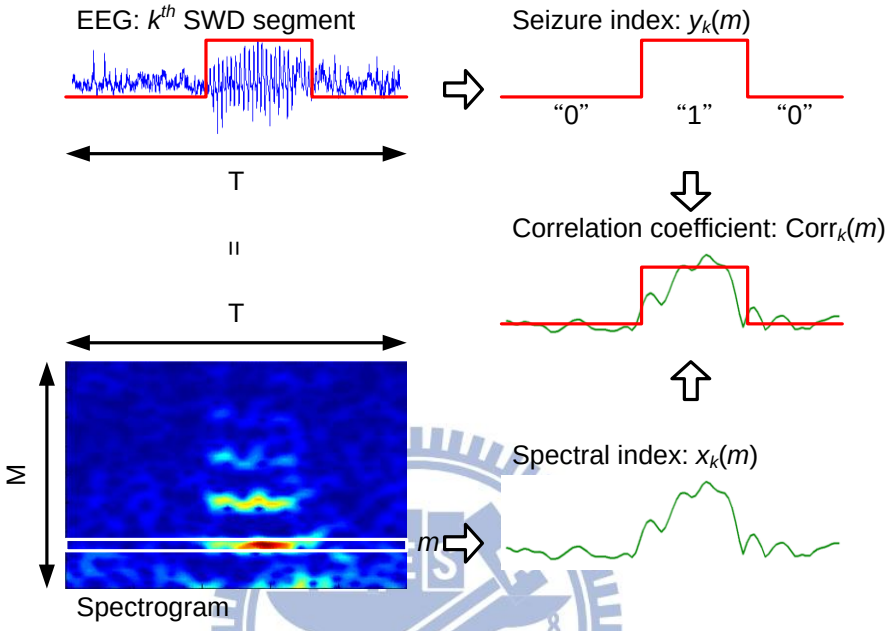


Fig. 4.8 Using correlations analysis identifies spectral indexes (Band1 and Band2).

The flowchart of the correlation analysis is shown in Fig. 4.8. Consider there are k SWD segments. SP(t,f) is the spectrogram at time t in frequency f.

1) Define the spectral indexes X_k to be

$$X_k = \begin{bmatrix} \vdots \\ x_k(m) \\ \vdots \end{bmatrix} \quad (16)$$

where

$$x_k(m) = \left[\mathrm{SP}_k(1,m), \mathrm{SP}_k(2,m), \ldots, \mathrm{SP}_k(\mathrm{T},m)\right] \quad (17)$$

$x_k(m)$ is the spectral index which is the spectrogram in frequency m.

2) Define the seizure index

$$y_k = \left[\phi_k(1), \phi_k(2), \ldots, \phi_k(\mathrm{T})\right] \quad (18)$$

where

$$\phi_k(t) = \begin{cases} 1, \text{ if the state is SWD in time } t \\ 0, \qquad \text{else} \end{cases} \quad (19)$$

3) The correlation coefficient $\mathrm{Corr}_k(m)$ of the seizure index y_k and the spectral index x_k is

$$Corr_k(m) = \frac{\sum\left(x_k(m) - \overline{x_k(m)}\right)\left(y_k - \overline{y_k}\right)}{\sqrt{\sum\left(x_k(m) - \overline{x_k(m)}\right)^2 \sum\left(y_k - \overline{y_k}\right)^2}} \quad (20)$$

4) The averaged correlation coefficient of k segments is

$$C(m) = \frac{\sum_K Corr_k(m)}{k} \quad (21)$$

Fig. 4.9 shows an example of correlations between the spectral index and the seizure index. The selected frequency bands are Band1=8-11 Hz and Band2=17-20 Hz for subject #1. In this project, the sampling frequency F_s is 200 Hz, and the sampled data are N points. The spectral index n of bands is calculated by the following equation, where F_n is spectral frequency. As a result, the spectral index of selected frequency bands is n=4 for Band1 and n=7 for Band2 for subject #1.

$$F_n = \frac{F_s \times (n-1)}{N} \quad (22)$$

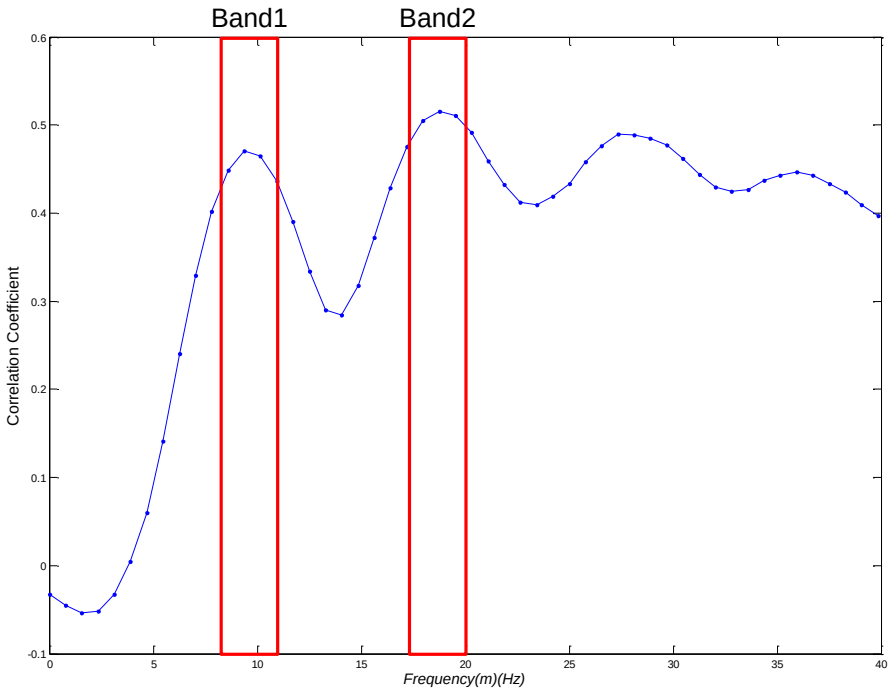


Fig. 4.9 Result of correlation analysis.

After determining the selected frequency bands, we use 64-point radix-4 FFT to calculate the power of Band1 and Band2 of 64-point EEG signals as shown in Fig. 4.10.

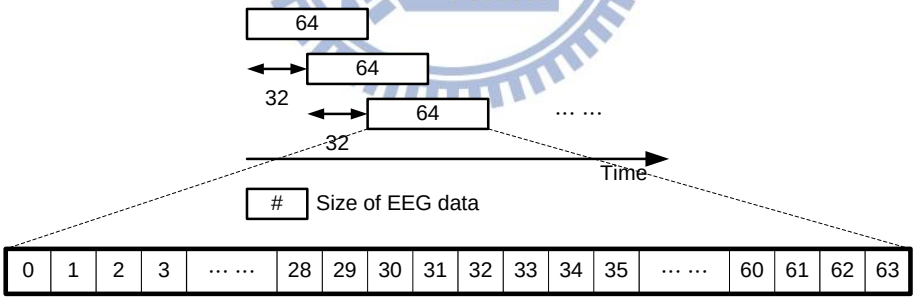


Fig. 4.10 Data size of EEG signals for FFT calculation.

Basically, discrete Fourier transform (DFT) is to compute the sequence $X(k)$ of N complex-valued numbers given another sequence of data $x(n)$ of length N.

$$X(k)=\sum_{n=0}^{N-1}x(n)W_N^{kn} \quad (23)$$

where

$$W_N^{kn}=e^{\frac{-j2\pi kn}{N}},\ \text{for } 0\le k\le N-1 \quad (24)$$

The radix-4 decimation-in-time algorithm rearranges the DFT equation into four parts as follows.

$$X(k) \quad (25)$$

$$=\sum_{n=0}^{N/4-1}x(n)W_N^{kn}+\sum_{n=N/4}^{N/2-1}x(n)W_N^{kn}+\sum_{n=N/2}^{3N/4-1}x(n)W_N^{kn}+\sum_{n=3N/4}^{N-1}x(n)W_N^{kn} \quad (26)$$

$$=\sum_{n=0}^{N/4-1}x(n)W_N^{kn}+W_N^{Nk/4}\sum_{n=0}^{N/4-1}x\left(n+\frac{N}{4}\right)W_N^{kn}+W_N^{Nk/2}\sum_{n=0}^{N/4-1}x\left(n+\frac{N}{2}\right)W_N^{kn} \quad (27)$$
$$+W_N^{3Nk/4}\sum_{n=0}^{N/4-1}x\left(n+\frac{3N}{4}\right)W_N^{kn}$$

$$=\sum_{n=0}^{N/4-1}\left[x(n)+(-j)^k x\left(n+\frac{N}{4}\right)+(-1)^k x\left(n+\frac{N}{2}\right)+(j)^k x\left(n+\frac{3N}{4}\right)\right]W_N^{nk} \quad (28)$$

Using k_1+4k_2 to substitute k, we rearrange Eq. (28) into Eq. (29). In this algorithm, there are three stages involving 64-point uniform radix-4 algorithmic processes. The data flow of 64-point radix-4 FFT is shown in Fig. 4.11.

$$X(k_1+4k_2)=\sum_{n=0}^{N/4-1}\left\{\left[x(n)+(-j)^{k_1}x\left(n+\frac{N}{4}\right)+(-1)^{k_1}x\left(n+\frac{N}{2}\right)+(j)^{k_1}x\left(n+\frac{3N}{4}\right)\right]W_N^{nk_1}\right\}W_{N/4}^{nk_2} \quad (29)$$

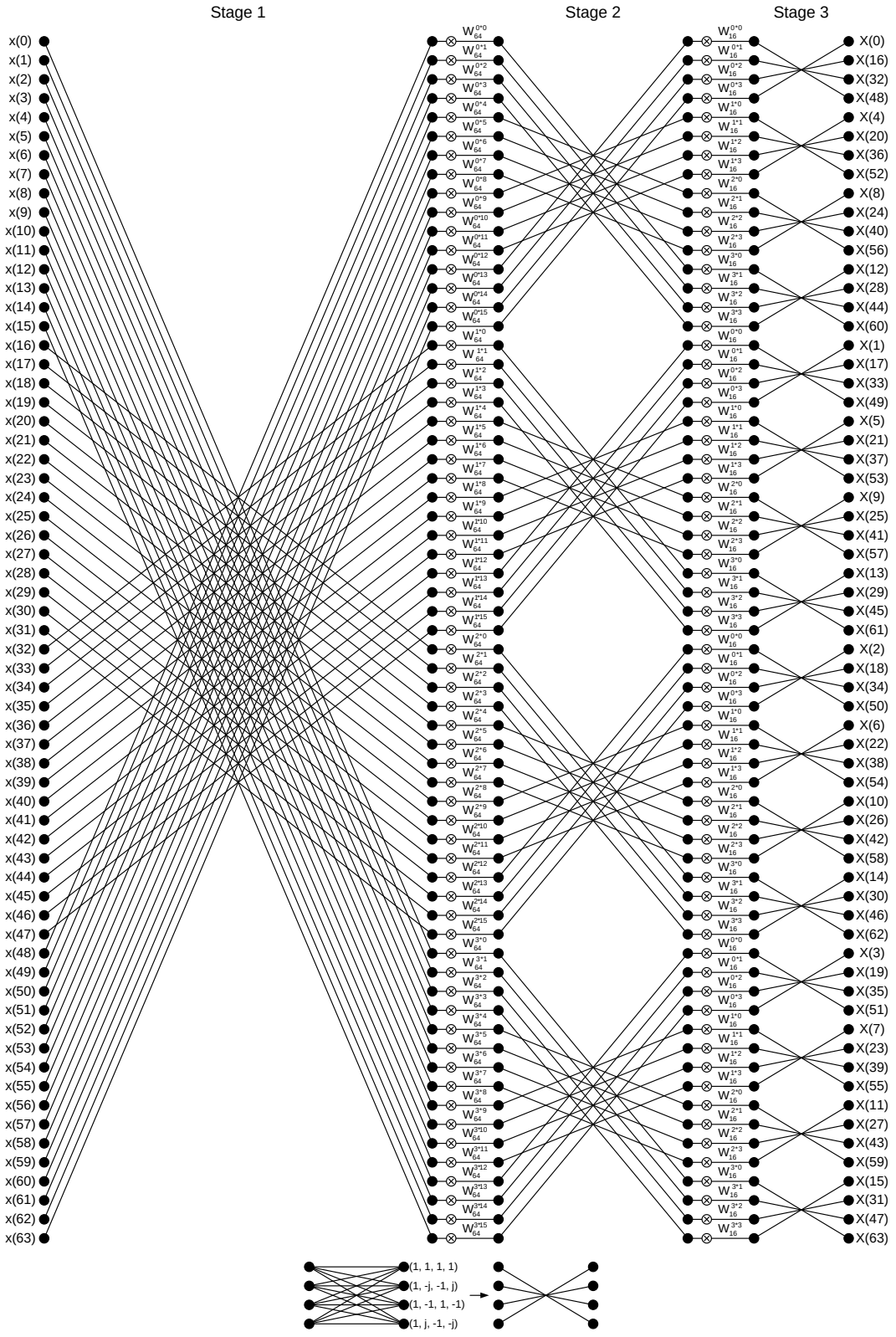


Fig. 4.11 64-point radix-4 FFT decimation-in-time algorithm.

4.2 Classifier

Three feature indexes (CM and power of Band1 and Band2) are input into a classifier to verify seizure occurrences. In order to implement the proposed seizure detection method on an embedded system, a linear classifier called linear least squares (LLS) [35] is utilized. In mathematics, a system of linear equations is considered over-determined if there are more equations than unknowns. The method of least squares is a standard approach to the approximate solution of over determined systems. The LLS method finds the most approximate linear model which is minimized the mean square error between the system output and the desired output. Because the model's output is only the weighted sum of three input features, it is suitable for processing on-line system without complicated computation.

Consider an over-determined system

$$y_i = \sum_{j=1}^{n} X_{ij}\beta_j, \text{for } i = 1, 2, \ldots, m \quad (30)$$

of m linear equations in n unknown coefficients, β_1, β_2, …, β_n with $m>n$. It can be written in matrix form as

$$y = X\beta \quad (31)$$

where

$$y = \begin{bmatrix} y_1 \\ \vdots \\ y_n \end{bmatrix}, X = \begin{bmatrix} x_{11} & \cdots & x_{1n} \\ \vdots & \ddots & \vdots \\ x_{m1} & \cdots & x_{mn} \end{bmatrix}, \beta = \begin{bmatrix} \beta_1 \\ \vdots \\ \beta_n \end{bmatrix} \quad (32)$$

In this thesis, we let the output of LLS be y, the input of LLS be X, and the weighted coefficient of input be β. Such a system usually has no solution, so the goal is instead to find the coefficients β which fit the equations best. The coefficients β can be find by following equations.

The residual r is the difference between the observed value y and the calculated value $X\beta$ by the model:

$$r_i = y_i - \sum_{j=1}^{n} X_{ij}\beta_j, \text{ for } i = 1, 2, \ldots, m \quad (33)$$

Then the sum of square of the residuals S can be written

$$S = \sum_{i=1}^{m} r_i^2 \quad (34)$$

S is minimized when its gradient vector is zero. The elements of the gradient vector are the partial derivatives of S with respect to the parametersβ

$$\frac{\partial S}{\partial \beta_j} = 2\sum_{i=1}^{m} r_i \left(\frac{\partial r_i}{\partial \beta_j} \right) = 0, \text{ for } j = 1, 2, \ldots, n \quad (35)$$

and the residuals r

$$\frac{\partial r_i}{\partial \beta_j} = -X_{ij} \quad (36)$$

We use Eq. (33) and Eq. (36) in substitution for Eq. (35)

$$\frac{\partial S}{\partial \beta_j} = 2\sum_{i=1}^{m} \left(y_i - \sum_{k=1}^{n} X_{ik}\beta_k \right) \left(-X_{ij} \right) = 0, \text{ for } j = 1, 2, \ldots, n \quad (37)$$

If $\hat{\beta}$ minimizes S, we have

$$\frac{\partial S}{\partial \beta_j} = 2\sum_{i=1}^{m} \left(y_i - \sum_{k=1}^{n} X_{ik}\hat{\beta}_k \right) \left(-X_{ij} \right) = 0, \text{ for } j = 1, 2, \ldots, n \quad (38)$$

Upon rearrangement, the normal equations can be rewritten

$$\sum_{i=1}^{m} \sum_{k=1}^{n} X_{ij} X_{ik} \hat{\beta}_k = \sum_{i=1}^{m} X_{ij} y_j, \text{ for } j = 1, 2, \ldots, n \quad (39)$$

The normal equations are written in matrix notation as

$$\left(X^T X \right) \hat{\beta} = X^T y \quad (40)$$

The optimal coefficients $\hat{\beta}$ can be determined by following equation.

$$\hat{\beta} = \left(X^T X \right)^{-1} X^T y \qquad (41)$$

In training phase, all SWD durations and the non-seizure segments with the length equivalent to the SWDs are selected for the LLS model training. In the non-seizure segments, the ratios of the data corresponding to WK, SWS, and the artifact are 1:1:1. For example, in Fig. 4.12, the ratios of the six data corresponding to SWD, WK, SWS, and the artifact are 3:1:1:1. The inputs X_{ij} of LLS classifier are formed into Eq. (42). The target value y_i is 0 for non-seizure segments, and 1 for seizure segments. The optimal coefficients $\hat{\beta}$ can be determined by Eq. (41) for each rat through an off-line process.

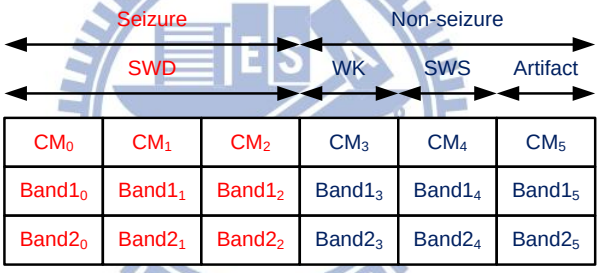


Fig. 4.12 An example of LLS classifier's input *X*.

$$y = \begin{bmatrix} 1 \\ 1 \\ 1 \\ 0 \\ 0 \\ 0 \end{bmatrix}, X = \begin{bmatrix} \mathrm{CM}_0 & \mathrm{Band1}_0 & \mathrm{Band\,2}_0 & 1 \\ \mathrm{CM}_1 & \mathrm{Band1}_1 & \mathrm{Band\,2}_1 & 1 \\ \mathrm{CM}_2 & \mathrm{Band1}_2 & \mathrm{Band\,2}_2 & 1 \\ \mathrm{CM}_3 & \mathrm{Band1}_3 & \mathrm{Band\,2}_3 & 1 \\ \mathrm{CM}_4 & \mathrm{Band1}_4 & \mathrm{Band\,2}_4 & 1 \\ \mathrm{CM}_5 & \mathrm{Band1}_5 & \mathrm{Band\,2}_5 & 1 \end{bmatrix}, \hat{\beta} = \begin{bmatrix} Coeff_{\mathrm{CM}} \\ Coeff_{\mathrm{Band1}} \\ Coeff_{\mathrm{Band\,2}} \\ Coeff_{\mathrm{Const}} \end{bmatrix} \qquad (42)$$

In testing phase, the optimal coefficients $\hat{\beta}$ are applied for Eq. (43), where three features are obtained from testing data. If the output LLS is larger than a threshold (T1 or T2), the input EEG signals is classified as a seizure event.

$$\mathrm{LLS} = \mathrm{CM} \times Coeff_{\mathrm{CM}} + \mathrm{Band1} \times Coeff_{\mathrm{Band1}} + \mathrm{Band\,2} \times Coeff_{\mathrm{Band\,2}} + Coeff_{\mathrm{Const}} \qquad (43)$$

4.3 EEG Data for Training and Testing

4.3.1 Training Phase

The purpose of training is to determine a fitting model which contains four coefficients and four thresholds for each subject. Fig. 4.13 shows the procedure of training phase. Continuous EEG signals of each rat are recorded for marking and training. After recorded, EEG signals which correspond to seizures (SWD) and non-seizures (WK, SWS, and artifact) are marked by specialist. The marked events as mentioned above are used to extract CM, Band1, Band2, and Band0 values. After that, we start to train eight parameters including four coefficients and four thresholds. The following are the details of EEG data training.

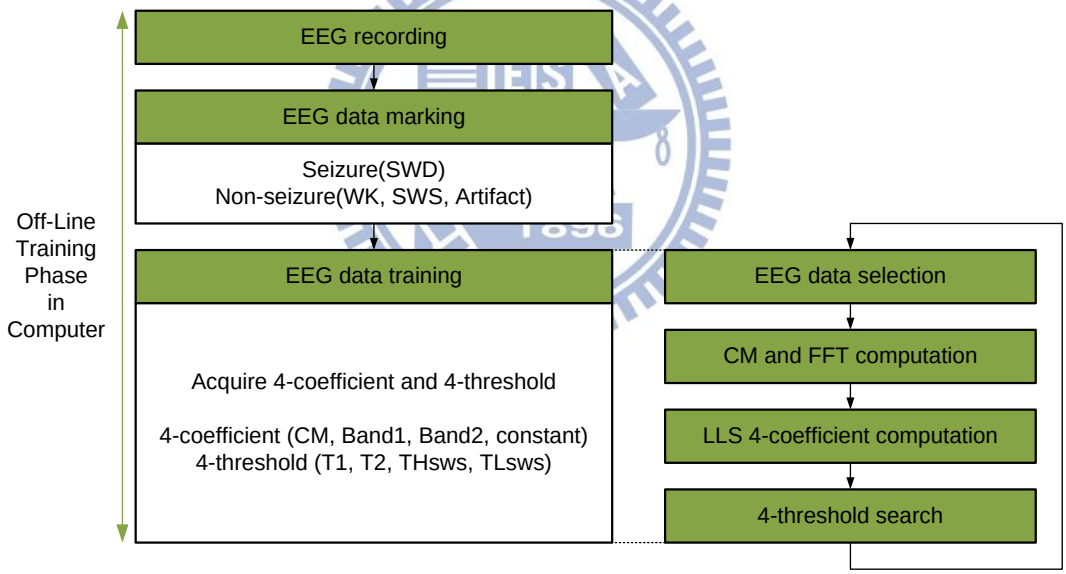


Fig. 4.13 Procedure of training phase.

First, we randomly select the EEG segments of four states, and the ratios of the segments corresponding to SWD, WK, SWS, and the artifact must be 3:1:1:1 as shown in Fig. 4.14. Second, we execute CM and FFT computation to obtain CM, Band1, Band2, and Band0 values. Third, combined feature substitute the X of Eq. (41), and desired output substitutes the y of Eq. (41) like Eq. (42). Then, the optimal coefficients $\hat{\beta}$ can be determined. Fourth,

the optimal coefficients $\hat{\beta}$ are applied for Eq. (43), where three features are obtained from training data. Then, we search the optimal thresholds from LLS and Band0 values in order to recognize a seizure event. The flowchart of seizure determination is shown in Fig. 4.15, and we test many sets of thresholds in detection rate and false detection rate for finding the most optimal thresholds.

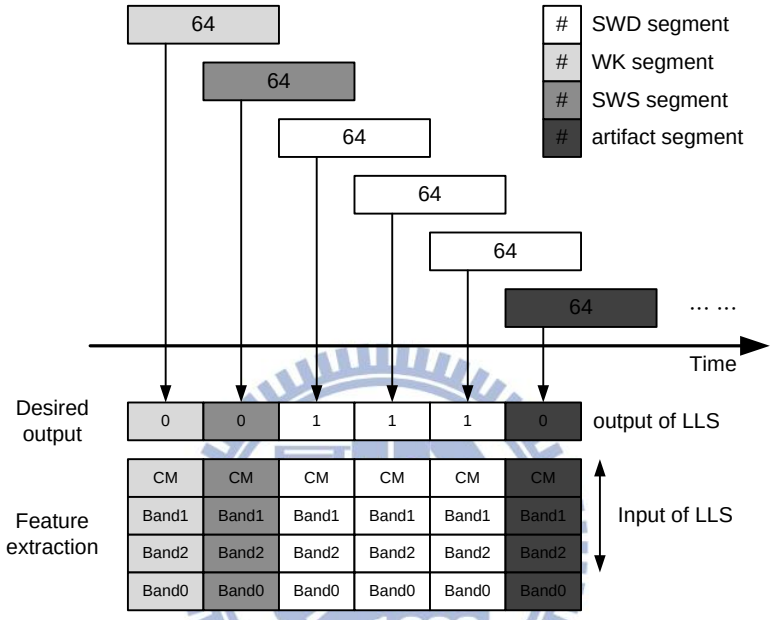


Fig. 4.14 Feature extraction and LLS classifier training.

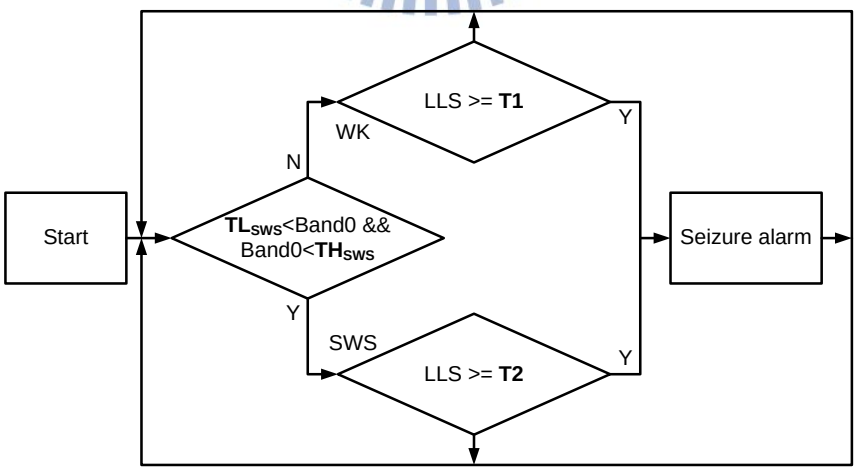


Fig. 4.15 The flowchart of seizure determination.

In previous work, four thresholds are obtained by using exhaustive key search. In Fig. 4.16 (a), we do not calculate the distribution of seizure's and non-seizure's values of LLS and Band0, and we use every set of 4-threshold to test detection rate and false detection. We need $(M\times N)^2$ times of iterations to find the best thresholds. As a result, original method wastes a lot of time on parameter determination. To speed up parameter determination, it is proposed that using the mean and the multiples of standard deviation finds four thresholds rapidly. We calculate the distribution of seizure's and non-seizure's values of LLS and Band0. According to the step as mentioned above, we only need $\left(\frac{M}{m}\times\frac{N}{n}\right)^2$ times of iterations to find the best thresholds.

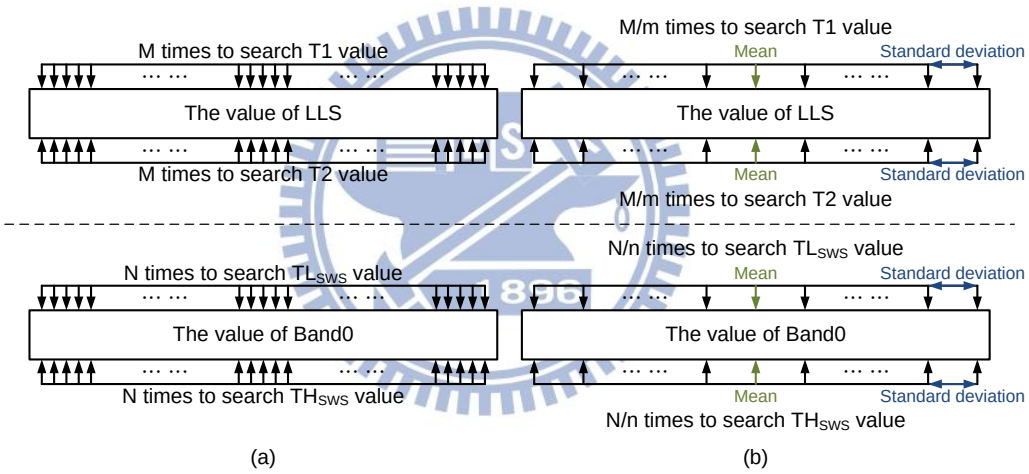


Fig. 4.16 (a) Original search for 4-threshold, (b) Proposed search for 4-threshold.

The following are the steps of the fast parameter determination method. Moreover, the flowchart of fast parameter determination method is depicted in Fig. 4.17.

1) The four coefficients of Eq. (43) is substituted for optimal coefficients $\hat{\beta}$, and we calculate the LLS value of Eq. (43).
2) We compute the mean and the standard deviation of actual non-SWD's LLS value as shown in Fig. 4.18 (a), so T1 can be written

$$\mathrm{T1}=\overline{\mathrm{nonSWD's\ LLS}}+i\times\sigma\left(\mathrm{nonSWD's\ LLS}\right) \qquad (44)$$

where *i* is multiple of standard deviation. We choose a real number to substitute *i* for calculating T1, and the detection rate of our system is determined in this step.

3) We compute the mean and the standard deviation of actual SWD's Band0 value as depicted in Fig. 4.18 (a), so TH_{SWS} can be written

$$TH_{SWS} = \overline{\text{SWD's Band 0}} + j \times \sigma(\text{SWD's Band 0}) \quad (45)$$

where *j* is multiple of standard deviation. We choose a real number to substitute *j* for calculating TH_{SWS}, and the false detection rate is reduced in this step.

4) After executing three steps as mentioned above, we compute the mean and the standard deviation of FP's LLS value and FP's Band0 value as shown in Fig. 4.18 (c). T2 and TL_{SWS} can be written

$$T2 = \overline{\text{FP's LLS}} + k \times \sigma(\text{FP's LLS}) \quad (46)$$

$$TL_{SWS} = \overline{\text{FP's Band 0}} + l \times \sigma(\text{FP's Band 0}) \quad (47)$$

where *k* and *l* are multiple of standard deviation. We choose real numbers separately to substitute *k* and *l* for calculating T2 and TL_{SWS}, and the false detection rate is also reduced in this step.

5) We test the detection rate and the false detection rate for 4-threshold which is determined by Step(2) to Step(4).

6) Changing the real number of *i* and *j*, we iterate form Step (2) to Step (5). In Step (4), we also change the real number of *k* and *l*, we iterate form Step (4) to Step (5). Finally, we can select the best threshold from the test in Step (5).

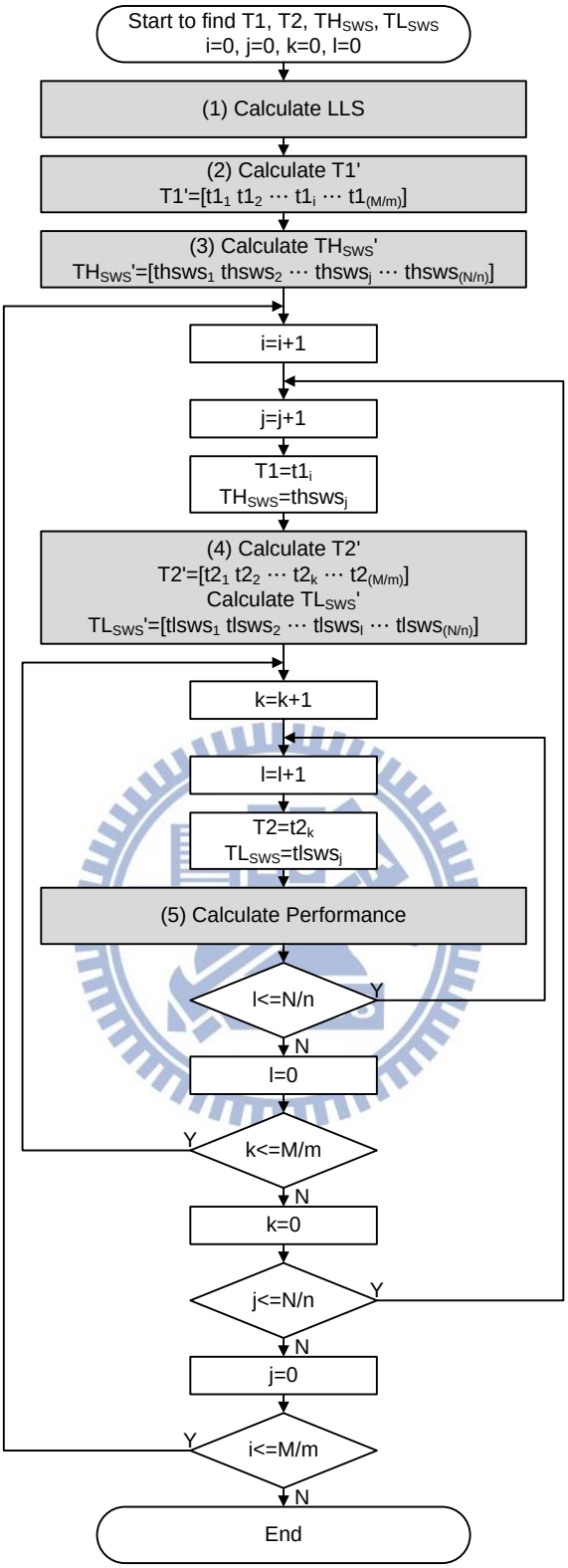


Fig. 4.17 Flowchart of fast parameter determination method.

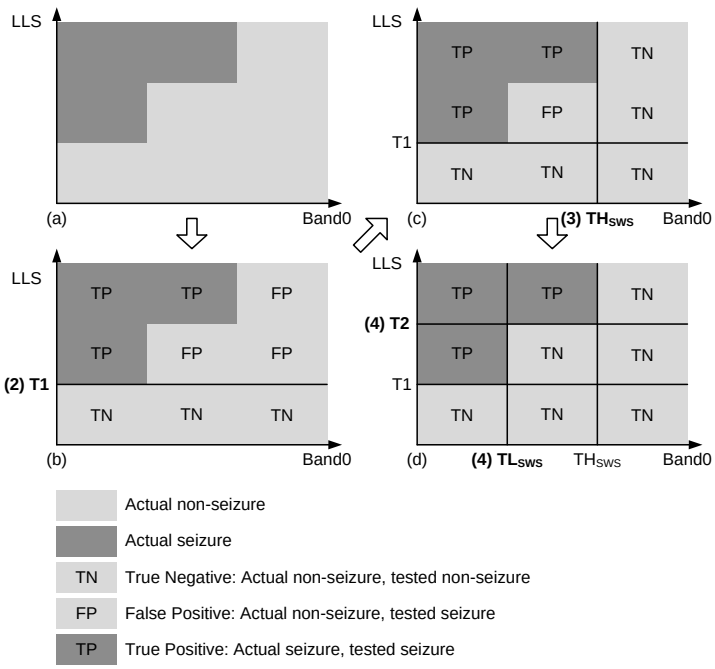


Fig. 4.18 (a) Original data, (b) Determine T1,

(c) Determine TH_{SWS}, (d) Determine T2 and TL_{SWS}.

4.3.2 Testing Phase

Fig. 4.19 shows the procedure of testing phase. In testing phase, after the parameters of a seizure detection model, which include 4-coefficient of LLS classifier and 4-threshold of seizure determination, are determined from training phase, the parameters are downloaded to our processor. The seizure detection algorithm as shown in Fig. 4.20 is executed on OpenRISC. After initializing the system, we start to acquire 32-point EEG data. Then, we compute 64-point data of time domain CM and frequency domain FFT. After the CM, Band1, and Band2 values are obtained, LLS value is calculated by Eq. (43). A seizure alarm is discriminate from normal EEG signals by determining LLS and Band0 values. When the counter reaches "3"; that is, N_C equals 3 in Fig. 4.20, a seizure is determined. In the meantime, an enable signal is generated to stimulator in our system.

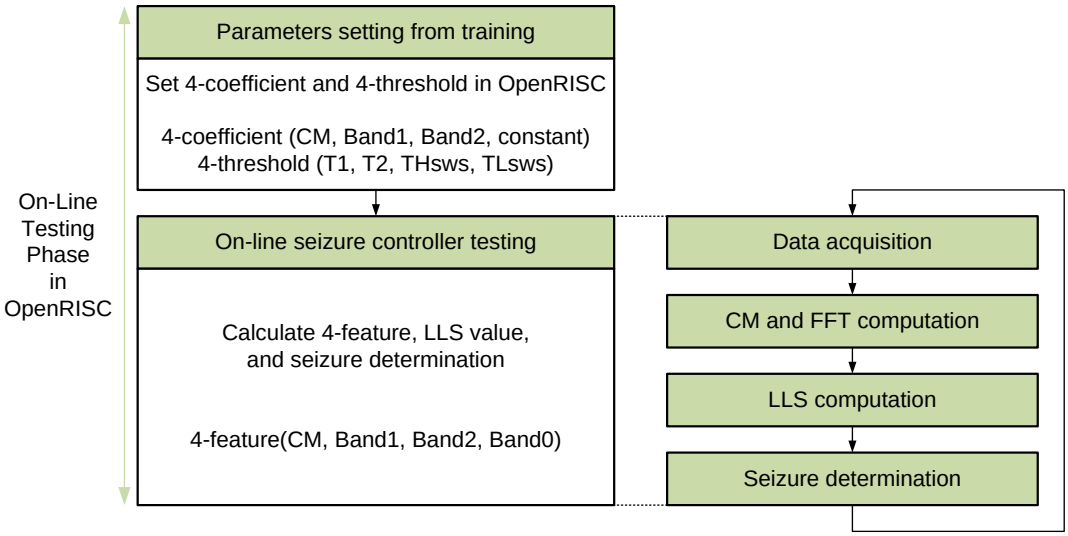


Fig. 4.19 Procedure of testing phase.

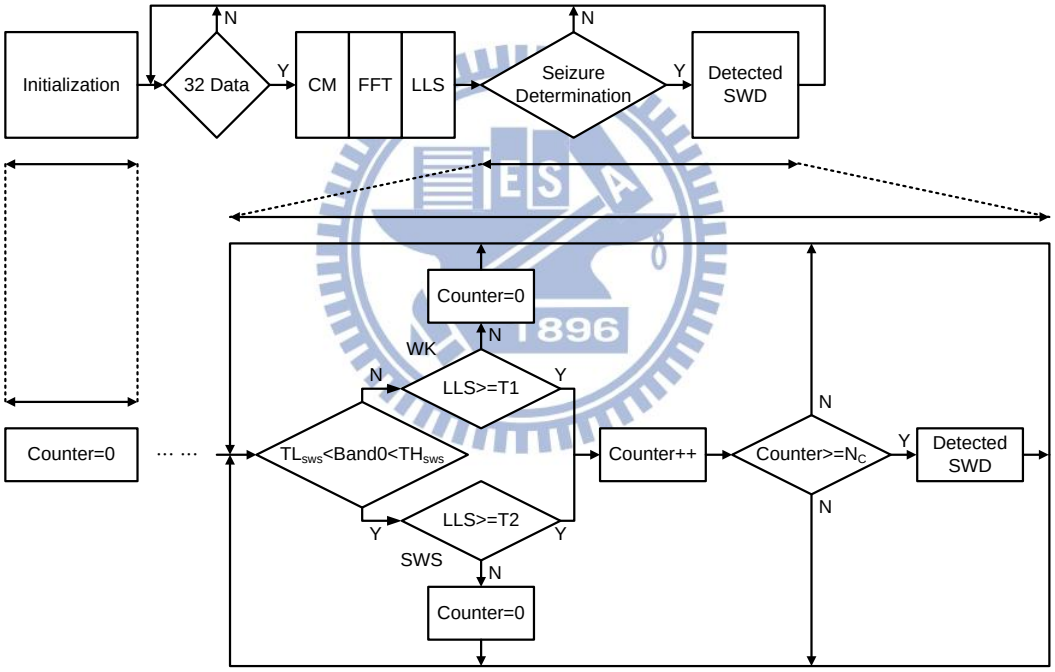


Fig. 4.20 Flowchart of on-line seizure detection algorithm.

Chapter 5 Design and Implementation

This chapter presents the design and implementation of the proposed low-power BSP, including hardware architecture and firmware.

5.1 The Low-Power Biomedical Signal Processor

The low-power BSP implementation bases on the OR1200 for epileptic seizure control. OR1200 is a 32-bit scalar RISC with Harvard micro-architecture, five stage integer pipeline, memory management units (MMU), and basic DSP capabilities. Supplemental facilities include debug unit for real-time debugging, high resolution tick timer, programmable interrupt controller, and power management support. OR1200 is designed for embedded, portable, and networking applications. Fig. 5.1 (a) shows the block diagram of OR1200.

Because the area is proportional to power consumption, the unnecessary interfaces and modules are removed for optimizing power consumption. The external interfaces of the power management, debug module and interrupt controller are removed. Some modules which consist of the memory management units and the caches are also removed. Furthermore, the instruction and data bus are controlled by an arbiter. Instruction and data bus are merged, so the data bandwidth is reduced. Instruction bus has the highest priority to access bus. The purpose of merged buses is a trade-off between power and execution time. Fig. 5.1 (b) shows the block diagram of the proposed low-power BSP for epileptic seizure control.

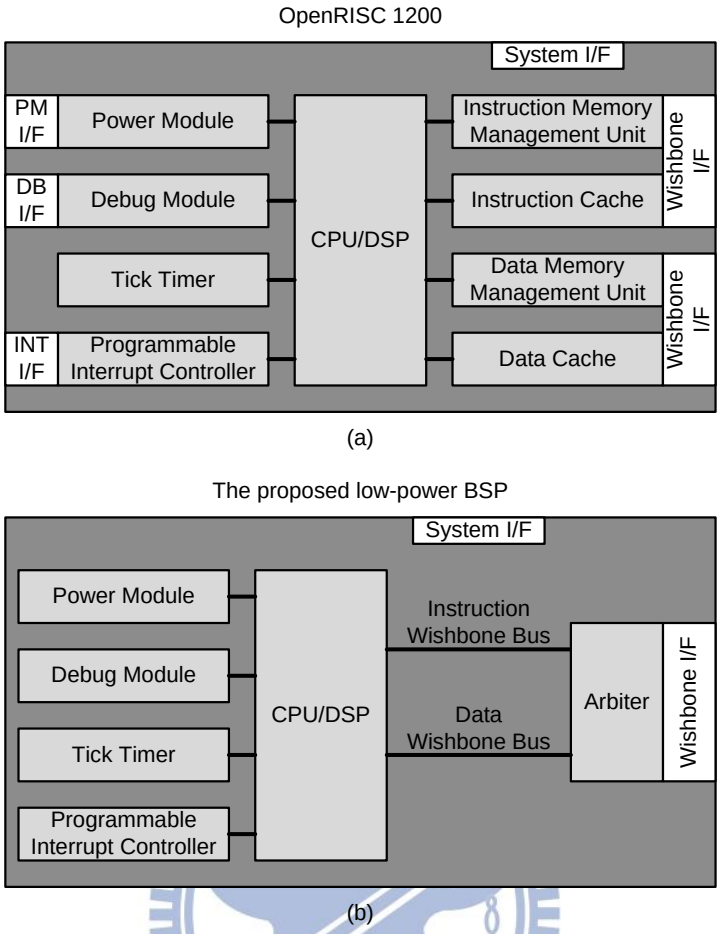
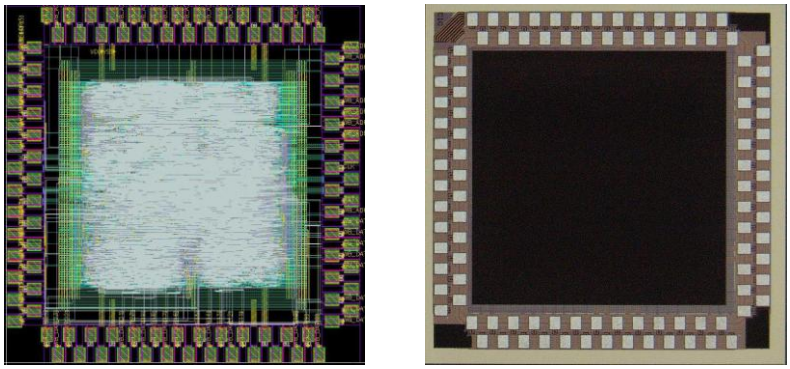


Fig. 5.1 (a) Block diagram of OR1200 processor, (b) Block diagram of the proposed low-power BSP.

The proposed BSP is implemented in TSMC 0.18 μm complementary–metal–oxide semiconductor 1P6M process and ARM design kit by using cell-based design flow. Fig. 5.2 shows the chip layout and die photo. A total of 104 pads are utilized in this work, which are 71 input/output pads and 33 power pads. The core area is 1.0×1.0 mm and the chip area is 1.75×1.75 mm. The maximum operating clock rate is 110.0 MHz at 1.8 V core supply and 3.3 V input/output (I/O) pads supply. The power consumption of core and I/O pads is 0.23 mW/MHz and 0.26 mW/MHz, respectively. One vertical and two horizontal power strips are distributed in the core to reduce voltage drop. The summary of circuit characteristics is listed in Table 5.1.



(a) (b)

Fig. 5.2 The (a) chip layout and

(b) die photo of the implemented low-power BSP.

Technology	TSMC 0.18 μm 1P6M Logic Process
Cell Library	TSMC SAGE-X Standard Cell Library
Core / Chip Area	1000×1000 mm^2 / 1750×1750 mm^2
Core Supply Voltage / I/O Supply Voltage	1.8V / 3.3V
Maximum Operating Clock Rate	110.0 MHz
Gate Count	60,132
Power Dissipation of Core	0.23 mW/MHz
Power Dissipation of I/O	0.26 mW/MHz
Power Dissipation of Chip	0.49 mW/MHz

Table 5.1 Summary of the proposed low-power BSP.

5.2 Firmware Implementation

In brief, the firmware in the low-power BSP consists of three parts, data acquisition, seizure detection, and stimulation pulse generation. Fig. 5.3 shows the flowchart of the main program which comprises seizure detection algorithm and two interrupt service routines (ISRs) for a timer. In previous work, ISR1 also computes S^1 and S^2, and the timing diagram is depicted in Fig. 5.4 (b). It wastes time on calling subprogram which is S^1 and S^2 computation, when ISR1 is started up. Moreover, because of the subprogram as mentioned above, the result of previous 32 samples is delayed. As a result, we rearrange main program, and the timing diagram is shown in Fig. 5.4 (a). The result of previous 32 samples is obtained earlier than that of previous work. The following are the details of three sub-programs.

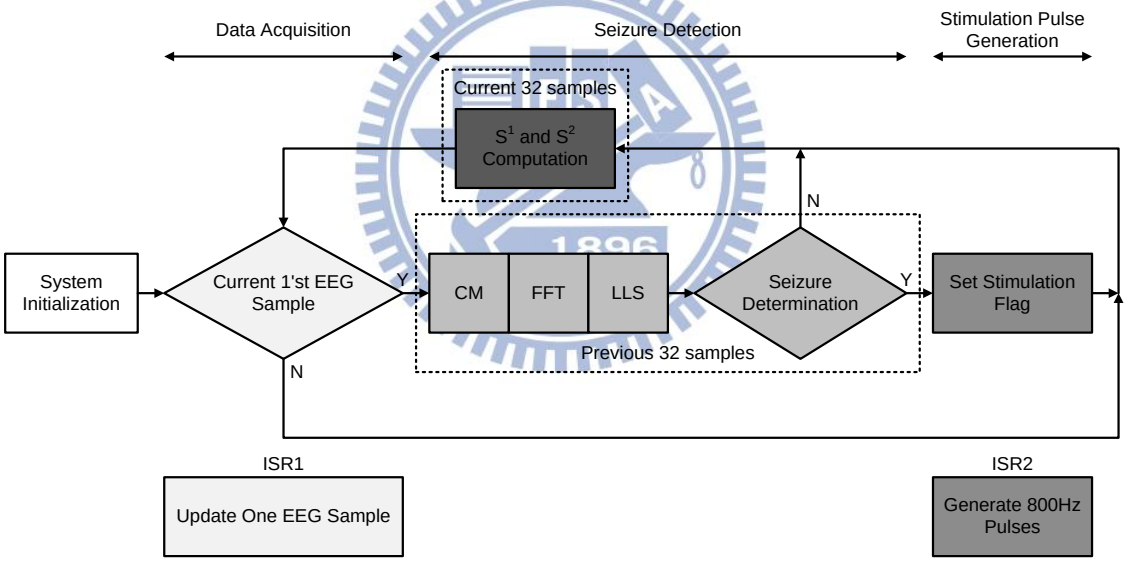


Fig. 5.3 Flowchart of (a) data acquisition, (b) seizure detection, and (c) stimulation pulse generation.

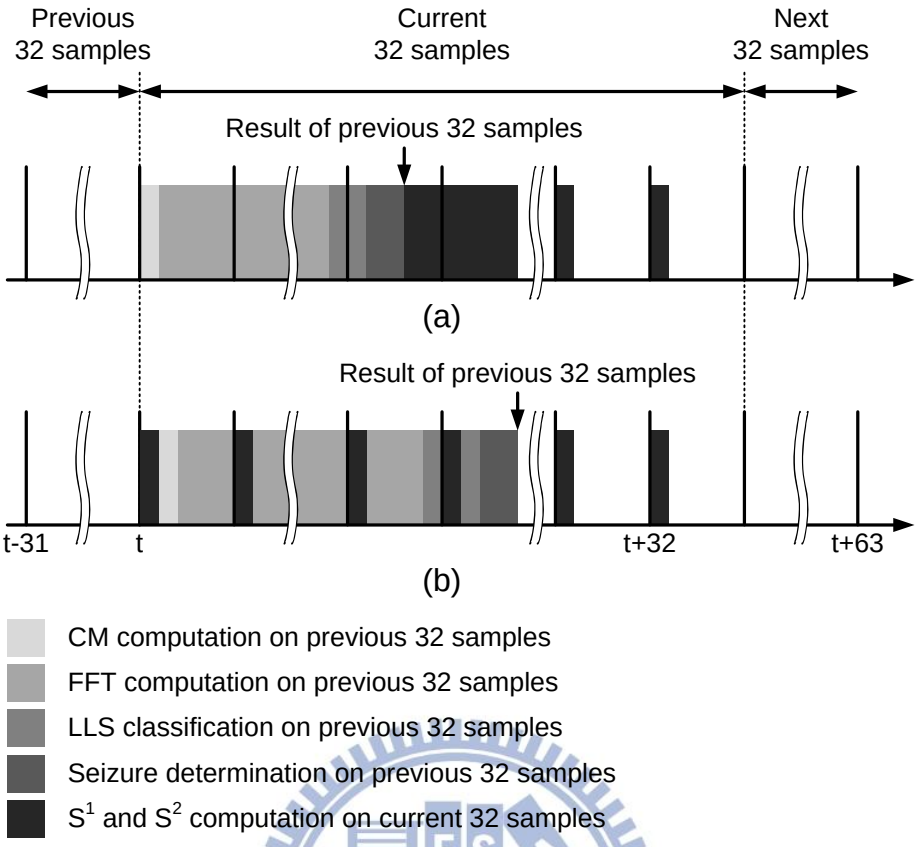


Fig. 5.4 (a) The proposed timing diagram, (b) Original timing diagram.

5.2.1 Data Acquisition

In data acquisition stage, the processor download digitized 8-bit EEG signals from GPIO registers which save the digitized data of ADC conversion. The acquisition rate is 200 Hz in this project. As a result, ISR1 is configured as 5-ms period for the data acquisition.

In previous work, declaring three arrays processes digitized data in the main program as shown in Fig. 5.5. A data buffer downloads digitized data from GPIO registers every 5ms. Before computing S^1, S^2, and FFT, main program must copy data to the S^1S^2 buffer and the FFT buffer. It wastes a lot of time on duplicating data. In this work, declaring two arrays processes digitized data in the main program as shown in Fig. 5.6. The main program also downloads digitized data to data buffer. However, the program directly computes S^1 and S^2 from the data buffer's data. It does not need time to copy data. The program also copy data to the FFT buffer because the values of FFT buffer are changed after computed. Despite additional memory the program declared, the main program which we proposed is more efficient than previous one.

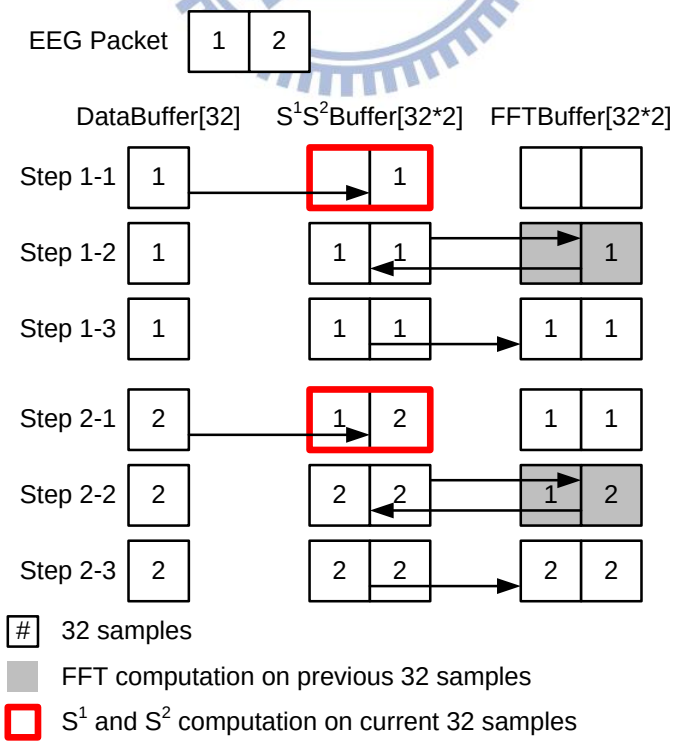


Fig. 5.5 Original data flow.

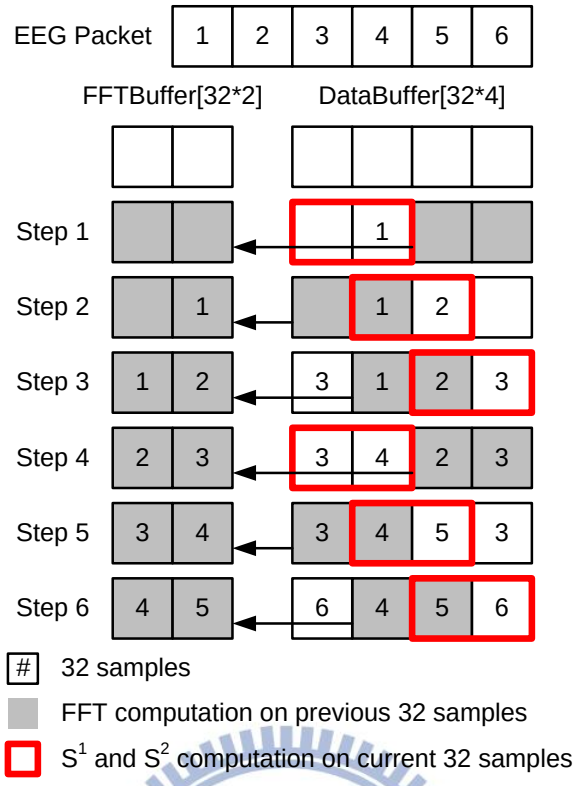


Fig. 5.6 The proposed data flow.

5.2.2 Seizure Detection

After 32-sampled data are buffered, program start to execute digital signal processing (DSP) including time domain CM, frequency domain FFT, classification LLS, seizure determination. In order not to interfere with the precise sampling time, the DSP computation is performed in the background with the lowest priority. The CM is calculated by Eq. (13) after the S^1 and S^2 values are updated by the 32-sampled data. The FFT is accomplished by applying 64-point radix-4 FFT algorithm. The counter of seizure detection is incremented if a seizure alarm is determined by the LLS calculation; otherwise, the counter is cleared. When the counter reaches “3”, the flag for the seizure suppression is set. Then, stimulation pulses are generated in ISR2.

5.2.3 Stimulation Pulse Generation

When classifier determines a seizure occurrence, the processor starts tick timer to generate 800-Hz, 40% duty cycle pulses for 0.5 s. ISR2 is set to a lower interrupt priority than ISR1, so the sampling time of EEG signals is guaranteed.

Chapter 6 Evaluation

A prototype system is implemented for the purpose of verifying the functionality and evaluating real-time performance. Fig. 6.1 illustrates the functional block diagram of the experiment setup, and Fig. 6.2 shows the testing board of the proposed low-power BSP with FPGA-based evaluation platform. In the prototype system, DE-2 70 FPGA-based evaluation board links the implemented processor and the host computer together. The host computer is used to train optimal parameters and save EEG signals of Long-Evans rats. The evaluation board which is able to upload instructions, start processor, halt processor, download results, etc. plays a role of a debugger of the processor. The EEG dataset and the instructions of processor are stored in the 2 MB memory. The proposed processor executes main program of seizure detection algorithm. Fig. 6.3 presents function verification flow of this prototype system. The power of the processor is supplied by the Keithly 2400 digital source meter, which provides 100-nA resolution under 10-mA measurement range [36]. After the system is started up, the evaluation board downloads codes of seizure detection and an EEG dataset from the host computer. Then, evaluation board enables processor. The processor accesses an EEG dataset and executes seizure detection algorithm continuously. As long as the execution is finished, the detection results are downloaded into the host computer for functional verification and performance evaluation.

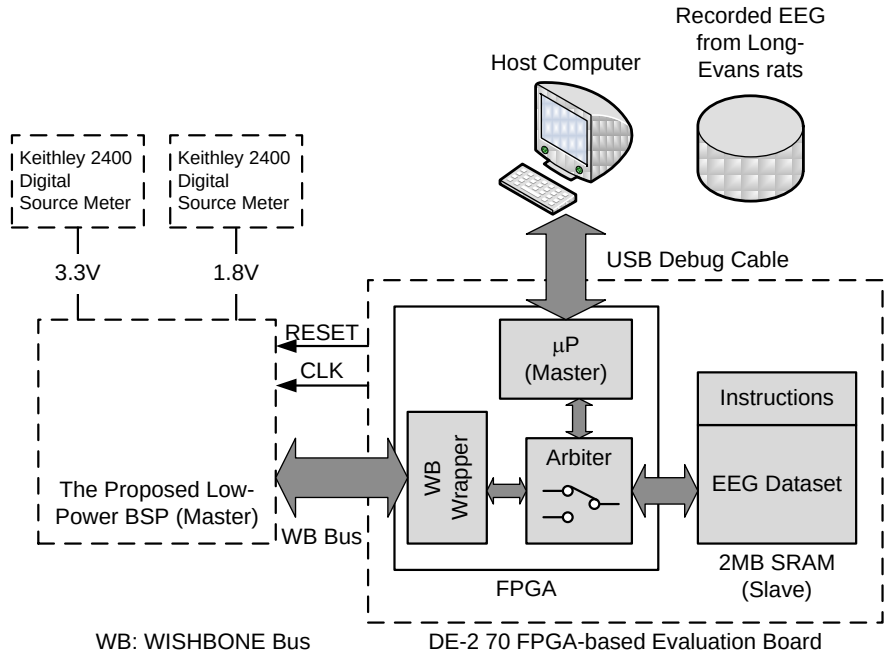


Fig. 6.1 Functional block diagram of experiment setup.

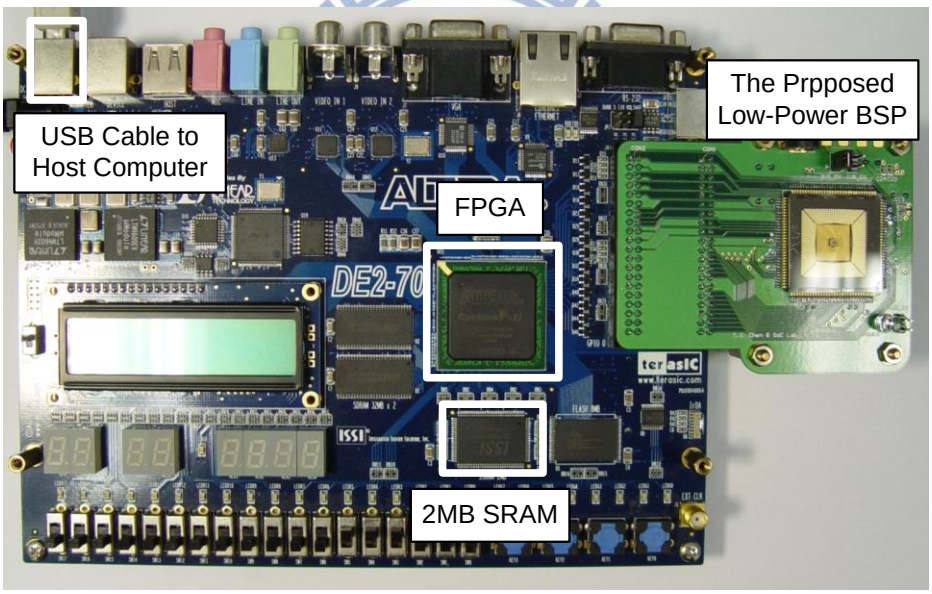


Fig. 6.2 The testing board of the proposed low-power BSP with FPGA-based evaluation platform.

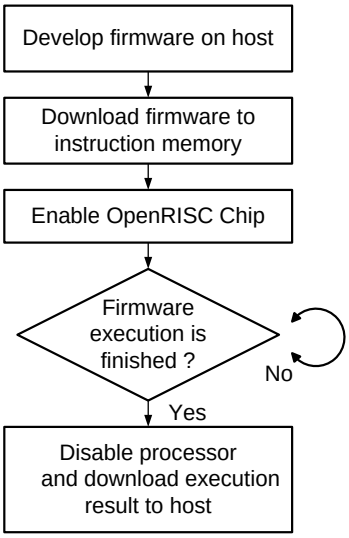


Fig. 6.3 Function verification flow.

6.1 Real-Time Seizure Detection

Fig. 6.4 shows the timing diagram of the seizure detection firmware. The highest operating clock rate can be 110 MHz. However, in order to reduce power consumption, we decrease clock rate of the low-power BSP as low as possible. In this thesis, the proposed BSP operates at 12.56 MHz clock rate for real-time seizure detection. The execution time is obtained by ticking timer between the start and the end of each task. Then, each task of the execution time downloads to host computer. In Fig. 6.4, when previous 32 samples are retrieved, the S^1 and S^2 values for CM computation are updated. After the computation of CM, FFT, and LLS classification is finished in current 32-sample cycle, the seizure determination is started to calculate. Although the DSP computation spans several sampling periods, sampled data collection which performs with the highest priority is not interfered. As shown in Fig. 6.4, after 32 sampled data are collected, determining the seizure occurrence requires about 38.8 ms latency. The total computation time is 159.35 ms, and it is less than a 32-sample cycle (160 ms). The timing diagram shows that the seizure detection algorithm can be executed continuously in the implemented processor. In order to optimize power

consumption, the subprograms are rescheduled to reduce data hazard and branch hazard, which can slow down operation frequency. After a seizure is onset, determining the seizure occurrence requires from three to four times of 32-sample (0.48-0.64 s) cycles along with DSP computation duration. As a result, it takes about 0.52-0.68 s to start the seizure suppression. Theoretically, we consider one 32-sample cycle for tolerance. The range of seizure determination delay is from four to five times of 32-sample cycles (0.64-0.80 s) and DSP computation duration (38.8 ms); that is, it needs about 0.68-0.84 s for seizure detection. Fig. 6.5 presents the EEG signals with accurate or false seizure detection. It shows that the seizure detection delay is about 0.6-0.8 s after the seizure onset.

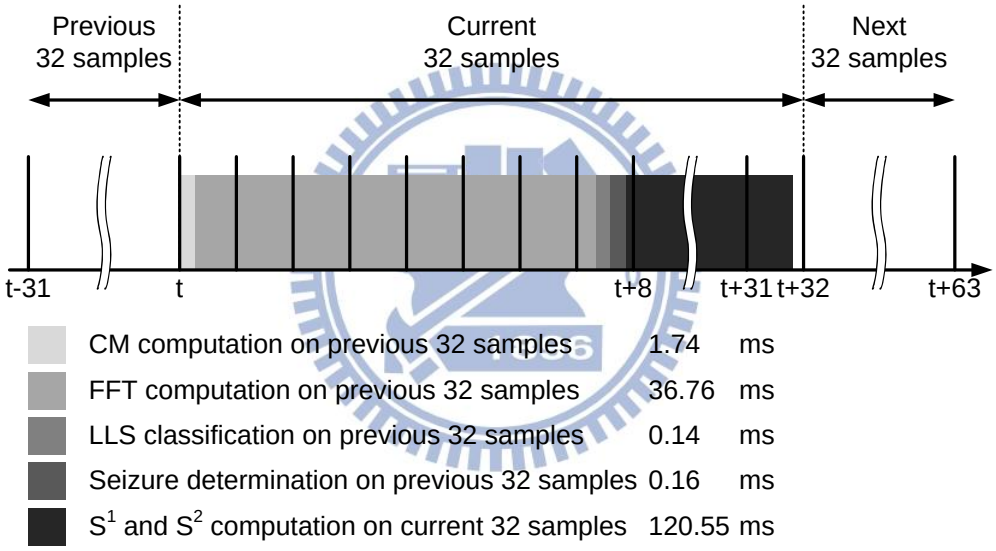


Fig. 6.4 Timing diagram of the seizure detection firmware.

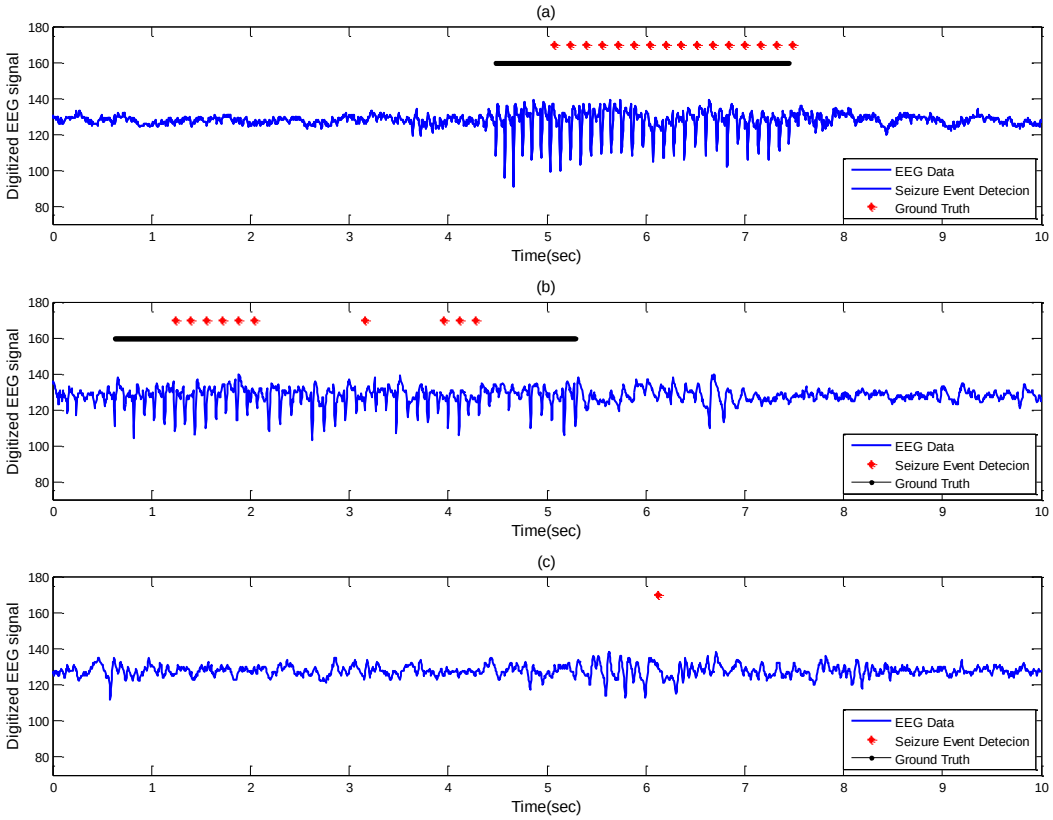


Fig. 6.5 EEG data and the seizure events detection by proposed BSP.

(a) SWD in WK state, (b) SWD in SWS state, (c) false detection in SWS state.

6.2 Seizure Detection Accuracy

Performance of the seizure detection algorithm which applies on four adult male Long–Evans rats is assessed. The four rats are affected by absence seizures. After the training procedure which describes in Chapter 4 is executed in each individual rat, and then the parameters of a training model are used for on-line seizure detection. In order to evaluate the performance of the algorithm, two rats are measured under a 5-hour execution of the system, and other two rats are measured under a 24-hour execution of the system to verify robustness. Table 6.1 shows the observed SWD duration, and the two selected frequency bands for each rat.

Subjects	Total Duration (h:m:s)	SWD Duration (h:m:s)	SWD Min (s)	SWD Mean (s)	SWD Max (s)	Band1 (Hz)	Band2 (Hz)
#1	05:00:00	00:27:34	0.50	5.09	25.69	7-10	15-18
#2	05:00:00	00:16:42	0.50	3.96	42.75	7-10	15-18
#3	24:00:00	00:49:34	0.19	4.94	43.32	7-10	15-18
#4	24:00:00	01:11:36	0.20	6.17	49.51	7-10	15-18

Table 6.1 Observed SWD duration and two selected frequency bands.

The function of the seizure detection algorithm is depicted in Fig. 6.5. The SWD signals of subject #2 in WK state, and the detection event are shown in Fig. 6.5 (a). Fig. 6.5 (b) also shows a similar detection event when the SWD signals of subject #2 occurs in SWS state. Fig. 6.5(c) shows a false detection happens on subject #2 in SWS state because the seizure detection algorithm regards the EEG signals in SWS as a seizure event. Fig. 6.6 shows that five SWDs are marked by neurologist during 40 seconds on subject #2. These SWDs are all detected by the proposed processor. One SWD marked by specialist may contain more than one detected event because of calculation of 32-sample window. We regard these detected events within marked SWD as same event; otherwise, we treated them as false detection. The definition of detection accuracy is

$$\text{Detection Accuracy}(\%) = \frac{\text{Detected SWD}}{\text{SWD}} \times 100\% \qquad (48)$$

Table 6.2 shows the results of the seizure detection algorithm. The seizure detection accuracy is above 92% as shown in Table 6.2, and it demonstrates the functionality of the implemented processor and the effectiveness of the algorithm. The robustness of the algorithm is also verified by 24-hour execution of the continuous EEG signals of rats. Although the theoretical seizure detection delay of the proposed algorithm is about 0.68 s-0.84 s, the delay would be slightly varied among subjects due to variation of EEG complexity and spectrum energy. Table 6.2 shows the detection delay is varied from 0.63 s to 0.79 s, and the average is 0.6975 s. Table 6.3 summarizes the performance of two parameter

determination methods. The fast parameter determination method is $\left(\frac{1000}{7}\right)^4$ times faster than previous work. The seizure detection algorithm is still shown several advantages, including high seizure detection rate and low detection delay after seizure onset, with the fast parameter determination method.

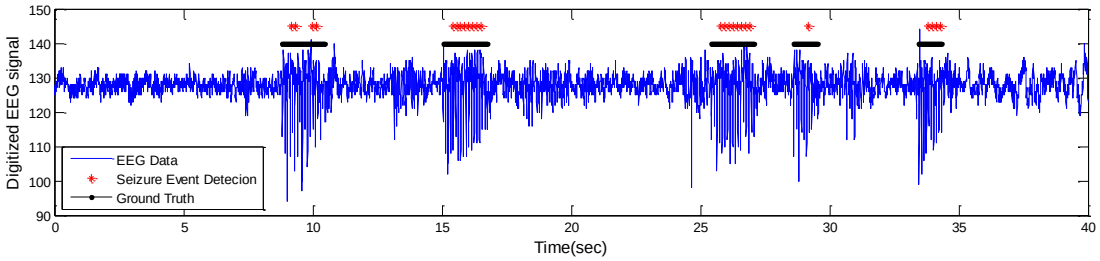


Fig. 6.6 EEG containing multiple absence seizure SWDs and detected seizure events by proposed low-power BSP.

Subjects	State	SWD	Detected SWD	Accuracy (%)	False Detection	Detection delay (s)
#1	Awake Sleep	294 31	285 28	96.31	8 28	0.79
#2	Awake Sleep	222 30	215 30	97.22	14 4	0.69
#3	Awake & Sleep	600	554	92.33	150	0.63
#4	Awake & Sleep	684	631	92.25	94	0.68

Table 6.2 Accuracy and false detection of the epileptic seizure detection algorithm.

	Original Parameter Determination Method	Proposed Parameter Determination Method
Iteration	1000^4	7^4
Detection Accuracy (%)	92-99	92-99
Detection delay (s)	<1	0.63-0.79

Table 6.3 Performance of two parameter determination methods.

6.3 Power Consumption Comparison

The clock rate of the implemented processor is 12.56 MHz for real-time seizure detection algorithm computation, and the BSP consumes 6.66 mW. The power consumption of core and I/O is 3.128 mW and 3.536 mW, respectively. The total power consumption is evaluated about 7.21 mW, including our low-noise pre-amplifier, filter [37, 38] (468 μW), 10-bit analog-to-digital converter (80 μW), and proposed BSP (6.66 mW). In previous work [23], using enhanced 8051 microcontroller and a signal conditioning board consumes 117.66 mW. Energy per seizure event determination (32-sample window) is 1.15 mJ for this work and 18.8 mJ for enhanced 8051 prototype, respectively. Compared with previous microcontroller implementation, over 90% power reduction and energy saving are improved. The evaluation results show that the overall system is powered by a 3.7-V, 1100-mAh battery, and it can be operated for 18.9 weeks. Moreover, the proposed BSP has passed the stress testing for 2 weeks to guarantee the stability. Table 6.4 summarizes the comparison of epileptic seizure detectors.

	Enhanced 8051 microcontroller + signal conditioning board	This work + our AFE
Operating Frequency	32 MHz	12.56 MHz
Power Consumption of Analog Part	N/A	0.548 mW
Power Consumption of Digital Part	N/A	6.66 mW
Total Power Consumption	117.66 mW	7.21 mW
Energy per Seizure Event Determination	18.8 mJ	1.15 mJ
Power Normalization	100%	6.2%
Battery Life (3.7V, 1100 mAh)	28 hours	18.9 weeks

Table 6.4 Comparison of epileptic seizure detectors.

Chapter 7 Conclusion and Future Work

7.1 Conclusion

In this thesis, a fast parameter determination method is proposed. It is proposed that using the mean and the multiples of standard deviation finds the optimal model rapidly. The proposed parameter determination method is 416×10^6 times faster than our previous work, and it can attain the same performance. Moreover, a processor core which bases on RISC technology consumes only 6 mW for real-time epileptic seizure detection algorithm. Compared with our previous prototype, the measurement results show that the implemented processor can reduce 93.8% power consumption. The developed bio-signal processor, firmware and epileptic seizure detection algorithm is able to detect the seizure signals in 0.63-0.79 s, and the detection accuracy is 92-99%. The measurement results are based on the recorded EEG signals of four free moving animal models.

7.2 Future Work

The OpenRISC core will be integrate with analog front-end circuitries and stimulators to realize a chip-on-board seizure controller as shown in Fig. 7.1 (a). The AFE and stimulator board is shown in Fig. 7.1 (b), and the epileptic seizure detector board which uses Altera Cyclone III FPGA is shown in Fig. 7.1 (c). The successful of this research provides a solid base to integrate with analog front-end circuitries and stimulators to build up a system-on-a-chip solution. The developed seizure detector can be applied to monitor the online EEG signals and integrate with analog front-end circuitries and an electrical stimulator to perform a closed-loop seizure controller in the future.

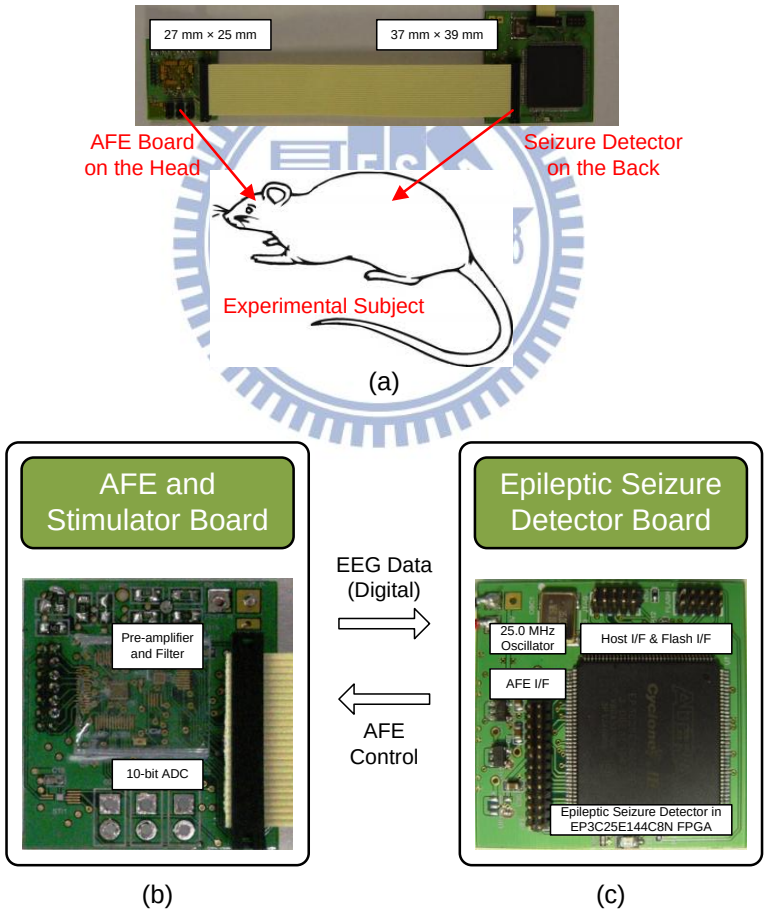


Fig. 7.1 Closed-loop seizure controller using FPGA.

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- T.-J. Chen, H. Chiueh, S.-F. Liang, **S.-T. Chang**, C. Jeng, Y.-C. Hsu, and T.-C. Chien, "The Implementation of a Low-Power Biomedical Signal Processor for Real-Time Epileptic Seizure Detection on Absence Animal Models," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 1, no. 4, Dec. 2011.
- T.-J. Chen, C. Jeng, **S.-T. Chang**, H. Chiueh, S.-F. Liang, Y.-C. Hsu, and T.-C. Chien, "A Hardware Implementation of Real-Time Epileptic Seizure Detector on FPGA," in *IEEE Biomedical Circuit and Systems Conference (BioCAS '11)*, San Diego, USA, Nov. 10-12, 2011.
- **S.-T. Chang**, T.-J. Chen, C. Jeng, S.-F. Liang, and H. Chiueh, "Fast Training for Epileptic Seizure Detector," in *3rd International Conference on Neuroprosthetic Devices (ICNPD '11)*, Sydney, Australia, Nov. 25-26, 2011, pp. 26-28.
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