國 立 交 通 大 學

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碩 士 論 文

多通道閉迴路癲癇偵測之低功率積體電路實現

Design and Implementation of a Low-power Multi-channel Closed-loop Epileptic Seizure Detector

研究生：鄭　錡

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中　華　民　國　一　百　年　十　二　月

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摘要

全球約有五千萬的人患有癲癇疾病，為第三大神經系統失調疾病。約有 75%的病人可以透過藥物長期治療，或是利用外科手術切除患部而控制癲癇，但仍然有 25%的癲癇患者無法透過上述兩種方式成功治療。因癲癇是由大腦的不正常放電引起，可刺激腦部達到治療癲癇，並透過腦電圖進行臨床評估及癲癇偵測發作。早期利用腦部刺激開迴路控制器進行癲癇治療，但因準確率只有 45%，為了提高準確率，近年提出的癲癇腦部刺激閉迴路控制器為創新及有效的替代方案。

在本團隊先前的研究中，已透過 8051 平台實現即時癲癇偵測與抑制系統。但為了降低整個系統的功率以及面積，在此篇研究中，先利用 FPGA 驗證演算法的準確率，再使用 ASIC 方式實現多重頻道低功率閉迴路癲癇偵測電路，具有多重頻道、低功率、低面積和即時運算判斷的特點。偵測癲癇的準確率可達到 94.6%，在 0.63-0.80s 內偵測到癲癇啟動電刺激。利用台積電 0.18μm CMOS 製程製作晶片，功率消耗可降低到 114.4μW，比原先系統降低了 99.5%。

關鍵字：癲癇、SoC、腦電圖、閉迴路、系統晶片。

Design and Implementation of Low-power Multi-channel Closed-loop Epileptic Seizure Detection

Student: Chi Jeng Advisor: Professor Herming Chiueh

SoC Design Lab, Institution of Communication Engineering,

National Chiao Tung University

Hsinchu 30010, Taiwan

Abstract

Epilepsy is one of the most common neurological disorders, by which around 1% of the people in the world are affected. Unfortunately, 25% of the epilepsy patients cannot be treated sufficiently by antiepileptic drugs and epilepsy surgery. If seizures cannot be well controlled, the patients experience major limitations in their lives. In recent years, open-loop seizure controllers, such as vagus nerve and deep brain stimulation devices, have been proposed, but the effective rates of these devices are limited to 45%.

In addition, low power and small hardware area are two important targets for implantable and portable devices. To overcome these issues, a real-time closed-loop seizure detection method is proposed. A multi-channel closed-loop epileptic seizure detector (MCESD) receives EEG signals of rats through ADC and delivers a stimulus at seizure. The seizure detection algorithm is realized by MCESD. The MCESD is implemented in a TSMC 0.18μm CMOS process. The seizure detection accuracy of device is above 94.6% from seizure detection algorithm with MCESD implementation, and the power of chip consumes 114.4μW.

Keywords: Epilepsy, seizure detection, closed-loop, System-on-a-chip (SOC).

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經過兩年半的訓練，終於順利完成論文。首先誠摯地感謝指導教授闕河鳴老師。老師在研究的過程中，不時討論並指點我正確的方向，使我從研究中學到思考邏輯的正確性及嚴謹性，謝謝老師在我第一次下線失敗時，給我機會重新下線。此外，並強調口頭報告的格式及態度，加強學生的表達能力，讓我學到許多寶貴的經驗。

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要感謝乾媽一家讓我在新竹可以吃到熱騰騰的家常菜，感受家庭的溫暖。謝謝母親和狗兒多多的關心及付出，給我繼續努力的動力。謝謝碩士生活的給予幫助的大家，讓我的生活變得多采多姿更加有趣。

鄭錡

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Chapter 1 Introduction

1.1 Motivation

Epilepsy is a common neurological disorder characterized by a predisposition to an unprovoked recurrent seizure. Approximately 1% of the people in the world have epilepsy. Antiepileptic drugs are the mainstay of treatment but many suffer from systemic side effects, and one-third of the patients are non-responsive. Half of the refractory patients may profit from epilepsy surgery [1]. Unfortunately, 25% of the epilepsy patients cannot be treated sufficiently by any available therapy [2]. If seizures cannot be well controlled, the patients experience major limitations in family, social, educational, and vocational activities.

Epilepsy is caused by abnormal discharges in the brain, and electroencephalogram (EEG) is the physiological signals reflecting the brain dynamics. Thus EEG has been an especially valuable tool for evaluation, detection, and treatment of epilepsy. In recent years, there has been growing interests in developing responsive epilepsy therapy devices that like electrical stimulation to stop seizures at their onset. Hence, current devices for epilepsy can be categorize two types, open-loop and closed-loop [3].

Open-loop devices chronically modulate brain activity, and the stimulation is regularly switched through an internal clock to restrain seizures, such as the vagus nerve stimulation or deep brain stimulation. However, the effective rates of these devices are limited to 45%. Therefore, a closed-loop device is proposed, which is more complex devices that monitor physiological signals and make a therapeutic response based on changes in these signals. One important technique required for a on-line seizure detection system is that it can suppress the seizure as early as possible when the seizure occurs.

A real-time signal process and feedback are the kernel of a closed-loop seizure controller. Recent research has proposed the implementation of hardware prototypes for epileptic seizure detection [4-12]. Some available epilepsy-related systems primarily focus on off-line analysis of recording brain activities. Lately, some groups have developed real-time epileptic seizure detection systems. Wavelet analysis, spectral analysis and support-vector machine (SVM) are used to analyze signals and detect seizures, and the epileptic seizure detection accuracy average is above 86% in most of papers. The response time for seizure detection is more than 3.7 seconds or often not mentioned. In [4, 7, 12], closed-loop seizure control systems relied on analog circuits extracting seizure features. In these closed-loop systems, the discontinuous EEG data fragments are often used to validate detection algorithm. However, it's unsatisfactory to validate the robustness of detection algorithm.

Therefore, the seizure detection algorithm combining approximate entropy (ApEn) with the EEG spectrum to detect seizures has been proposed. We use the continuous EEG signals to prove that the detection algorithm works and keeps the highly successful detection rate. However, the previous implementations based on 8051 microprocessor consume more power and occupy more area compared with pure hardware implementations. Consequently, we propose a multi-channel closed-loop epileptic seizure detector (MCESD) for detection seizure on different locations of brain, which designed and synthesized to register transfer language (RTL). The MCESD is implemented in a TSMC 0.18μm CMOS process.

1.2 Thesis Organization

The rest of this thesis is organized as follows. In Chapter 2, the system architecture of seizure detection will be the beginning. After that, the previous work, 8051 microcontroller will be mentioned. Next, a brief introduction of multi-channel closed-loop epileptic seizure detector is introduced. Finally, the animal models used will be end of Chapter 2.

Chapter 3 describes the epileptic seizure detection algorithm, which contain four parts. First and second parts are feature extraction, and third part is linear classifier. Fourth part, the adaptive threshold will be described. Finally, the training method will be presented. The topic of Chapter 4 is design of the hardware. One is 2-channel seizure detector, which is main function of the chip. Another is I^2C register bank, which is an interface to transmit data. Last are data receiver and clock generator to control external components.

The following Chapter 5 is function verification and simulation. In Chapter 6, the testing and experimental result of MCESD is presented. Chapter 7 ends the whole thesis. Brief conclusion and the future works will be arranged in this chapter.

Chapter 2 System Architecture

In this chapter, the architecture of seizure detection are introduced, including previous work - 8051 microcontroller and this study - multi-channel closed-loop epileptic seizure detector (MCESD). Next, the fundamental of seizure types are illustrated. Then, all kinds of EEG patterns in a continuous recording of a Long-Evans rats are described. Finally, the animal preparation is presented.

2.1 Architecture of Seizure Detection

The closed-loop seizure control system contains implantable electrodes and an implantable processor including epileptic seizure detector and analog front end, as shown in Fig. 2.1. First, the EEG signals are delivered into analog front end by implantable electrodes. Then analog front end, which consists of amplifier, band-pass filter and A/D converter, transform the small and analog signals into digital data. Next, the epileptic seizure detector could perform continuous real-time detection and control stimulators. Finally, a 20-50μA constant current stimulation pulse is generated to restrain seizure from simulators.

In this study, the real-time closed-loop system scheme is based on large portion of epileptic seizure detector. Many technology can implement the digital seizure detector, such as digital signal processor (DSP), field-programmable gate array (FPGA), and application-specific integrated circuit (ASIC). DSPs have high processing capability but the large power is consumed by other hardware accelerators. Modern high-density FPGA combine embedded processor and custom hardware accelerator to achieve high performance;

however, it also consumes high static power cause of its advanced fabrication technology. ASIC is an integrated circuit which is highly specialized for a particular scenario or application. This solution is highly optimized in terms of area, power, and speed to perform its designated task. Therefore, ASIC is chosen in this research.

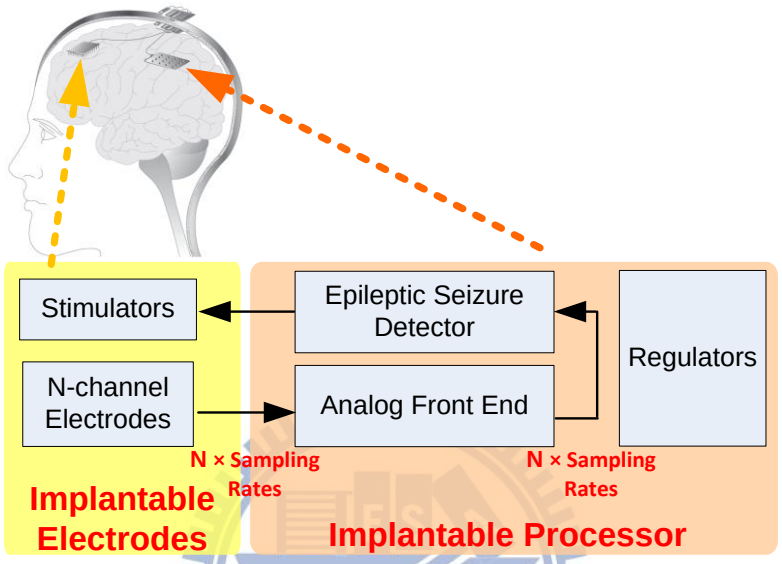


Fig. 2.1 The architecture of the proposed closed-loop seizure control system

2.1.1 Previous Work: 8051 Microcontroller

In our previous implementation, a wireless on-line seizure controller has been implemented with an enhanced 8051 microcontroller in freely moving subjects [13]. The seizure controller consisted of three modules: signal conditioning, microcontroller and stimulator. Spontaneous brain activities of the rat were amplified and band-pass filtered by the conditioning board. The core component on a microcontroller board was a CC2430 system-on-chip RF IC. The board was carried by each experimental subject, and a host computer for remote real-time monitors of spontaneous brain activities, while they were communicated based on a 2.4GHz wireless IEEE 802.15.4/ZigBee protocol.

8051 microcontroller was built up on single-channel, 200Hz sampling rate, 32MHz computing rate, and the execution time is 24.1ms. An 800Hz, 40% duty cycle, and 30-50146.19μA stimulation pulse train for 0.5s was feedback to the rat to stop spontaneous SWDs. The 8051 microcontroller consumed 117.66mW, and the power consumption of such implementation was significant for implantable devices.

2.1.2 Multi-channel Closed-loop Epileptic Seizure Detector (MCESD)

In this research, the hardware of epileptic seizure detector for closed-loop seizure control is proposed. Fig. 2.2(a) illustrates the prototype system, which supports 2-channel EEG signals, is implemented in board level to verify real-time capability. A multi-channel closed-loop epileptic seizure detector (MCESD) receives EEG signals of rats through ADC and delivers a stimulus at seizure. The seizure detection algorithm is realized by MCESD, and the algorithm is detailed in Chapter 3. The hardware block diagram is shown in Fig. 2.2(b). 2-channel seizure detector is the main function of MCESD chip, and detail of four blocks are introduced in Chapter 4.

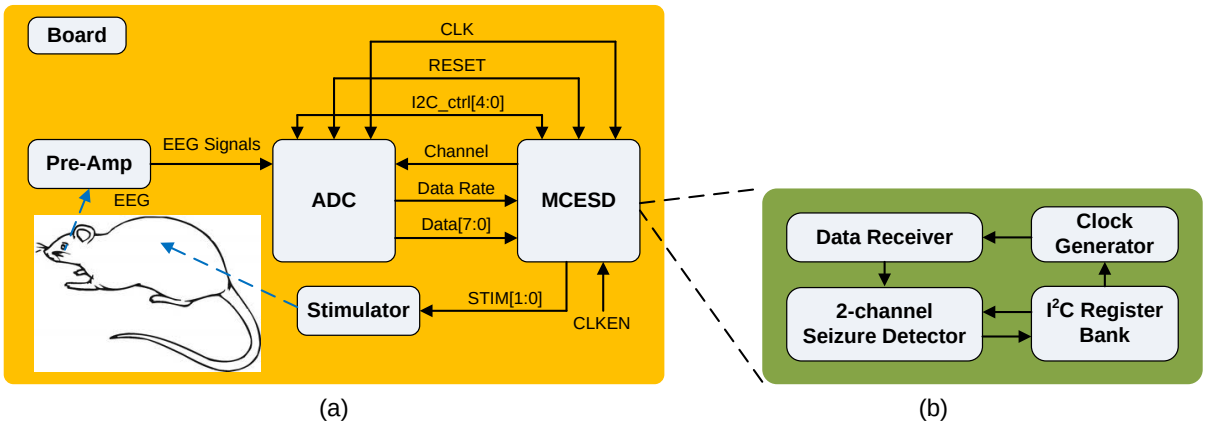


Fig. 2.2 (a) The closed-loop system architecture; (b) the hardware block diagram

2.2 Materials

In order to develop an epileptic seizure controller, we have to understand the seizure type. The epilepsy detection algorithm is applied to absence seizures that is described in this section. In addition, the EEG signals are classified to five events, which are the materials for training animal's model. Finally, the surgery details of rats are evaluated for animal test.

2.2.1 Seizure Types

Seizures are often associated with a sudden and involuntary contraction of a group of muscles and loss of consciousness. However, a seizure can also be as subtle as a fleeting numbness of a part of the body, a brief or long term loss of memory. Clinicians organize different types of seizure according to the source of the seizure within the brain. The two major seizures are partial seizures and generalized seizures. Partial seizures are divided on the extent to which consciousness is affected. If consciousness is unaffected, then it is a simple partial seizure; otherwise it is a complex partial seizure. Generalized seizures are classed according to the effect on the body, but all involve loss of consciousness. These include absence, myoclonic, clonic, tonic, tonic-clonic, and atonic seizures. Our experimental rats with absence seizures are Long-Evans rats, so absence seizures is introduced in this study.

Absence seizure — also known as petit mal — involves a brief, sudden lapse of consciousness. Absence seizures are more common in children than adults. Someone having an absence seizure may look like he or she is staring into space for a few seconds. The difference between absence seizure and normal trance is that someone made a response immediately from external impetus when he or she was in a trance; however, the patient

didn’t answer until a absence seizure ended. Absence seizures appear mild compared with other types of epileptic seizures, but they can be dangerous. Children must be supervised carefully while swimming or bathing because of the danger of drowning. Teens and adults may be restricted from driving and other potentially hazardous activities.

Absences seizures are brief, generalized epileptic seizures of sudden onset and termination. They have 2 essential components: clinically the impairment of consciousness and EEG generalized spike-and-slow (SWD) wave discharges. The time–frequency structure of SWDs contains important information about the mechanisms of this type of brain paroxysmal activity. The frequency of SWD in patients with absence epilepsy is typical in the range of 3-5Hz [14, 15].

2.2.2 Animal Preparation

The genetic defect of Long-Evans rats causes spontaneous SWD, so adult Long-Evans rats with spontaneous spike-and-wave discharges (SWDs) were used in the study. The EEG characteristic of spontaneous SWD is much more close to epileptic patients’ EEG in the clinical aspect. The animals were kept in a room under a 12:12-hour light-dark cycle with food and water provided ad libitum. All surgical and experimental procedures were reviewed and approved by the Institutional Animal Care and Use Committee of the National Cheng Kung University.

The rats were anesthetized with sodium pentobarbital (50mg/kg, i.p.). Subsequently, it was placed in a standard stereotaxic apparatus. Screw electrodes were bilaterally implanted over the area of the frontal barrel cortex (anterior 2.0mm, lateral2.0 mm with regard to the bregma). A four-microwire bundle, each made of Teflon-insulated stainless steel microwires

(#7079, A-M Systems), was used to stimulate the right-side zona incerta (ZI). A ground electrode was implanted 2mm caudal to the lambda. Dental cement was applied to fasten the connection socket to the surface of the skull. Following suturing to complete the surgery, animals were given antibiotics and housed individually in cages for recovery.

Two weeks after the surgery, each animal was placed in the recording environment at least two times (1 hour/day) prior to testing. In this procedure, about 90% of Long-Evans rats show spontaneous SWDs, which were used for continuous EEG recording. Continuous EEGs from 5 hours to 24 hours (contained one circadian cycle) were recorded and analyzed to assess our seizure detector in this study.

2.2.3 Continuous EEG Recording

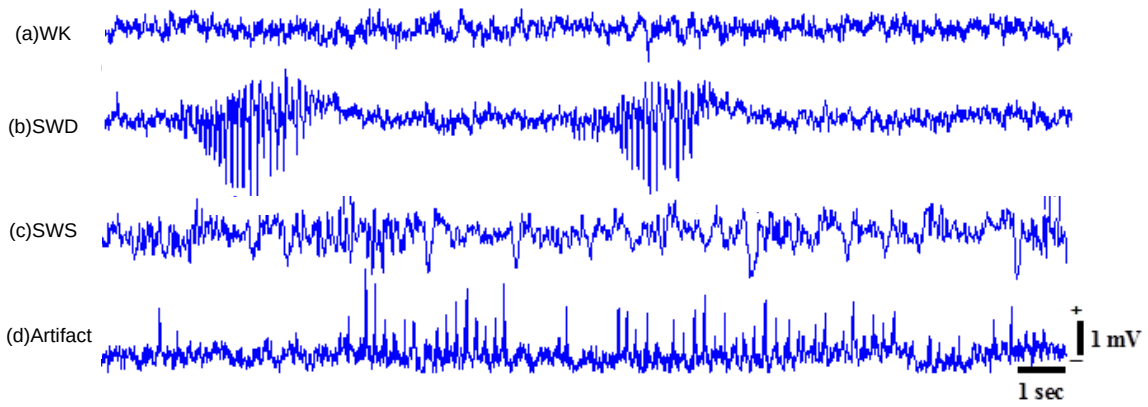


Fig. 2.3 All kinds of EEG patterns in a continuous recording of a Long-Evans rats

In order to develop high accuracy of a seizure detection system, the controller must be powerful enough to avoid false alarms caused by various activities. Fig. 2.3 shows all kinds of EEG patterns in a continuous recording of a Long-Evans rat. (a) and (b) are wakefulness (WK), spike-and-slow wave discharges (SWDs) respectively. We could observe obvious

shake-up waves in EEG signal. Slow-wave sleep (SWS) and movement artifact are included in (c) and (d) respectively.

Two essential stages of EEG signal processing were executed in Long-Evans rats. In the first stage, continuous EEG signals of each rat were recorded without providing electrical stimulation, and the data were classified according to seizures (SWD) and non-seizures (WK, SWS, and artifact) for feature extraction. These spontaneous events were used to off-line training and got the parameters of a seizure detection model. The second stage, optimal parameters is loaded into seizure detector at initial. The rats went through an on-line closed-loop seizure controller with immediate feedback and electrical stimulation.

Chapter 3 Epileptic Seizure Detection Algorithm

The seizure detection algorithm is realized by MCESD. The chapter illustrate the four parts of algorithm, entropy analysis, spectral analysis, linear least squares, and adaptive threshold, respectively. In addition to the algorithm, experimental flow is described in the end of this chapter.

3.1 Detection Algorithm

The seizure detection algorithm is realized by MCESD. Fig. 3.1 shows the flow of the algorithm. In this algorithm, the sampling rate is 200Hz (5ms), and 64-point EEG data is defined a sampling window (0.32s) with 50% overlap, in Fig. 3.2. The 64-point window is to reduce the detection delay time and inspirit quick seizure detection.

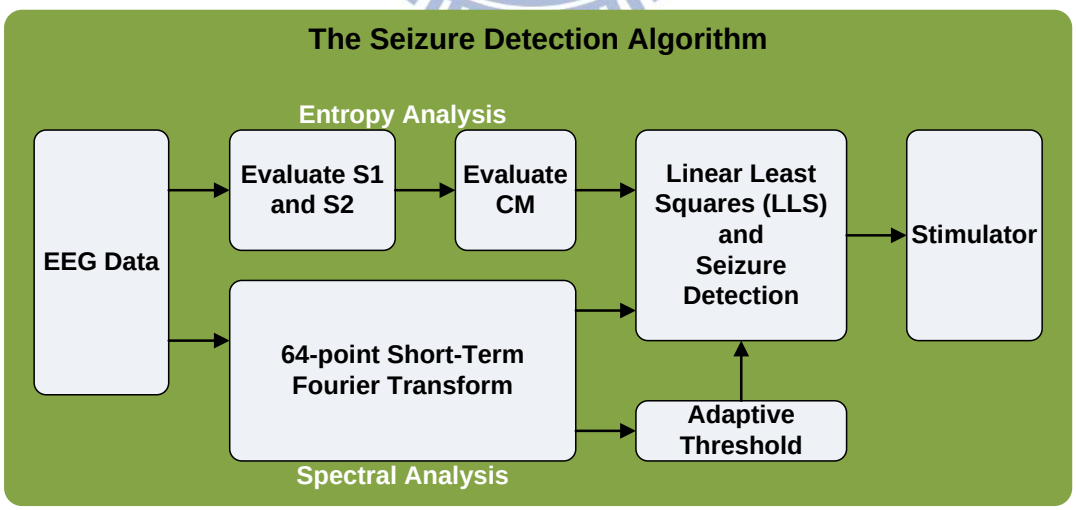


Fig. 3.1 The steps of seizure detection algorithm

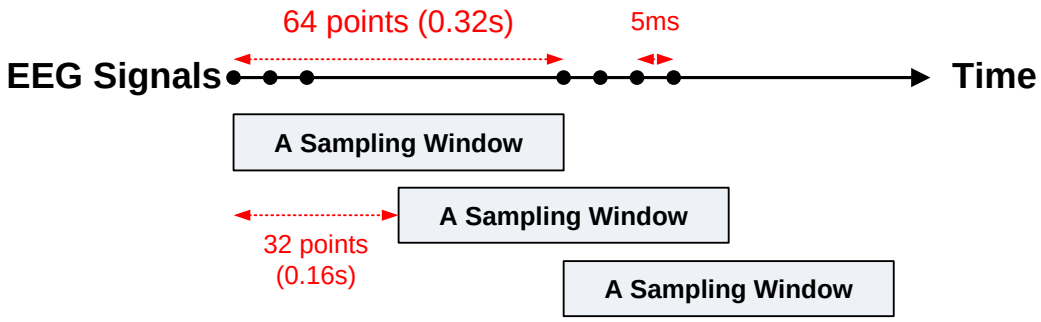


Fig. 3.2 A sampling window include 64 EEG data with 50% overlap

The time-domain and frequency-domain characteristics of EEG signals were integrated as the features and the linear least square (LLS) model was utilized to implement seizure classifier. Entropy has been used for seizure because the EEG pattern of a seizure is more regular than that in normal states [16]. According to the animal test, the absence seizure has large power at 7-9 Hz and 14-18Hz [17]. The fast Fourier transform (FFT) was used to calculate powers of frequency bands. Therefore, EEG band powers were combined to ApEn analysis to improve the performance of epileptic seizure detection. Because the objects' seizure conditions are different, we need to train the optimal parameters by EEG of subjects through an off-line process. The three features and the parameters of LLS classifier compute at on-line seizure detector [18].

3.1.1 Complexity Analysis

According to the phenomenon that the EEG signals of a seizure is more regular than that in normal states, entropy has been used for analysis and detection. Approximate entropy (ApEn) is a measure, quantifying a time series of signals and is therefore a preferred measure of randomness or regularity.

Approximate entropy

First, given a time-series of data $u(1)$, $u(2)$,. . . , $u(N)$, from measurements equally spaced in time, forming a sequence of vectors $x(1)$, $x(2)$, . . ., $x(N-m+1)$ in R^m, defined by $x(i) = [u(i), u(i+1), . . ., u(i+m-1)]$ for $1 \le i \le N-m+1$, where N is the window size, and m is the compared length. Then, We must define $d[x(i), x(j)]$ for vectors $x(i)$ and $x(j)$. The two vectors compare each element. For each i and j, $1 \le j$, $i \le N-m+1$.

$$d[x(i), x(j)] = \max_{k=1,2,\ldots,m-1} (|u(i+k) - u(j+k)|) \tag{3.1}$$

$$C_i^m(r) = \frac{\sum_{j=1}^{N-m+1} \omega_j}{N-m+1} \qquad \omega_j = \begin{cases} 1, & if\ d[x(i), x(j)] \le r \\ 0, & else \end{cases} \tag{3.2}$$

where r is the tolerance of d. Finally, the approximate entropy is calculated by

$$\Phi^m(r) = \frac{\sum_{i=1}^{N-m+1} \ln C_i^m(r)}{N-m+1} \tag{3.3}$$

$$ApEn(m, r, N) = \Phi^m(r) - \Phi^{m+1}(r) \tag{3.4}$$

CM Entropy

A simplified measurement based on the ApEn is proposed to reduce the computational cost, so we define a complexity measurement, *CM*.

$$S^m = \frac{\sum_{i=1}^{N-m+1} C_i^m(r)}{N-m+1} \tag{3.5}$$

$$CM^m = \frac{S^{m+1}}{S^m} \tag{3.6}$$

The average of r is 5 for Long-Evan rats which is determined in off-line training, but in fact it's variable for each object. Therefore, we could define the four steps to calculate the *CM*,

as shown in Fig. 3.3 . The first step is to load EEG signals. Although we define the sampling window size is 64-point EEG before, at this step the entropy window is divided to four parts, N= 16, to decrease the complicated of algorithm, as shown in Fig. 3.4. Besides, the parameter setting is m=1.

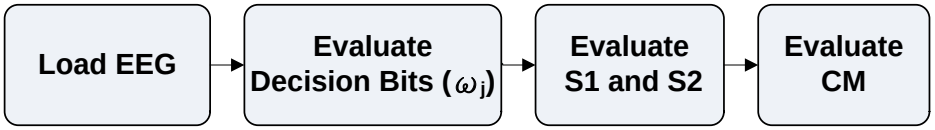


Fig. 3.3 The Entropy Extraction Flow

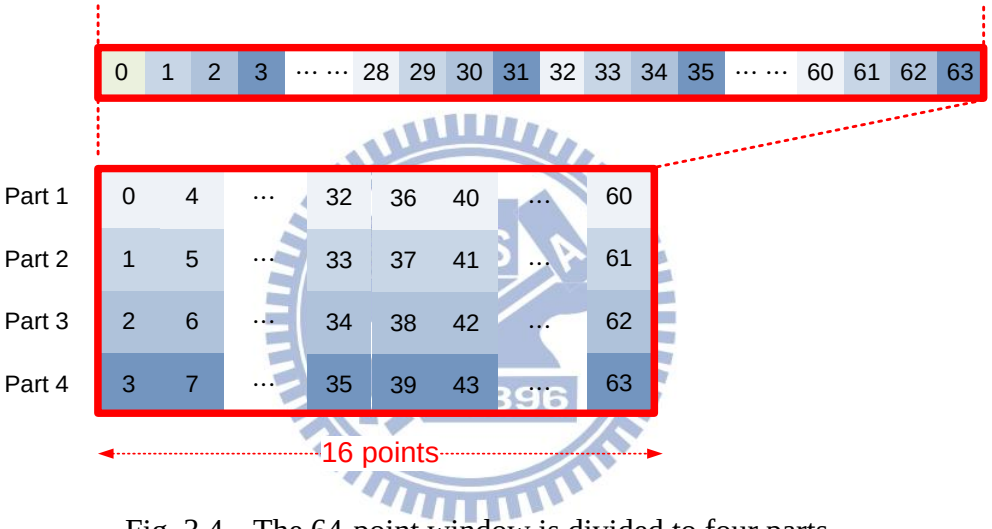


Fig. 3.4 The 64-point window is divided to four parts

The second step evaluates decision bit (ω_j), and next step evaluates S^1 and S^2. The equations are (3.7) to (3.10). The decision bits are shown in Fig. 3.5, in which (a) correspond to $d[x(i), x(j)]= |u(i) – u(j)|$; (b) correspond to $d[x(i+1), x(j+1)]= |u(i+1) – u(j+1)|$. If the comparison distance between data is less than a threshold (r), decision bits are set to be logic 1; else are set to be logic 0. The decision bits, A_{ij}, B_{ij}, and C_{ij} are one bits (0 or 1), and C_{ij} equate A_{ij}& B_{ij} in equation (3.10) which correspond to $d[x(i), x(j)]= \max| u(i) – u(j), u(i+1) – u(j+1)|$, in Fig. 3.5(c). S^1 is evaluated by A_{01} to A_{de}, and S^2 is evaluated by C_{01} to C_{de}. Then, the CM^p is evaluated by S^2/ S^1 for p = 1, 2, 3, 4. Finally, the CM is evaluated by four CM^p, which ranging from 0 to 4.

$$d[x(i),x(j)] = |u(i) - u(j)|$$

$$A_{ij} = \begin{cases} 1, & if\ d[x(i),x(j)] \le r \\ 0, & else \end{cases} \tag{3.7}$$

$$S^1 = \sum_{i=1}^{14} \sum_{j=i+1}^{15} A_{ij} \tag{3.8}$$

$$B_{ij} = \begin{cases} 1, & if\ d[x(i+1),x(j+1)] \le 2r \\ 0, & else \end{cases} \tag{3.9}$$

$$C_{ij} = A_{ij} \,\&\, B_{ij} \tag{3.10}$$

$$S^2 = \sum_{i=1}^{14} \sum_{j=i+1}^{15} C_{ij} \tag{3.11}$$

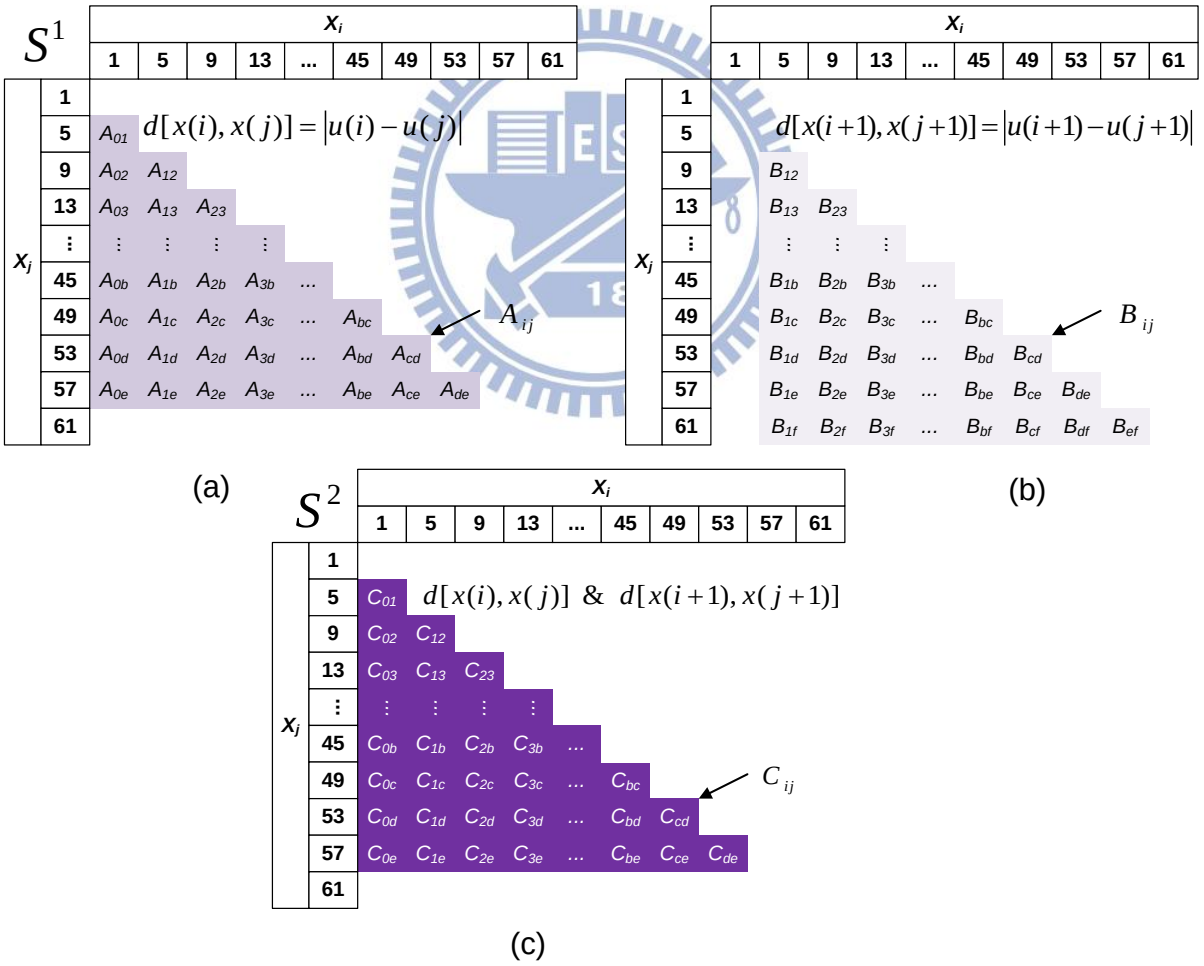


Fig. 3.5 Evaluate decision bit (ω_j)

However, the sleep signal is similar to seizure signals at time-domain, because those signals revealed a rhythmic-like pattern. Fig. 3.6 shows the results of entropy. According to Fig. 3.6(c) and (d), the entropy result of SWS and artifact are instable. Thus, to improve the performance, spectral features combine with entropy analysis.

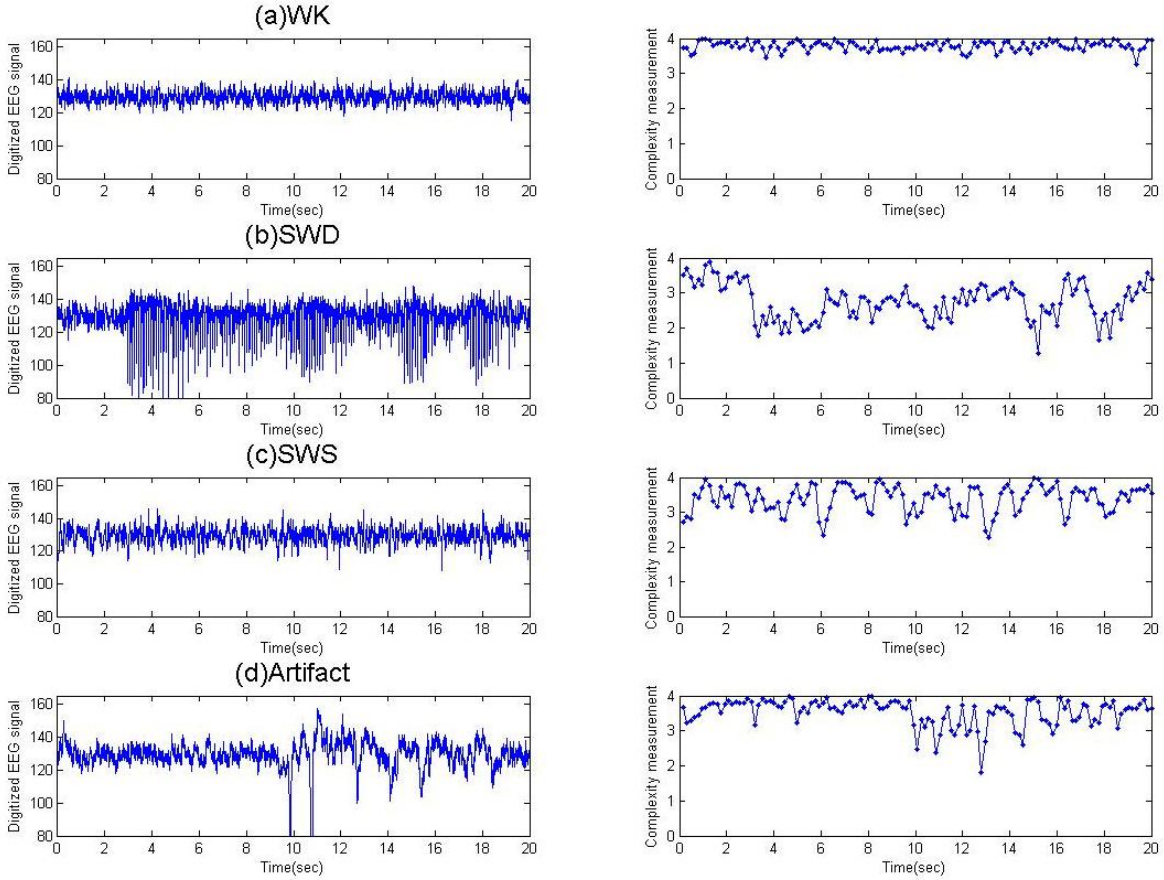


Fig. 3.6 Entropy values in different behavioral states

(a) WK, (b) SWD, (c)SWS, and (d) Artifact

3.1.2 Spectral Analysis

The fast Fourier transform (FFT) is used to calculate powers of frequency bands, and it is well-established in various microprocessor. Fig. 3.7 shows the methods to build the correlation between time domain and frequency domain. In time domain, seizure events are set to one, or else are set to zero. The vectors are correlated with powers of specific frequency bands. In this algorithm, we use Pearson correlation coefficient to determine spectral features. Consider there are k segments, and let $SP_k(t,f)$ be the spectrogram of the k^{th} segment. Define $x_k(m)$ as the spectrum index which is the spectrogram in frequency m. Then, define y as the SWD index. The correlation coefficient $Corr_k(m)$ of the seizure index and spectrum index is given by (3.14). Finally the average correlation coefficient of k segments is given by (3.15).

$$x_k(m) = [SP_k(1,m), SP_k(2,m), \ldots] \tag{3.12}$$

$$y_k = [\phi_k(1), \phi_k(2), \ldots] \quad \phi_k(t) = \begin{cases} 1, & \textit{if the state in time t is seizure} \\ 0, & \textit{else} \end{cases} \tag{3.13}$$

$$Corr_k(m) = \frac{\sum (x_k(m) - \overline{x_k(m)}) \times (y_k - \overline{y_k})}{\sqrt{\sum (x_k(m) - \overline{x_k(m)})^2 \times \sum (y_k - \overline{y_k})^2}} \tag{3.14}$$

$$C(m) = \frac{\sum_k Corr_k(m)}{k} \tag{3.15}$$

The absence seizure has large power at first harmonic (7-11 Hz) and second harmonic (14-18 Hz). Sleep states contain delta rhythms and have large power under 4Hz. Artifact does not have large power obviously. Fig. 3.8 shows the spectrogram in four states of time-frequency analysis, which based on short-term Fourier transform. Therefore, spectral analysis is combined to entropy analysis to improve the performance of epileptic seizure detection [17, 19-21]. In this study, three frequency bands (0-4Hz, 7-11Hz, and 15-18Hz) are selected as spectral indexes.

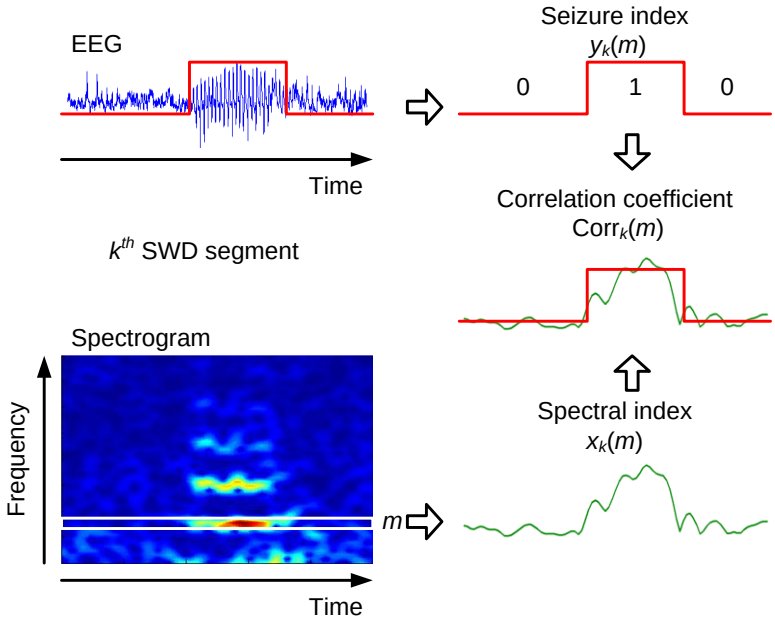


Fig. 3.7 Seizure event and a particular frequency band combine to identify effective spectral indexes for seizure detection

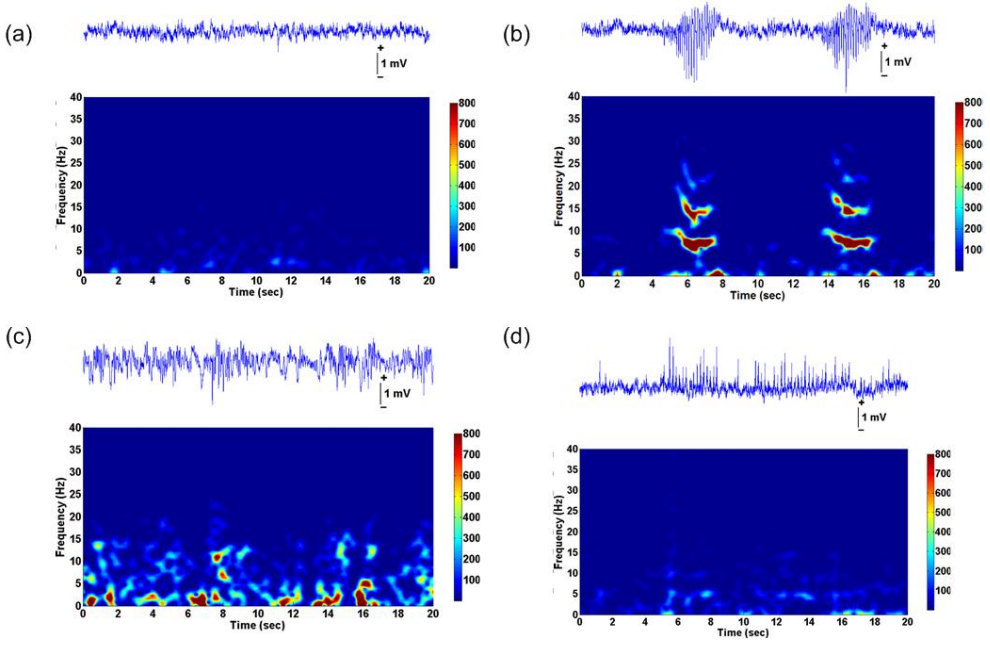


Fig. 3.8 The five behavioral states of time-frequency analysis (a) AW, (b) absence seizures, (d) SWS, and (e) Artifact

3.1.3 Linear Classifier

Because the objects' seizure conditions are different, the algorithm must have flexible model by EEG of subjects. The linear least squares (LLS) method is used to find a best fitting linear model. LLS is the problem in approximately solving an over-determined system of linear equations, where the best approximation is defined as that which minimizes the sum of squared differences between the data and the desired data. Besides, the method could reduce the computational cost for implementation, because the model output is only the weighted sum of the input.

At first, consider an over-determined system (3.16), m is number of data pair for training in n coefficients. y_i is the output of LLS. β_j is the weight parameter. This can be written in matrix form as (3.17). The residual is the difference between the observed value and the value calculated by the model (3.18). Next, S is minimized when its gradient vector is zero. The elements of the gradient vector are the partial derivatives of S with respect to the parameters (3.19). We obtain the normal equations (3.20), and the $\hat{\beta}$ is minimizes S. Finally, the normal equations are written in matrix notation as (3.21). Thus, the solution of the normal equations yields the vector of $\hat{\beta}$ the optimal parameter values (3.22).

$$y_i = \sum_{j=1}^{n} X_{ij}\beta_j \ , \quad i = 1, 2, ..., m \tag{3.16}$$

$$y = X\beta$$
$$y = \begin{bmatrix} y_1 \\ y_2 \\ \vdots \\ y_m \end{bmatrix} \quad X = \begin{bmatrix} X_{11} & X_{12} & \cdots & X_{1n} \\ X_{21} & X_{22} & \cdots & X_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ X_{m1} & X_{m1} & \cdots & X_{mn} \end{bmatrix} \quad \beta = \begin{bmatrix} \beta_1 \\ \beta_2 \\ \vdots \\ \beta_n \end{bmatrix} \tag{3.17}$$

$$S(\beta) = \sum_{i=1}^{m} \left(y_i - \sum_{j=1}^{n} X_{ij}\beta_j \right)^2 \tag{3.18}$$

$$\frac{\partial S}{\partial \beta_i} = -2\sum_{i=1}^{m} X_{ij}(y_i - \sum_{k=1}^{n} X_{ij}\beta_k) = 0 \ , \ j = 1,2,...,n \tag{3.19}$$

$$\sum_{i=1}^{m} X_{ij} y_j = \sum_{i=1}^{m}\sum_{k=1}^{m} X_{ij} X_{ik} \hat{\beta}_k \tag{3.20}$$

$$(X^T X)\hat{\beta} = X^T y \tag{3.21}$$

$$\hat{\beta} = (X^T X)^{-1} X^T y \tag{3.22}$$

In this study, LLS is used in two stages. The first stage is off-line training. Three feature indexes, which are CM, band 1 (7-1Hz), and band 2 (17-22Hz), are input into classifier to verify seizure occurrences. The target output values are zero for non-seizure windows, and one for seizure windows. Therefore, the equation (3.17) can be written to (3.23), and used (3.22) to find the best model β for each subject. The second stage is on-line computing. Optimal parameters ware determined at last stage, which compute with three features at on-line seizure detector (3.24).

$$y = \begin{bmatrix} 0(non-seizure) \\ 1(seizure) \\ \vdots \\ 1 \ or \ 0 \end{bmatrix} \qquad \beta = \begin{bmatrix} \beta_{CM} \\ \beta_{Band1} \\ \beta_{Band2} \\ \beta_{Const} \end{bmatrix}$$
$$X = \begin{bmatrix} CM_1 & Band1_1 & Band2_1 & 1 \\ CM_2 & Band1_2 & Band2_2 & 1 \\ \vdots & \vdots & \ddots & \vdots \\ CM_m & Band1_m & Band2_m & 1 \end{bmatrix} \tag{3.23}$$

$$LLS_{on-line} = CM \times \beta_{CM} + Band1 \times \beta_{Band1} + Band2 \times \beta_{Band2} + \beta_{Const} \tag{3.24}$$

3.1.4 Adaptive Threshold

Because the entropy analysis of SWS state usually leads to false detection easily, but the state has large power less than 4Hz, an adaptive threshold is proposed to decrease the false alarms. Adaptive threshold is to switch the threshold of LLS between SWS state and SWD state. According to Fig. 3.6 and Fig. 3.8, although the SWS signals resemble with SWD signals at time-domain, the frequency power of SWS has an oscillation within delta frequency range (0.5-4Hz). Therefore, the frequency band 0 is used to determine the SWS state. If band 0 has higher energy than a threshold of sleep (Th_{sws}), the threshold of LLS is switched to a higher value to avoid the false alarms. Equation (3.25) shows an adaptive threshold. At training stage, average band0 of the sleep EEG minus or plus standard deviation of the sleep EEG (3.26). Th_{wake} is decided by the LLS result of seizure event, and Th_{sleep} is based on the LLS result of seizure event in SWS state, (3.27). Fig. 3.9 shows the false detection without adaptive threshold.

$$LLS_{Th} = \begin{cases} Th_{wake}, & otherwise \quad ,Wake\ state \\ Th_{sleep}, & if\ Band0 > Th_{sws}, Sleep\ state \end{cases} \tag{3.25}$$

$$Th_{sws} = mean\left[Band0\right] \pm Std\left[Band0\right] \tag{3.26}$$

$$Th_{sleep} = mean\left[LLS_{sws}\right] \pm Std\left[LLS_{sws}\right] \tag{3.27}$$

In addition, the window constraint is set to avoid the influence of EEG signals. If the LLS classifier output is larger than the LLS_{Th} in consecutive three 32-sample, the seizure event is detected. Therefore, the delay time of seizure detection is 0.48s least (5ms×32×3), but it is the tolerable delay time to restrain seizure. Fig. 3.10 shows the seizure detection algorithm include three features and Band 0.

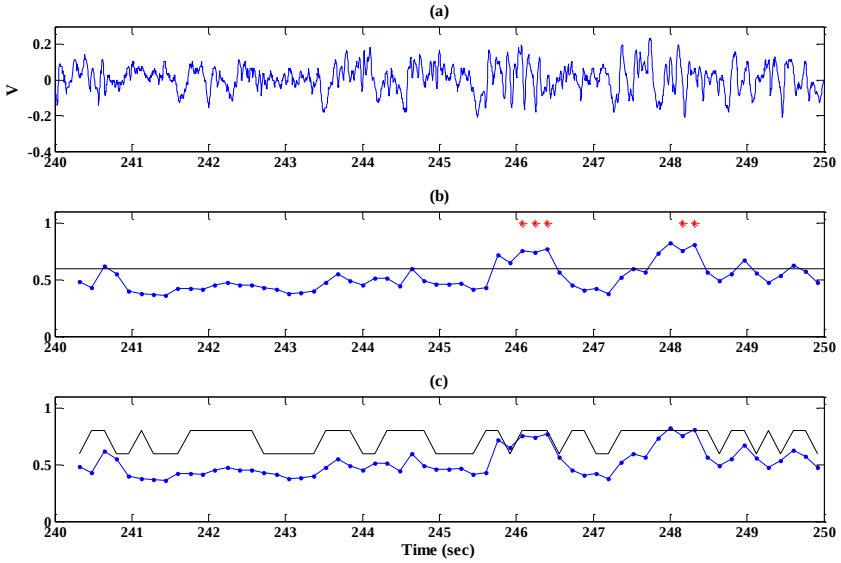


Fig. 3.9 Non-adaptive and adaptive threshold of SWS:

(a) EEG signal, (b) without adaptive threshold, (c) adaptive threshold

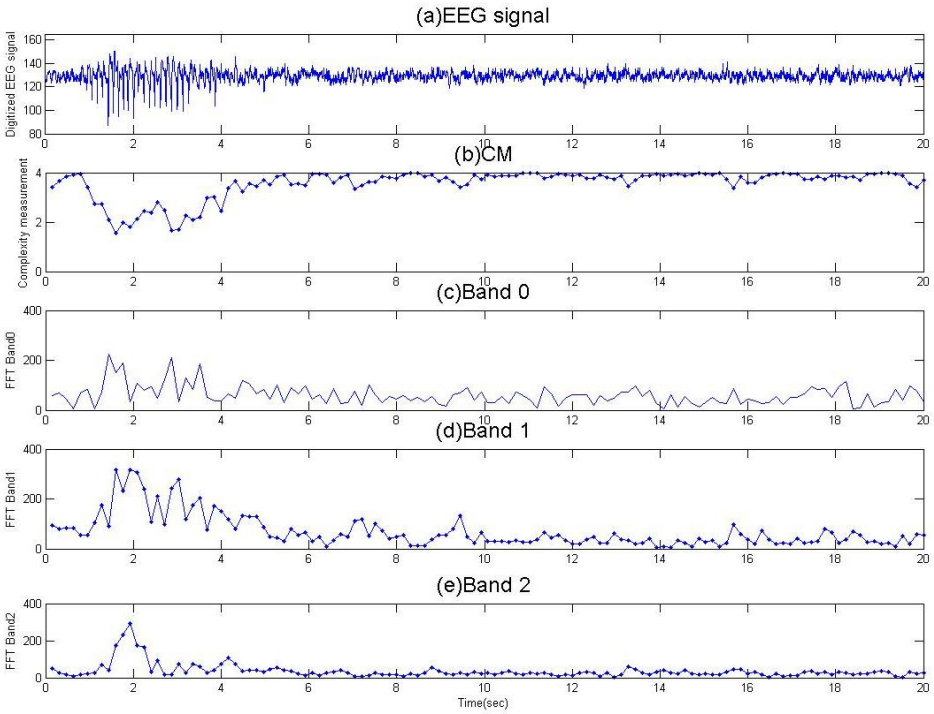


Fig. 3.10 (a) EEG signals, (b) CM, (c) Band 0, (d) Band 1, (e) Band 2

3.2 Experimental Flow

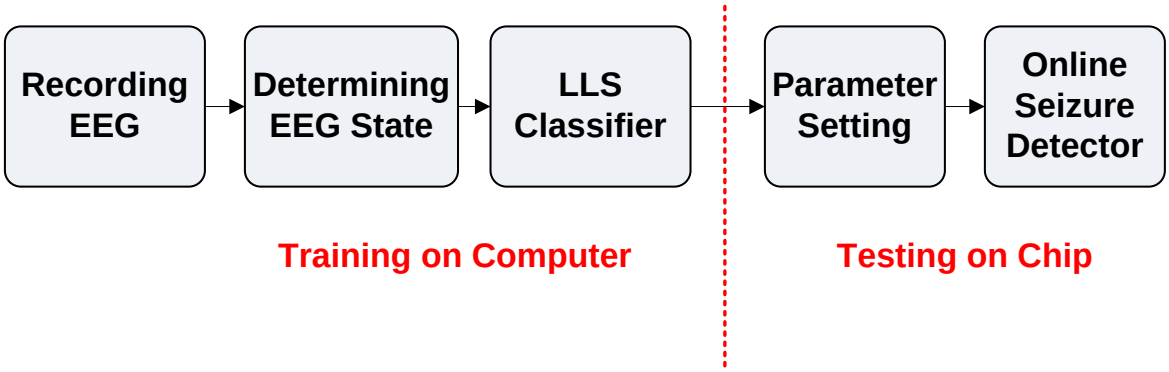


Fig. 3.11 Experimental flow

To make sure the seizure detector is useful, experimental flow is divided into five stages, in Fig. 3.11. The first stage is recording EEG data. In this study, the long-term recording is five hours and twenty-four hours of continuous EEG data without electrical stimulation. The second stage is determining EEG state. After recording the EEG data, the EEG data is distinguished behavioral states by experts. The spontaneous events include AW, SWD, SWS, and artifact. The first stage and the second stage are both executed at the Institutional Animal Care and Use Committee of the National Cheng Kung University.

Next stage is LLS classifier. For finding the best model of objects, LLS classifier is utilized by Matlab. In the train step, seizure and non-seizure segments with equivalent length are selected for LLS model, and the ratio of non-seizure segments including WK, SWS, and artifice are 1:1:1, as shown in Fig. 3.12. Two hours of three feature indexes are trained to get a pair of parameters, and those parameters is testing five hours of EEG data. When the detection accuracy is above 92%, the parameters are applied to on-line stage, else data is trained repeatedly.

Then, the optimal parameters are downloaded to MCESD chip by I^2C interface at initial stage. I^2C interface will be described in next section. Finally, the online seizure detector is developed to seizure detection.

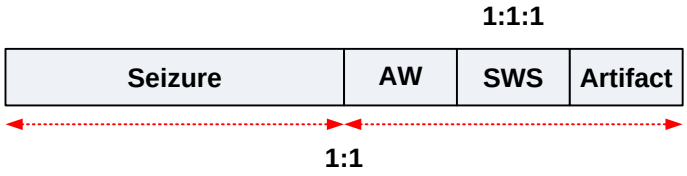


Fig. 3.12 The weight of training segments

Chapter 4 Design and Implementation

According to Fig. 2.2, the block diagram shows four blocks in MCESD chip, including 2-channel seizure detection, I^2C register bank, data receiver, and clock generator. The first part, 2-channel seizure detector implements the seizure detection algorithm. The computing rate is 3.2 kHz. MCESD needs to generate the control signal and clock for different ADC circuits, so the second part and third part are clock generator and data receiver, which synchronized ADC signal and generated the clock for seizure detector (3.2kHz). The last part is I^2C register bank, which loads the parameters to system at initial, and saves the value of seizure detector for verifier function.

4.1 2-channel Seizure Detector

In Chapter 3, the seizure detection algorithm is described in detail, and it is implemented in the 2-channel seizure detector. Fig. 4.1 shows the block diagram of seizure detector. The 2-channel seizure detector is composed of two 1-channel seizure detector, and a switch determining that data are delivered to channel 0 or channel 1, as shown in Fig. 4.1(a).

Fig. 4.1 (b) illustrates the blocks of 1-channel seizure detector which correspond with the algorithm. Clk means clock of detector. In this block, the computing clock is 3.2kHz (200Hz ×16). Because the sampling clock is 200Hz, and the entropy window size is 16-point, 3.2kHz is the lowest clock of computing to handle the data in real-time. Rst is 1 in normal state, and all registers are cleared when Rst is 0. Clken is clock enable; the system is paused when Clken is set to 0. The block detail will be introduced in following section. Clk, Clken, and Rst all connect to each block.

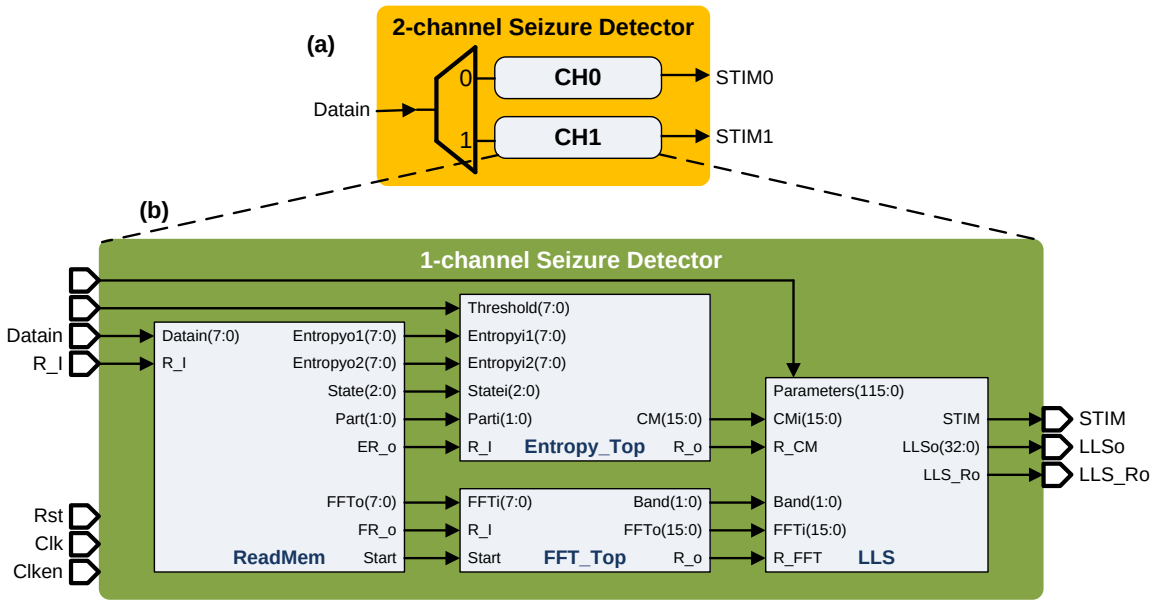


Fig. 4.1 Block diagram of seizure detector (a) 2-channel detector (b) one channel detector

4.1.1 Read Memory

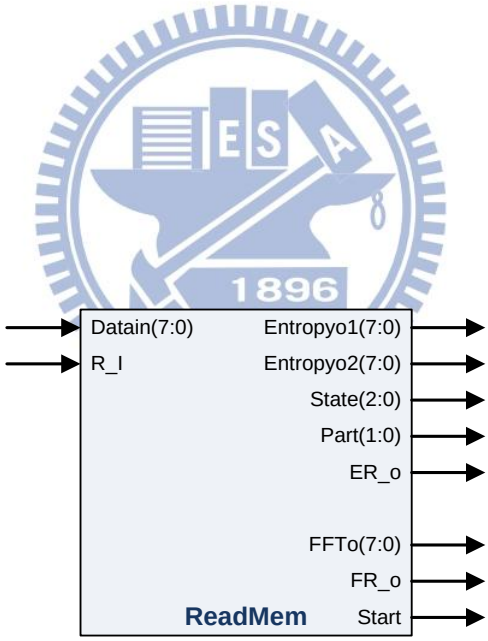


Fig. 4.2 Interface of read memory

This block receives EEG data and saves data, than it feds data to entropy block and FFT block. Read memory contains a 2-port 128×8 memory. An input port of memory writes the Datain into memory when the R_I is set to 1, and the other is unused. One output port is for entropy, and the other is for FFT. Entropyo1 is output which correspond to $u(i) - u(j)$; Entropyo2 corresponds to $u(i+1) - u(j+1)$. Because the 64-point is divided into four segments,

Part is display the segments, and State is show the order of the 16-point data. On the other hand, there are three signals for FFT block. Start is used to wake up the FFT block to be ready for received FFT data, and FFTo will deliver continuous data to next block. ER_o and FR_o are set to 1, which means the data are ready to be delivered. All inputs and outputs are shown in Fig. 4.2.

4.1.2 Entropy Extractor

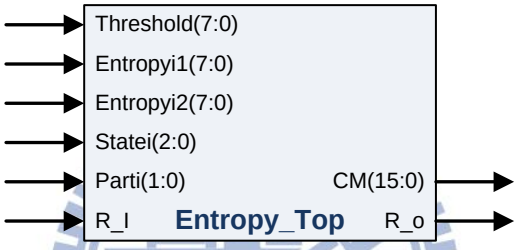


Fig. 4.3 Interface of entropy extractor

Fig. 4.3 shows the input and output of entropy extractor, and the threshold is equal to "r". The inputs (Entropyi, Statei, Parti, and R_I) are connected with outputs of ReadMem (Entropyo, State, Part, and ER_o), and CM is output. Fig. 4.4 and Fig. 4.5 illustrate the hardware implementation of entropy extractor. First, $u(i)–u(j)$ and $u(i+1)–u(j+1)$ are implemented with two subtracters, and decision bits (ω_j) are decided that the values compare with r and $2r$. Next, accumulators save the decision bits, and $S^1_{t+1} = S^{11}_{t} + S^{12}_{t+1} + S^{11}_{t+1}$, S^2_{t+1} is also. The detail of S^{11} and S^{12} is shown in Fig. 4.6. A divider computes S^2/S^1. The complexity measurement is sun of CM^p. The output of CM is 4-bit unsigned integer and 12-bit fractional.

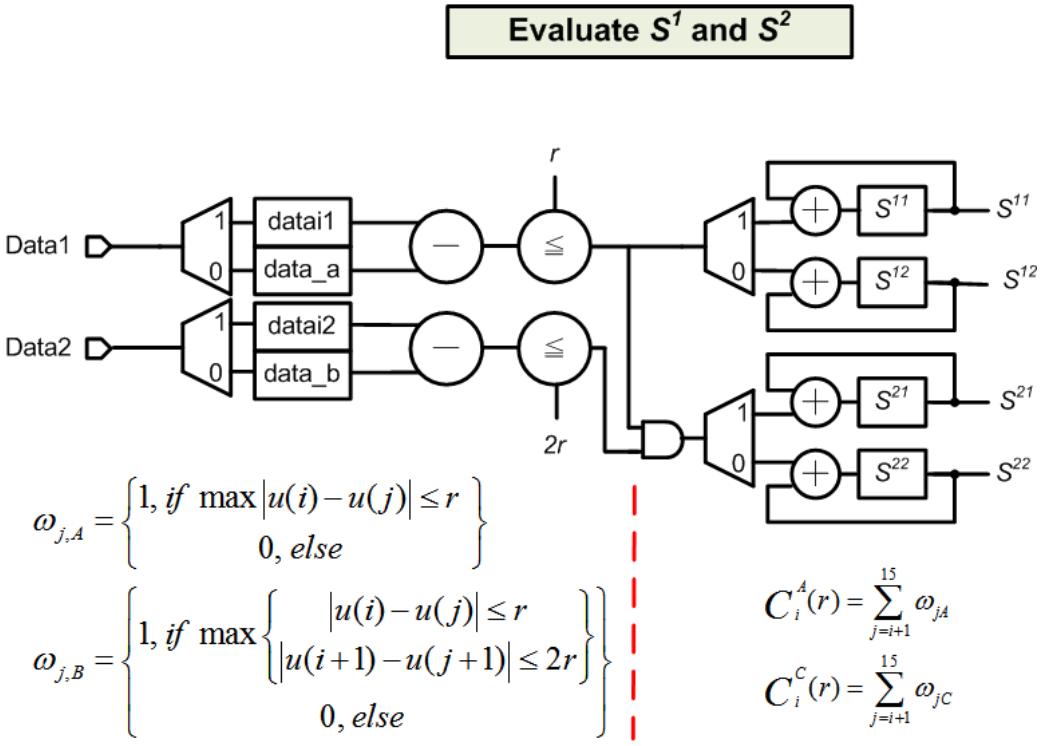


Fig. 4.4 The implementation of evaluate S^1 and S^2

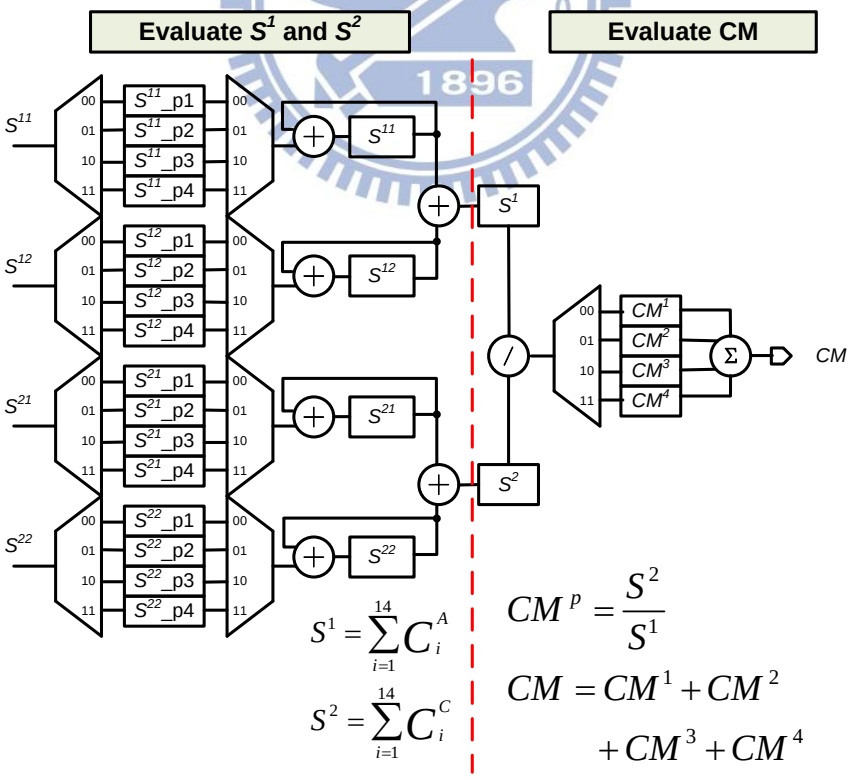


Fig. 4.5 The implementation of evaluate CM

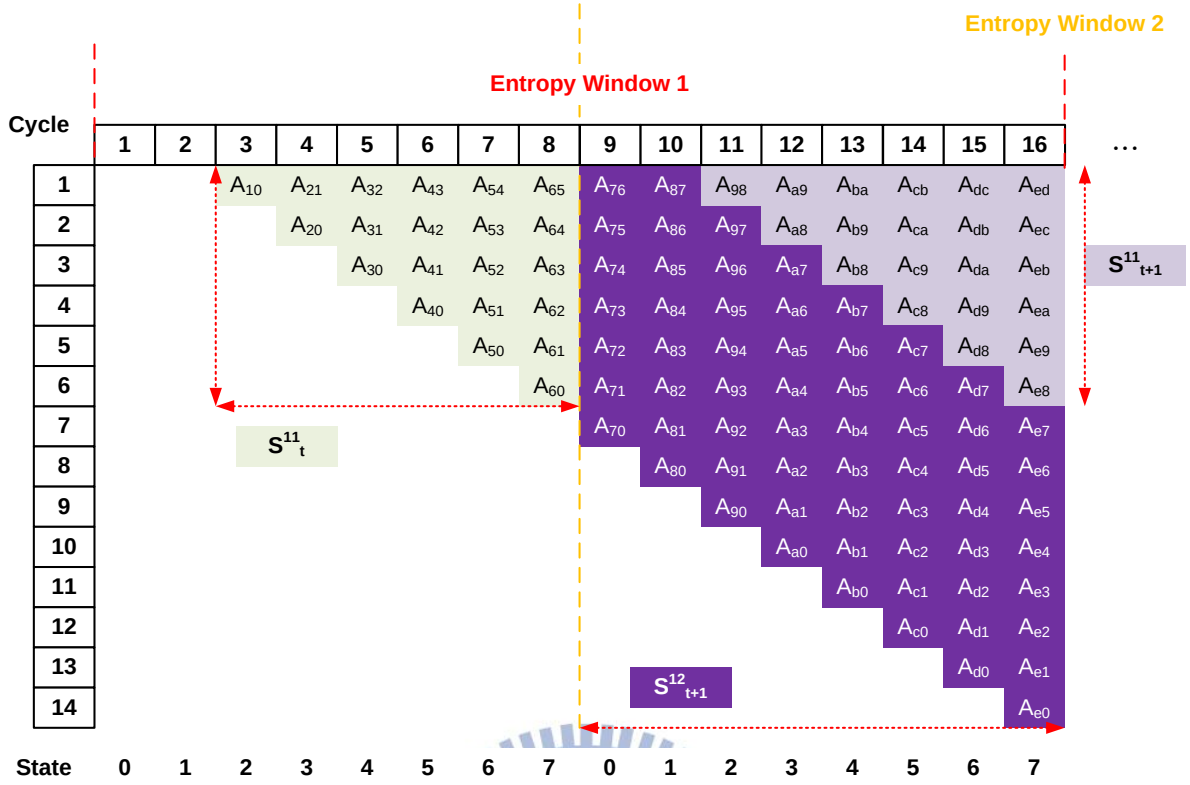


Fig. 4.6 The relation between S^{11}, S^{12}, and State

4.1.3 64-point FFT

The overview of the 64-point FFT is shown in Fig. 4.7, including FFT main function and FFT_process. FFT is a core from SoC Design Lab, Instituation of Communication Engineering, NCTU, which supports 9-bit signed complex input and 15-bit signed complex output. Four modes are selected, because the FFT core could compute 8, 16, 32, and 64 size of FFT. In this study, the size of FFT are always 64 points, so mode is fix value. When the IN_VALID is high, the data will deliver the data to do the computation. Due to EEG signals is real numbers, imaginary numbers are zero.

The architecture of 64-point radix-2/4/8 FFT is shown in Fig. 4.8, and the main advantage of radix-2/4/8 is reducing number of complex multipliers. Fig. 4.9 shows the signal

flow of 64-point radix-2/4/8 FFT [22]. Fixed multiplicand like ±j and $\sqrt{2/2(1\pm j)}$ are used to replace complex multipliers. Therefore, the algorithm apply to length of 8n FFT and decrease the computational cost. Consider to the SQNR is achieve 30dB, so the bit of output increase 2 bits at radix-2 butterfly stages. Then, the least three stage fix the bit number to retrench area. Twiddle factor is used one bit integer and sixteen bits fractional.

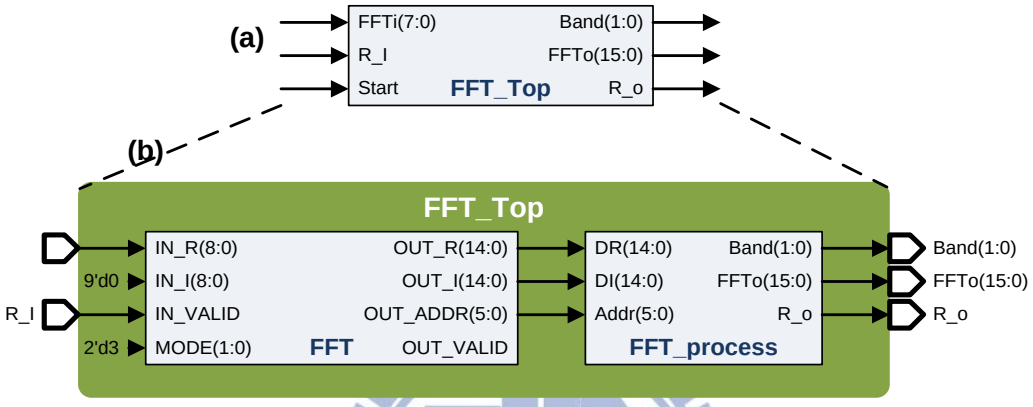


Fig. 4.7 (a) interface of 64-point FFT (b) block diagram of FFT

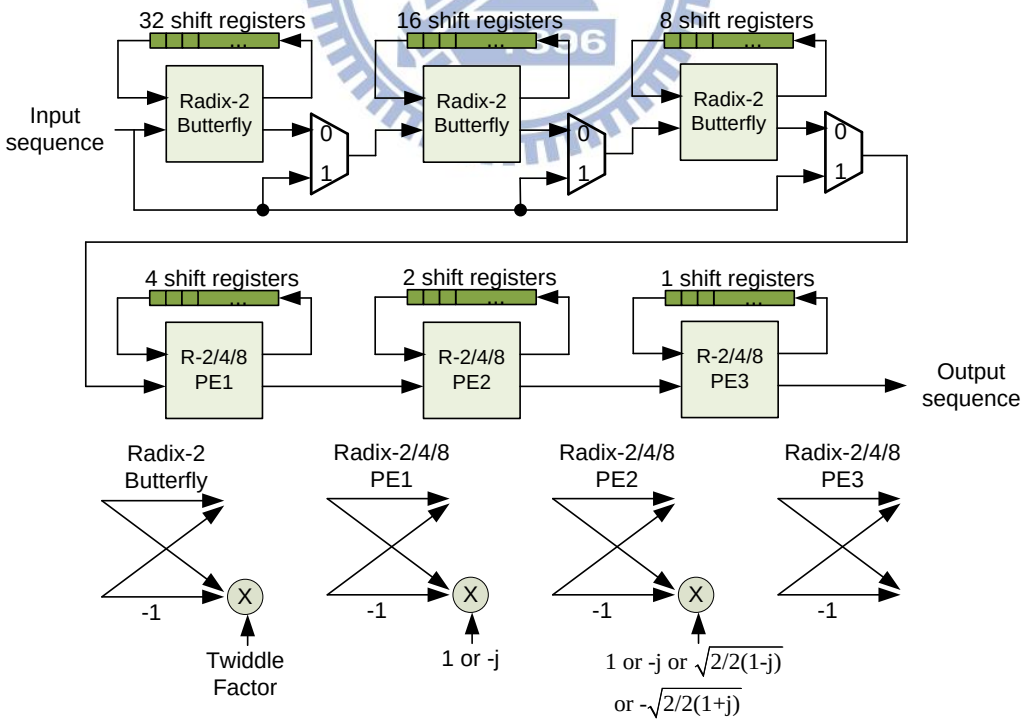


Fig. 4.8 The architecture of 64-point radix-2/4/8 FFT

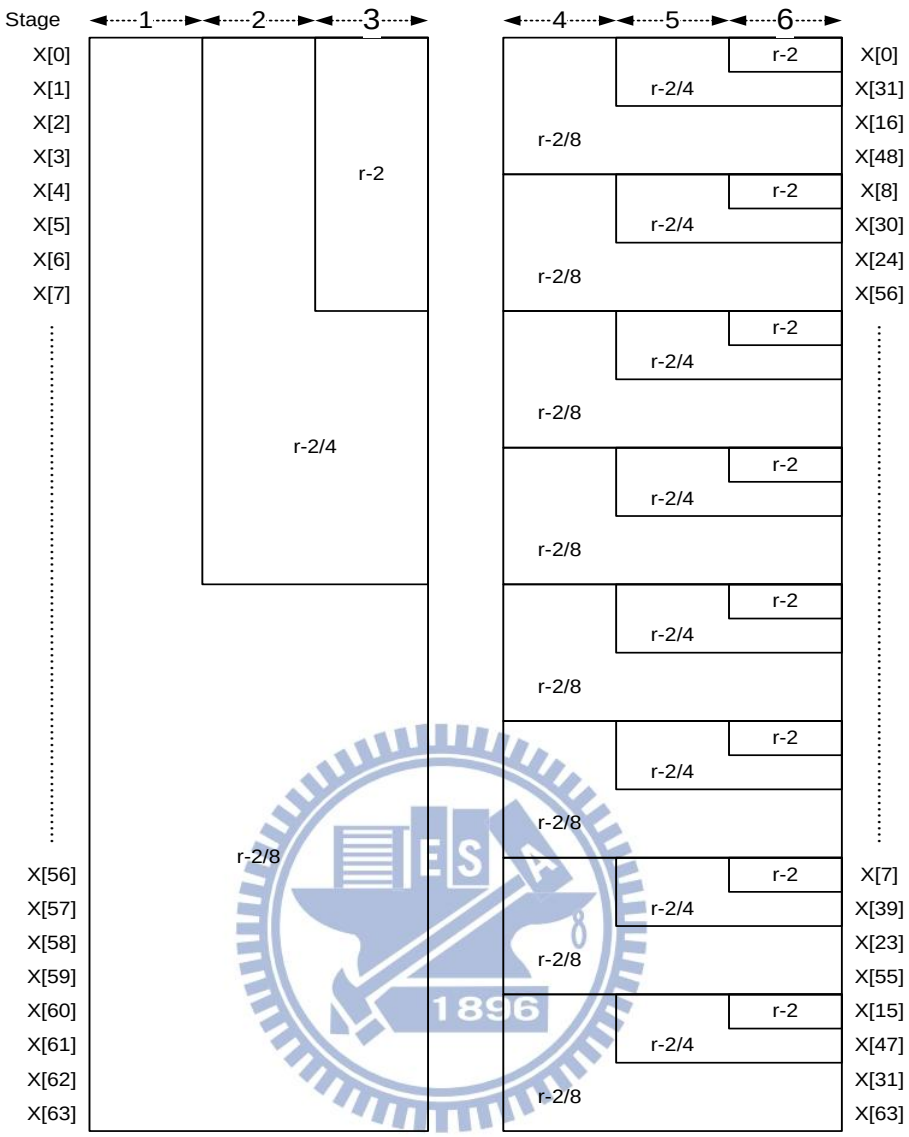


Fig. 4.9 Signal flow of 64-point radix-2/4/8 FFT

FFT_process calculates power of specific frequency bands by spontaneous brain waves. FFT output is DR+DIj, and the power of FFT is means $|FFTo| = \sqrt{DR^2 + DI^2}$. The input of DR and DI are 16 bits signed integer, and ADDR display the frequency of FFT. When the address is 0, 4, and 7 which correspond with Band0, Band1, and Band2, the FFTo are computed. The output of FFTo is 9-bit unsigned integer and 7-bit fractional. Fig. 4.10 illustrates the hardware implementation of FFT_process.

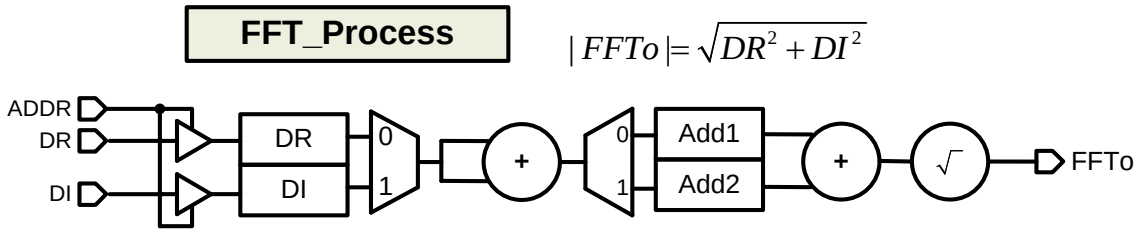


Fig. 4.10 The implementation of FFT_process

4.1.4 LLS Classifier

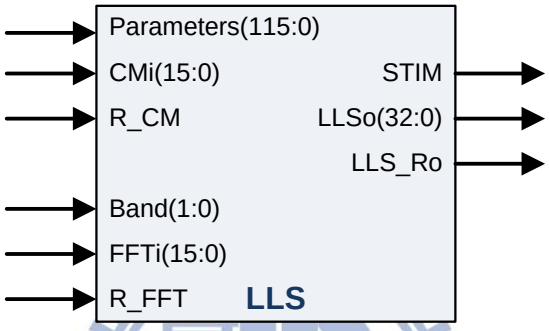


Fig. 4.11 Interface of LLS Classifier

Fig. 4.11 shows the input and output ports of LLS block. Input acquire data by last stage, and the parameters are input from I^2C register bank, which detail is on next section. LLSo will save into I^2C register bank to check the values. In the training phase, the large matrix are used to training on computer, but the hardware implementation on chip just need three features from previous blocks and the parameters in registers. Band 0 is a condition to switch the LLS_{Th}. Fig. 4.12 illustrate the hardware implementation of LLS. First, LLS out is calculated by the input. Next, the seizure detection counter is incremented when a seizure occur; otherwise, the counter is zero. If the counter reaches *DET_WINDOW*, STIM, a flag of stimulation is set, and the flag keep *DET_STIM*×0.16 seconds. The optimal parameters' detail is shown in Table 4.1, and the default values of *DET_WINDOW* and *DET_STIM* are 3.

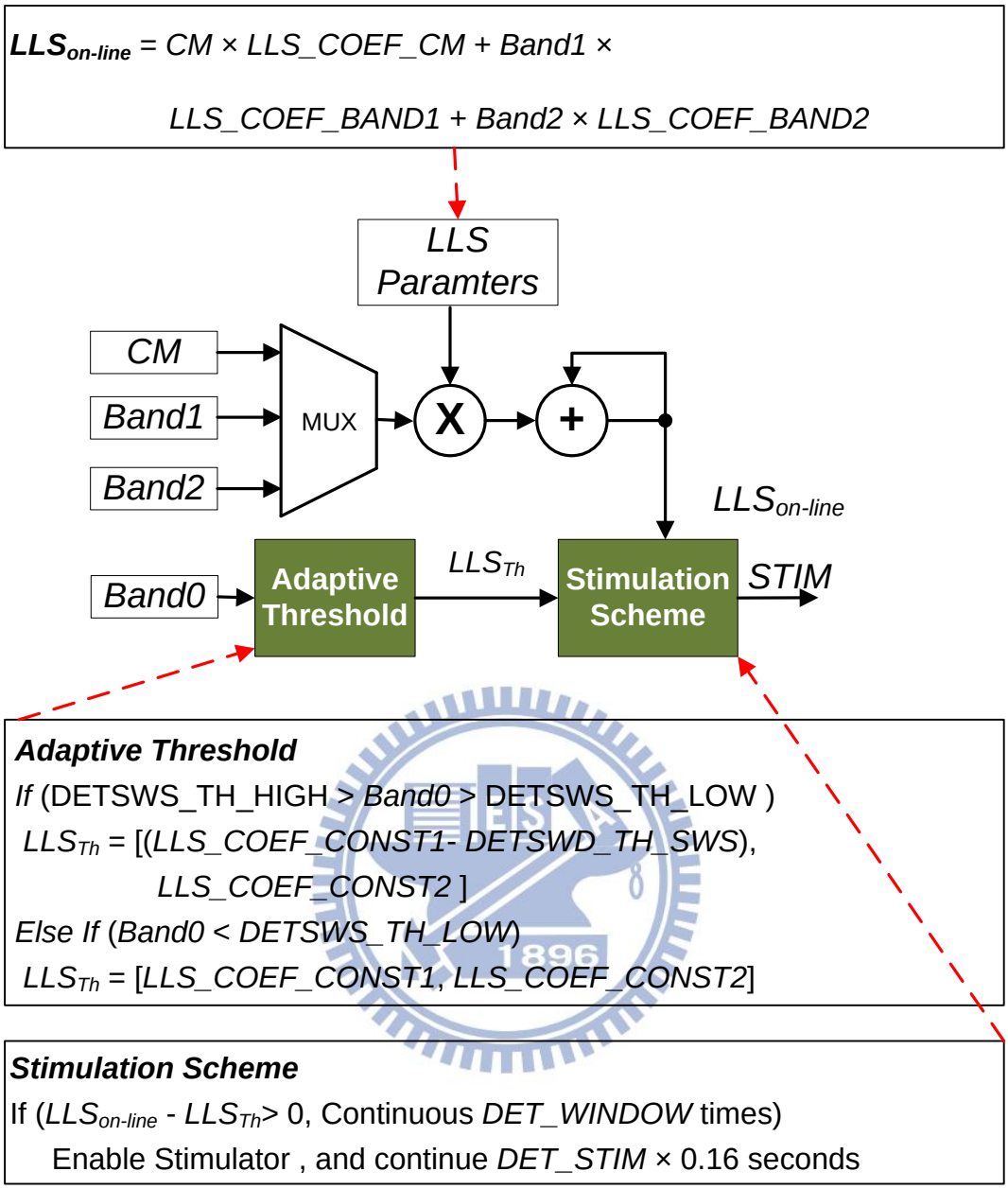


Fig. 4.12 The implementation of LLS Classifier

Table 4.1 Specifics of features and parameters

Name	Integer (bits)	Fractional (bits)	Default Value
Features			
CM	4	12	N/A
Band0	9	7	N/A
Band1	9	7	N/A
Band2	9	7	N/A
Parameters			
THRESHOLD(r)	8	0	5
LLS_COEF_CM	12	4	N/A
LLS_COEF_BAND1	7	9	N/A
LLS_COEF_BAND2	7	9	N/A
LLS_COEF_CONST1	16	0	N/A
LLS_COEF_CONST2	0	16	N/A
DETSWD_TH_SWS	16	0	N/A
DETSWS_TH_LOW	9	7	N/A
DETSWS_TH_HIGH	9	7	N/A
DET_WINDOW	4	0	3
DET_STIM	4	0	3
LLS_{Th}	16	16	N/A
$LLS_{on\text{-}line}$	17	16	N/A

4.2 I^2C Register Bank

Because there are many parameters is need to set in MCESD chip at initial, I^2C interface is used to save numbers of pad. Inter-integrated circuit register bank (I^2C register bank) is an interface integrated with 8-bit×N register bank for sub-circuit configuration, and 8-bit×M inputs for sub-circuits status readout [23]. The block diagrams are shown in Fig. 4.13. Control pins of target sub-circuits can be reduced to only 3 pins (sda, saddr and scl), because clk and reset are integrated with 2-channel seizure detector. The pins are controlled by I^2C master, as shown in Fig. 4.14.

Scl is a clock signal, and being utilized for synchronizing I^{2}C data input. Sdain, Sdaout, Oe are the data and direction control pin for bidirectional pad. Saddr is used for I^{2}C slave identification. In this case, only less significant bit is connected out, and the other two pins are set to zero. ctrl0 – ctrlN are 8-bit×64 registers and they connect to 2-channel seizure detector for configuration purpose. readin0 – readingM are 8-bit×64 reading registers for 2-channel seizure detector status readout purpose. Table 4.2 shows the relation between seizure detector and I^{2}C register bank.

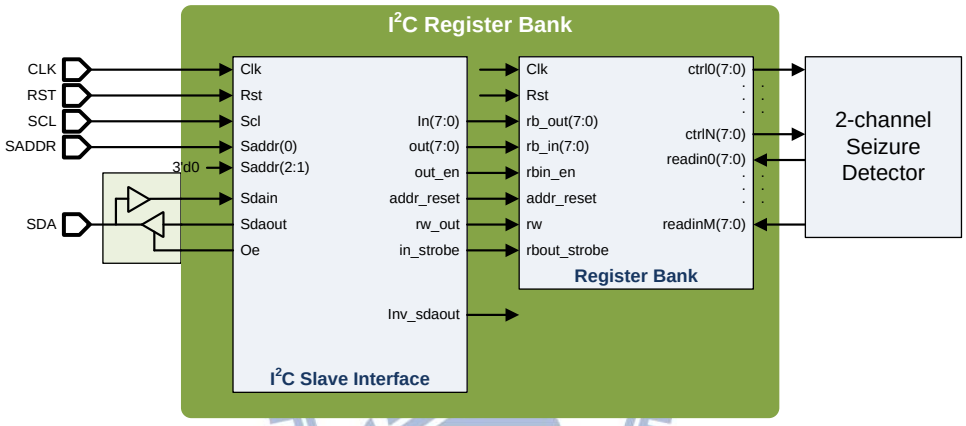


Fig. 4.13 The block diagrams of the I^{2}C register bank

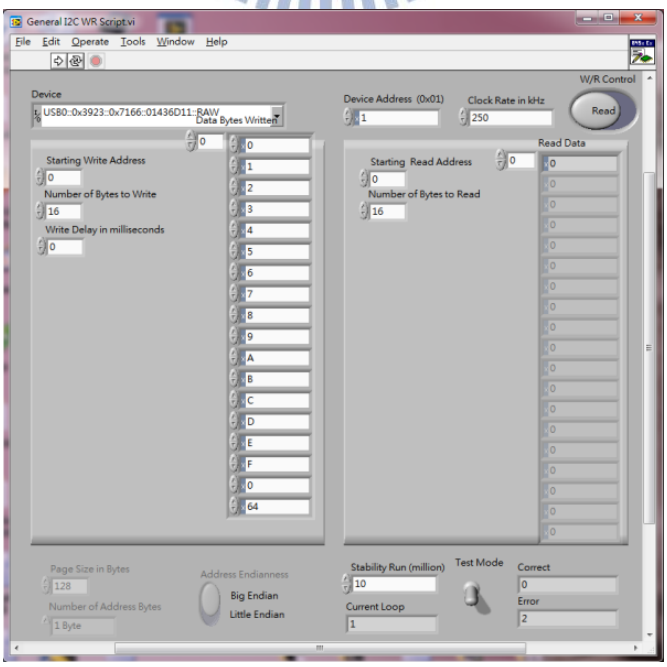


Fig. 4.14 The interface of I^{2}C master in computer

Table 4.2 Parameters of MCESD correspond with I^2C register bank

Parameters	I^2C Register (8bits)	Parameters	I^2C Register (8bits)
Clock Generator		CH1_LLS_COEF_CONST1	ctrl29,ctrl28
DIV_3200	ctrl1[3:0],ctrl0	CH1_LLS_COEF_CONST2	ctrl31,ctrl30
DIV_500K	ctrl1[7:4]	CH1_DETSWD_TH_SWS	ctrl33,ctrl32
MODE	ctrl2[1:0]	CH1_DETSWS_TH_LOW	ctrl35,ctrl34
CH0 Parameters		CH1_DETSWS_TH_HIGH	ctrl37,ctrl36
CH0_THRESHOLD(r)	ctrl3	CH1_DET_WINDOW	ctrl38[3:0]
CH0_LLS_COEF_CM	ctrl5,ctrl4	CH1_DET_STIM	ctrl38[7:4]
CH0_LLS_COEF_BAND1	ctrl7,ctrl6	***CH0 Results***	
CH0_LLS_COEF_BAND2	ctrl9,ctrl8	CH0_FFTo	readin1,readin0
CH0_LLS_COEF_CONST1	ctrl11,ctrl10	CH0_CMo	readin3,readin2
CH0_LLS_COEF_CONST2	ctrl13,ctrl12	CH0_LLSo	readin8[0],readin7 ,readin6,readin5 ,readin4
CH0_DETSWD_TH_SWS	ctrl15,ctrl14		
CH0_DETSWS_TH_LOW	ctrl17,ctrl16		
CH0_DETSWS_TH_HIGH	ctrl19,ctrl18	CH0_R_LLS	readin8[1]
CH0_DET_WINDOW	ctrl20[3:0]	***CH1 Results***	
CH0_DET_STIM	ctrl20[7:4]	CH1_FFTo	readin10,readin9
CH1 Parameters		CH1_CMo	readin12,readin11
CH1_THRESHOLD(r)	ctrl21	CH1_LLSo	readin17[0],readin16 readin15,readin14, readin13
CH1_LLS_COEF_CM	ctrl23,ctrl22		
CH1_LLS_COEF_BAND1	ctrl25,ctrl24		
CH1_LLS_COEF_BAND2	ctrl27,ctrl26	CH1_R_LLS	readin17[1]

4.3 Clock Generator and Data Receiver

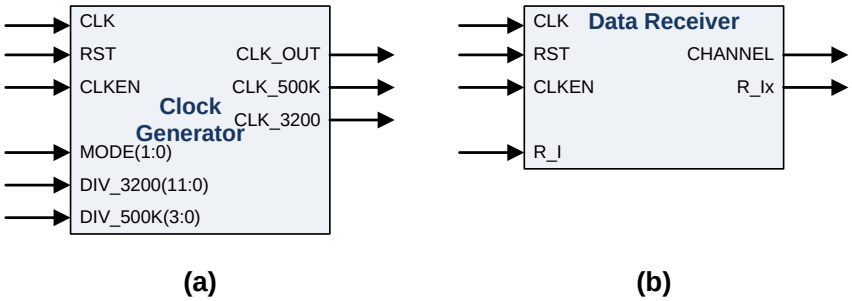


Fig. 4.15 Interface of (a) CLK_GEN and (b) DATA_REQ

MCESD needs to generate the control signal and clock for different ADC circuits, so the third part is clock generator and data receiver, which synchronized ADC signal and generated the clock for seizure detector (3.2kHz). The interface of clock generator and data receiver are shown in Fig. 4.15. MCESD clock can input 10MHz to 1MHz. The clock is equal CLK_OUT, and CLK also divide to CLK_3200, CLK_500K. CLK_3200 is always 3.2KHz whatever the clock is input frequency. Meanwhile, CLK_500K can be regulate by DIV_500K, so the frequency of CLK_500K is frequency/N where N is between 2 to 32. MODE control CLK_OUT, and CLK_500K, in Table 4.3. In Fig. 4.15 (b), the R_I is a 400Hz clock, and it synchronize ADC datain.

Table 4.3 The active of CLK_OUT and CLK_500K with MODE

MODE	CLK_OUT	CLK_500K
00	Frequency	Frequency/N
01	Frequency	1
10	1	Frequency/N
11	1	1

4.4 The Timing of MCESD

Fig. 4.16 presents the timing diagram of the epileptic seizure detector based on the above setup. At initial, the I^2C register bank is utilize to load the parameters of MCESD. The frequency of MCESD can regulate the computing cycles, and cycles of I^2C setting is 19 at 1MHz. The epileptic seizure detector operated at 3.2kHz. When previous 32 sampled data is retrieved, the computation of entropy, FFT, and LLS classification is finished in current 32-sample cycle and then determine the seizure event. As shown in the figure, each time when 32-sampled data have been collected, about 23.5 ms latency is required to determine the seizure occurrence. Again, a seizure detection need 32-sample cycle×3+23.5ms latency at 3.2kHz clock rate at least. The timing diagram shows the seizure detection algorithm can be executed continuously in the implemented epileptic seizure detector.

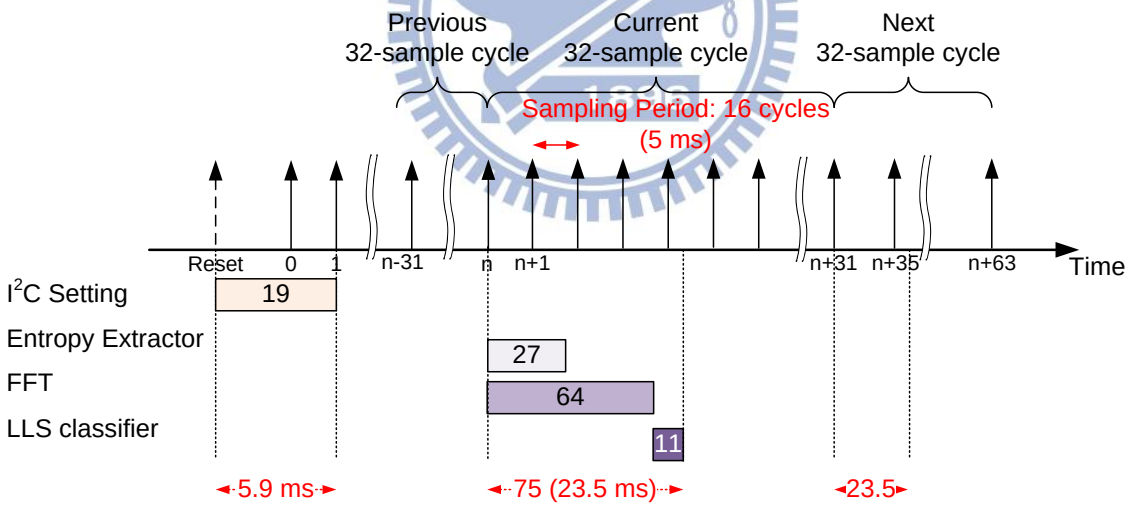


Fig. 4.16 The timing diagram of the MCESD

Chapter 5 Result and Comparison

After system level design and considerations is dealt with Chapter 4, this chapter describes the implementation flow at first. Next, behavior simulation is displayed. Then, the functional verification in FPGA and implementation results are described. The test setup and experimental results are illustrated. Finally, the seizure detection accuracy and comparison with related researches are discussed in the end of this chapter.

5.1 Design and Implementation Flow

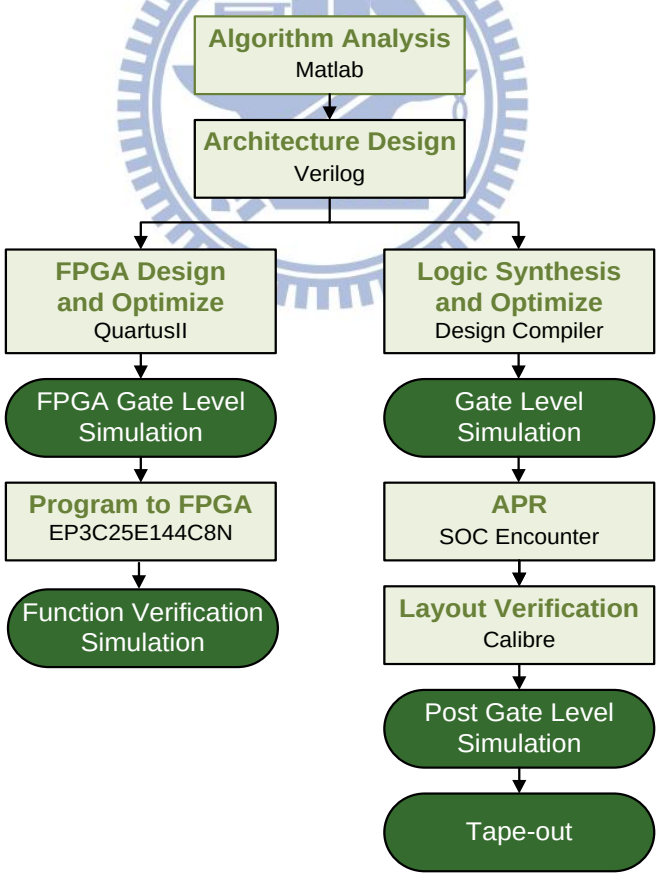


Fig. 5.1 The design and implementation flow

Fig. 5.1 show the design and implementation flow. At first, the seizure detection algorithm is analyzed by Matlab. the architecture design is implemented to RTL. Then the behavior code is turned into logic gates by two tools, FPGA and Design Compiler. On the one hand, after the gate level simulation of FPGA is correct, it program in FPGA to test the function. On the other hand, the gate level code is changed to physical layout by SOC Encounter, and Caliber verify the layout. Finally, the MCESD is tape-out in CIC.

5.2 Behavior Simulation

The simulation environment is based on TSMC 0.18 libraries and simulated after logic synthesizing. The clock cycle is set up with 1μs. In other words it is simulated in 1MHz. The simulation has four steps. The first one is to write coefficients into MCESD. As shows in Fig. 5.2, IO_I2C_SDA is controlled by I^2C master, and total numbers of coefficients written in the first step are thirty-nine. They will be fed into the ctrl0-ctrl38.

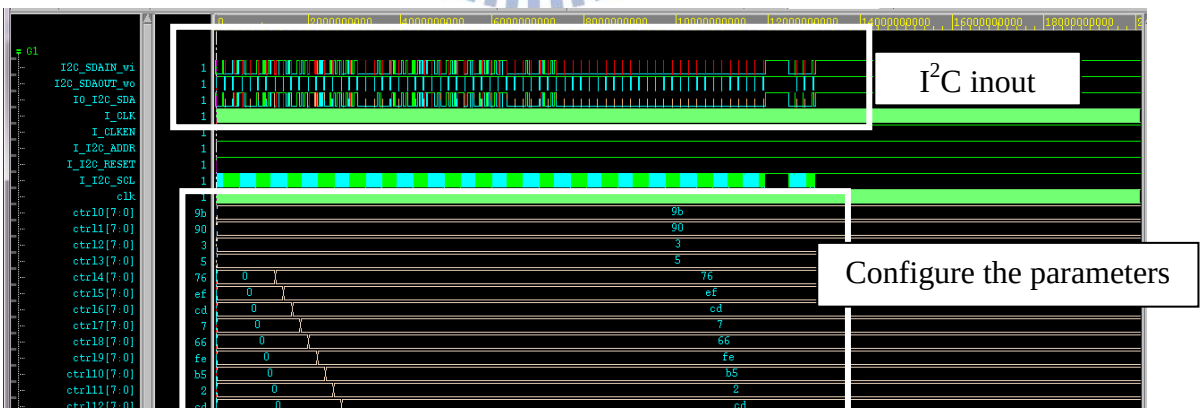


Fig. 5.2 Waveform of I^2C register bank initial MCES

The second step is read-write memory. R_I is a sampling clock which is 400Hz for two channel. The sampling data is written when R_I is high, and the entropy data is read after writing data. After 64-point sampling data are collected, FFT data are read to FFT blocks, as

shown in Fig. 5.3. Next, Fig. 5.4 shows the result of CM and FFT Bands. Three features and one condition(Band0) are loaded into LLS classifier when R_o is high. Finally, after all data are ready, a pulse is sent to start computing LLS classifier. The computing cycles spends 12cycles at 3.2kHz, as shown in Fig. 5.5. When successive EEG data are received, the second step to fourth step are executed repeatedly

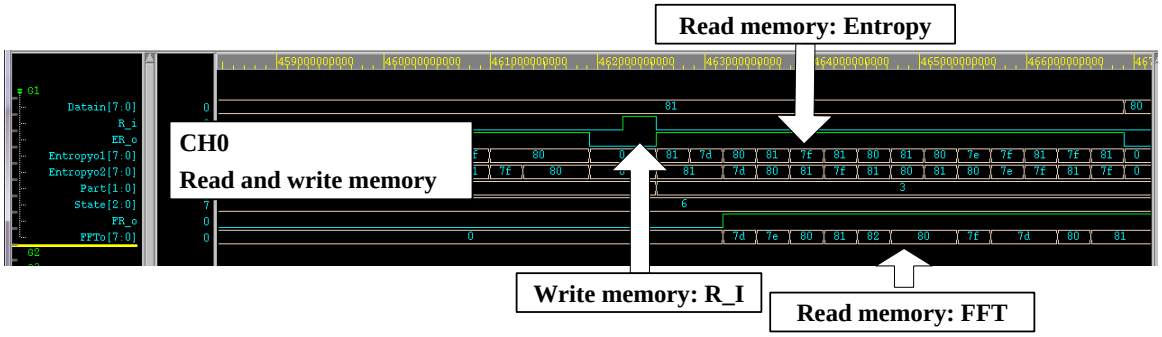


Fig. 5.3 Waveform of read and write memory

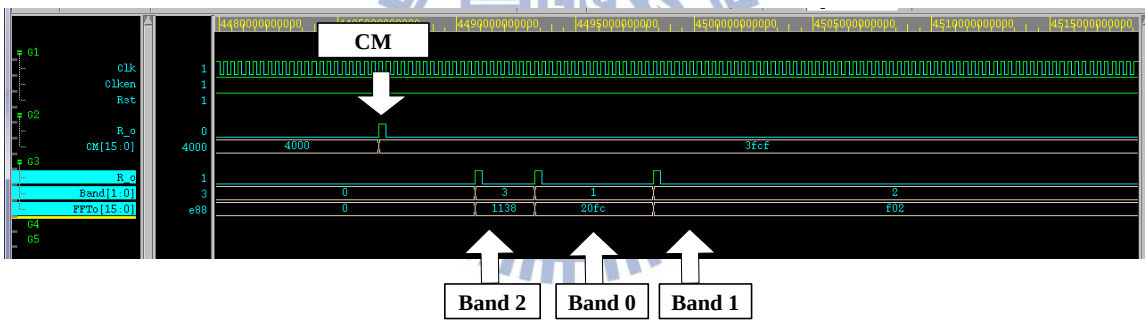


Fig. 5.4 Waveform of CM and FFT bands

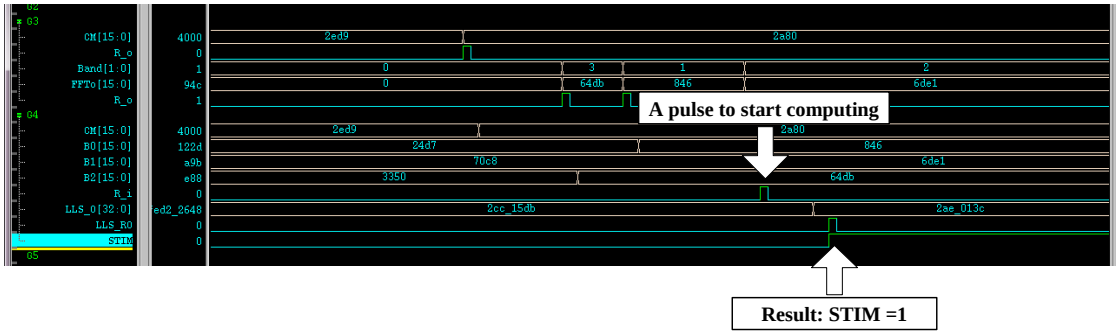


Fig. 5.5 Waveform of LLS classifier and STIM

5.3 Functional Verification in FPGA

1-channel seizure detector is verified function by FPGA for optimized architecture. The integration result of closed-loop seizure control system is shown in Fig. 5.6(a). The AFE and stimulator board is shown in Fig. 5.6(b)[24, 25]. The die of pre-amplifier and ADC is bonded on the board. The epileptic seizure detector board shown in Fig. 5.6(c) consists of an Altera Cyclone III FPGA. The utilized FPGA, EP3C25E144C8N [26], is manufactured with 65nm CMOS technology; it provides 25K logic elements and 600K memory bits.

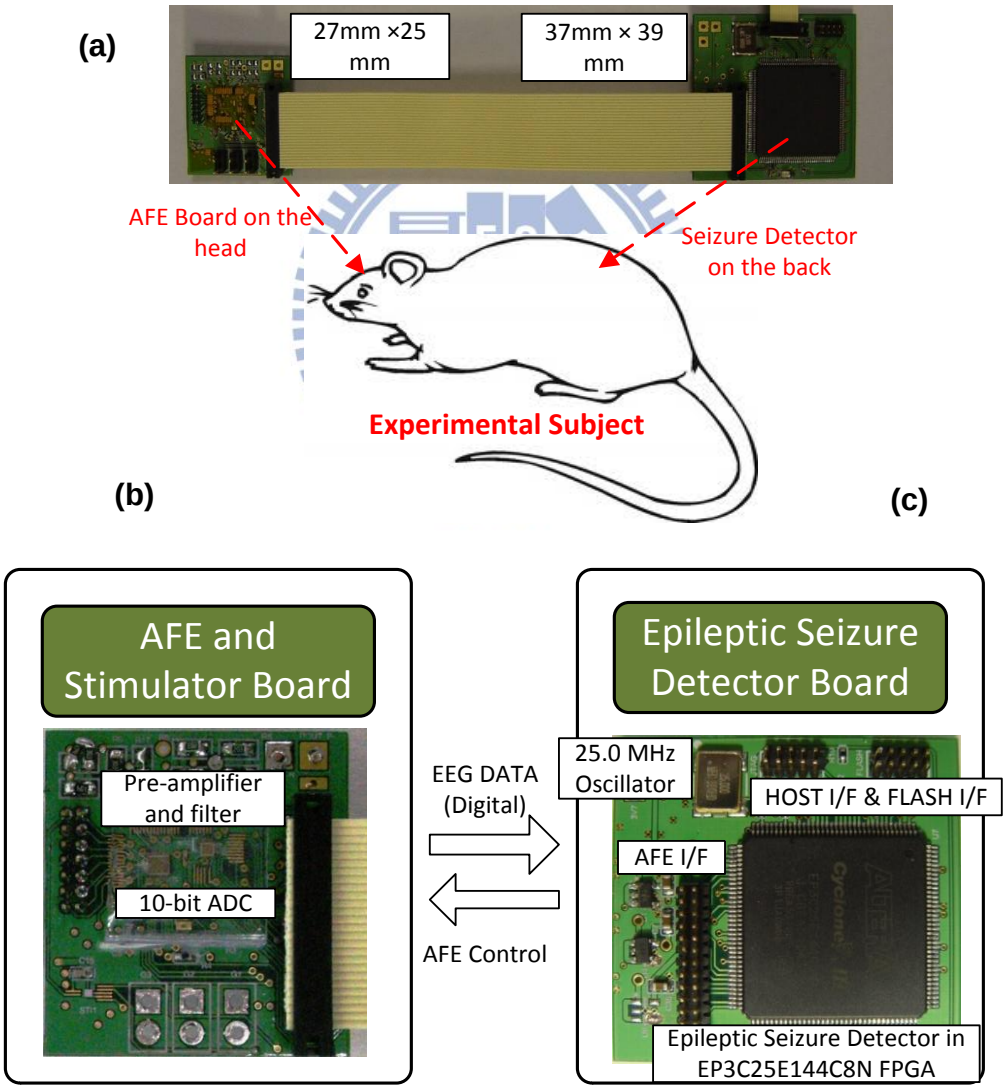


Fig. 5.6 Closed-loop seizure control system on FPGA

The total logic Elements and memory bits are 3160/1828. The total dynamic, static and I/O power consumption are evaluated about 0.01mW, 82.34mW, and 16.86mW, respectively. The summary of circuit characteristics of this work is listed in Table I. The static power of proposed design can be eliminated in future ASIC implementation was caused by leakage currents of idle transistors in FPGA.

Table 5.1 Summary of 1-channel Epileptic Seizure Detector on FPGA

	Read memory	**64-point entropy extractor**	**64-point FFT core**	**LLS classifier**
Operating frequency (kHz)	3.2			
1-channel execution time (cycles)	N/A	27	64	11
Logic elements usage	196	846	1868	360
Memory (bits)	1024	31	0	0
Dynamic / static / I/O power dissipation (mW)	0.01 / 82.34 / 16.86			
Total power dissipation (mW)	99.2			

5.4 Implementation Results of MCESD

The summary of implementation results are listed in Table 5.2. It is through 0.18μm process of TSMC and cell based design kit of CIC. The operating frequency of post-layout simulation is 10MHz. The MCESD chip size is about 1760×1760μm^2, and the core size is 1230×1230μm^2. The gate count of the chip is 169905. It must be noted that the 2-channel are implemented in MCESD. There for, we need two 128×8 dual port static RAM (SRAM) which are generated by memory compiler with Artisan library.

The power dissipation of total chip is 581.2μW at 10MHz, and 114.1μW at 1MHz. The details of power consumption are listed in Table 5.3. The ratio of IO pads is 17%. Meanwhile the ratio of core power is 83%, including I^{2}C register bank, clock generator, data receiver, and

2-channel seizure detector. In 1- channel seizure detector, FFT accounts for 12.4%, which is the most distribution rate. Therefore, decreasing the power consumption of FFT is feature work.

Table 5.2 Summary of Implementation Results

Specification	
Technology	TSMC 0.18μm CMOS
Package	SB32
Die Size	1760x1760μm^2
Core Size	1230x1230μm^2
Utilization	91%
Gate Count	169,905
On-Chip Memory	128x8 Dual port SRAM × 2 2048bits
Clock Rate	CHIP:1MHz-10MHz Epileptic seizure detector: 3.2kHz
Execution Time	23.5ms
Power Consumption	114.1μW@ 1MHz,1.8V
Input Pads/Output Pads/ Inout Pads/Power Pads	14/5/ 1/12

The die photo is shown in Fig. 5.7(a), and two memories are in right location. The floor plan of MCESD is in Fig. 5.7(b). MCESD are fourteen input pads, five output pads, and one inout pad for I2C_SDA. The first pad is VSSC0, and the least pad is I2C_ADDR according to counterclockwise order. There are three pairs of power pads for core and three pairs of power pads for chip pads. The package of MCESD is SB32. The detail of pads is listed as Table 5.4.

Table 5.3 Detail of power consumption

	Internal Power	Switch Power	Leakage Power	Total Power	Ratio %
IO Pads (μW)	7.322	11.600	0.200	19.000	17 %
I^2C Register Bank (μW)	0.001	21.100	2.430	33.500	29.4 %
Clock Generator (μW)	0.125	1.180	0.095	1.400	1.2 %
Data Receiver (μW)	0.001	0.002	0.028	0.031	0.0 %
2-channel Seizure Detector (μW)	0.505	2.530	56.800	59.900	52.4 %
1-channel Seizure Detector					
Read Memory (μW)	0.006	0.459	10.500	10.900	9.6 %
Entropy (μW)	0.008	0.104	2.510	2.620	2.3%
FFT (μW)	0.237	0.637	13.200	14.100	12.4%
LLS (μW)	0.001	0.051	2.150	2.200	1.9%

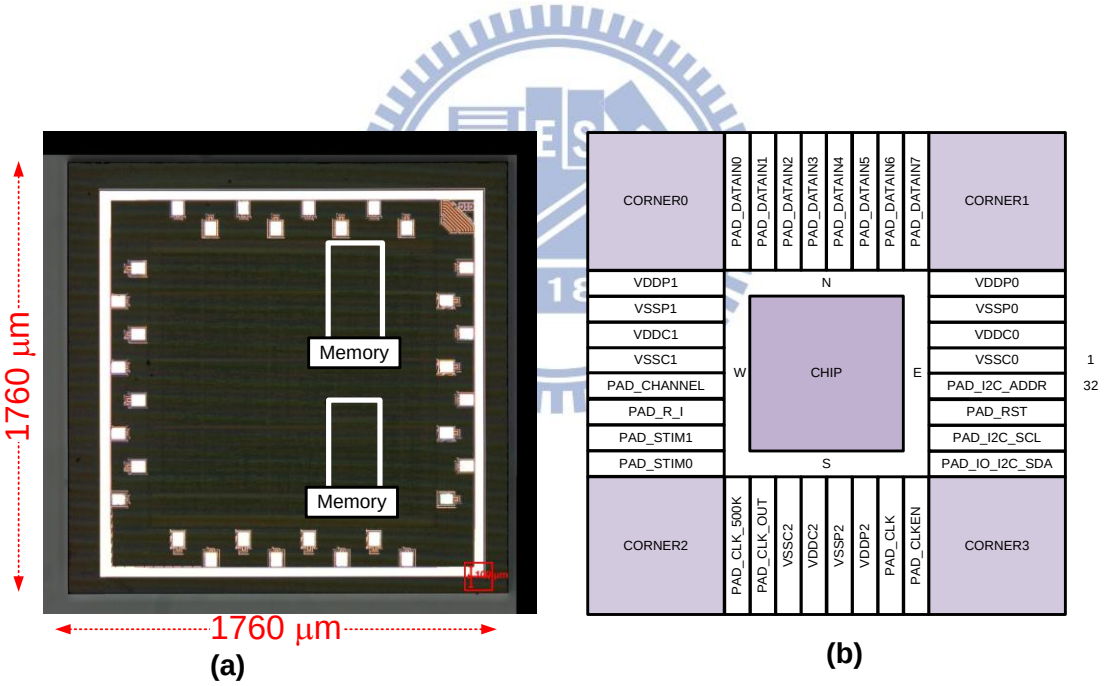
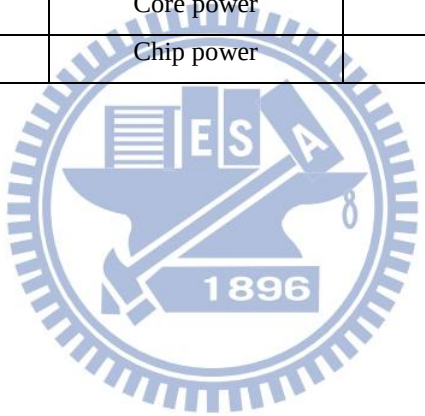


Fig. 5.7 (a) Die photo of the MCESD, (b) floor plan of MCESD

Table 5.4 The pin assignment of the chip with SB32 package

PAD Name	PAD Type	Description
PAD_DATAIN0-7	Input	EEG signals
PAD_RST	Input	Reset system
PAD_CLKEN	Input	Clock enable
PAD_CLK	Input	Clock
PAD_CHANNEL	Output	Display the channel
PAD_R_I	Output	Clock of sampling data
PAD_STIM0-1	Output	A flag for stimulus
PAD_CLK_10M	Output	Clock output
PAD_CLK_500K	Output	Divided clock
PAD_I2C_ADDR	Input	Address of I^2C
PAD_I2C_SCL	Input	Clock of sampling data for I^2C
PAD_I2C_SDA	Inout put	Data input for I^2C
VDDC, VSSC	Core power	1.8V VDD
VDDP, VSSP	Chip power	3.3V VDD



5.5 Testing Environment Setup

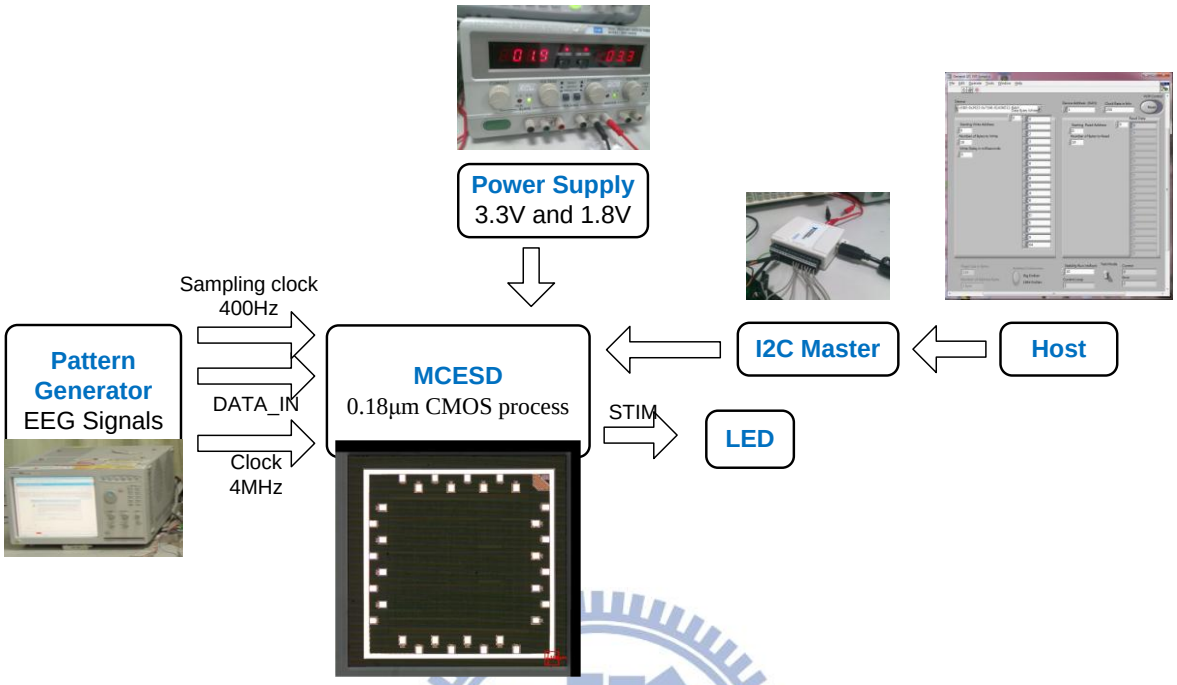


Fig. 5.8 Testing environment

Fig. 5.8 is the testing environment of the MCESD chip. The input signal, 4MHz clock, and 400Hz sampling clock are generated by the Agilent Technologies 16720A pattern generator. The power supply for the chip core is 1.8V, and the supply voltage of MCESD pads and components on PCB board is 3.3V. Initial set is configured by I^2C master, and the values of FFT, CM, and LLS classifier are checked through I^2C master read. Meanwhile, the LEDs light when STIM is set to logic 1. Fig. 5.9 show the PCB photo. The power consumption of measurement is listed in Table 5.5. The frequencies include 1MHz (lowest), 4MHz, and 10MHz (highest), and the 4MHz clock is for the CoB system in the future. The core power and pad power are the worst case, which enable CLK_OUT and CLK_500K.

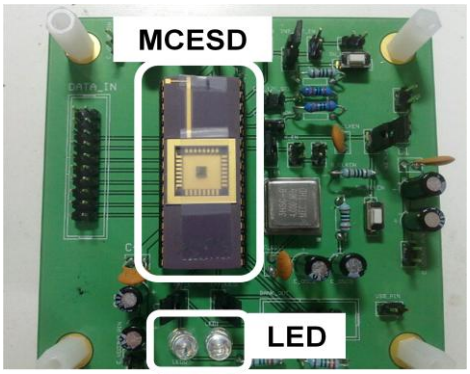


Fig. 5.9 Photo of MCESD PCB

Table 5.5 The power consumption of measurement

Frequency	Core Power (1.8V)	Pad Power (3.3V)	Total Power
1MHz	56.88μW	146.19μW	203.07μW
4MHz	217.82μW	569.58μW	787.40μW
10MHz	540.54μW	1408.11μW	1948.65μW

5.6 Seizure Detection Accuracy

Functionality of seizure detector is assessed by continuous EEG signals acquired from four Long-Evans rats. Four rats are subjected to absence seizures. The optimal parameters of train model are used to detect seizures for each rat. The training procedure is described in previous section 3.2. The length of data is 5 hours for subject #1 and #2, and the other two rats are measure under 24 hours execution time. Table 5.6 shows the SWD duration and the detail of SWD.

Table 5.6 The detail of SWD duration and two frequency bands

Subjects	TOTAL DURATION (H:M:S)	SWD Duration (h:m:s)	SWD Min (s)	SWD Mean (s)	SWD Max (s)	Band1 (Hz)	Band2 (Hz)
#1	05:00:00	00:27:34	0.50	5.09	25.69	7-10	15-18
#2	05:00:00	00:16:42	0.50	3.96	42.75	7-10	15-18
#3	24:00:00	00:49:34	0.19	4.94	43.32	7-10	15-18
#4	24:00:00	01:11:36	0.20	6.17	49.51	7-10	15-18

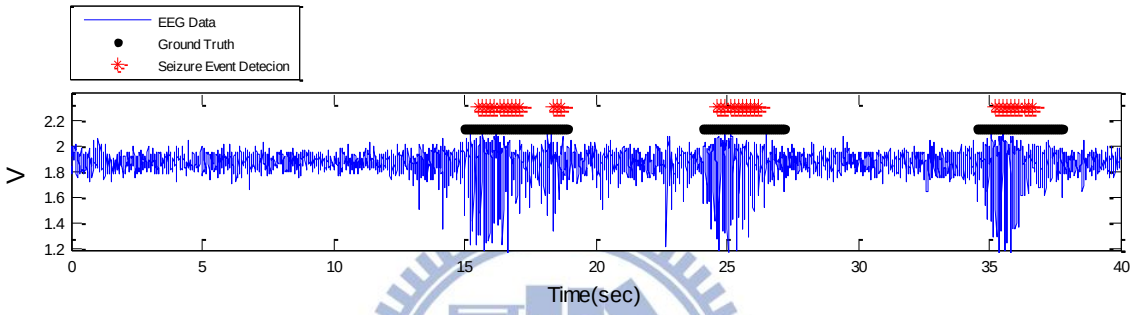


Fig. 5.10 Detected seizure events by MCESD

The function of the seizure detector is demonstrated in Fig. 5.10. Three seizures' events are detected by our proposed detector during a 40-s period on rats #1. The ground truth is distinguished by specialist in neurology. Fig. 5.11 shows the different statuses of simulation. Three seizures' times occur as shown in Fig. 5.11(a), which determined that a seizure event is detected; Fig. 5.11(b) shows that a miss event occurs at 39984s; Fig. 5.11(c) shows that a false detection event occurs between 758s and 759s. Accuracy and false stimulation of seizure detection algorithm as shown in Table 5.7. Detection accuracy equation show in (27). As shown in the table, the seizure detection accuracy average 94.59%, which was consistency with previous works (92%-99%) [13]. The delay would be slightly varied among subjects due to variation of EEG complexity and spectrum energy. Therefore, the seizure detection delay is about 0.63 s-0.8 s, which is the tolerable delay time to restrain seizure.

$$Detection\ Accuracy\ (\%) = \frac{Detected\ SWD}{SWD} \times 100\% \tag{5.1}$$

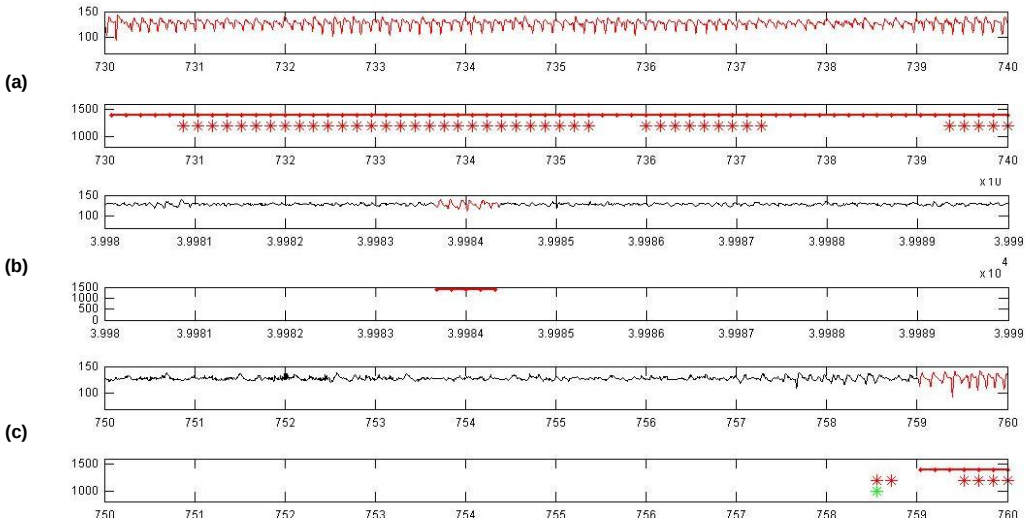


Fig. 5.11 The different type of simulation

Table 5.7 Performance of the seizure detection algorithm

Subjects		SWD	Detected SWD	Accuracy (%)	False Detection	Hardware Detection delay (s)
#1	Awake	294	285	97.23	28	0.80
	Sleep	31	31		25	
#2	Awake	223	214	96.83	28	0.68
	Sleep	30	30		4	
#3	Awake & Sleep	600	553	92.17	218	0.63
#4	Awake & Sleep	684	630	92.11	193	0.69

5.7 Comparison with Related Researches

The previous 8051 implementation[13] operated at 32MHz and consumed 117.66mW. The MCESD operated at 3.2 kHz clock rate and consumed 114.1μW, and it is capable of detecting the seizure signals in 0.63s to 0.8s with 94.59% accuracy. The power consumption of our low-noise pre-amplifier, filter, [24] (468μW), and 10-bit analog-to-digital converter [25] (80μW) was evaluated about 548μW. The totally power of our system is 662.1μW, which decrease 99.5% power compared with previous system. The evaluation results show that the overall system powered by a 3.7-V, 1100-mAh battery can be operated for 7.5 months. The detail of two system are listed in Table 5.8.

Table 5.8 Comparison of seizure detector

	Previous 8051 implementation + signal conditioning board [13]	**This work +AFE[24], [25]**
Operating Frequency(Hz)	32M	3.2k
Single-channel processing time (ms)	24.1	23.5
Area	N/A	$1230 \times 1230 \mu m^2$ (Core) / $1760 \times 1760 \mu m^2$ (Chip)
Power Consumption of Analog Part	N/A	548μW
Power Consumption of Digital Part	N/A	114.1μW
Total Power Consumption	117.66mW	662μW
Power Normalization	100 %	0.5 %
Battery Life (3.7V, 1100 mAh)	28 hours	7.5 months

Chapter 6 Conclusion and Future Work

In this thesis, a 2-channel epileptic seizure detector for closed-loop seizure control is proposed to achieve low power consumption and continuous real-time processing. Both detection accuracy and functions has been verified by continuous EEG signals recorded from freely moving Long-Evans rats. The implementation results have been showed the proposed epileptic seizure detector in FPGA reduced 15% power consumption while achieve the same real-time performance compared with previous prototype, and it is reduced above 99% in MCESD. An implantable continuous time seizure detector is implemented, and the detection accuracy is 94.6%. Recently, the chip on board include MCESD, AFE, and stimulator is proceeding, as shown in Fig. 6.1. In the future, the MCESD chip will integrate with analog front-end circuitries and stimulators to a real-time closed-loop seizure detector to build up a system-on-a-chip solution.

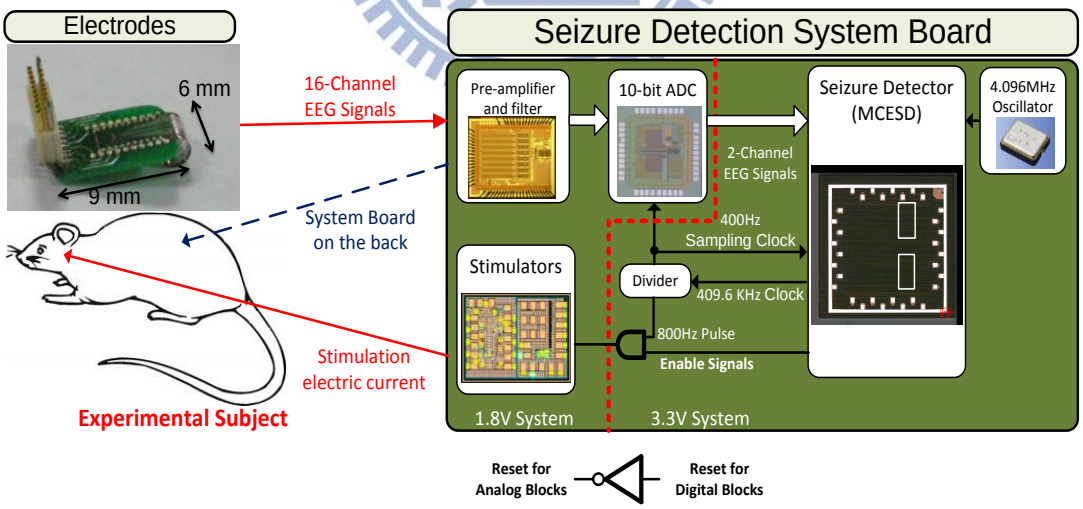


Fig. 6.1 The block diagram of CoB

Publications

1. T.-J. Chen, H. Chiueh, S.-F. Liang, S.-T. Chang, **C. Jeng**, Y.-C. Hsu, and T.-C. Chien, "The Implementation of a Low-Power Biomedical Signal Processor for Real-Time Epileptic Seizure Detection on Absence Animal Models," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 1, no. 4, Dec. 2011.
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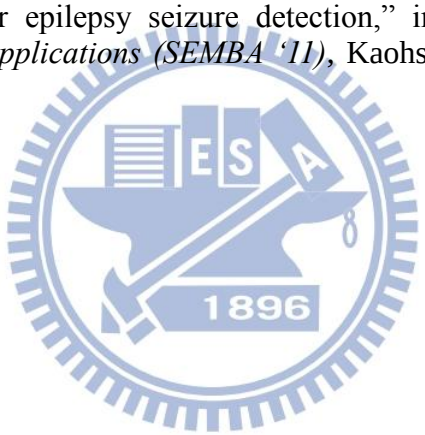

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