國 立 交 通 大 學

電信工程研究所

碩 士 論 文

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A Low-Power Binary Phase Shift Keying Demodulator for Power and Data Telemetry Systems in Biomedical Implants

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摘要

本論文成功地實現一個同時傳輸功率和資料之遙測系統，並針對相位鍵移解調變的部分有特別的改善。以往的相位鍵移解調變電路都是使用鎖相迴路來重現基頻資料，但由於鎖相迴路之功率消耗過大，本論文將以數位電路實現相位鍵移解調變器。首先線圈接受到的載波訊號會經過比較器等電路做數位化的處理，再由後續數位電路偵測訊號之正緣或負緣來做資料的解調。相比以往的解調變電路，此電路的功率消耗很低，適用於植入性的系統。理論上，此解調方式並可支持百分之百的資料率對載波頻率之比例。我們使用台積電 0.18 微米製程實現一個操作在 13.56 兆赫茲的相位鍵移解調變電路，此解調電路之功率消耗為 191 毫瓦。我們考慮到線圈、整流器與解調變器之關係，且選擇適當品質因數的線圈，成功實現一個同時傳輸資料與功率的遙測系統。線圈之品質因數因線圈尺寸的限制而有一定的最佳值，在此最佳之線圈下我們傳輸的資料率可達到每秒傳 678 千位元之資料率。並且位元錯誤率可達到十的負九次方。

A Low-Power Binary Phase Shift Keying Demodulator for Power and Data Telemetry Systems in Biomedical Implants

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Abstract

This paper presents a fully digital binary-phase-shift keying (BPSK) demodulator for data and power telemetry. This demodulator recovers BPSK signals by detecting the symbol edge of the digitized received carrier. Parameters of the coupling coils, rectifier DC output, and data rate are taken into consideration in the early design stage. The demodulator achieves a data rate of 13.56Mb/s at a carrier frequency of 13.56MHz, achieving 100% data rate to carrier frequency ratio. Given a limited coil size and quality factor, the maximum data rate of this system achieves 678kb/s with BER < 10^{-9}. Fabricated in a 0.18μm CMOS process, the chip area is 0.445mm^2. The chip core dissipates 191μW at 13.56MHz. A system prototype was developed to transmit data and power simultaneously through a pair of coils.

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我要感謝鄭銘椮在電路設計給我很多寶貴的意見，還有在工具使用與量測方面也教我很多正確的觀念。感謝魏暐庭在我電路模擬與下線的時候給了我很大的建議跟幫助。

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王俐嵐

9 月 21 日, 2012 於新竹

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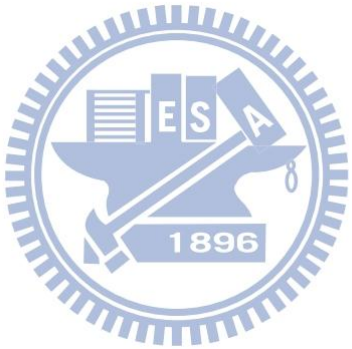


Chapter 1

Introduction

1.1 Power and Data Telemetry

Telemetry is used to transmit data or power from external coil to internal coil. Telemetry consists three parts. Part I consists a modulator and a power amplifier which is used to transmit modulated wave (for data) to coil. Modulator multiplies baseband data with carrier frequency. Modulator is not required in power transmission. Part II is the channel which is used for transmission. Part III is the receiver end, which is rectifier (for power) or demodulator (for data). For power transmission, rectifier is used to convert alternating current (AC) to direct current (DC). For data transmission, demodulator is used to modulation signal to baseband data. In the later section, power and data telemetry are introduced respectively. A data and power transmission is introduced in section 1.2 as well.

Power telemetry [1][2] is used to transmission power from external to implant, as shown in Figure 1. The power transmitter uses a nonlinear power amplifier to increase the power transfer efficiency, reducing heat in the external devices and maintaining a reasonable battery lifetime. Efficiency is the most important issue in power transmission, and there are three parameters influence the efficiency at theory. One is coupling coefficient which is determined by two coil distance and coil inductance, and the others are the quality factor of two coils. With the coupling coefficient and quality factor increasing, the power efficiency is improving.

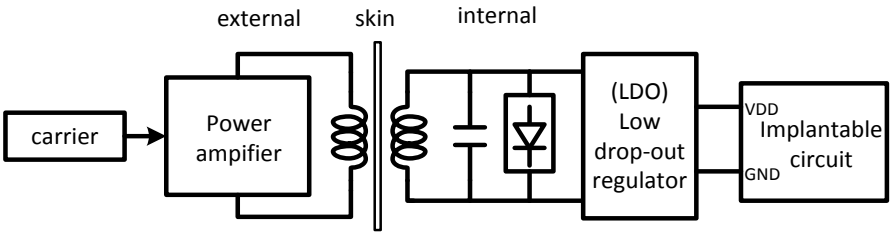


Figure 1. A basic power telemetry

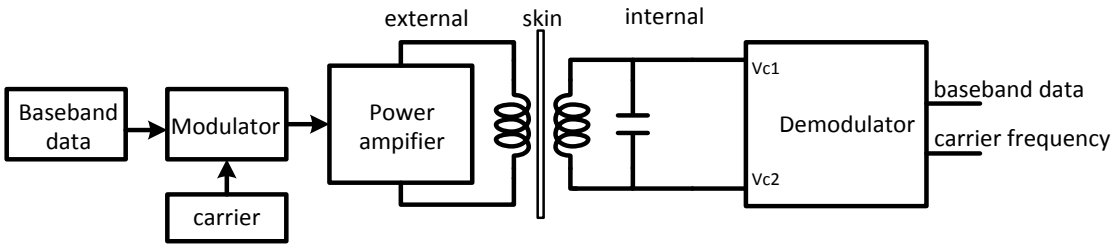


Figure 2. A basic data telemetry

The telemetry is used for data transmission, as shown in Figure 2. Modulation scheme is chosen by different situation. There are two options to increase the data rate. The first option is to reduce the quality factor of the power amplifier, but this reduces the power transfer efficiency. The second option is to increase the carrier frequency, which will increase the skin absorption of electromagnetic energy. How to increase the data rate is an important issue, and the solution will be different in different system.

1.2 Motivation

Epilepsy is a common disease of nervous system disorder, brain damage which is caused by Seizures Epilepsy is after stroke. About 50 million people around the world is suffering from Epilepsy, 70% of patients may control Epilepsy by drugs, 25% of patients by surgery, but 5% of patients' Epilepsy can't be suppressed by drugs and surgery.

Physiological signal monitoring system in the past only record the signal and use computer for subsequent analysis, but the lack of timely analysis function is found.

Therefore, a closed-loop detection and suppression method system is developed. We monitor the real time brain wave, and the signals are also transmitted to a computer to do the processing. Seizures start electrical stimulation inhibits timely monitoring and suppression Epilepsy as shown in Figure 3.

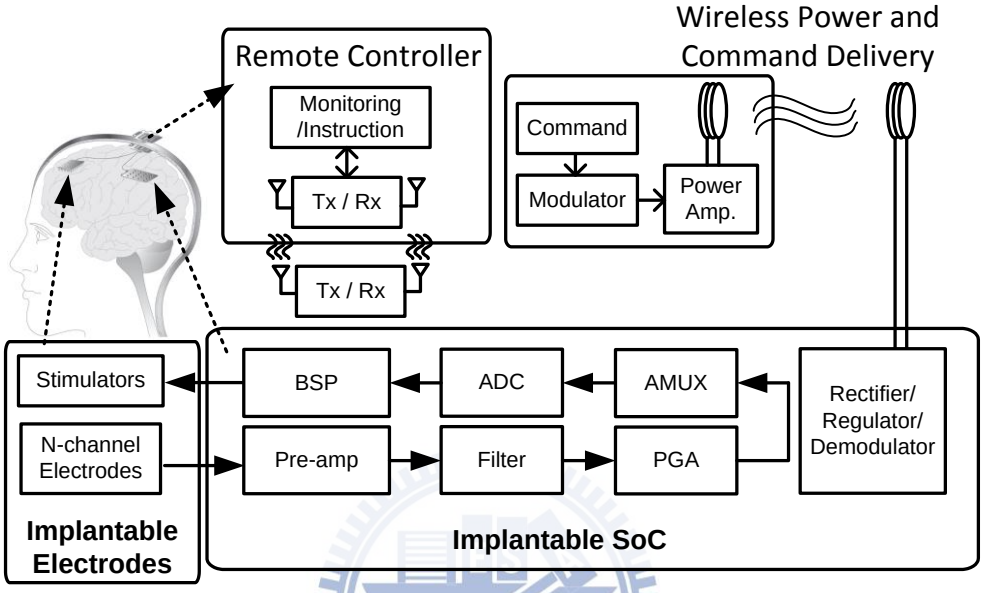


Figure 3. A close loop seizure detector block diagram

Power and data telemetry is the key to battery-less biomedical implants. Wireless power transmission and wireless data telemetry have been extensively studied in [1][2] and [18]-[27], respectively. In order to transmit command to implants, BER performance is an important issue but high data rate. Some groups have developed two pair coils to transmit power and data as shown in Figure 4 and [23]. In order to reduce the number of implanted coils, systems that transmit both data and power were proposed in [18][19]. Figure 5 shows the overall data and power transmission system. The power is transmitted through coils and received inside the human body. The data demodulator is powered by the rectified power.

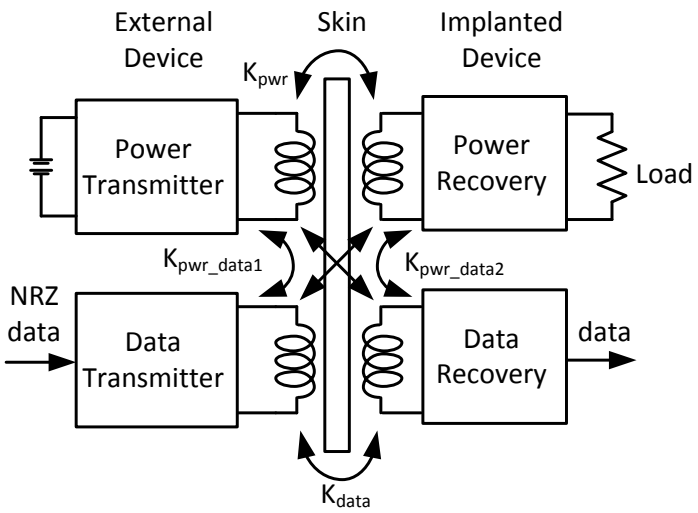


Figure 4. Dual coils power and data telemetry

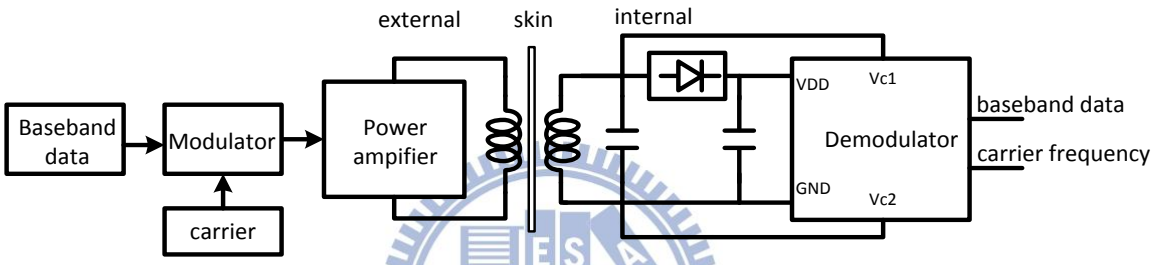


Figure 5. A data and power telemetry

The relation of power efficiency and channel capacity is an issue. The drop-out voltage of rectifier decides the input peak to peak voltage if a stable DC value is desired. Power efficiency is calculated by the parameter of coil and internal coil AC resistance. Once the power consumption of implant circuit is decide, the external transmitted power is derived. According to the transmission power and coil bandwidth, capacity is estimated roughly. Detail equations will be introduced in section 3.1.

1.3 Thesis Organization

This thesis covers theoretical analysis of data and power telemetry and practical circuit design implementation. After introducing the fundamentals of power and data telemetry, the design challenge of system is discussed. According to the target specifications of the telemetry, the design procedure from system level to transistor

level is introduced in detail. The transistor level simulation and prototype chip measurement are also presented. The thesis is organized as following:

Chapter 1 consists of simple introduction and motivation of this thesis.

Chapter 2 is an overview of general telemetry. The principles of channel capacity and power efficiency are also described. The fundamental of modulation scheme is introduced briefly, such as ASK and BPSK. Furthermore, advance techniques of BPSK demodulator are introduced, which can achieve lower power consumption. Finally, the related paper is also discussed.

Chapter 3 proposes the system level design procedure. Due to bandwidth of coil, demodulator must be designed carefully. Power efficiency and channel capacity are estimated roughly. Finally, a system which connects the coil and demodulator is simulated by h-spice.

In Chapter 4, practical circuits design and implementation is introduced. Some non-idealities of practical circuit implementation are considered. The building block designs of proposed demodulator are detailed. Finally, the transistor level simulation of BPSK demodulator is presented.

Chapter 5 and Chapter 6 cover the test environment and the experimental result and conclude the thesis and future work respectively.

Chapter 2

Fundamentals of Power and Data Telemetry

2.1 Relation of Power Efficiency and Channel Capacity

An inductive power link is composed of a transmitter's and receiver's coils (L_1 and L_2), as shown in Figure 6 (a). The coupling coefficient of two coils k ($0 < k < 1$) depends on the portion of the total flux lines that cuts both primary and secondary coils. An AC voltage V_{in} is applied across the transmitter's coil, and this induces an AC voltage V_{c1} on the receiver's coil. Receiving coil is connected to a load R_{load} (Figure 6 (a) [4]). V_{peak} is a fixed value according to data rate, if rectifier output has to achieve 1.8 volts. Rectifier input power is defined by equation (1). Therefore, we estimate the AC resistance by equation (2).

$$\text{rec input power} = \frac{R_{load}\ \text{power}}{\text{rectifier efficiency}} \tag{1}$$

$$R_{ac} = \frac{V_{peak}^2}{2\times\ \text{rec input power}} \tag{2}$$

The equivalent AC parallel resistance can be transform into equivalent AC series resistance Figure 6 (b) [4]. The quality factor of the series LC transmitting circuit is given by

$$\omega_0 = 1/\sqrt{L_1C_1} = 1/\sqrt{L_2C_2} \tag{3}$$

$$Q_1 = \omega_0 L_1/R_1,\ R_L = \frac{(\omega L)^2}{R_{ac}} \tag{4}$$

Where ω_0 is the frequency of oscillation and R_1 is the primary coil series

resistance. R_e represents reflected impedance from secondary coil to primary coil.

$$R_e = \frac{(\omega M)^2}{R_2 + R_L} = \frac{R_{ac} k^2 Q_1 Q_2}{R_{ac} + Q_2^2 R_2} R_1 \tag{5}$$

A bridge rectifier s used to for convert AC-to-DC conversion. The power efficiency η between transmitted and received powers (P_0 and P_1) is represented by

$$P_o = \frac{R_L}{R_L + R_2} \times \frac{R_e}{R_e + R_1} P_1 \tag{6}$$

$$\eta = \frac{P_o}{P_1} = \frac{k^2 Q_1 Q_2^3 R_2 R_{ac}}{\left(R_{ac} + Q_2^2 R_2\right)\left[\left(1 + k^2 Q_1 Q_2\right) R_{ac} + Q_2^2 R_2\right]} \tag{7}$$

As shown in Figure 6(b), R_2 is the resistance of internal coil and R_{ac} is the input resistance of the rectifier. Q_1 (Q_2) is the quality factor of coil L_1 (L_2). This relationship provides the maximum power efficiency given these circuit parameters.

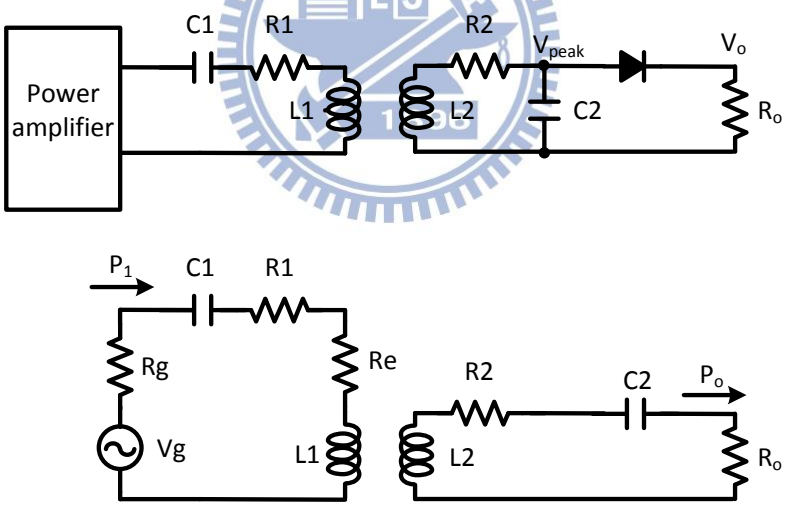


Figure 6. Basic circuit for wireless power transmission

This paper presents a scheme that the coils transmit power and data simultaneously, so we must calculate the system capacity to estimate the limitation of transmission data rate. However, received power is one of important factors for determination of the system capacity. This is well known that higher capacity can be achieved with the higher received signal power.

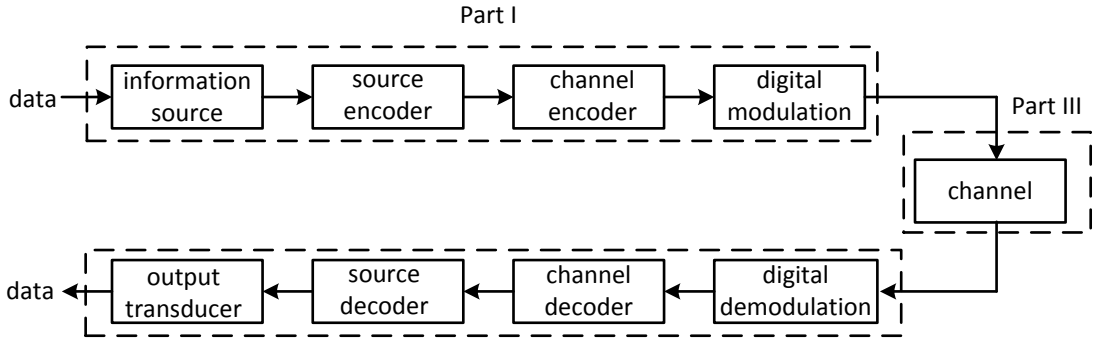


Figure 7. Basic communication system

According to Figure 7 in this book, as shown in [4], data rate can be discussed by three part, where are transmitter part, receiver part, and the channel. At first, the transmitter baseband data rate is half of signal bandwidth, as shown in Figure 8 and [4].

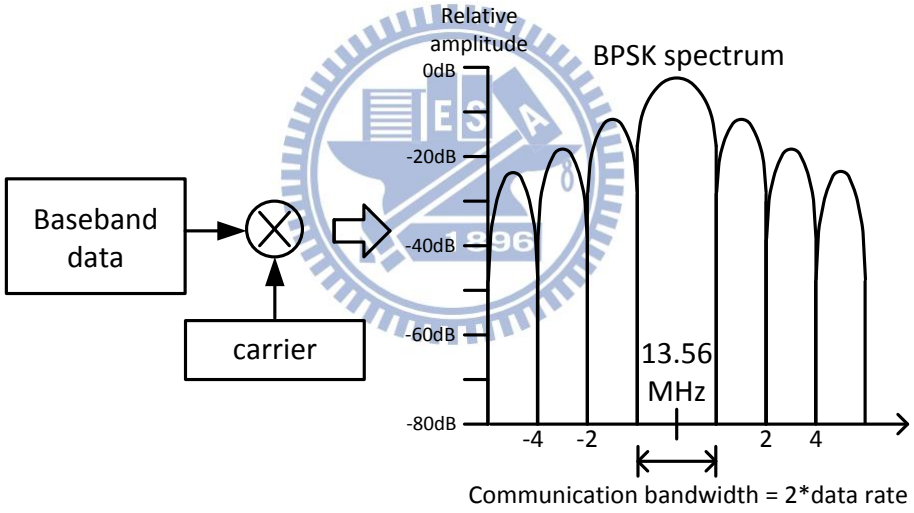


Figure 8. BPSK modulator and power spectrum

$$C = B\log(1+\frac{P_R}{N}) \tag{8}$$

The received power also affects the data transmission. In order to evaluate the maximum data rate, channel capacity is evaluated, as shown in [10]. Channel capacity C is impacted by the received signal power P_R, LC tank bandwidth B, and noise power N. Considering only thermal noise, the noise power N is given by the Johnson's noise formula: (10)

$$N_{power}(watts) = BKT \tag{9}$$

where T is the temperature in Kelvin and K is the Boltzmann constant (1.38×10^{-23}). In our simulation, we assume that the system operate at the room temperature of 27^{o}. The achievable bandwidth B is a function of the Q-factor of transmitter's and receiver's coils [10]. The ratio between signal bandwidth B and carrier frequency f_0 is described below. (10)

$$\frac{B}{f_0} = \frac{\sqrt{-(Q_1^2+Q_2^2)+\sqrt{(Q_1^2+Q_2^2)^2+4Q_1^2Q_2^2}}}{\sqrt{2}Q_1Q_2} \tag{10}$$

The third part is receiver, the receiver's sensitivity, the sensitivity of an RF receiver is defined as the minimum signal level that the system can detect with Acceptable signal-to-noise ratio, as shown in equation (11)-(13) and [6]. SNR_{in} and SNR_{out} are signal-to-noise ratios measured at the circuit input and output respectively. Bandwidth is the twice of baseband data rate.

$$P_{sig,total} = P_{RS}\cdot NF\cdot SNR_{out}\cdot BW \tag{11}$$

$$P_{RS} = \frac{4kT}{R_S}\frac{1}{R_{in}} = kT = -174dBm/Hz \tag{12}$$

$$P_{in,\min|dB} = P_{RS|dB/Hz} + NF_{|dB} + SNR_{\min|dB} + 10\log BW \tag{13}$$

Where $P_{sig,total}$ is received power, P_{RS} is thermal noise, and P_{in} is the minimum received power without error. Once the transmitter, channel capacity, and receiver specs are fixed, we can estimate the highest data rate. The bottleneck of this system data rate will be the channel capacity, because the transmitter bandwidth is decided by the data rate we want to transmit, and the receiver bandwidth is wider than channel capacity because of high received power. There is another issue we have to discuss, the bit error rate in the communication system. Because the receiver circuit is implanted, we have to ensure the high BER performance avoiding from additional circuit to check and

correct the data, as shown in equation (14), equation (15) and [4]. The BER is estimated by the formula which is use for the binary modulation, where f_b is bit rate, and the *BW* means channel bandwidth:

$$\frac{S}{N} = \frac{E_b}{N_0} \bullet \frac{f_b}{BW} \tag{14}$$

$$\begin{aligned} P(n_2 - n_1 > \sqrt{\varepsilon_b}) &= \frac{1}{\sqrt{2\pi N_0}} \int_{\sqrt{\varepsilon_b}}^{\infty} e^{-x^2/2N_0} dx \\ &= \frac{1}{\sqrt{2\pi}} \int_{\sqrt{\varepsilon_b/N_0}}^{\infty} e^{-x^2/2} dx \\ &= Q(\sqrt{\frac{\varepsilon_b}{N_0}}) \end{aligned} \tag{15}$$

2.2 Modulator Scheme Comparison

The common used modulation schemes are ASK, FSK and PSK as shown in Figure 9. ASK modulate the baseband data with the amplitude. One means that the carrier will be transmitted, zero means that a DC voltage is transmitted. FSK modulate the baseband data with the frequency. One means that the carrier$_1$ is transmitted, zero means the carrier$_2$ is transmitted, where the carrier$_1$ and carrier$_2$ is at different frequency tone. PSK modulate the baseband data with the phase. One means that the 0^o will be transmitted, zero means that the 180^o is transmitted. 1 and -1 are the baseband data, the modulator is like a switch which changes data back and forth. The modulated data is transmitted by coil operating at the carrier frequency.

Amplitude-shift keying (ASK) or on-off keying (OOK) is frequently used for data transmission due to its simplicity. However, ASK and OOK modulations suffer from low data rate and instability for power transmission. In contrast, frequency-shift keying (FSK) modulation requires a LC resonator with a low quality factor, but this leads to low power efficiency. Constant-envelope, fixed-carrier frequency modulations conveys stable power regardless of data pattern, which is a better

solution for simultaneous data and power transmission. Binary phase-shift keying (BPSK) is preferred in order to reduce the power consumption of demodulator. Another advantage of BPSK is that it requires less transmitted power to achieve the same bit-error rate (BER) when compared to FSK or ASK, as shown in Table 1.

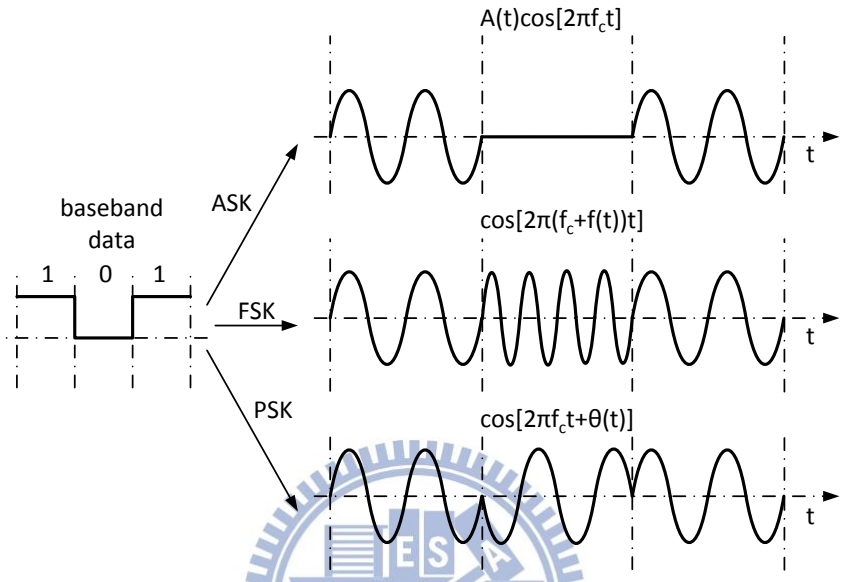


Figure 9. Common modulation scheme

Table 1. Pros and cons of the different modulation scheme

Mod. scheme	Bit Error Rate	Advantage	Disadvantage
ASK	worst of all	1.easy to implement 2.low power consumption	1.increased susceptibility to amplitude noise 2.low data transmission rate
FSK	worse than BPSK or QPSK	high power efficiency	poor bandwidth efficiency
BPSK	Better than FSK	increased noise immunity	1 bit/symbol
QPSK	same as BPSK	better bandwidth efficiency	increased susceptibility to phase noise

Figure 10 shows the BPSK modulator [6], the baseband data is modulated by a switch.For BPSK demodulation, phase-locked loop (PLL) was proposed and it provides stable data and power transmission [6][7]. However, the high power consumption of PLL-based demodulator is not suitable for implantable devices since

PLL requires phase synchronization for coherent detection. For instance, the most commonly used squaring or COSTAS loop, as shown in Figure 11 (b). Extracting clock from received data can be used to eliminate the use of PLL, as shown in Figure 12 (a). This clock-recovery technique was adopted for data transmission [9][10][18], but applying this technique to simultaneous data and power transmission has not been explored.

In this work, we propose a clock-recovery-based BPSK demodulator for data and power telemetry targeting for epilepsy seizure detection. Since power consumption is an important issue for implantable devices, a symbol edge detector is used instead of a power-hungry oscillator, as shown in Figure 12 (b). This replacement further reduces power consumption.

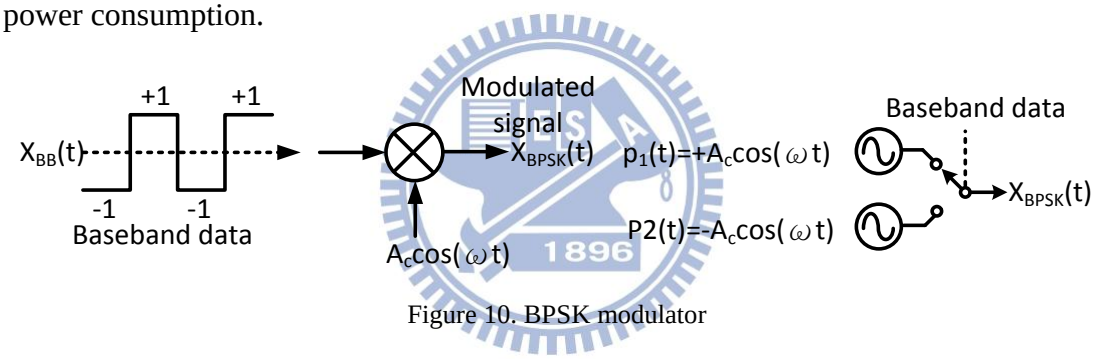


Figure 10. BPSK modulator

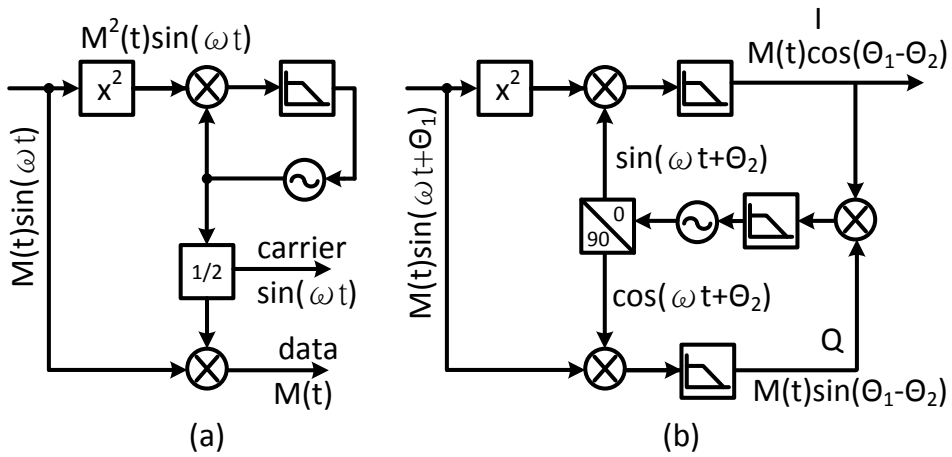


Figure 11. (a) Squaring loop (b) Costas loop

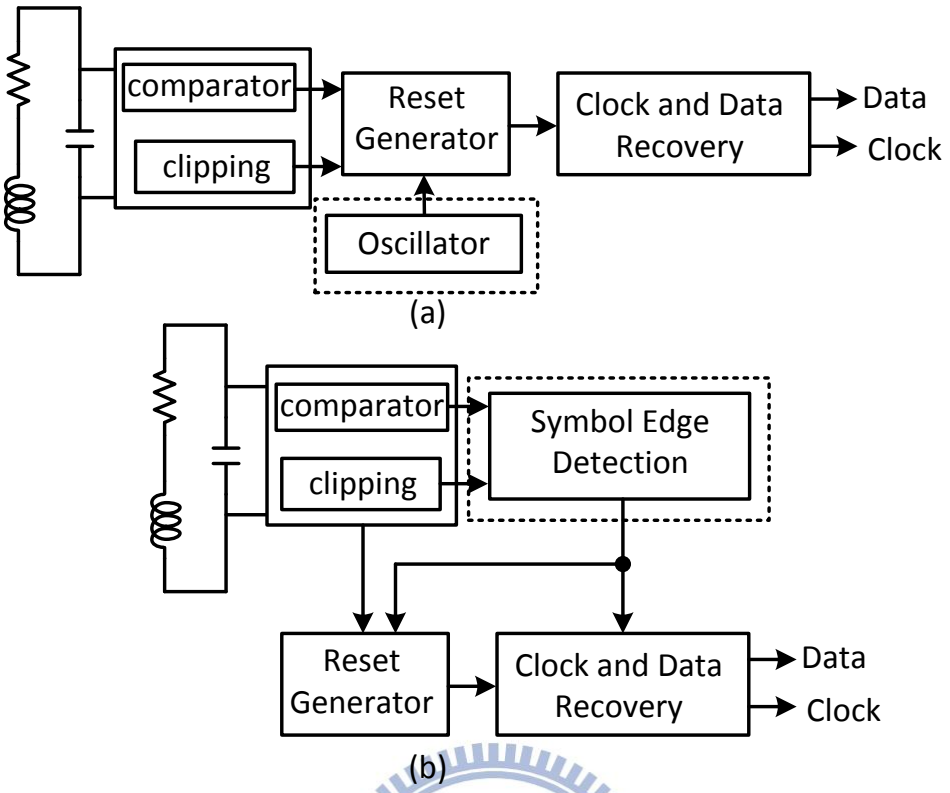


Figure 12. (a) Conventional clock-recovery-based demodulator and (b) proposed oscillator-less demodulator.

2.3 Related Telemetry Paper Review

As we introduce in section 2.2, we prove the theory by the related work. Every work is used for different telemetry, so data rate and power efficiency demand will be different. Reference [12][13][14][15] use the ASK modulation, as we can see the data-to-carrier ratio range is from 0.01 to 0.1. It means that if we transmit 13.56MHz carrier frequency, the most data rate will be 1.356 Mbps, not mention that these systems are not take stable power into account. The only one work which transmits power simultaneously is reference [10]. According the record of this paper, power varies with the data.

FSK demodulator is introduced in reference [17]. FSK is not use frequently in biomedical telemetry. The data-to-carrier ratio is high to 0.5, but the power supply and

power consumption is not mentioned in paper.

BPSK modulation is implemented by reference. Data-to-carrier ratio is from 0.0015 to 1. The reference [18] and [19] successfully transmit a stable 22.5mW to implant. The reference [22] provides a scheme improving the data-to-carrier ratio to 100%, and the demodulator power consumption is low compared to another scheme, but this demodulator is not connected to any communication channel.

Table 2. Comparison of the related demodulator

Article	Data Transmission		Power Transmission		CMOS Tech. (μm)	Area (mm^2)
	Mod. , Data rate (Mbps)	Carrier freq. (MHz)	Power supply (mW)	Power consumption (mW)		
[12]	ASK , 1	13.56	136	–	0.35	–
[13]	ASK , 0.02	2	–	0.815 @ 3.3V	0.35	0.0195
[14]	ASK , 2	10	–	0.84 @ 3.3V	0.35	–
[15]	ASK , 0.3	4	–	1 @ 1.8V	0.18	0.0168
[16]	ASK , 2	10	–	–	0.35	–
[17]	FSK , 2	4 or 8	–	–	1.5	–
[18]	BPSK , 1.69	13.56	22.5	5 @ 3.3V	0.5	0.1
[19]	BPSK , 1.69	13.56	22.5	2.3 @ 3.3V	0.5	0.293
[20]	BPSK , 0.02	13.56	–	3 @ 3.3V	0.5	1
[21]	BPSK , 0.8	4	–	0.059 @ 1.8V	0.18	0.0043
[22]	BPSK , 0.8 / 4 / 8 / 20	0.8 / 4 / 8 / 20	–	0.046 / 0.093 / 0.148 / 0.31 @ 1.8V	0.18	–
[23]	DPSK , 2	20	100	6.3 @ 1.8V	0.35	4.42
[24]	QPSK , 4	13.56	–	0.75 @ 1.8V	0.18	–
[25]	QPSK , 8	13.56	–	0.91/0.68 @1.8V	0.18	0.238

The other modulations are DPSK and QPSK respectively. First, we discuss the DPSK modulation [23], this paper transmit power and data separately (using two coils) for the optimal power efficiency and data rate. The most important issue of two coils is the interference between two channels. This paper implements a DPSK modulation to

cancel the interference by inter-symbol noise subtraction. The other modulation is QPSK [24][25], as the theory, outstanding data-to-carrier ratio which is high to 0.58, but the power consumption is much higher than BPSK scheme. According to theory, the QPSK demodulator is two sets of BPSK basically, so the power consumption of QPSK will be twice the BPSK using the same circuit.

For a stable power transmission, low demodulator power consumption and high BER. BPSK modulation scheme is used in this paper.

Chapter 3

System Level Design

3.1 System Level Parameters

Figure 13 shows the block diagram of this power and data transmission system. First at all, the coil parameter is defined. Owing to the constraint of implant size, the inductance of internal coil must be low, where the quality factor of internal coil is low. The quality factor of internal coil is 30.99. Higher quality factor of coil achieves higher power efficiency, and High power efficiency upgrade the channel capacity, so external quality factor of coil must be great for better power efficiency and channel capacity. In our work, the external quality factor is 165.66 [1].

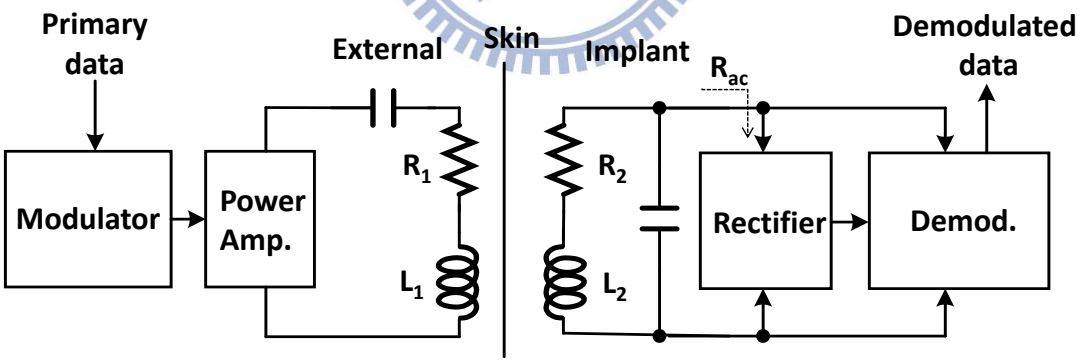


Figure 13. A data and power telemetry block diagram

We use a bridge rectifier to convert AC voltage to DC. For the high frequency (13.56MHz) operation in this power and data telemetry, Schottky diode is chosen to rectify the received signal. Once the rectifier spec is known, the rectifier efficiency and the implant circuit power consumption are fixed. In this paper, efficiency of rectifier achieves 70% based on the datasheet. 5mW is needed for implant circuits.

The minimum power received by the inter coil is 7.14mW=5mW/0.7. R_{load} is rectifier input resistance parallel with the demodulator input resistance, and input resistance of the demodulator is high impedance. The input resistance of internal implants is about R_{load}. When we measure the coil and rectifier to estimate the power efficiency, demodulator circuit is no need to connect. We want to rectify a 1.8 DC voltage for the demodulator circuit, and V_{peak} of internal coil is $5.8V_{pp}$. Once the internal coil V_{peak} and received power is obtained, the R_{ac} is known to be 2356Ω. The parameter of coil power efficiency is known, the coupling coefficient is 0.05122, the quality factor of L_1 is 165.66, and the quality factor of L_1 is 30.99. R_2 is 1.05Ω. The power efficiency is about 26.84%. The external coil has to transmit 26.6mW=7.14mW/0.2684.

Once the received signal is obtained, the channel capacity could be estimated. We know that the $C=Blog(1+S/N)$. The channel bandwidth B is 78kHz which is calculated by equation. The S is the received power 7.14mW. The $N=BW*K*T$. In our simulation we have assumed that the system is operating at the room temperature of about 27^o in the resonance frequency 13.56MHz. If the communication bandwidth is varied with data rate, N=828*data rate*10^{-17}. We assume that the data bandwidth is 1 Mbps. Then the channel capacity is estimated to 942.9 kbps. After the SNR is known, the BER is estimated as well. E_b/N_0=(SNR*(channel bandwidth))/bit rate. E_b/N_0=6.81*10^{10} (BER < 10^{-9}).

3.2 Coil and Rectifier Architecture

Once the implant physical size constraint is decided by system application, the coupling coefficient(k) can be maximize by proper choosing the outer diameter size of coils, and the Q factor can be maximize by the coils' structure and coils' material. Since Q factor and coupling coefficient are increase as the outer diameter increase, the first step of efficient near-field coils design maximizing the coupling coefficient would not conflict

the design parameter of maximizing the Q factor. Once we maximize the coupling coefficient by deciding the primary and outer diameter of secondary coil, that recent research have been widely studied [34], we can maximize the Q factor by using allowable wide copper metal and low loss coil structure. The coil structure mainly divides into three parts: multi-layer cylindrical coil, single layer cylindrical coil and spiral coil, as shown in Figure 14 (c). The different structure have different Q factor, because the skin effect and the proximity effect [35]. In this paper, the single layer cylindrical coil is used for external coil because the greater quality factor. The internal coil which we choose is the spiral coil, because the cylindrical coil is too thick to implant.

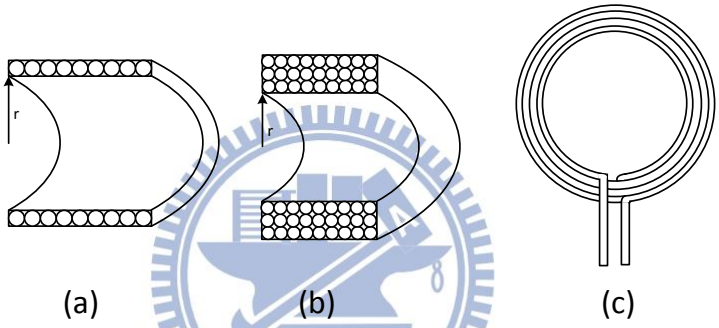


Figure 14. (a) Single layer cylindrical coil (b) Multi-layer cylindrical coil (c) Spiral coil which is winded by copper conductor

The carrier resonance frequency is set to 13.56MHz.The parameters of coils are summarized in Table 3.

Table 3. External and internal coil spec

	Primary coil	Secondary coil
L (μH)	7	0.382
C (pF)	18.8	374.25
R (Ω)	3.6	1.05
Q	165.66	30.99
diameter (cm)	4.2	1.1
thickness(cm)	1.8	0.2

After coil parameters are fixed, the rectifier spec is known. We use simple bridge rectifier by using schottky diode, as shown in Figure 15 (a). When the positive cycle

is applied to the rectifier (the solid line), D1 and D3 is conducting, and the D2 and D4 are cut off. The induced current in internal coil goes through the red path, as shown in Figure 15 (b). When the negative cycle is applied to the rectifier (the solid line), D2 and D4 is conducting, and the D1 and D3 are cut off. The induced current in internal coil goes through the red path, as shown in Figure 15 (c).

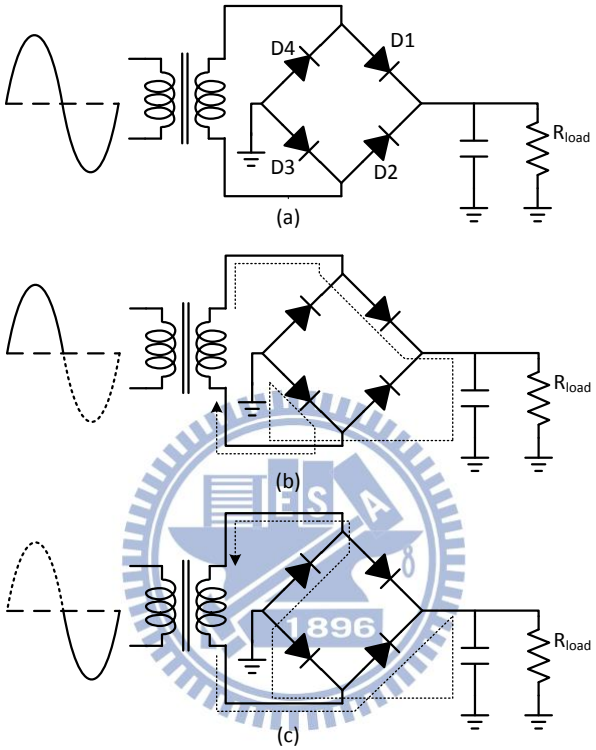


Figure 15. (a) Bridge rectifier (b) Positive cycle function of the bridge rectifier (c) Negative cycle function of the bridge rectifier

Once the rectifier function is working, we let that the rectifier conducting voltage be V_r. DC voltage applied to the R_{load} is that V_{peak} minus $2V_r$ as shown in Figure 16. R_{load} is input resistance of VDD and GND in demodulator which is 1.2kΩ. We connect a large capacitor 1μF to make the ripple of V_o as small as we can.

If we transmit all 0 or all 1 data (a 13.56 MHz sine wave without modulated), we can derive the rectified DC value by the equation (16)-(19) and Figure 16.

$$V_O = V_S - 2V_\gamma \tag{16}$$

$$V_{O\min} \cong V_p \exp\left(-\frac{T}{2RC}\right) \tag{17}$$

$$V_p \cong V_p \frac{T}{2RC},\ V_r \cong \frac{V_{r\_pp}}{2\sqrt{3}} \cong V_p \frac{T}{4\sqrt{3}RC} \tag{18}$$

$$V_O = V_p - \frac{V_{r\_pp}}{2} = V_p\left(1-\frac{T}{2RC}\right) \tag{19}$$

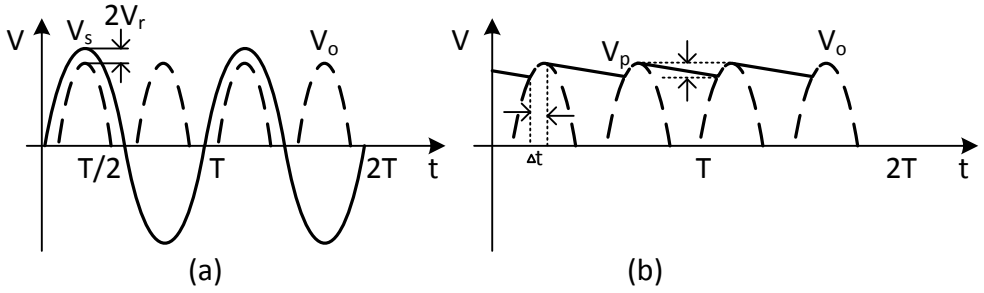


Figure 16. (a) Relation of rectifier drop-out voltage and input V_{peak} (b) Ripple of V_r

3.3 BPSK Demodulator Architecture

A clock-recovery-based demodulator architecture is adopted to reduce the complexity induced by PLL. The BPSK demodulator circuit is presented in Figure 17. There are four blocks, and the first block of comparator and clipping which is connected to internal coil. The second block is enable circuit, and it's an important part to power on at the symbol edge. The third block is reset generator which is used for generating the right reset signal at inter-symbol. The last block is data and clock recovery, where is used to regenerate the baseband data and carrier frequency.

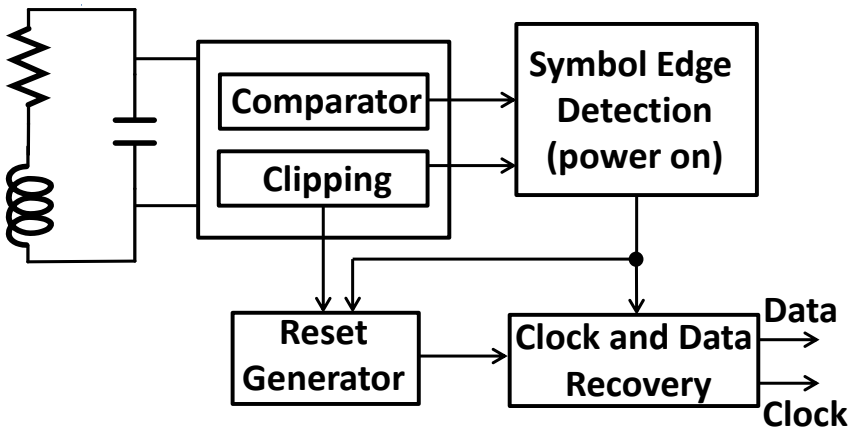


Figure 17. A BPSK demodulator block diagram in this work

Figure 18 shows waveform of first block. BPSK modulation converts baseband data 0 and 1 into two in-phase waveforms. It converts analog signals to digital signals through comparator and clipping circuit. When the $V_{c1} > 0$ and $V_{c2} < 0$, the comparator_out+ is high and comparator_out- is low. When $V_{c1} > 1.05V$, the clip_out+ is high and clip_out- is low. When the $V_{c2} > 0$ and $V_{c1} < 0$, the comparator_out- is high and comparator_out+ is low. When $V_{c2} > 1.05V$, the clip_out- is high and clip_out+ is low. Once these four signals are obtained, the later circuit will start by detecting these signals.

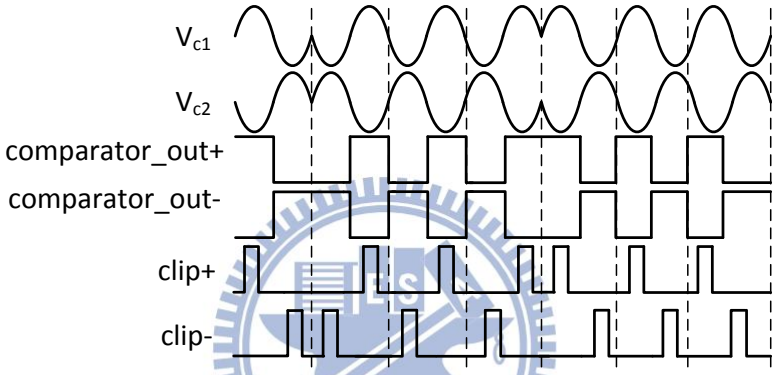


Figure 18. Comparator and clipping circuits function

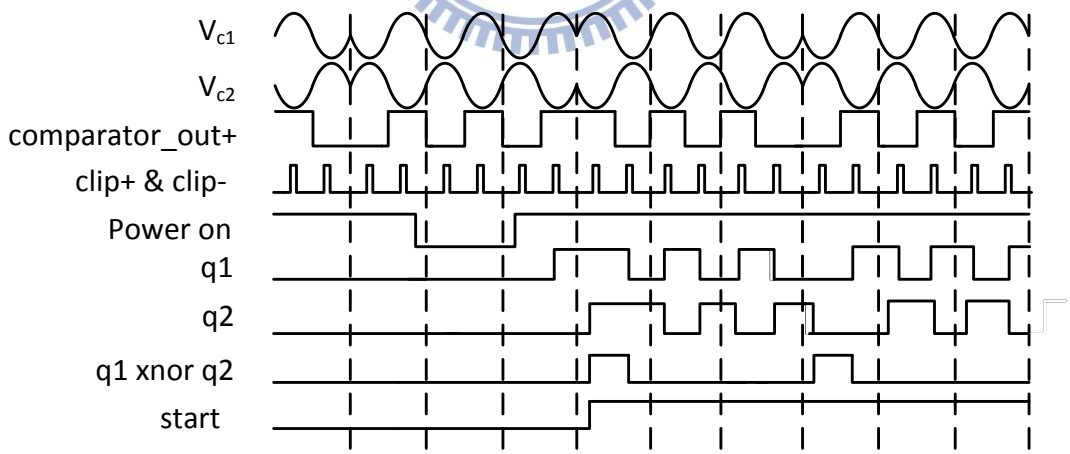


Figure 19. Start circuit's function

The right symbol edge should be detected in order to recover the data. There are two circuits to generate the enable signal. The first is a circuit named start circuit, one of the differential outputs of the clipping circuit (clip+ or clip-) is used to extract the clock frequency and trigger the start signal. Figure 19 shows the functionality of the

start circuit. An external power on signal is switched to enable the detection process. The second circuit is named enable circuit. Because the start circuit is triggered at the clip_out edge, which will make the enable signal is leading for a half cycle. We use a 3-bit counter which counts to 7 to start the enable signal as shown in Figure 20. The counter counts to 7, so the signal is triggered leading for a half cycle also. The final enable signal is triggered at symbol edge correctly.

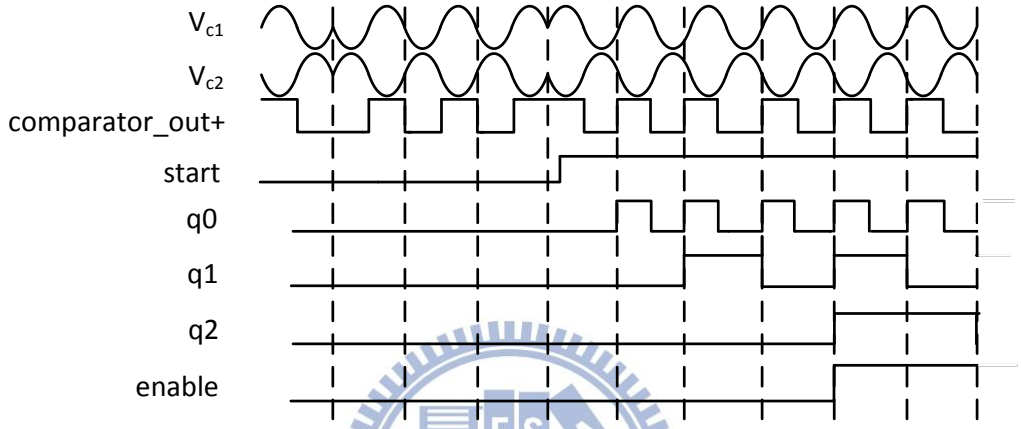


Figure 20. Enable circuit's function

The third block is the reset generator, as shown in Figure 21. After digital signals are extracted, there is an edge detection circuit to detect rising or falling edges. When two falling edges are detected, the reset signal is pulled to high. The reset signal goes down if a rising edge is detected. The reset generator is working until the enable signal is pulled to low.

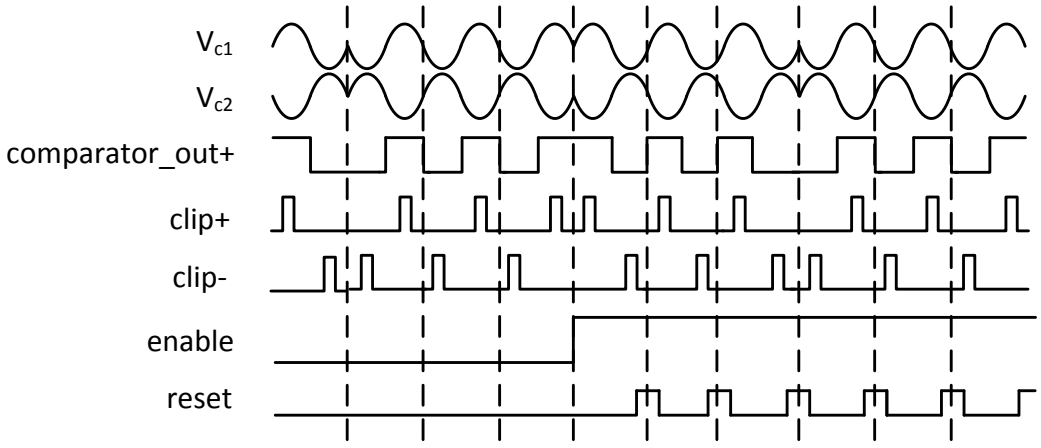


Figure 21. Reset circuit's function

We propose an area-efficient circuit implementation for data-and-clock recovery (DCR). It consists of two D flip-flops whose clocks come from the differential outputs of the comparator and data input is connected to high. Timing diagram of the key signals are shown in Figure 22.

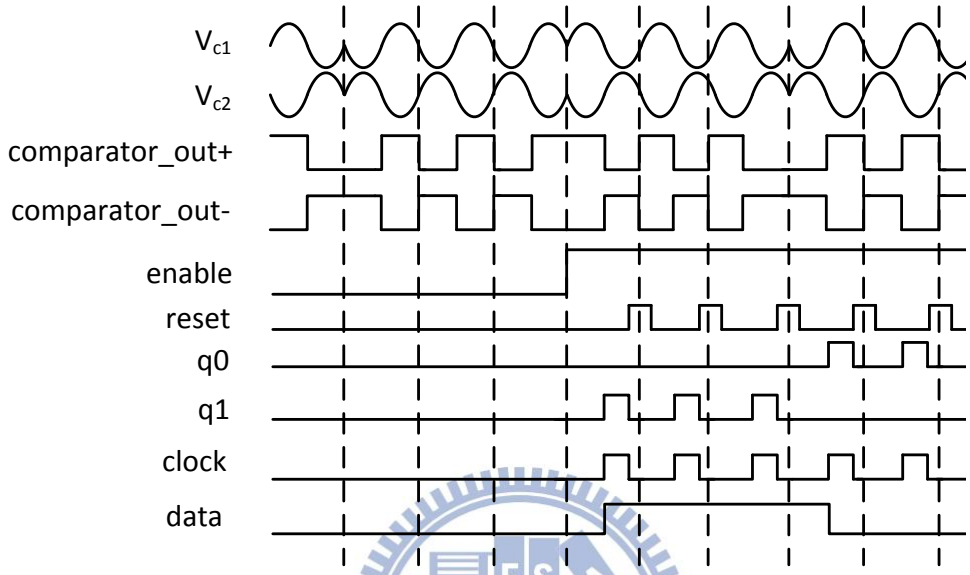


Figure 22. Data and clock recovery circuit's function

The q_0 and q_1 signals are generate by the comparator_out+ and comparator_out- respectively. Reset signal is used to reset the q_0 and q_1 signal at symbol edge. The q_0 and q_1 generate a clock. Frequency of this clock is the same as carrier from the coil. Once the reset signal goes high, an edge detector generates right signals to DCR.

3.4 System Level Simulation

We simulation the coil and demodulator circuit simultaneously by h-spice. If we transmit the same power to the external coil, the received coil amplitude changes with different data rate as shown in Figure 23. The last line is the received waveform at 13.56 Mbps data rate, and it's clearly that the power is not transmitted to the internal at all. Figure 23 shows that the data rate higher than channel capacity. It's clearly that the received input waveform's distortion is too large to detect by our BPSK demodulator. We estimate that comparator_out+ is wrong at every symbol edge. The

data is impossible to be recovery.

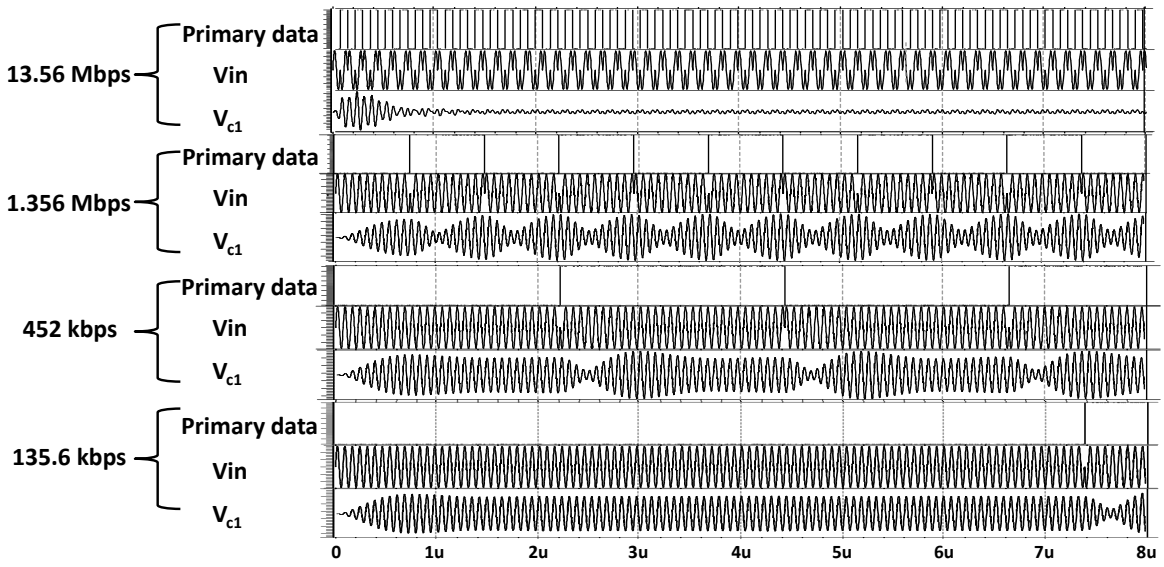


Figure 23. Received waveform in internal coil at data rate higher than 678 kbps with PRBS

Chapter 4

Circuit Design and Implementation

4.1 Comparator and Clipping Circuit

As introduced in Chapter 3, we have to digitize the modulated signals. In the beginning, comparator and clipping circuits are needed. The most important issue of comparator and clipping circuit is to make sure that the transitions of these two circuits occur on different input voltage.

A common mode DC voltage in the comparator circuit is 0 volt. We assume that the differential input varies from -4 volt to 4 volt. In this part, we separate the DC and transient analysis into 4 regions, as shown in Figure 25 (a).

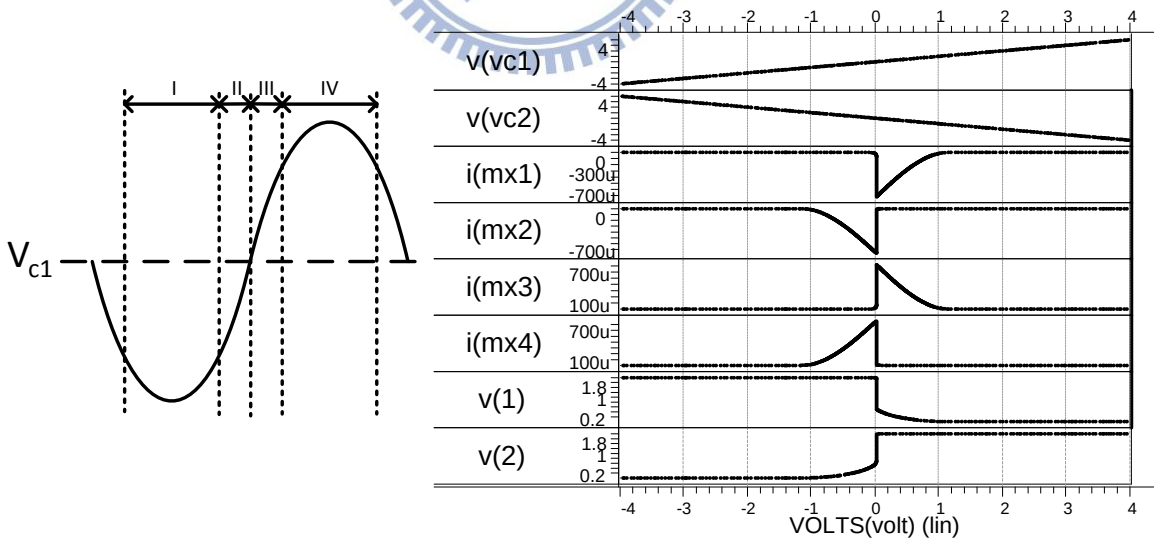


Figure 24. (a) Transient analysis of comparator (b) Direct current analysis of comparator

Region I: when V_{c1} = -4 volts and V_{c2} = 4 volts, $|V_{sgM1}| > |V_{thp}|$ and $|V_{sgM1} - V_{thp}| > |V_{sd}|$. M1 is operating in saturation region. M2, M3 and M4 are in cut off region. The point V_1 is at high level, and V_2 pulls to low, as shown in Figure 25 (b).

Region II: When V_{c1} decreases and V_{c2} increases, as $|V_{sgM2}| > |V_{thp}|$ and $|V_{sgM2}-V_{thp}| < |V_{sd}|$, M2 is going to operate at triode region. Once current of M2 is not 0 volt, V_2 and V_{dsM4} increase to conduct M4. When $|V_{gsM3}| < |V_{thn}|$, M3 is still in cut off region, as shown in Figure 25 (c).

Region III: When V_2 continues to increase, as $|V_{gsM3}| > |V_{thn}|$, M3 is operating at triode region. Once V_1 decreases simultaneously, as $|V_{gsM4}| < |V_{thn}|$, M4 is in cut off region, as shown in Figure 25 (d) .

Region IV: When V_{c1} still increases, as $|V_{sgM1}| < |V_{thp}|$, M1 is cut off, and current of M3 is 0 volt. We can derive that V_1 is at 0 volt and V_2 is at 1.8 volt, as shown in Figure 25 (e).

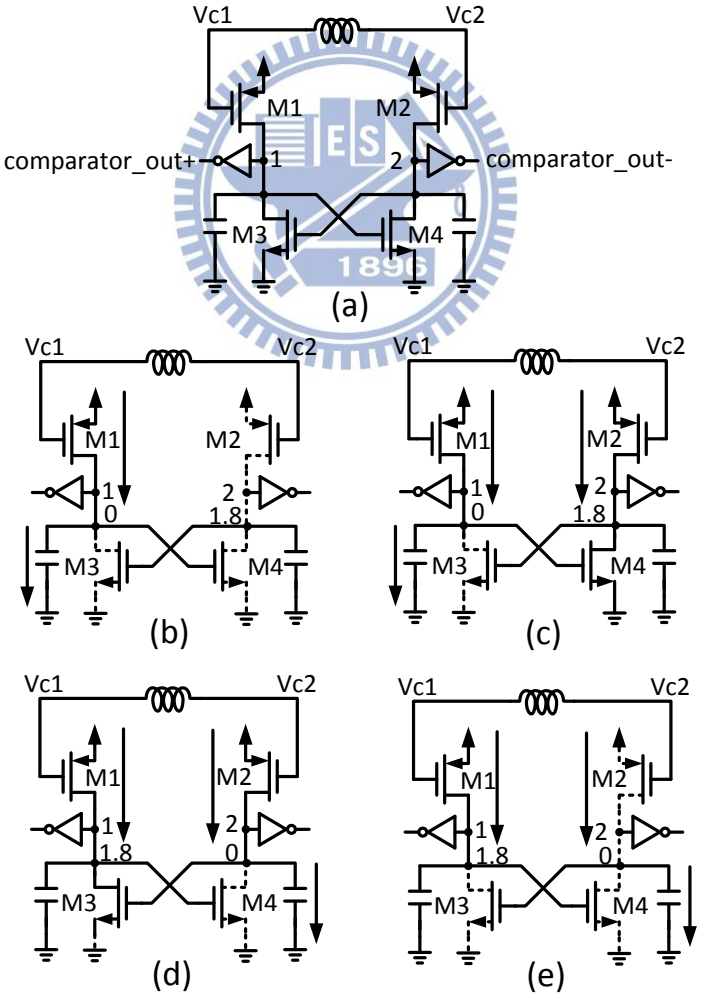


Figure 25. States of the comparator (a) comparator circuit (b) region I (c) region II (d) region III (e) region IV

The other circuit is clipping. According to chapter 3, we know that the output spec of clipping and comparator. Clipping pulls differential output to high when input signal is larger than 1 volt, as shown in Figure 26. We separate the transient and DC analysis into 5 regions, as shown in Figure 27 (a).

Region I: when V_{c1} = -4 volt and V_{c2} = 4 volt, as $|V_{sgM1}| > |V_{thp}|$ and $|V_{sgM1} - V_{thp}| > |V_{sd}|$, M1 is operating at saturation region. When $|V_{sgM2}| < |V_{thp}|$, M2 is cut off. Current of M4 and M6 are zero. When V_2 is 0 volt, we can derive that $|V_{gsM3}| < |V_{thn}|$. $|V_{gsM5}|$ is smaller than $|V_{thn}|$, as shown in Figure 27 (b).

Region II: When V_{c1} increases and V_{c2} decreases, as $|V_{sgM2}| > |V_{thp}|$, M2 is at triode region. However, V_2 is still too low to make M4 and M6 to operate in triode region, as shown in Figure 27 (c).

Region III: In this region, V_2 is still larger than 2 V_{thn}. M3 and M5 is operating at saturation region. We can see that M1 to M6 are at saturation region. V_1 and V_2 are 1.8 volt right now. If we connect a small size inverter to V_1 and V_2, clipping differential outputs will be 0 volt at the same time, as shown in Figure 27 (d).

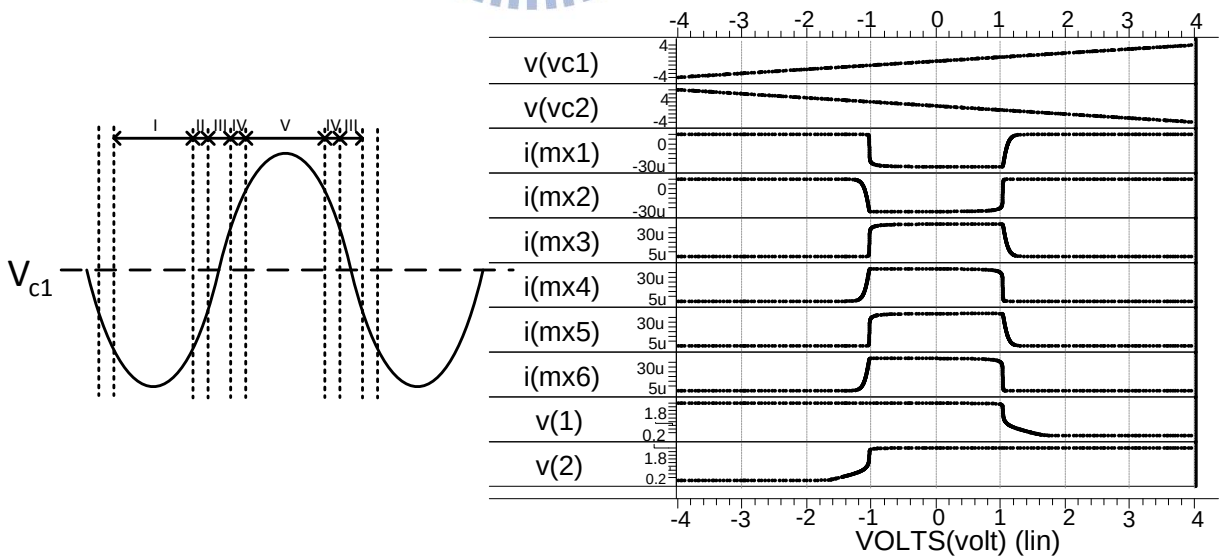


Figure 26. (a) Transient analysis of clipping (b) Direct current analysis of clipping

Region IV: Once V_{c1} increase and V_{c2} decrease, M1 is going to operate in triode region. With the decreasing current of M1, V1 will be smaller than 2 V_{thn}. M4 and M6

are in cut off region, as shown in Figure 27 (e).

Region V: In final region, $V_{sgM2=} V_{DD}-V_{c1}$. When $|V_{sgM2}| < |V_{thp}|$, M1 is cut off. V1 is at 0 volt and V_2 is at 1.8 volt, as shown in Figure 27 (f).

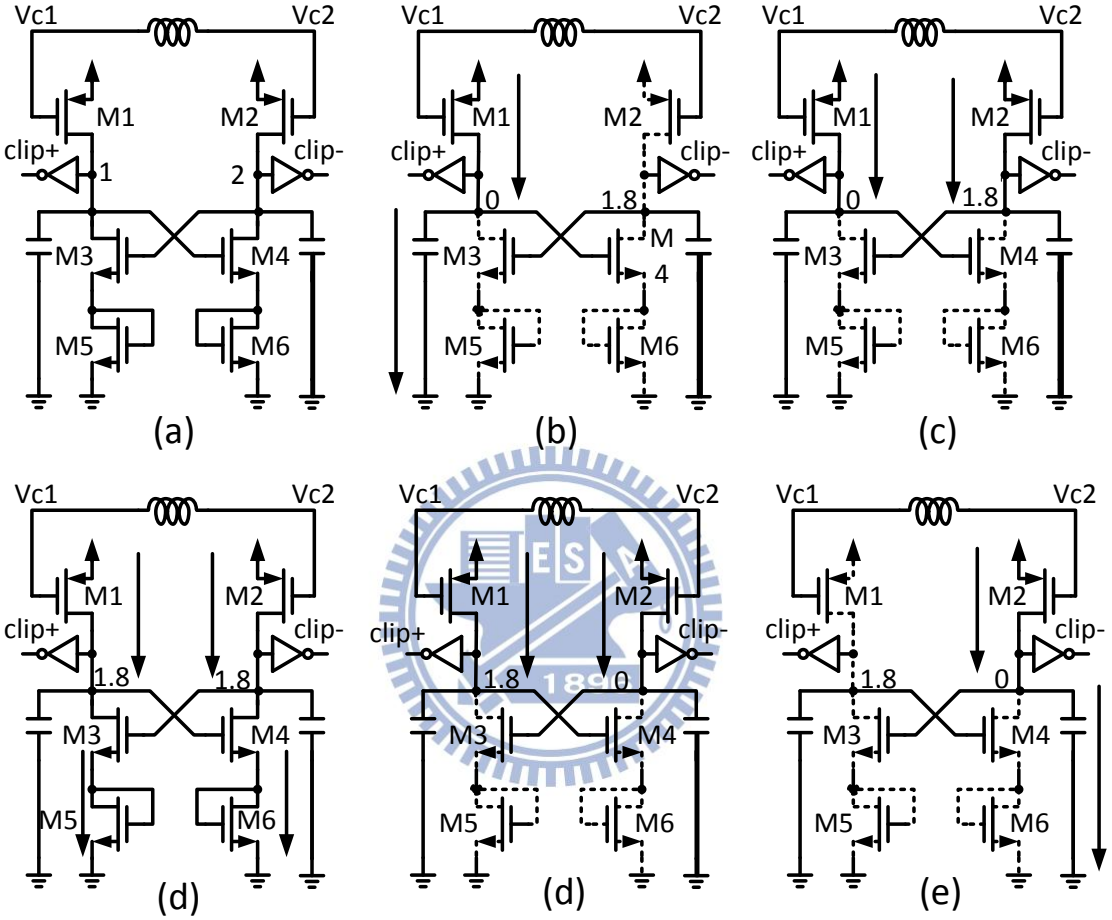


Figure 27. States of the clipping (a) clipping circuit (b) region I (c) region II (d) region III (e) region IV (f) region V

4.2 Power and Data Distinguish

This paper shows the telemetry which transmits power and data simultaneously, so it's important to distinguish the power and data. When the data is prepared to deliver, we must sure that the signal which starts the whole demodulator circuit will be triggered at symbol edge. First, there is a start circuit which uses two DFFs to ensure the correctness of start signal. If a transition of data occurs, comparator

positive end output will be zero or one for a cycle as shown in Figure 28.

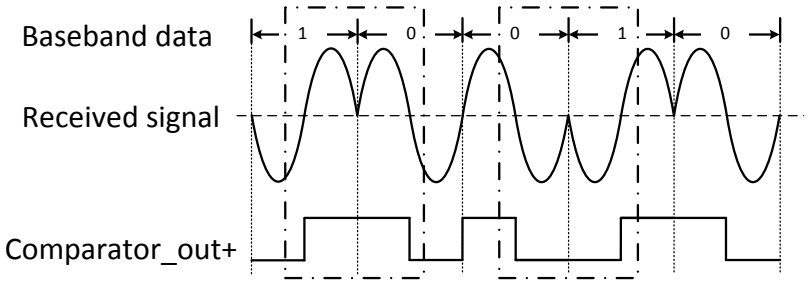


Figure 28. Waveform of received analog signal and comparator output

The input of the first stage DFF is comparator single end output named comparator_out+. Power on signal which is triggered by user will be the reset input of these two DFFs, as shown in Figure 29. The second stage output will delay half cycle compared to first stage. Once data transition occurs, the output of these DFFs will be the same (all 0 or all 1). We use a XOR gate and an inverter to detect the transition. A signal where q_0 XNOR q1 is obtained, it will be a clock of the last DFF. Once the DFF is triggered, the start will be high until the power on signal reset it.

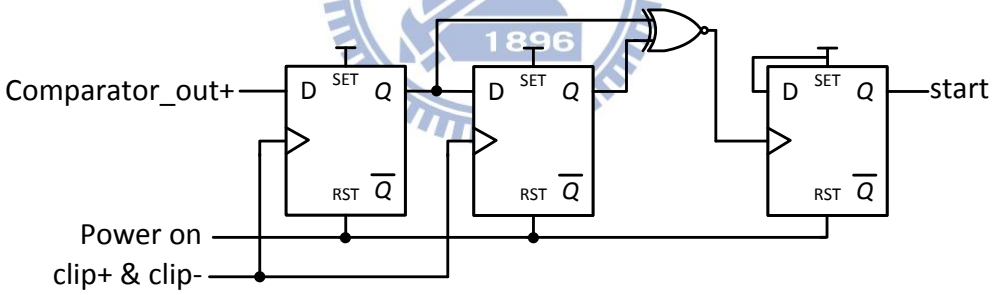


Figure 29. Start circuit in this work

After start signal is triggered, a 3-bit counter is used to enable the data demodulator. The enable signal is given by power on circuit, as shown in Figure 30. Once we start to transmit data, the counter counts to 7 to enable the whole demodulator circuit. The initial value of this counter is reset to zero by and gate and XOR gate. Once the counter counts to 7. q_0、$q_1$and q_2 are all high, at this time, if power on signal is low, the XOR gate output will be low. The initial value is set.

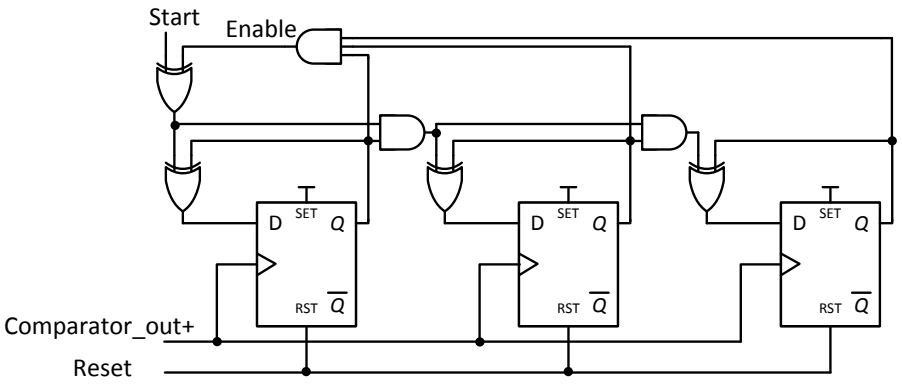


Figure 30. Enable circuit in this work

These DFF clock signal are comparator output. In this section, transmit bit data which is zero, it means that the first half cycle of comparator output is 1.8 volt, and the last half cycle is 0 volt. If we transmit data one, the output will be opposite to zero. One thing is sure that the start signal is triggered at symbol edge. As we can see (Figure 31), if DFF is positive triggered, the start signal will be right when data is one, but it will be error when data is zero. We have to use two sets counter to fixed it, one counter is positive edge triggered, and another one is triggered by negative edge. The two counters input are comparator_out+ and comparator_out- separately. The enable signal will be trigger at symbol edge, as shown in Figure 32.

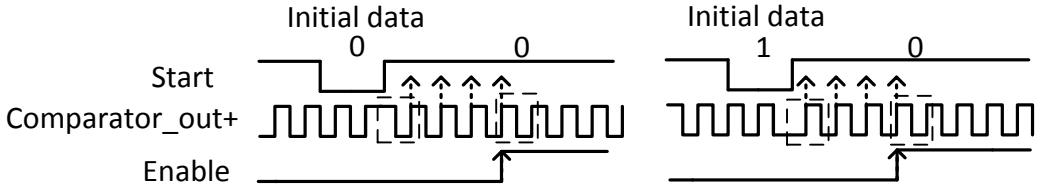


Figure 31. Waveform of positive triggered enable circuit

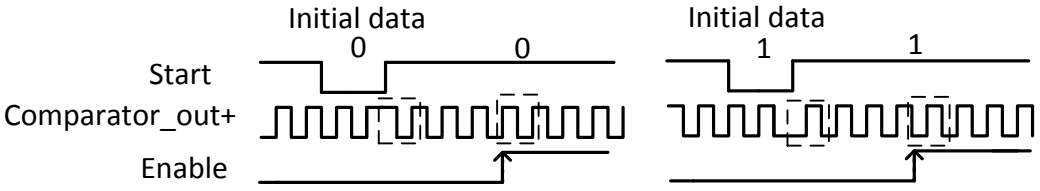


Figure 32. Waveform of positive and negative triggered enable circuit

4.3 Reset Generator

After the enable signal is triggered, the reset generator starts to work. It's important to produce a reset signal at symbol edge. A cycle of received data will output one clip+ and clip- signals no matter the data is one or zero. The circuit detects two falling edge of clip+ and clip-, and it means one cycle is received, and then the rest signal is pulled to high. Inter symbol transitions will be reset.

We use two DFFs to divide frequency of clip+ and clip-. The enable pulls to high at symbol edge, but the clip+ and clip- signal have a little delay. We assume that the clock (clip+ and clip-) will trigger after delay compared to enable as shown in Figure 33 and Figure 34. We separate the flow to four parts.

Part I: When enable is low, DFF is set to be high using set=1 and reset=0.

Part II: When enable is high, but the clip+ and clip- is not going to high yet. At this time, enable exclusive or Q will be zero.

Part III: clip+ or clip- pulls to high, DFF will pass value zero from D to Q, and it will make the enable exclusive or Q signal become one. Then the state will be keeping until the next positive edge trigger.

Part IV: the clock trigger again, the D value one will pass to Q.

D is twice period of clock as shown in Figure 34. The signal which is enable exclusive or Q becomes zero. And the D value will be zero.

Part III and Part IV will be a loop until the enable become low again.

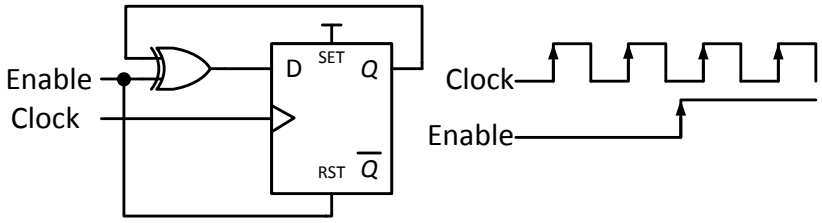


Figure 33. DFF cell of reset circuit

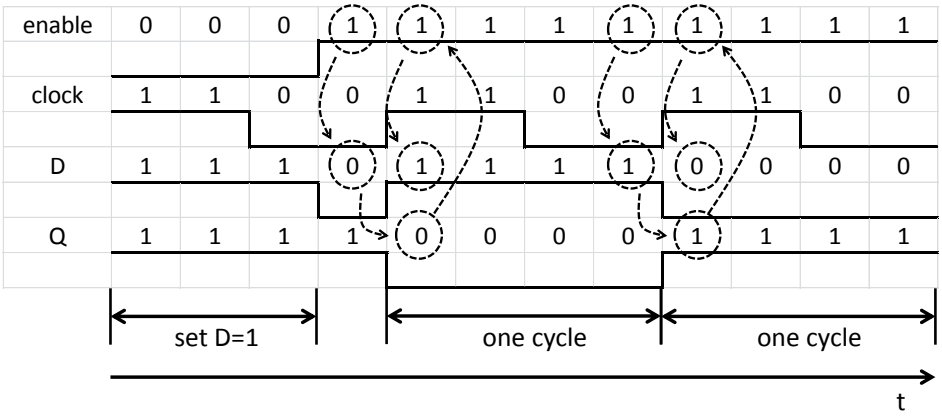


Figure 34. DFF function of the reset circuit

The whole reset generator circuit shows in Figure 35. The upper DFF is used to detect the rising edge. And the lower DFF is used for falling edge detecting. The lower DFF clock input will be opposite to the upper DFF.

After we obtained the str and stf signals, as shown in Figure 36. We can use these two signals to construct the signal we want. We know that these two signals will be high simultaneously at one symbol end to the start of the next symbol. We can successfully produce a reset signal, as shown in Figure 36.

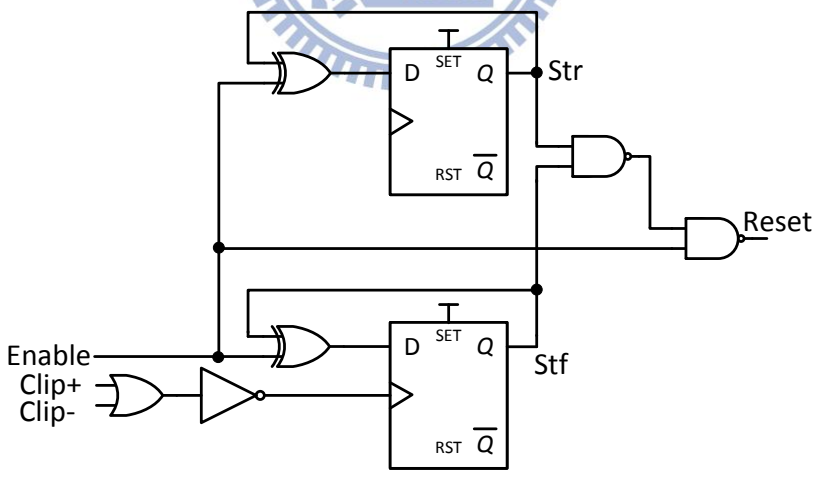


Figure 35. Reset circuit in this work

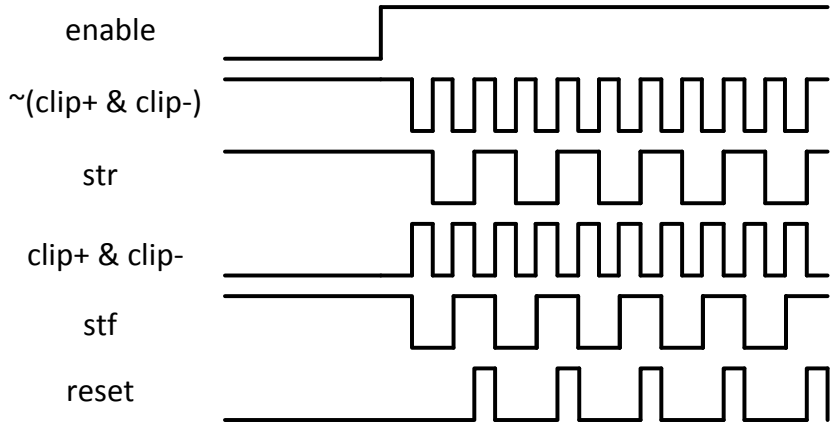


Figure 36. Waveforms of the reset circuit

4.4 Data and Clock Recovery

A data and clock recovery system is introduced here, as shown in Figure 37. First, we want to get the clock signal. The data input D of these two DFFs are high, and the clock input will be comparator differential output respectively. The reset signal is generated by the reset circuit. If data which we transmit is one, the upper DFF output q_bar will be pull to low when the positive edge occurs, and q_bar will pull to high when reset signal is high. If data which we transmit is zero, the lower DFF is working like the upper one. After the q_1_bar and q_2_bar are obtained, a NAND gate is used to recover a periodic clock. The clock frequency will be the same as carrier frequency. At last, baseband data must be generated. The last stage DFF data input is Q1. If data is one, the first half cycle of symbol is low, and after the half cycle is high. If data is zero, the whole cycle is low. When the last DFF clock is triggered at the later cycle of symbol, data is obtained.

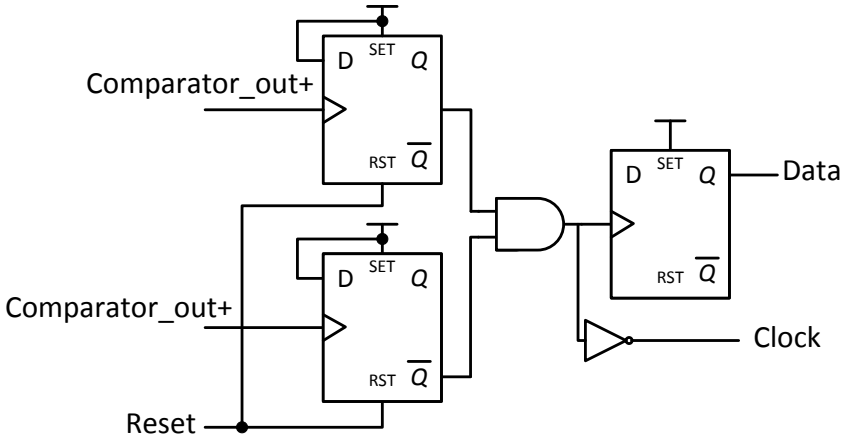


Figure 37. Data and clock recovery circuit in this work

4.5 Transistor Level Simulation

We use radio-frequency h-spice to simulate our BPSK demodulator. In this section, we show the simulation results of each part which we mention in 4.1 to 4.4. At first, transistor size of comparator and clipping circuits are showed in Figure 38. We have to sure that the common mode DC value of these two circuits. When input V_{c1} and V_{c2} common mode DC is ground, the comparator differential output 0 and 1 transition will occur at 133mV which is near to 0 volt, as shown in Figure 39 (a). Table 4 shows the input offset versus the comparator and clipping transition. If the input offset is higher than 0.6 volts, the comparator and clipping output transition will be at the same input voltage. This situation will make the later circuit malfunction.

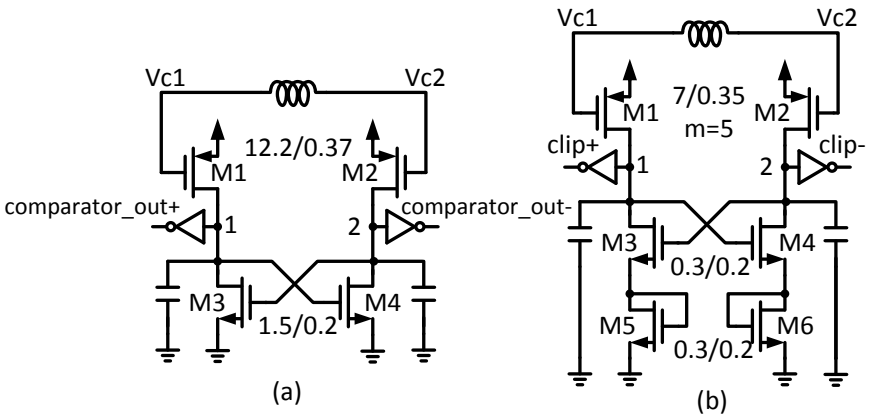


Figure 38. Comparator and clipping circuit with transistor size

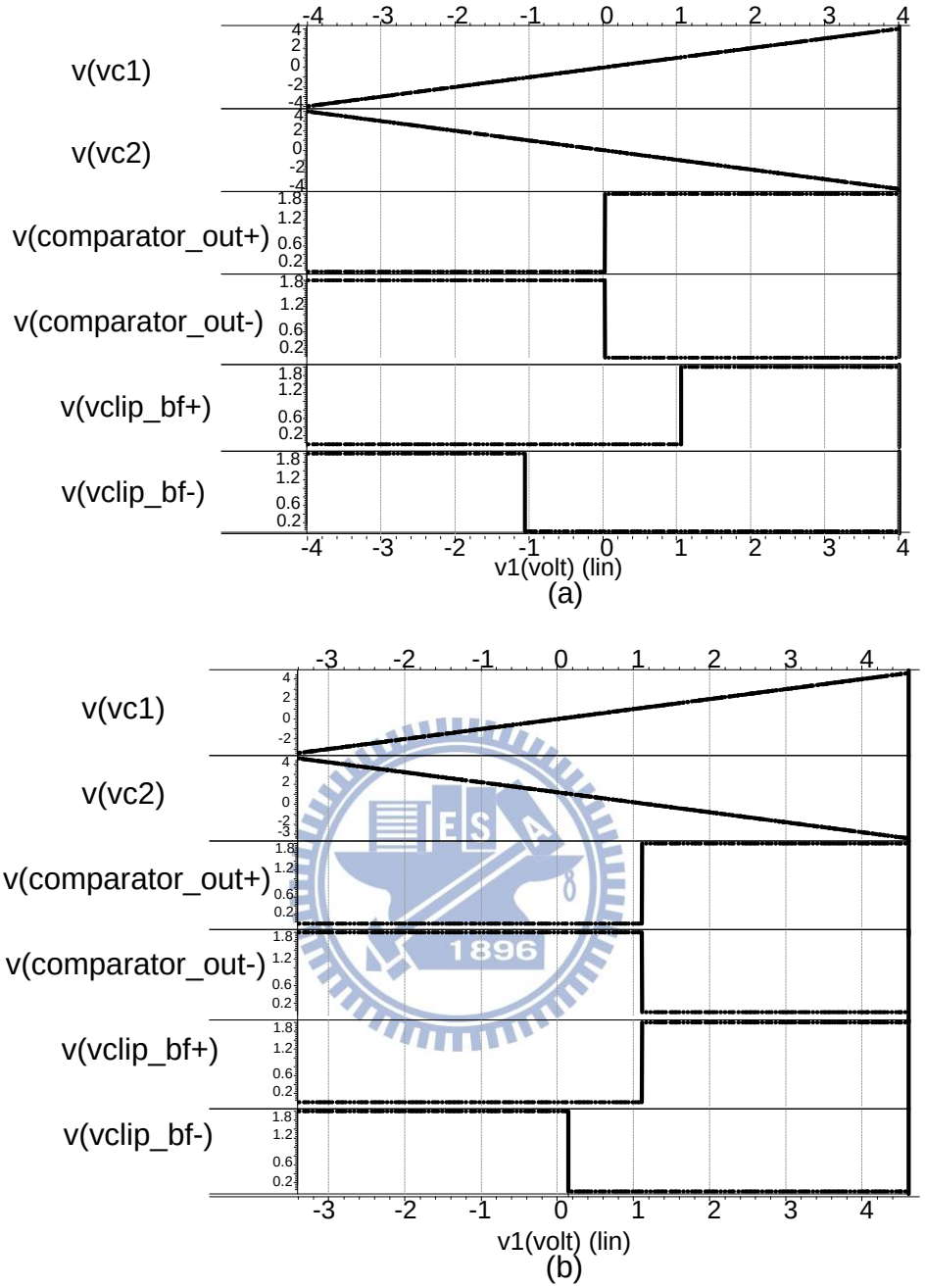


Figure 39. (a) Pre-simulation waveforms of comparator and clipping DC analysis at 0V offset (b) 0.6 V offset

Table 4. DC offset versus comparator and clipping transition voltage

offset (V)	comparatot_out+(mV)	comparatot_out- (mV)	clip+ (V)	clip- (V)
0	0.133	0.133	1.05	-1.06
0.6	1.11	1.11	1.11	-0.126

After the comparator and clipping circuit is determined, we have to ensure that the later circuit delay is smaller than our function limitation. There are four states

when we transmit data. They were one to zero、zero to zero、zero to one and one to one.

Case I: Symbol edge at transition of data from 1 to 1 is shown in Figure 40 (a). The enable circuit delay from comparator output to enable is less than 1.04ns. As we can see that the clip- is 4.3ns far from comparator output. The enable will be triggered before the transition of clip+. The reset generator circuit latency is less than 0.425ns. The comparator output transition is 3ns from clip+. So the reset signal is working at the right time here. Once the enable and reset signal are ready, data and clock will be right.

Case II: Symbol edge at transition of data from 0 to 0 is shown in Figure 40 (b). The enable circuit delay is less than 1.02ns. The clip- is 4.6ns far from comparator output. Enable is triggered before the transition of clip+. The reset generator circuit latency is less than 0.425ns. The comparator output transition is 0.8ns from clip+. Reset signal is working at the right time here. Once the enable and reset signal are ready, data and clock will be right.

Case III: Symbol edge at transition of data from 0 to 1 is shown in Figure 40 (c). Start circuit's latency is 0.64ns. The enable circuit delay is less than 1.04ns. The clip- transition is 7.4ns far from clip+ transition. The enable will be triggered after the transition of clip-. Correctness of the reset generator circuit is sure. Reset generator circuit output will be wrong if the comparator transition is complete before clipping transition, but the comparator transition won't happen in this case. So the reset signal is always right. Once the enable and reset signal are ready, data and clock will be right.

Case IV: Symbol edge at transition of data from 1 to 0 is shown in Figure 40 (d). The enable circuit delay from is less than 1.02ns. As we can see that the clip-

transition is 7ns from clip+ transition. Enable is triggered after the transition of clip-. It is sure that the correctness of the reset generator circuit. The reset generator circuit output will be wrong if the comparator transition is complete before clipping transition, but the comparator transition won't happen in this case. Reset signal is always right. Once the enable and reset signal are ready, data and clock will be right.

Figure 41 shows that the transient simulation of comparator and clipping output. Once the data transition occurs, one end of clipping differential output is low, and the other end has two pulses. One end of comparator differential output is high, and the other end is high.

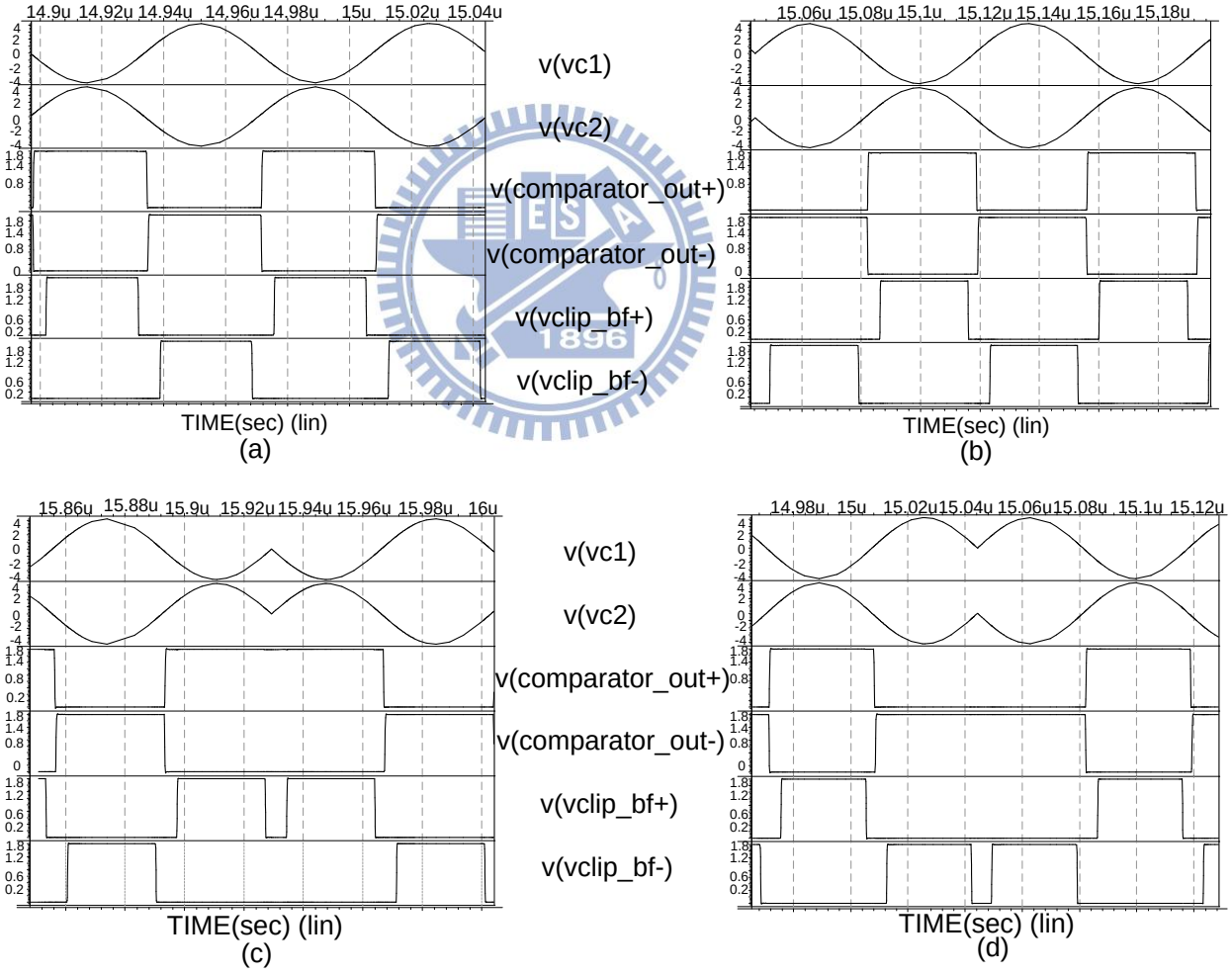


Figure 40. (a) Transition of data from 1 to 1 (b) Transition of data from 0 to 0 (c) Transition of data from 0 to 1 (d) Transition of data from 1 to 0

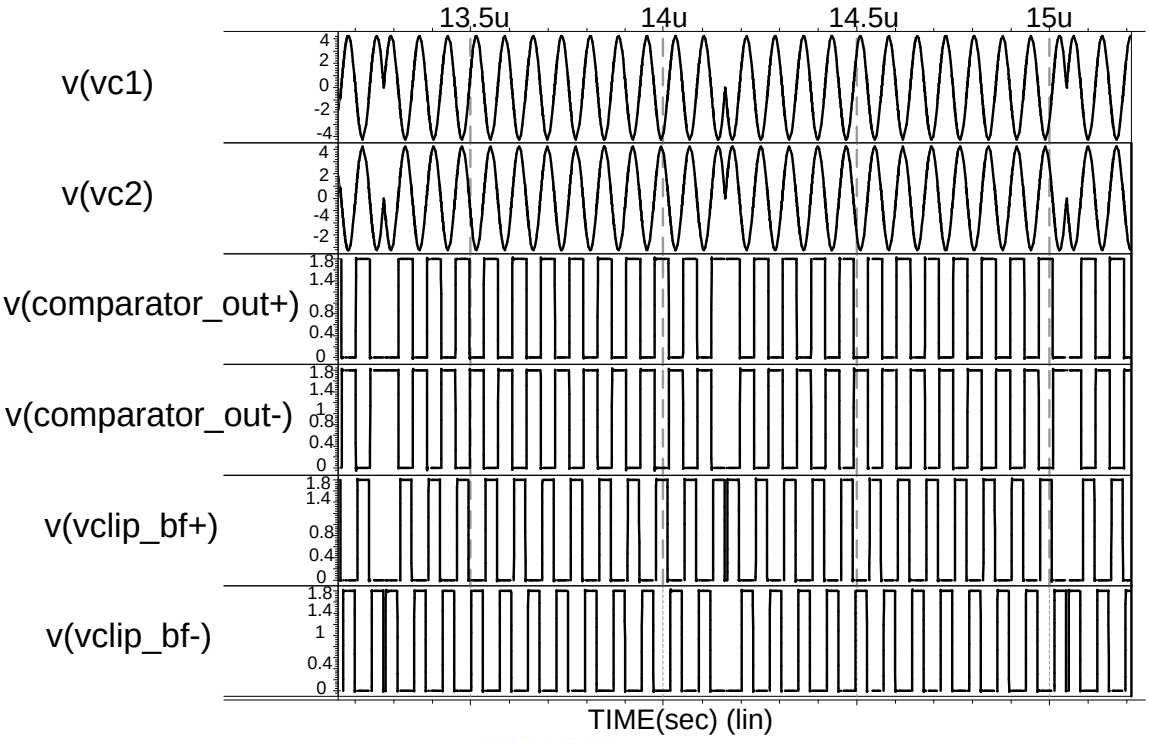


Figure 41. Pre-simulation waveforms of differential input, comparator and clipping output

At the beginning, we simulate the delay between power on signal and start signal. As we introduce in 4.2, when the power on is triggered by user, the start signal is triggered at the data transition (0 to 1 or 1 to 0). Table 5 shows the gate delay of this circuit. When the data is from zero to one, we can know that the start signal pulls to high after 0.64ns delay from clip+ and clip-. Figure 42 (a) shows the simulation waveform. When the data is from one to zero, we can know that the start signal pulls to high after 0.6ns delay from clip+ and clip-. Figure 42 (b) shows the simulation waveform.

Table 5. Delay of the start circuit with data from 1 to 0 or 0 to 1

Data=1-0			Data=0-1		
input	output	rise_delay (ns)	input	output	rise_delay (ns)
clip	start	0.64	clip	start	0.6

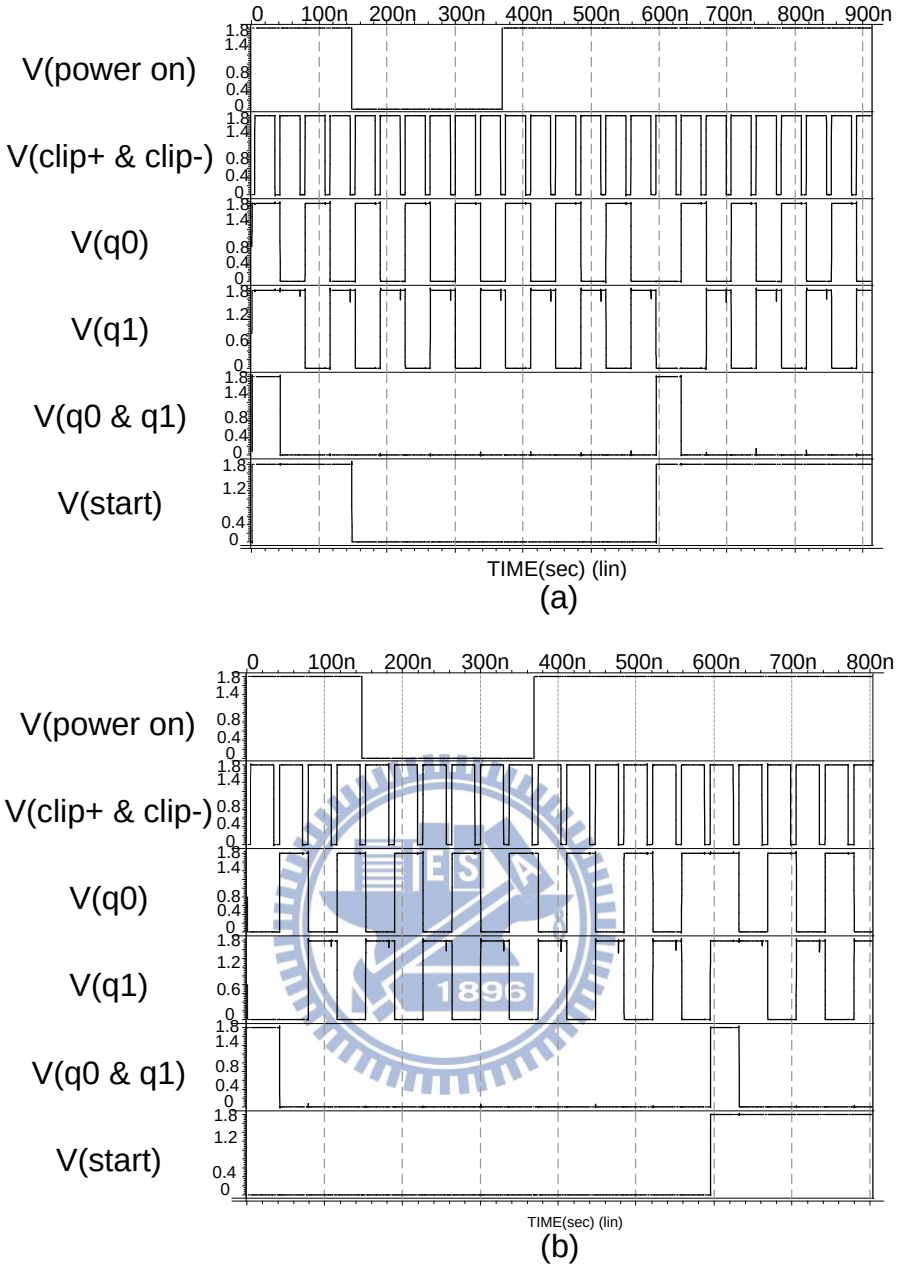


Figure 42. (a) Pre-simulation waveform of start circuit which the data is from 0 to 1 (b) Pre-simulation waveform of start circuit which the data is from 1 to 0

After the start signal is obtained, there is a 3 bit counter to generate the enable signal. The start signal is always trigger at symbol edge. If the start signal is triggered when the transmitted data is one, the total gate delay from comparator_out+ and comparatot_out- are 1.04ns and 0.77 ns separately. Figure 43 (a) shows the simulation waveform. If the start signal is triggered when the transmitted data is zero, the total gate delay from comparator_out+ and comparatot_out- are 0.74ns and 1.02 ns

separately. Figure 43 (b) shows the simulation waveform.

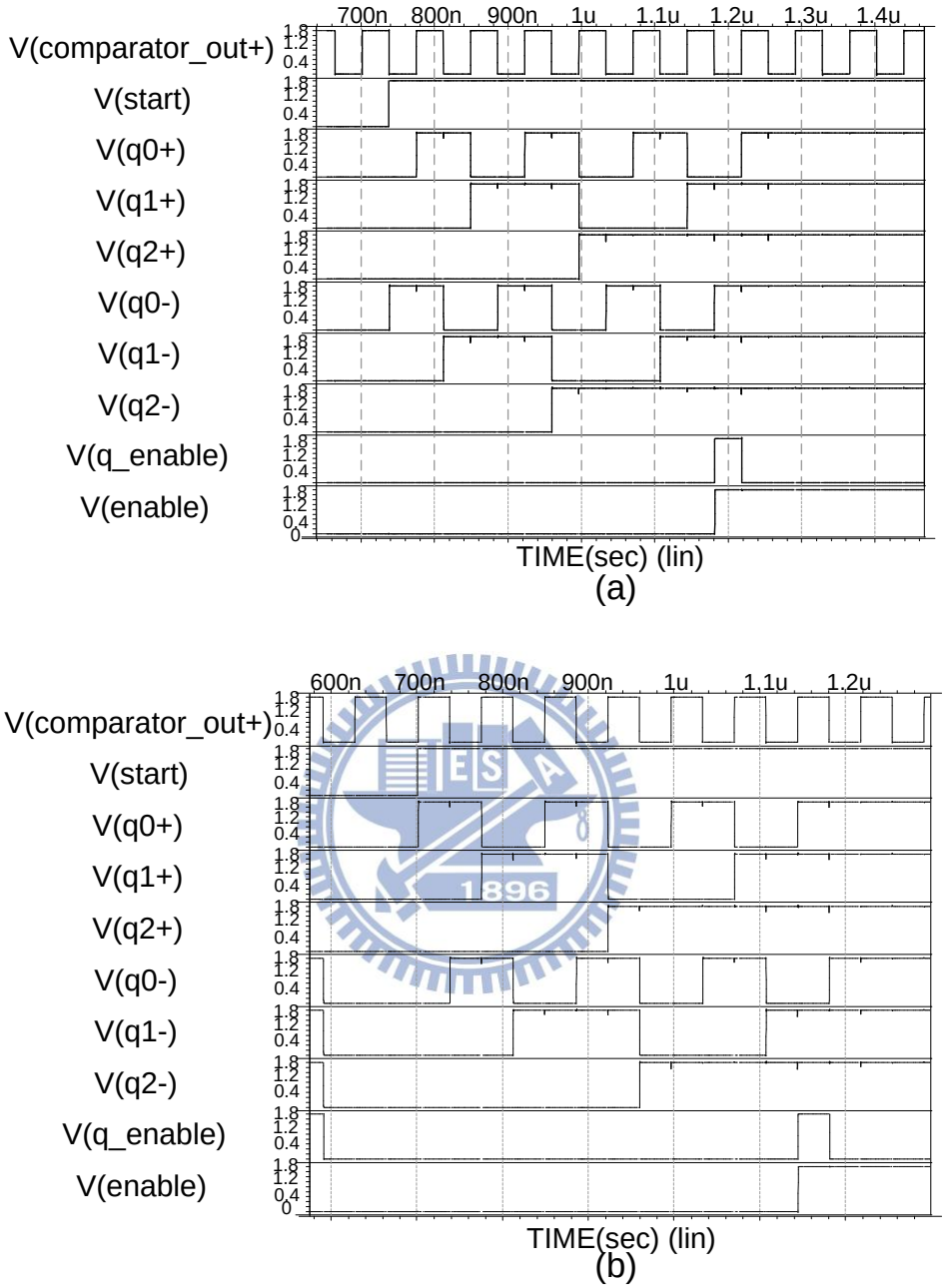


Figure 43. (a) Pre-simulation waveform of enable circuit which the data is 0 (b) Pre-simulation waveform of enable circuit which the data is 1

Table 6. Delay of enable circuit with data 1 or 0

Data=1			**Data=0**		
input	output	rise_delay (ns)	input	output	rise_delay (ns)
comparator_out+	enable	1.04	comparator_out+	enable	0.74
comparator_out-	enable	0.77	comparator_out-	enable	1.02

Once the enable signal is high, the reset generator is triggered. The reset circuit's inputs are clip+ and clip-. The rising delay of the circuit is 0.391ns and the falling delay is 0.425ns. Figure 44 (a) shows the simulation waveform. Table 7 and Table 8 show delay of reset generator and data and clock recovery respectively.

Table 7. Delay of the reset circuit

input	output	rise_delay (ns)	fall_delay (ns)
clip+	reset	x	0.425
clip-	reset	0.391	x

Table 8. Delay of the data and clock circuit

input	output	rise_delay (ns)	fall_delay (ns)
comparator_out+	clock	0.495	x
comparator_out+	data	0.62	0.894
comparator_out-	clock	0.448	x
comparator_out-	data	0.606	0.91
reset	clock	x	0.492

When the reset signal is obtained, DCR circuit is triggered. Delay from comparator_out+ to clock is 0.495n, and delay between comparator_out- and clock is 0.448n. comparator_out+ and comparator_out- delays to data are 0.62ns and 0.606ns separately. We know that the reset will pull these DFFs to low level to make the clock transition. Delay from reset to clock is 0.492ns. Figure 44 (b) shows the functionality of the DCR circuit.

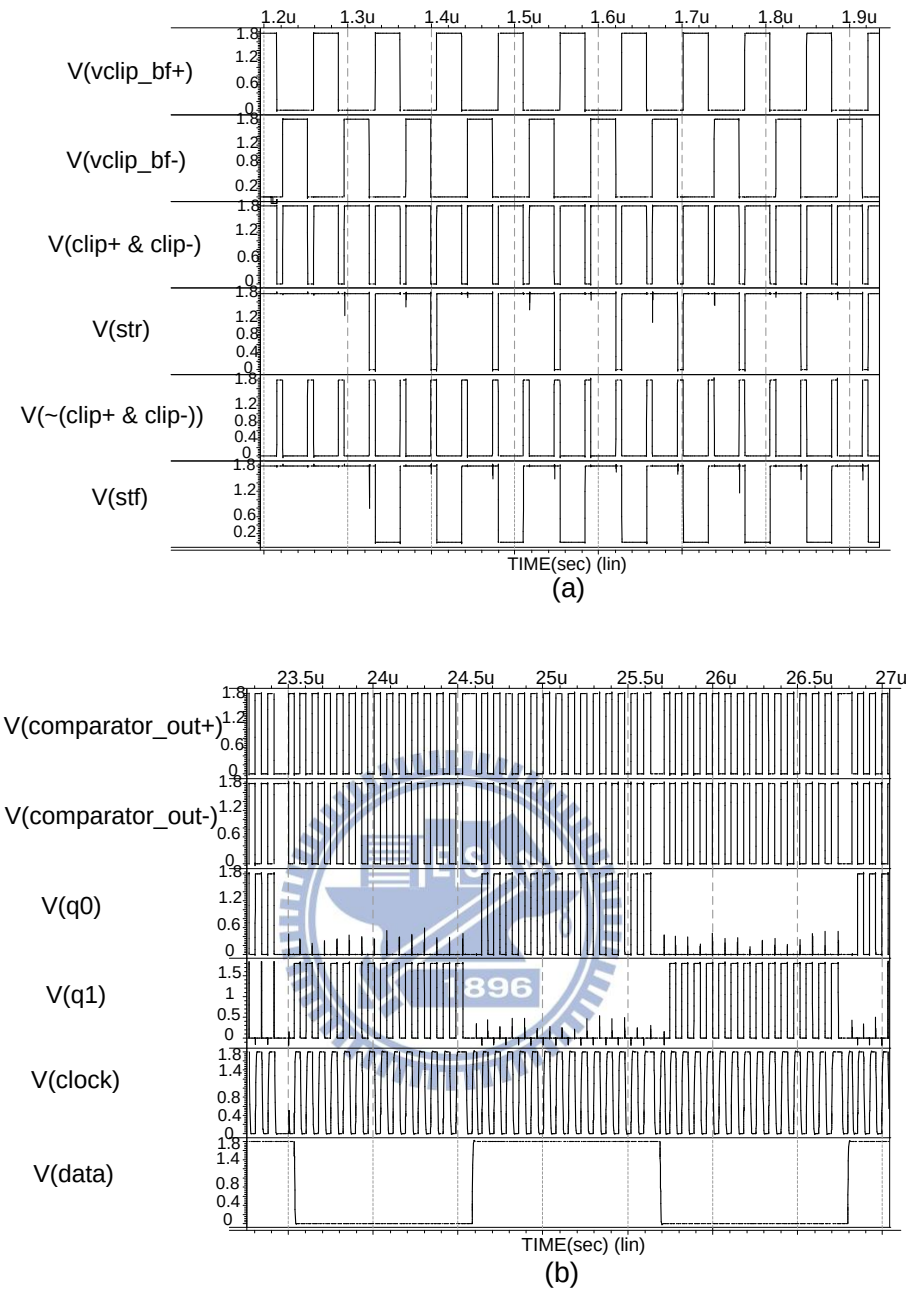


Figure 44. (a) Pre-simulation waveform of reset circuit (b) Pre-simulation waveform of data and clock circuit

4.6 Layout Consideration and Post-layout Simulation

Comparator and clipping layout is shown in Figure 45 , fully symmetrical layout style is employed for the differential signal path. Owing to the comparator and clipping circuit are fully differential, we layout these circuit using common centroid to improve the matching, as shown in Figure 45. For avoiding noise from the circuit,

every circuit is rounded by guard ring. The enable circuit, reset generator circuit and DRC circuit are digital circuits. We know that the circuit delay is very important here, so we make the path of these circuits to be as short as we can.

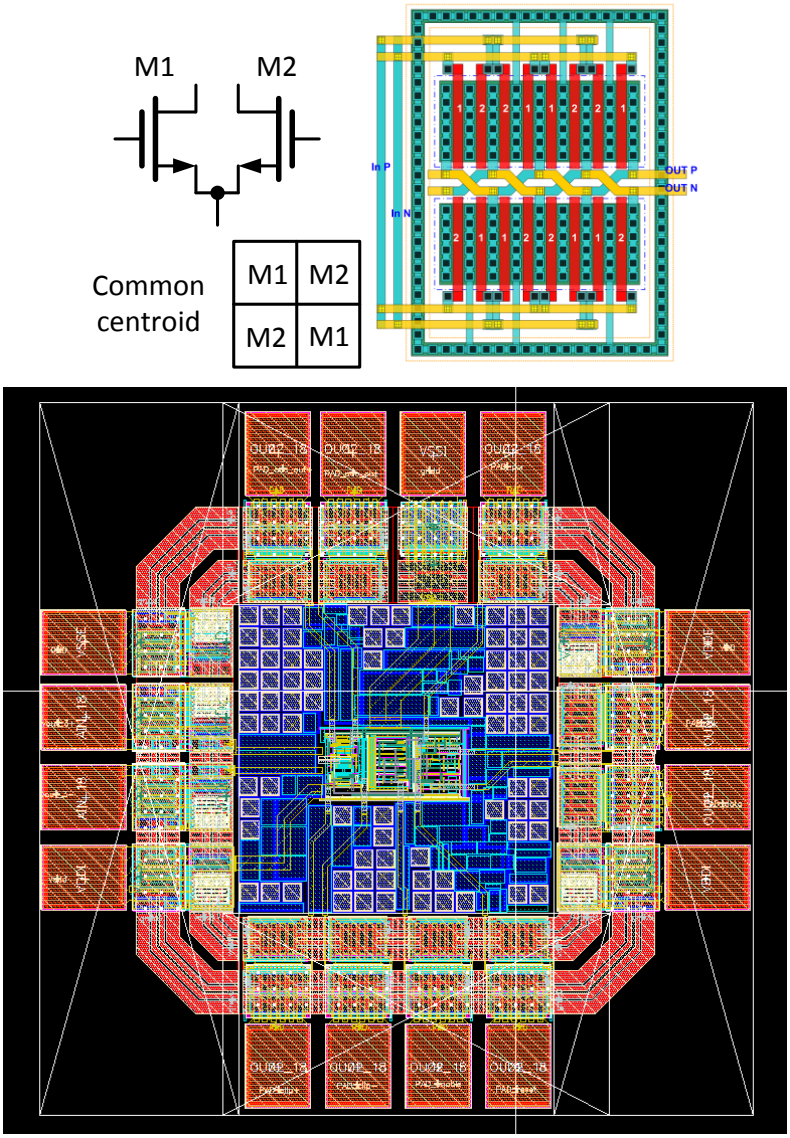


Figure 45. (a) Common centroid (b) BPSK demodulator layout

Figure 46 shows simulation result of demodulator without connected the coil we design. Input BPSK modulated waveform is ideal, and the clock and data is demodulated successfully. We assume that the output loading is 0.2 pF which is the probe loading, so these output signals have the RC charge and discharge phenomenon.

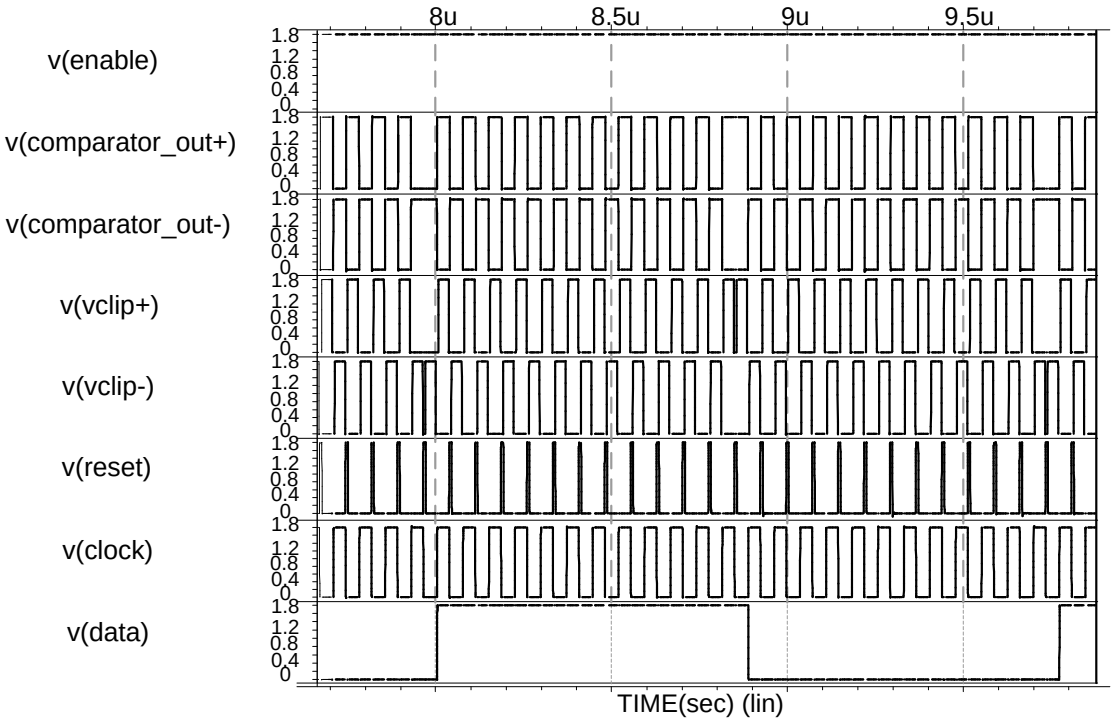


Figure 46. Post- layout simulation of reset generator and DCR circuit with ideal BPSK modulated input

Owing to the coil bandwidth, distortion of received BPSK waveform occurs. The higher the data rate, the higher the distortion produce. Figure 47 shows the function of data and clock. Figure 48 shows the comparison of primary data and demodulated data at 678 kbps data rate.

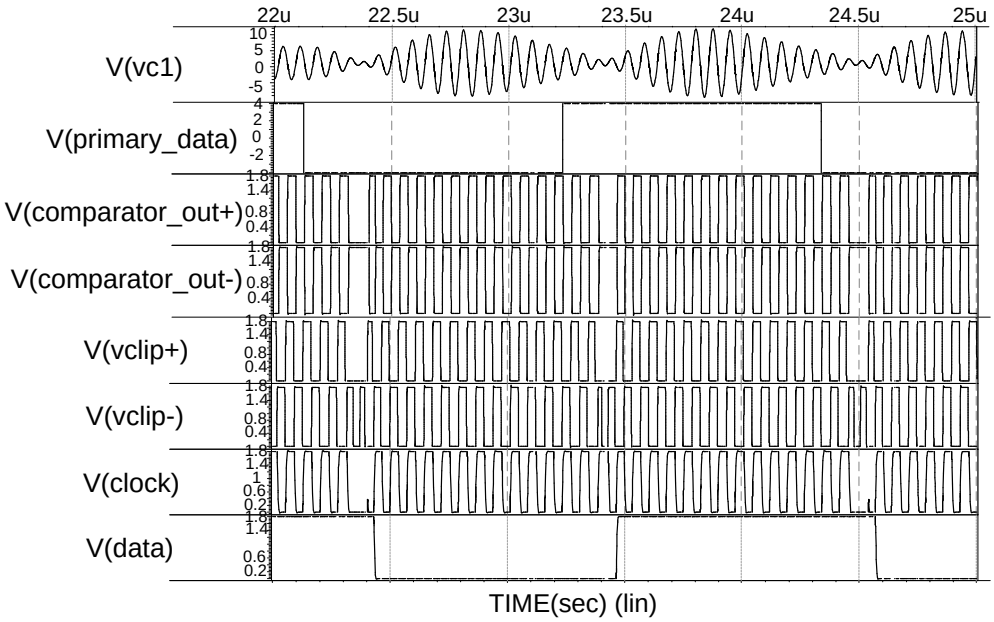


Figure 47. Post- layout simulation of DCR circuit

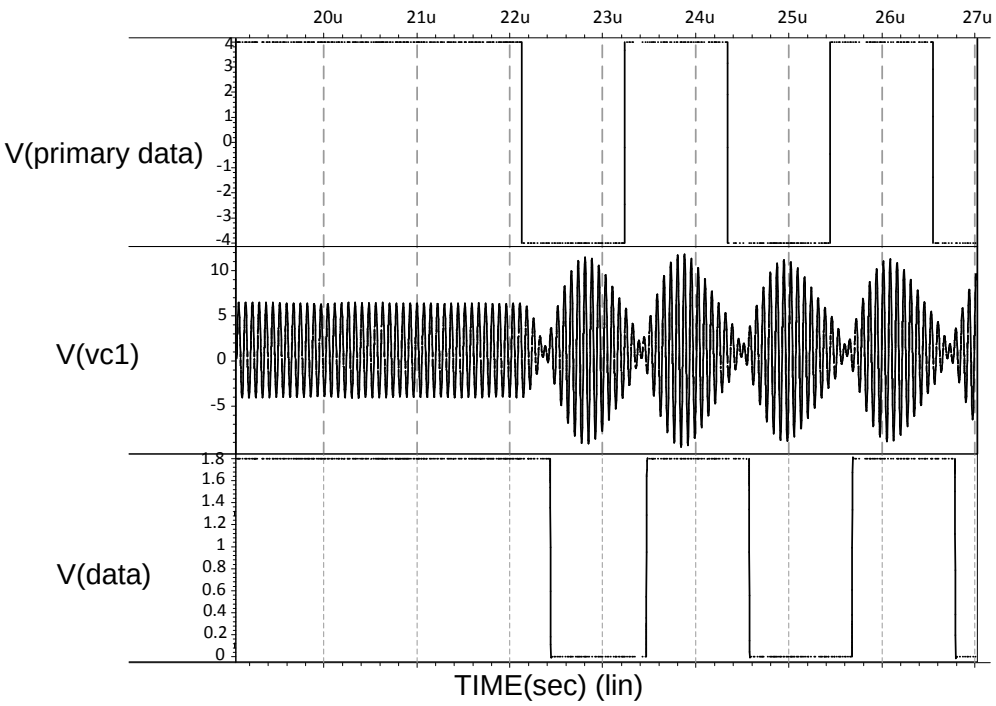


Figure 48. Post- layout simulation of BPSK demodulator with coil at 678 kbps

Table 9 shows the power consumption of the demodulator circuit from pre-simulation and post-simulation. Owing to the probe loading, the buffer power consumption increase severely.

Table 9. Power consumption of the demodulator in pre-simulation and post-simulation

	Pre-simulation	percent	Post-layout simulation	percent
Reset generator & Power on & Data and Clock Recovery (μW)	40.7	20.1%	50.94	19.82%
Comparator & Clipping (μW)	98	48.4%	115.9	45.1%
Buffer (μW) (loading = 0.2p)	63.8	26.75%	85.18	33.14%
Core (μW)	138.7	68.49%	166.84	64.92%
Total (μW)	202.5	100%	252.02	100%

Chapter 5

Test Setup and Experimental Results

5.1 Test Board Design

In order to achieve the expected performance of the prototype chip, the test board must be designed for some considerations. The four-layer PCB for the test chip is shown in Fig. The top layer is used to place components such as switch. The second layer is VDD layer, and the third layer is GND layer. The bottom layer is used to routing the signal also. In order to avoid parasitic effect of the package in high speed operation, the raw die is directly connected to PCB by bonding wires. The output of regulator is decoupled by a 10 μF tantalum capacitor for the lower-frequency noise, and high-frequency noise are decoupled by capacitors of 0.1 μF and 1μF placed at each supply pin of the prototype chip. We use two PCBs to verify the demodulator function and whole system function. The first project is SMA input for better matching. Figure 49 shows the top layer and bottom layer. The power layer is not available here. The second project is used to connect the coil, and the rectifier output is used for connecting with rectifier. The power layer is separate to two parts. One is used for supplying VDD and GND to the circuit, and another area is not connected to VCC and GND, because the area is for coil placing, we don‘t want the coupling from VCC or GND to affect the coil input waveform, as shown in Figure 50.

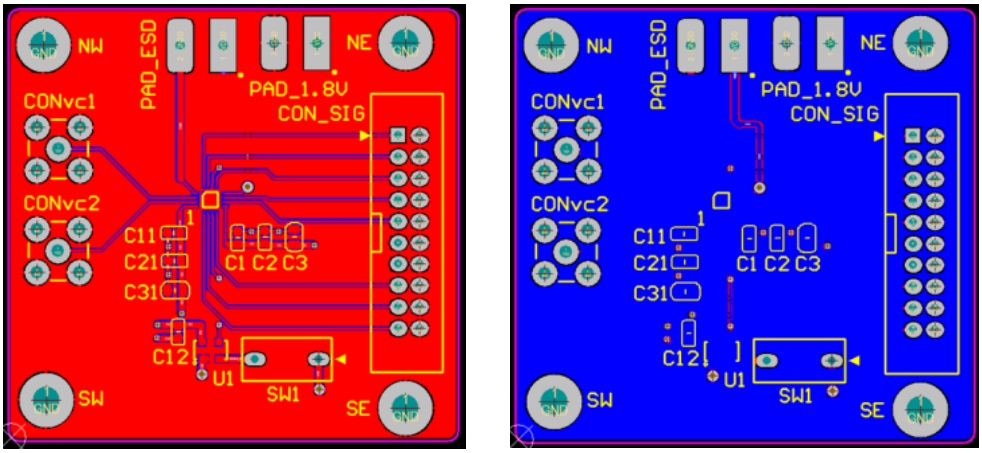


Figure 49. (a) Top layer of PCB board for data verification (b) Bottom layer of PCB board for data verification

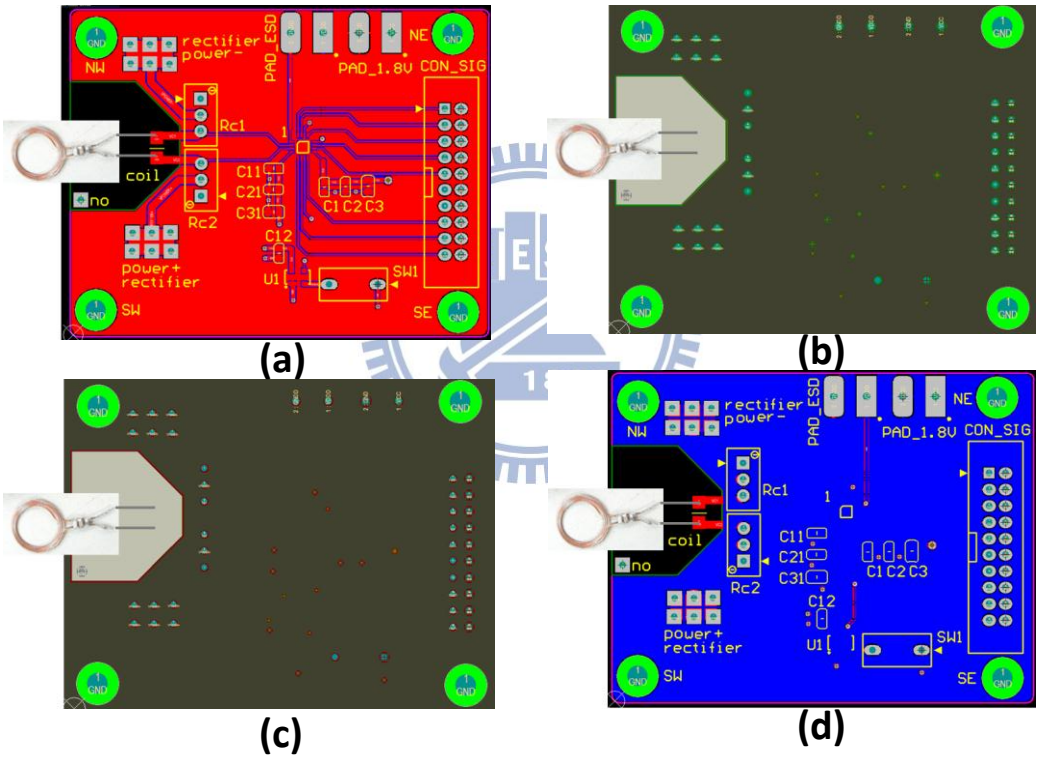


Figure 50. (a) Top layer of PCB board for system verification (b) VDD layer of PCB board for system verification (c) GND layer of PCB board for system verification (d) Bottom layer of PCB board for system verification

5.2 Test Environment Setup

A Schottky diode bridge rectifier connects to internal coil. The DC output of the rectifier supplies stable 1.8V to BPSK demodulator circuit. The test setup,

measurement environment, and chip implementation are shown in Fig. 5, the diameter and thickness of the external (internal) coil are 4.2cm (1.8cm) and 1.1cm (0.2cm), respectively. The spacing between two coils is 1cm. The die size of the chip is 0.668x0.666 mm^2 and the core area is 0.139x0.07 mm^2 in a 0.18μm CMOS process.

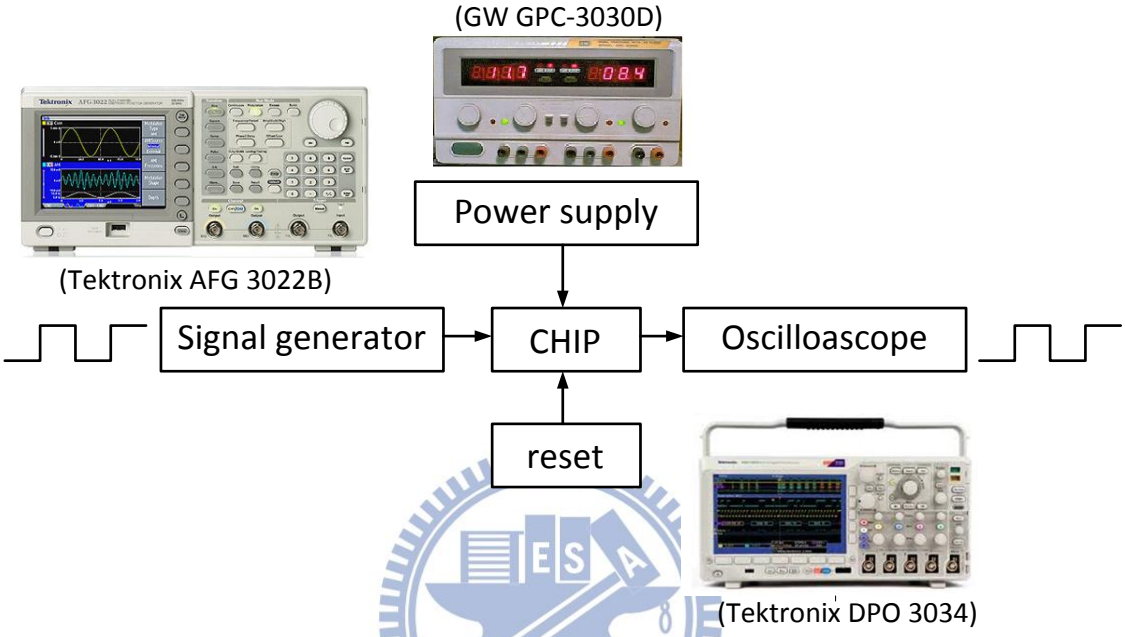


Figure 51. Test environment of data verification

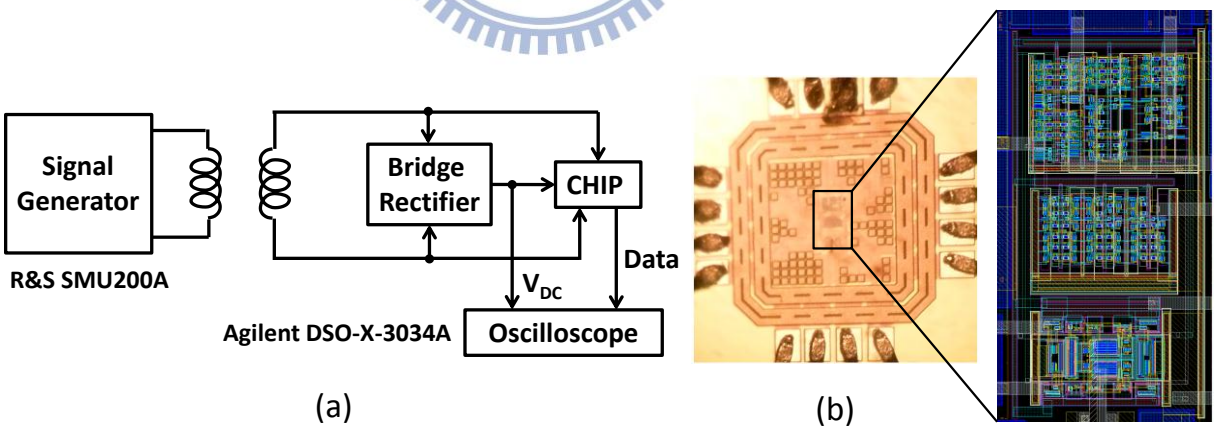


Figure 52. (a) Test environment of system verification (b) Die photo

Figure 51 is test environment of the BPSK data demodulator chip. Input BPSK modulated signals are generated by Tektronix AFG 3022B signal generator. Two channel signal generator can supply two in-phase sine waves at 13.56MHz. For data verification, the PCB input is used connected by SMA connector. The output is

display on the Agilent DSO-X-3034A. The GW GPC-3030D power supply is used to bias the buffer which is used for primary coil.

Figure 52 shows the test environment of the test chip. The input BPSK modulated signal generated by Rohde & Schwarz signal generator. The data rate is setup from 400bps to 25 Mbps, and our design can be test under the range. The signal also can supply a 13.56MHz carrier for wireless transmission. The output if signal generator is connected to primary coil by BNC transmission line. The power and data is transmitted by a pair of coil which we introduce in section 3.2. The internal coil receives the modulated wave and sent to the demodulator and rectifier. The rectifier convert modulated wave to DC value which is the VDD supply for demodulator. The demodulator output clock and data is displayed on the oscilloscope (Agilent DSO-X-3034A). The GW GPC-3030D power supply is used to bias the buffer which is used for primary coil. The additional power supply is no need for our internal system. The only power source is from a pair of coil. We also can connect our demodulated data to the Rohde & Schwarz signal generator to test the bit error rate.

Figure 53 and Figure 54 show the testing environment of the data and the whole system respectively. Figure 55 (a) shows the data verification. Figure 55 (b) shows the demodulator which is connected to the coil. Figure 56 shows the whole system including coil, rectifier and demodulator.

The BER testing mechanism is provided by Rohde & Schwarz signal generator. The demodulated is connected to the BER testing inputs to compare with the signal generator baseband data.

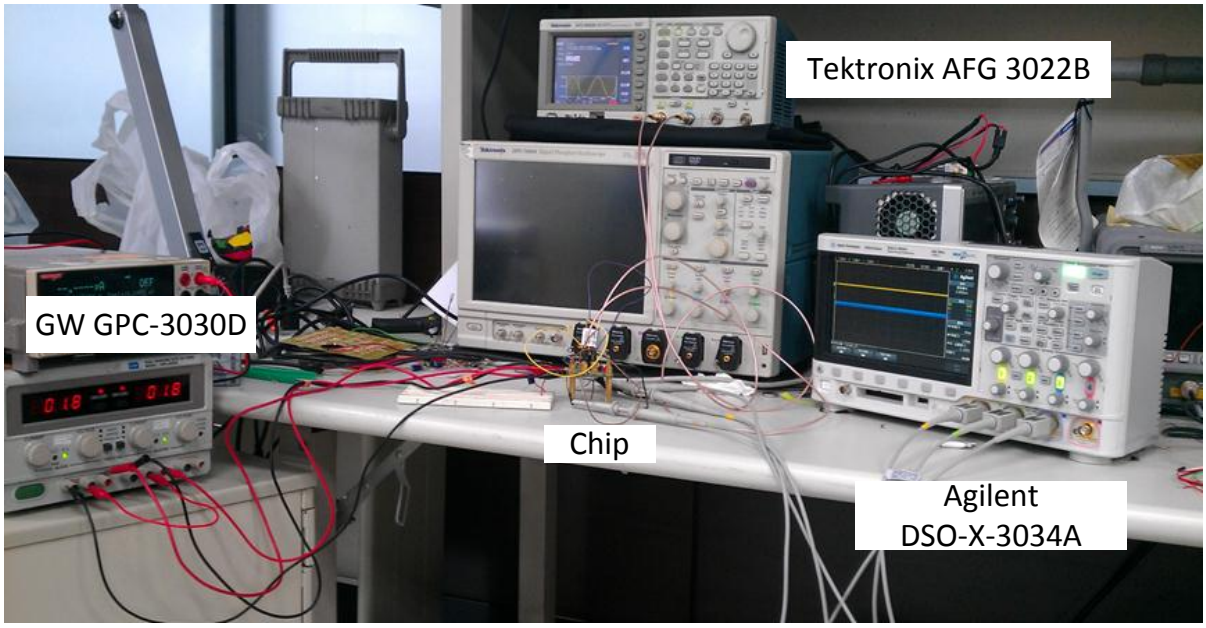


Figure 53. Photo of the testing environment in data verification

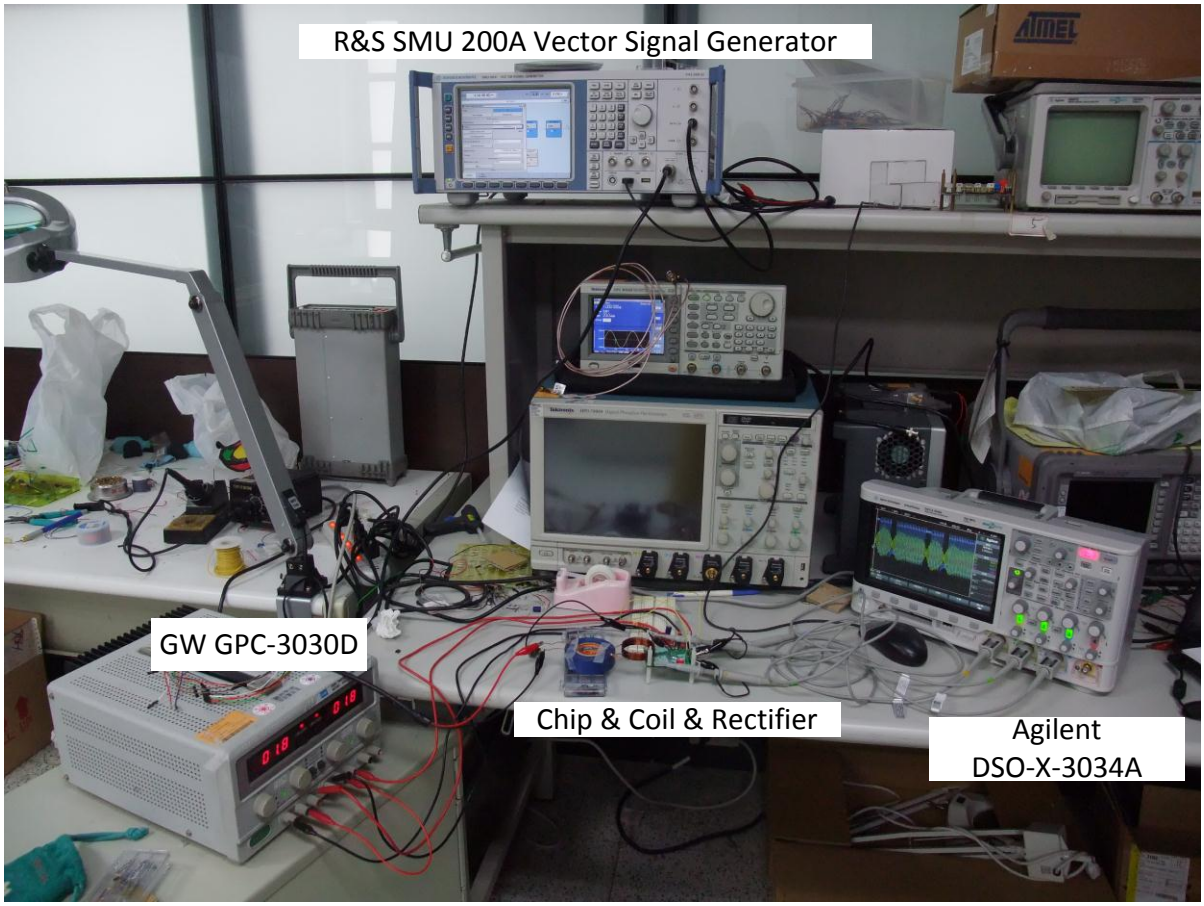
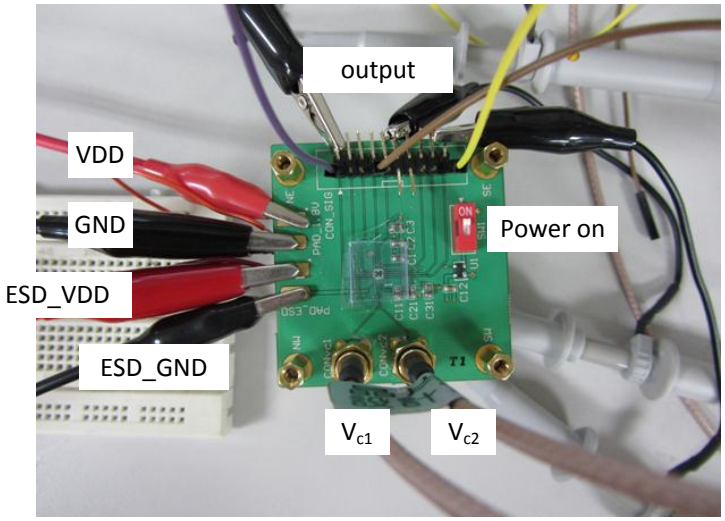
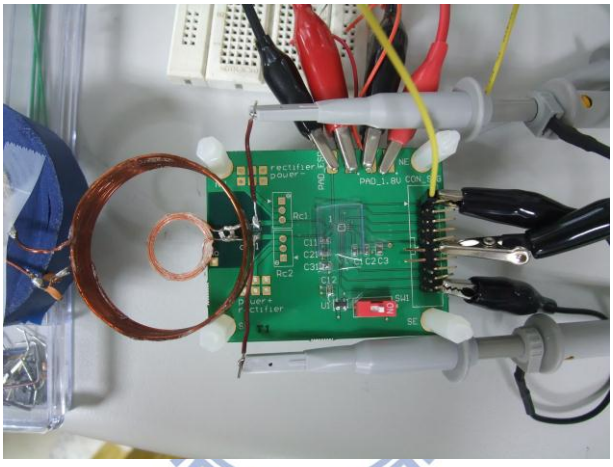


Figure 54. Photo of the testing environment in system verification



(a)



(b)

Figure 55. (a) Measurement of data verification (b) Measurement of the coil and demodulator

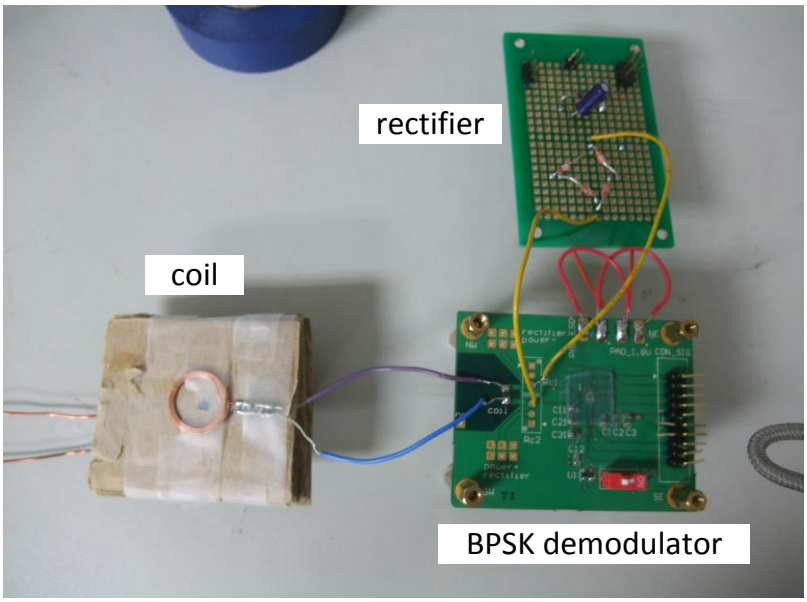


Figure 56. Measurement of rectifier, coil and demodulator

5.3 Measurement Results

5.3.1 Function of BPSK Demodulator

After we setup a bridge rectifier using schottky diode (1ss106) which connects to internal coil, the DC output supplies stable 1.8 volts to BPSK demodulator circuit. Figure 57 shows some testing outputs of the demodulator chip. The Figure 57(a) is the com, and Figure 57(b) is the comparator+ and clipping+ output. Figure 57(c) is the comparator-and clipping-output. Figure 57(d) is the clip differential output and the reset signal.

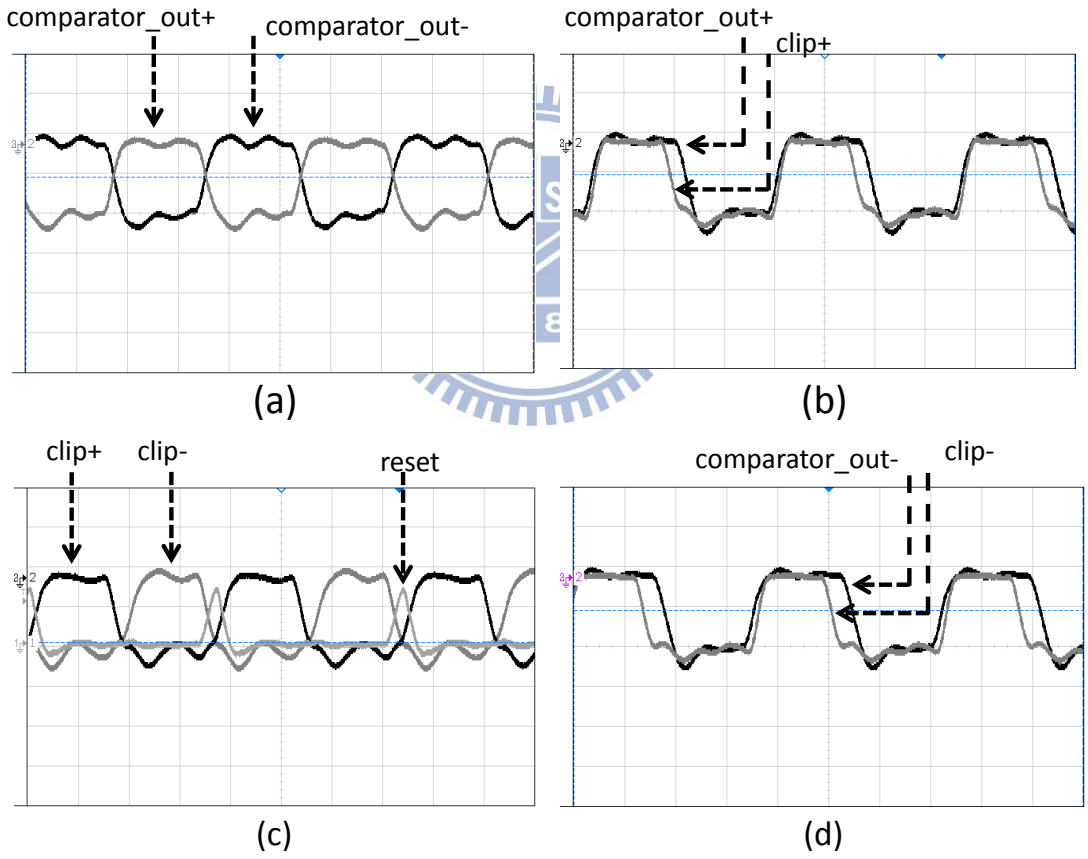


Figure 57. (a) Comparator differential output (b) Comparator_out+ and clip+ (c) Comparator_out- and clip- (d) Clip differential output and reset

Figure 57 shows a screen shot of the measurement result of data transmission. The signal is attenuated by 10 times for detecting larger-amplitude signals. Therefore,

the measured coil input voltage of 580mVpp is equivalent to received voltage of 5.8Vpp on channel 2. The 1.8V DC voltage from rectifier is measured on channel 3. Once the fixed pattern is verified, the random data must be verified, too. The Rohde & Schwarz signal generator can generate the PRBS (Pseudo Random Binary Sequence) signals. The circuit design of the PRBS is shown in Figure 58. If we use the PRBS9, there will be 9 stages of left shift registers. The maximum length is 2^9-1, and it will repeat the sequence periodically. The function of this Figure 58 is $1+x^5+x^9$. Figure 59 shows the demodulated data and V_{DC} at highest data rate 678 kbps. Channel 1 is the demodulated data, and channel 2 is the data which is external and base band data.

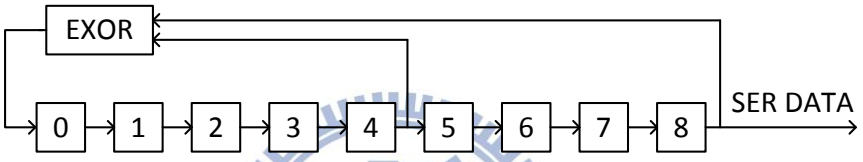


Figure 58. Function of PRBS9 (Rohde & Schwarz signal generator)

Figure 59. Waveform of coil receive input, demodulated data and baseband data (from signal generator) at 678 kbps with PRBS9 pattern

5.3.2 Power Efficiency

The received signals are modulated at a carrier frequency of 13.56MHz carrier frequency, resulting in a non-single tone wave. Owing to the bandwidth of coil, the

input of the demodulator is not ideal, as shown in Figure 60. The upper line is ideal waveform, and the lower line is the coil input transmitted by the coil we design in the section 3.2.

Figure 61 shows that the rectifier drop-out voltage varies according to the supply voltage and modulated data rate. The drop-out voltage increase with the increased supply voltage and it increases with increased data rate.

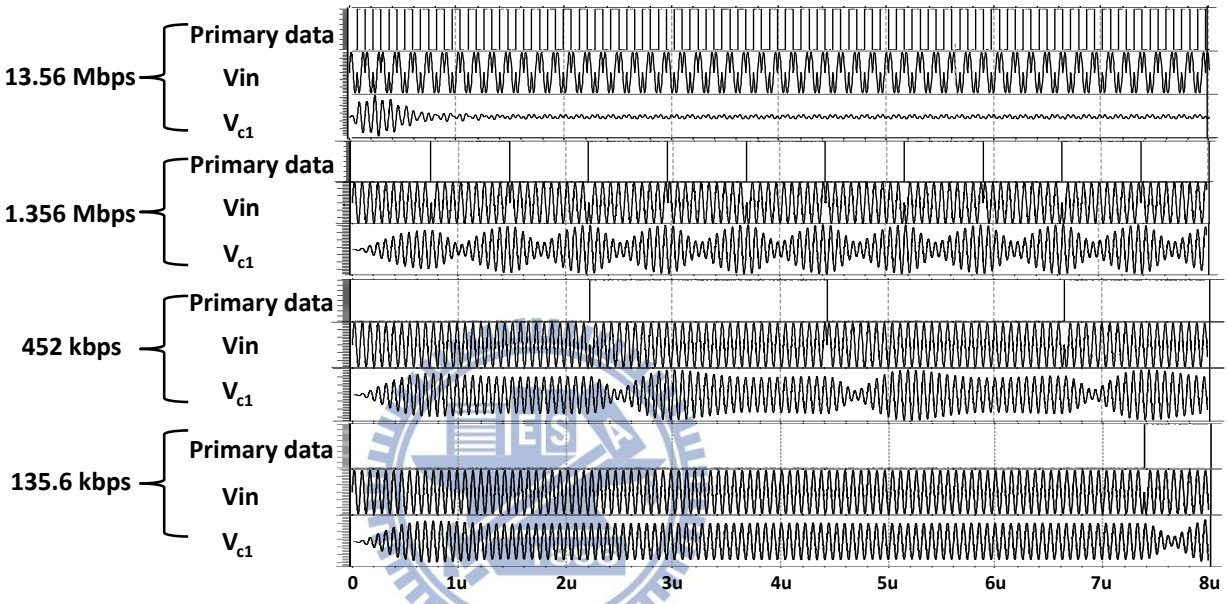


Figure 60. Received peak-to-peak voltage by internal coil at different data rate

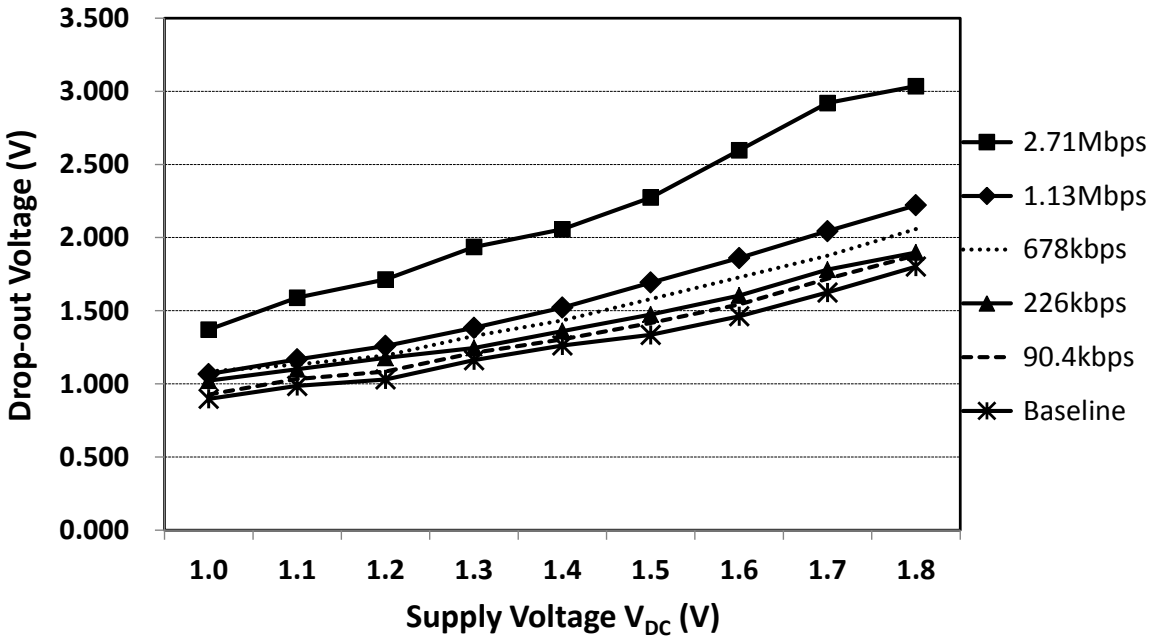


Figure 61. Equivalent drop-out voltage versus V_{dc} at different data rate

Once the rectifier drop-out voltage is measured, the rectifier efficiency is derived also as shown in Figure 62. We can see that the rectifier efficiency is 70% at sine-wave, but when we apply a different data rate, the rectifier efficiency varies as well. If the data rate is low, the efficiency is higher. With the increasing of data rate, the efficiency decreases slightly.

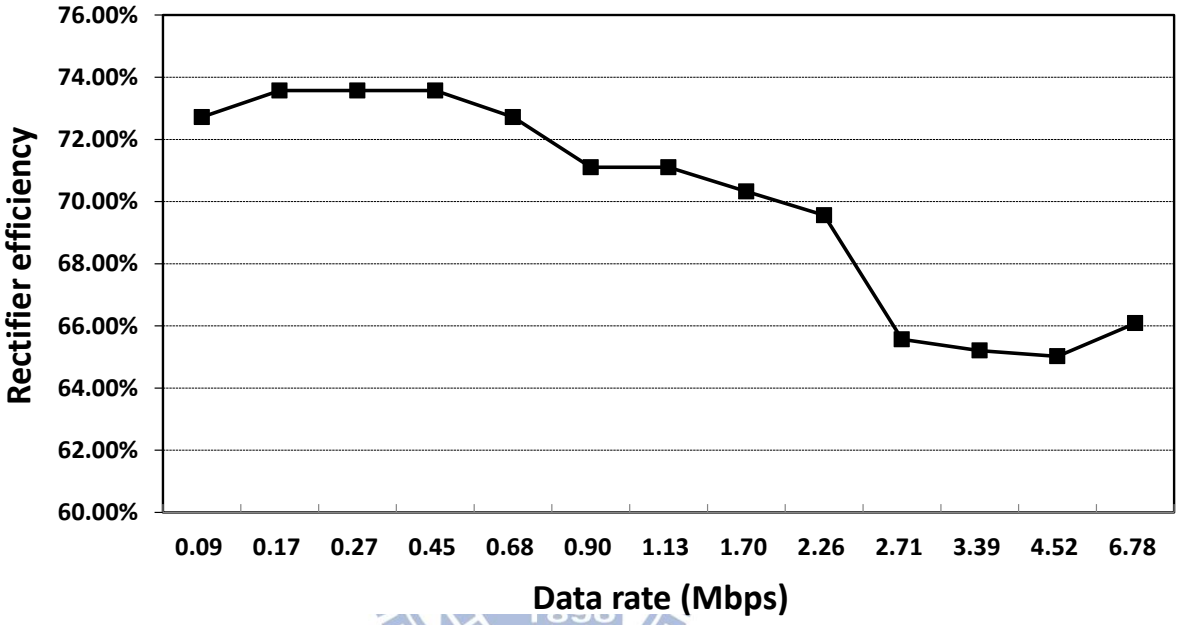


Figure 62. Rectifier efficiency at different data rate with a stable 1.8 VDC

Figure 63 shows the received power at different data rate. When the data rate is higher, and the received power is higher to make the rectifier output 1.8 volts. We use current probe which is shown that 5mV represents 1mA. We multiply the differential voltage where is Vc1 minus Vc2 with the current to get the average power. The value on oscilloscope is five times of real power (Avg-FS) we received. It's obviously that the primary input power varies with the data rate. If we want to supply a stable 1.8 volts DC at different data rate, higher primary power is expected at higher data rate as shown in Figure 64.

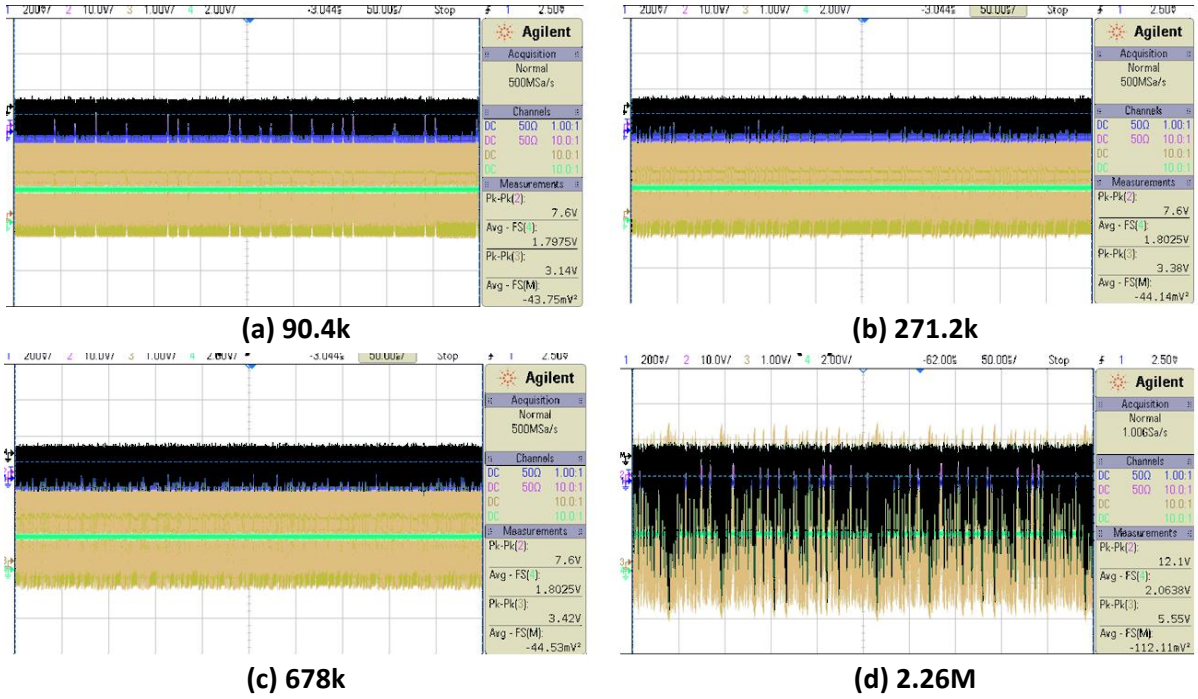


Figure 63. (a) Received power at 90.4 kbps (b) Received power at 271.2 kbps (c) Received power at 678 kbps (d) Received power at 2.26 Mbps

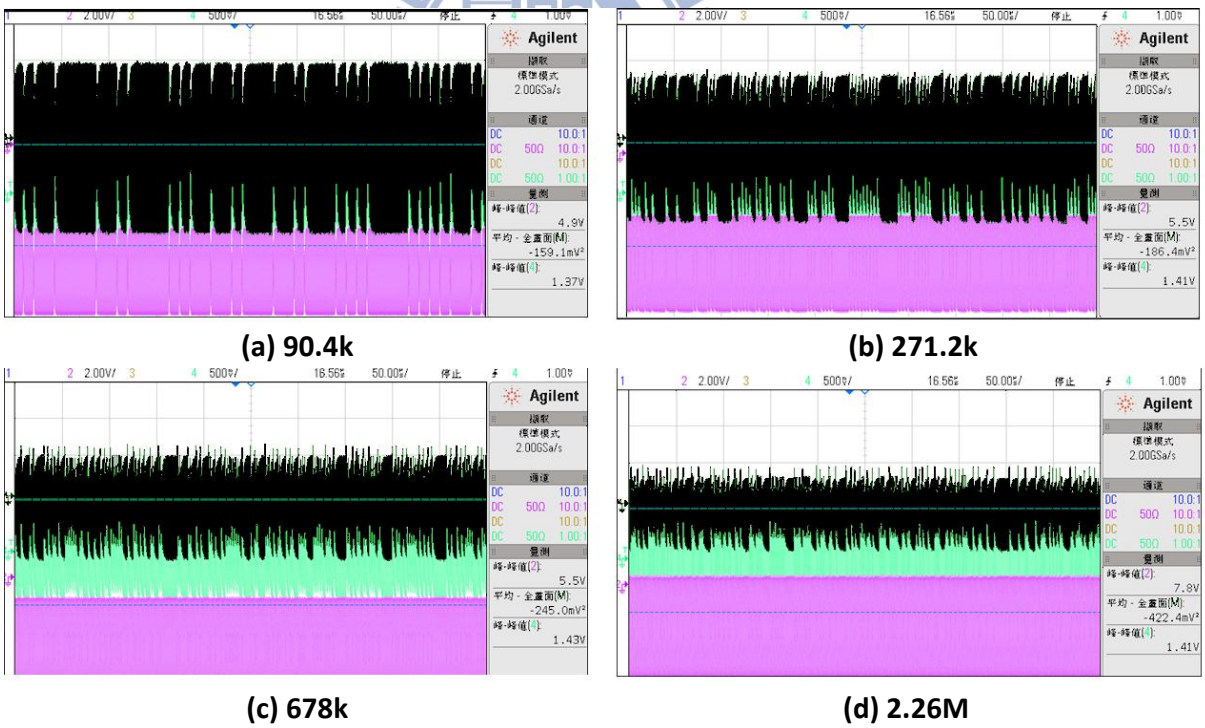


Figure 64. (a) Transmitted power at 90.4 kbps (b) Transmitted power at 271.2 kbps (c) Transmitted power at 678 kbps (d) Transmitted power at 2.26 Mbps

The degradation of drop-out voltage is used to adjust the transmit power to compensate the power loss. To supply a stable 1.8V DC power for different data rates,

appropriate primary (external) input power must be chosen. To maintain a constant received power, more primary power is needed for higher data rate, resulting in lower power efficiency. Figure 65 shows the required primary power and corresponding power efficiency for the change of data rate. The dotted line is calculation results, and the solid line is measurement results.

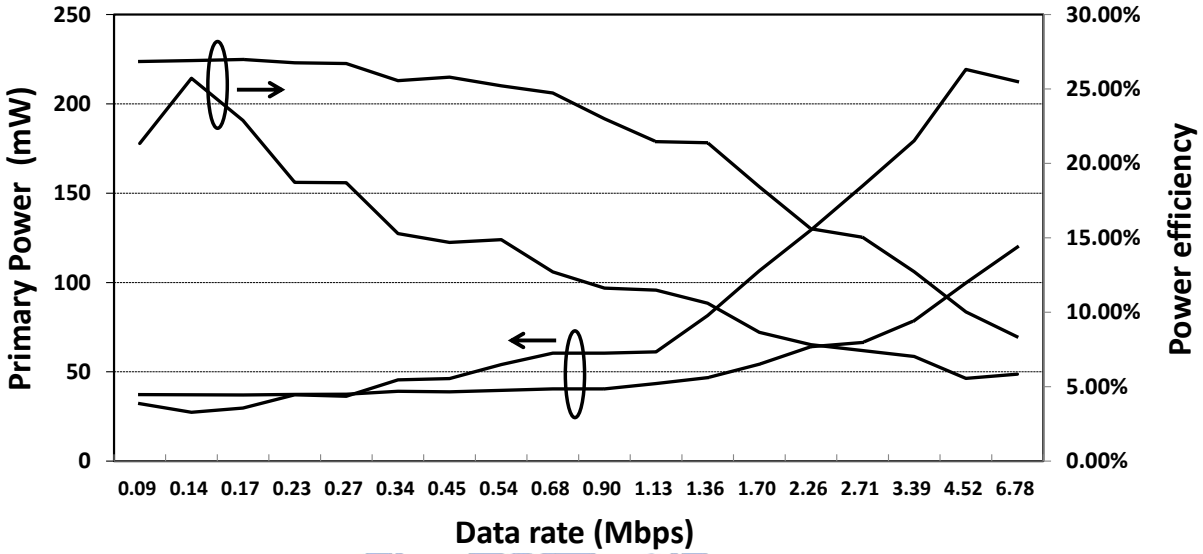


Figure 65. Primary power and power efficiency versus data rate

5.3.3 Bit Error Rate

Figure 66 shows that BER at AWGN channel. In theory, high SNR may convert to outstanding BER performance. But it's impossible to measure the wonderful signal as we estimate because of the additional additive disturbances man-made noise. It may make the unexpected error appear.

According to this demodulator design, common mode of received signal will be limited. When data rate is higher than 904 kbps (13.56MHz/15cycles), the common mode is out of the range the circuit can tolerant. It will produce a serial error during transmission. As we can see that the modulated data will be wrong at 904 kbps, as shown in Figure 67.

Once the receive power at different data rates is known, the channel capacity can

be derived from (2). When data rate achieves 1.13 Mbps, the received power decreased, leading to degradation of the channel capacity. This causes unreliable data transmission. Therefore, data rate must be lower than 1.13 Mbps according to the measurement result. In theory, higher SNR contributes to higher BER performance, but it is impossible to achieve the theoretical bound because additional noise sources are not taken into consideration. The unexpected noise causes extra transmission errors. Figure 68 shows the relation of channel capacity and data rate. The maximum data with near-errorless performance (BER < 10^{-9}) can be achieved at data rate of 678 kbps. The BER = 10-9 bound is limited by the test infrastructure.

Figure 69 (a) is bit error rate value at different data rate which we measure, so we can prove that the maximum data rate we transmit with a better BER is 678 kbps (13.56 MHz/20cycles). When the E_b/N_0 is 29 dB, the output data is recorded for more than $1x10^9$ bits with no error found. However, due to the limited recording length of the analyzer, the exact BER is not obtained. Figure 69 (b) shows the bit error rate of 904 kbps data rate. Accurate relation of data rate and BER is not measured between 678 kbps and 904 kbps.

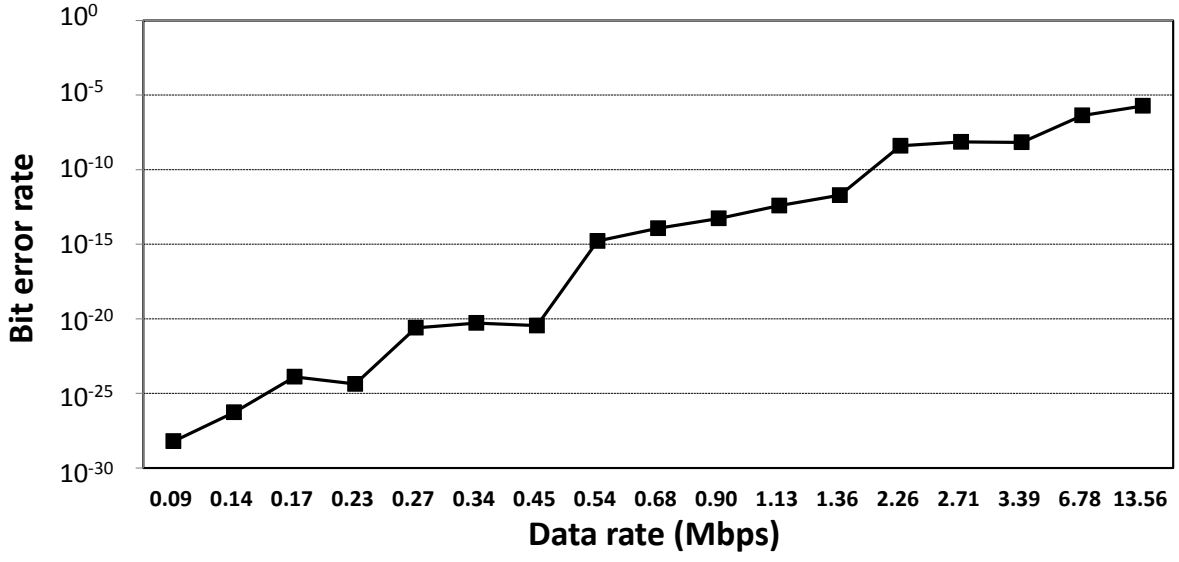


Figure 66. Bit error rate versus data rate

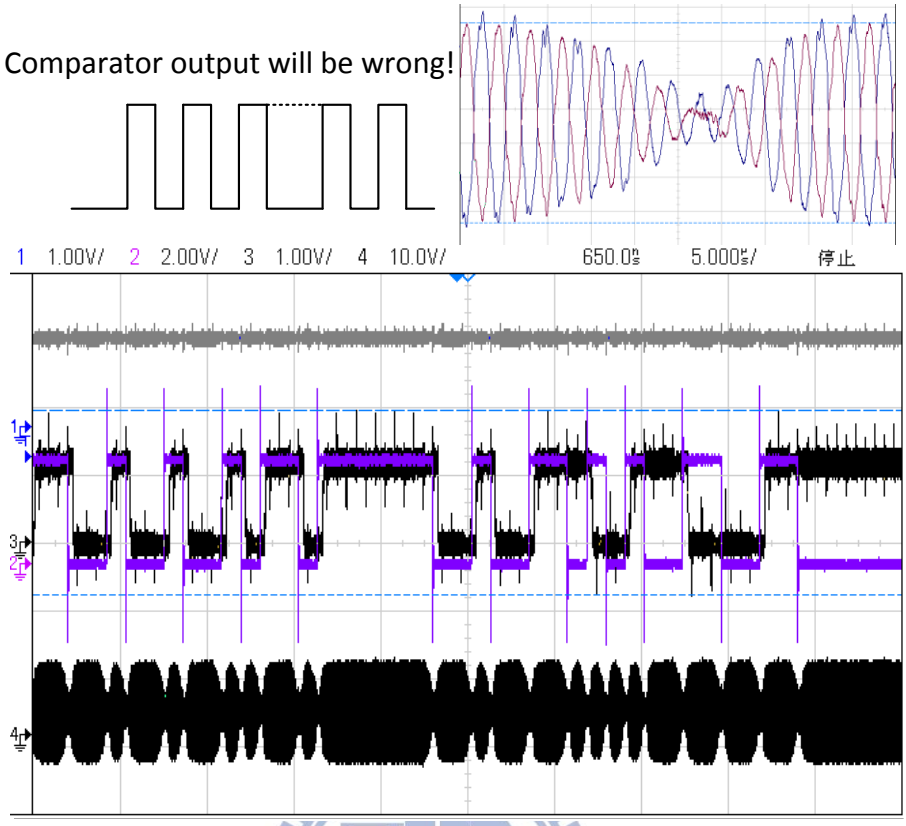


Figure 67. Frequent errors of the demodulator at 904 kbps with the coil

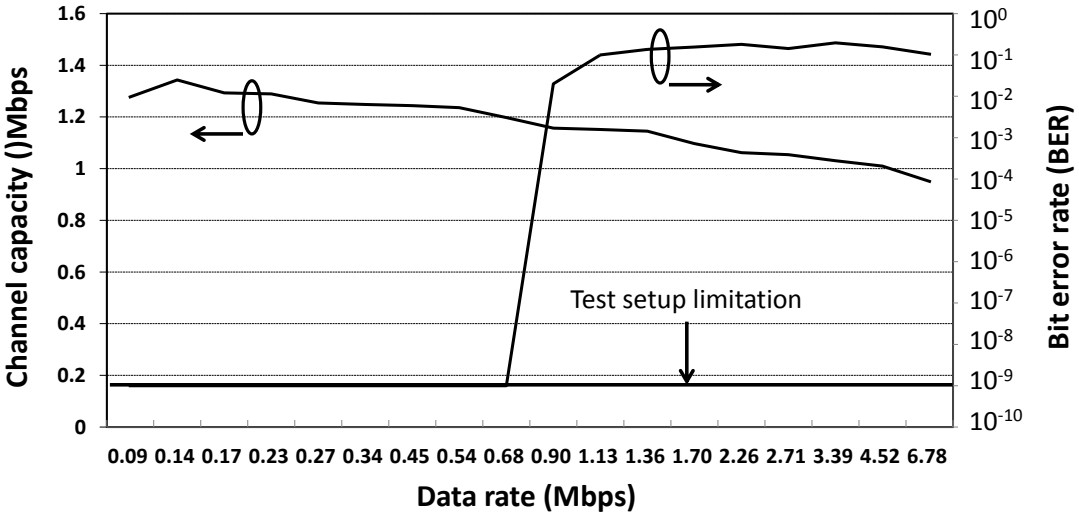
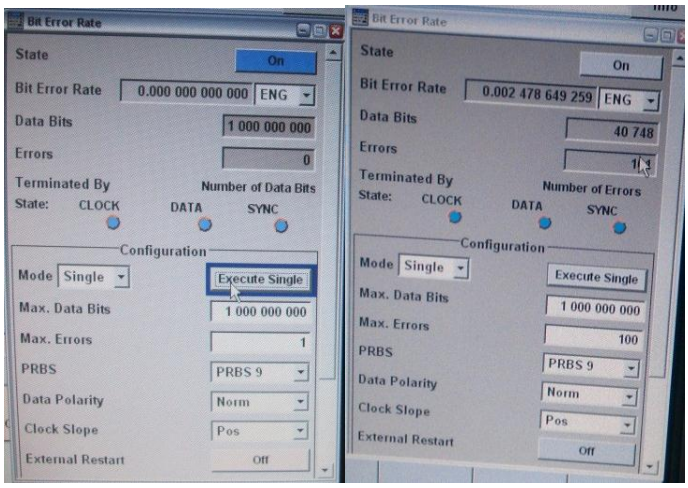


Figure 68. Bit error rate and channel capacity versus different data rate



(a) (b)

Figure 69. (a) BER testing result at 678 kbps (b) BER testing result at 904 kbps

5.4 Discussion

In order to find out the problems about the incorrect work of the prototype chip, the real waveform of digital output must be checked as well as the supply voltage for the chip powers. The digital output can be observed through oscilloscope directly, and we can compare the waveform of these data with ideal simulation results to verify that whether the chip working is correct or not. The digital output of measurement is shown in Figure 70. Compared with the output waveform of simulation in Figure 70, it is obvious that the ripples occurs in measurement results, hence the noise floor must be higher than estimated.

Owing to the narrow bandwidth of channel, the DC common mode will vary with the different data sequence at the data rate higher than 904 kbps. Even the DC common mode is in the demodulator input range, the common mode DC will be varied with the length of data sequence as shown in Figure 71. Data will be transmitted in a better BER is under tha678 kbps data rate.

Our circuit is used for seizure detection implant circuit, so for reducing the heat in the brain, the implanted circuit is designed to low power as we can. For voiding the

additional circuit (another correlation circuit) to improve the data stability, we have to ensure that the demodulator have good BER at one data rate. The final data rate we test which has high BER performance is 678 kbps. Output data is recorded for more than $1x10^9$ bits with no error found. However, due to the limited recording length of the analyzer, the exact BER is not obtained.

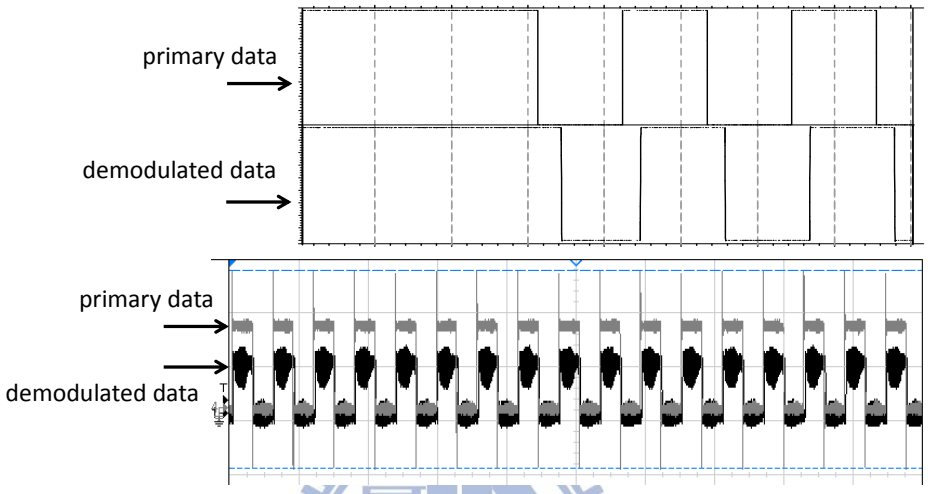


Figure 70. Pre-simulation and measurement of the primary data and demodulated data

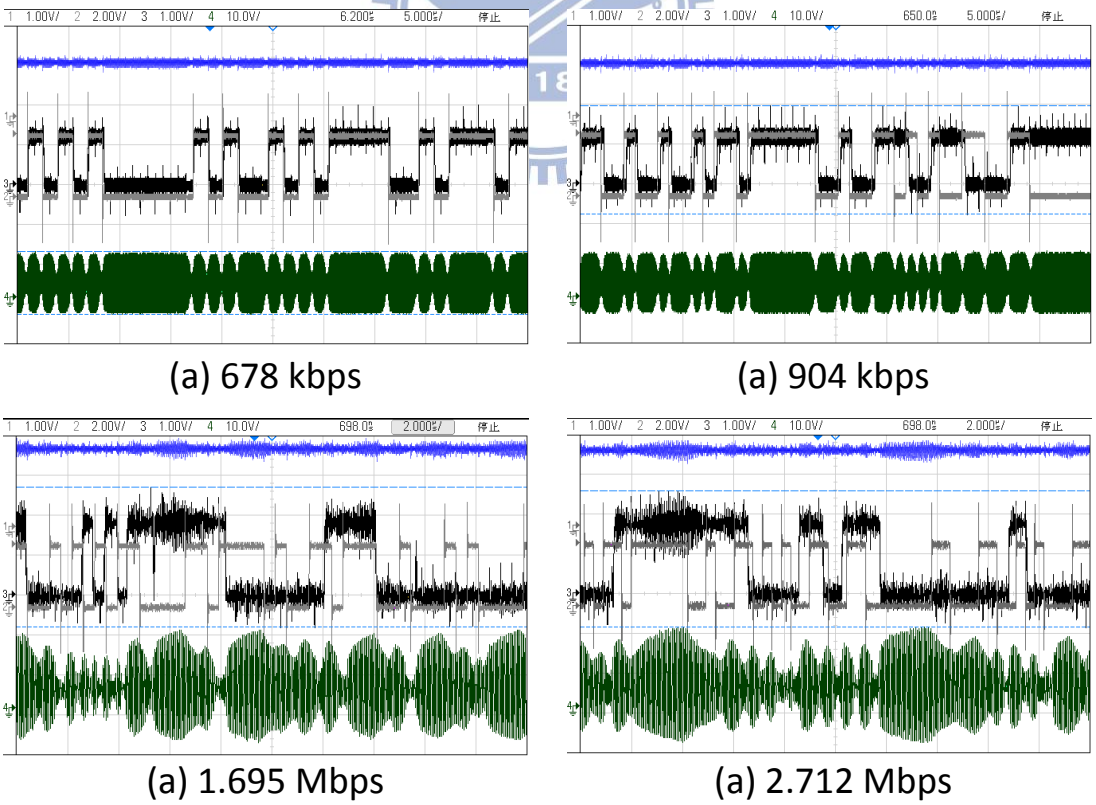


Figure 71. Received input varied common mode DC value at different data rate

5.5 Summary

A performance comparison with prior clock-recovery-based BPSK demodulators is listed in Table 10. Except this work, other designs are only verified in simulation and coils are not included in the system. The data rate to carrier frequency ratio of this work achieves 100% with comparable power consumption.

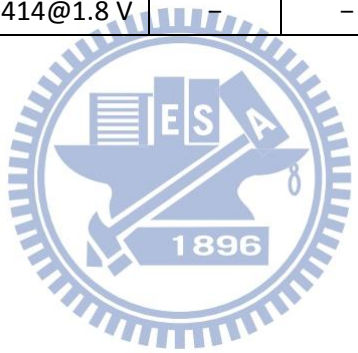
Table 11 shows a performance comparison of this work with other demodulators for biomedical implants. Most of the designs are designed for data transmission only. Compared with designs with capability of data and power transmission [18][19], this work dissipates less power and the core area is smaller. Reference [18] and [19] show the telemetry which transmits data and power using one coil as shown in Table 11. As we can see, power consumption of demodulators in [18] and [19] are large than this work. Power transmission of [18] and [19] are high because of short distance of coil pair. Reference [21] shows a low-power demodulator using digital circuits. After we normalize 4MHz to 13.56MHz, the power consumption of [21] is about 200μW excluding buffer, and this demodulator power consumption is about 196μW excluding buffer. When compared with other BPSK demodulators dedicated to data transmission, this design still has the lowest power consumption normalized by carrier frequency.

Table 10. Comparison of the related BPSK demodulator

	Data Transmission			Power consumption (μW)	CMOS Tech. (μm)	
	Data rate (Mbps) Mod: BPSK	Carrier freq. (MHz)	Data rate to carrier ratio			
This work	13.56	13.56	100%	(chip) 294 @ 1.8 V (core) 191 @ 1.8 V	0.18	measured
[22]	0.8 / 4 / 8 / 20	0.8 / 4 / 8 / 20	100%	46 / 93 / 148 / 310 @ 1.8V	0.18	simulation
[26]	10	10	100%	119 @ 1.8V	0.18	simulation
[27]	10	10	100%	232 @ 1.8V	0.18	simulation

Table 11. Comparison of the related data telemetry

	Data Transmission		Power consumption (μW)			CMOS Tech. (μm)	Area (mm^2)	Jouel per bit (mJ /Mbps)
	Data rate (Mbps)	Carrier freq. (MHz)	Power consumption (mW)	Coil distance (cm)	Received power (mW)			
This work	13.56	13.56	(chip) 294 @ 1.8 V (core) 191 @ 1.8 V	1	5	0.18	(chip) 0.445 (core) 0.097	281.7
[18]	1.69	13.56	5 @3.3V	0.22	22.5	0.5	0.1	2958.8
[19]	1.69	13.56	2.3 @3.3V	0.22	22.5	0.5	0.293	1361
[20]	0.02	13.56	3 @3.3V	–	–	0.5	1	15000
[21]	0.8	4	0.059@1.8 V	–	–	0.18	0.004	250
[28]	2.5	10	0.485 @3.3V	–	–	0.35	0.161	194.16
[29]	0.02	13.56	0.594@1.8 V	–	–	0.18	1.35	29680
[9]	1.12	13.56	0.414@1.8 V	–	–	0.18	0.148	369.64



Chapter 6

Conclusion and Future Work

6.1 Conclusion

A clock-recovery-based BPSK demodulator for data and power telemetry is designed and implemented for biomedical implantable devices. A symbol detector is used instead of oscillator circuitry for power and area reduction. The measurement results show that the rectifier output supplies a stable 1.8V power supply for the BPSK demodulator. The maximum data rate for reliable data transmission is up to 678 kbps with BER < 10^{-9}. The power consumption of the chip is 191μW from a 1.8V supply. Compared to prior work, this work supports both data and power transmissions and it dissipates the lowest power.

6.2 Future Work

This paper introduces a telemetry which transmits data and power using one pair of coil. Our demodulator is design for low power consumption. We did not optimize the power efficiency, so in the future this system which is connected to a higher power efficiency rectifier will be a good issue.

Figure 72 shows the external and internal coils quality factor, we assume that the primary power is fixed. According to the power we want to receive and the rectifier input peak voltage to make V_{DC} 1.8 volts, R_{AC} is derived. Efficiency and channel capacity are estimated. For example, the primary power is set up to be 100mW. The rectifier efficiency is 85%, and the implant circuit power consumption is 40mW. The received power must be greater than 47.06mW=40mW /0.8. The other assumption is

that the distance of external and internal coil is fixed to be 1cm. The coupling coefficient is assumed to be 0.098. After these assumptions are set, we can run a MATLAB program to estimate the relation of Q1, Q2 and channel capacity by our equation in section 2.1.

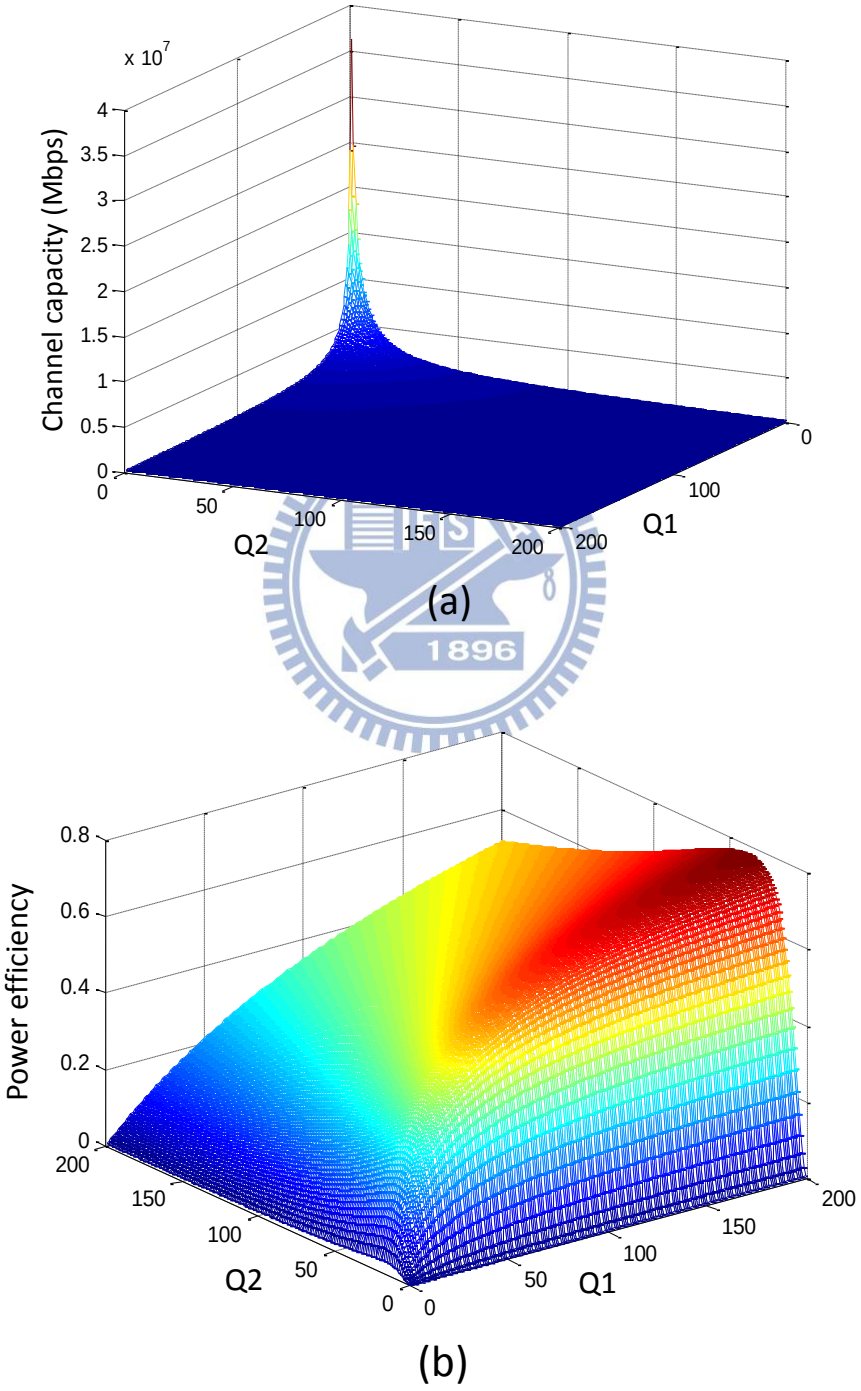


Figure 72. (a) Relation of the Q1, Q2 and capacity (b) Relation of the Q1, Q2 and power efficiency

In order to reach higher power efficiency, the efficiency calculation must to be taken into account. The other MATLAB program is the relation of Q1, Q2 and power efficiency. After these two programs are obtained, we enter a threshold to run this program. If we want to make the power efficiency greater than 70%, and capacity is up to 500 kbps. This program will show the Q1 and Q2 value as shown in Figure 73, and two quality factor values are obtained. The only thing we have to do is choosing the coil size and material to meet the condition.

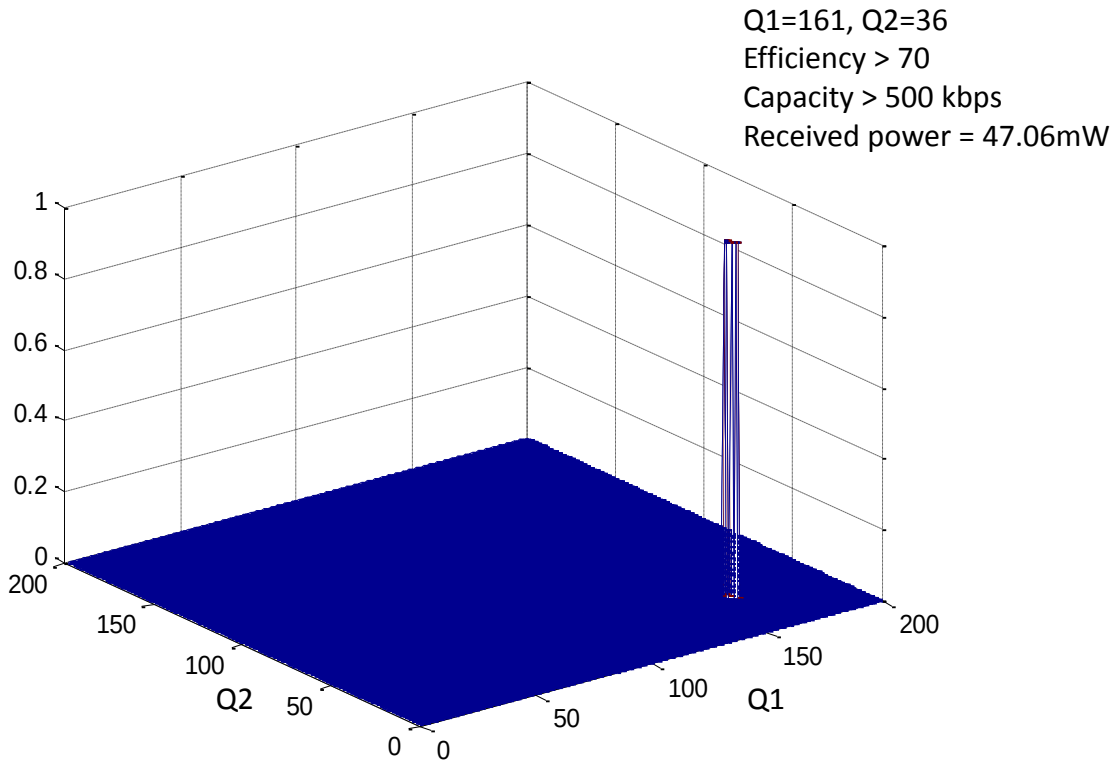


Figure 73. Reasonable Q1, and Q2 value with 500 kbps data rate and the 70% power efficiency

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