國 立 交 通 大 學

電信工程學系

碩 士 論 文

應用於無線區域網路與藍芽系統之全積體化
低功率低相位雜訊整數型及三角積分之分數型頻率合成器

Fully Integrated, Low-Power, Low Phase-Noise Integer-N and Sigma-Delta Fractional-N Frequency Synthesizers for Wireless LAN and Bluetooth Applications

研究生：連偉誠

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中　華　民　國　九十四　年　六　月

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碩 士 論 文

A Thesis

Submitted to Department of Communication Engineering

College of Electrical Engineering and Computer Science

National Chiao Tung University

In Partial Fulfillment of the Requirements

For the Degree of Master of Science In Communication Engineering

June 2005

Hsinchu, Taiwan, Republic of China

中 華 民 國 九十四 年 六 月

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摘要

本論文中主要提出三角積分之分數型頻率合成器，另外還提出兩種不同架構之整數型頻率合成器及兩種不同架構之壓控振盪器，這些電路皆應用於無線區域網路及藍芽無線通訊上。

首先三角積分之分數型頻率合成器，利用0.18微米CMOS製程實現此頻率合成器，以低功率消耗及低相位雜訊為設計主要考量。量測結果如下：可調頻寬為2381 ~ 2606兆赫茲(於頻率控制訊號為10時)，相位雜訊為-118.4分貝/赫茲@1兆赫茲，總功率消耗22.9毫瓦，鎖定時間為30微秒，寄生雜頻較主頻低56.5分貝。

接下來是利用0.18微米CMOS製程實現兩個整數型頻率合成器：第一個為寬頻之頻率合成器，其量測結果如下：可調頻寬為2178 ~ 2629兆赫茲(於頻率控制訊號為011時)，相位雜訊為-108.8分貝/赫茲@1兆赫茲，總功率消耗38.4毫瓦，鎖定時間為40微秒，寄生雜頻較主頻低26.15分貝；第二個為低功率、低相位雜訊之頻率合成器，其量測結果如下：可調頻寬為2399 ~ 2633兆赫茲(於頻率控制訊號為10時)，相位雜訊為-114.0分貝/赫茲@1兆赫茲，總功率消耗28.3毫瓦，鎖定時間為90微秒，寄生雜頻較主頻低41.50分貝。

最後利用0.35微米SiGe BiCMOS製程實現寬頻、低功率之壓控振盪器，量測結果如下：可調頻寬為4310 ~ 5430兆赫茲，相位雜訊為-114.1分貝/赫茲@1兆赫茲，總功率消耗16.7毫瓦。另外利用0.18微米CMOS製程實現四相位壓控振盪器，利用基底端做訊號耦合。量測結果如下：可調頻寬為2093 ~ 2206兆赫茲(於頻率控制訊號為100時)，相位雜訊為-124.3分貝/赫茲@1兆赫茲，總功率消耗19.8毫瓦。

Fully Integrated, Low-Power, Low Phase-Noise Integer-N and Sigma-Delta Fractional-N Frequency Synthesizers for Wireless LAN and Bluetooth Applications

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Abstract

This thesis contents a sigma-delta fractional-N synthesizer mainly. Besides, it contents two integer-N synthesizers and two voltage-controlled oscillators. These circuits are implemented for WLAN and Bluetooth applications.

First, we describe the sigma-delta fractional-N frequency synthesizer, using 0.18μm CMOS technology. Design consideriation contants low power consumption and the low phase noise. The measurement results are listed as following: the oscillation frequency is tunable between 2381 ~ 2606-MHz (as frequency bank is 10), phase noise is -118.4dBc/Hz @1-MHz offset, the power consumption is 22.9mW, locking time is approximately 30μs, and spurious tone is -56.5dBc.

Then we describe two integer-N frequency synthesizers, using 0.18μm CMOS technology. One is wide tuning range frequency synthesizer. The measurement results are listed as following: the oscillation frequency is tunable between 2178 ~ 2629-MHz (as frequency bank is 011), phase noise is -108.8dBc/Hz @1-MHz offset, the power consumption is 38.4mW, locking time is approximately 40μs, and spurious tone is -26.15dBc. Another is low power, low phase noise range frequency synthesizer. The measurement results are listed as following: the oscillation frequency is tunable between 2399 ~ 2633-MHz (as frequency bank is 10), phase noise is -114.0dBc/Hz @1-MHz offset, the power consumption is 28.3mW, locking time is approximately 90μs, and spurious tone is -41.50dBc.

Finally we describe a wide tuning range, low power VCO, using 0.35μm SiGe BiCMOS technology. The measurement results are listed as following: the oscillation frequency is tunable between 4310 ~ 5430-MHz, phase noise is -114.1dBc/Hz @1-MHz offset, and the power consumption is 16.7mW. Besides we also describe a low power, low phase back-gate quadrature VCO, using 0.18μm CMOS technology. The measurement results are listed as following: the oscillation frequency is tunable between 2093 ~ 2206-MHz (as frequency bank is 100), phase noise is -124.3dBc/Hz @1-MHz offset, and the power consumption is 19.8mW.

Acknowledgement

能夠順利取得碩士學位，首先要感謝指導教授周復芳老師給予悉心的指導與教誨，在射頻積體電路設計領域上從空有興趣直到略有所得，而能夠一探射頻積體電路領域的廟堂之美；感謝口試老師：張志揚教授、胡政吉博士在論文上的指導與建議，使得本論文得以更加完整。還有感謝國家晶片系統設計中心提供先進的半導體製程，以及研究員蕭旭峰先生在量測方面的協助，讓晶片的製作與量測得以順利完成。

感謝實驗室的博士班學長鄭國華常常給予我們技術與設計環境上的幫助和意見交換，不厭其煩地帶領學弟們成長；實驗室的學長呂盈蒼、陳政良、劉炳宏、汪揚在課業、電路設計及生活上的幫忙；實驗室的同窗好友政宏、家良、欽賢、柏達、俊賢，在和你們的談話之中，常常讓我觸發出許多珍貴的靈感，課業和生活上也得到你們許多協助，有了大家的陪伴，使得平淡的研究生活多了不少樂趣，這兩年的生活因為你們而顯得多采多姿。還有實驗室可愛的學弟們：仕豪、政展、博揚、秋榜、文明、宏斌，這一年來的陪伴，你們不斷的發問是讓我努力充實自己的原動力，幫忙打理實驗室事務，讓我們才得以致力於研究工作。

最重要的是感謝我的父母親，雖然他們沒受過高等教育，但是他們秉持教育子女的信念，用盡苦心撫育和教導，並提供了我穩定的環境，讓我能專心致力於自我的發展。感謝所有的親朋好友，一直給我關懷與鼓勵，千萬個感謝都無以表達我心中的感受，今日之我是你們合力所造就完成，由衷的感謝各位。

Wei-Cheng June 28, 2005.

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Chapter 1

Introduction

1.1 Background and motivation

By the rapid development and large demand of wireless communication, fully integrated monolithic radio transceivers are the most significant considerations for communication applications. The recent rapid growth of the wireless communication market inspires many people to research the concerned region with strong passion. Of such a many developments, enhanced operating frequency of CMOS technology encourages the designer to implement single-chip RF-to-baseband systems with it instead of bipolar or GaAs. One of the important design goals of portable wireless systems is low power consumption for long battery life. CMOS technology satisfies the requirements of low power consumption, low cost, reduced size, and also a few GHz operating frequency in wireless systems.

In typical RF front-end circuits, frequency synthesizer actions as a local oscillator (LO) for up/down conversion in communication transceivers. Fig. 1-1 shows a general block diagram of a transceiver. It contains a low-noise amplifier (LNA), a power amplifier (PA), mixers, and band-pass filters. In order not to distort the received signals, the excellent noise performance of frequency synthesizer is required. Besides, the switching time of circuit is also significant. The design of

phase-locked loops (PLLs) must generally deal with a tight tradeoff between the settling time and the amplitude of the ripple on the oscillator control line. In conclusion, we can judge a synthesizer by following three parameters: phase noise, sideband interferes (spurious tones), and locking time. Based on the above reason, we realize two integer-N type synthesizers, one sigma-delta fractional-N type synthesizer and two voltage-controlled oscillators.

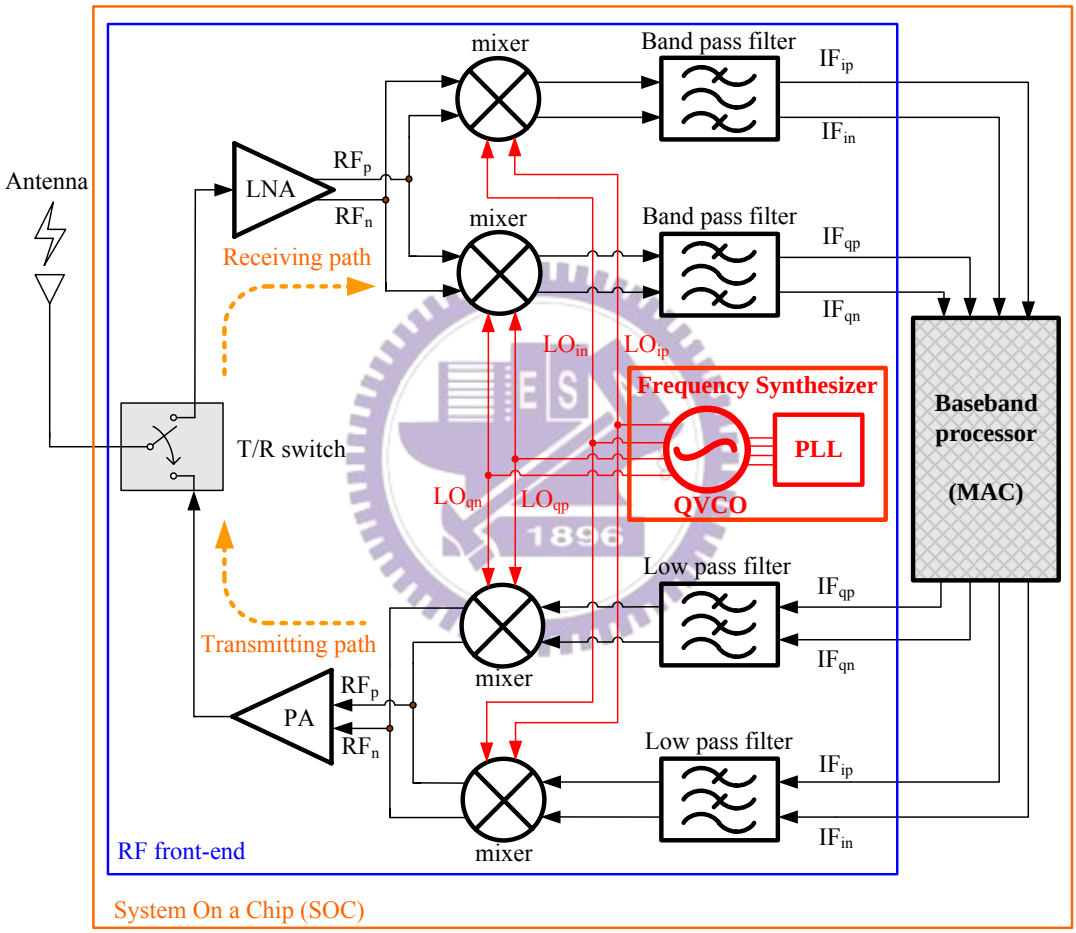


Fig. 1-1 Block diagram of a general transceiver front-end

Wireless LANs and Bluetooth provide wideband wireless connectivity between PCs and other consumer electronic devices, allowing access to core networks and other equipment in office and home environments. There are Home RF, IEEE 802.11 b/g, Bluetooth, and et cetera which operate at 2.4-GHz industrial, scientific, and medical (ISM) band. The Bluetooth standard provides a data rate of 1Mbps at 10m

distance [1]. In addition, the 802.11b standard provides data rates up to 11 Mbps with the direct sequence spread spectrum (DSSS) [2]. The 802.11a/g PHY are based on coded Orthogonal Frequency Division Multiplexing (OFDM) modulation [3-4]. The 802.11a standard operates in the 5-GHz unlicensed national information infrastructure (UNII) band, which provides a total available bandwidth of 300 MHz as compared to the 83.5 MHz available for 802.11b/g. The specifications for these standards summarize in Table 1-1.

Table 1-1 Frequency synthesizer in wireless communication systems

Parameter	**Bluetooth (ISM) [1]**	**IEEE 802.11 b (ISM, USA) [2]**	**IEEE 802.11 g (ISM, USA) [3]**	**IEEE 802.11 a (U-NII, USA) [4]**
RF frequency (MHz)	2402 ~ 2480	2400 ~ 2483.5	2400 ~ 2483.5	5150 ~5250 (lower) 5250 ~ 5350 (middle) 5725 ~ 5825 (upper)
Number of channels	78	6 (Max.)	6 (Max.)	12
Channel spacing	1MHz	20MHz	20MHz	20MHz
Data rate	1Mbps	1 ~ 11Mbps (CCK)	1 ~ 11Mbps (CCK) 6 ~ 54Mbps (OFDM)	6 ~ 54Mbps (OFDM)
Quadrature outputs	Yes	No	Yes	Yes
Phase noise (dBc/Hz)	-80@1MHz -120@3MHz	-110@1MHz	-110@1MHz	-110@1MHz
Locking time	< 200μs	< 200μs	< 200μs	< 200μs

For the noise consideration, the integer-N type has an unavoidable disadvantage that the frequency multiplication (by M) raises the phase noise level by 20log(M) dB. In order to improve the phase noise, “Fractional-N” type frequency synthesizer was

introduced. The first work adopts a complete fractional-N frequency synthesizer, including third order sigma-delta modulator for high degree noise shaping. This architecture is used to allow a high reference frequency, fine step size, and low divided ratio to achieve low in-band phase noise. Besides, a capacitor is placed at the common mode node of the VCO to provide AC ground on this node. Therefore the phase noise of output signal is much lower. On the other hand, the power issue is also an important consideration. The frequency divider adopts the fully integrated multi-modulus type which is composed by seven stages-cascaded dual modulus asynchronous divide-by-2/3 circuits [5]. Hence, no power hunger preamplifier or buffer is needed to drive the divider. It is easy to design and integration compared with programmable pulse-swallow counter or phase-switching circuit [6-7].

Today there are many works focusing on fractional-N synthesizer, especially on sigma-delta modulation type. The in-band noise performance (such as spurious tone and phase noise) has been improved by adding sigma-delta modulator or other noise shaping circuits. Table 1-2 list this work compared with others.

Although the fractional-N type has better performance than the integer-N type, it is more complicated and more difficult to design. Furthermore, in order to improve the low phase noise, the VCO tuning range must be designed in smaller range for lower sensibility. Therefore, the multi-bits frequency bank circuits are used in this design.

Based on above reason, we realize two 2.4-GHz integer-N frequency synthesizers; one is for wide tuning range purpose and the other is for low power and low phase noise purpose. The wide tuning range synthesizer is suited for the concurrent dual-band transceiver front-end [10]. Only one synthesizer is required in

this topology. Otherwise, the wide-band means the much sensitive to phase noise performance. In order to reduce phase noise and spurious tones, we re-design the VCO part of synthesizer. Table 1-3 list these two 2.4-GHz integer-N frequency synthesizers compared with senior's works. It shows that the power consumption is greatly reduced and noise performance is still better than senior's works.

Table 1-2 Fractional-N frequency synthesizer: comparison of recent papers

Performance	**Sigma delta fractional-N synthesizer**	**JSSC Sep. 2004 [8]**	**JSSC Mar. 2005 [9]**
Technology	CMOS 0.18μm	CMOS 0.18μm	SiGe BiCMOS 0.5μm
Architecture	3-rd △-∑ fractional-N synthesizer	3-rd △-∑ fractional-N synthesizer	3-rd △-∑ fractional-N synthesizer
Chip area	1.15 x 1.0 mm^2	1.9 x 1.8 mm^2	2.3 x 1.4 mm^2
Voltage	1.8V	1.8V	2.75V
Center frequency	2.4GHz	2.1GHz	2.4GHz
Reference frequency	16MHz	35MHz	40MHz
Output frequency resolution	125kHz	35Hz	468.75kHz
3dB closed loop BW	100kHz	700kHz	100kHz
Phase noise	-118.4dBc/Hz @1MHz	-112dBc/Hz @1MHz	-120dBc/Hz @1MHz
Spur tones	-56.5dBc @3.125MHz	-60dBc	-50dBc
Settling time	30μs	7μs	30μs
Total power consumption	22.9mW	28mW	99mW

Table 1-3 Integer-N frequency synthesizer: comparison of senior's works

Performance	Wide tuning range synthesizer [10]	Low power and low phase noise synthesizer	Thesis 2004 [11]	Thesis 2003 [12]
Technology	CMOS 0.18μm	CMOS 0.18μm	CMOS 0.25μm	CMOS 0.25μm
Architecture	Integer-N (11 stages of %2/3)	Integer-N (11 stages of %2/3)	Integer-N (11 stages of %2/3)	Integer-N (11 stages of %2/3)
Chip area	1.5 x 1.1 mm^2	1.45 x 0.9 mm^2	1.4 x 0.95 mm^2	1.25 x 0.96 mm^2
Quadrature VCO types	transistor coupling	transistor coupling	transistor coupling	Poly-phase
Voltage	1.8V	1.8V	2.5V	2.5V
Reference frequency	1MHz	1MHz	1MHz	1MHz
Tuning range (GHz) / %	2.123 ~ 2.786 / 27.6%	2.371 ~ 2.678 / 12.8%	2.38 ~ 2.52 (for one bank condition) / 5.7%	2.35 ~ 2.53 (for one bank condition) / 7.5%
Phase noise (dBc/Hz)	-108.8 @1MHz -119.7 @3MHz	-114.0 @1MHz -120.5 @3MHz	-102 @1MHz	-88.4 @1MHz
Spurious tone	-26.15dBc @1MHz	-41.5dBc @1MHz	~ -40dBc @1MHz	-14dBc @1MHz
Settling time	40μs	90μs	130μs	25μs
Total power consumption	38.4mW	28.3mW	87.5mW	58.6mW

Recently, there are still many works focusing on integer-N type synthesizer because the system requirement is not stringent in the short-distance communication systems such as Bluetooth, ZigBee, WLAN, and etc. Table 1-4 list these two synthesizers compared with recent papers. We can see that the power consumption and phase noise of these two synthesizers is better than most of recent papers.

Table 1-4 Integer-N frequency synthesizer: comparison of recent papers

Performance	Wide tuning range synthesizer [10]	Low power and low phase noise synthesizer	JSSC Nov. 2004 [7]	JSSC Mar. 2004 [13]	JSSC Jul. 2003 [1]	RFIC 2001 [5]
Technology	CMOS 0.18μm	CMOS 0.18μm	CMOS 0.18μm	CMOS 0.35μm	CMOS 0.18μm	CMOS 0.25μm
Architecture	Integer-N	Integer-N	Integer-N	Fractional-N	Integer-N	∑-Δ fractional-N
Voltage	1.8V	1.8V	1V	3.3V	1.8V	2.5V
Reference frequency	1MHz	1MHz	11MHz	256MHz	500kHz	13MHz
Tuning range (GHz) / %	2.123 ~ 2.786 / 27.6%	2.371 ~ 2.678 / 12.8%	5.45 ~ 5.65 / 3.6%	2.4 ~ 2.5 / 4.2%	2.26 ~ 2.66 / 16.7%	2.24 ~ 2.50 / 10.8%
Phase noise (dBc/Hz)	-108.8 @1MHz -119.7 @3MHz	-114.0 @1MHz -120.5 @3MHz	-111 @1MHz	-97 @1MHz	-125 @3MHz	-133 @3MHz
Spurious tone	-26.15dBc @1MHz	-41.5dBc @1MHz	-80dBc @11MHz	-55dBc @62.5kHz	-30dBc @500kHz	-68dBc @13MHz
Settling time	40μs	90μs	51μs	-	120μs	-
Power	38.4mW	28.3mW	27.5mW	49.5mW	15mW	55mW

Voltage-Controlled Oscillator (VCO) plays an important role in communication systems because the phase noise of the VCO determines the out-of-band noise of the frequency synthesizer. In recently high-frequency operation VCO designs, high power consumption is always an unavoidable limitation, which can be obviously observed in [15-19, 21-24]. The design of VCO becomes even more challenging in RF applications, where stringent requirements of phase noise and power consumption remain as the toughest tasks that RFIC engineers have to deal with. The local oscillator circuits used in radio frequency (RF) systems such as wireless (local area

networks) LANs and Bluetooth system must have sufficient tuning ranges and good phase noise characteristics. In order to extend the tuning range of VCO, enlarge the varactor gain must be used. We choose the suitable p-n junction varactor for large varactor gain. Hence, we implement a 5.2-GHz low power, low cost, and wide tuning range voltage-controlled oscillator with 0.35-μm SiGe BiCMOS process. Table 1-5 lists this work compared with others.

In addition, fully integrated voltage-controlled oscillators (VCOs) are important building blocks for implementation of a single radio-frequency chip in today's communication systems. In low-IF or direct conversion transceivers, quadrature signals are required for base-band (de)modulation. It is important to offer quadrature generator circuits as minimal power consumption. However, the local oscillator circuits must have sufficient lower power consumption and better phase noise characteristics. Traditional quadrature VCO used additional transistors coupling between two core circuits, so the 1/f come from coupling transistors results in worse phase noise. The new quadrature VCO architecture is presented in [21]. The back-gate (body) node of transistor is used for coupling circuit. The triple-well technique makes this idea practicable. Hence, we also implement a 2.4-GHz low power, low phase noise back-gate quadrature VCO with 0.18-μm triple-well CMOS process. Table 1-6 lists this work compared with others.

Table 1-5 Low power and wide tuning-range SiGe VCO: comparison of recent papers

Performance	Center freq. (GHz)	Tuning range / %	Phase noise (dBc/Hz)	Core circuit power (mW)	Vdd (V)	FOM
[14] APMC, 2004 (This work) 0.35-μm SiGe BiCMOS	5.35	1120MHz / 21.5%	-96.1 @100kHz -114.1 @1MHz -125.0 @3MHz	3.3	3.3	185.38 @100kHz 183.38 @1MHz 184.84 @3MHz
[15] MTT, 2001 0.25-μm CMOS	5.35	340MHz / 6.4%	-93 @100kHz	7	1.5	183.12 @100kHz
[16] MTT-S, 2002 0.24-μm CMOS	5.8	810MHz / 14.0%	-112 @1MHz	5	2.5	180.28 @1MHz
[17] RFIC, 2003 0.4-μm SiGe BiCMOS	5	870MHz / 17.4%	-116 @1MHz	7.5	2.5	179.83 @1MHz
[18] MWCL Jul. 2003 0.18-μm CMOS	5.8	166MHz / 2.9%	-110 @1MHz	8.1	1.8	176.2 @1MHz
[19] MWCL May 2005 0.25-μm CMOS	5	980MHz / 20.3%	-114.6 @1MHz	7.3	2.5	179.9 @1MHz
[20] Thesis, 2002 0.25-μm CMOS	5.4	260MHz / 4.8%	-102 @1MHz	17.5	2.5	164 @1MHz
[12] Thesis, 2003 0.25-μm CMOS	5.68	670MHz / 11.8%	-100 @1MHz	3	1.5	170 @1MHz

Table 1-6 Low phase noise quadrature VCO with back-gate coupling: comparison of recent papers

Performance	Center freq. (GHz)	Tuning range (GHz) / %	Phase noise (dBc/Hz)	Core circuit power	Vdd (V)	FOM
This work 0.18µm CMOS	2.1	2.067 ~2.232 / 7.9%	-99.9 @100kHz -120.2 @600kHz -124.3 @1MHz -133.9 @3MHz	9mW	1.8	-176.8 @100kHz -181.5 @600kHz -181.2 @1MHz -181.3 @3MHz
[21] JSSC Jun. 2004 0.18µm CMOS	1.1	1.047 ~1.39 / 32.76%	-120 @1MHz	5.4mW	1.8	173.5 @1MHz
[22] JSSC Jul. 2001 0.25µm CMOS	1.8	1.71 ~1.99 / 15.56%	-143 @3MHz	20mW	2.5	185.5 @3MHz
[23] JSSC Jun. 2003 0.18µm SiGe BiCMOS	6.3	6.3 ~6.6 / 4.76%	-106 @1MHz	6.8mW	1.8	176.7 @1MHz
[24] JSSC Apr. 2005 0.18µm CMOS	1.8	1.14 ~2.46 / 73%	-126.5 1MHz	4.8mW	1.5	184.8 @1MHz

1.2 Thesis organization

This thesis constructs a fully integrated 2.4-GHz sigma-delta fractional-N frequency synthesizer, two fully integrated 2.4-GHz integer-N frequency synthesizers, and two voltage-controlled oscillators.

Chapter 2 introduces the fully integrated 2.4-GHz sigma-delta fractional-N frequency synthesizer and presents the simulation results of each building block and measurement results.

Chapter 3 introduces two 2.4-GHz integer-N frequency synthesizers (one is for wide tuning range purpose and the other is for low power and low phase noise purpose) and presents the simulation results of each building block and measurement results.

Chapter 4 introduces two voltage-controlled oscillators (one is for wide tuning range purpose and the other is for low phase-noise purpose) and presents the simulation results and measurement results.

Finally, we discuss our measurement results, self-criticisms of the shortcomings in specifications, and future prospects in Chapter5.

Chapter 2

A 2.4-GHz Low Power, Low Phase-Noise, Sigma-Delta Fractional-N Frequency Synthesizer

2.1 Architectures

The demand for high-speed wireless data communications increases dramatically in recent years. By the rapid development and large demand of wireless communication, a fully integration monolithic transceivers are the most significant considerations for communication application. Since we now have a high-quality CMOS integrated VCO and a high-speed prescaler, it is possible to realize the ultimate goal of this research, i.e. a complete PLL LO synthesizer for a mobile communication system, integrated in a standard CMOS process without any external components, trimming or extra processing steps[25]. For the noise consideration, the integer-N type has an unavoidable disadvantage that the frequency multiplication (by M) raises the phase noise level by $20\log(M)$ dB. In order to improve the phase noise, "Fractional-N" type frequency synthesizer was introduced. According to its name, this type makes the output frequency f_{VCO} be fractional times to the reference frequency f_{ref} and therefore decline the phase noise. A fractional-N synthesizer allows the PLL to operate with a high reference frequency and meanwhile achieve a fine step size by constantly sweeping the loop division ratio between integral numbers, thus the

average division ratio is a fractional number. At this chapter, we choose the Fractional-N type synthesizer in this thesis. Fig. 2-1 is the general architecture of the Integer-N and fractional-N type PLLs. The division ratio of frequency divider is integer in the integer-N type. Otherwise, the division ratio of frequency divider is fractional in the fractional-N type.

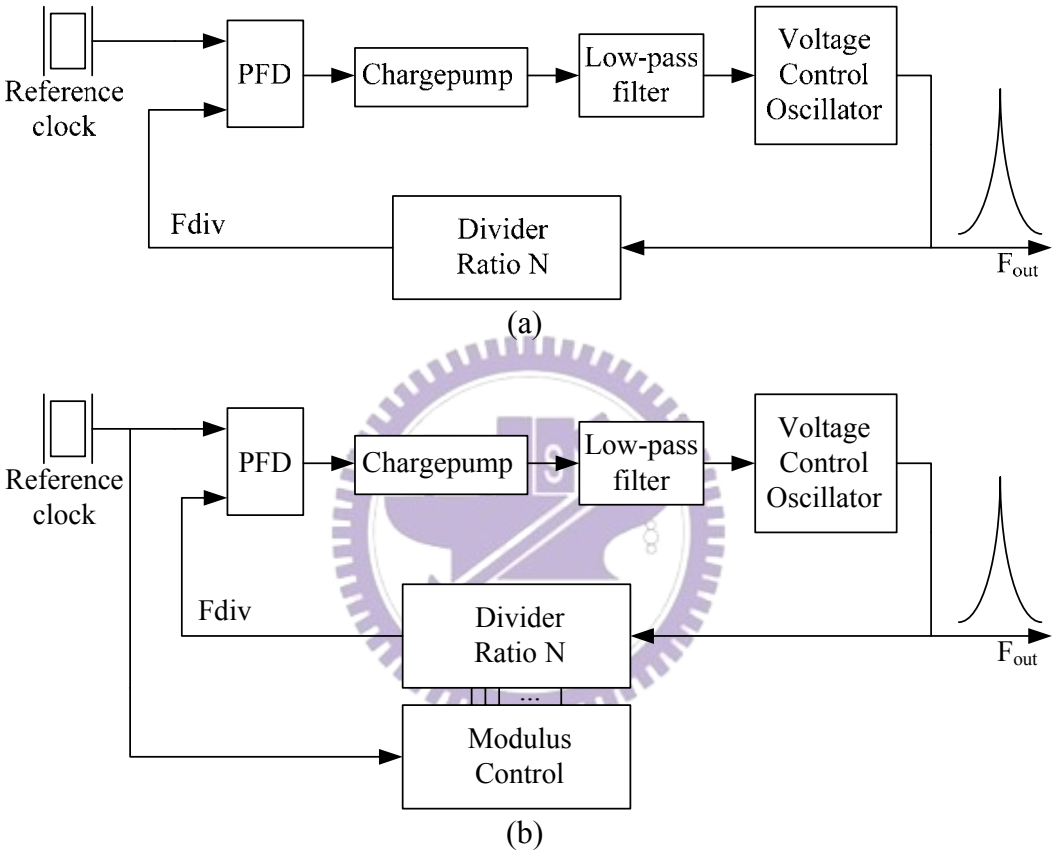


Fig. 2-1 General architecture of PLL (a) Integer-N type (b) Fractional-N type

2.2 Design considerations

This chip is fabricated in February 2005. This chip provides a fully integrated low power, low phase-noise, fractional-N frequency synthesizer with spurs noise shaping technique. This frequency synthesizer which consists of six functional blocks, which includes voltage controlled oscillator (VCO), third order sigma-delta modulator, fully programmable multi-modulus divider, phase frequency detector (PFD), charge

pump and low pass loop filter (LPF). Besides the reference crystal and LPF, all the functional blocks are all integrated in a single chip. The following sections will introduce them in detail.

In general, the design flow of radio frequency synthesizer is showing below: At first, determine and design the circuit architecture. Next simulate the whole circuits briefly by behavior simulation tools (ex. Simulink of Matlab). Then simulate each block in detail by transistor level simulation tools (ex. Eldo RF, Hspice, ADS, and etc.). After circuit pre-simulation, try to layout our circuit by layout tool (ex. Laker, Virtuoso, and etc.). Then use parasitic extraction tool (ex. Calibre xRC) for parasitic extraction (PEX). Finally simulate our circuits with parasitic by transistor level simulation tools. It also called post-simulation. There are three PEX levels we usually use: PEX-C (only including lumped capacitance), PEX-RC (including distributed resistance and intrinsic capacitance), and PEX-RCC (including distributed resistance and all parasitic capacitance). PEX-RCC is most accurate but it takes most time for post-simulation. Usually, simulation time with PEX-RCC is seven times than one with PEX-C. So we use PEX-C for normal circuits post-simulation and PEX-RCC for particular circuits post-simulation.

2.2.1 Voltage-controlled oscillator

Voltage-Controlled Oscillator (VCO) plays an important role in communication systems because the phase noise of the VCO determines the out-of-band noise of the frequency synthesizer. An oscillator can generate various frequencies for up/down conversion in communication transceivers. In order not to distort the received signals, the excellent noise performance of VCO is required. The design of VCO becomes

even more challenging in RF applications, where stringent requirements of phase noise and power consumption remain as the toughest tasks that RFIC engineers have to deal with.

There are two kinds of CMOS RFIC oscillators in common use: One is LC-tank oscillator and the other is Resonatorless oscillator. The later has not been popular in RF design. This is because they not only exhibit an open-loop Q close to unity but contain many noisy active and passive devices in the signal path. For example, in a three-stage differential ring oscillator, the open-loop Q is approximately equal to 1.3 [26], and nine transistors (including the tail current sources) and six load resistors add noise to the carrier. Hence, we adopt the LC-tank architecture.

An LC-tank oscillator is a feedback network with an LC-tank as the feedback circuit [27], as showing in Fig. 2-2. In this oscillator model, a noiseless load resistor R_p is present, so we want to provide energy replenished by a transconductor gm. The idea is that an active network generates impedance equal to $-R_p$ so that this feedback system allow steady oscillation [25]. The oscillator frequency and gm value are:

$$g_m = 1/R_p \tag{2-1}$$

$$f_0 = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \tag{2-2}$$

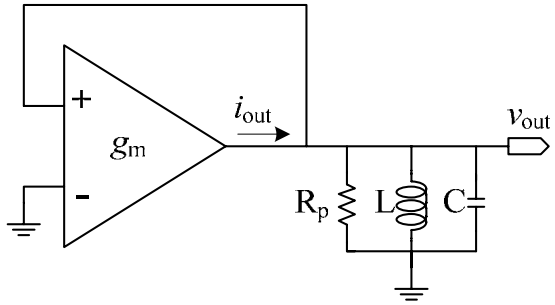


Fig. 2-2 Behavioral model of an ideal LC oscillator

Fig. 2-3 is conventional CMOS LC-tank VCO architecture. It contains an LC-Resonator with negative-Gm cross-coupled pairs of MOS transistors as active part. The architecture of cross-coupled pairs adopts both NMOS and PMOS transistors (M1, M2, M3, M4) to enhance negative conductance, besides, only one inductor is paralleled with varactors to build the LC-resonator, instead of two inductors paralleled to signal ground. Such architecture can save large chip area. The complementary architecture mentioned above also provides several excellences over conventional structure only adopt NMOS or PMOS to be -Gm cell.

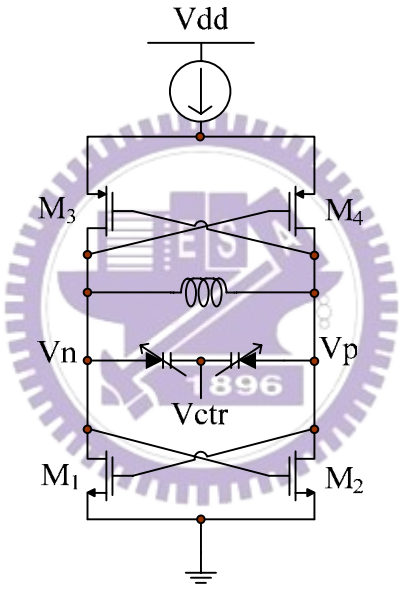


Fig. 2-3 Conventional CMOS LC-tank VCO architecture

For low power consideration, the bias voltage of current source should be chosen carefully. The V_{gs}-V_t and the gm of MOS in cross-coupled pair must be chosen correctly in order to achieve a good compromise between power consumption, phase noise and tuning range. A low value of V_{gs}-V_t gives a good transconductance-to-current ratio and hence low power consumption, but results in large transistor and small tuning range. From [25], the required negative transconductance G_M of MOS in negative transconductance cell must then be at least equal to

$$G_M = \frac{R_{eff}}{(\omega_0 L)^2} \tag{2-3}$$

R_{eff} means the effective resistance of the LC tank in the equation above. The safety factor in the transconductance value must be large enough to ensure proper start-up of the oscillator, and is chosen to be 2.5. In order words, g_m value equals to 2.5 times of G_M. The total current consumption is

$$I = 2 \cdot I_{M1} = 2 \cdot \frac{g_{m,M1} \cdot (V_{gs} - V_t)_{M1}}{2} \tag{2-4}$$

The PMOS transistors are approximately three times larger than the NMOS transistors. Assume the oscillation amplitude is V_A. The expected phase noise at Δf kHz offset then equals to

$$L\{\Delta f \text{ kHz}\} = \frac{kT \cdot R_{eff} \cdot (1+A) \cdot (\frac{\omega_0}{\omega})^2}{\frac{V_A^2}{2}} \tag{2-5}$$

The parameter “A” is defined to be the negative transconductance cell noise contribution factor and usually no less than 1. Through the equations above, the bias voltage can be considered and tradeoff between low-power and low phase-noise is also taken.

A widely used figure of merit (FOM) [28] to compare VCO for both phase noise and power consumption is defined as:

$$FOM = 10 \cdot \log\left[\frac{kT}{P_{\text{sup}}} \cdot \left(\frac{f_0}{f_{off}}\right)^2\right] - S_\phi(f_{off}) \tag{2-6}$$

Where P_{sup} is the power consumed by the VCO,

f_0 is the center frequency,

f_{off} is the frequency offset from the center,

and $S_\phi(f_{off})$ is the phase noise at a frequency f_{off} from the center.

Based on the above consideration, the circuit structure based on the LC-tank oscillator is used to implement this integrated VCO, as showing in Fig. 2-4.

Besides, the CMOS is entering an era of Deep-Sub-Micron (DSM). The process variation causes serious problems and more challenge for circuit designers. The tunable range must be designed in wider range but the gain of VCO (Kvco) should keep in smaller value. In order to make sure that oscillation frequency can cover Wireless LAN and Bluetooth system requirements with no effect upon frequency variation, 2-bits frequency bank circuits are used in this design. Therefore, the overall frequency range is widened to compensate for frequency variation but the Kvco can still remain in small value for smaller sensitivity and lower phase noise. There are two control bits and enables us to set the oscillator under 4 operating conditions: 00, 01, 10, and 11. Different control bit is connected to different amount of parallel capacitors; higher bit is connected to a larger capacitance. When a control bit of capacitor bank is at high level, the capacitor is enabled and the capacitance of LC-tank is increased.

In Fig. 2-4, the capacitor bank architecture adopts a MOS as a varactor. When a control bit of capacitor bank is at low level, the MOS varactor has small capacitance. Otherwise, when a control bit is at high level, the MOS varactor has large capacitance. It can prevent not start-up oscillation while some damage of switch happened.

Fortunately, there are new RF models released from TSMC standard model library. The symmetric inductor is able used to enhance the quality factor of LC-tank. The spiral inductor being used is shown with its layout (Fig. 2-5(a)) and equivalent lump circuit model (Fig. 2-5(b)) with radius=60μm, width=15μm, number of turns=3, and spacing=2μm. The total inductance is about 2.2nH. Use the MOS varactor

(Blanch=25 and Group=4, as showing in Fig. 2-6). So the oscillation frequency of this VCO can oscillate at 2.4-GHz.

After the trade off between low power consumption and low phase noise, the optimized bias current [25] is calculated. Each transistor in core circuit has the optimized bias condition for low power consumption. Based on this bias current, the expected phase noise at 1MHz offset can be figured out. Through the equations (2-3, 2-4), the bias voltage can be considered and tradeoff between low-power and low phase-noise is also taken.

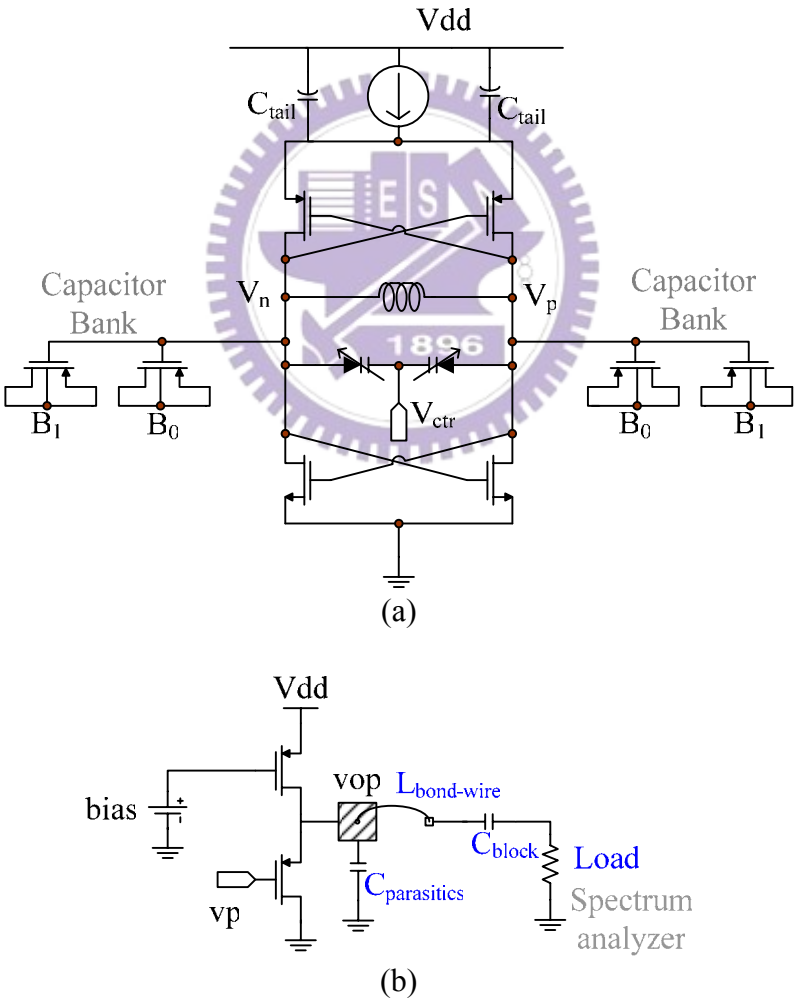
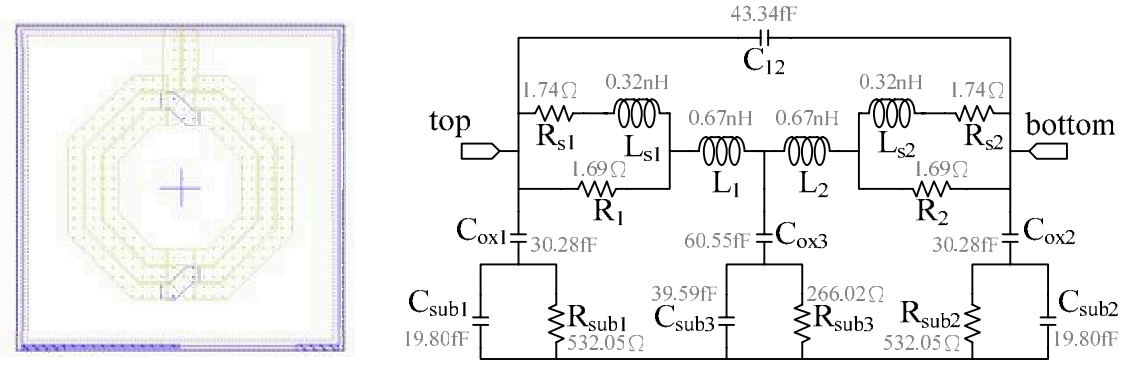


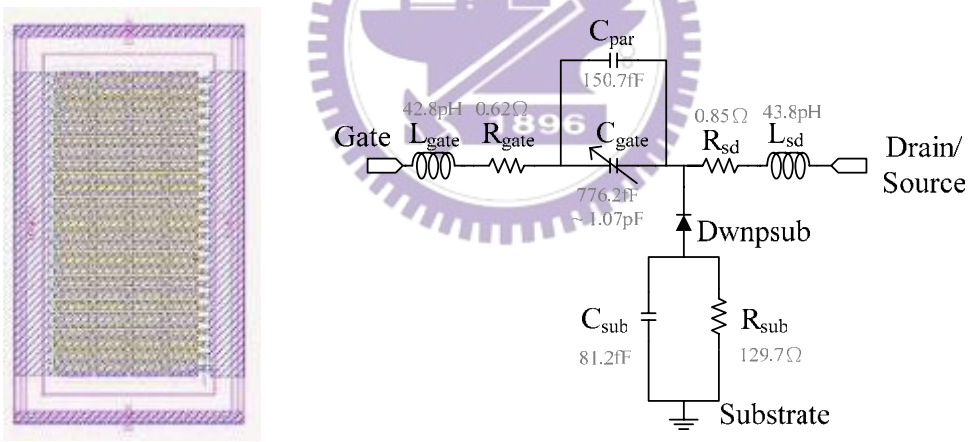
Fig. 2-4 Schematic of VCO (a) core circuit part (b) buffer stage



(a) (b)

Fig. 2-5 Spiral inductor in this synthesizer (a)layout (b)equivalent circuit model

In Fig. 2-4, a capacitor C_{tail} is placed at the common mode node of the VCO. For symmetry the capacitance is distributed over both sides and connected to the power supply. Adding the capacitance provides AC ground on the common mode node. As a result, the spectrum is much cleaner, which confirms that all 1/f noise comes from the bias current source.



(a) (b)

Fig. 2-6 MOS varactor in this synthesizer (a)layout (b)equivalent circuit model

After Eldo RF post-simulation, it shows that the oscillator is tunable between 2.347 and 2.561-GHz (214-MHz tuning range) at bank 10. Fig. 2-7 shows the tuning curve of VCO for bank 00, 10 and 11. The corner case of tuning curve for bank 10 is shown in Fig. 2-8. The frequency variation of corner case is quite distinct. We use the capacitor to compensate this variation, as showing Fig. 2-9. The output swing of VCO is shown in Fig. 2-10.

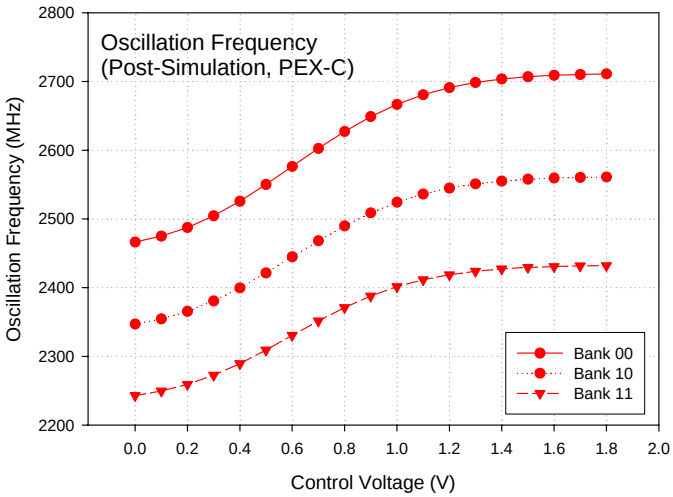


Fig. 2-7 Tuning curve of VCO
(corner case: TT; Bank condition: 00 10 11)

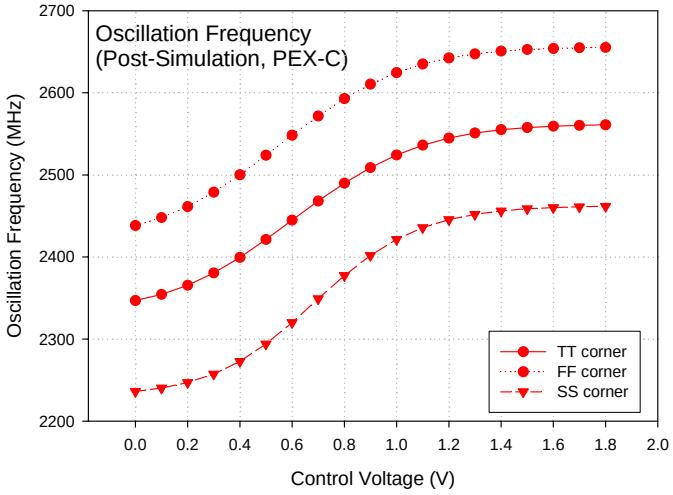


Fig. 2-8 Tuning curve of VCO
(corner case: TT, FF, SS; Bank condition: 10)

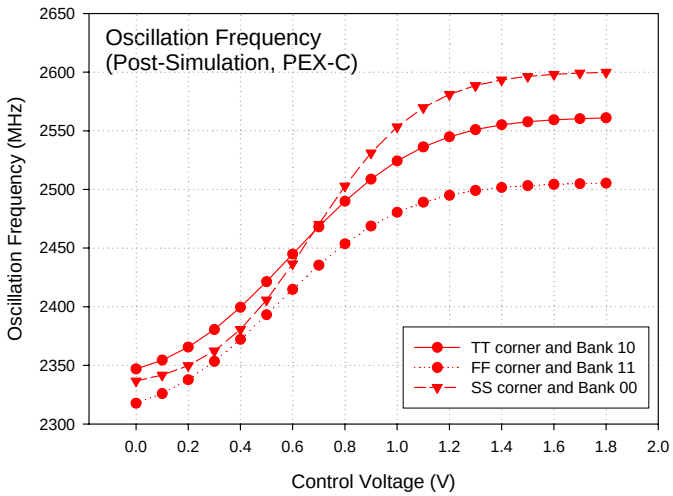


Fig. 2-9 Tuning curve of VCO
(corner case & Bank condition : TT&10, FF&11, SS&00)

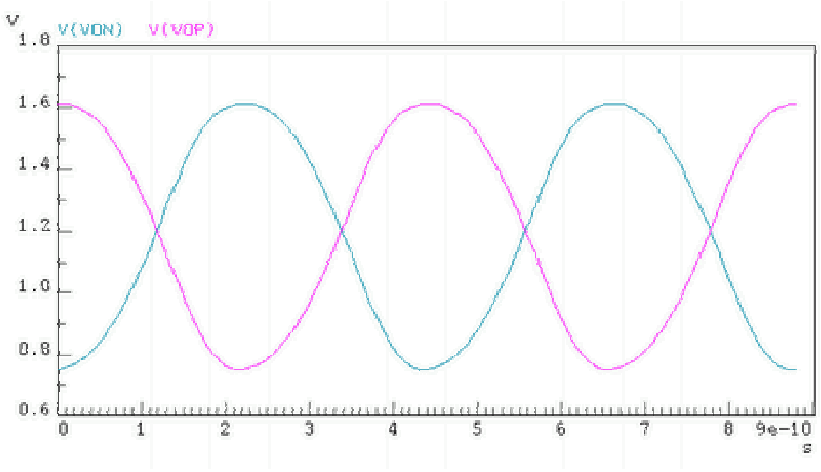


Fig. 2-10 Output swing of VCO (corner case: TT, Bank condition: 10)

The most critical part in the design of a low-phase noise VCO is the inductor of the resonance LC-tank. The phase noise is -118.0dBc/Hz at 1-MHz offset, and -129.0dBc/Hz at 3-MHz offset at 2.45-GHz, as showing in Fig. 2-11.

The power consumption of two quadrature VCO cores is 4.6mW. The overall power consumption is 10.7mW with buffer output stages.

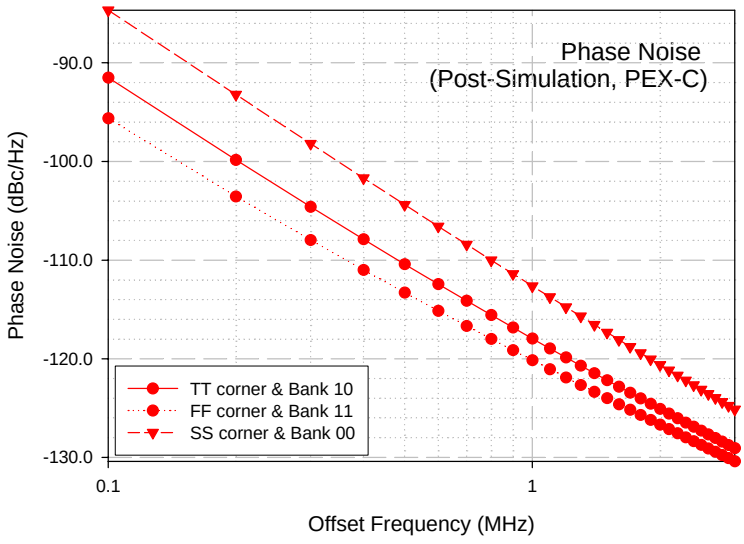


Fig. 2-11 Phase noise of VCO
(corner case & Bank condition : TT&10, FF&11, SS&00)

2.2.2 Sigma-delta modulator

The basic idea behind fractional-N synthesis is division by fractional ratios, instead of only integer ratios. To accomplish fractional division, the same frequency divider as in an integer-N frequency synthesizer is employed, but the division is controlled differently. In the Fig. 2-12 the division modulus of the frequency divider is steered by the carry output of a simple digital accumulator of k-bit width [29]. To realize a fractional division ratio N + n , with $n \in R[0,1]$, a digital input $K = n \cdot 2^k$ is applied to the accumulator. A carry output is produced every K cycles of the reference frequency f_{ref}, which is also the sampling frequency of the digital accumulator. This means that the frequency divider divides $2^k - K$ times by N and K times by N+1, resulting in a division ratio N_{frac}, given by Eq. (2-1).

$$N_{frac} = \frac{(N)\times(2^k - K)+(N+1)\times(K)}{2^k} = N + \frac{K}{2^k} = N + n \qquad (2\text{-}7)$$

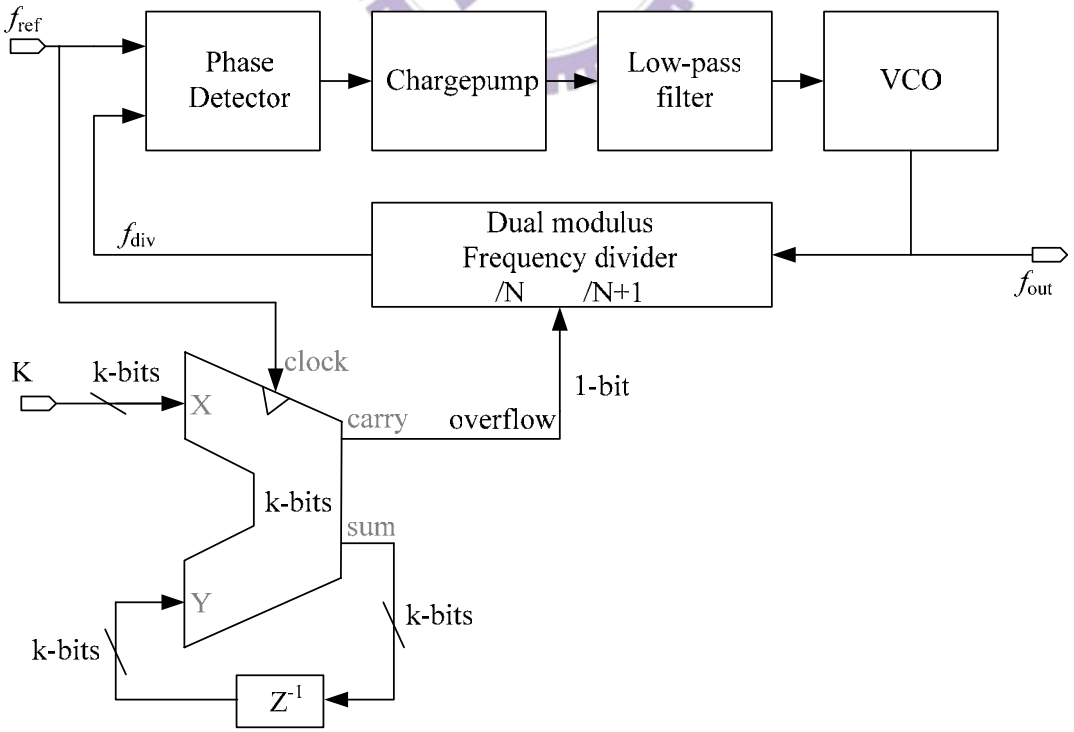


Fig. 2-12 General fractional-N frequency synthesizer

Eq. (2-7) states that for a given reference frequency, it is possible to make the frequency resolution arbitrary fine, by choosing the width of the accumulator sufficiently large. For example, in Bluetooth system the channel spacing of 1-MHz can be synthesized using a f_{ref} of 16-MHz, by realizing an accumulator width k of more than 4 bits.

However, the overflow signal is periodic under this architecture. The spurious tone of frequency synthesizer is more terrible than integer-N architecture. This is not results we expect. In order to overcome this problem, we replace this part with a sigma-delta modulator, as showing in Fig. 2-13. The sigma-delta modulator consists of integration, quantization, and differentiation. After sigma-delta modulator, the signal power doesn't change but quantization noise power integrates into high frequency (Fig. 2-14). The spurious problem due to the periodic overflow signal is greatly reduced.

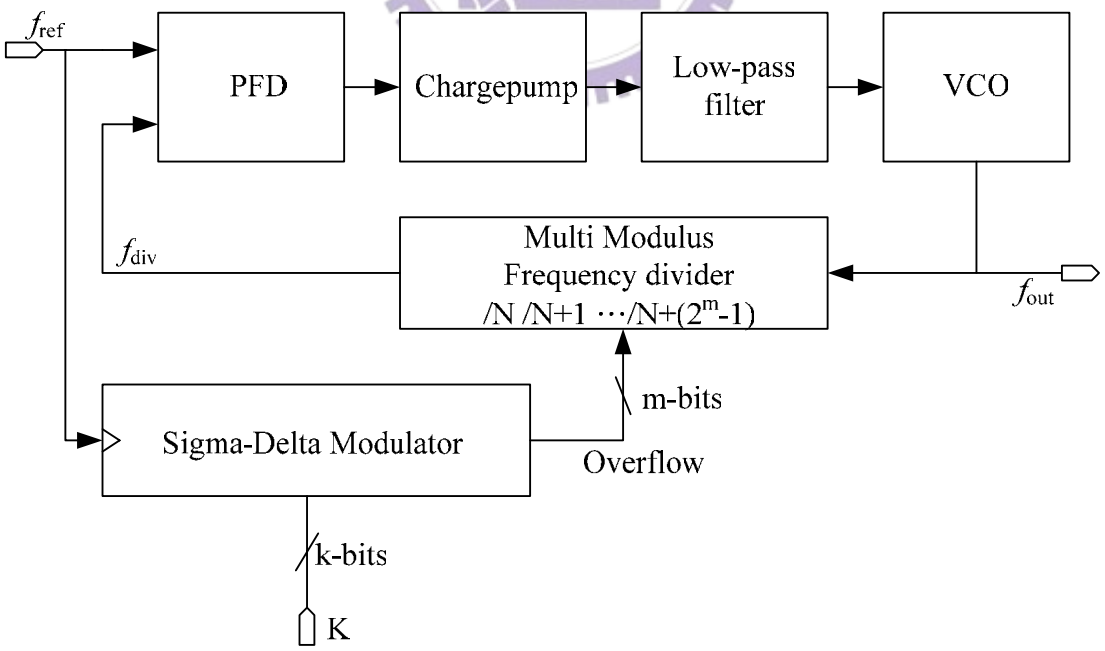


Fig. 2-13 Fractional-N frequency synthesizer with sigma-delta modulator

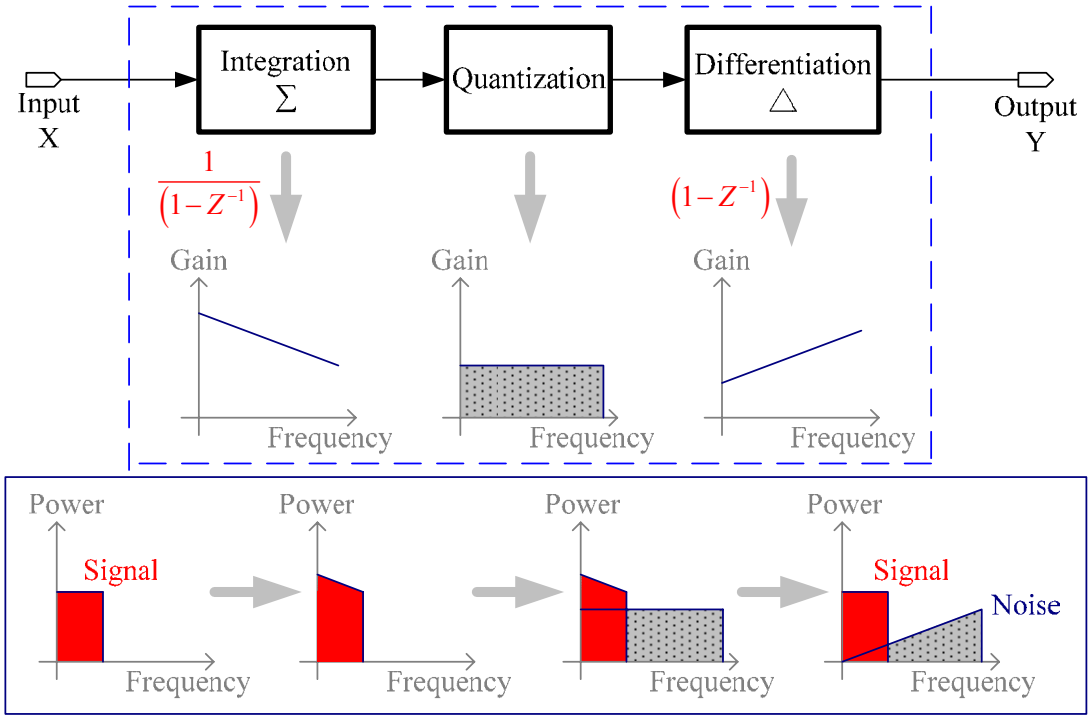


Fig. 2-14 Noise shaping of a sigma-delta modulator

The relation between output and input of sigma-delta modulator is:

$$Y = \begin{cases} X+q_a & (\text{w/o } \Sigma-\Delta \text{ modulator}) \\ X+(1-Z^{-1})q_a & (\text{w/i } \Sigma-\Delta \text{ modulator}) \end{cases} \quad (2\text{-}8)$$

Based on above question, we can realize the schematic of sigma-delta modulator. Next we will introduce two kinds of sigma-delta modulator: one is first order SDM and the other is third order SDM. Finally we have a comparison with these two architectures.

- First order sigma-delta modulator:

In this architecture (Fig. 2-15), the transfer function is the same as the accumulator architecture (Fig. 2-16). The transfer function is:

$$N[Z] = .f[Z] + (1-z^{-1}) \times q_a[Z] \quad (2\text{-}9)$$

It means that the quantization noise q_a transfers to $q_e[Z] = (1-z^{-1}) \times q_a[Z]$.

So the transfer function of quantization noise is:

$$H_{noise}(f) = 1 - z^{-1}$$

$$H_{noise}(f) = \left| 1 - \exp\left(-\frac{j2\pi f}{f_{ref}} \right) \right|$$

$$H_{noise}(f) = \left| 1 - \cos\left(\frac{j2\pi f}{f_{ref}} \right) - j \cdot \sin\left(\frac{j2\pi f}{f_{ref}} \right) \right|$$

$$H_{noise}(f) = \left| 2 \cdot \sin\left(\frac{\pi f}{f_{ref}} \right) \right| \qquad (2\text{-}10)$$

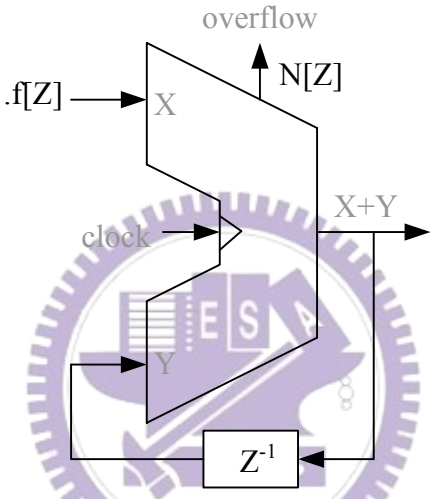


Fig. 2-15 First order sigma-delta modulator

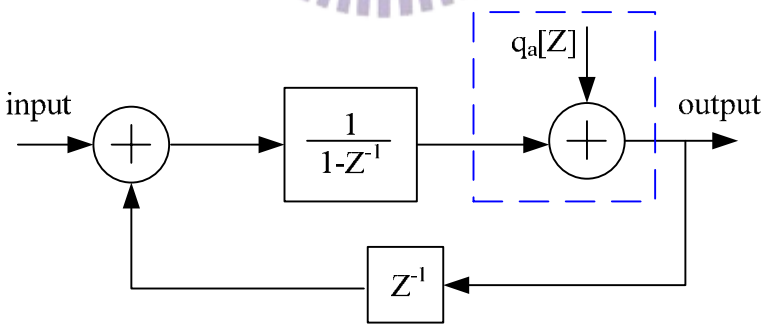


Fig. 2-16 Transfer function of first order sigma-delta modulator

Assume there is the k-bit accumulator with input signal K, the ideal output frequency of prescaler is:

$$f_{div} = \frac{f_{vco}}{N + .f} = \frac{f_{vco}}{N + \frac{K}{2^k}} \qquad (2\text{-}11)$$

But real output frequency of prescaler is:

$$f_{div,r}(t)=\frac{f_{vco}}{N+\left[.f+q_e(t)\right]}=\frac{f_{vco}}{N+\frac{k}{2^M}+q_e(t)}=\frac{f_{vco}}{N_T+q_e(t)}$$

$$N_T=N+\frac{k}{2^M} \tag{2-12}$$

To normalize the frequency error term:

$$\triangle f(t)=\frac{f_{div}-f_e(t)}{f_{div}}=1-\frac{\frac{f_{vco}}{N_T+q_e(t)}}{\frac{f_{vco}}{N_T}}=1-\frac{1}{1+\frac{q_e(t)}{N_T}}\cong\frac{q_e(t)}{N_T} \tag{2-13}$$

The definition of phase error is:

$$\theta_e(t)\triangleq 2\pi\times\int\triangle f(t)dt=2\pi\times\frac{f_{div}}{N_T}\times\int q_e(t)dt \tag{2-14}$$

Differential both sides at the same time, we can get:

$$\theta_e'(t)=2\pi\times\frac{f_{div}}{N_T}\times q_e(t) \tag{2-15}$$

The Power spectrum density (PFD) of phase error is:

$$\theta_e(t)=\int\theta_e'(t)dt\Rightarrow\theta_e(f)=\frac{1}{s}\times\theta_e'(f)\Rightarrow S_{\theta_e}(f)=\left(\frac{1}{s}\right)^2\times S_{\theta_e'}(f) \tag{2-16}$$

So,

$$S_{\theta_e}(f)=\frac{1}{(2\pi f)^2}\times\left(\frac{2\pi\times f_{div}}{N_T}\right)^2\times S_{q_e}(f)$$

$$S_{\theta_e}(f)=\left(\frac{f_{div}}{f\times N_T}\right)^2\times S_{q_e}(f) \tag{2-17}$$

Assume the ideal PFD of quantization noise is: $S_{q_a}(f)=\frac{1}{12\cdot f_{ref}}$

So, the PFD of phase error is:

$$S_{\theta_e}(f)=\left(\frac{f_{div}}{f\times N_T}\right)^2\times\left\{\frac{1}{12\cdot f_{ref}}\cdot\left[2\cdot\sin\left(\frac{\pi f}{f_{ref}}\right)\right]^2\right\}=\frac{f_{ref}}{3\cdot(N_T\cdot f)^2}\sin^2\left(\frac{\pi f}{f_{ref}}\right) \qquad (2\text{-}18)$$

As close to center frequency, $S_{\theta_e}(f)\simeq\frac{f_{ref}}{3\cdot(N_T\cdot f)^2}\cdot\left(\frac{\pi f}{f_{ref}}\right)^2=\frac{\pi^2}{3\cdot N_T{}^2\cdot f_{ref}}$

The in-band transfer function is flat (Fig. 2-17 and Fig. 2-18), so it can't suppress the spurious effectively.

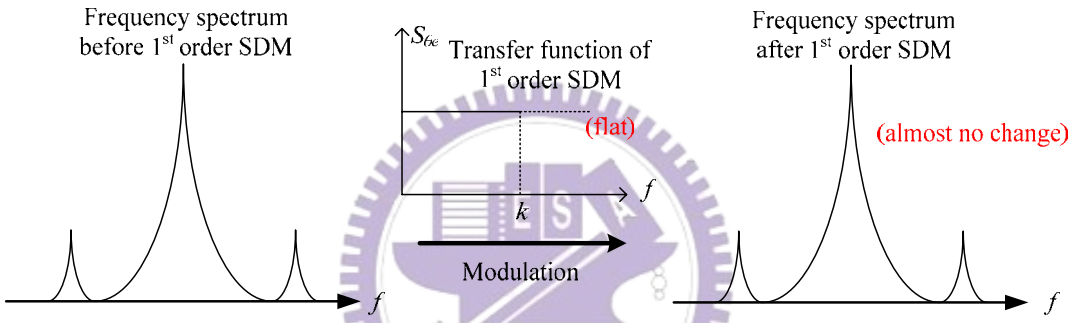


Fig. 2-17 Influence of first order sigma-delta modulator on signal power

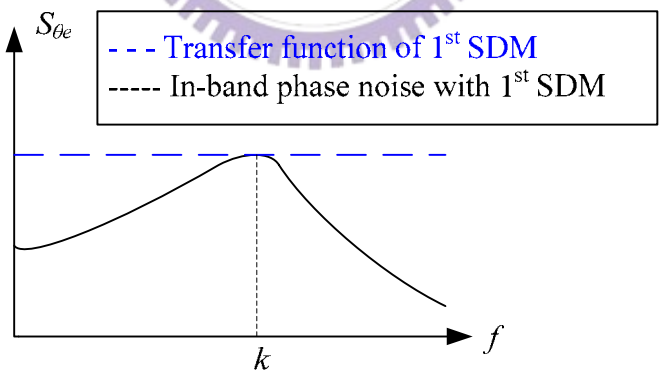


Fig. 2-18 Influence of first order sigma-delta modulator on in-band signal

♦ Third order sigma-delta modulator:

In order to transfer more quantization noise to high frequency offset, we adopt the third stage accumulators, as showing in Fig. 2-19. The transfer function is: (Fig. 2-20)

$$N[Z] = .f[Z] + (1 - z^{-1})^3 \times q_a[Z] \tag{2-19}$$

It means that quantization noise transfers to $q_e[Z] = (1 - z^{-1})^3 \times q_a[Z]$ 。

Hence the transfer function of quantization noise is:

$$H_{noise}(f) = \left(1 - z^{-1}\right)^3$$

$$H_{noise}(f) = \left|1 - \exp\left(-\frac{j2\pi f}{f_{ref}}\right)\right|^3$$

$$H_{noise}(f) = \left|1 - \cos\left(\frac{j2\pi f}{f_{ref}}\right) - j \cdot \sin\left(\frac{j2\pi f}{f_{ref}}\right)\right|^3$$

$$H_{noise}(f) = \left|2 \cdot \sin\left(\frac{\pi f}{f_{ref}}\right)\right|^3 \tag{2-20}$$

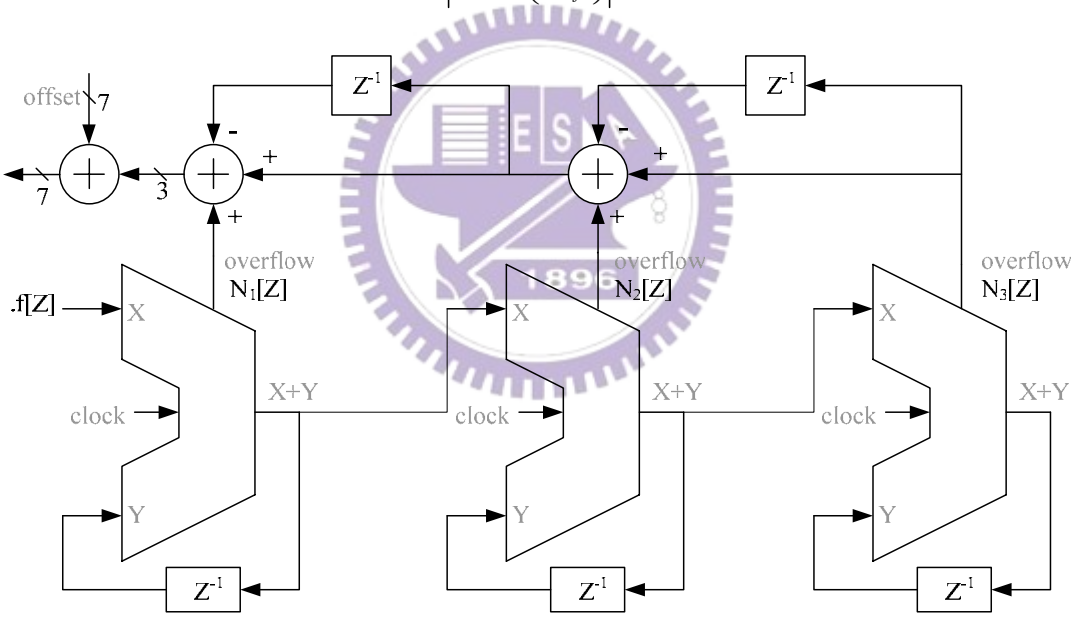


Fig. 2-19 Third order sigma-delta modulator

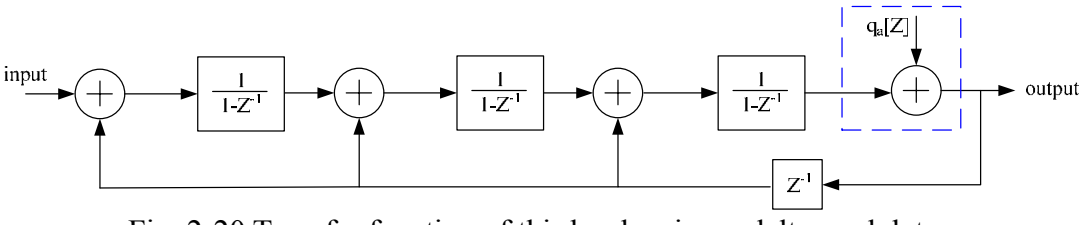


Fig. 2-20 Transfer function of third order sigma-delta modulator

Assume the ideal PFD of quantization noise is: $S_{q_a}(f) = \frac{1}{12 \cdot f_{ref}}$

So, the PFD of phase error is:

$$S_{\theta_e}(f)=\left(\frac{f_{div}}{f\times N_T}\right)^2\times\left\{\frac{1}{12\cdot f_{ref}}\cdot\left[2\cdot\sin\left(\frac{\pi f}{f_{ref}}\right)\right]^6\right\}=\frac{16\cdot f_{ref}}{3\cdot(N_T\cdot f)^2}\sin^6\left(\frac{\pi f}{f_{ref}}\right) \qquad (2\text{-}21)$$

As close to center frequency,

$$S_{\theta_e}(f)\simeq\frac{16\cdot f_{ref}}{3\cdot(N_T\cdot f)^2}\cdot\left(\frac{\pi f}{f_{ref}}\right)^6=\frac{16\cdot\pi^6\cdot f^4}{3\cdot {N_T}^2\cdot f_{ref}^5}$$

The in-band transfer function is proportional to 4th power of offset frequency (Fig. 2-21 and Fig. 2-22), so it can suppress the spurious effectively.

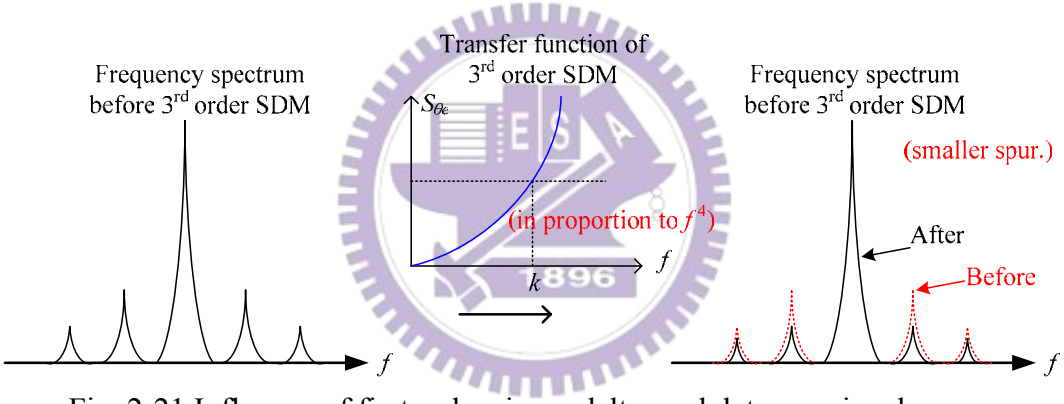


Fig. 2-21 Influence of first order sigma-delta modulator on signal power

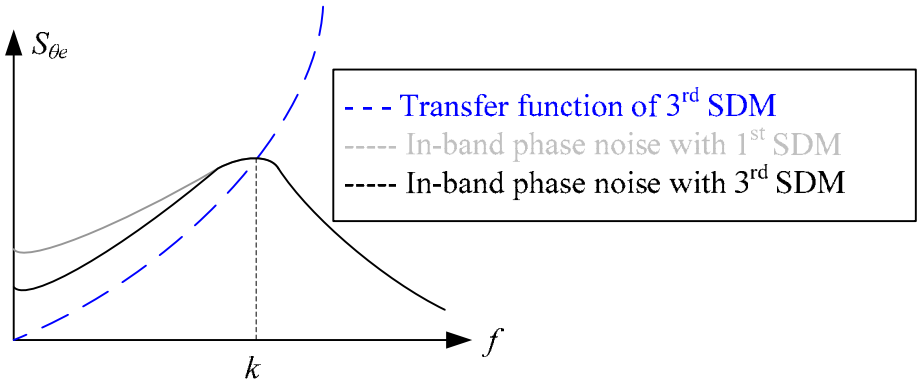


Fig. 2-22 Influence of first order sigma-delta modulator on in-band signal

Hence, we choose 3rd sigma-delta modulator in this fractional-N synthesizer design. The whole schematic of sigma-delta modulator is showing in Fig. 2-23.

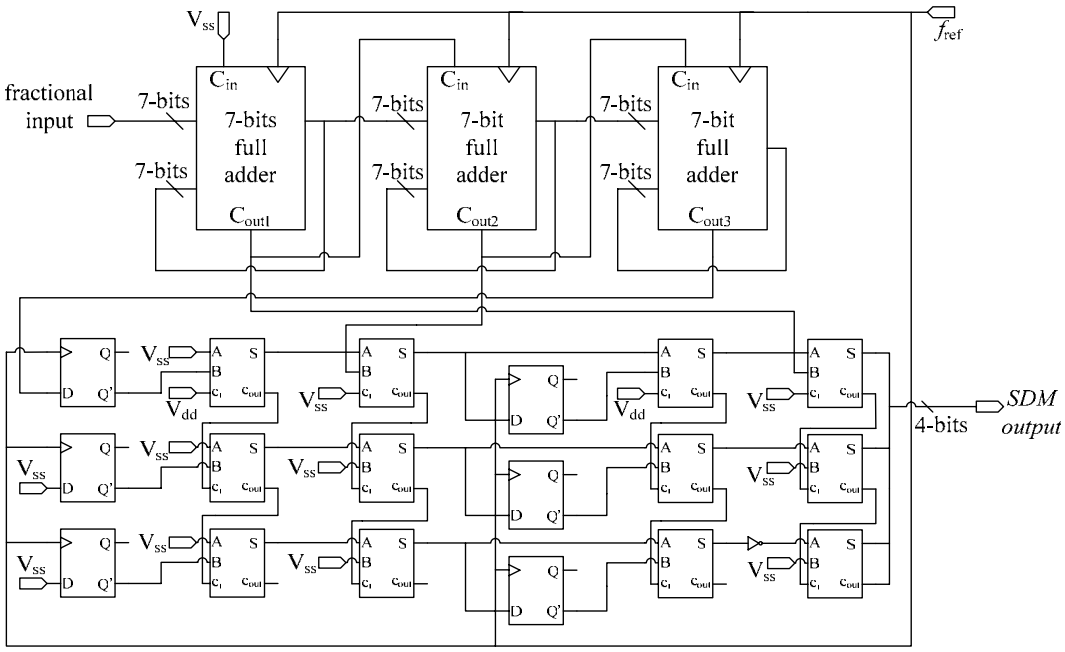


Fig. 2-23 Schematic of sigma-delta modulator in this synthesizer

2.2.3 Fully programmable multi-modulus frequency divider

Fully programmable multi-modulus divider is adopted to achieve both high-speed frequency division and moderate power consumption. Fig. 2-24 is the block diagram of a fully programmable multi-modulus frequency divider [5]. It is composed by 7 cascaded dual modulus asynchronous divide-by-2/3 circuits. This design assures only the first two stages of the divider works at the high frequency. We can set divide modulus N by changing the input level of each program bits (b_0, b_1, b_2…). In this design, our VCO frequency is about 2.4-GHz and divider can be programmed to all integers between 128 and 255, depending on the input bits b_0 to b_6 to divide the VCO frequency down to 16-MHz of reference frequency. The programmable dividing ratio is:

$$N = 2^7 + \sum_{n=0}^{6} b_n \cdot 2^n = 128 + \sum_{n=0}^{6} b_n \cdot 2^n \qquad (2\text{-}22)$$

The simple logic of the AND/OR-gates assures the modulus signals of the last

stages are produced first and given to the next stage. Thus the delay of the first divider stage is minimized.

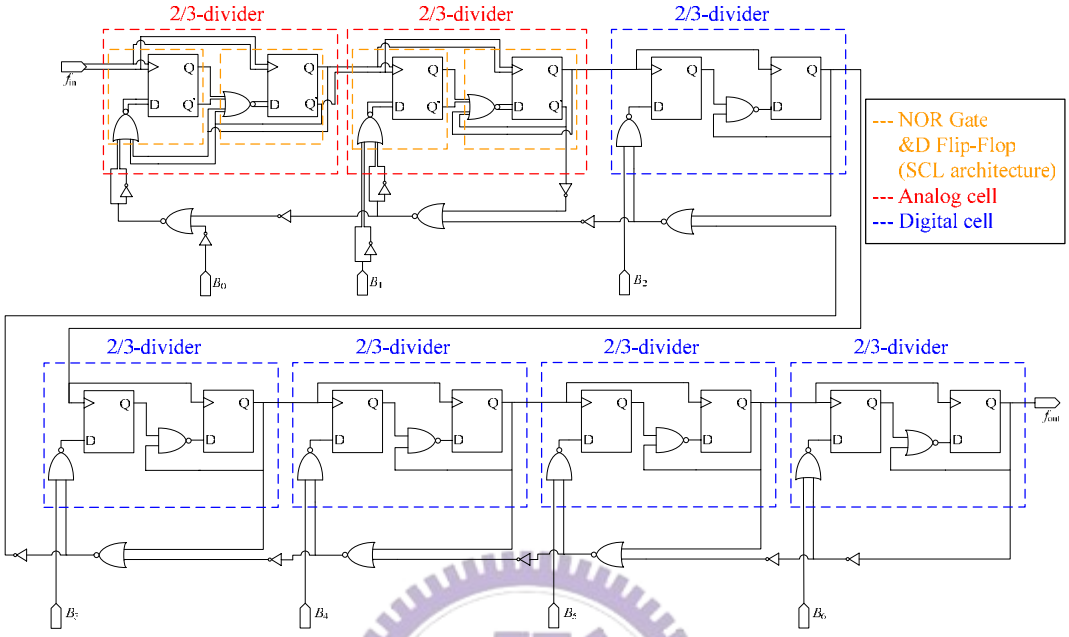


Fig. 2-24 Fully programmable multi-modulus frequency divider

The common choice of the frequency divider architecture in frequency synthesizer is usually phase-switching circuit or programmable pulse-swallow counter. These techniques have lower flexibility. Therefore, fully programmable multi-modulus divider architecture [5] is adopted in this fully integrated integer-N synthesizer circuit, which is simple, easy to implementation. Besides, compared with other divider architecture, more important point is the delay time of every stage only related to next stage that can reduce divider error. Such architecture only requires change the number of divide-by-2/3 block for different range of divider. No power hunger preamplifier or buffer is needed to drive the divider.

Frequency divider is also a critical part besides VCO because of its high operating speed. Just like mentioned above, the first stage of the divider works at the high speed (at 2.4-GHz). The maximum operating frequency is limited by the parasitic capacitance of the feedback of the first stage. In order to reach a maximum

operate frequency at 2.5-GHz, the first stages are realized in a differential Source Coupled Logic (SCL) and logic gates are embedded in it (Fig. 2-25). This architecture requires smaller signal swing from VCO outputs [5]. Although true single phase clock (TSPC) flip-flops divider cell architecture has less power consumption, it requires almost full swing signals to complete divided-two function. However, the maximum operating speed is limited by the parasitic capacitance of the feedback of the first stage. The very accurate layout of first stage is necessary to reduce the parasitic components.

The following 5 stages are realized with less power-hungry single ended digital cells, which provide a maximum operating frequency of several hundred MHz to lower the total current consumption.

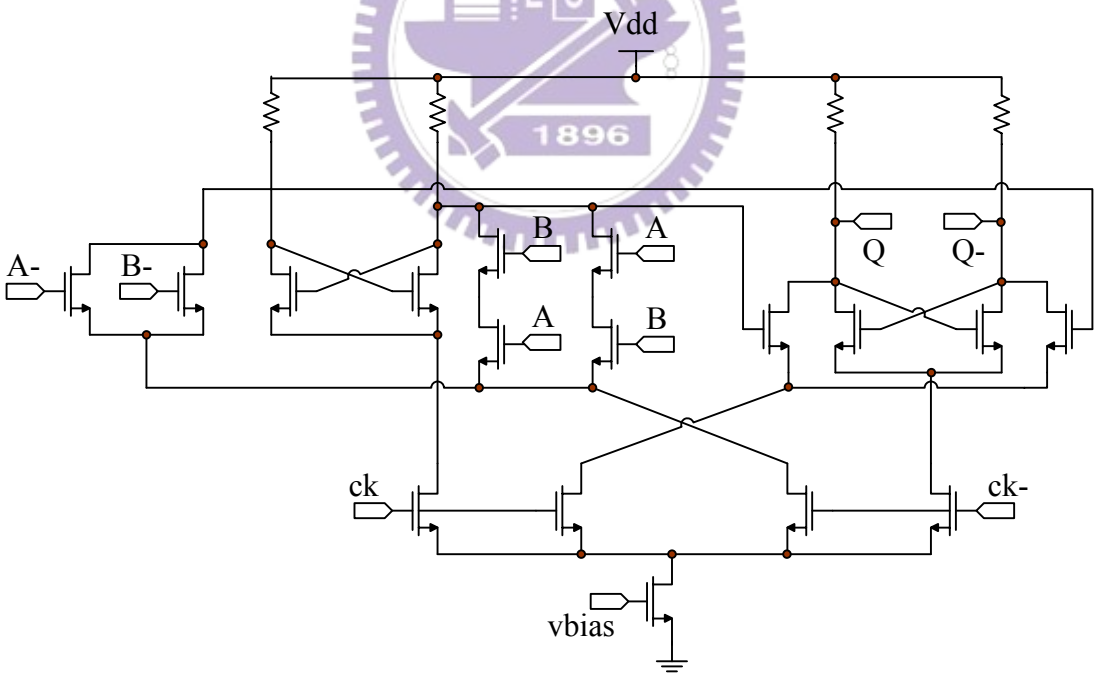


Fig. 2-25 Differential source coupled logic (SCL)

The co-simulation result of fully programmable frequency multi-modulus divider and VCO is as shown in Fig. 2-26. The VCO output frequency is set at 2400-MHz and the divide modulus is set at 150, too. We can obviously observe the period of output

divided signal is 62.5ns, this figures out our divider is working regularly.

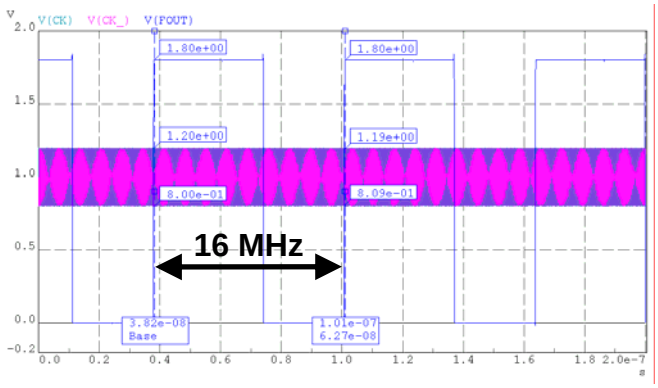


Fig. 2-26 Output signal of frequency divider simulated with VCO

2.2.4 Phase frequency detector

We choose three state phase frequency detector (PFD) for the design. A conventional three state PFD is widely used in many purposes for its simplicity, wide linear range of ±2π radians. Another significant excellence is it detects both phase and frequency.

Fig. 2-27 shows the schematic of a three state PFD. Flip-flops FF1 and FF2 are falling edge-triggered D-flip-flops with their D input connected to Vdd. The clock of FF1 is connected to the reference signal f_{REF}; and FF2 is clocked with the output of the frequency divider f_{div} (Fig. 2-28). If the falling edge of f_{REF} arrives before the falling edge of f_{div}, output upp is set to speed up the VCO. In a different case if the falling edge of f_{div} arrives prior to the falling edge of f_{REF}, the VCO is faster than the reference signal and dwp is set to slow down the VCO. In either condition the falling edge of the late signal resets both upp and dwp. The next cycle starts with the next falling edge of f_{div} or f_{REF}.

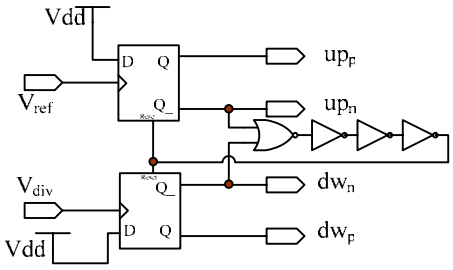


Fig. 2-27 Phase frequency detector circuit

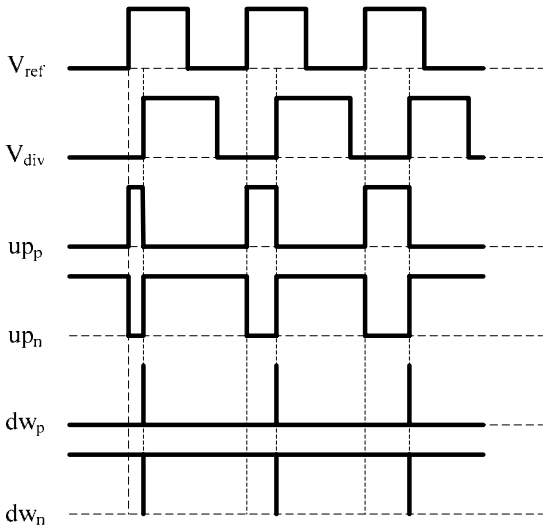


Fig. 2-28 Phase frequency detector timing diagram

However, this topology of PFD has a serious limitation for its "dead zone". In the case the reset signal is not delayed sufficiently, the output of charge pump will not change for small phase error (as shown in Fig. 2-29). Dead zone causes a jitter in PLL and should be removed. For this purpose, we add inverter chains to form a delay chain in reset path, generate enough delay to eliminate the dead zone of the PFD [30].

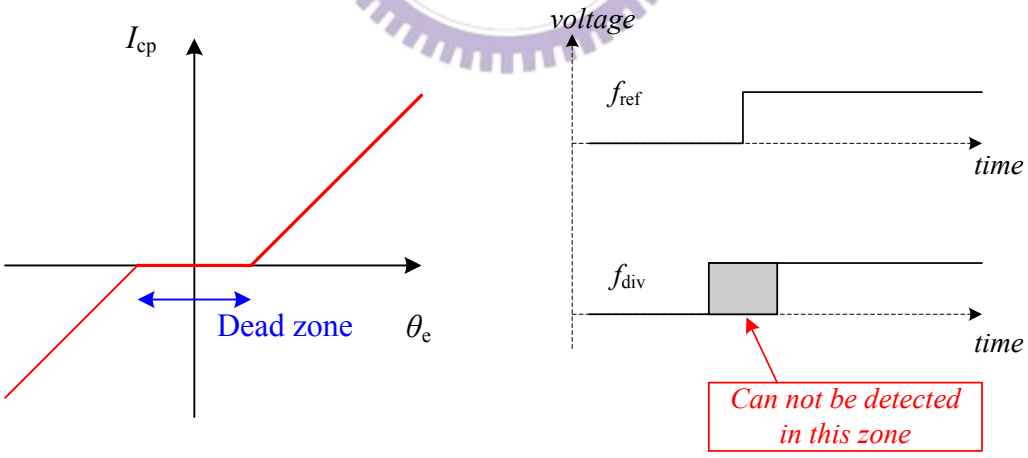


Fig. 2-29 Limitation caused by dead zone

2.2.5 Charge pump

The charge pump [5] (Fig. 2-30) adopted in this project works with a fixed reference current. To achieve a high voltage output range at the charge pump, the

transistor size of the current mirror transistors (M_1 - M_{11}) must be designed carefully. Also an accurate layout of the charge pump is important to improve the matching of the positive and negative current to avoid mismatch currents. Mismatch current may cause spurious tones and interfere with adjacent channel in RF receiver; it also produces undesired spectral emission in RF transmitter. We implement two additional transistors (M_{12}, M_{14}). They guarantee in case of switching the transistors M_{13} and M_{15}, their sources are already pre-charged. Above reduces current peaks during the switching time and suppressing the spurious tones, too. According to our design, the simulation of current I_{cp} is about 76μA and the corresponding power consumption is 0.9mW.

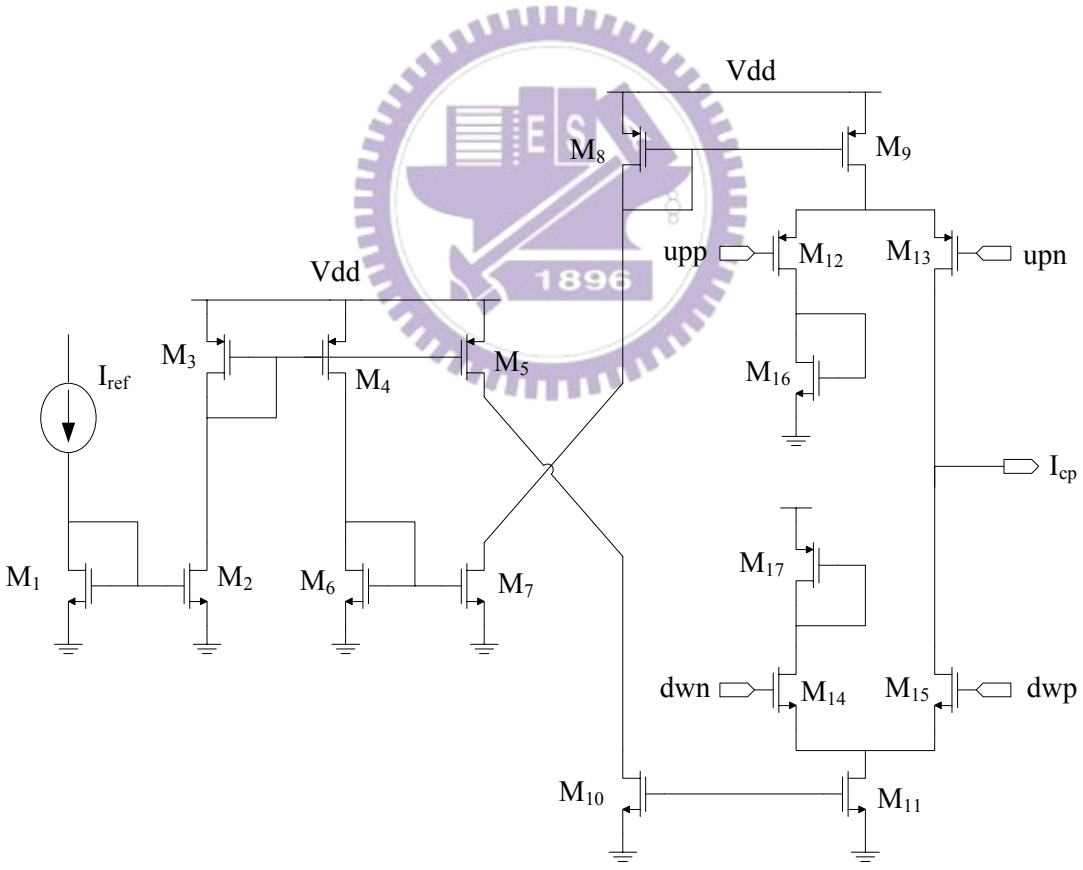


Fig. 2-30 Schematic of charge pump

We can test the PFD and charge pump together. The inputs of PFD feed two signals which has variable phase difference in order to observe output current of charge pump. Fig. 2-31 shows the phase difference versus average output current of

charge pump.

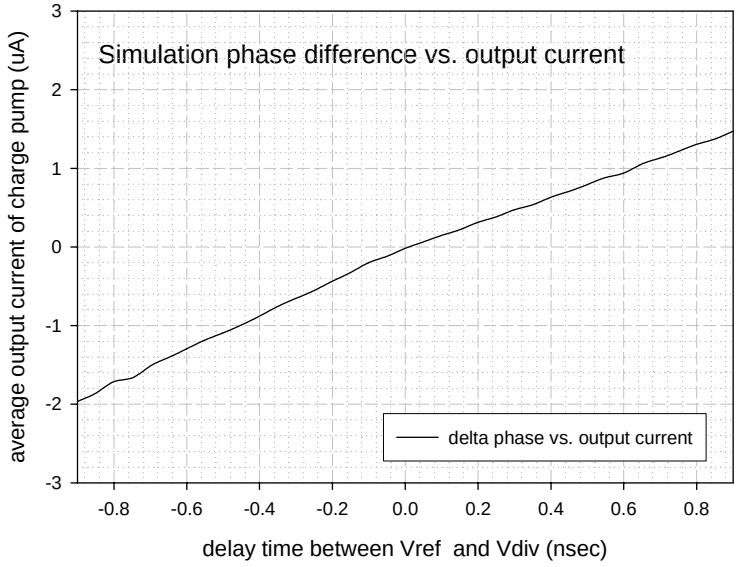


Fig. 2-31 Phase difference versus average output current

2.2.6 Loop filter

The characteristic of PLL helps frequency synthesizers partially alleviate their phase noise contributed by VCO. Extending the band width of PLL can reduce sideband phase noise. However, a wide band PLL suffers from higher level of spurious tones.

We adopt 3rd order passive loop filter for our design. Fig. 2-32 shows a standard third order loop filter used in most synthesizers. This comprises a second order filter section and an RC section providing an extra pole to assist the attenuation of the side bands at multiples of the comparison frequency that may appear. Use the simulated tool (Fig. 2-33) to find the suitable values of loop filter component.

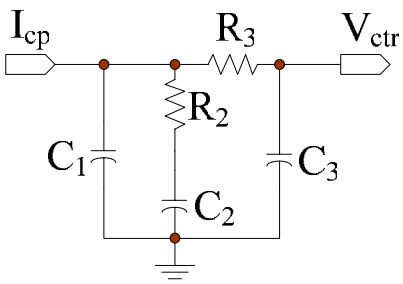


Fig. 2-32 Third order loop filter

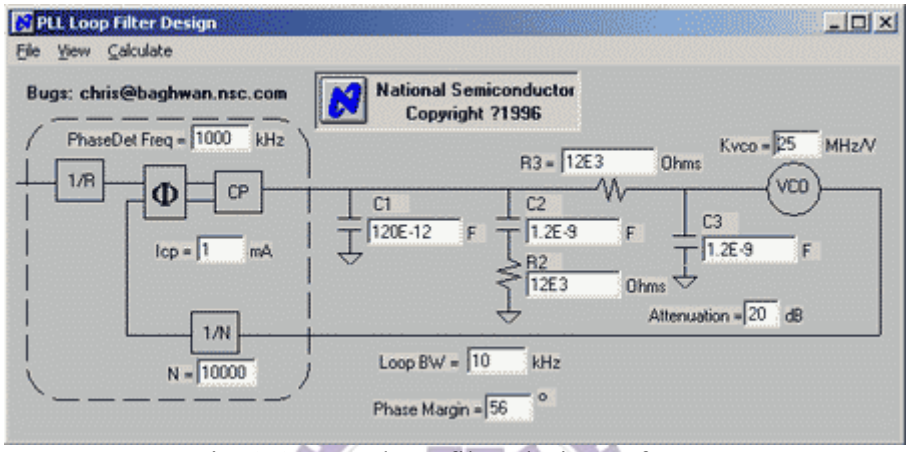


Fig. 2-33 PLL loop filter design software

Based on simulation results, we can obtain a set of element values. The optimized values are shown in Table 2-1.

Table 2-1 Optimized loop filter elements

Component	Value
C1	47pF
C2	820pF
R2	5.1kΩ
C3	39pF
R3	5.1kΩ

2.3 Whole circuit simulation and layout

All of the building blocks mentioned in previous sections will be combined to be a whole frequency synthesizer and simulated together. Fig. 2-34 shows the whole circuit schematic. Synthesizer circuit contains many sub-circuits; whole circuit simulation takes a lot of time. At first, we use MATLAB software to perform behavioral simulation of frequency synthesizer's settling time. And then we choose Eldo RF as our simulation tool to verify whether the connections of whole loop are correct or not.

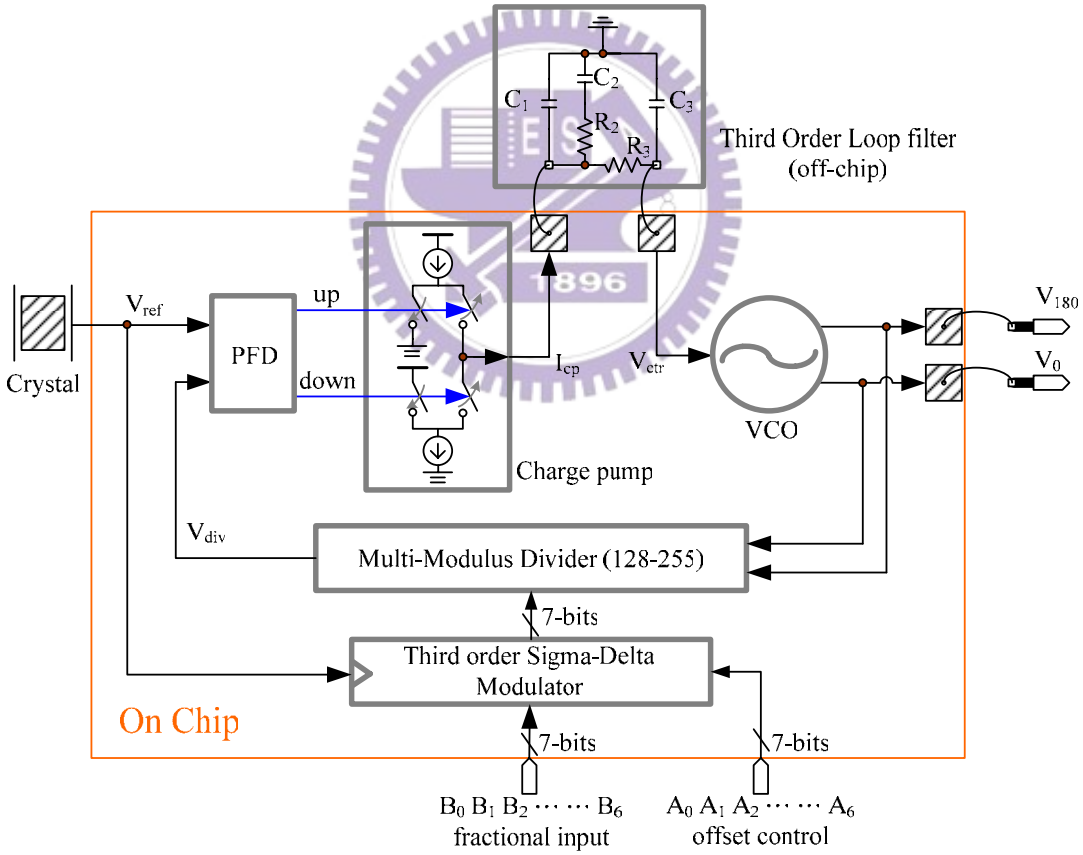


Fig. 2-34 Building blocks of sigma-delta fractional-N frequency synthesizer

Based on behavior level simulation result, the phase margin is more than 50 degree and the settling time is about 30μs, as shown in Fig. 2-35 and Fig. 2-36. After transistor level simulation with Eldo RF, the settling time is less than 30μs, as shown

in Fig. 2-37. It shows the settling time less than 200μs as the spec. of WLAN and Bluetooth systems requirement.

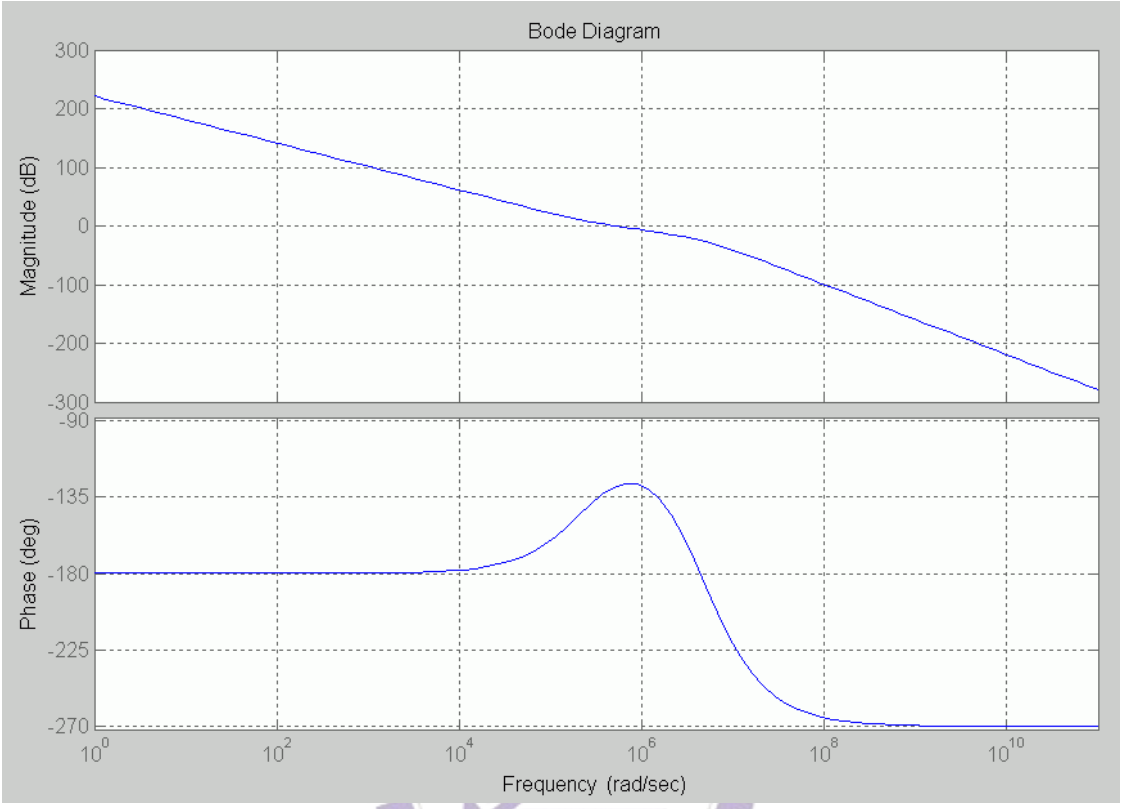


Fig. 2-35 Whole circuit open loop simulation (Behavior level)

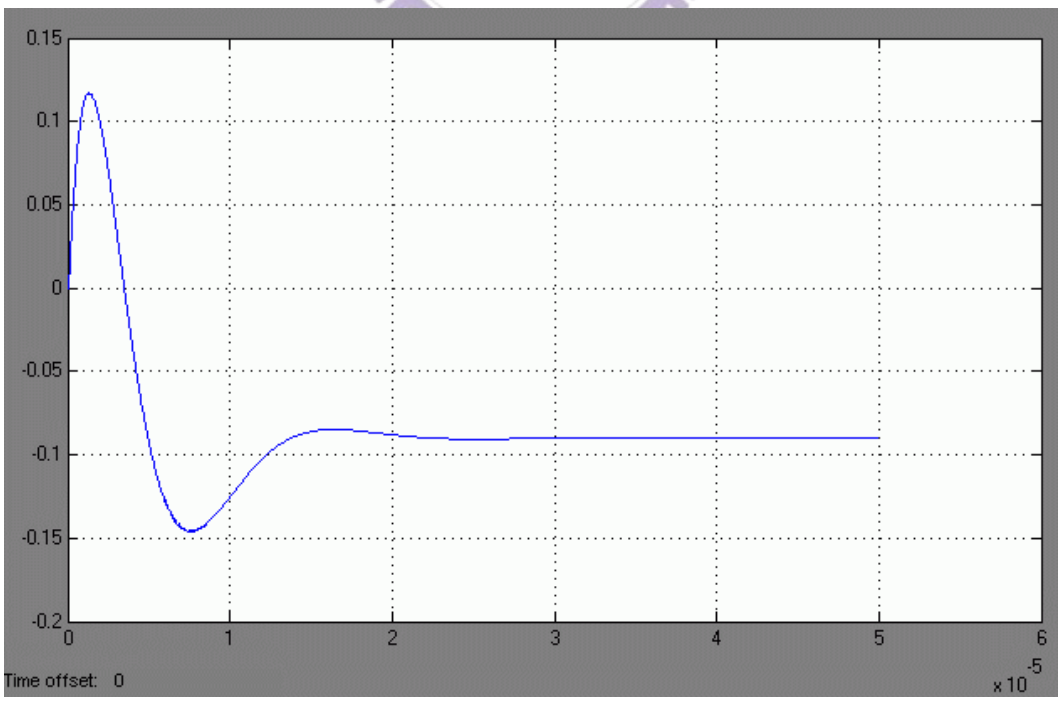


Fig. 2-36 Whole circuit close loop simulation (Behavior level)

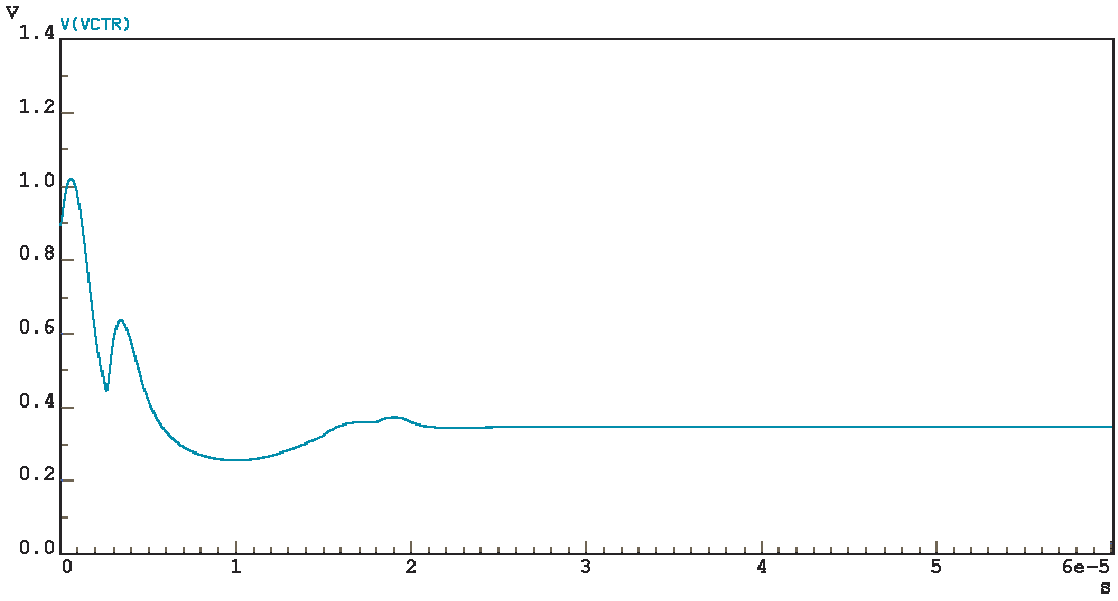


Fig. 2-37 Locking transient simulation (Transistor level)

Fig. 2-38 shows the output spectrum of SDM frequency synthesizer after Fast Fourier Transformation (FFT) of VCO output transient and Fig. 2-39 shows the output spectrum of traditional fractional-N frequency synthesizer. We can see that in-band spurious tone of the former is less than the latter.

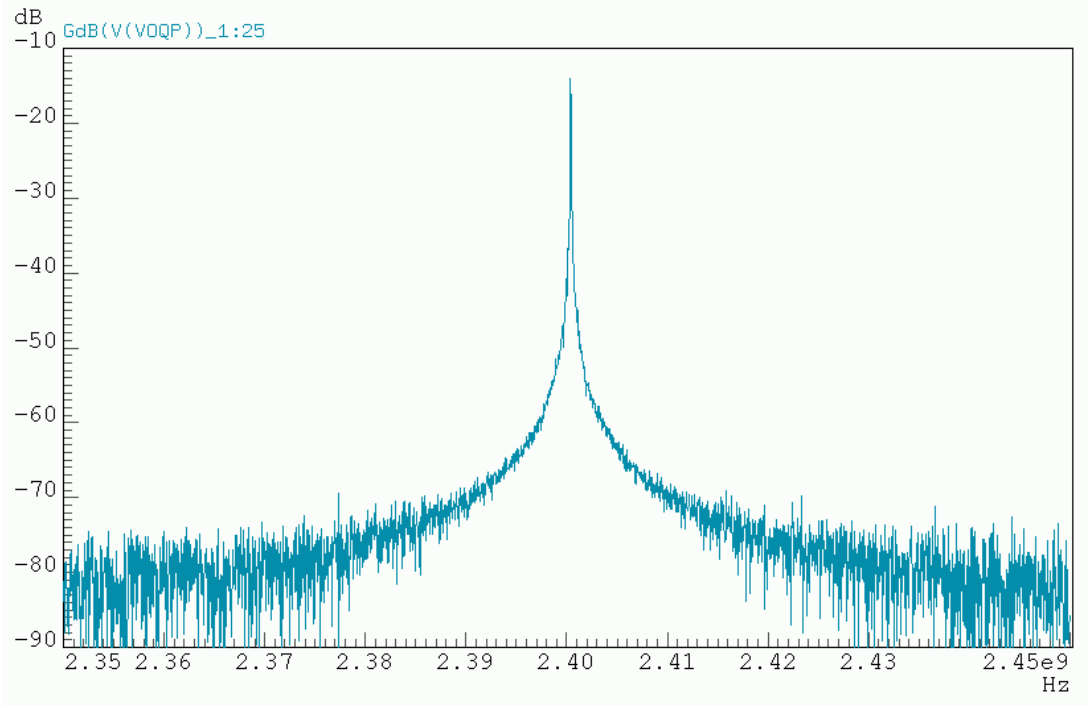


Fig. 2-38 Output spectrum of sigma-delta fractional-N frequency synthesizer

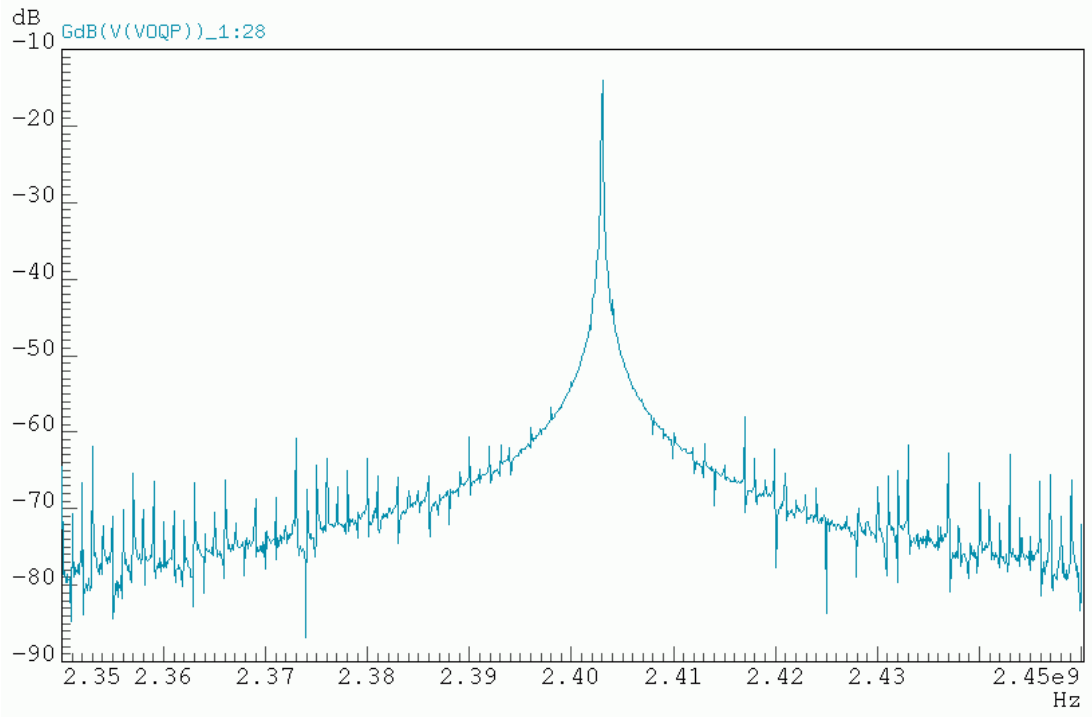


Fig. 2-39 Output spectrum of traditional fractional-N frequency synthesizer

Fig. 2-40 shows the layout of whole chip and Fig. 2-41 shows the die-photograph of whole chip. The die size is roughly 1150μm×1000μm.

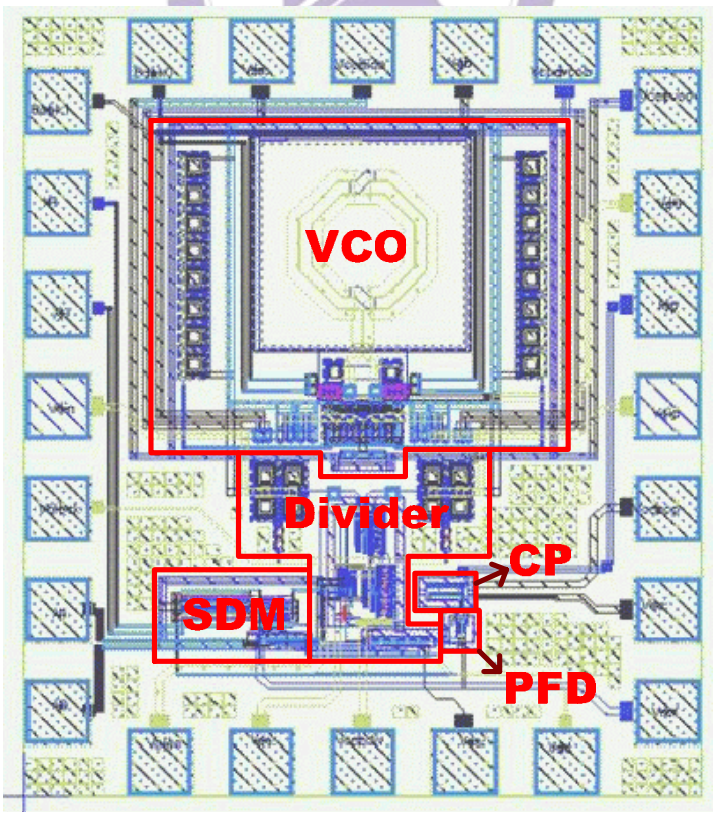


Fig. 2-40 Layout of sigma-delta fractional-N frequency synthesizer

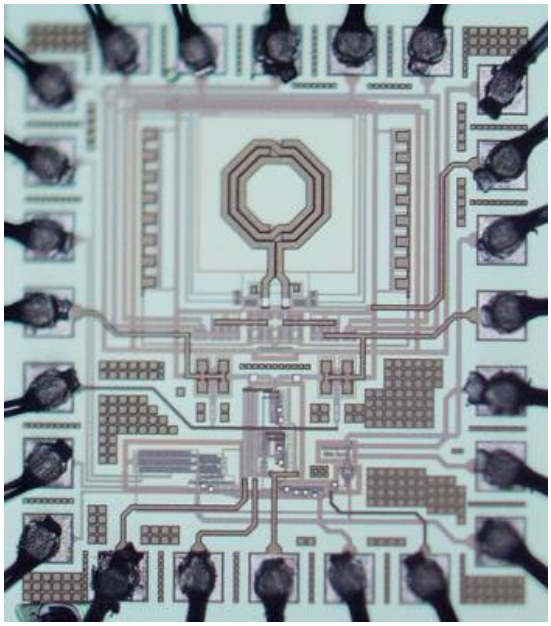


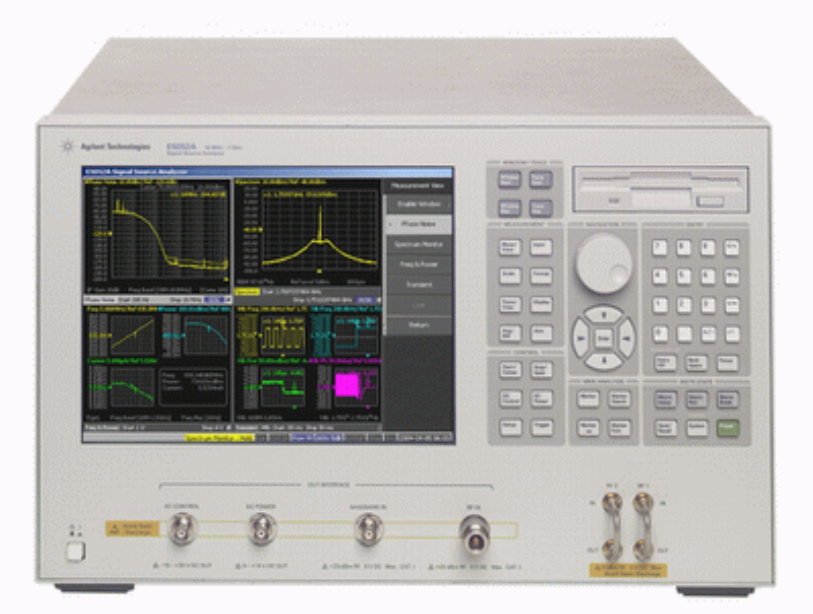
Fig. 2-41 Die-photograph of sigma-delta fractional-N frequency synthesizer

Table 2-2 Performance summary of sigma-delta fractional-N synthesizer

Post-simulation (PEX-C)	**TT corner**	**FF corner**	**SS corner**
Power supply	1.8 V		
Crystal frequency	16-MHz		
VCO bank condition	(B1, B0)=(1, 0)	(B1, B0)=(1, 1)	(B1, B0)=(0, 0)
VCO tuning range	2.347 ~ 2.561GHz 214MHz	2.318 ~ 2.505GHz 187MHz	2.337 ~ 2.600GHz 263MHz
Phase noise (dBc/Hz)	-118.0 @1MHz -129.0 @3MHz	-120.2 @1MHz -127.1 @3MHz	-112.6 @1MHz -129.5 @3MHz
Settling time	30μs	-	-
VCO power consumption	One core circuit: 4.6mW Two buffer stages: 6.1mW	One core circuit: 5.8mW Two buffer stages: 7.7mW	One core circuit: 3.6mW Two buffer stages: 4.7mW
Prescaler power consumption	10.2mW	13.6mW	7.9mW
CP power consumption	0.9mW	1.5mW	0.8mW
Total power consumption	22.1mW	28.6mW	17.0mW

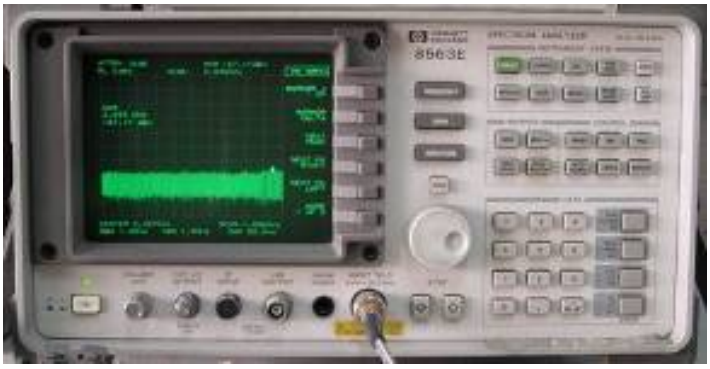
2.4 Measurement results

This work is bond-wire measurement on PCB. The measuring equipment for VCO and frequency synthesizer contains Agilent E5052A signal source analyzer (Fig. 2-42a, at CIC), Agilent E4407B spectrum analyzer (Fig. 2-42b, at CIC), HP 8563E spectrum analyzer (Fig. 2-42c, at LAB), HP 54610B oscilloscope (Fig. 2-42d, at LAB), HP E3611A power supply (Fig. 2-42e, at LAB), and HP 33120A function generator (Fig. 2-42f, at LAB). The above measuring equipment is also used in the following chapters.

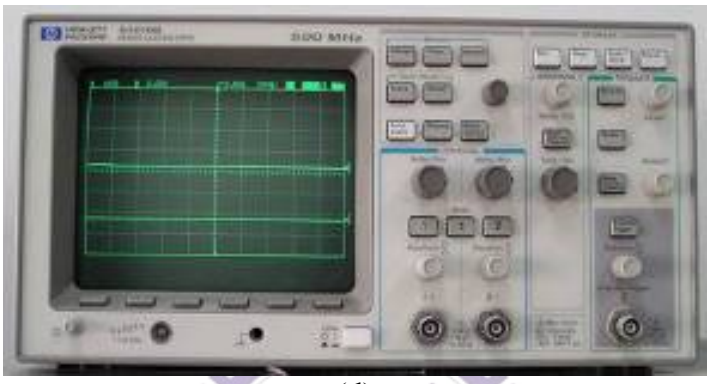


(a)

(b)



(c)



(d)

(e)

(f)

Fig. 2-42 Measurement instruments
(a) Agilent E5052A signal source analyzer (b) Agilent E4407B spectrum analyzer
(c) HP 8563E spectrum analyzer (d) HP 54610B oscilloscope
(e) HP E3611A power supply (f) HP 33120A function generator

Fig. 2-43 shows the testing board. The chip is stuck on testing PCB, and wires are bonded from the pad on chip to feed bias voltages. An off-chip 16-MHz crystal oscillator instead of function generator is used to produce reference clock for suppressing the noise coming from reference signal. The loop filter is also designed off-chip for easily modifying element values and decrease chip area although it introduces more noise than designed fully on-chip.

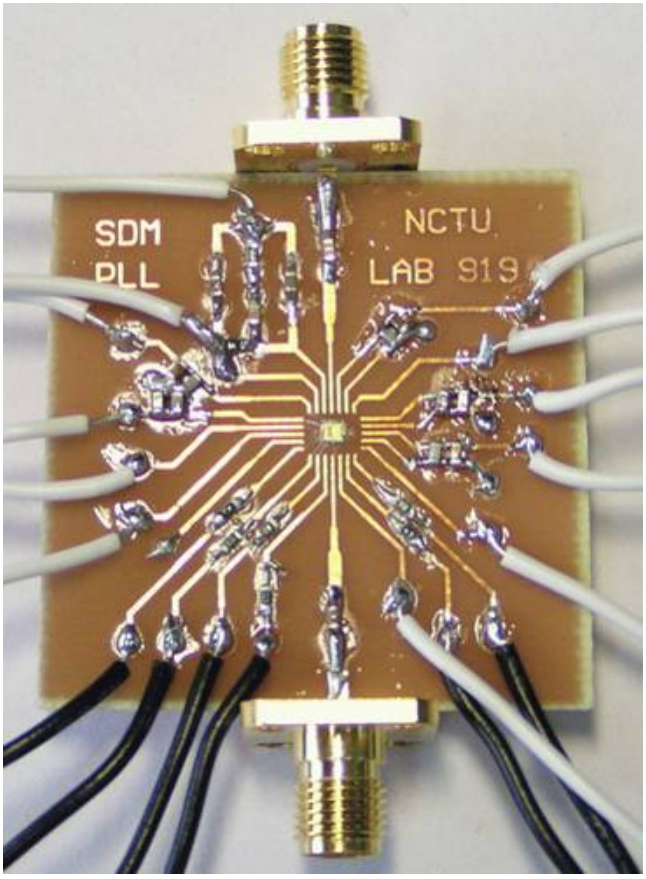


Fig. 2-43 Testing board of sigma-delta fractional-N frequency synthesizer

2.4.1 VCO measurement results

The measured tuning curve and spectrum of VCO used in this work is shown as following figures. We can obviously observe that all the bank conditions (from 00 to 11) are all contains the frequency area we need, i.e. whether the oscillator is set in which bank condition, the frequency synthesizer may lock successfully. The tuning curve at bank 00, 10, and 11 is shown in Fig. 2-44.

The measured tuning range is 2.381 ~ 2.606-GHz (at bank condition 10), comparing with our simulation results, the tuning range is 2.347~2.561-GHz at TT corner, it's approximately equal to simulation result (Fig. 2-45). But there's still a little difference when control voltage is approximately 0V and 1.8V. While control voltage is about 0.9V, tuning curve is almost linear, the same as simulation result. That means the extra parasitic effects are perfectly evaluated during our simulation.

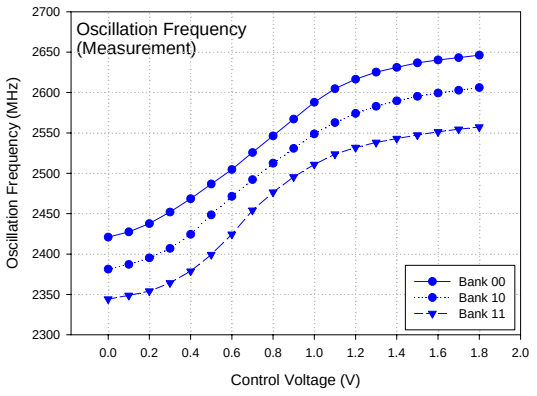


Fig. 2-44 Measured tuning curve of VCO in this synthesizer under different bank conditions

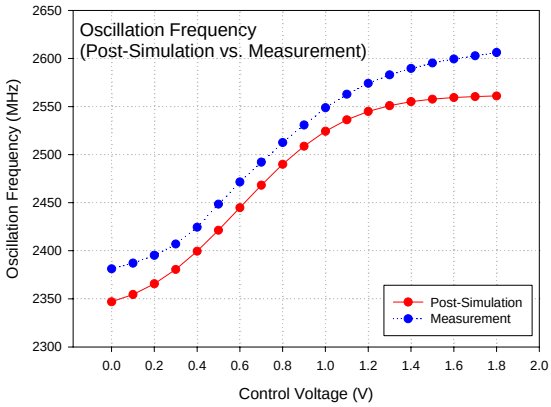


Fig. 2-45 Tuning curve of VCO in this synthesizer at bank 10 (Simulation vs. measurement)

The tuning range is just as the original design. Next we measure phase noise performance of this circuit. We adopt the measurement at lab with analog power supply. The measured phase noise @ 1-MHz offset form the carrier is -118.44dBc/Hz,

as shown in Fig. 2-48. Comparing with simulation results, the phase noise is -118.44dBc/Hz @ 1-MHz offset at TT corner, it's approximately equal to simulation result.

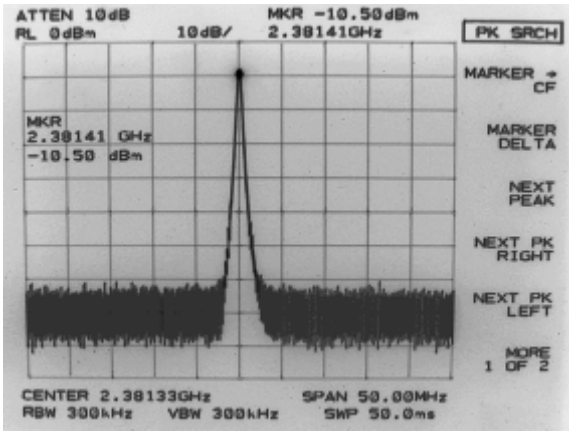


Fig. 2-46 Measured output spectrum of VCO in this synthesizer

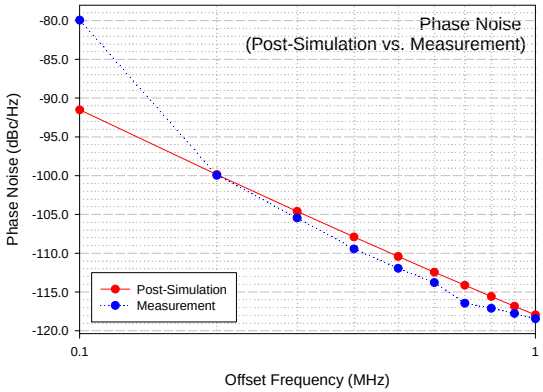
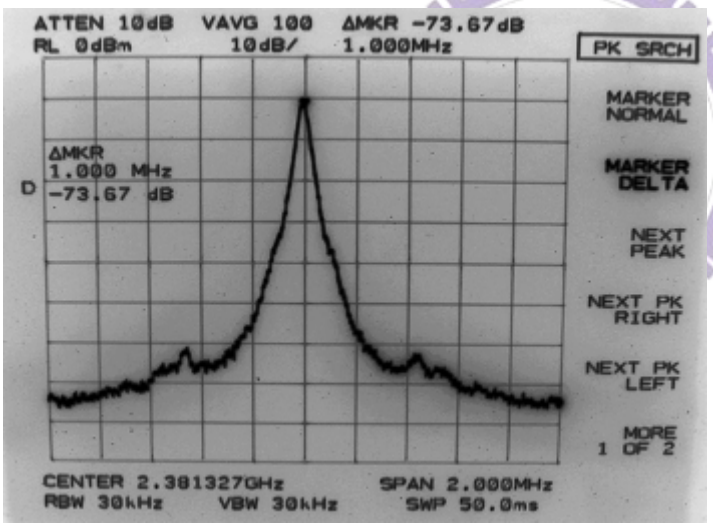


Fig. 2-47 Phase noise of VCO in this synthesizer (Bank 10, at LAB)



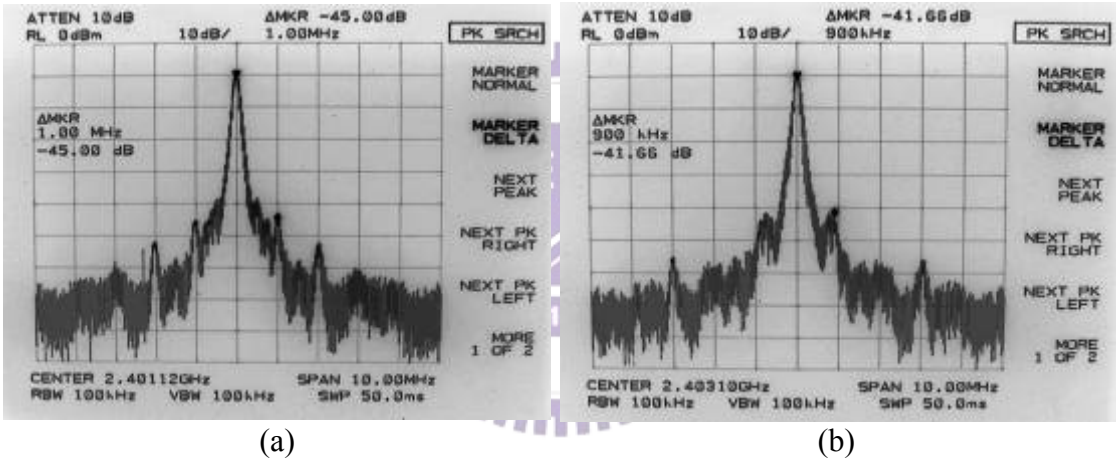
$$-73.67dB - 10\log(30 \cdot 10^3)$$
$$= -118.44dBc/Hz$$
@ 1MHz offset

Fig. 2-48 Measured phase noise of VCO in this synthesizer @ 1-MHz offset (Bank 10)

2.4.2 Whole circuit measurement results

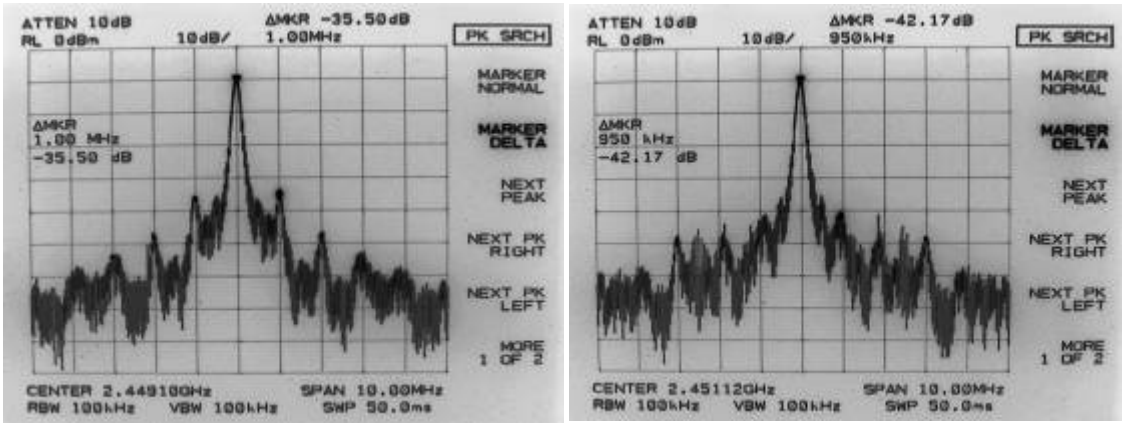
We measure this close-loop circuit at LAB, using HP 8563E spectrum analyzer. The whole sigma-delta fractional-N synthesizer's measurement data are shown in following figures. Fig. 2-49 is the output spectrum while synthesizer locked at 2401-MHz, 2403-MHz, 2449-MHz, 2451-MHz, 2481-MHz, and 2483-MHz. These

fractional inputs are reduction of a fraction so that the spur tones are more terrible. Next we observe other fractional inputs which are unable to reduce a fraction. Fig. 2-50 is the output spectrum while synthesizer locked at 2401.125-MHz, 2403.125-MHz, 2449.125-MHz, 2451.125-MHz, 2481.125-MHz, and 2483.125-MHz. We can see that the spur tones are better than that at the former condition. When fractional input is 25/128, the spurious tones over carrier of synthesizer is -47.83dB ~ -56.50dB. The spur tones of this fractional-N type synthesizer are better than that of integer-N type synthesizer. Fig. 2-51 shows the reference spur tones which are less than -50dBc @16MHz.



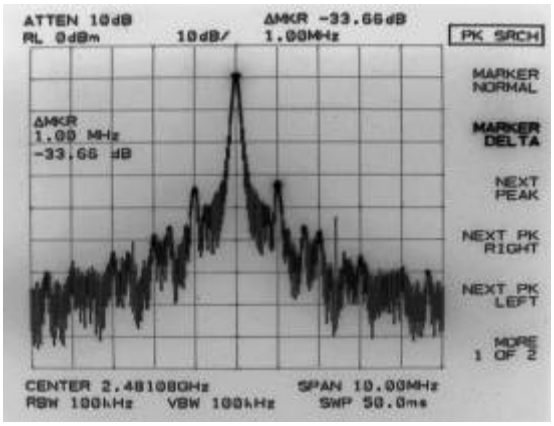
(a)
fractional input=(8/128)
divider ratio=150

(b)
fractional input=(24/128)
divider ratio=150

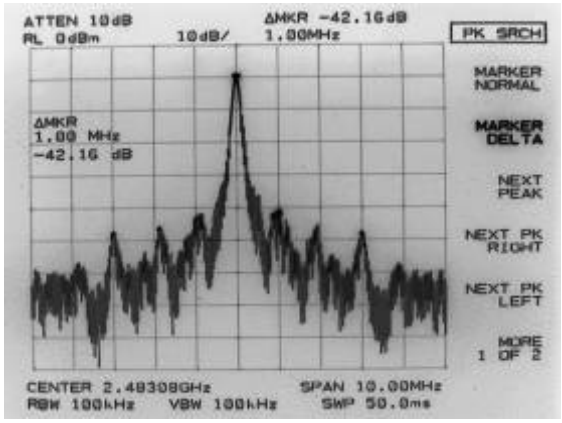


(c)
fractional input=(8/128)
divider ratio=153

(d)
fractional input=(24/128)
divider ratio=153

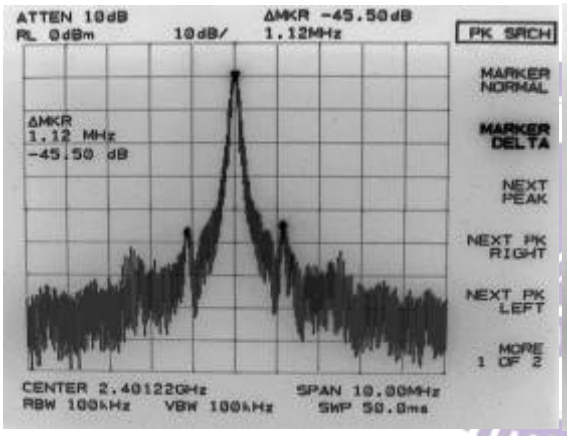


(e)
fractional input=(8/128)
divider ratio=155

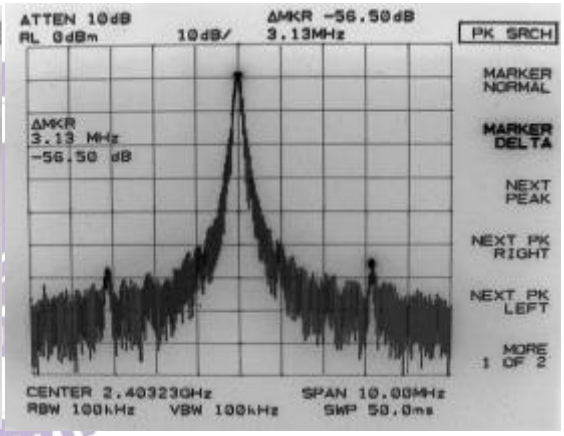


(f)
fractional input=(24/128)
divider ratio=155

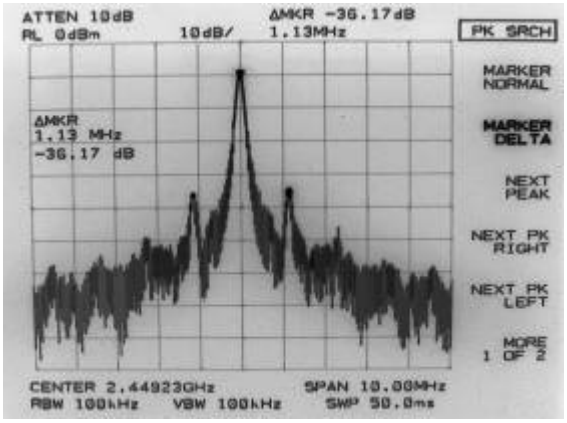
Fig. 2-49 Measured locking spectrum
(a) at 2401MHz (b) at 2403MHz (c) at 2449MHz
(d) at 2451MHz (e) at 2481MHz (f) at 2483MHz



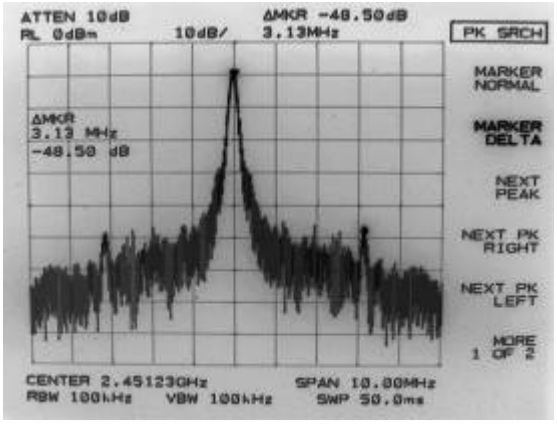
(a)
fractional input=(9/128)
divider ratio=150



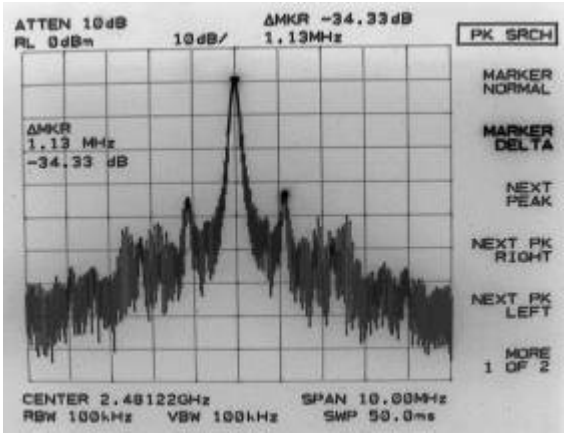
(b)
fractional input=(25/128)
divider ratio=150



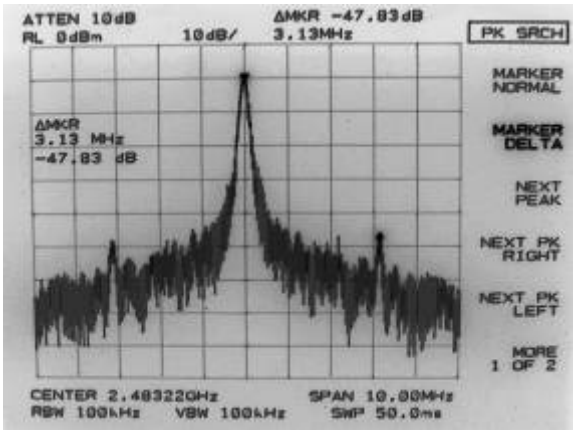
(c)
fractional input=(9/128)
divider ratio=153



(d)
fractional input=(25/128)
divider ratio=153



(e)
fractional input=(9/128)
divider ratio=155



(f)
fractional input=(25/128)
divider ratio=155

Fig. 2-50 Measured locking spectrum
(a) at 2401.125MHz (b) at 2403.125MHz (c) at 2449.125MHz
(d) at 2451.125MHz (e) at 2481.125MHz (f) at 2483.125MHz

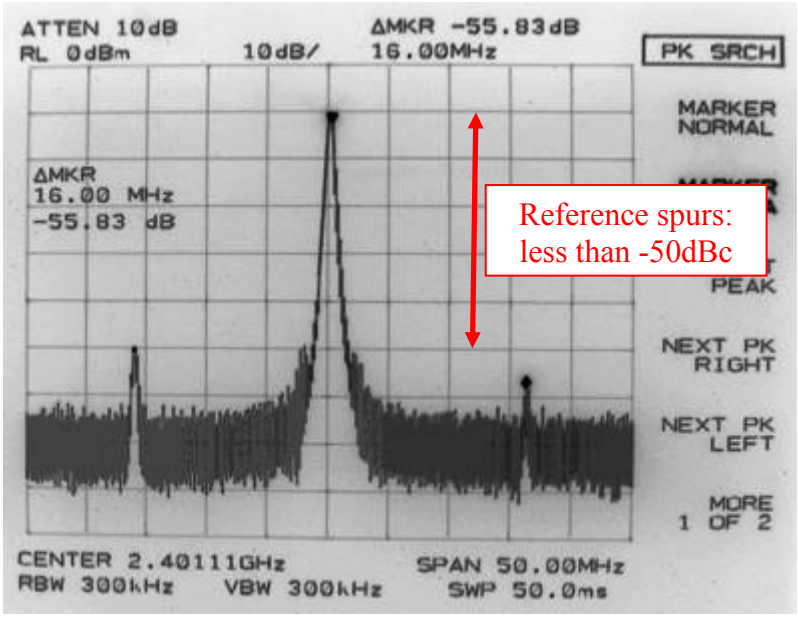
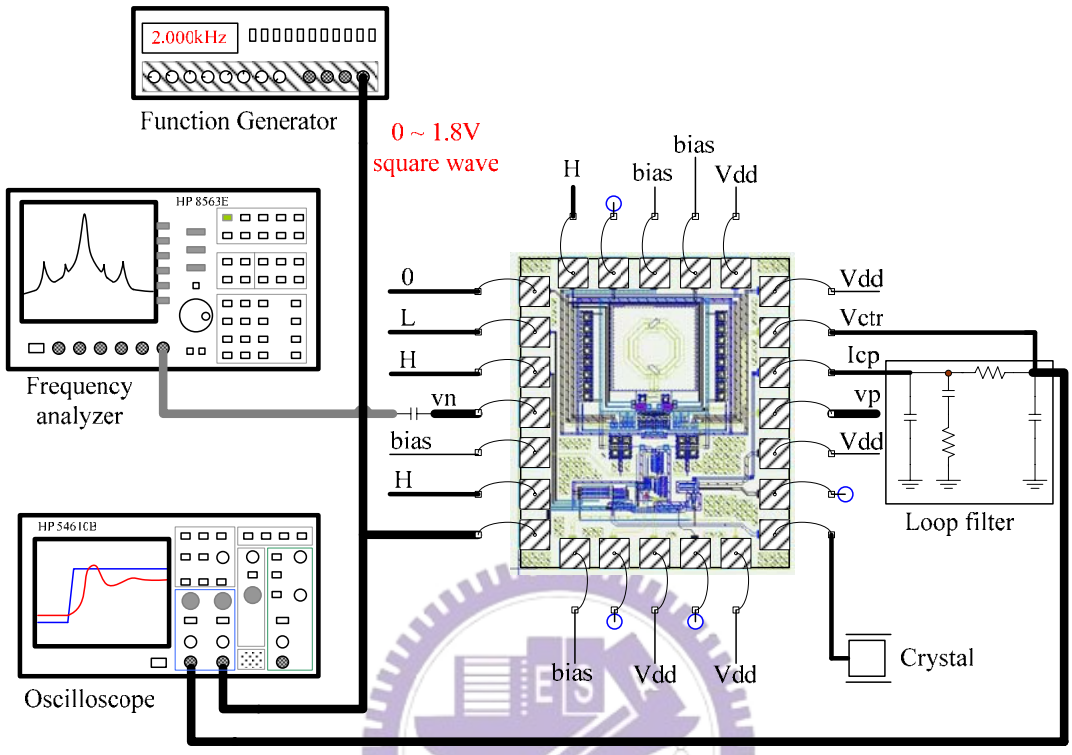


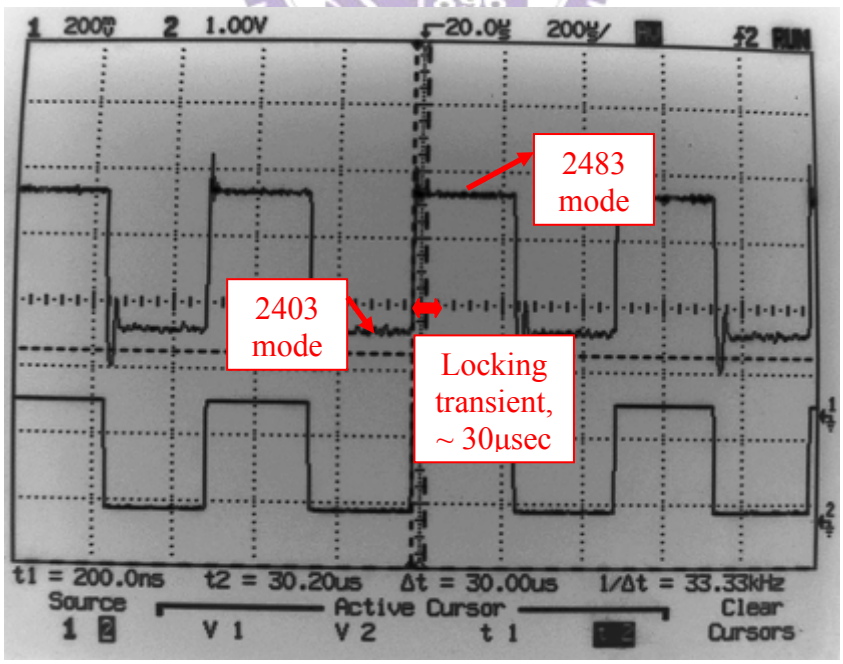
Fig. 2-51 Measured reference spurs of locking spectrum

Next we use the function generator as a trigger source. The measurement consideration of settling time is showing in Fig. 2-52a. The function generator outputs low frequency signal to feed the control bit of multi-modulus divider. It results that the output frequency is changed between 2403-MHz and 2483-MHz. So we can measure the settling time using a normal oscilloscope. Fig. 2-52b and Fig. 2-52c are the VCO input control voltage node waveforms. They represent the locking transient

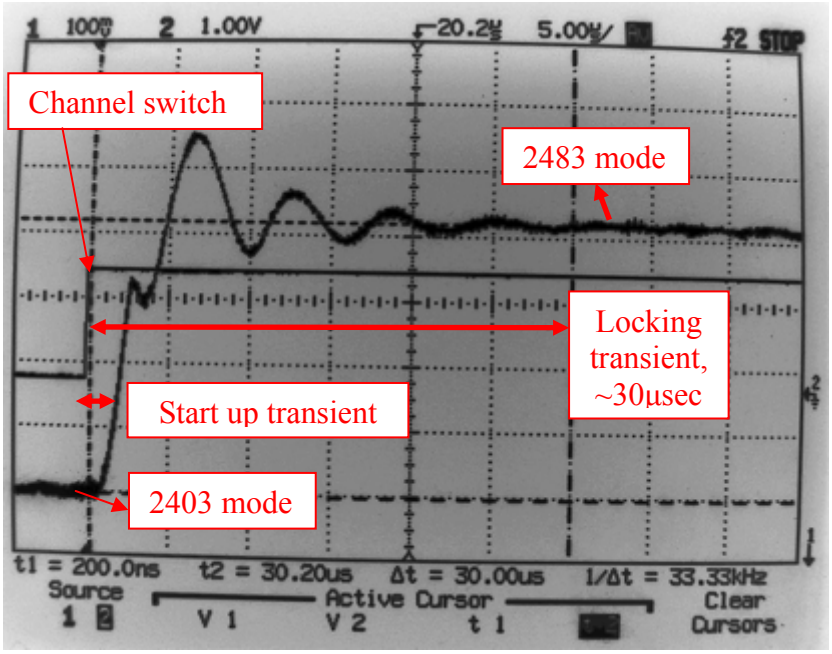
waveforms of this frequency synthesizer. The locking settling time shows it is less than 30μs.



(a)



(b)



(c)

Fig. 2-52 (a) Measurement consideration of settling time
(b) Transient of settling time
(c) Zoom in of the transient of settling time

2.5 Measurement Discussion

The simulation and measurement results of power consumption are very close, and all parts work successfully. Based on measurement results, the tuning range and phase noise is close to simulation results. But the spur performance is not acceptable. We can reduce the loop bandwidth of loop filter to suppress the reference spurious tone. However, reducing the loop bandwidth causes longer settling time. On the other hand, in order to get better spurs performance, we use the fractional inputs which are unable to reduce a fraction. The measured data in this chapter are summarized in Table 2-3 and 2-4.

Table 2-3 Summary of specifications

Performance	**Post-simulation (PEX-C)**	**Measurement**
Power supply	1.8V	
Reference frequency	1MHz	
Bank condition	10	
Tuning range of VCO	2.347 ~ 2.561GHz	2.381 ~ 2.606GHz
Phase noise	-118.2dBc/Hz @1MHz	-118.4dBc/Hz @1MHz
Output power level	-9.13dBm	-10.5dBm
Spurious tones	N/A	-56.5dBc @3.125MHz
Locking time	30μs	30μs

Table 2-4 DC current consumption

Block	**Post-simulation**	**Measurement**
VCO core	4.6mW	4.5mW
Buffer	6.1mW	6.3mW
Frequency divider	10.2mW	10.8mW
Charge pump	0.9mW	1mW
Rest parts of PLL	0.3mW	0.3mW
Total	22.1mW	22.9mW

Chapter 3

2.4-GHz Wide Tuning-Range and Low-Power, Low Phase-Noise Integer-N Frequency Synthesizers

3.1 A 2.4-GHz wide tuning-range quadrature output integer-N frequency synthesizer

3.1.1 Circuit description

This chip is fabricated in July 2004. Most of the dual-band receivers now use individual receiving path, however, it requires large hardware areas and more power consumption. A fully monolithic dual band concurrent receiver chip for 802.11 a/b/g applications is designed using 0.18μm RF CMOS process [10]. Fig. 3-1 shows this dual band receiver block diagram. Only a single 2.4-GHz frequency synthesizer can complete both bands down conversion because sub-harmonic mixer is used in the 5.2-GHz receiving path. This single integer-N frequency synthesizer provides quadrature phase outputs for 2.4-GHz and octal phase outputs for 5.2-GHz in order to generate an IQ signal for the sub-harmonic mixer. So it is only required one frequency synthesizer with 2390 ~ 2670-MHz tuning range if Intermediate frequency (IF) is 10-MHz. The frequency plan of this dual-band receiver is shown in Fig. 3-2.

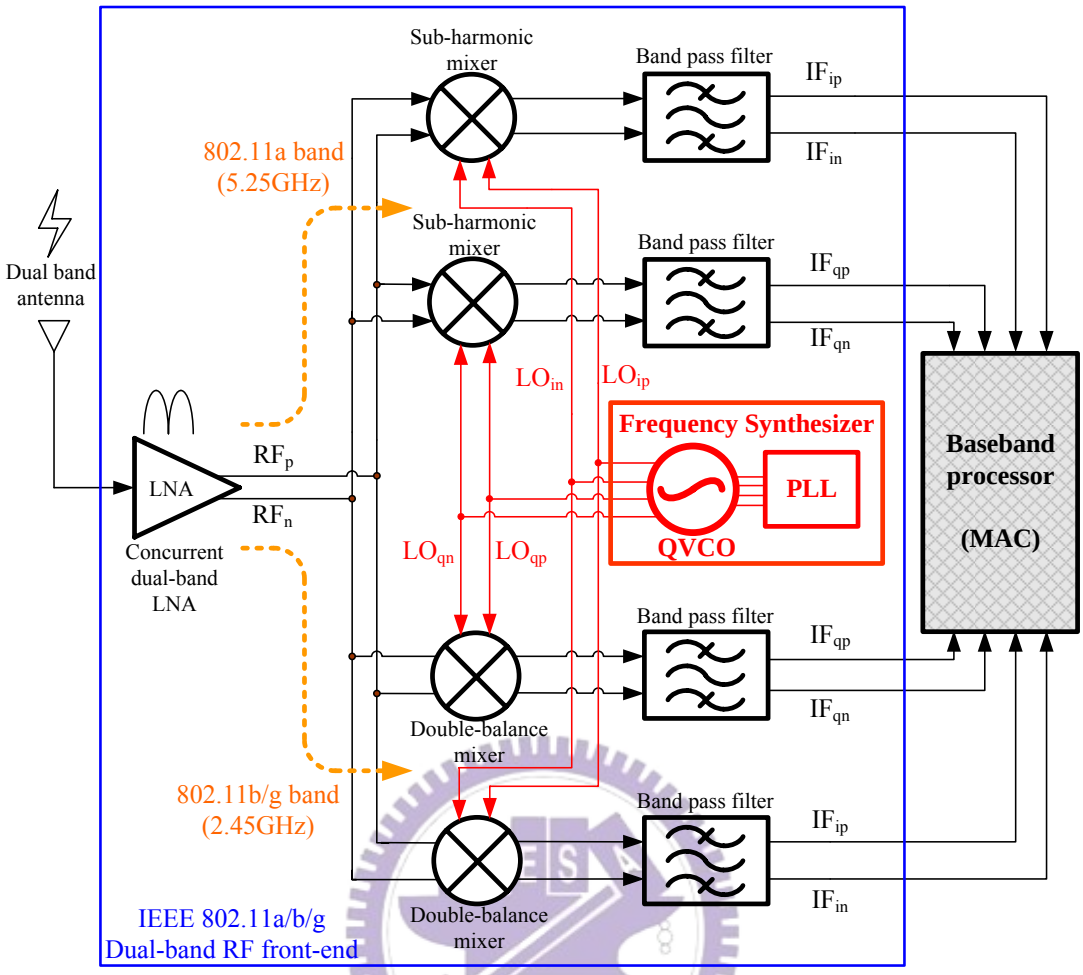
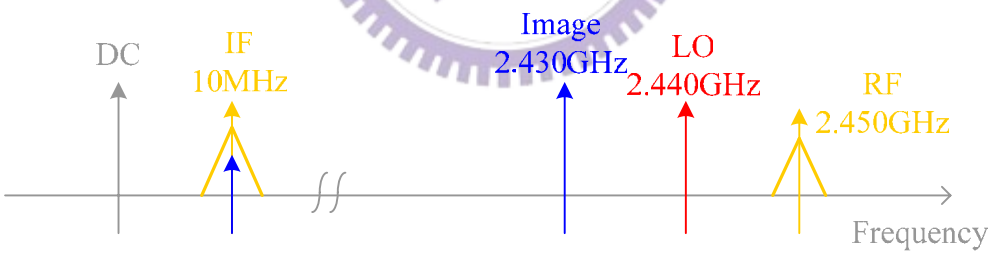
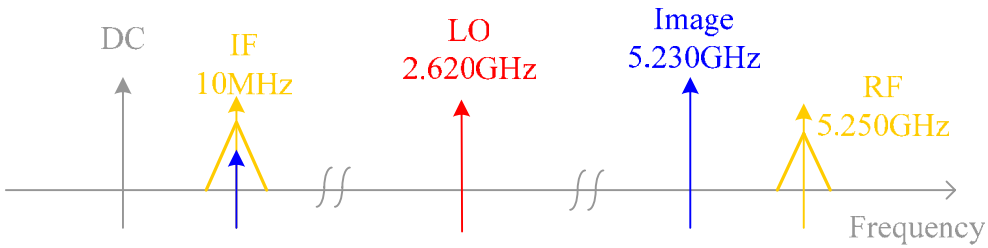


Fig. 3-1 Block diagram of concurrent dual-band receiver



(a)



(b)

Fig. 3-2 Frequency plans of dual-band receiver
(a) 2.45-GHz receiving path (b) 5.25-GHz receiving path

◆ Quadrature VCO:

Here, we adopt the LC-tank oscillator rather than ring oscillator for better phase noise consideration. For image cancellation, we hope VCO can provide quadrature phase output signal. For the most part, there are three ways to generate quadrature output signals: Divided-by-two circuit [31], RC poly-phase network [12], and two VCOs which cross connect with each other [20]. Using divided-by-two circuit needs to design a VCO which operate at the double frequency of original frequency. VCO operating at higher frequency will consume more power and have poor phase noise. Besides, this structure also shows poor quadrature accuracy because of the requirement of 50% duty cycle VCO. A VCO with RC-poly-phase network consumes less power than others, but RC network is signal power hungry. Based on the above consideration, the circuit structure based on the LC-tank oscillator is used to implement this integrated quadrature VCO, as showing in Fig. 3-3.

The 3-bit capacitor bank circuits are used in this design, i.e. there's three control bits and enables us to set the oscillator under 8 operating conditions: 000, 001, 010, 011, 100, 101, 110, and 111. Different control bit is connected to different amount of parallel capacitors; higher bit is connected to a larger capacitance. In Fig. 3-3, the capacitor bank architecture adopts a capacitor series a transistor as a switch. When a control bit of capacitor bank is at low level, the switch is open and the capacitor doesn't connect to ground, so the capacitance of LC-tank doesn't change. Otherwise, when a control bit is at high level, the switch is closed and the capacitor connects to ground, so the capacitance of LC-tank is increased.

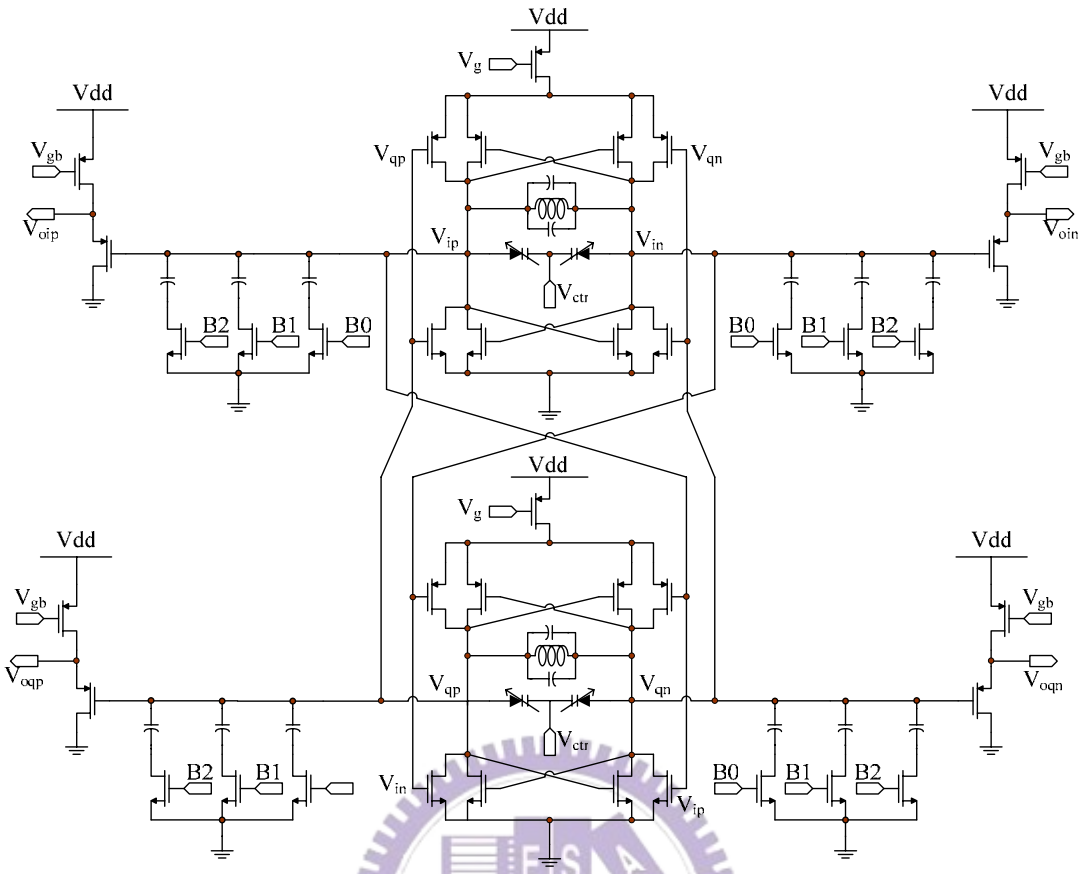
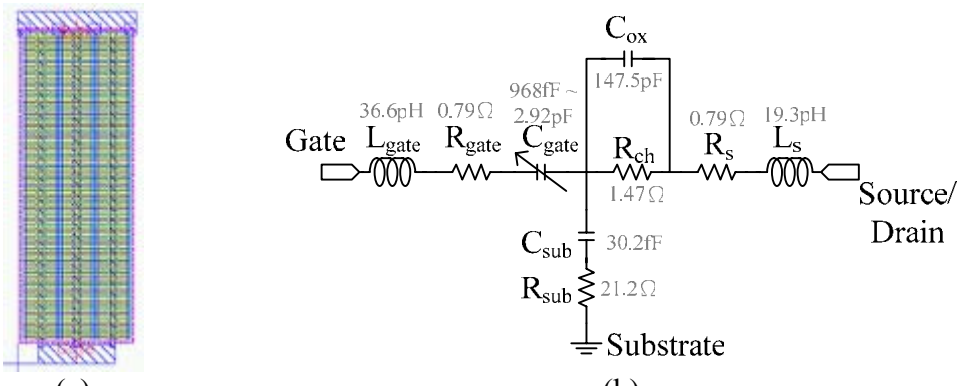


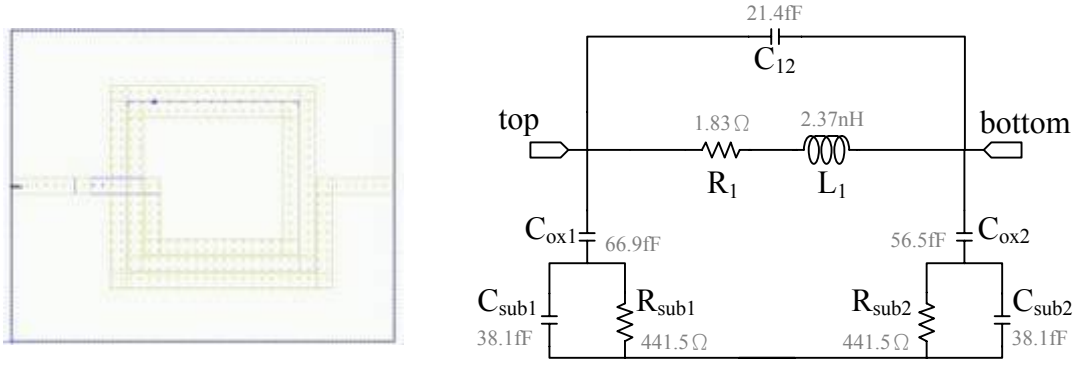
Fig. 3-3 Schematic of QVCO

In order to implement frequency synthesizer for dual-band receiver, more than 300MHz tuning range is required. Use the MOS varactor (Blanch=50 and Group=3, shown in Fig. 3-4). Also, we adopt the minimum turns (2.5) of inductor in the standard model which has better quality factor than others. The inductance of this inductor is about 2.37nH (Fig. 3-5). So the oscillation frequency of this VCO can oscillate at 2.4-GHz.



(a) (b)

Fig. 3-4 MOS varactor in this synthesizer (a)layout (b)equivalent circuit model



(a) (b)

Fig. 3-5 Spiral inductor in this synthesizer (a)layout (b)equivalent circuit model

Fig. 3-6 shows the tuning curve of VCO for bank 000, 011, and 111. At bank 011, it shows that the oscillator is tunable between 2.08-GHz and 2.57-GHz (490MHz tuning range) at bank 011 condition. The corner case of tuning curve for bank011 is shown in Fig. 3-7. The output swing of VCO is shown in Fig. 3-8.

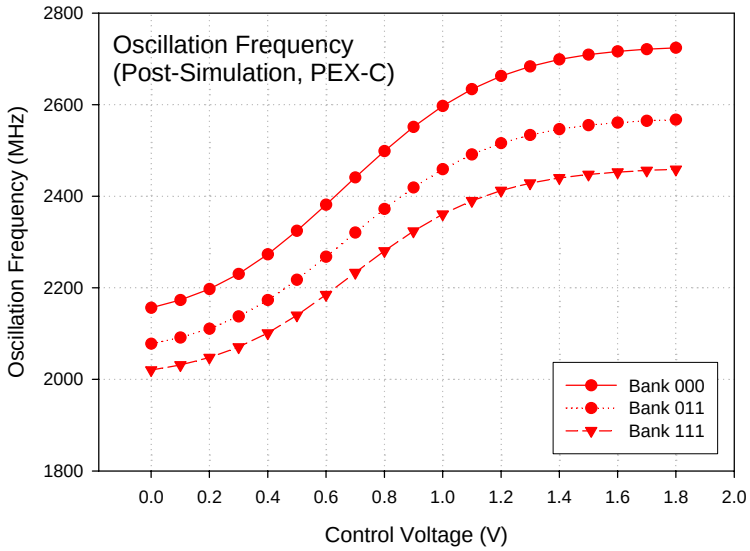


Fig. 3-6 Tuning curve of QVCO (Capacitor Bank)

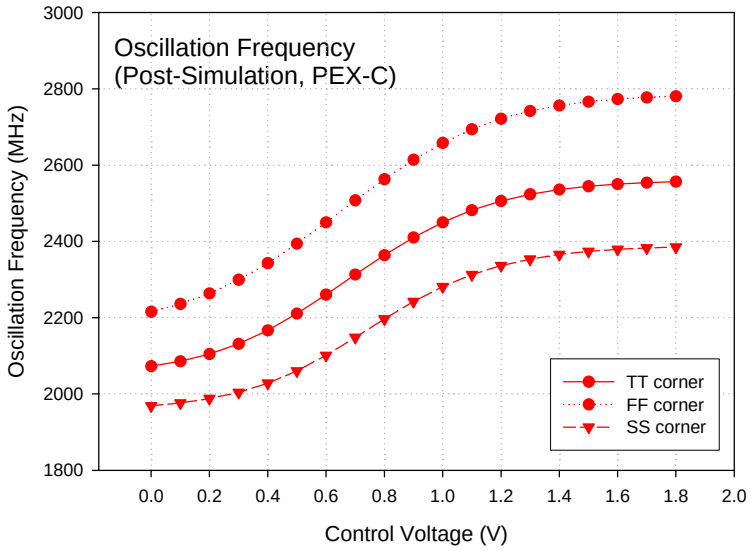


Fig. 3-7 Tuning curve of QVCO (Corner Case)

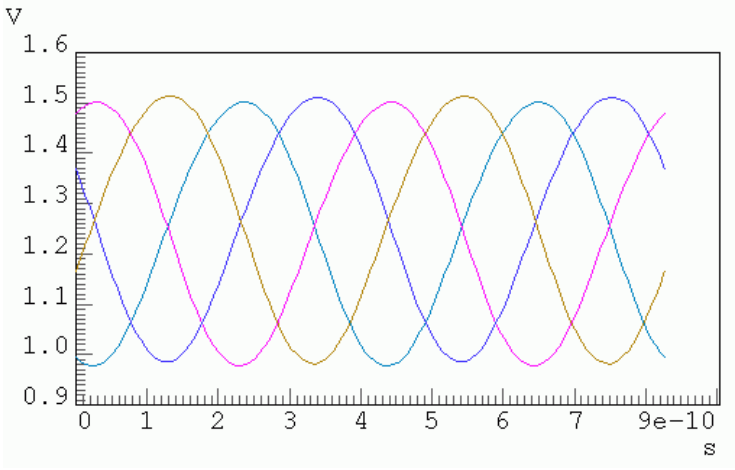


Fig. 3-8 Output Swing of QVCO

The most critical part in the design of a low-phase noise VCO is the inductor of the resonance LC-tank. Based on post-simulation result (PEX-C), the phase noise of this VCO is -111.3dBc/Hz @ 1-MHz offset, and -124.3dBc/Hz @ 3-MHz offset at 2.45-GHz, as showing in Fig. 3-9. The corner case of phase noise is shown in Fig. 3-10. The power consumption of two quadrature VCO core circuits is 10.6mW. The overall power consumption is 23.8mW with buffer output stages.

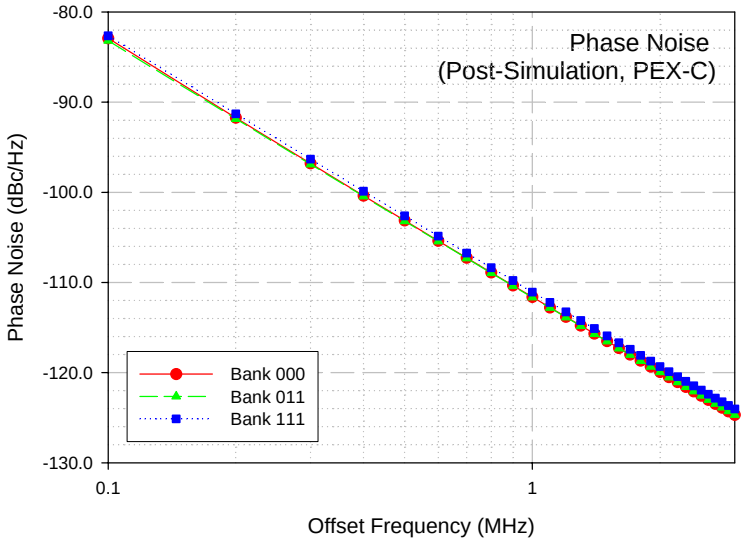


Fig. 3-9 Phase noise of QVCO (Capacitor bank)

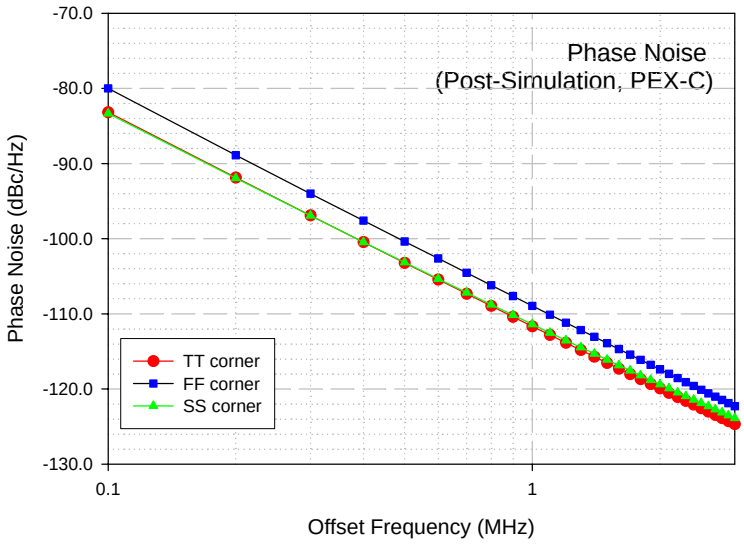


Fig. 3-10 Phase noise of QVCO (Corner case)

◆ Fully programmable multi-modulus frequency divider:

The fully programmable multi-modulus frequency divider is used in this synthesizer. The same as the former chapter, we also adopt this architecture to implement frequency divider. Use two stages of analog divided-by 2/3 and nine stages of digital divided-by 2/3 for saving power consumption. In such design, divider can be programmed to all integers dividing ratio between 2048 and 4095, depending on the input bits b_0 to b_{10}:

$$N = 2^{11} + \sum_{n=0}^{10} b_n \cdot 2^n = 2048 + \sum_{n=0}^{10} b_n \cdot 2^n \tag{3.1}$$

The co-simulation result of fully programmable frequency multi-modulus divider and VCO is as shown in Fig. 3-11. The VCO output frequency is set at 2400-MHz and the divider modulus is set at 2400, too. We can obviously observe the period of output divided signal is 1μs, this figures out our divider is working regularly.

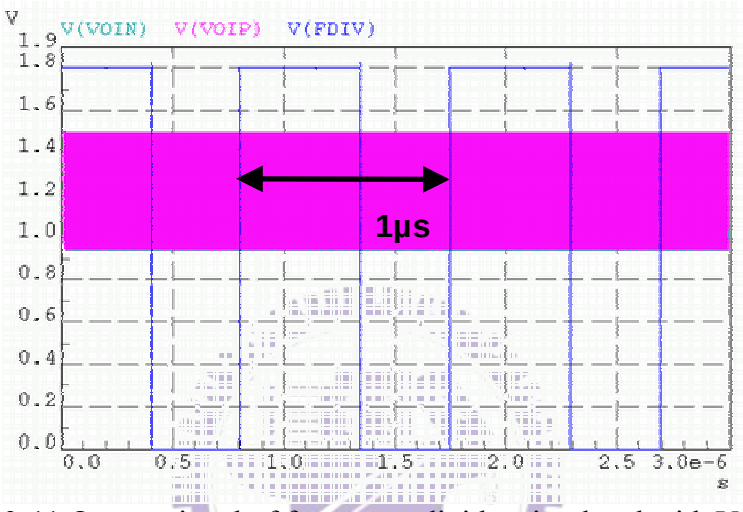


Fig. 3-11 Output signal of frequency divider simulated with VCO

◆ PFD, charge pump, and loop filter:

Also, we adopt the architecture of PFD and charge pump the same as ones in former chapter. 3rd order passive loop filter is used for our design. The optimized values are shown in Table 3-1.

Table 3-1 Optimized loop filter elements

Component	Value
C1	68pF
C2	1000pF
R2	13kΩ
C3	68pF
R3	6.2kΩ

3.1.2 Whole Circuit Simulation and layout

All of the building blocks mentioned in previous sections will be combined to be a whole frequency synthesizer and simulated together. Frequency synthesizer circuit contains many sub-circuits; whole circuit simulation takes a lot of time. So at first, we use MATLAB software to perform behavioral simulation of frequency synthesizer's settling time. It can help us to save much time in close loop simulation. And then we choose Eldo RF as our simulation tool to verify whether the connections of whole loop are correct or not.

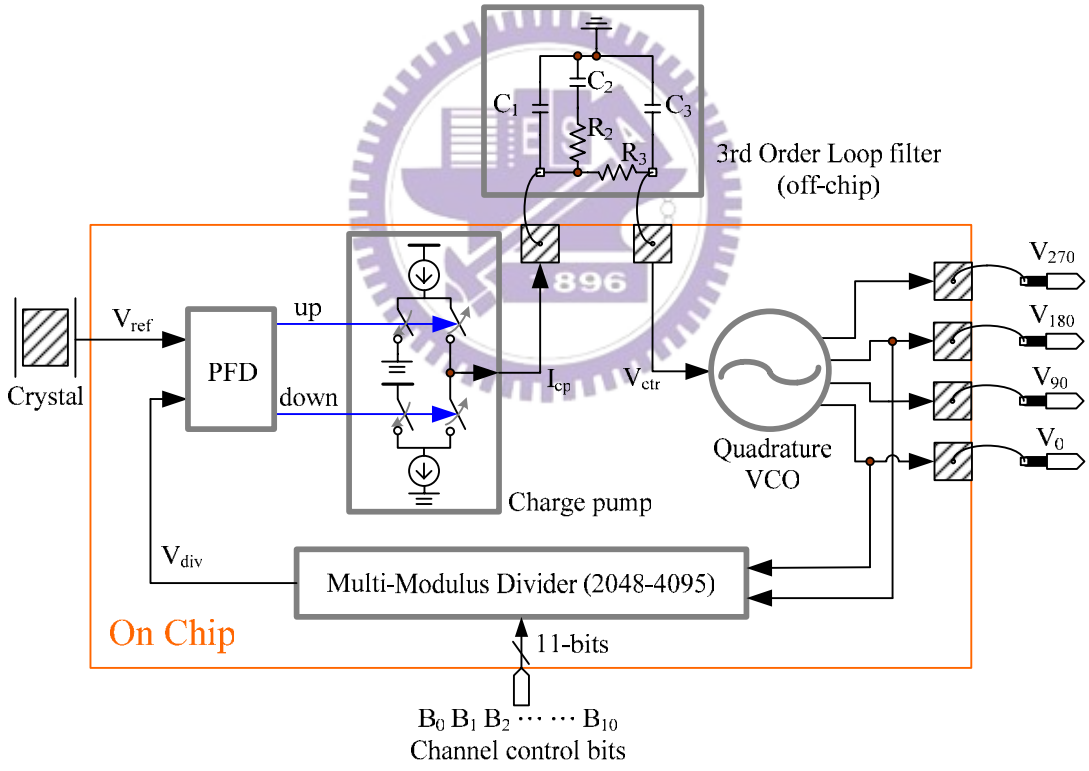


Fig. 3-12 Building blocks of wide tuning range integer-N frequency synthesizer

Based on behavior level simulation result, the settling time is about 60μs, as shown in Fig. 3-13. After transistor level simulation with Eldo RF, the settling time is less than 60μs, as shown in Fig. 3-14. It shows the settling time less than 200μs as the specification of Bluetooth system and WLAN applications required.

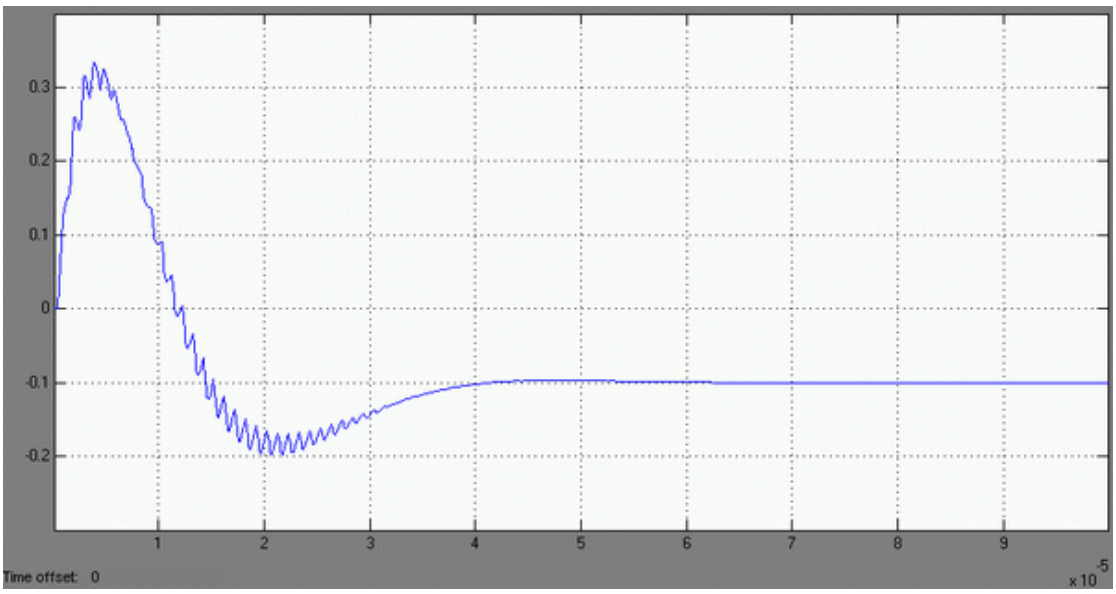


Fig. 3-13 Locking transient simulation (Behavior level)

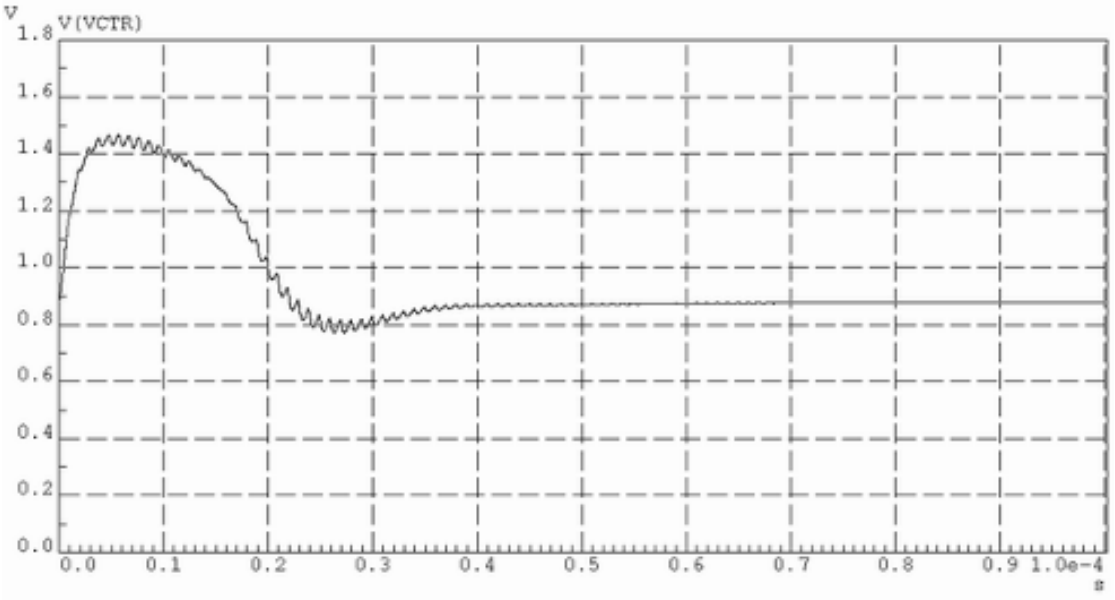


Fig. 3-14 Locking transient simulation (Transistor level)

Fig. 3-15 shows the layout of whole chip and Fig. 3-16 shows the die-photograph of whole chip. The die size is roughly 1500μm×1100μm.

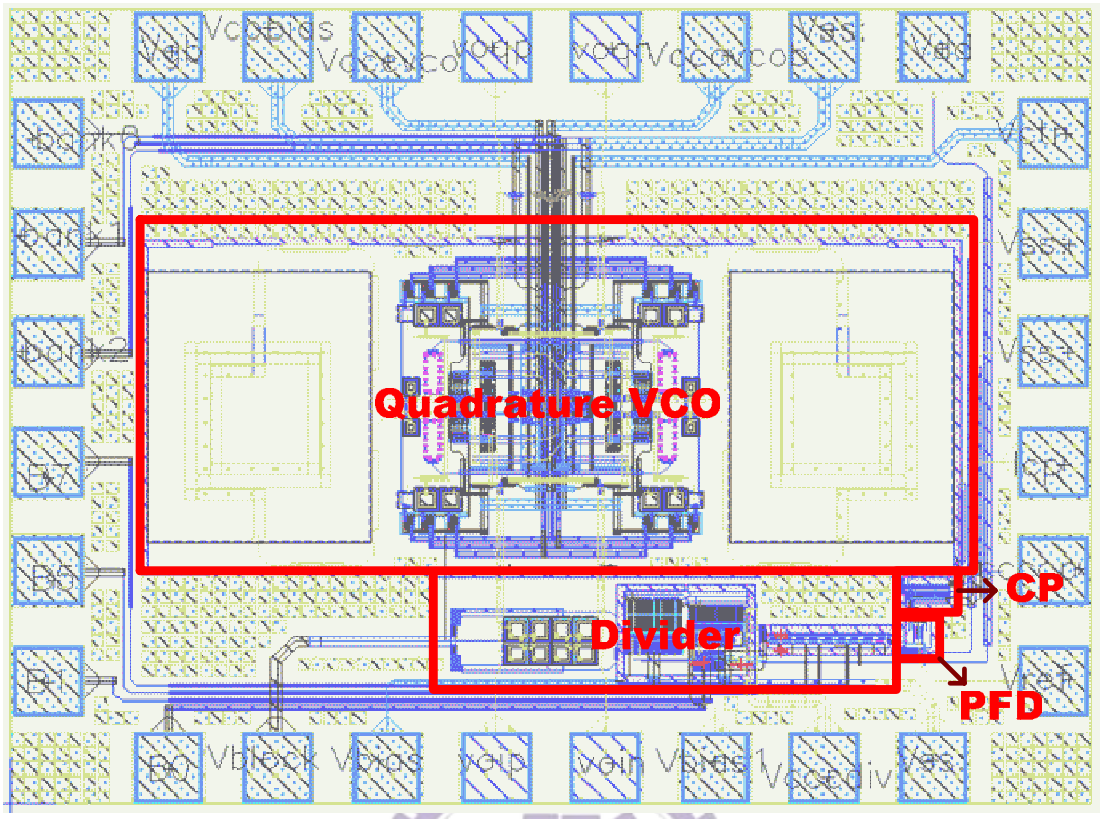


Fig. 3-15 Layout of wide tuning range integer-N frequency synthesizer

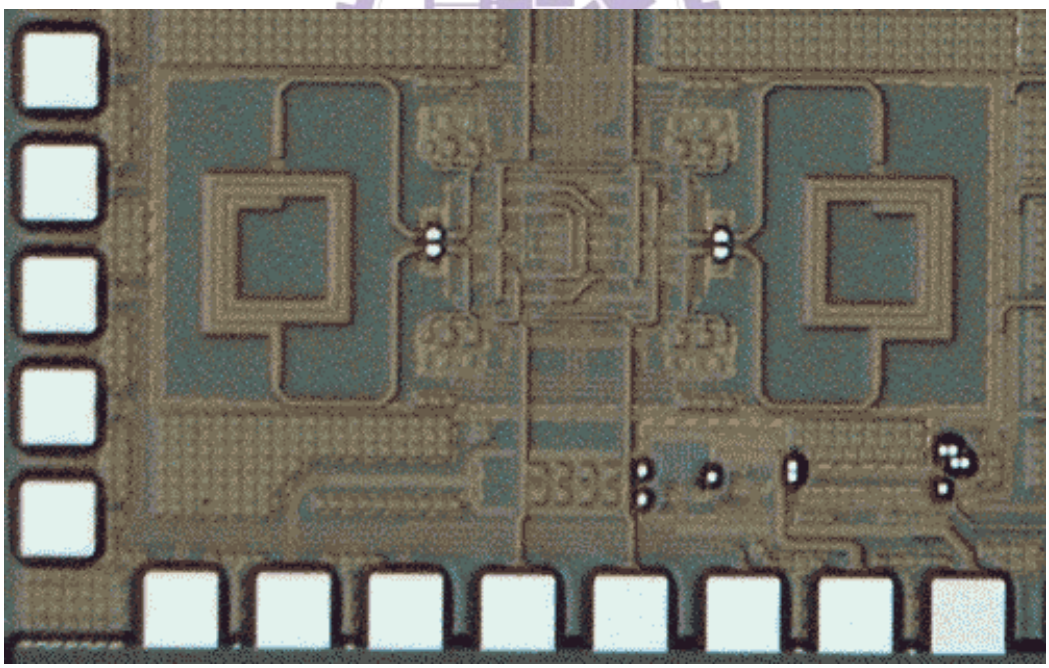


Fig. 3-16 Die-photograph of wide tuning range integer-N frequency synthesizer

Table 3-2 Performance summary of wide tuning range integer-N synthesizer

Post-simulation (PEX-C)	**TT corner**	**FF corner**	**SS corner**
Power supply	1.8 V		
Crystal frequency	1MHz		
VCO center frequency	2.42GHz	2.51GHz	2.38GHz
VCO bank condition	(B2 B1 B0)=(011)	(B2 B1 B0)=(000)	(B2 B1 B0)=(111)
VCO tuning range	2.08 ~ 2.57GHz 490MHz	2.15 ~ 2.65GHz 500MHz	2.05 ~ 2.54GHz 490MHz
Phase noise (dBc/Hz)	-111.3 @1MHz -124.3 @3MHz	-109.1 @1MHz -122.1 @3MHz	-112.5 @1MHz -125.5 @3MHz
VCO output swing	530mV($V_{peak\ to\ peak}$)	590mV($V_{peak\ to\ peak}$)	450mV($V_{peak\ to\ peak}$)
Settling time	60μs	-	-
VCO power consumption	Two core circuits: 10.6mW Four buffer stages: 13.2mW	Two core circuits: 13.0mW Four buffer stages: 16.0mW	Two core circuits: 8.5mW Four buffer stages: 11.2mW
Prescaler power consumption	12.6mW	16.0mW	8.6mW
Total power consumption	37.7mW	46.3mW	29.1mW

3.1.3 Measurement Results

This work is bond-wire measurement on PCB. The measuring equipment contains 8563E spectrum analyzer, 54610B oscilloscope, E3611A power supply and HP 33120A function generator.

Fig. 3-17 shows the testing PCB. The chip is stuck on testing PCB, and wires are bonded from the pad on chip to feed bias voltages. An off-chip 1-MHz crystal oscillator instead of function generator is used to produce reference clock for suppressing the noise coming from reference signal. The loop filter is also designed off-chip for easily modifying element values and decrease chip area although it introduces more noise than designed fully on-chip.

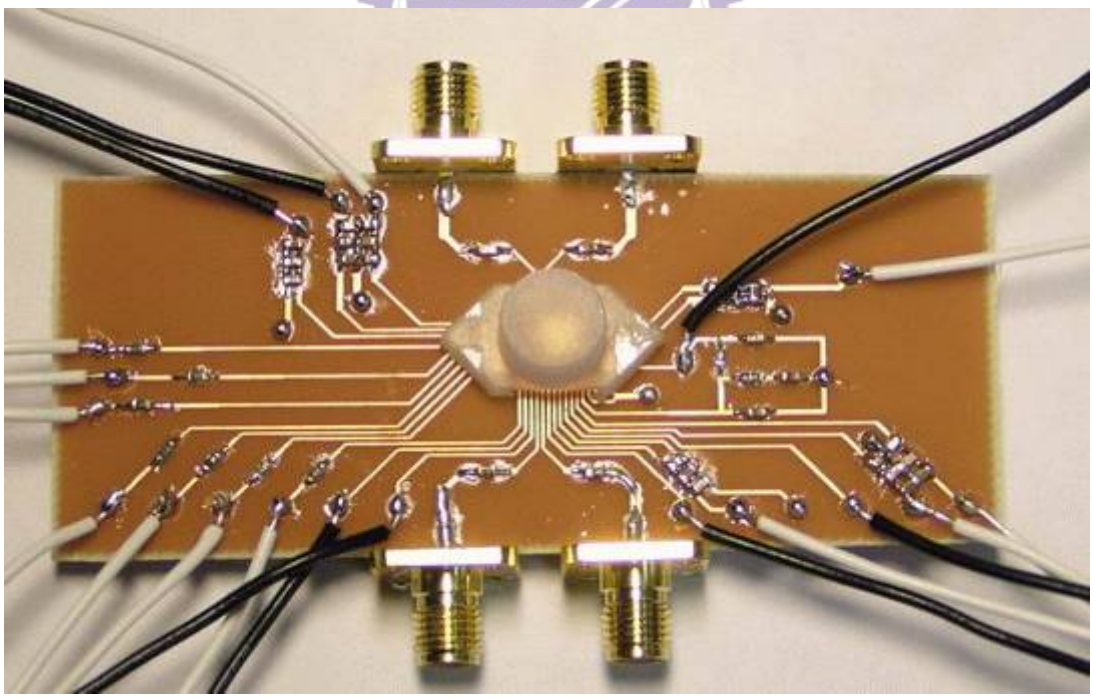


Fig. 3-17 Testing board of wide tuning range integer-N synthesizer

3.1.3.1 VCO Measurement Results

The measured tuning curve and spectrum of VCO in this work is shown as following figures. We can obviously observe that all the bank conditions (from 000 to 111) are all contains the frequency area we need, i.e. whether the oscillator is set in which bank condition, the frequency synthesizer may lock successfully. We use the signal source analyzer to measure QVCO characteristic at bank 011, as showing in Fig. 3-18.

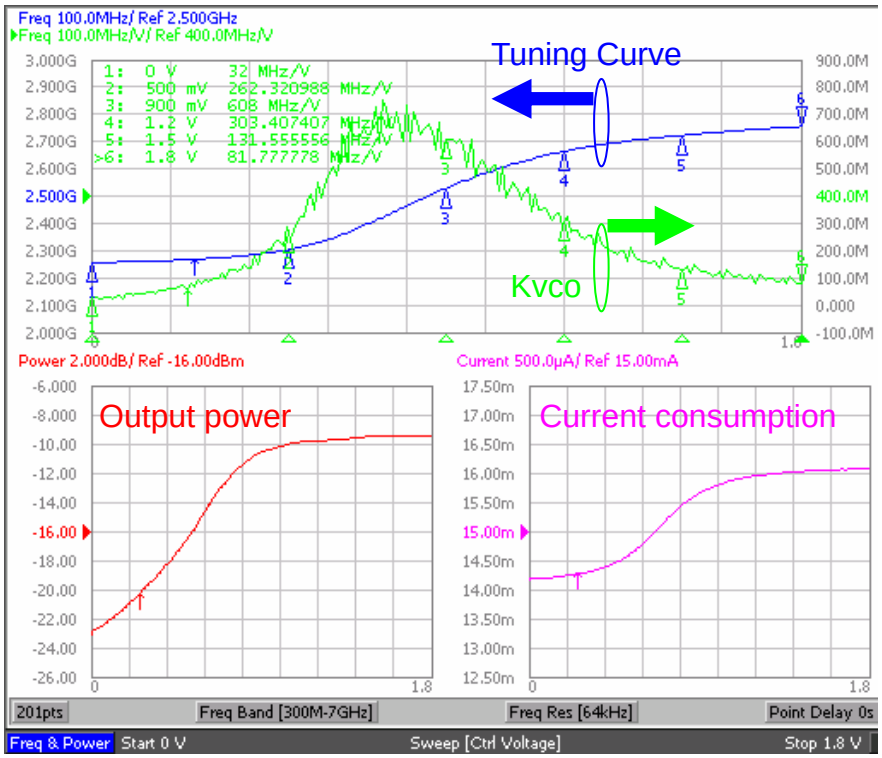


Fig. 3-18 Measured characteristic of QVCO in this synthesizer

The tuning curve at bank 000, 011, and 111 is shown in Fig. 3-19a. The measured tuning range is 2.178 ~ 2.629-GHz (at bank condition 011), comparing with our simulation results, the tuning range is 2.078~2.567-GHz at TT corner, it's approximately equal to simulation result. But there's still a little difference when control voltage is approximately 0V and 1.8V. While control voltage is about 0.9V,

tuning curve is almost linear, the same as simulation result. That means the extra parasitic effects are perfectly evaluated during our simulation. Fig. 3-20 shows the output spectrum while control voltage is 0.9V at bank 011.

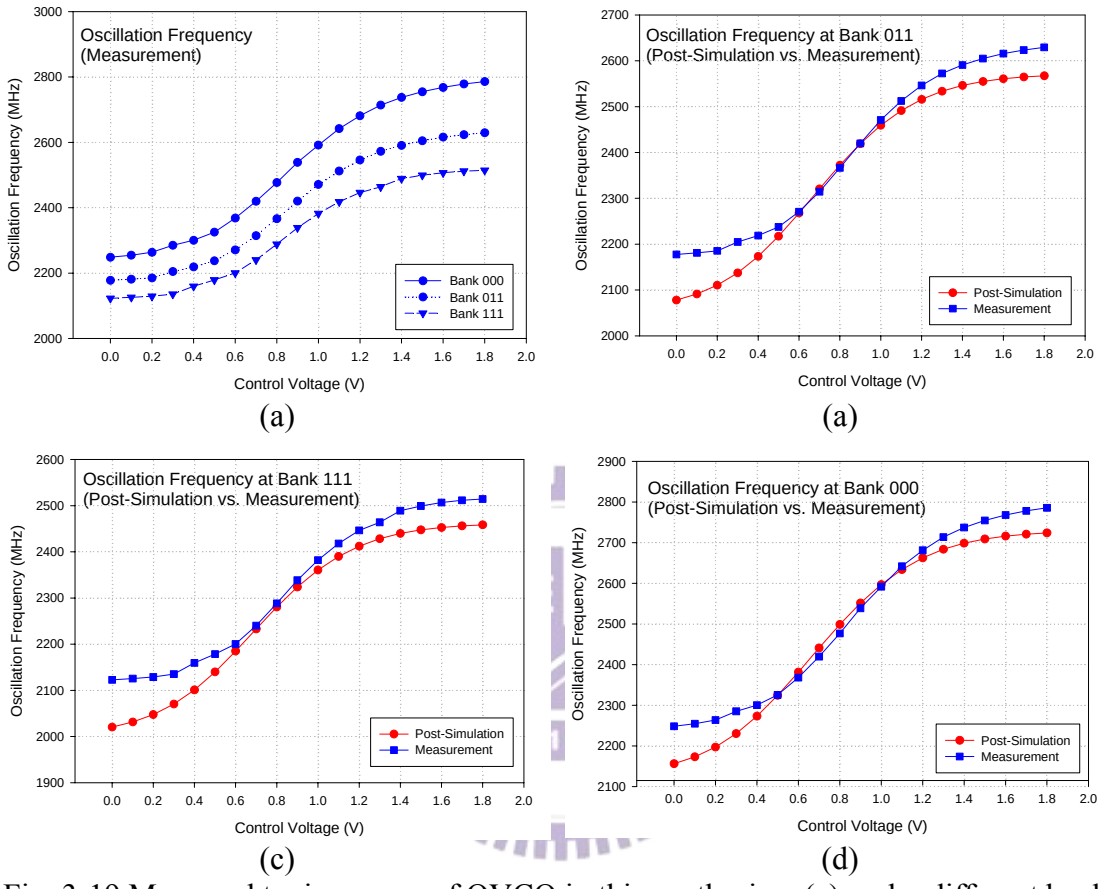


Fig. 3-19 Measured tuning curve of QVCO in this synthesizer (a) under different bank conditions (b) at bank 011 (c) at bank 111 (d) at bank 000

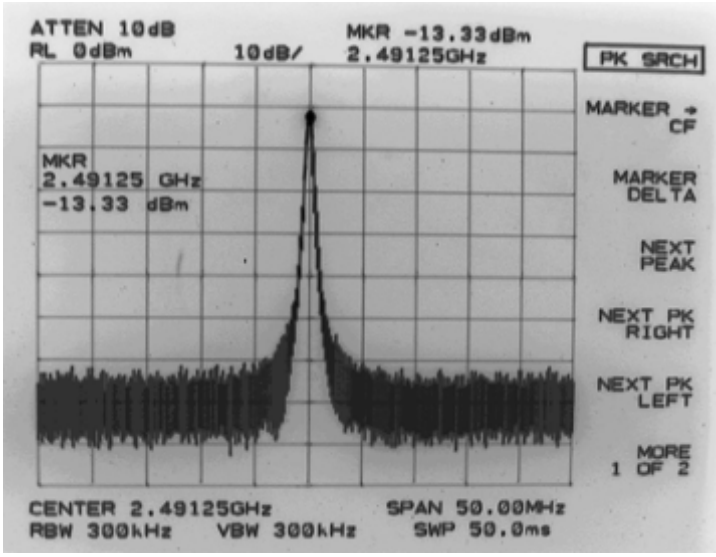


Fig. 3-20 Measured output spectrum of QVCO in this synthesizer

The tuning range is just as the original design. Next we measure phase noise performance of QVCO in this circuit at CIC with Agilent E5052A signal source analyzer. However, noise performance is worse than simulation result. Phase noise is low offset frequency is more terrible, as shown in Fig. 3-21. It is supposed to be the effect of large tuning range (about 700MHz/volt). The output frequency has larger variation while VCO is at free-running state. The small variation on control voltage results in output frequency uncertainty.

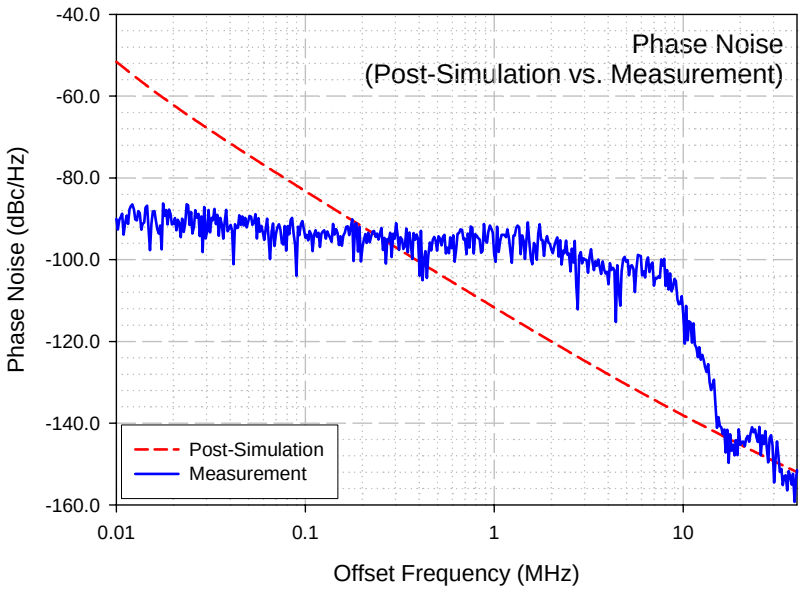


Fig. 3-21 Phase noise of QVCO in this synthesizer (Bank 011, at CIC)

We adopt another measurement at lab with analog power supply which has less noise voltage. We use the average mode of spectrum analyzer to measure the phase noise performance. Noise performance is only worse than simulation result about 2.5dB (Fig. 3-22). Phase noise @ 1-MHz offset form the carrier is -108.83dBc/Hz, as shown in Fig. 3-23. This result is much better than measurement at CIC. The noise on power source causes the poor phase noise performance. More noise on supply voltage and larger Kvco result in the wrong measured phase noise performance.

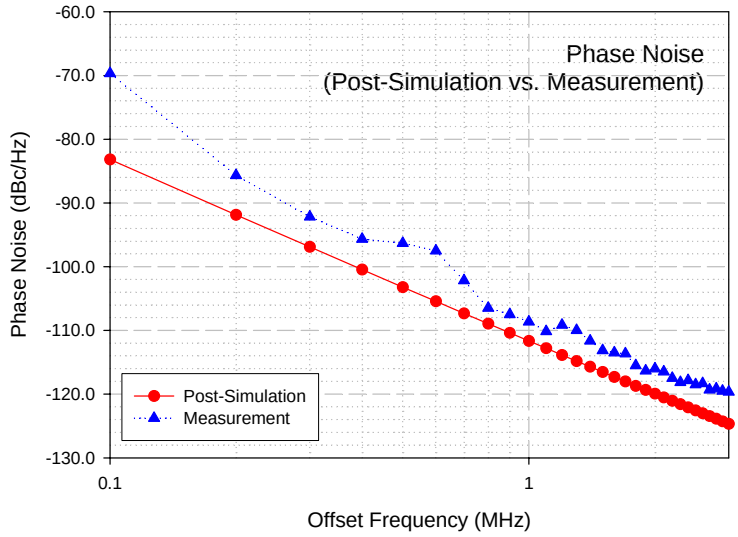
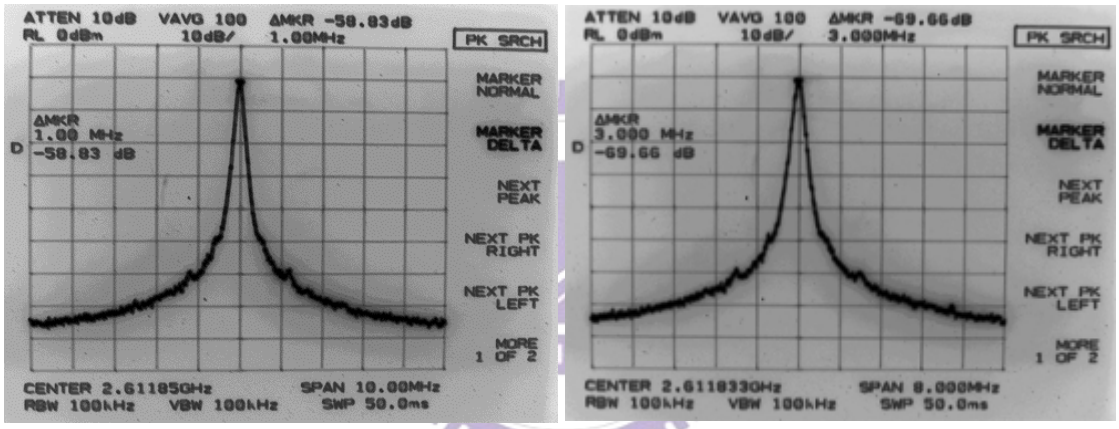


Fig. 3-22 Phase noise of QVCO in this synthesizer (Bank 011, at LAB)



$-58.83dB - 10\log(100\times10^3)$ $-69.66dB - 10\log(100\cdot10^3)$

$= -108.83dBc/Hz$ $= -119.66dBc/Hz$

@1MHz offset @3MHz offset

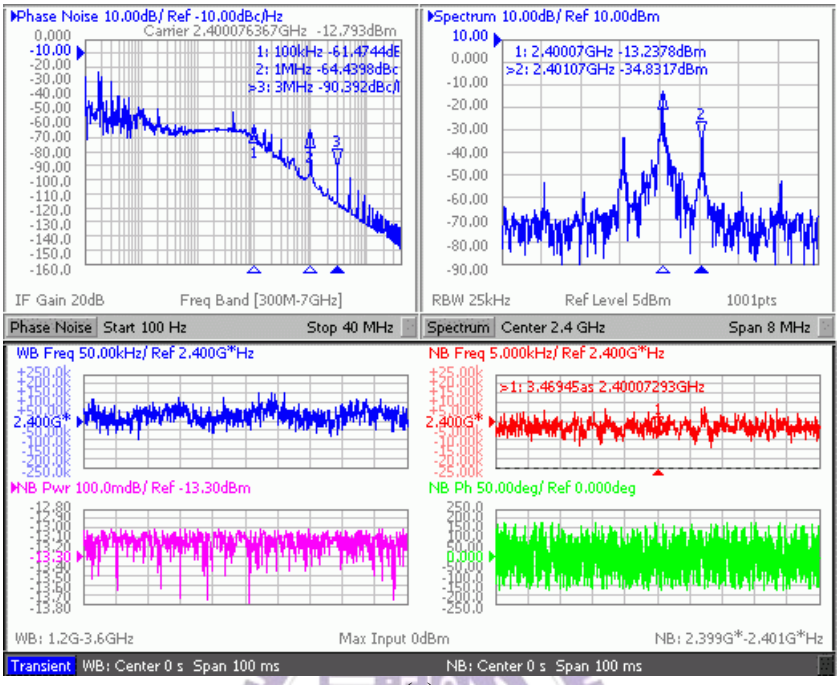
(a) (b)

Fig. 3-23 Measured phase noise of QVCO in this synthesizer (Bank 011, at LAB)
(a) at 1-MHz offset (b) at 3-MHz offset

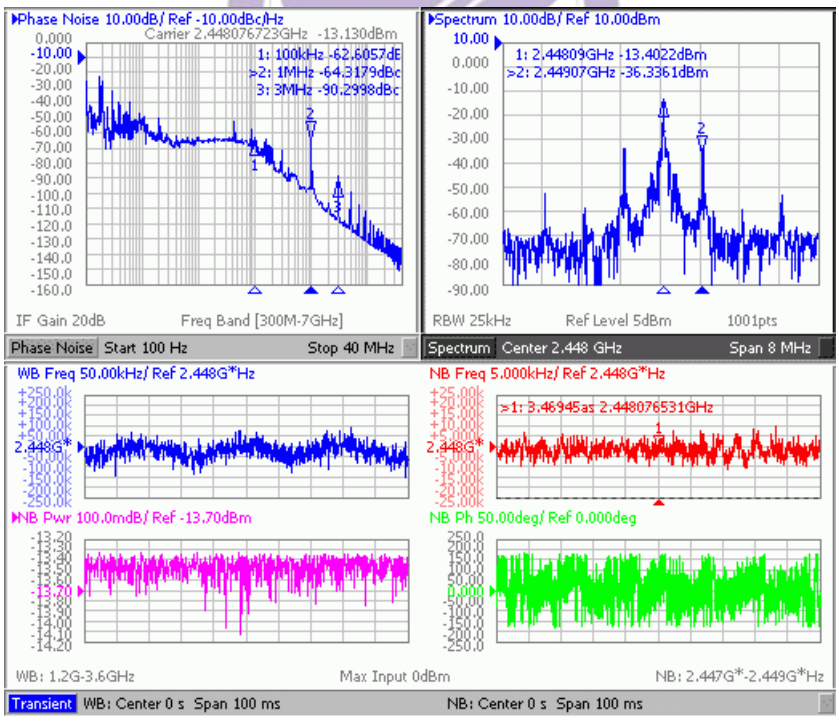
3.1.3.2 Whole Circuit Measurement Results

We measure this circuit at CIC, using Agilent E5052A signal source analyzer. The whole synthesizer's measurement data at CIC are shown in following figures. Fig. 3-24a and Fig. 3-24b are total measurement results using this instrument. Fig. 3-25 is the output spectrum while frequency synthesizer locked at 2400-MHz and 2448-MHz. These figures show the spurious tone vs. carrier of this frequency synthesizer is about

-23dBc @1-MHz. Fig. 3-26 is the phase noise performance while frequency synthesizer locked at 2400-MHz, 2448-MHz and 2480-MHz.

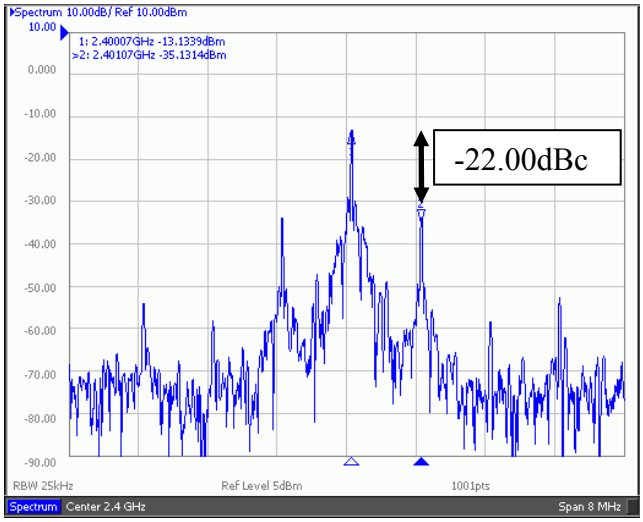


(a)

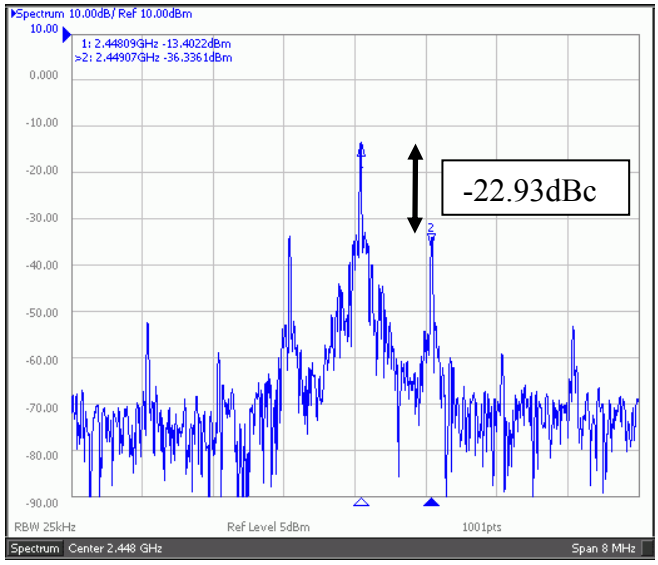


(b)

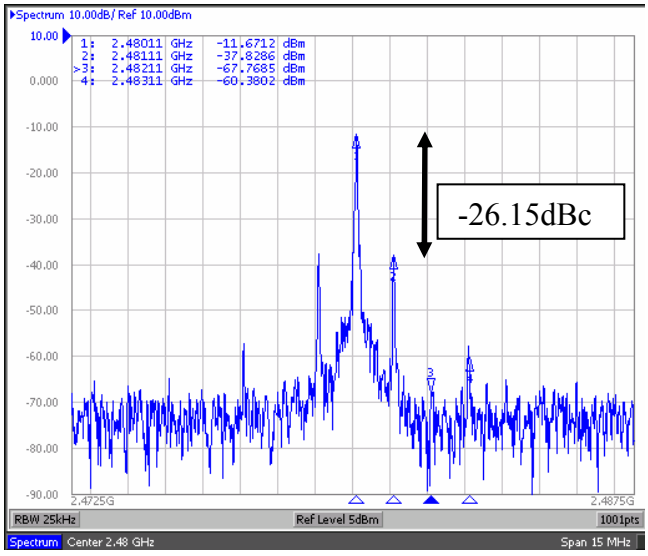
Fig. 3-24 Data measured from signal source analyzer
(a) at 2400-MHz (b) at 2448-MHz



(a)

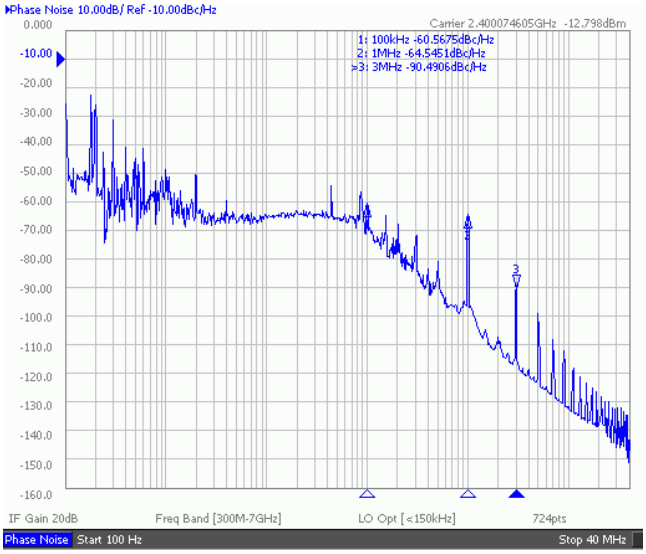


(b)

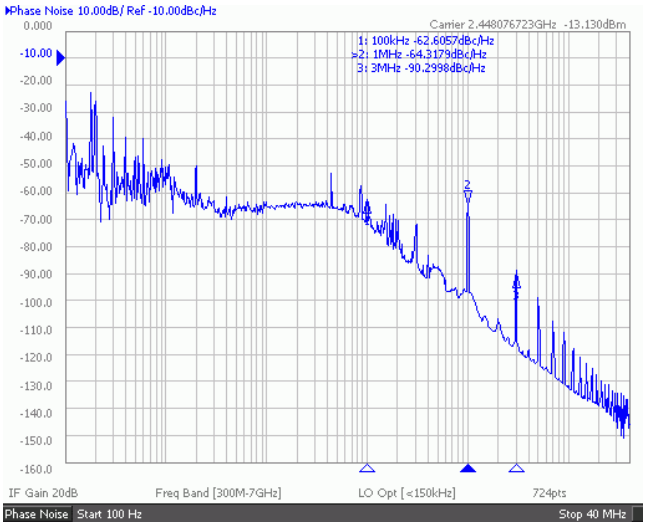


(c)

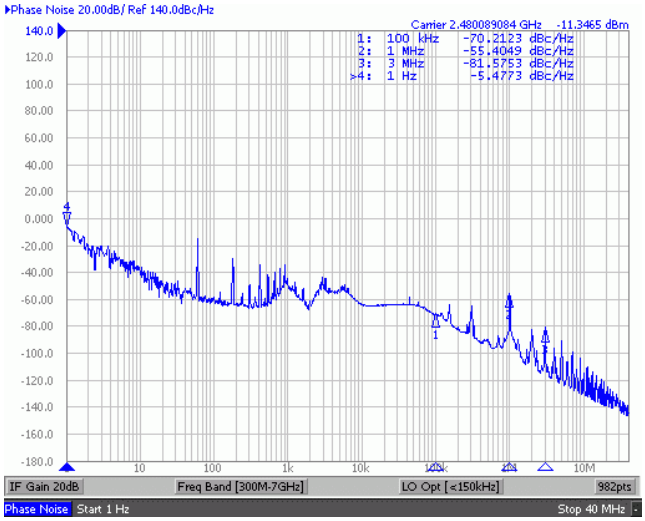
Fig. 3-25 Measured locking spectrum at (a)2400MHz (b)2448MHz (c)2480MHz



(a)



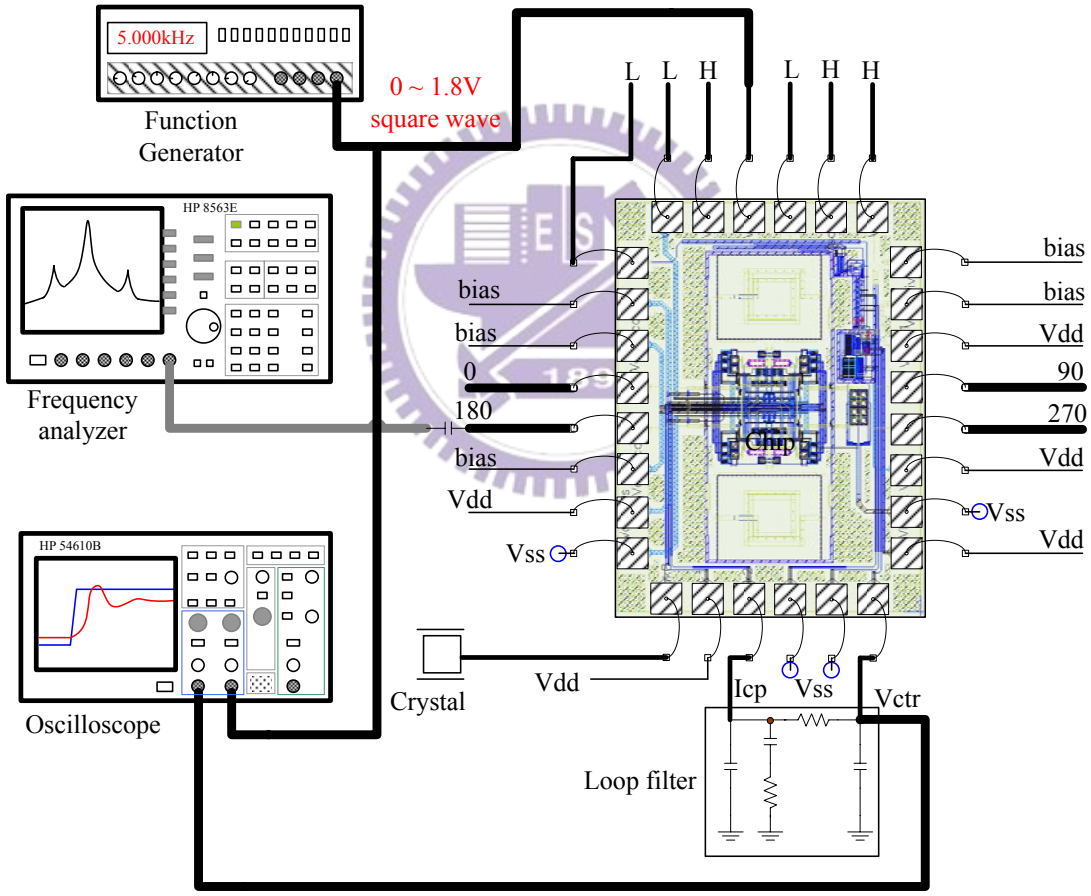
(b)



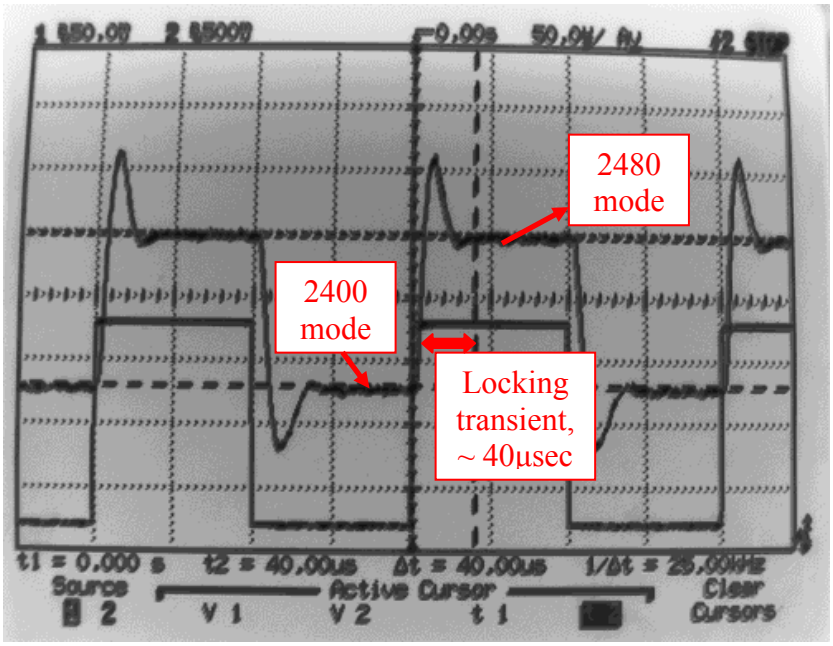
(c)

Fig. 3-26 Measured phase noise while locking at (a) 2400MHz (b) 2448MHz (c) 2480MHz

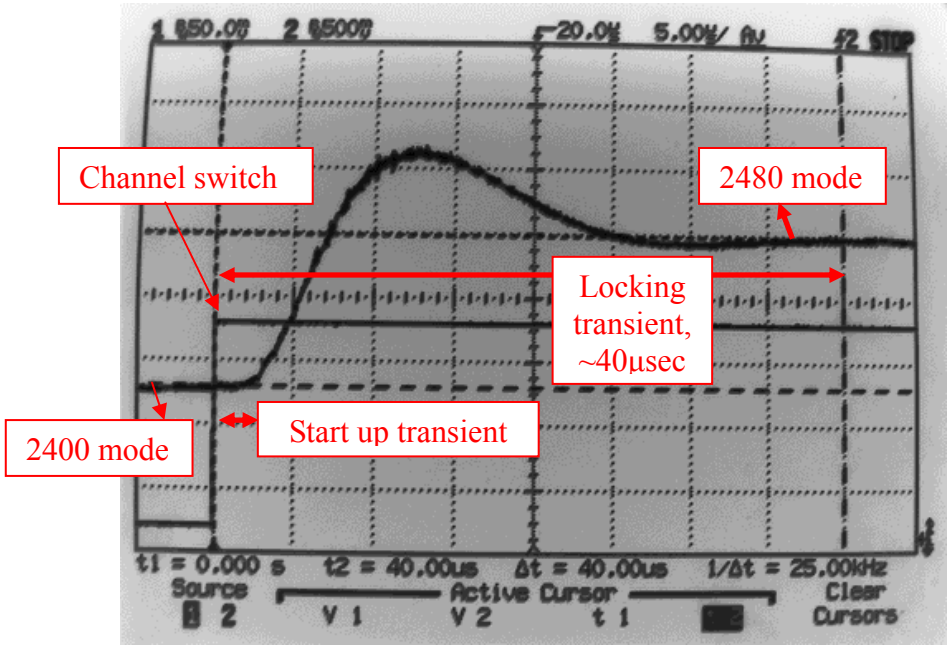
Next we use the function generator as a trigger source. The measurement consideration of settling time is showing in Fig. 3-27a. The function generator outputs low frequency signal to feed the control bit of multi-modulus prescaler. It results that the output frequency is changed between 2400-MHz and 2480-MHz. So we can measure the settling time using a normal oscilloscope. Fig. 3-27b and Fig. 3-27c are the VCO input control voltage node waveforms. They represent the locking transient waveforms of this frequency synthesizer. The locking settling time shows it is less than 40μs.



(a)



(b)



(c)

Fig. 3-27 (a) Measurement consideration of settling time
(b) Transient of settling time
(c) Zoom in of the transient of settling time

3.1.4 Measurement Discussions

The simulation and measurement results of power consumption are very close, and all parts work successfully. Based on measurement results, the tuning range and phase noise is close to simulation results. But the spur performance is not acceptable.

We can reduce the loop bandwidth of loop filter to suppress the reference spurious tone. However, reducing the loop bandwidth causes longer settling time. The measured data in this chapter are summarized in Table 3-3 and 3-4.

Table 3-3 Summary of specifications

Performance	**Post-simulation (PEX-C)**	**Measurement**
Power supply	1.8V	
Reference frequency	1MHz	
Bank condition	(B2 B1 B0)=011	
Tuning range of VCO	2.078 ~ 2.567GHz	2.178 ~ 2.629GHz
Phase noise	-111.3dBc/Hz @1MHz -124.3dBc/Hz @3MHz	-108.8dBc/Hz @1MHz -119.7dBc/Hz @3MHz
Output power level	-11.48dBm @Vctr=0.9V	-13.33dBm @Vctr=0.9V
Spur tone vs. carrier	N.A.	-26.15dBc @1MHz
Locking time	60μs	40μs

Table 3-4 DC current consumption

Block	**Post-simulation**	**Measurement**
Two VCO cores	10.6mW	10.8mW
Four buffer stages	13.2mW	12.8mW
Frequency divider	12.6mW	13.5mW
Charge pump	1.1mW	1.1mW
Rest parts of PLL	0.2mW	0.2mW
Total	37.7mW	38.4mW

3.2 A 2.4-GHz low power, low phase-noise, quadrature output integer-N frequency synthesizer

3.2.1 Circuit description

This chip is fabricated in September 2004. In the former section, a wide tuning range VCO is implemented. The wider tuning range results the worse noise performance because large tuning range enhances the sensitivity of VCO the substrate noise while we design the frequency range of VCO. Besides, it is more sensitive to the power supply. The frequency pushing from power source may happen. Small Kvco is advantage for phase-locked loop system because the residual frequency variation is small while system is locking. Here, we design a small frequency range of frequency synthesizer. This circuit is in comparison with the circuit in former section later.

- Quadrature VCO:

We adopt the LC-tank quadrature output oscillator rather than ring oscillator in order for better phase noise consideration and image cancellation. The whole schematic of the quadrature VCO is shown in Fig. 3-28. The 2-bit capacitor bank circuits are used in this design, i.e. there's three control bits and enables us to set the oscillator under 4 operating conditions: 00, 01, 10, and 11. Different control bit is connected to different amount of parallel capacitors; higher bit is connected to a larger capacitance. When a control bit of capacitor bank is at high level, the capacitor is enabled and the capacitance of LC-tank is increased.

In Fig. 3-28, the capacitor bank architecture adopts a MOS as a varactor. When a

control bit of capacitor bank is at low level, the MOS varactor has small capacitance. Otherwise, when a control bit is at high level, the MOS varactor has large capacitance. It can prevent not start-up oscillation while some damage of switch happened.

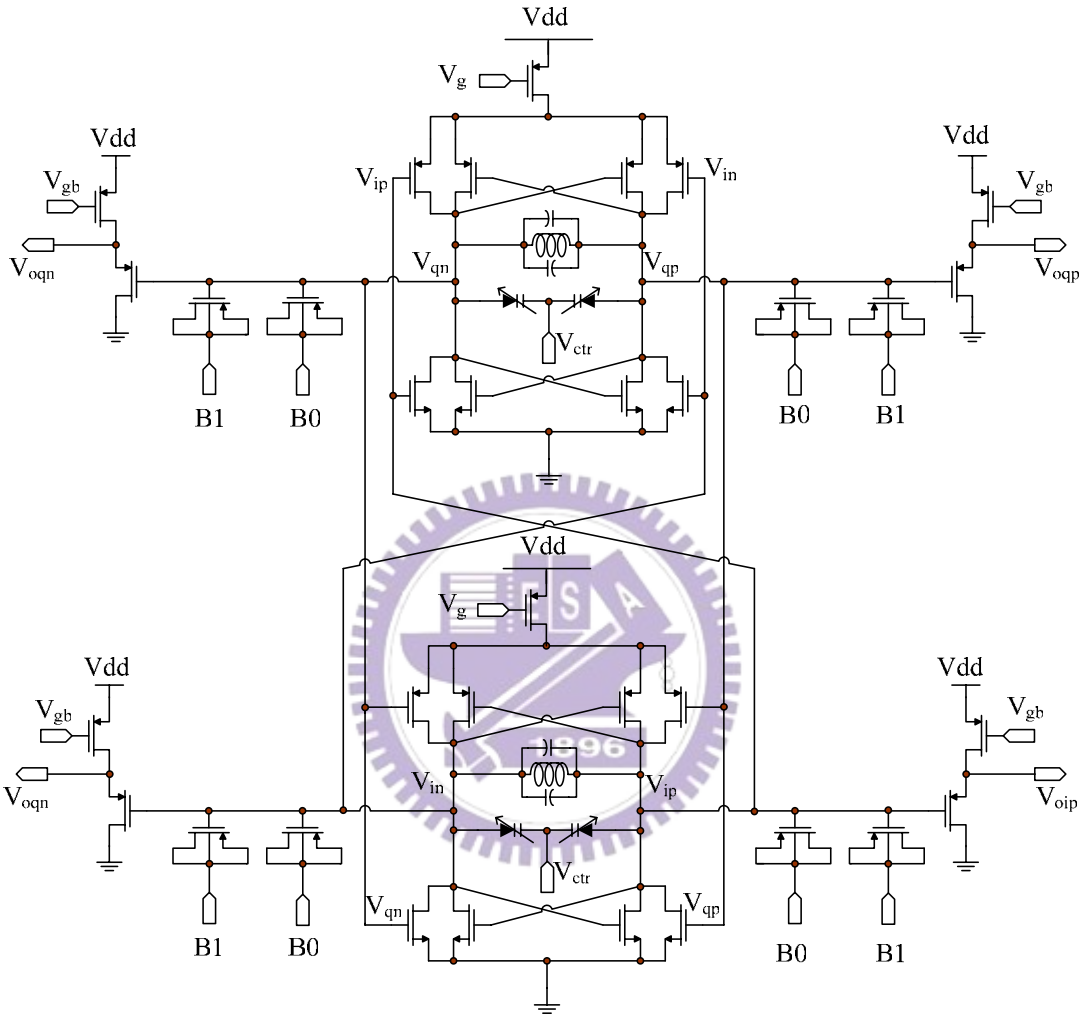
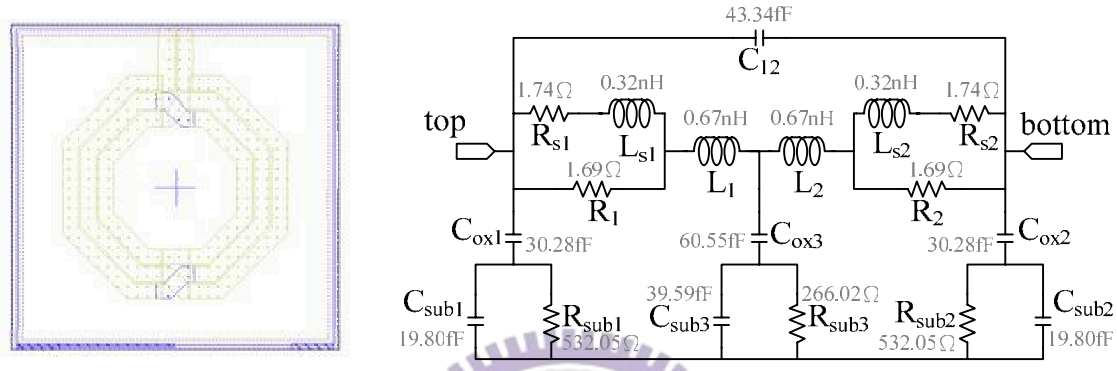


Fig. 3-28 Schematic of QVCO

Fortunately, there are new RF models released from standard model library. The symmetric inductor is able used to enhance the quality factor of LC-tank. We adopt the inductor with radius=60μm, with=15μm, number of turns=3, and spacing=2μm (Fig. 3-29). The total inductance of this inductor is about 2.20nH. Use the MOS varactor (Blanch=25 and Group=4, as showing in Fig. 3-30). So the oscillation frequency of this VCO can oscillate at 2.4-GHz.

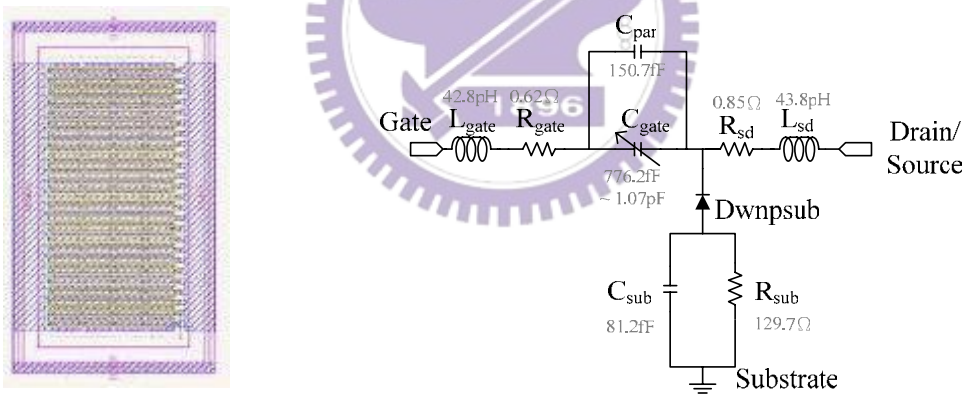
After the trade off between low power consumption and low phase noise, the

optimized bias current [8] is calculated. On the other hand, the transistor size ratio of 3:1 between the core circuit and coupling circuit was used for the best phase noise performance. Therefore, the coupling circuits contribute minimum noise to VCO phase noise performance. These methods reduced the phase noise and power consumption to minimum.



(a) (b)

Fig. 3-29 Spiral inductor in this synthesizer (a)layout (b)equivalent circuit model



(a) (b)

Fig. 3-30 MOS varactor in this synthesizer (a)layout (b)equivalent circuit model

After Eldo RF post-simulation, it shows that the oscillator is tunable between 2.346-GHz and 2.542-GHz (196MHz tuning range) at bank 10. Fig. 3-31 shows the tuning curve of VCO for bank 00, 10 and 11. The corner case of tuning curve for bank 10 is shown in Fig. 3-32. The frequency variation of corner case is quite distinct. We use the capacitor to compensate this variation, as showing Fig. 3-33. The output swing of VCO is shown in Fig. 3-34.

The simulated phase noise is -114.2dBc/Hz @ 1-MHz offset and -127.1dBc/Hz @ 3-MHz offset at 2.45-GHz, as showing in Fig. 3-35. The corner case of phase noise is shown in Fig. 3-36.

The power consumption of two quadrature VCO cores is 8.6mW. The overall power consumption is 16.7mW with buffer output stages.

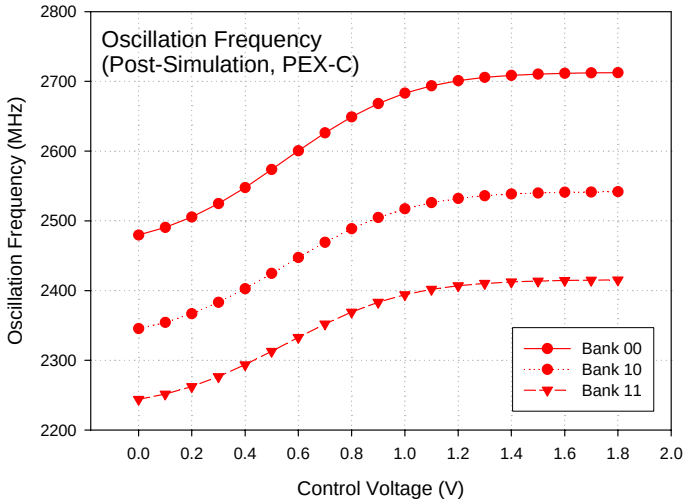


Fig. 3-31 Tuning curve of QVCO (Capacitor bank)

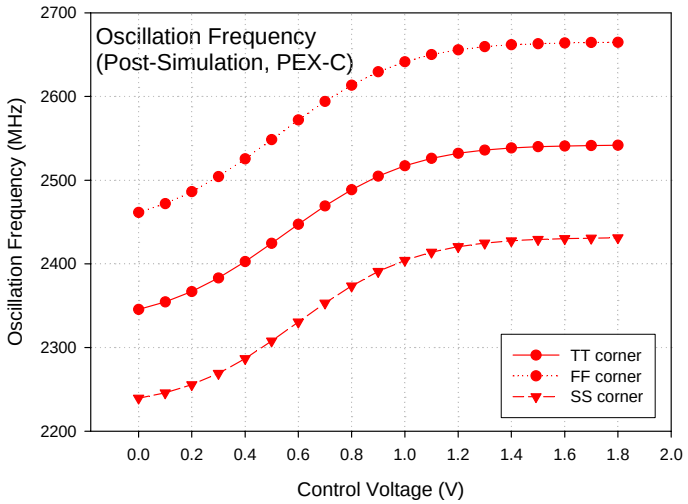


Fig. 3-32 Tuning curve of QVCO (Corner case)

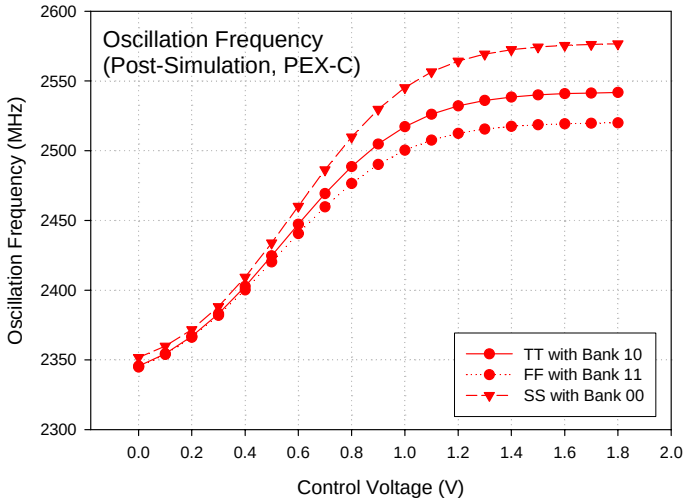


Fig. 3-33 Tuning curve of QVCO (Corner case with bank)

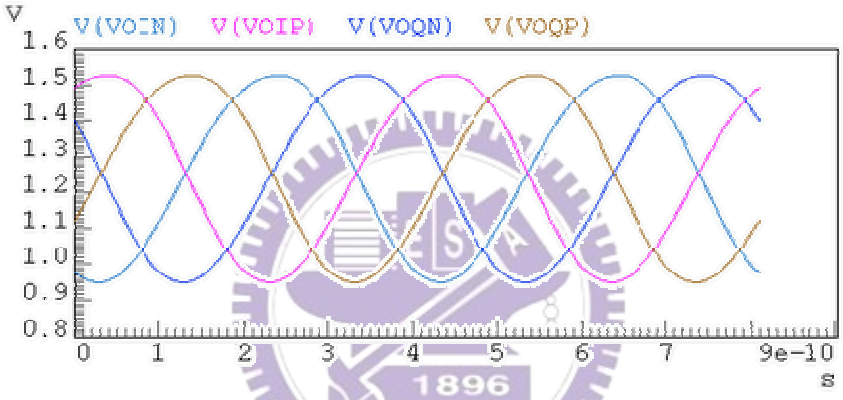


Fig. 3-34 Output Swing of QVCO

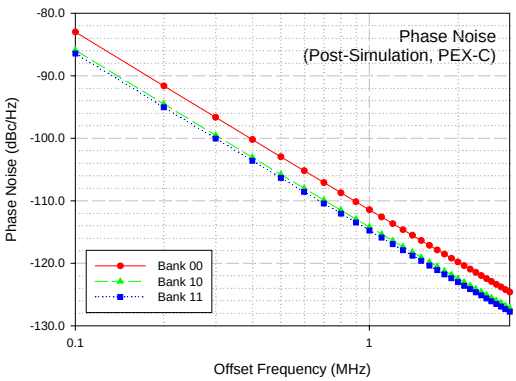


Fig. 3-35 Phase noise of QVCO (Capacitor bank)

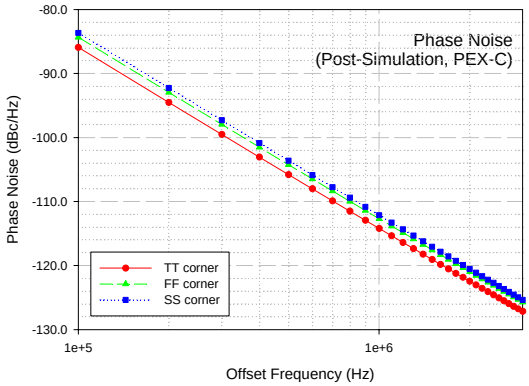


Fig. 3-36 Phase noise of QVCO (Corner case)

◆ Fully programmable multi-modulus frequency divider:

The architecture of fully programmable multi-modulus frequency divider is the same as the former section. We adopt this architecture to implement frequency divider.

The co-simulation result of fully programmable frequency multi-modulus divider and VCO is as shown in Fig. 3-37. The VCO output frequency is set at 2400-MHz and the divide modulus is set at 2400, too. We can obviously observe the period of output divided signal is 1μs, this figures out our divider is working regularly.

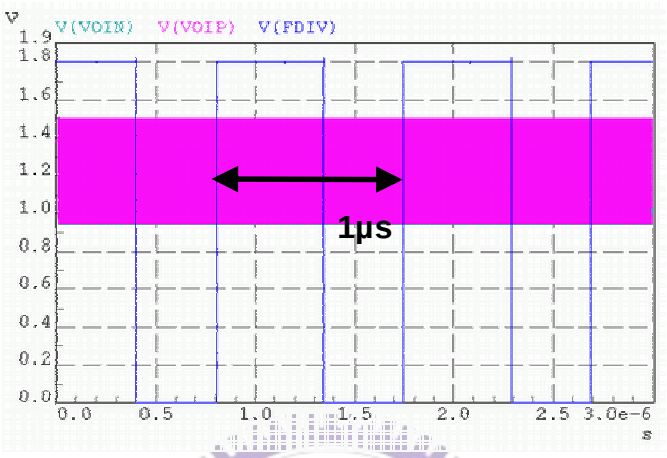


Fig. 3-37 Output signal of frequency divider simulated with VCO

◆ PFD, charge pump, and loop filter:

Also, we adopt the architecture of PFD and charge pump the same as ones in former chapter. 3rd order passive loop filter is used for our design. The optimized values are shown in Table 3-5.

Table 3-5 Optimized loop filter elements

Component	Value
C1	18pF
C2	390pF
R2	47kΩ
C3	18pF
R3	20kΩ

3.2.2 Whole Circuit Simulation and layout

All of the building blocks mentioned in previous sections and chapter will be combined to be a whole frequency synthesizer and simulated together. Synthesizer circuit contains many sub-circuits; whole circuit simulation takes a lot of time. We choose Eldo RF as our simulation tool to lessen simulation time effectively.

The locking transient simulation is shown in Fig. 3-38 and Fig. 3-39, from the simulation result, we can evaluate the lock time is no more than 60μs.

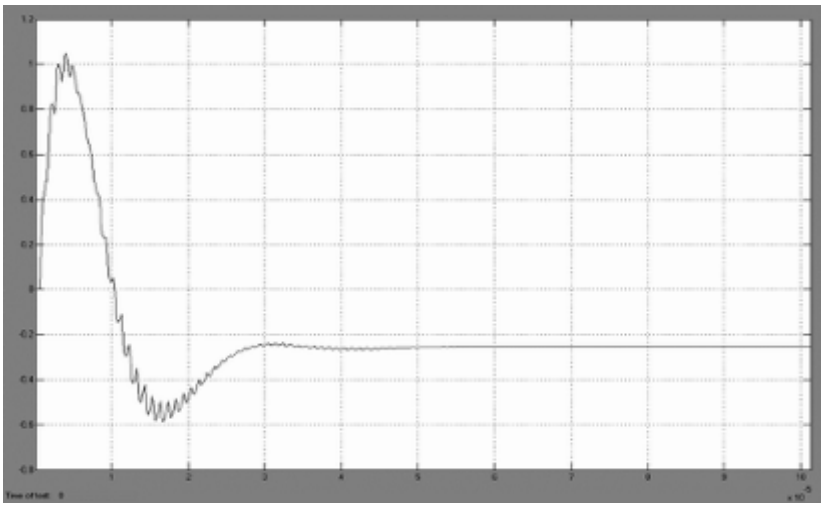


Fig. 3-38 Locking transient simulation (Behavior level simulation)

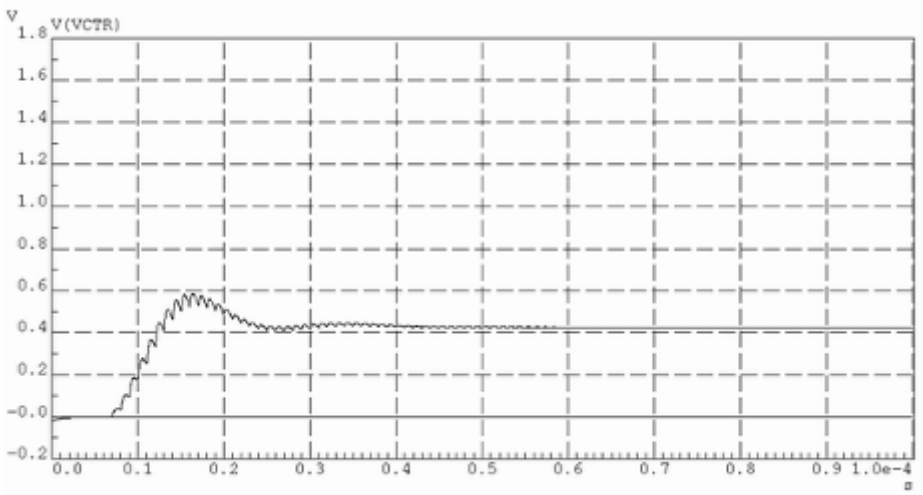


Fig. 3-39 Locking transient simulation (Transistor level simulation)

Table 3-6 Performance summary of low power, low phase-noise integer-N synthesizer

Post-simulation (PEX-C)	**TT corner**	**FF corner**	**SS corner**
Power supply	1.8 V		
Crystal frequency	1MHz		
VCO center frequency @Vctr=0.6V	2.45GHz	2.44GHz	2.46GHz
VCO bank condition	(B1 B0)=(0 1)	(B1 B0)=(0 0)	(B1 B0)=(1 1)
VCO tuning range	2.34 ~ 2.54GHz 200MHz	2.34 ~ 2.52GHz 180MHz	2.35 ~ 2.57GHz 220MHz
Phase noise (dBc/Hz)	-114.2 @1MHz -127.1 @3MHz	-112.3 @1MHz -125.6 @3MHz	-109.9 @1MHz -123.3 @3MHz
VCO output swing (Vpeak to peak)	570mV	650mV	540mV
Settling time	60μs	-	-
VCO power consumption	Two core circuits: 8.6mW Four buffer stages: 8.1mW	Two core circuits: 10.5mW Four buffer stages: 10.4mW	Two core circuits: 7.2mW Four buffer stages: 6.2mW
Prescaler power consumption	10.6mW	13.6mW	7.9mW
Total power consumption	29.1mW	35.6mW	22.0mW

Fig. 3-40 shows the layout of whole chip and Fig. 3-41 shows the die-photograph of whole chip. The die size is roughly 1450μm×900μm.

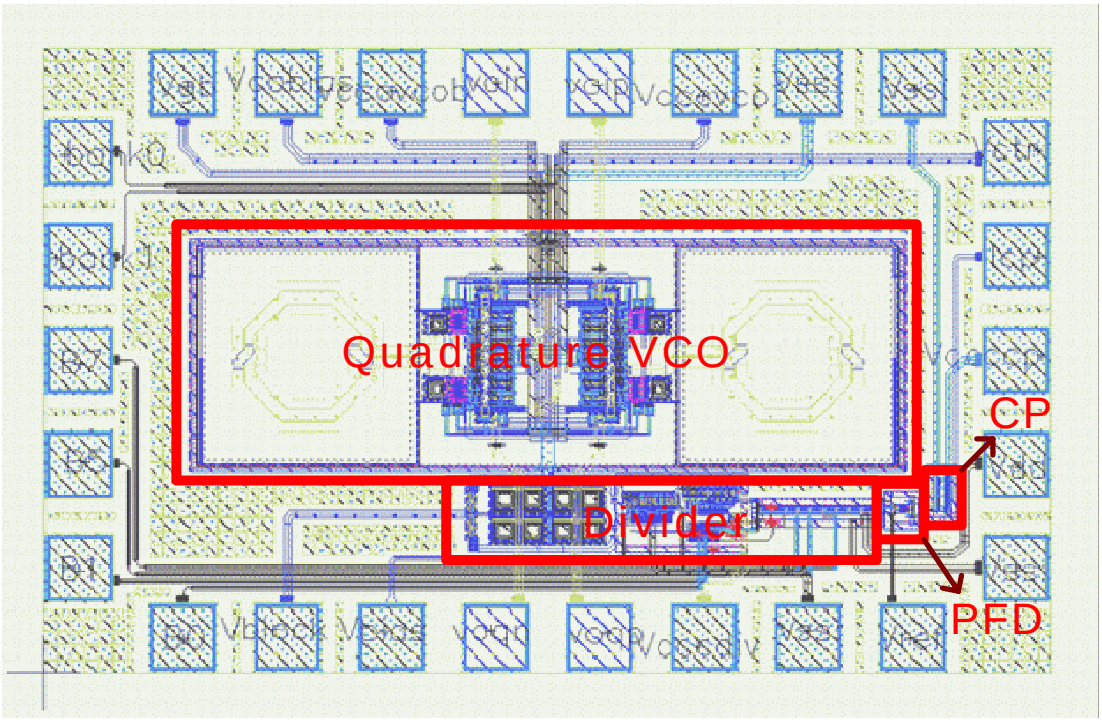


Fig. 3-40 Layout of low power, low phase-noise integer-N frequency synthesizer

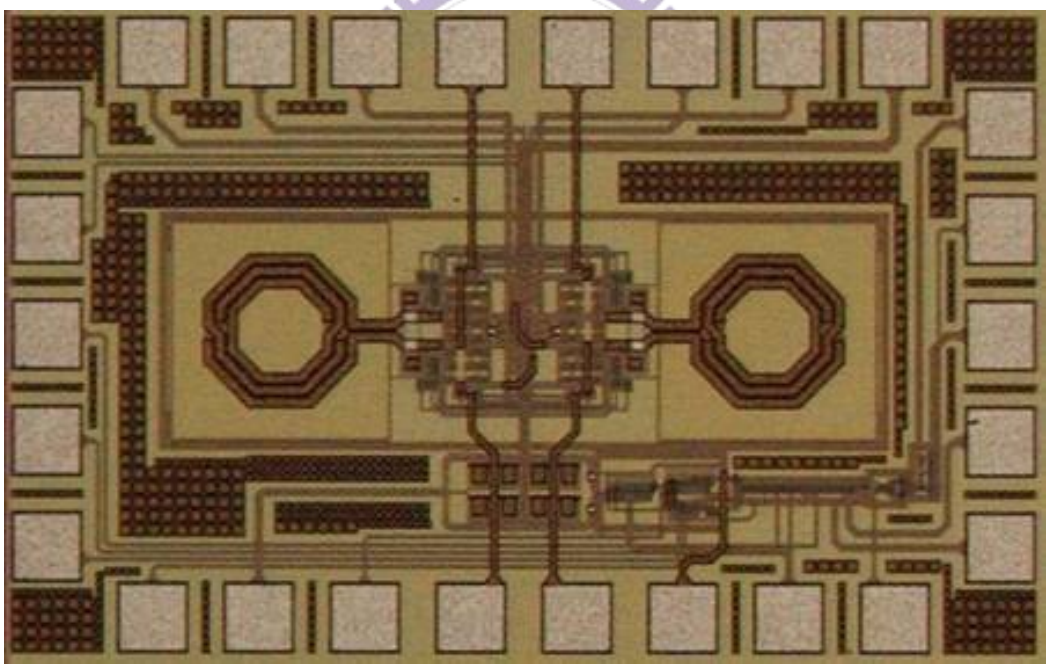


Fig. 3-41 Die-photograph of low power, low phase-noise integer-N frequency synthesizer

3.2.3 Measurement results

This work is bond-wire measurement on PCB. The measuring equipment contains 8563E spectrum analyzer, 54610B oscilloscope, E3611A power supply and HP 33120A function generator.

Fig. 3-42 shows the testing board. The chip is stuck on testing PCB, and wires are bonded from the pad on chip to feed bias voltages. An off-chip 1-MHz crystal oscillator instead of function generator is used to produce reference clock for suppressing the noise coming from reference signal. The loop filter is also designed off-chip for easily modifying element values and decrease chip area although it introduces more noise than designed fully on-chip.

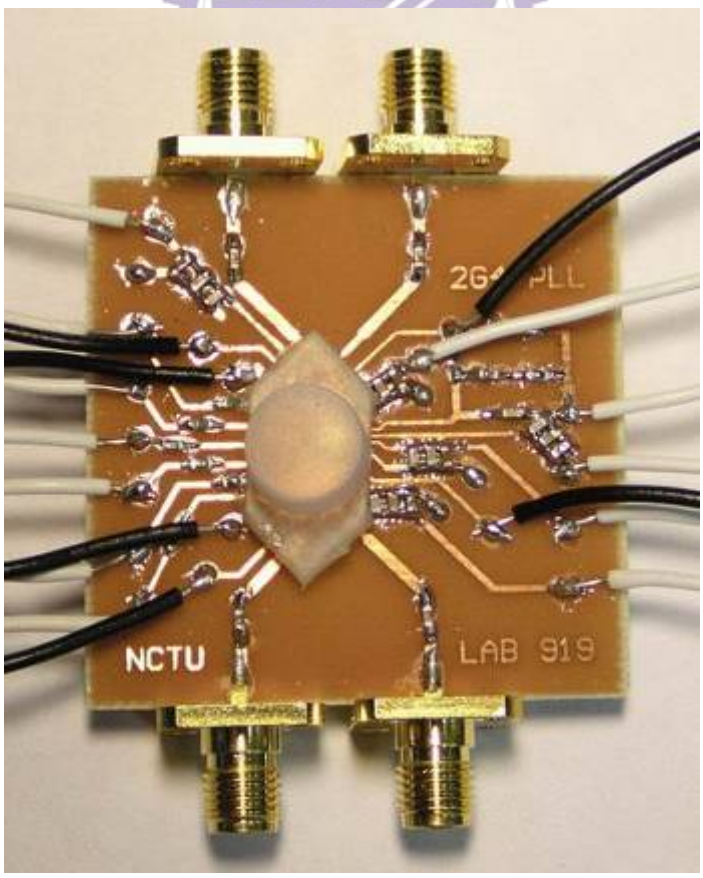


Fig. 3-42 Testing board of low power, low phase-noise integer-N frequency synthesizer

3.2.3.1 VCO Measurement Results

The measured tuning curve and spectrum of VCO in this work is shown as following figures. We can obviously observe that all the bank conditions (from 00 to 11) are all contains the frequency area we need, i.e. whether the oscillator is set in which bank condition, the frequency synthesizer may lock successfully. We use the signal source analyzer to measure QVCO characteristic at bank 10, as showing in Fig. 3-43.

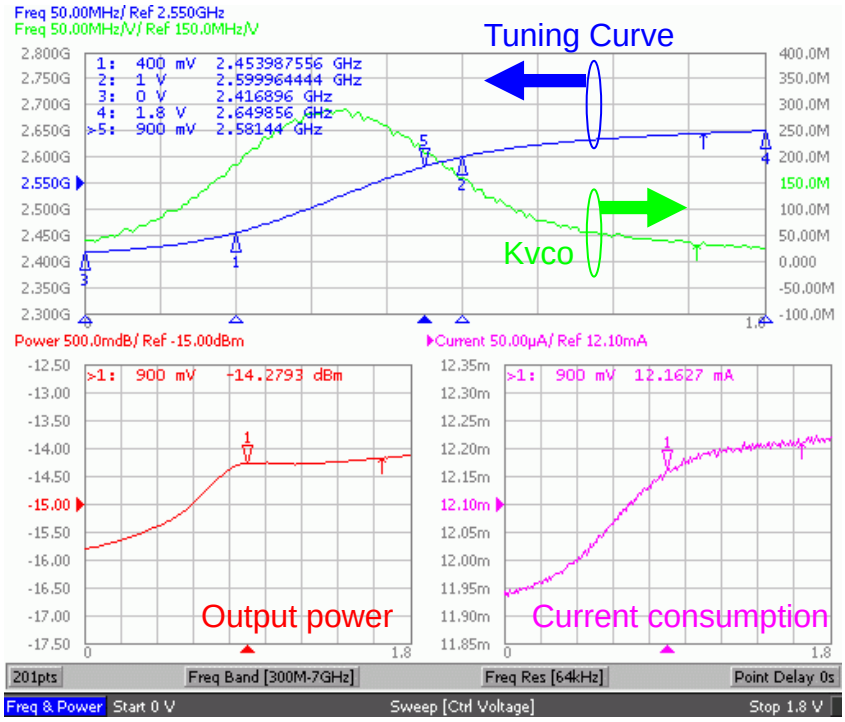
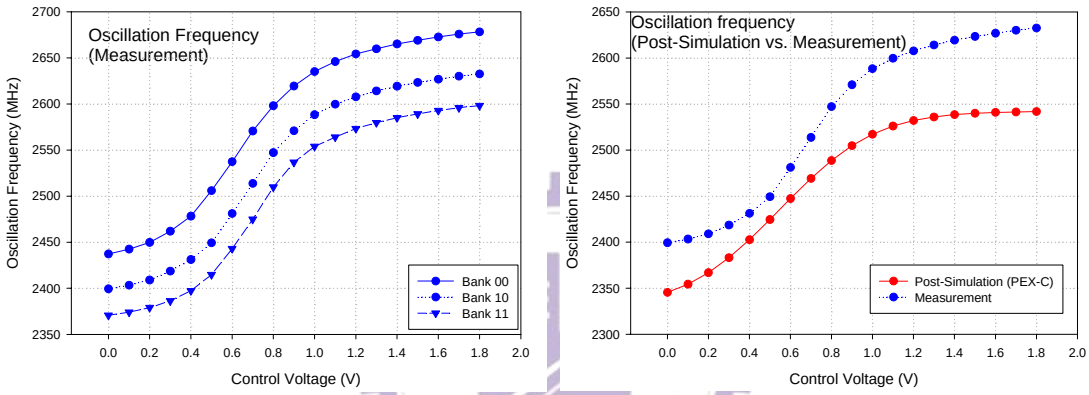


Fig. 3-43 Measured characteristic of QVCO in this synthesizer

The tuning curve at bank 00, 10, and 11 is shown in Fig. 3-44. The measured tuning range is 2.399 ~ 2.633-GHz (at bank condition 10), comparing with our simulation results, the tuning range is 2.350~2.545-GHz at TT corner, it's approximately equal to simulation result. But there is about several ten-MHz differences between simulation result and measurement result. The little difference means the extra parasitic effects are imperfectly evaluated during our simulation. The

main inductance value of spiral inductor may be something difference than the value in model files. Also, this may be resulted from the implemented chip is not at TT corner case. Besides, we use PMOS with mixed-mode model to build a varactor for smaller capacitance variation. It may be some parasitic difference at high operation frequency. Anyhow the tuning range can cover between 2400-MHz and 2483-MHz, just as the original design goal. Fig. 3-45 shows the output spectrum while control voltage is 0.9V at bank 10.



(a) (b)

Fig. 3-44 Measured tuning curve of QVCO in this synthesizer
(a) under different bank conditions (b) at bank 10

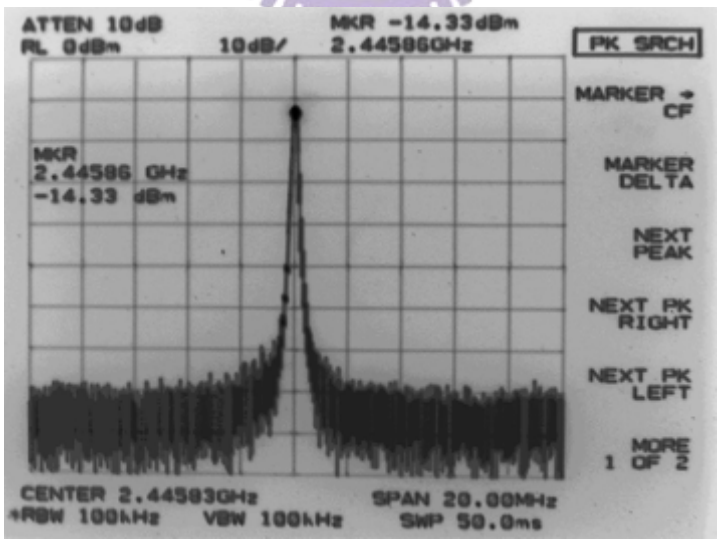


Fig. 3-45 Measured output spectrum of QVCO in this synthesizer

Then we measure noise performance at CIC with signal source analyzer. Noise performance is almost the same as the post-simulation (PEX-C) result: Based on

measurement result, the phase noise @ 1-MHz offset and @ 3-MHz offset form the carrier is about -114.0dBc/Hz and -127dBc/Hz, respectively (Fig. 3-46).

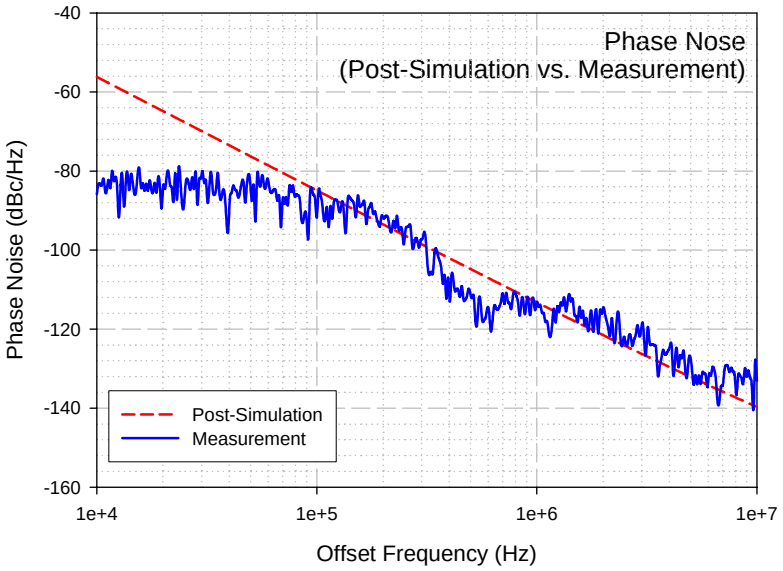


Fig. 3-46 Phase noise of QVCO in this synthesizer (Bank 10, at CIC)

Next we measure noise performance at lab with analog power supply for comparison. Noise performance is also almost the same as the post-simulation (PEX-C) result (Fig. 3-47): Based on measurement result, the phase noise @ 1-MHz offset form the carrier is -114.0dBc/Hz, as shown in Fig. 3-48. This result is 0.2dB difference between simulation (PEX-C) result and measurement result.

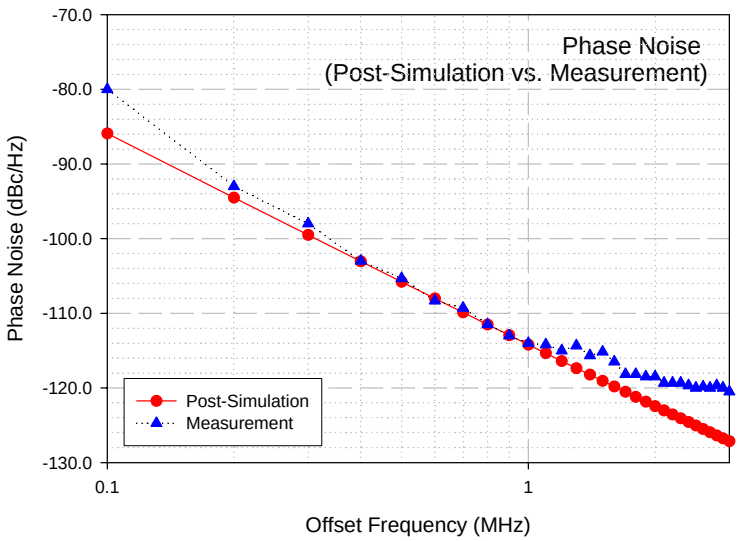
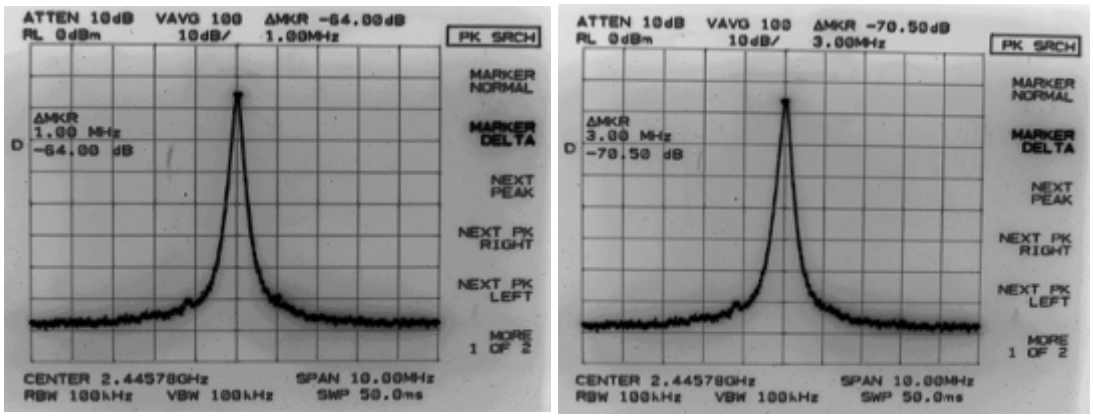


Fig. 3-47 Phase noise of QVCO in this synthesizer (Bank 10, at LAB)



$-64.00dB - 10\log(100 \cdot 10^3)$ $-70.50dB - 10\log(100 \cdot 10^3)$

$= -114.00dBc/Hz$ $= -120.50dBc/Hz$

@1MHz offset @3MHz offset

(a) (b)

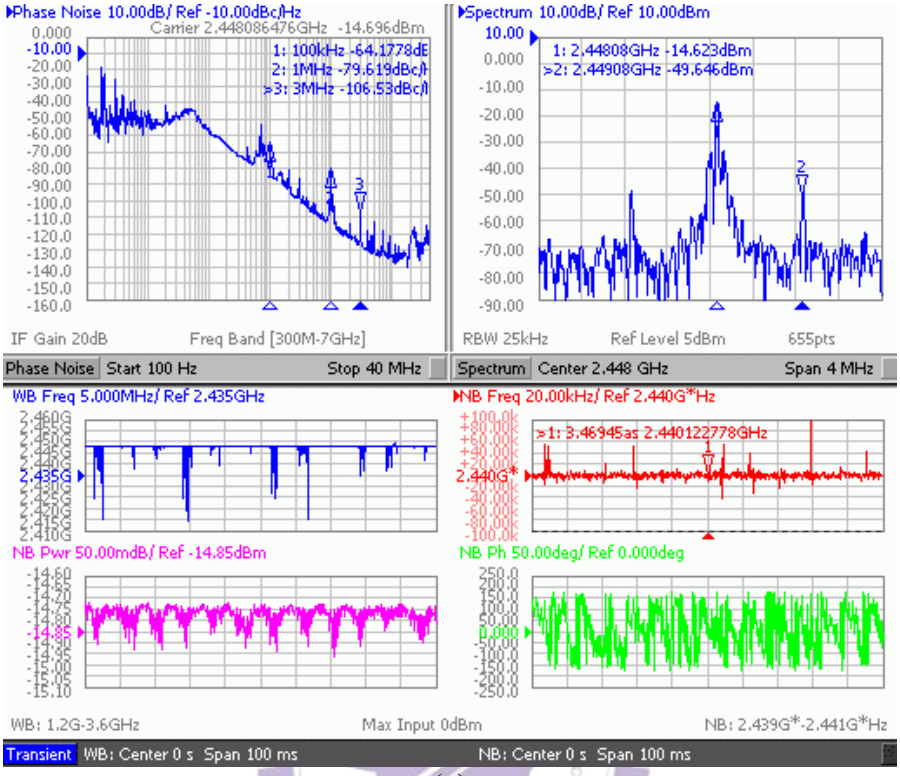
Fig. 3-48 Measured phase noise of QVCO in this synthesizer (Bank 10, at LAB)
(a) at 1-MHz offset (b) at 3-MHz offset

3.2.3.2 Whole Circuit Measurement Results

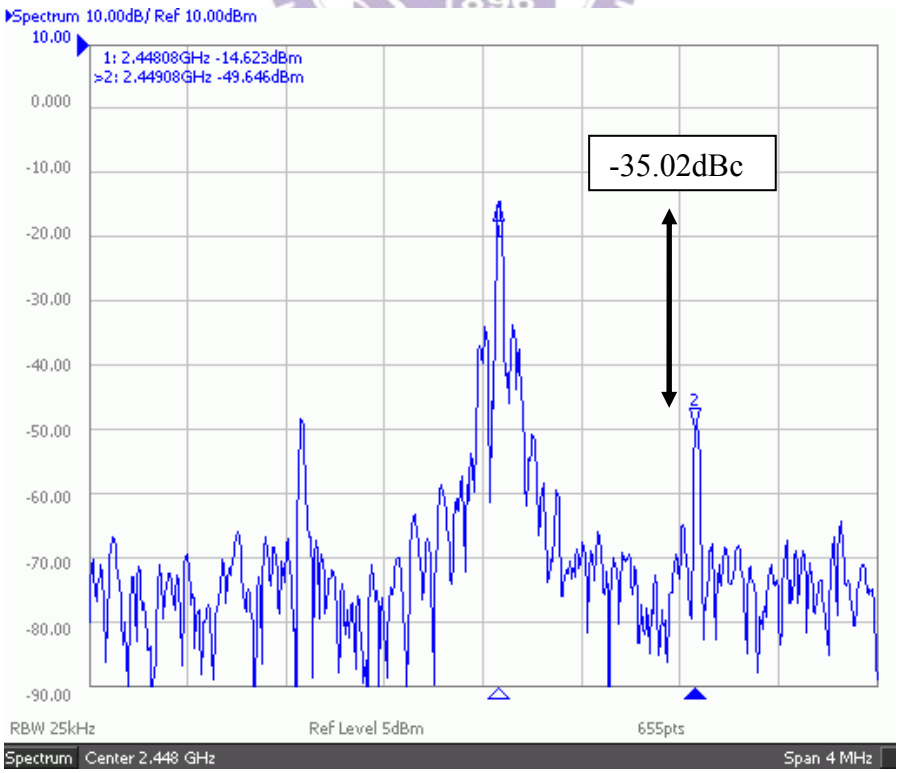
The whole frequency synthesizer's measurement data are shown in following figures. We measure this circuit at CIC. Fig. 3-49(a) is total measurement results using Agilent E5052A signal source analyzer and Fig. 3-49(b) is the output spectrum while frequency synthesizer locked at 2448-MHz. These figures show the spurious tone vs. carrier of frequency synthesizer is about -35.02dBc. Fig. 3-49(c) shows the phase noise performance while frequency synthesizer locked at 2448-MHz. The measured phase noise of close-loop synthesizer compared with VCO is showing in Fig. 3-50.

Fig. 3-51(a) is the measurement result while divider ratio changing from 2448 to 2480. We can see that the settling time is about 100μs. Fig. 3-51(b) is zooming in of measurement data. Based on NB (narrow band) frequency analyzer, it shows that output frequency variation is less than 60-kHz (25ppm of center frequency) while synthesizer is locking at 2480-MHz. Because there is the FM residue on output signal, the output phase is still change with about 16μs period (the frequency is about

60-kHz). The phase variation is a normal phenomenon while an imperfect output of frequency synthesizer.



(a)



(b)

(c)

Fig. 3-49 Measured locking spectrum
(a) All performance of synthesizer (b) Output spectrum (c) Phase noise performance

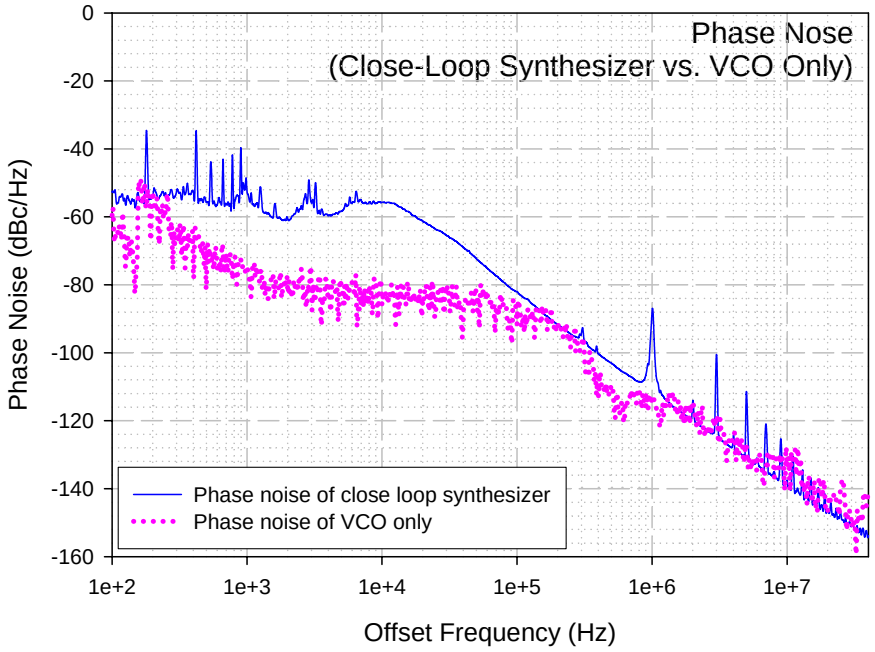
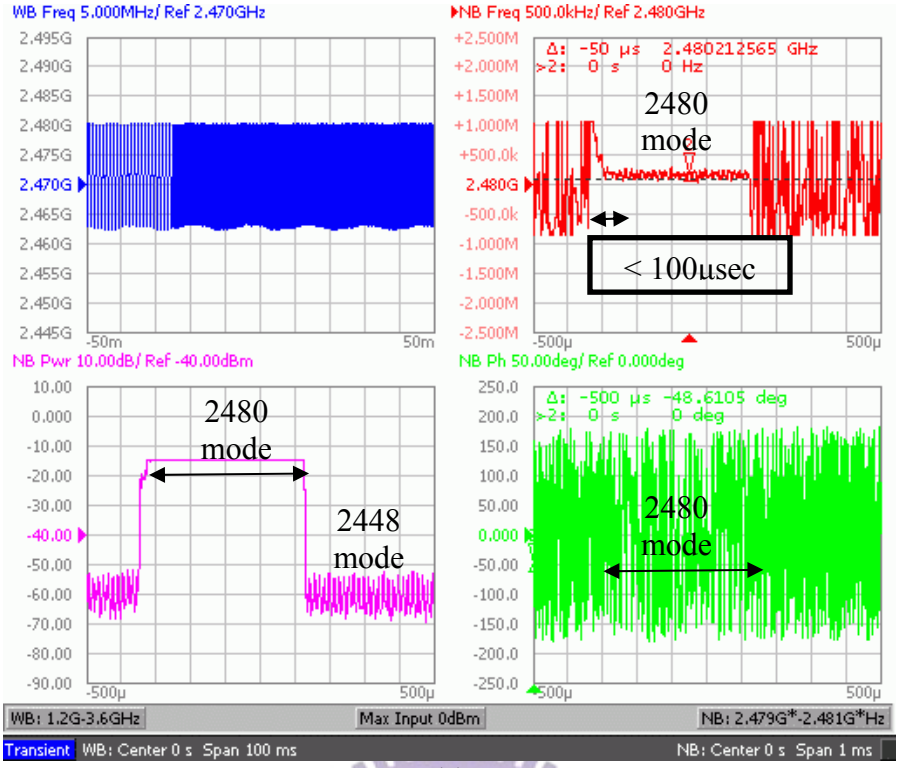
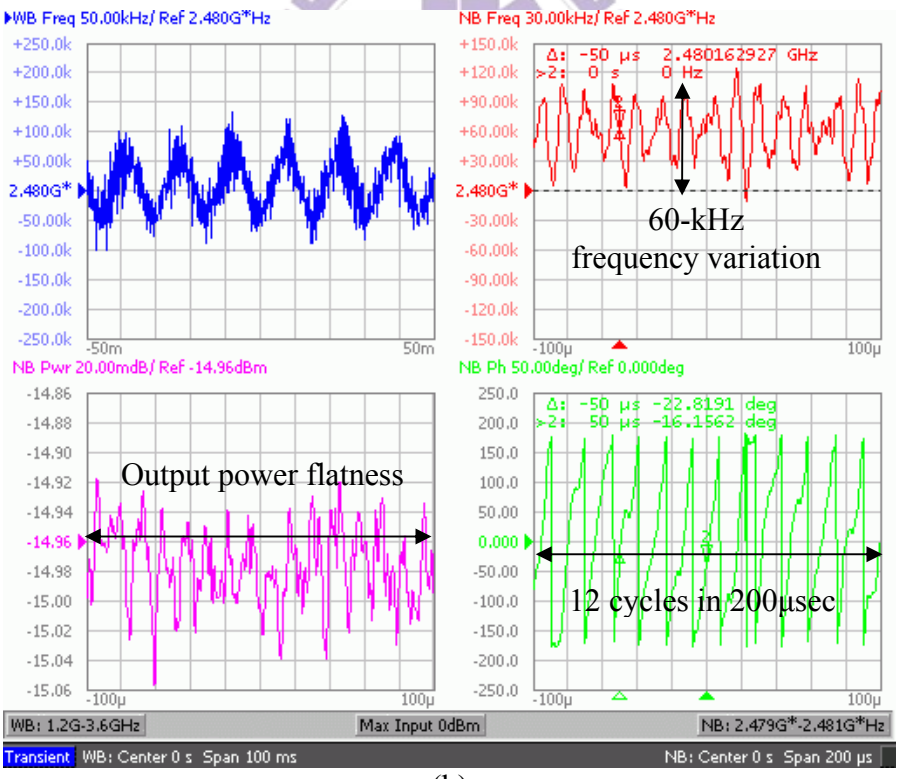


Fig. 3-50 Measured phase noise (close-loop synthesizer vs. VCO only)



(a)



(b)

Fig. 3-51 (a) Measurement result while divider ratio changing from 2448 to 2480
(b) Zoom in of measurement results

We adopt another measurement at lab using HP 8563E spectrum analyzer, as shown in Fig. 3-52. These figures show the spurious tone vs. carrier of frequency synthesizer is about -41.50dBc. The spurious performance is about 6dB better than data at CIC.

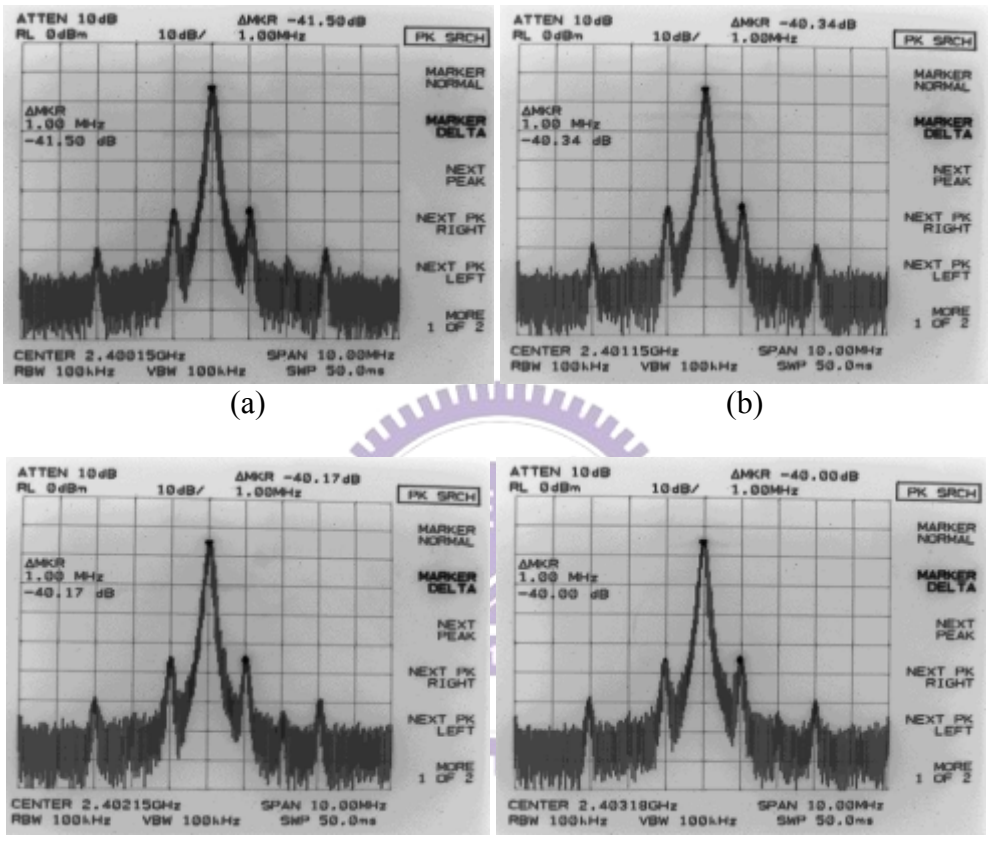
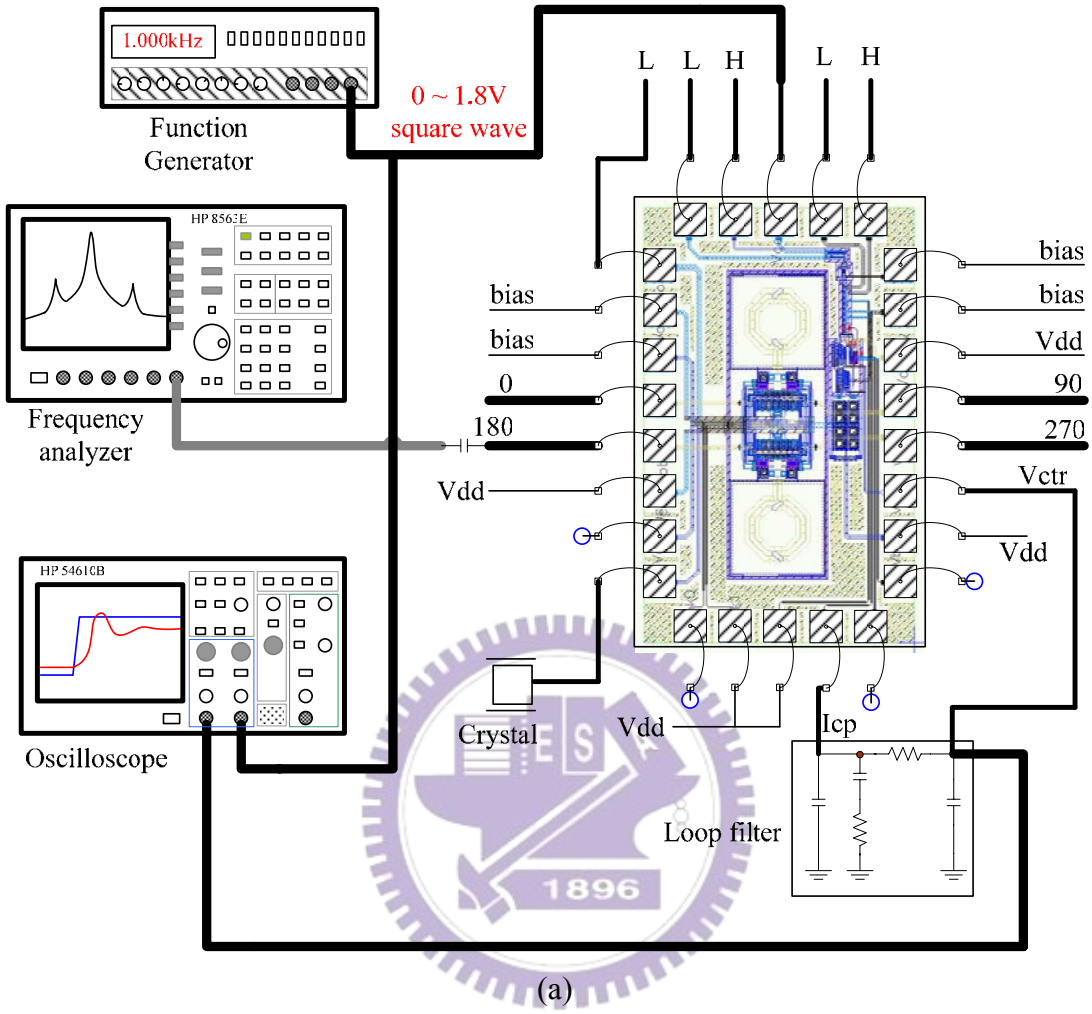


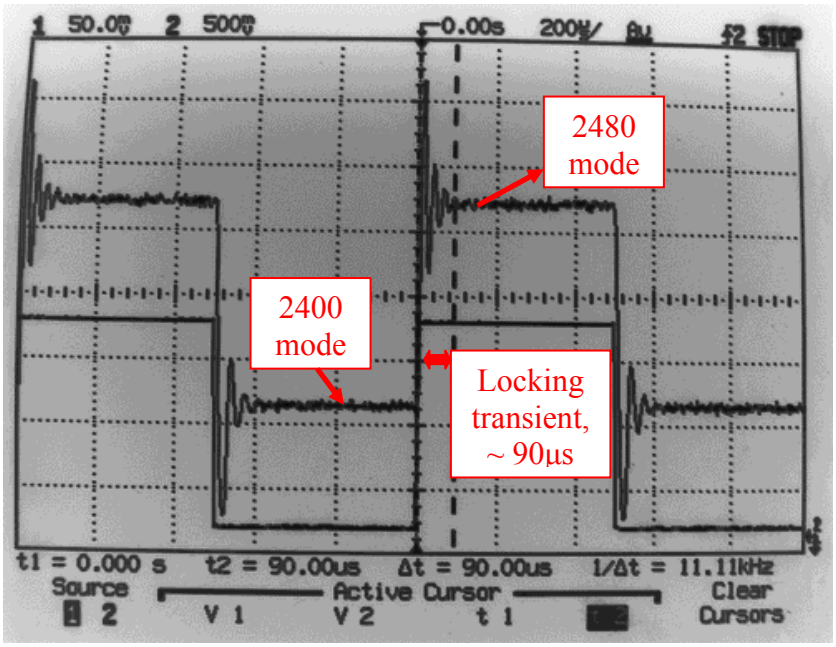
Fig. 3-52 Measured locking spectrum
(a) at 2400-MHz (b) at 2401-MHz (c) at 2402-MHz (d) at 2403-MHz

Next we use the function generator as a trigger source. The measurement consideration of settling time is showing in Fig. 3-53a. The function generator outputs low frequency signal to feed the control bit of multi-modulus prescaler. It results that the output frequency is changed between 2400-MHz and 2480-MHz. So we can measure the settling time using a normal oscilloscope. Fig. 3-53b and Fig. 3-53c are the VCO input control voltage node waveforms. They represent the locking transient waveforms of this frequency synthesizer. The locking settling time shows it is about

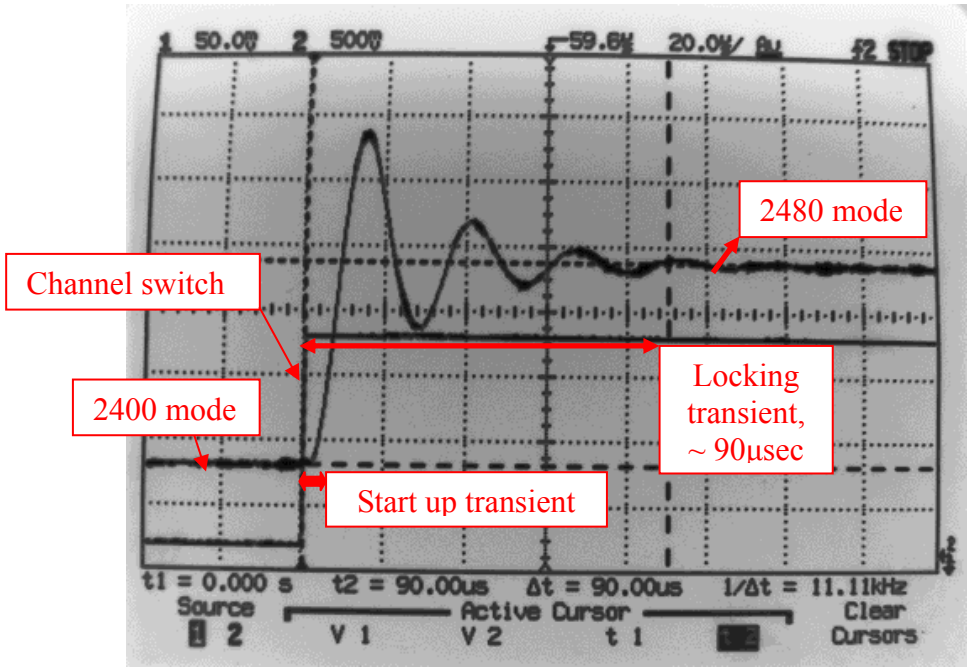
90μs.


1.000kHz
Function Generator
0 ~ 1.8V square wave
HP 8563E
Frequency analyzer
HP 54610B
Oscilloscope
L L H L H
bias
bias
0
180
Vdd
bias
bias
Vdd
90
270
Vctr
Vdd
Crystal
Vdd
Icp
Loop filter

(a)


2480 mode
2400 mode
Locking transient, ~ 90μs
t1 = 0.000 s
t2 = 90.00us
Δt = 90.00us
1/Δt = 11.11kHz
Source
Active Cursor
Clear Cursors
V 1
V 2
t 1

(b)



(c)

Fig. 3-53 (a) Measurement consideration of settling time
(b) Transient of settling time
(c) Zoom in of the transient of settling time

3.2.4 Measurement Discussions

Based on measurement results, the phase noise is almost the same as simulation results. The spur performance is excellent, -41.50dBc @1-MHz reference frequency. But there is some difference in tuning curve. However, the tuning range can cover between 2400-MHz and 2483-MHz, just as the original design goal. The measured data in this chapter are summarized in Table 3-7 and 3-8.

Table 3-7 Summary of specifications

Performance	**Post-simulation (PEX-C)**	**Measurement**
Power supply	1.8V	
Reference frequency	1MHz	
Bank condition	10	
Tuning range of VCO	2.346 ~ 2.542GHz	2.399 ~ 2.633GHz
Phase noise	-114.2dBc/Hz @1MHz -127.1dBc/Hz @3MHz	-114.0dBc/Hz @1MHz -120.5dBc/Hz @3MHz
Output power level	-10.72dBm	-14.33dBm
Spur. tone vs. carrier	N/A	-41.50dBc @1MHz
Locking time	60μs	90μs

Table 3-8 DC current consumption

Block	**Post-simulation**	**Measurement**
Two VCO cores	8.6mW	8.1mW
Four buffer stages	8.1mW	8.1mW
Frequency divider	10.6mW	10.8mW
Charge pump	1.1mW	1.08mW
Rest parts of PLL	0.2mW	0.2mW
Total	29.1mW	28.3mW

3.3 Comparison of Measurement results

Table 3-9 compares the measurement results. In wide tuning range frequency synthesizer, the tuning range is approach 27.6% of center frequency with overall bank conditions (code-000 to code-111) and locking time is less than 40μs. In the low

power, low phase noise frequency synthesizer, the phase noise is -114.0dBc/Hz@1-MHz offset and the power consumption is only 28.3mW. The locking time is less than 90μs and spurious tone is -41.50dBc @1-MHz reference frequency.

Table 3-9 Performance summaries with two integer-N frequency synthesizer

Performance		**Wide tuning range synthesizer [10]**	**Low power and low phase-noise synthesizer**
Technology		CMOS 0.18μm	
Architecture		Integer-N (11 stages of %2/3)	
Voltage		1.8V	
Reference frequency		1MHz	
Bank condition		(B2 B1 B0)=(0 1 1)	(B1 B0)=(1 0)
Chip size		1500μmX1100μm	1450μmX900μm
Tuning range (GHz)		2.18~ 2.63 (18.8%)	2.39~ 2.63 (10%)
Phase noise (dBc/Hz)		-108.8 @1MHz	-114.0 @1MHz
Spur tone vs. carrier		-26.15dBc @1MHz	-41.5dBc @1MHz
Settling time		40μs	90μs
Power	**Two VCO cores**	10.8mW	8.1mW
	Four buffer stages	12.8mW	8.1mW
	Frequency divider	13.5mW	10.8mW
	Charge pump	1.1mW	1.08mW
	Rest parts of PLL	0.2mW	0.2mW
	Total	38.4mW	28.3mW

Chapter 4

5.2-GHz Low Power, Wide Tuning-Range SiGe BiCMOS VCO and 2.4-GHz Low Power, Low Phase-Noise, Quadrature Output CMOS VCO

Through this chapter, we discuss the design of VCO for various purposes. For low cost requirement, we design a 5.25-GHz low-power VCO by 0.35-μm 3P3M SiGe BiCMOS technology. Another view of VCO designing is low phase noise requirement. We design a low phase noise 2.4-GHz VCO by 0.18-μm 1P6M CMOS technology. In order to realize the system-on a chip (SOC), the CMOS technology is considerate because of it is compatible with digital ICs of base-band circuits.

4.1 A 5.2-GHz low power, wide tuning-range SiGe BiCMOS VCO

4.1.1 Design Consideration

This chip is fabricated in October 2003. In recently high-frequency operation VCO designs, high power consumption is always an unavoidable limitation, which can be obviously observed in [15-19]. In this design, LC-tank structure is used for a low-power, low-phase-noise oscillator design. The VCO core is based on conventional

cross-coupled negative-Gm topology, as shown in Fig. 4-1, contains a LC-resonator with cross-coupled pairs of NPN and PMOS transistors as active part. The architecture of cross-coupled pairs adopts both NPN and PMOS transistors to enhance negative conductance. Considering that NPN transistors have lower flicker noise (1/f noise) than NMOS transistors, we replace NMOS with NPN transistors. By using a PMOS transistor on the top, the phase noise contributed from the low frequency noise of a bias circuitry can be reduced [15].

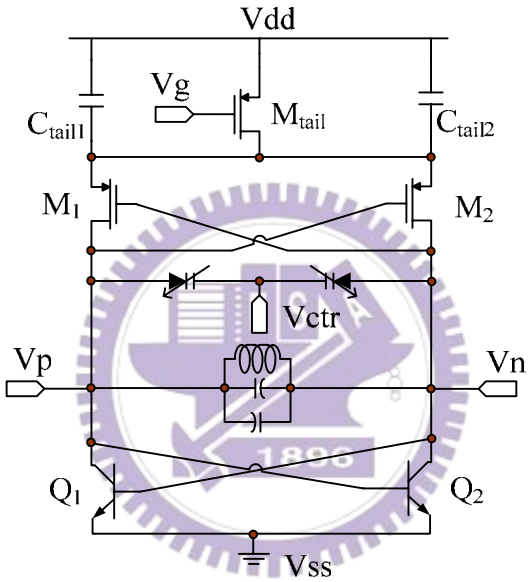
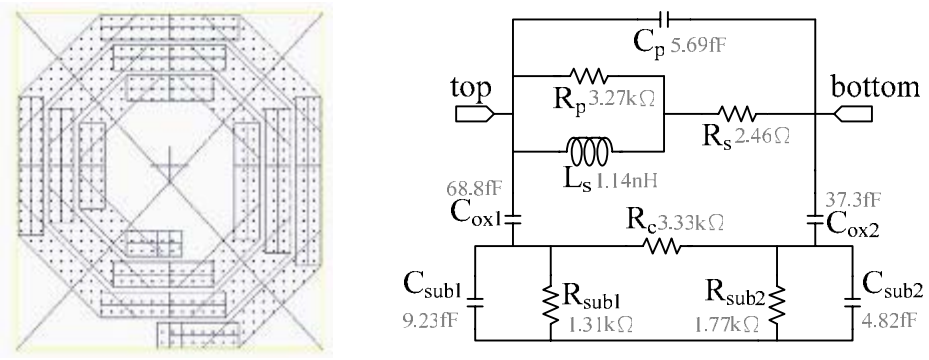


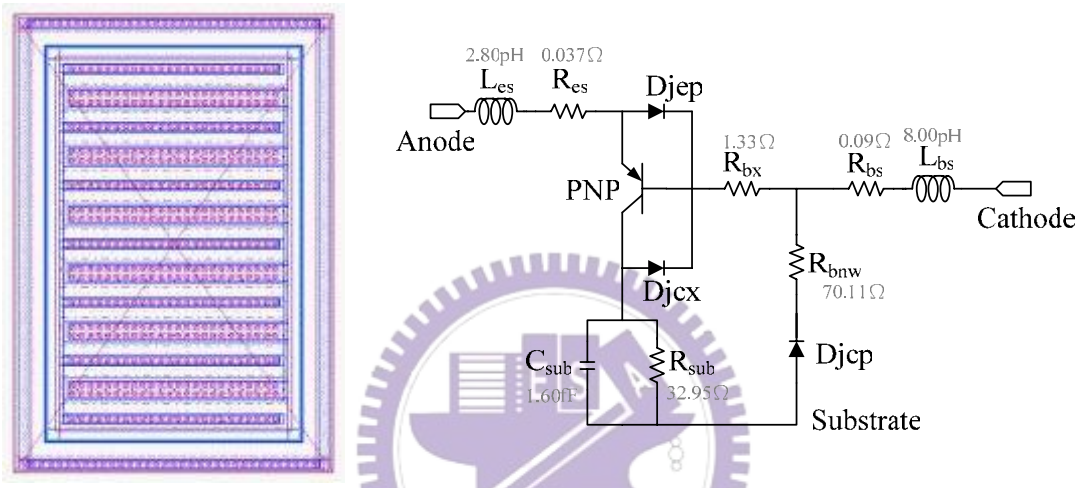
Fig. 4-1 Schematic of the low-power VCO

The LC-resonator is implemented as an on chip spiral inductor (Fig. 4-2), a pair of p+/n junction varactors (Fig. 4-3) and MIM capacitors. The junction varactor has the higher capacitance tuning range and is adopted in the VCO to extend the frequency tuning range, although it has worse phase noise than MOS varactor. The MIM capacitor has the higher quality factor to improve the quality factor of LC tank. In this topology, only one inductor is paralleled with varactors to build the LC-resonator, instead of two inductors paralleled to ground.



(a) (b)

Fig. 4-2 Spiral inductor in this VCO (a) layout (b) equivalent circuit model



(a) (b)

Fig. 4-3 Junction varactor in this VCO (a) layout (b) equivalent circuit model

For low power consideration, the bias current of VCO core circuit should be less than normal value when this circuit is operated at V_{DD}=3.3V. The bias voltage of current source should be chosen carefully under this low voltage condition. From [25], we have the following equations:

$$G_M = \frac{R_{eff}}{(\omega_0 L)^2} = \frac{2.455\Omega}{(2\pi \cdot 5.35GHz \cdot 1.141nH)^2} \approx 1.669mS \qquad (4\text{-}1)$$

G_M means the trans-conductance of MOS in –Gm cell, and R_{eff} means the effective resistance of the LC tank. Which gives a good trans-conductance to current ratio and hence power consumption can be reduced. However, ensuring the oscillation start-up, 2.5 times of value is G_M chosen. After g_m=2.5·G_M is set, the total current consumption can be calculated:

$$I_{Total} = 2I_{M1} = 2 \cdot \frac{1}{2} gm \cdot (V_{GS} - V_T) \quad (4\text{-}2)$$

Under this bias condition, the VCO output waveform swing is V_A. Assume V_A is 300mV (peak-to-peak). Then phase noise at 1-MHz offset L {1MHz} can be estimated easily:

$$\begin{aligned} L\{\Delta f\} &= \frac{kT \cdot R_{eff} \cdot [1 + A] \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2}{\frac{V_A^{\,2}}{2}} \\ &= \frac{kT \cdot 2.455\Omega \cdot (1 + 2.5)(\frac{5.35GHz}{1MHz})^2}{\frac{(0.3)^2}{2}} \\ &\approx -106.45dBc/Hz \end{aligned} \quad (4\text{-}3)$$

Δω and A represent frequency offset from carrier, and noise from the active device of oscillator amplifier respectively. Through the equations above, the bias voltage can be set and tradeoff between low-power and low phase-noise is also better than the required specification. The above estimation is about 3dB estimation will be given by measurement in the following section.

RF output buffer, shown in Fig. 4-4, is used for VCO output frequency measurement with a spectrum analyzer directly. There are two reasons we adopts the PMOS source follower architecture as output buffer:

First, source follower exhibits high input impedance and a moderate output impedance. It also can improve the isolation between the circuit and output pads, and the spectrum analyzer. Such design prevents the loading effects from the measurement to influence the oscillation frequency.

Second, in the p-type substrate process the bulk of the PMOS is tied to the source, so the body effect can be eliminated. The harmonic term due to output buffer can be

reduced because PMOS source follower in the N-well eliminates the nonlinearity.

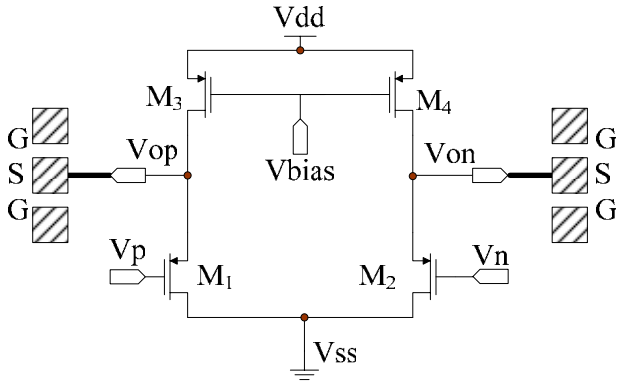


Fig. 4-4 Schematic of the output buffer stage

4.1.2 Simulation results and layout

A low-power SiGe VCO is designed and optimized through Eldo RF simulator. Fig. 4-5 shows the whole circuit layout. The total chip size including pads is 860μm x 610μm. This design of VCO is implemented using 0.35-μm 3P3M SiGe BiCMOS process. At high frequencies, the drain and source of a MOSFET, pads, inductors, and other elements on the silicon substrate have resistive components due to lossy silicon substrate. These parasitic resistances generate additional thermal noise, degrade the phase noise performance. To avoid these effects from pads, we also take advantage of the shielded signal PAD as shown in Fig. 4-6 to reduce noise coupling from the noisy silicon substrate. Besides, the symmetry of layout is very important in this circuit.

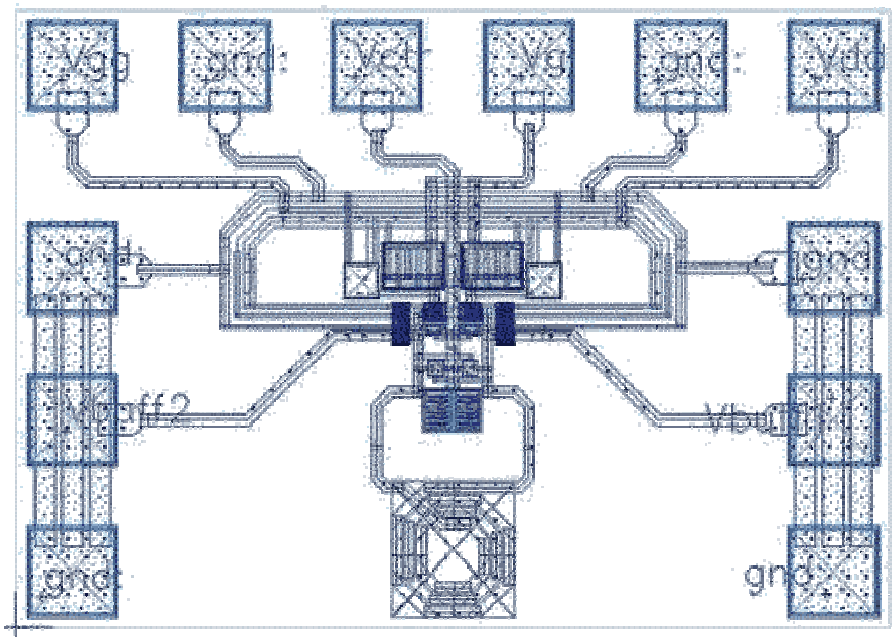


Fig. 4-5 Layout of the low-power VCO

The Eldo RF post-simulation performances including all extracted parasitic are shown in the following. Based on simulation result, it shows this oscillator is tunable between 4.80-GHz and 5.46-GHz (12.3 % tuning range), as showing in Fig. 4-7. From 5.15-GHz to 5.35-GHz, the curve is approximately linear. This implies a constant K_{VCO} in the operation range; it is an advantage for phase-locked loop or frequency synthesizer design. Since the parameter K_{VCO} is nearly constant, the open loop gain of PLLs or synthesizers will be constant during locking and so that we don't require dynamic adjustment of the charge pump circuit. In this design, the average K_{VCO} is about 470 MHz/V.

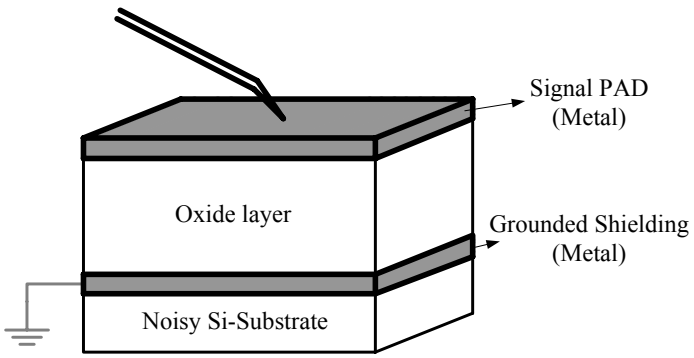


Fig. 4-6 Shielded signal PAD structure

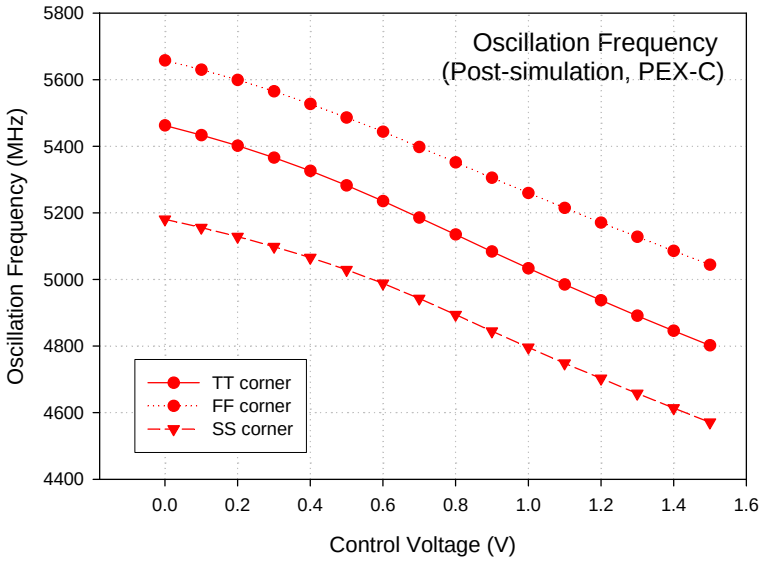


Fig. 4-7 Tuning curve of the low-power VCO

The phase noise is -92dBc/Hz at 100-kHz offset from the carrier, -112dBc/Hz at 1-MHz offset, and -122dBc/Hz at 3-MHz offset, as showing in Fig. 4-8. This specification is below -110dBc/Hz at 1MHz offset, which satisfies IEEE 802.11a standard. The output transient waveform simulation result is shown in Fig. 4-9. It shows that the amplitude of plus and minus output signals are about equaled. Table 4-1 summarizes the specifications of this VCO.

Table 4-1 Post-simulation result of the low-power VCO with corner case

Post-simulation (PEX-C)	**TT corner**	**FF corner**	**SS corner**
VCO core circuit power (mW)	3.59	4.60	2.78
Total power consumption (mW)	17.86	22.07	15.13
Center frequency (GHz)	5.20	5.41	4.94
Tuning range (GHz)	4.80 ~ 5.46	5.05 ~ 5.67	4.57 ~ 5.18
Phase noise (dBc/Hz) @1MHz offset	-112.0	-108.3	-108.7

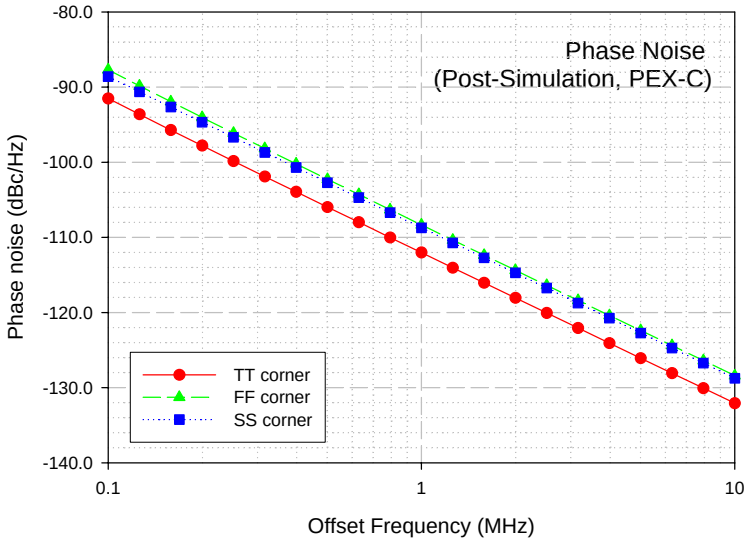


Fig. 4-8 Phase noise of the low-power VCO

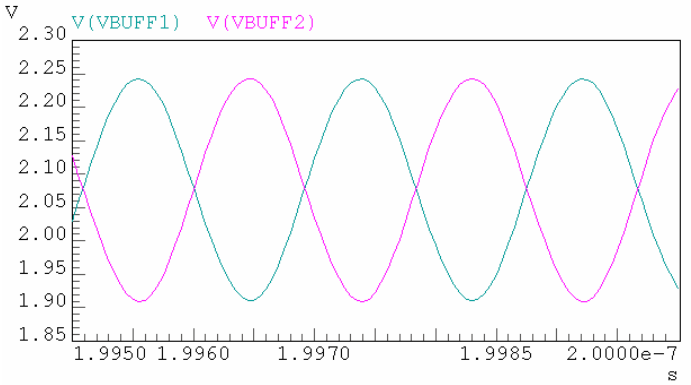


Fig. 4-9 Output waveforms of the buffer stages

4.1.3 Measurement results

The measurement arrangement for our design of low-power VCO is shown in Fig. 4-10. Fig. 4-11 shows the die-photograph of the VCO. We applied for Chip Implementation Center (CIC) on wafer RF GSG (Ground-Signal-Ground) probe measurement. The measurement is performed by a probe station, spectrum analyzer (HP8563E, frequency range: 9-kHz ~ 26.5-GHz), and RF GSG probe. The total power consumption is 16.7mW. Fig. 4-12 shows measured spectrum of the VCO for a center frequency of 5.5-GHz. In the Fig. 4-13, a tuning range of 770-MHz (4.73 ~ 5.50-GHz, about 15%) is measured for control voltage variation from 0 to 1.5V. If the control

voltage is larger than 1.5V, this circuit doesn't oscillate. Based on Fig. 4-12, phase noise of the VCO is about -92.8dBc/Hz @ 1-MHz offset from the carrier.

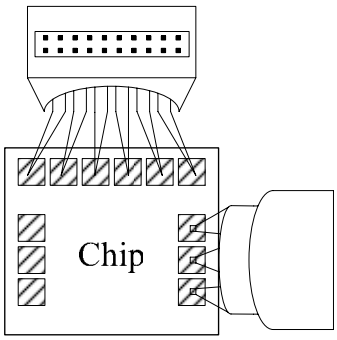


Fig. 4-10 On wafer measurement arrangement

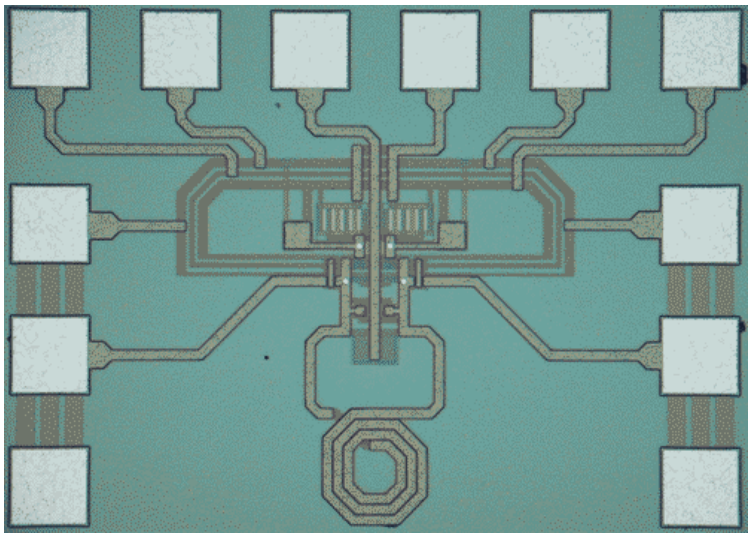


Fig. 4-11 Die-photograph of the low-power VCO

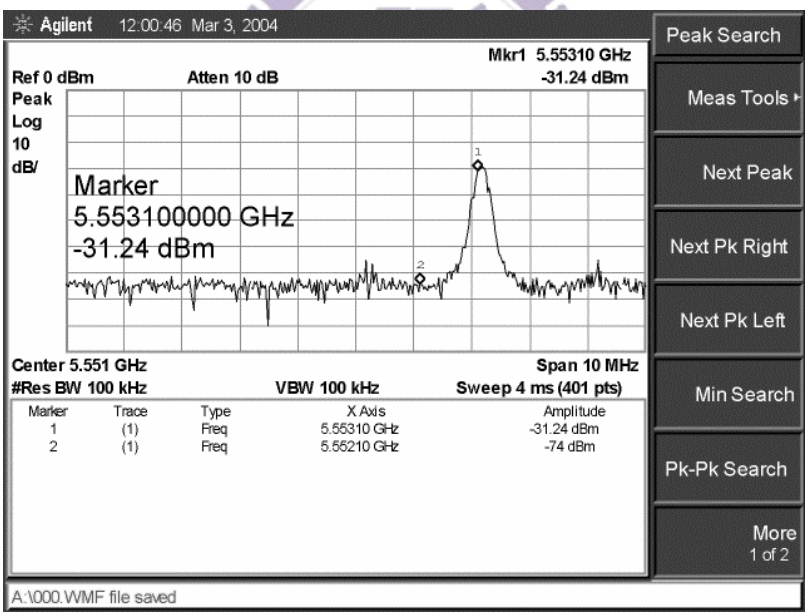


Fig. 4-12 Measured output spectrum of VCO (On wafer)

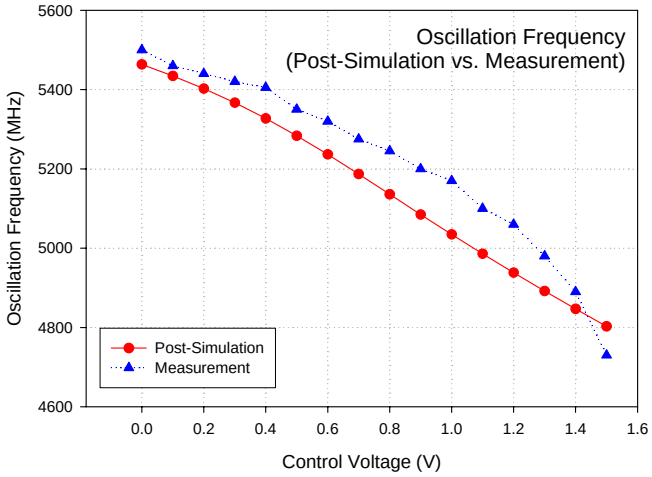


Fig. 4-13 Tuning curve of the low-power VCO (On wafer)

Next we made a comparison test in lab. We adopt testing PCB and bond wire from IC output pads. Fig. 4-14 shows measured spectrum of the VCO for a center frequency of 5.545-GHz. A tuning range of 1040-MHz (4.50 ~ 5.54-GHz, about 19.4 %) is measured for control voltage variation from 0 to 1.5V. The measured tuning characteristic of the VCO is shown in Fig. 4-15. Phase noise performance of the VCO has been measured using HP 8563E spectrum analyzer with phase noise measurement utility. Phase noise @ 1-MHz offset form the carrier is -103dBc/Hz, as shown in Fig. 4-16. This result is even better than data obtained in CIC. The difference above may be caused by the purity of power supply.

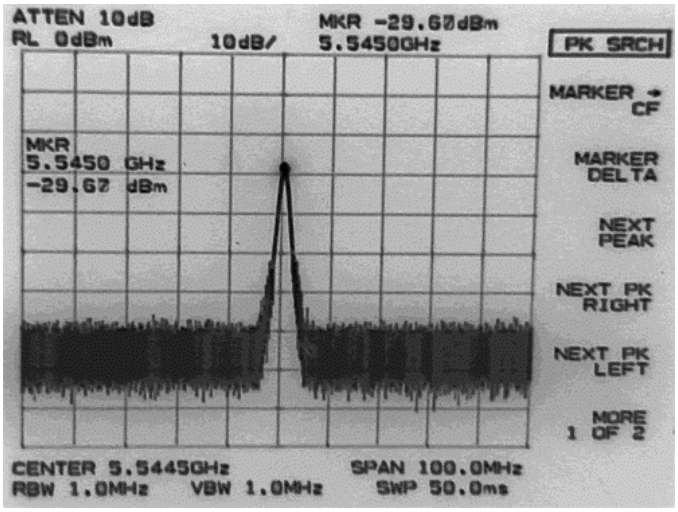


Fig. 4-14 Measured output spectrum of VCO (Bond-wire)

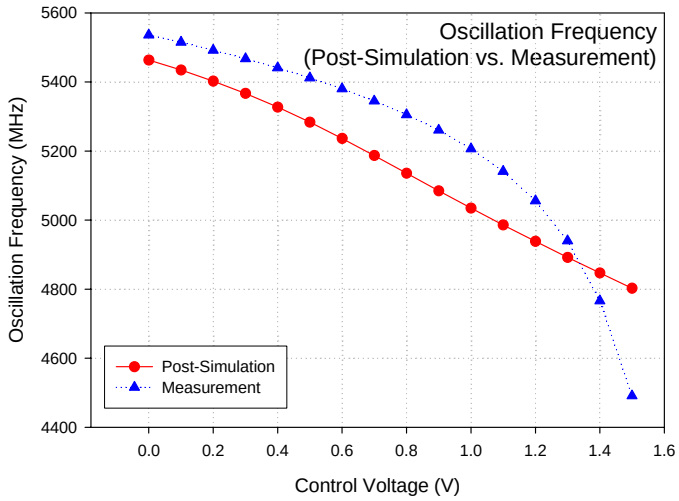


Fig. 4-15 Tuning curve of the low-power VCO (Bond-wire)

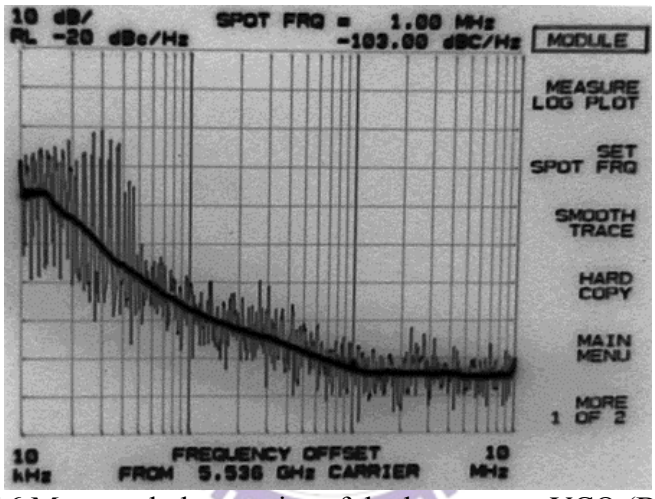


Fig. 4-16 Measured phase noise of the low-power VCO (Bond-wire)

We made another comparison test in lab. Also, we adopt testing PCB and bond wire from IC output pads. Add the DC-blocking capacitor between buffer output and SMA, as showing in Fig. 4-17. Also, we add the De-coupling capacitor between power line and ground line. Digital or analog power supply is noisy power source, so we add the 100nF and 100pF capacitor as near the pad of chip as possible to suppress the noise coming from power supply. Fig. 4-18 shows the PCB testing board of the chip. The chip is stuck on testing PCB, and wires bonded from the pad on chip to feed the bias voltages.

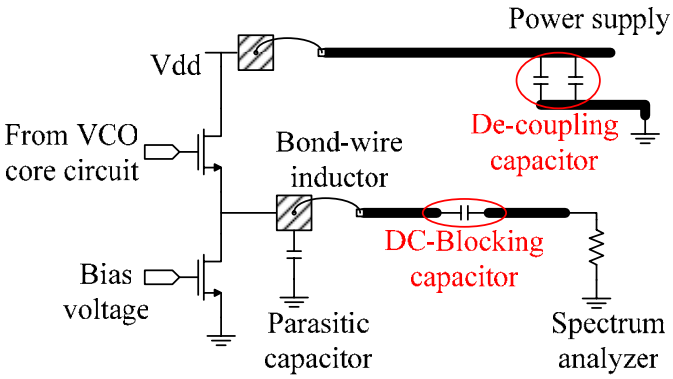


Fig. 4-17 Measured consideration (Adding a DC-blocking capacitor and De-coupling capacitor)

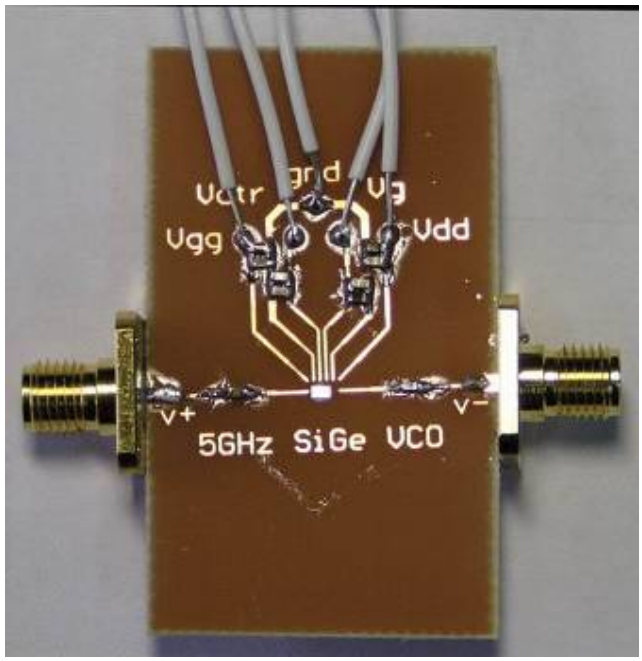


Fig. 4-18 Testing board of the low-power VCO

Fig. 4-19 shows measured spectrum of the VCO for a center frequency of 5.430-GHz after adding the DC-blocking capacitor and de-coupling capacitors. A tuning range of 1120-MHz (4.310 ~ 5.430-GHz, about 21.5 %) is measured for control voltage variation from 0 to 1.5V. The measured tuning characteristic of the VCO is shown in Fig. 4-20. Phase noise @ 1-MHz offset form the carrier is -109dBc/Hz, as shown in Fig. 4-21. The output power level is shown in Fig. 4-22. We can detect that the output power of measurement is close to simulation result. We can find that it is less influence on loading effect after adding DC-blocking capacitor. In conclusion, this result is better than the former data without DC-blocking capacitor

and de-coupling capacitor. The difference above may be caused by the loading effect of intrinsic resistor in the spectrum analyzer and the noise from power source.

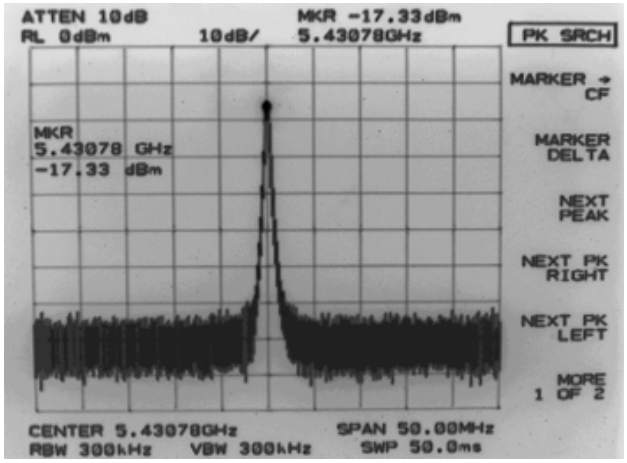


Fig. 4-19 Measured output spectrum of the low-power VCO
(With DC-block and de-coupling capacitor)

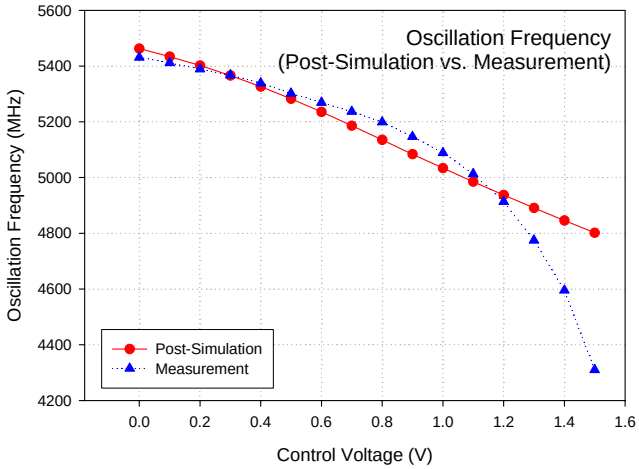
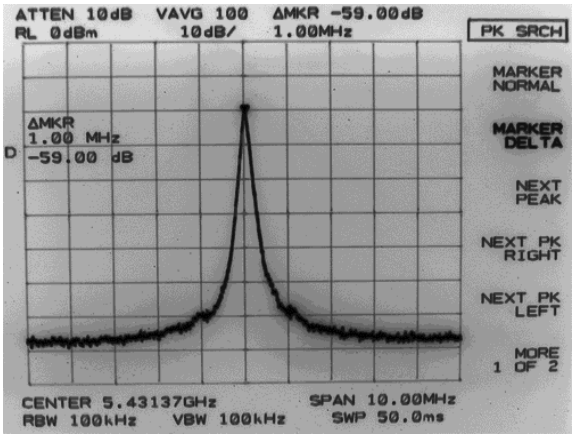


Fig. 4-20 Tuning curve of the low-power VCO
(With DC-block and de-coupling capacitor)



$$-59.0dB - 10\log(100 \cdot 10^3)$$
$$= -109dBc/Hz$$
@ 1MHz offset

Fig. 4-21 Measured phase noise of VCO
(With DC-block and de-coupling capacitor)

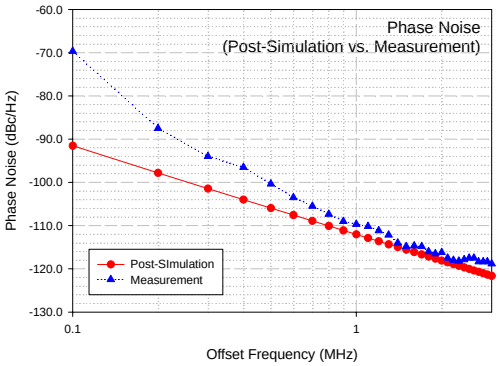


Fig. 4-22 Phase noise of the low-power VCO (With DC-block and de-coupling capacitor)

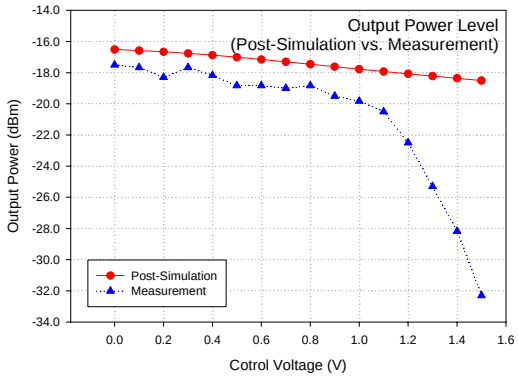
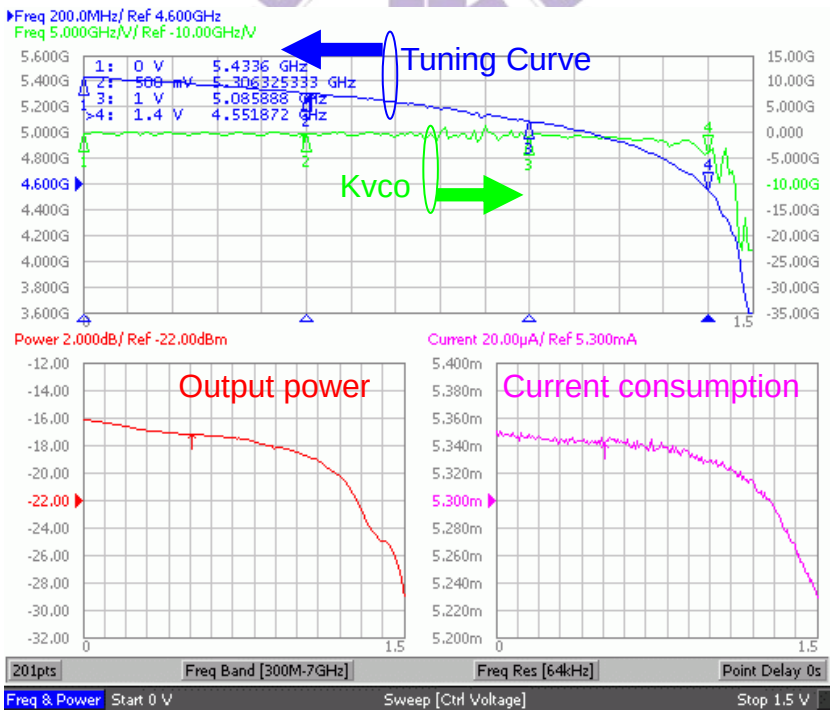
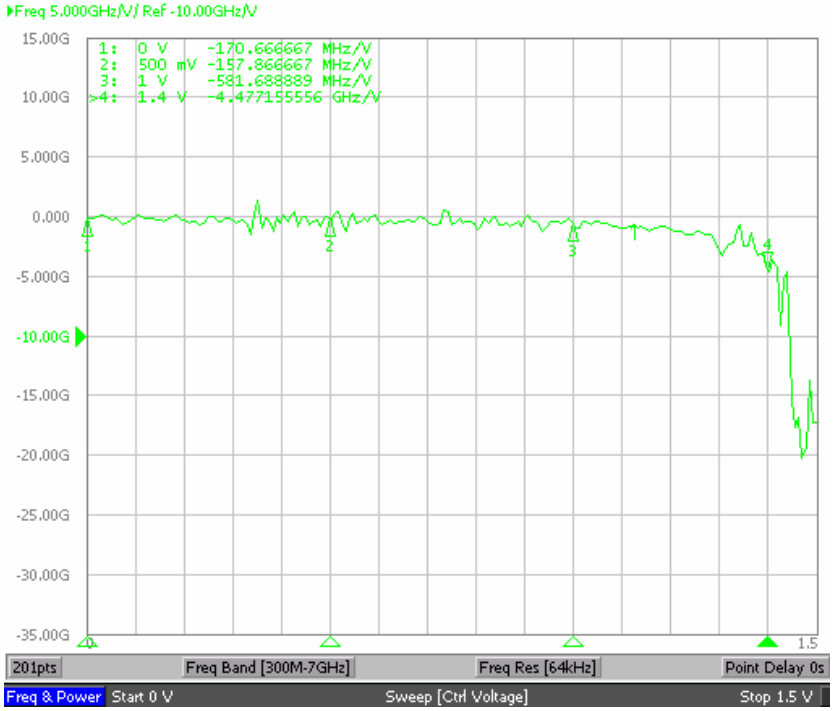


Fig. 4-23 Output power level of the low-power VCO (With DC-block and de-coupling capacitor)

To increase the accuracy of measurement, we made a comparison test in CIC using signal source analyzer. We use the signal source analyzer to measure SiGe VCO characteristic, as showing in Fig. 4-24.



(a)



(b)

Fig. 4-24 (a) Measured characteristic of VCO (b) Measured Kvco of VCO

Next we measure phase noise performance of VCO. The measured phase noise performance is almost the same as simulation result. Based on measurement result, the phase noise @ 1-MHz offset and @ 3-MHz offset form the carrier is -114.1dBc/Hz and -125.0dBc/Hz, respectively (Fig. 4-25).

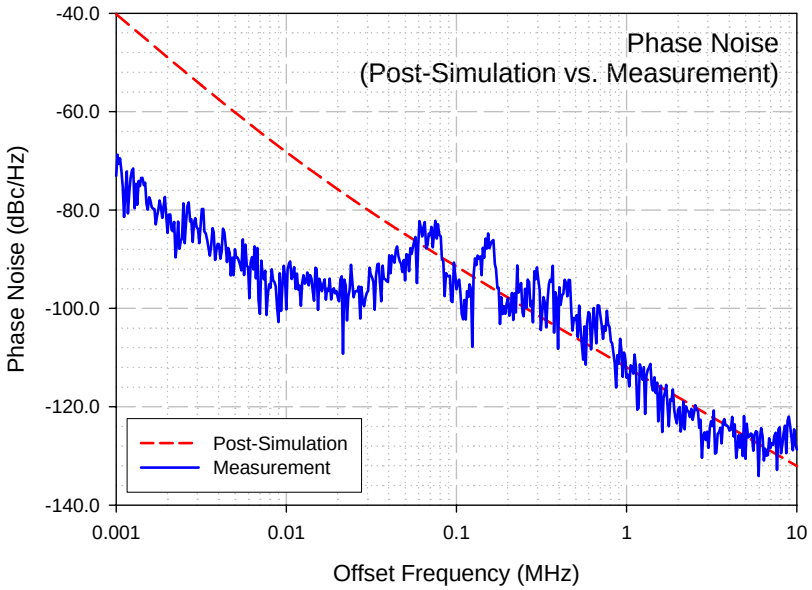


Fig. 4-25 Measured phase noise of VCO

4.1.4 Measurement discussion

A voltage-controlled oscillator suited for IEEE 802.11a system is implemented. This circuit is simulated with Eldo RF for pre-simulation and with Calibre for post-simulation. The VCO is fabricated by 0.35μm 3P3M SiGe BiCMOS. Based on the measurement results, the tuning range is from 4.31-GHz to 5.43-GHz while the control voltage varies from 0 to 1.5 volts, about 1120-MHz (about 21.5 %); phase noise is -114dBc/Hz @ 1-MHz offset at 5.43-GHz when the control voltage is 0 volt. The circuit draws only 1mA current for the VCO core from a 3.3V supply. The VCO core consumes only 3.3mW.

Table 4-2 summarizes the simulation and measurement results. Expect the noise performance is worse 3dB than simulation result, others performance is almost the same as the original design.

Table 4-2 Simulation and measurement performance summary

Specification	**Post-simulation (PEX-C)**	**Measurement**
Power supply	3.3V	
VCO core circuit power	3.59mW	3.3mW
Total power consumption	17.86mW	16.7mW
Tuning range	4.80 ~ 5.46GHz	4.31 ~ 5.43GHz
Phase noise	-92dBc/Hz @100kHz -112dBc/Hz @1MHz -122dBc/Hz @3MHz	-96.1dBc/Hz @100kHz -114.1dBc/Hz @1MHz -125.0dBc/Hz @3MHz
Output power	-16.51dBm	-17.33dBm

4.2 A 2.4-GHz low power, low phase-noise, quadrature output back-gate CMOS VCO

4.2.1 Design Consideration

This chip is fabricated in October 2004. The phase noise of the VCO determines the out-of-band noise of the frequency synthesizer. For the OFDM modulation in WLAN and Bluetooth system applications, the excellent phase-noise performance of VCO is required. A new quadrature VCO is proposed with the NMOS back-gate as coupling transistors [21]. So we design this low phase noise 2.4-GHz quadrature VCO by 0.18-μm 1P6M triple-well CMOS technology.

In this design, LC-tank structure is used for a low-power, low phase-noise oscillator design. The purpose output frequency of VCO is from 2400-MHz to 2483-MHz. The VCO core is based on conventional cross-coupled negative-Gm topology, which contains a LC-resonator with cross-coupled pairs of NMOS / PMOS transistors as active part. The LC-resonator is implemented as an on chip symmetric spiral inductor, MOS varactors and MIM capacitances. The MOS varactor has the higher quality factor and is adopted in the VCO to reduce the phase noise.

There are many ways to generate quadrature signals. The two VCOs which cross-connect to each other is conventional way and generally used in many designs. However, this architecture suffered from more noise than the others architecture. Fig. 4-26 shows the conventional LC-QVCO topology. In addition, eight transistors used for cross-connect with each other contribute additional noise to the LC tank and the

variation of the transconductance of the coupling transistors by 1/f noise degrades the phase noise. In the aspects of phase noise and power consumption, the presence of the additional coupling transistors makes it inherently inferior to the topology proposed in [21].

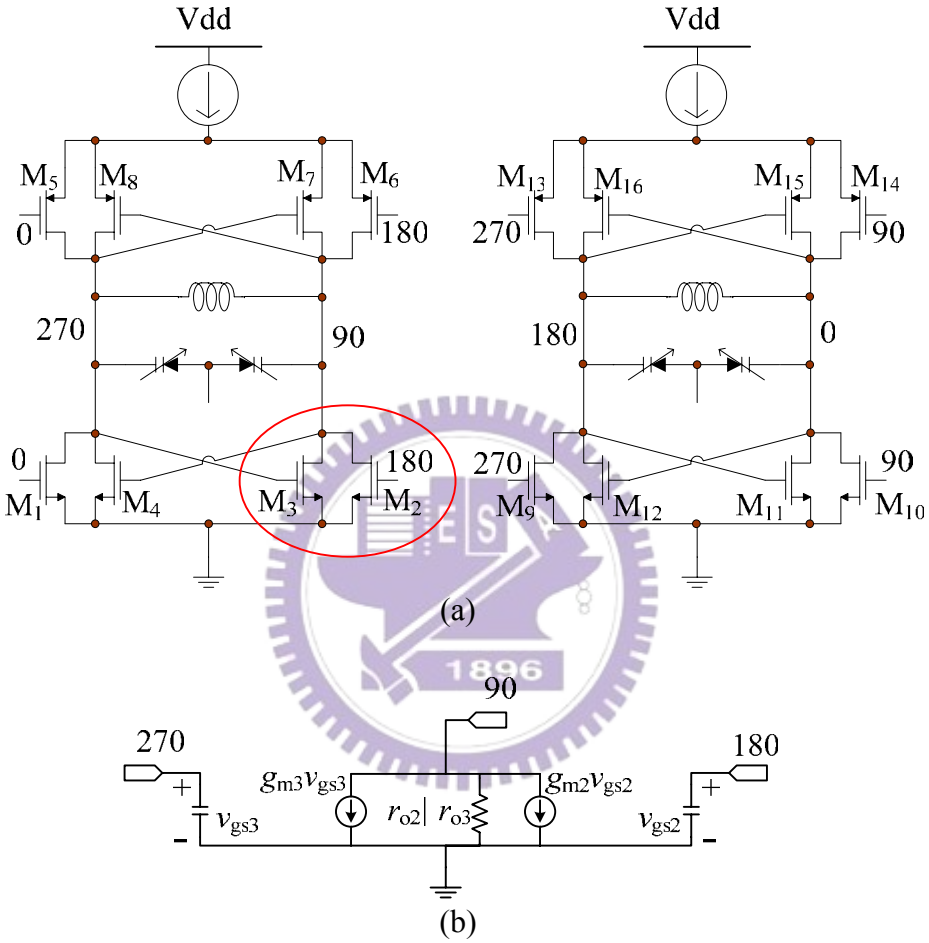


Fig. 4-26(a) Architecture of conventional quadrature VCO
(b) Small-signal equivalent circuit of the circled part

Fig. 4-27 shows the new QVCO topology. This VCO does not require additional coupling transistors. We use the substrate of NMOS to couple the signals between the two differential VCOs, instead of the transistors. The coupling signal is applied to the substrate of the core NMOS transistors. Fig. 4-28 compares the phase noise performance of the conventional and back-gate coupled LC-QVCO as well as the differential VCO [21]. It shows that the back-gate QVCO has better phase noise performance than others.

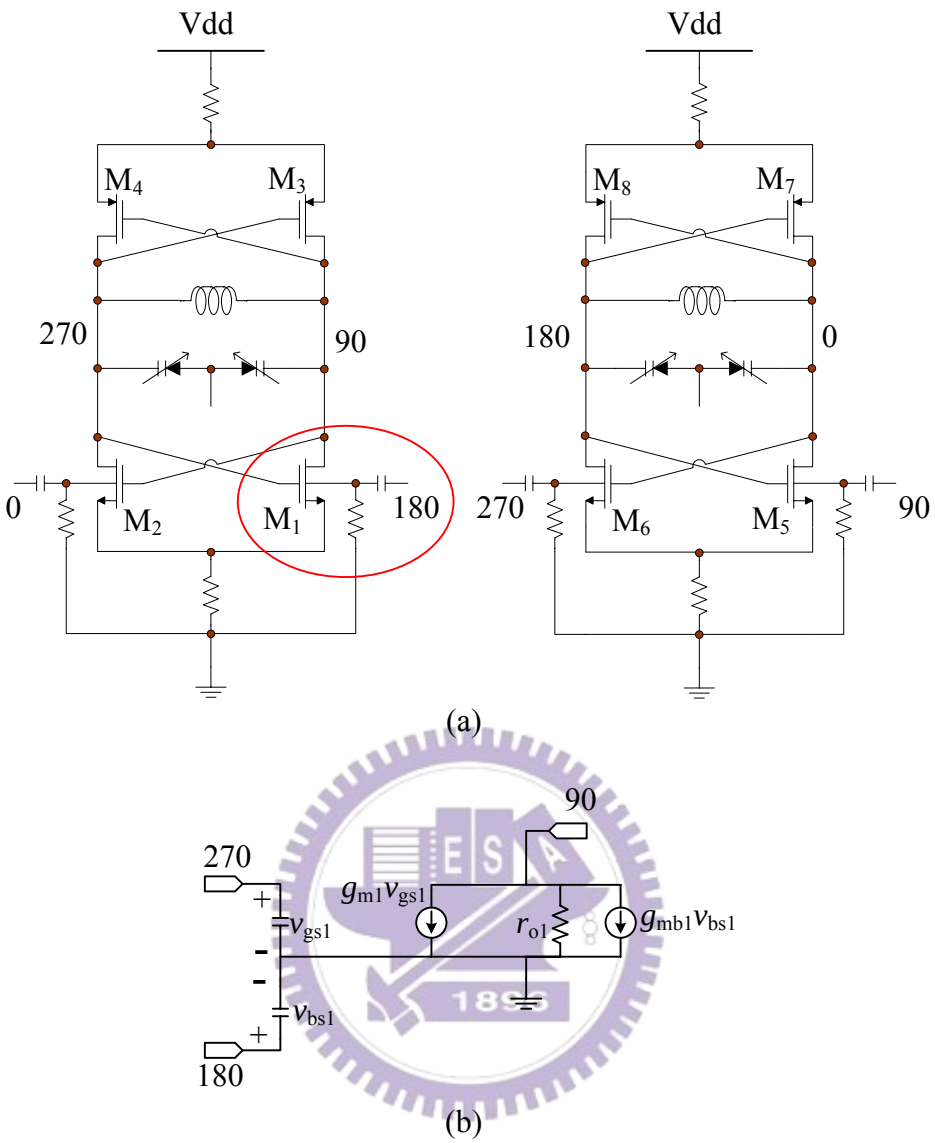


Fig. 4-27 (a) Architecture of the fabricated back-gate coupled LC-QVCO
(b) Small-signal equivalent circuit of the circled part

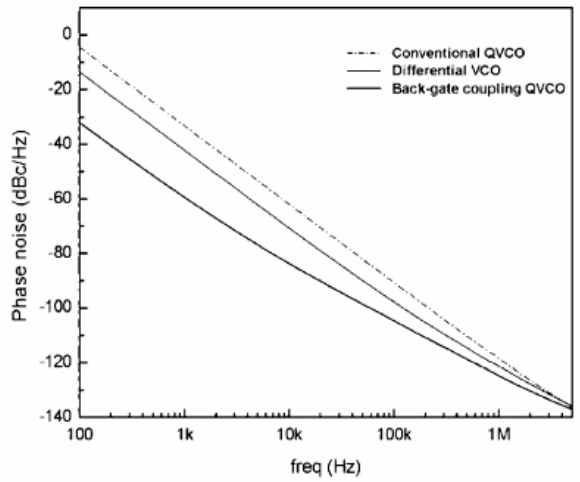


Fig. 4-28 Phase noise comparison of conventional QVCO, differential VCO, and back-gate coupling QVCO

The same as circuit architecture in former chapter, the 3 bit capacitor bank circuits are used in this design. The whole circuit schematic is showing in Fig. 4.29. The symmetric inductor is used to enhance the quality factor of LC-tank. We adopt the inductor with radius=47μm, with=9μm, number of turns=3, and spacing=2μm (Fig. 4-30). The total inductance of this inductor is about 1.72nH. Use the MOS varactor (Blanch=25 and Group=4, as showing in Fig. 4-31). So the oscillation frequency of this VCO can oscillate at 2.4-GHz.

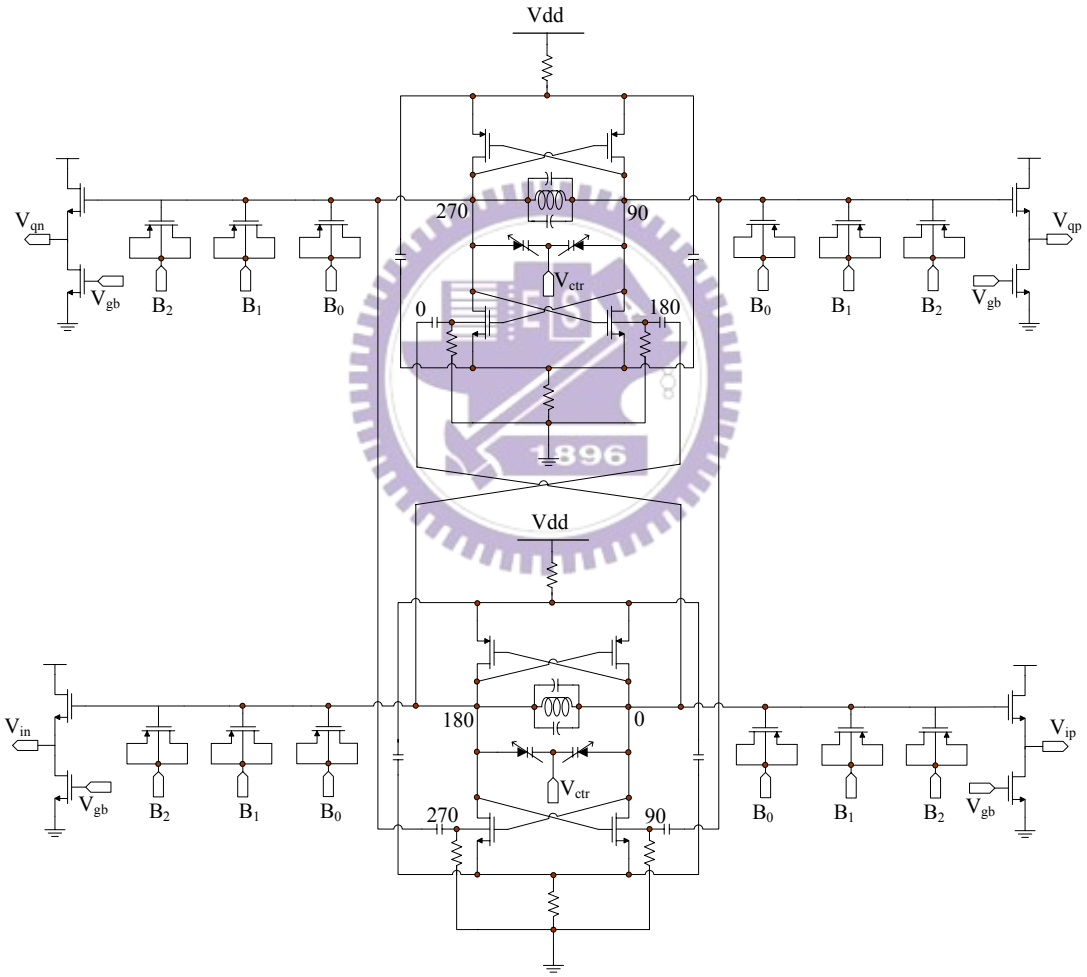
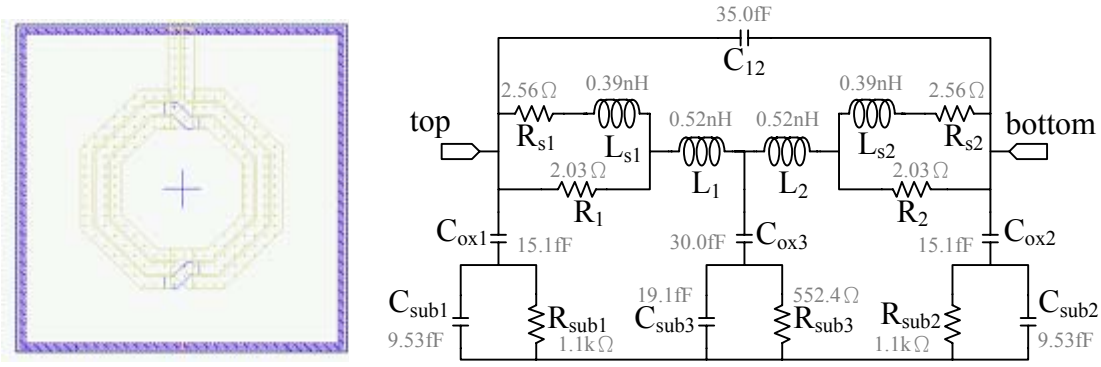
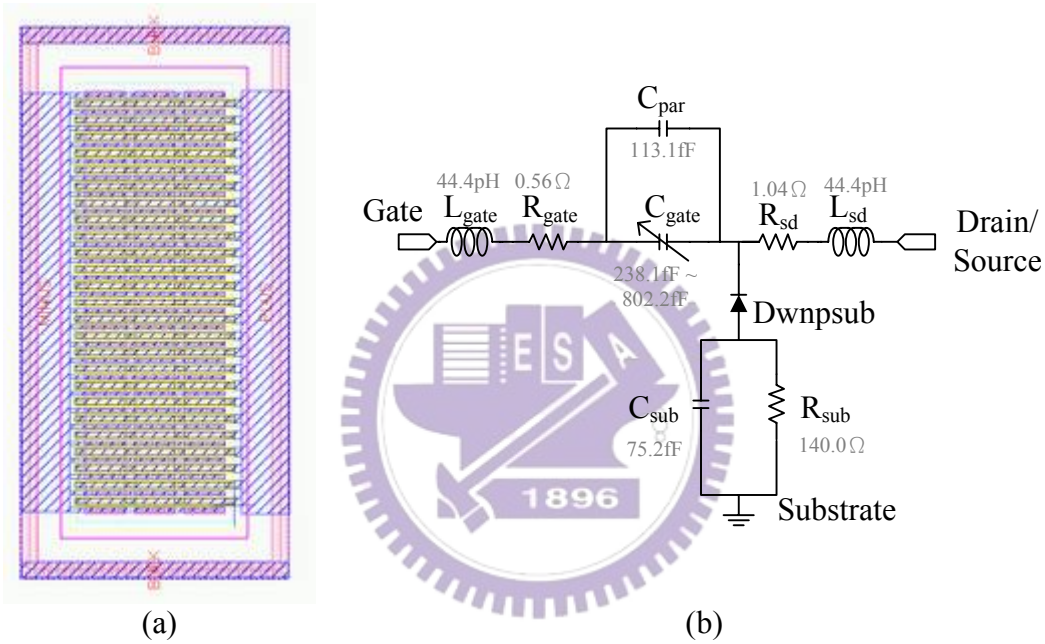


Fig. 4-29 Schematic of the back-gate coupling quadrature VCO



(a) (b)

Fig. 4-30 Spiral inductor in this QVCO (a) layout (b) equivalent circuit model



(a) (b)

Fig. 4-31 MOS varactor in this QVCO (a) layout (b) equivalent circuit model

4.2.2 Simulation results and layout

This design of quadrature VCO is implemented using 0.18-μm 1P6M triple-well CMOS process. After Eldo RF simulation, it shows that the oscillator is tunable between 2.40 and 2.53 GHz (130MHz tuning range) at bank 10. Fig. 4-32 shows the tuning range of VCO for bank 000, 001… and 111. The output swing of VCO is shown in Fig. 4-33.

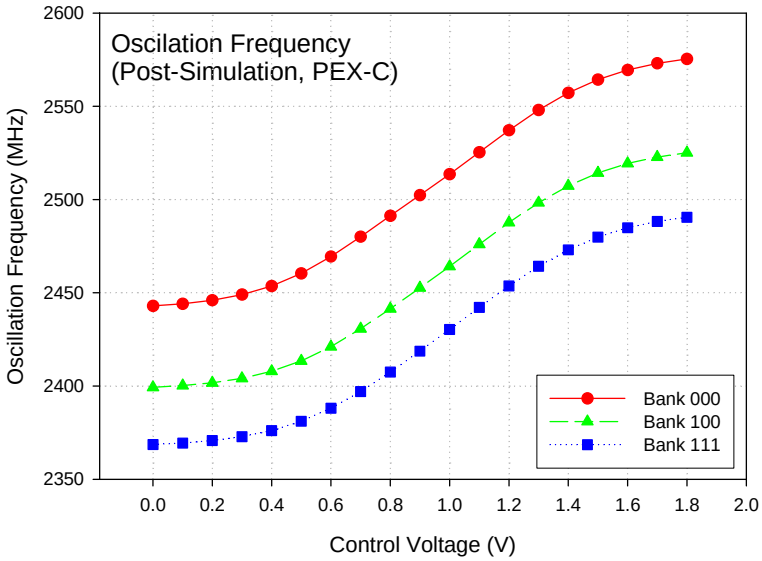


Fig. 4-32 Tuning curve of the back-gate coupling quadrature VCO

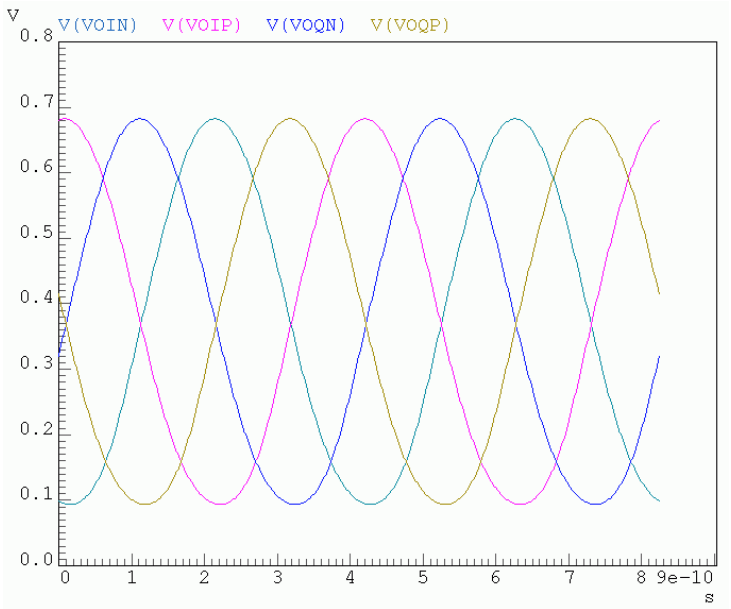


Fig. 4-33 Output waveform of the back-gate coupling quadrature VCO

The most critical part in the design of a low-phase noise VCO is the inductor of the resonance LC-tank. The simulated phase noise is -122.45dBc/Hz @ 1MHz offset and -130.89dBc/Hz @ 3MHz offset at 2.45 GHz, as showing in Fig. 4-34.

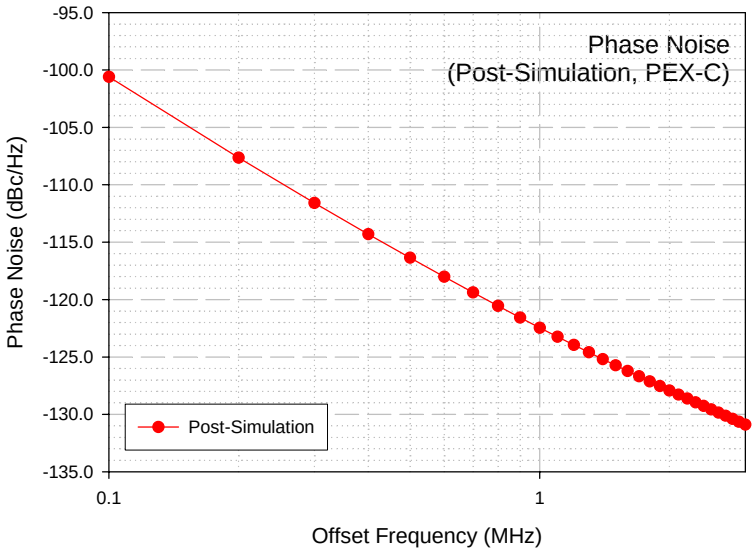


Fig. 4-34 Phase noise of the back-gate coupling quadrature VCO

The power consumption of two quadrature VCO cores is 8.2mW. The overall power consumption is 19.5mW with buffer output stages. Fig. 4-35 shows the whole circuit layout. The total chip size including pads is about 1400umX900um.

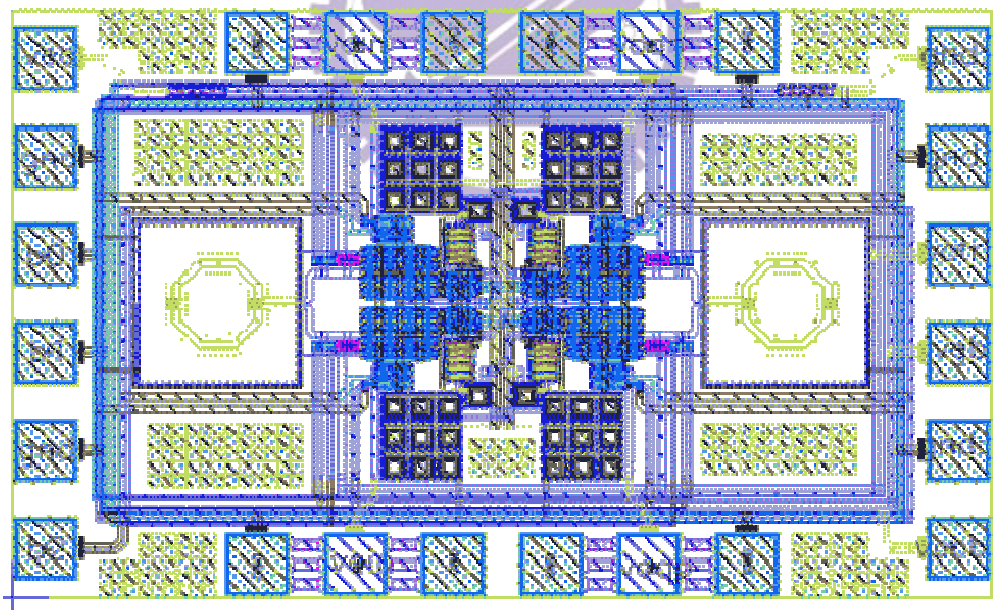


Fig. 4-35 Layout of the back-gate coupling quadrature VCO

Table 4-3 Summary of corner case performance

Post-simulation (PEX-C)	**TT corner**	**FF corner**	**SS corner**
Power supply	1.8 V		
Oscillator frequency @Vctr=0.9V	2.45GHz	2.46GHz	2.42GHz
VCO bank condition	(B2 B1 B0)=100		
VCO tuning range	2.40 ~ 2.53GHz 130MHz (5.31%)	2.41 ~ 2.54GHz 130MHz (5.31%)	2.37 ~ 2.49GHz 120MHz (4.90%)
Phase noise (dBc/Hz)	-122.5 @1MHz -130.9 @3MHz	-116.1 @1MHz -127.2 @3MHz	-104.5 @1MHz -114.8 @3MHz
VCO output swing ($V_{peak\ to\ peak}$)	590mV	780mV	350mV
Power consumption	Two core circuits: 8.2mW Four buffer stages: 11.3mW	Two core circuits: 12.9mW Four buffer stages: 14.6mW	Two core circuits: 5.7mW Four buffer stages: 8.6mW
Total power consumption	19.5mW	27.4mW	14.3mW

4.2.3 Measurement results

The measurement arrangement for our design of back-gate QVCO is shown in Fig. 4-36. Fig. 4-37 shows the die-photograph of QVCO. We applied for CIC on wafer RF GSG (Ground-Signal-Ground) probe measurement. The measurement is performed by a probe station, spectrum analyzer (HP8563E, frequency range: 9-kHz ~ 26.5-GHz), and RF GSG probe. Here we also add a dc blocking capacitor between VCO output node and spectrum analyzer. The total power consumption is 19.8mW. Fig. 4-38 shows measured spectrum of QVCO for a center frequency of 2.093-GHz. In the Fig. 4-39, a tuning range is 2.093 ~ 2.206-GHz (about 5.4%) for control voltage variation from 0 to 1.8V at bank 100.

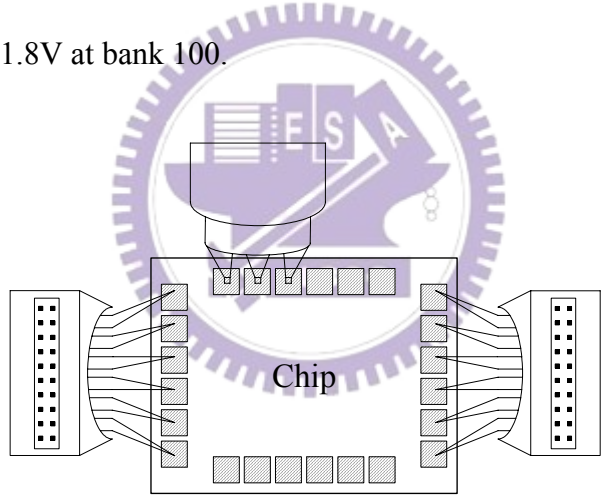


Fig. 4-36 The measured consideration

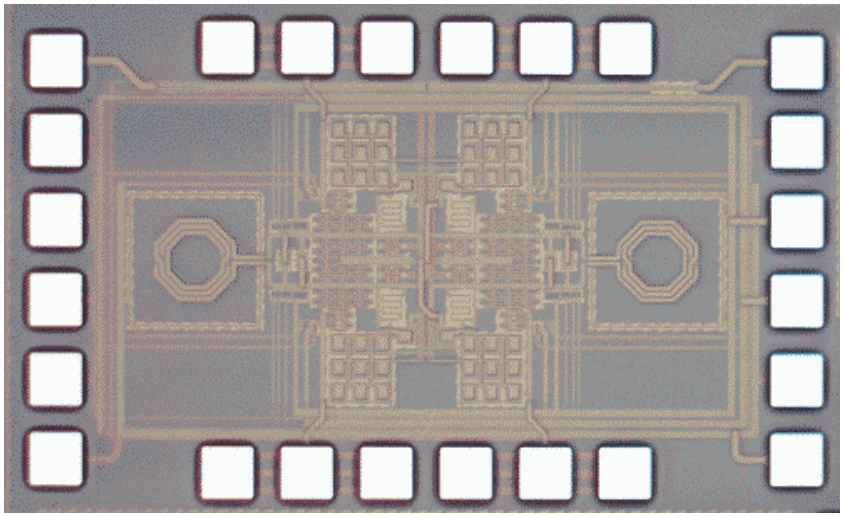


Fig. 4-37 Die-photograph of the back-gate coupling quadrature VCO

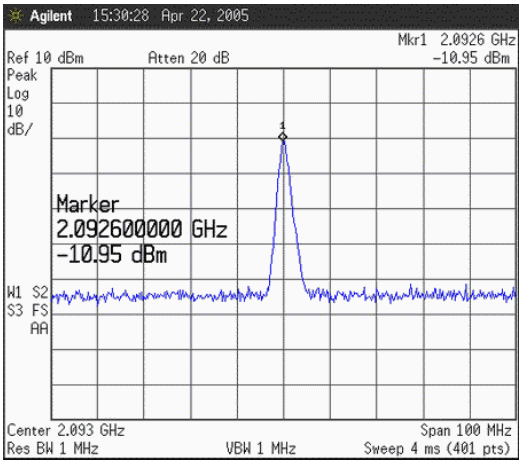


Fig. 4-38 Measured output spectrum of the back-gate coupling quadrature VCO (On wafer)

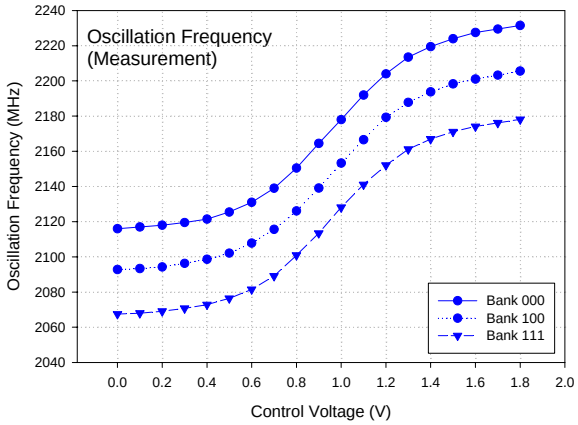


Fig. 4-39 Tuning curve of the back-gate coupling quadrature VCO

The measured oscillation frequency is different from simulation result. Next we adopt testing PCB and bond wire from IC output pads with de-coupling capacitors added between power lines and ground lines. Hence we made a comparison test in lab. The test PCB is showing in Fig. 4-40. The tuning range is almost the same as measurement at CIC. Fig. 4-41 is the output spectrum with bond-wire measurement. It shows that the output level is -11.50dBm.

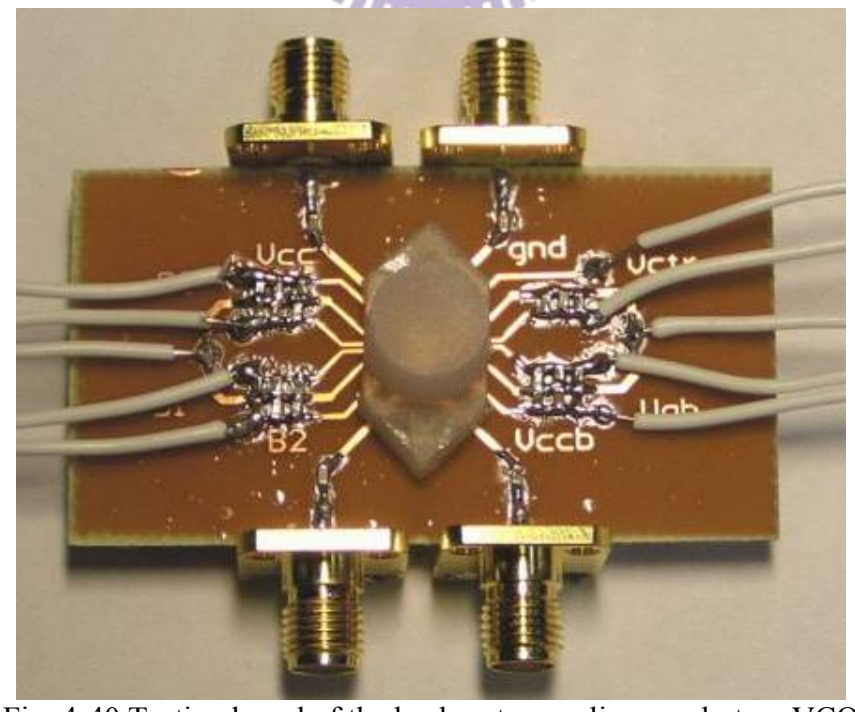


Fig. 4-40 Testing board of the back-gate coupling quadrature VCO

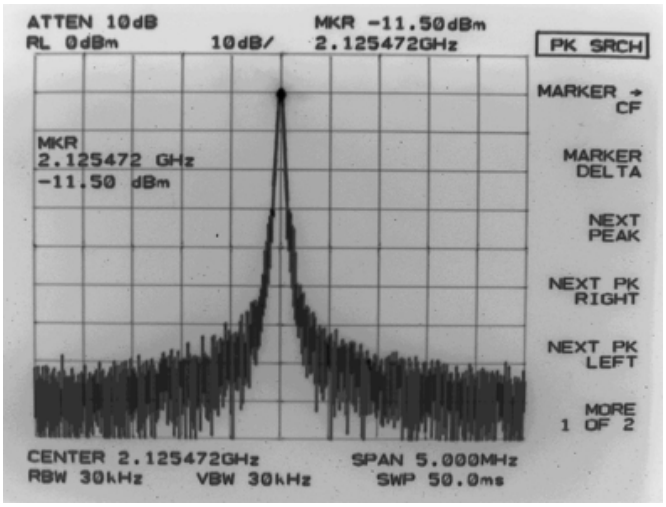


Fig. 4-41 Measured output spectrum of the back-gate coupling quadrature VCO

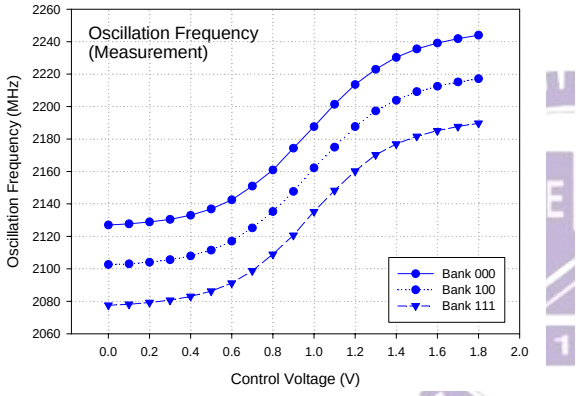


Fig. 4-42 Measured tuning curve of the back-gate coupling quadrature VCO

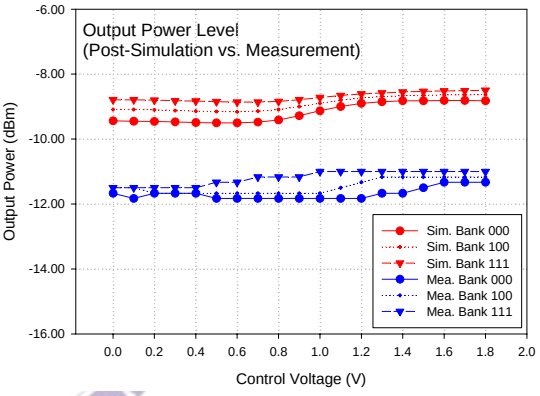
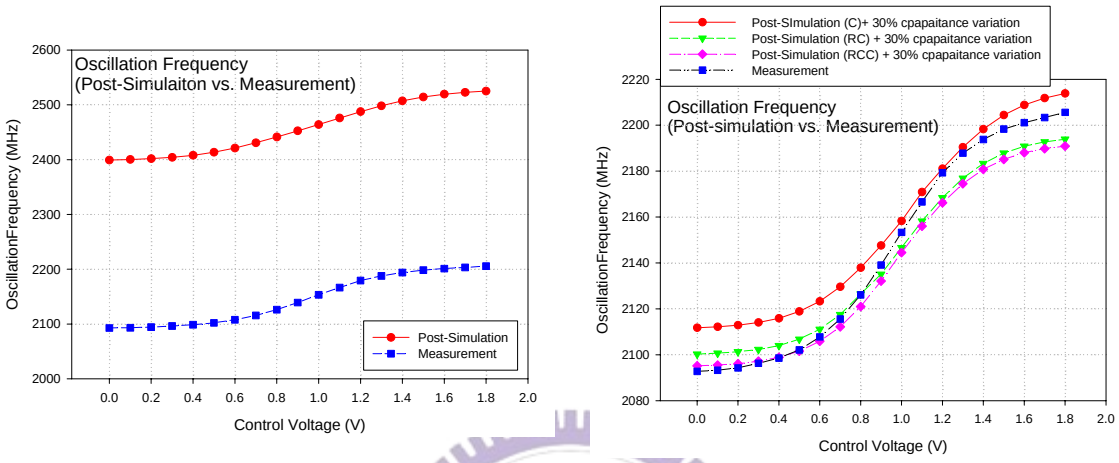


Fig. 4-43 Output power level of the back-gate coupling quadrature VCO

The measured oscillation frequency is 2.1GHz and the simulated oscillation frequency is 2.4GHz when control voltage is 0V. It may due to the capacitor bank which we use for fine frequency control. It is short channel device model such that the parasitic of larger device doesn't well control. This parasitic effect is not extracted exactly from post-simulation tool although the present software is stronger and stronger. Besides, the inductance of spiral inductor may vary from model specification. Based on oscillation theorem,

$$2\pi f = \frac{1}{\sqrt{LC_{total}}} \tag{4-4}$$

Hence, the product of inductance and capacitance is 30% variation. We re-simulate the oscillation frequency if the capacitance of varied 30%. After re-simulating the tuning range with 30% capacitance variation, we can get better fit of the measurement data with simulation results as showing in Fig. 4-44b.



(a) (b)

Fig. 4-44 (a) Measured tuning curve compared with simulation (Bank 100)
(b) Measured tuning curve compared with re-simulation (Bank 100)

Phase noise performance of the VCO has been measured using HP 8563E spectrum analyzer. Phase noise is -119.27dBc/Hz @ 1-MHz offset and -125.60dBc/Hz @ 3-MHz offset, as shown in Fig. 4-46. This result is much better than data obtained in CIC. The difference above may be caused by the purity of power supply. The power source is much purer because there are de-coupling capacitors used in this test board.

To increase the accuracy of measurement, we made a comparison test in CIC using signal source analyzer. We use the signal source analyzer to measure QVCO characteristic, as showing in Fig. 4-47. Next we measure phase noise performance of QVCO. The measured phase noise performance is almost the same as simulation result. Based on measurement result, the phase noise @ 1-MHz offset and @ 3-MHz

offset form the carrier is about -124.3dBc/Hz and -133.9dBc/Hz, respectively (Fig. 4-48).

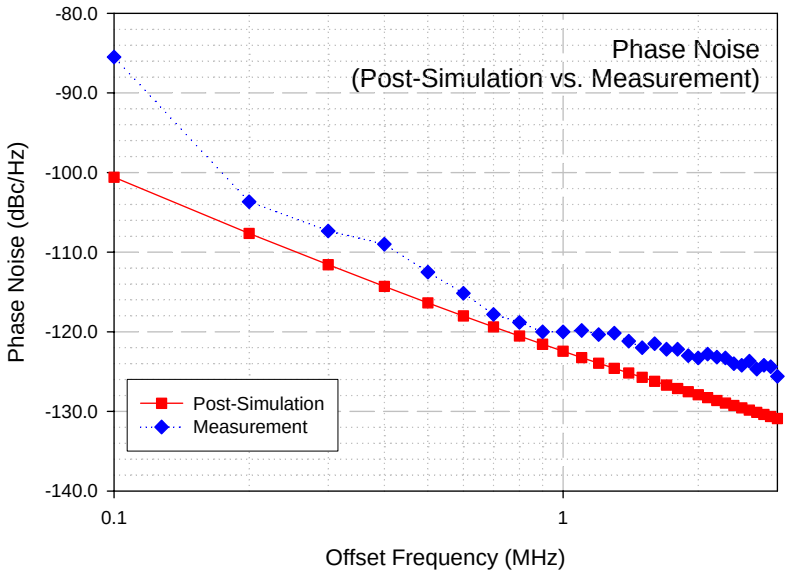
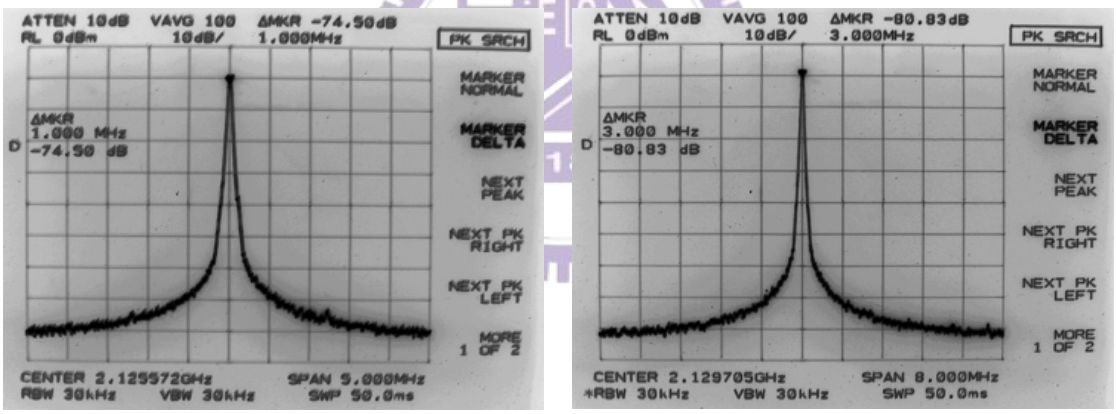


Fig. 4-45 Phase noise of the back-gate coupling quadrature VCO



$-74.50dB - 10\log(30 \cdot 10^3)$
$= -119.27dBc/Hz$
@ 1MHz offset
(a)

$-80.83dB - 10\log(30 \cdot 10^3)$
$= -125.60dBc/Hz$
@ 3MHz offset
(b)

Fig. 4-46 Measured the phase noise of the back-gate coupling quadrature VCO (Bond-wire) (a) at 1-MHz offset (b) at 3-MHz offset

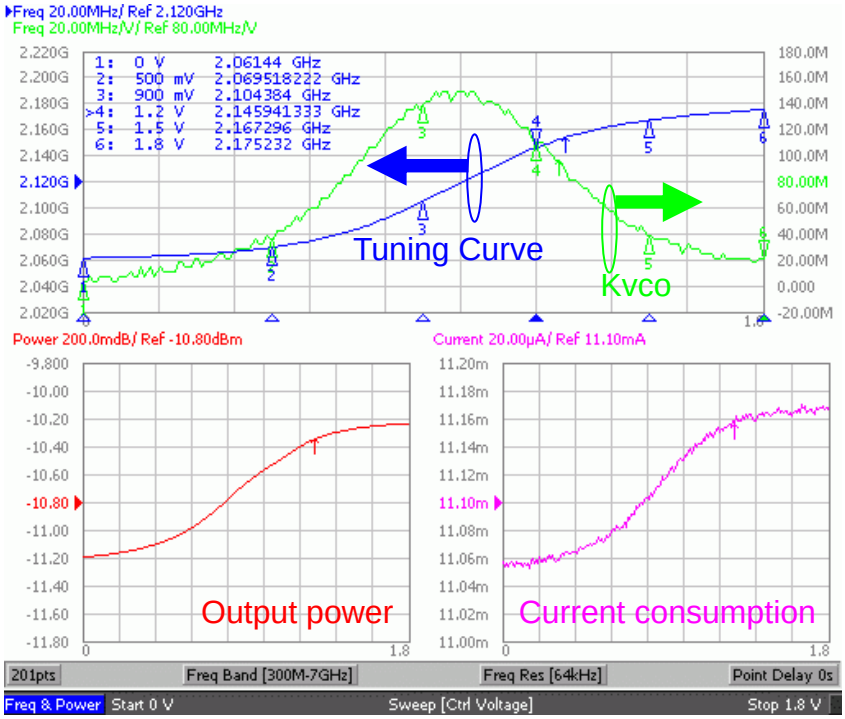


Fig. 4-47 Measured characteristic of the back-gate coupling quadrature VCO at bank 100

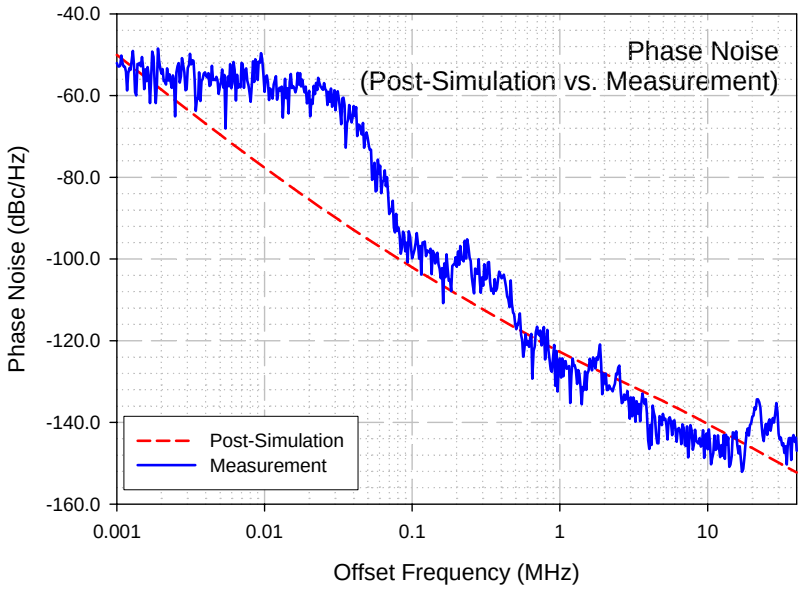


Fig. 4-48 Measured phase noise of the back-gate coupling quadrature VCO

4.2.4 Measurement discussion

A quadrature VCO suited for IEEE 802.11b/g application is implemented. This circuit is simulated with Eldo RF for pre-simulation and with Calibre for post-simulation. The VCO is fabricated by 0.18μm 1P6M triple-well CMOS technology. The simulation and measurement results of power consumption are very close, and all parts work successfully. Based on measurement results, the phase noise is close to simulation results. But the measured oscillation frequency is different from simulated results. The tuning range is about 300-MHz difference between simulation results and measurement results. The difference means the extra parasitic effects are imperfectly evaluated during our simulation. It may due to the capacitor bank used in this quadrature VCO. The same as the architecture in former chapter, we use the PMOS as a varactor by connecting the source, drain, and body node together. The capacitance may be not the same as simulation. It may be larger than model specification. After re-simulating the tuning range with 30% capacitance variation, we can get better fit of the measurement data with simulation results. Table 4-4 summarizes the simulation and measurement results.

Table 4-4 Simulation and measurement performance summary

Specification	**Post-simulation (PEX-C)**	**Measurement**
Power supply	1.8V	
Capacitor bank	(B2, B1, B0)=(1, 0, 0)	
VCO core circuit power consumption	8.2mW	9.0mW
Total power consumption	19.5mW	19.8mW
Tuning range	2.399 ~ 2.525GHz	2.093 ~ 2.206GHz
Phase noise	-100.59dBc/Hz @100kHz -118.01dBc/Hz @600kHz -122.45dBc/Hz @1MHz -130.89dBc/Hz @3MHz	-99.9dBc/Hz @100kHz -120.2dBc/Hz @600kHz -124.3dBc/Hz @1MHz -133.9dBc/Hz @3MHz
Output power	-9.0dBm	-10.95dBm (On wafer) -11.50dBm (Bond-wire)

Chapter 5

Conclusions and Future Works

5.1 Conclusions

A fully integrated 2.4-GHz fractional-N frequency synthesizer is demonstrated. The third order sigma-delta modulation circuit is adopted for high degree noise-shaping. Fully programmable multi-modulus divider architecture cans achieve both high-speed frequency division and moderate power consumption. The whole circuit power consumption including output buffer stages is only 22.9mW. Based on measurement results, the measured tuning range and phase noise is close to simulated results. The settling time is no more than 30μs. But the fractional spurious tone is worse than we expect.

We also introduce two 2.4-GHz integer-N frequency synthesizers, one of them is proposed for wide tuning rage and the other is for low power and low phase-noise. In wide tuning range frequency synthesizer, the tuning range is approach 27.6% of center frequency with overall bank conditions (code-000 to 111) and locking time is less than 40μs. In the low power, low phase noise frequency synthesizer, the phase noise is -114.0dBc/Hz@1-MHz offset and the power consumption is only 28.3mW. The locking time is less than 90μs and spurious tone is -41.50dBc @1-MHz reference frequency. Comparing the measurement results with others, the phase noise, the

settling time and the power consumption are acceptable. However, these designs still suffered from strong spurious problems. The performance summaries are showing in Table 5-1.

Table 5-1 Measurement data compared to spec requirement

Performance	Sigma-delta fractional-N synthesizer	Wide tuning-range integer-N synthesizer [10]	Low power, low phase-noise integer-N synthesizer	Spec. of Bluetooth	Spec. of WLAN
Power supply	1.8V			No specific	
Tuning range of VCO / %	2.34 ~2.65GHz 12.9% (bank 00 ~11)	2.12 ~2.79GHz 27.6% (bank 000 ~111)	2.37 ~2.69GHz 12.8% (bank 00 ~11)	2.402 ~2.480 GHz	2.400 ~2.4835 GHz
Reference frequency	16MHz	1MHz	1MHz	No specific	
Channel spacing	125kHz	1MHz	1MHz	1MHz	20MHz
Phase noise (dBc/Hz)	-118.4 @1MHz	-108.8 @1MHz	-114.0 @1MHz	<-80 @1MHz <-120 @3MHz	<-110 @1MHz
Spurious tones (dBc)	-56.5 @ 3.125MHz	-26.15 @ 1MHz	-41.5 @ 1MHz	-24 @ 1MHz	N.A.
Locking time	30μs	40μs	90μs	<200μs	<200μs
Power consumption	22.9mW	38.4mW	28.3mW	As low as possible	

Besides, two voltage-controlled oscillators suited for WLAN systems are implemented. One is 5.25-GHz low-power SiGe VCO and the other is 2.4-GHz low phase-noise CMOS QVCO. The local oscillator circuits used in radio frequency (RF) systems such as wireless (local area networks) LANs and Bluetooth system must have sufficient tuning ranges and good phase noise characteristics. In order to extend the tuning range of VCO, enlarge the varactor gain must be used. Based on measurement results, the circuit in the 5.25-GHz low-power SiGe VCO has 21.5 % tunable frequency range and draws only 1mA current for the VCO core from a 3.3V supply.

On the other hand, traditional quadrature VCO used additional transistors coupling between two core circuits, so the 1/f come from coupling transistors results in worse phase noise. The new quadrature VCO architecture is presented by using back-gate (body) node of transistor which connected with a capacitor as coupling circuit. Fortunately, the triple-well technique makes this idea practicable. The measured phase noise of the latter is -124.3dBc/Hz @ 1-MHz offset. The phase noise performance is quite excellent. But the oscillation frequency is 300-MHz difference between simulation and measurement results. After re-simulating the tuning range with 30% capacitance variation, we can get better fit of the measurement data with simulation results.

5.2 Future works

In the design of frequency synthesizer, there are several directions for future. First, the spurious tones are still strong and seriously influence the signal performance. We should re-design the charge pump and loop filter for lower glitches and acceptable settling time. The charging and discharging of charge pump should be more symmetrical while synthesizer is in locking state. Otherwise, we can choose higher order of the loop filter and reducing the loop bandwidth for larger spurious rejecting ability. Second, the power consumption should be reduced for lower power applications. In the first two stages of multi-modulus divider, we adopt the SCL type divider which has lager power consumption but more accuracy. We can choose the TSPC type for much lower power applications. We can also reduce the supply voltage to increase its competitiveness. Third, although the sigma-delta fractional-N type of synthesizer is implemented, the performance of synthesizer which we design, especially on phase noise performance during loop, is locked is not much better than

the commercial products for communication applications. We can add the band-gap reference for each bias voltage in our circuits. The band-gap reference voltage has lower noise component than voltage from off-chip supply voltage. It not only improves our circuit performance but also reduces the pads requirement. Besides, the frequency synthesizer with spurs compensation technique is presented in [8]. We can realize the spurs free frequency synthesizer by adding digital-to-analog circuit, as showing in Fig. 5-1. However, this circuit architecture becomes more complicated to design. This is a challenge to achieve this best architecture in recent works of frequency synthesizer.

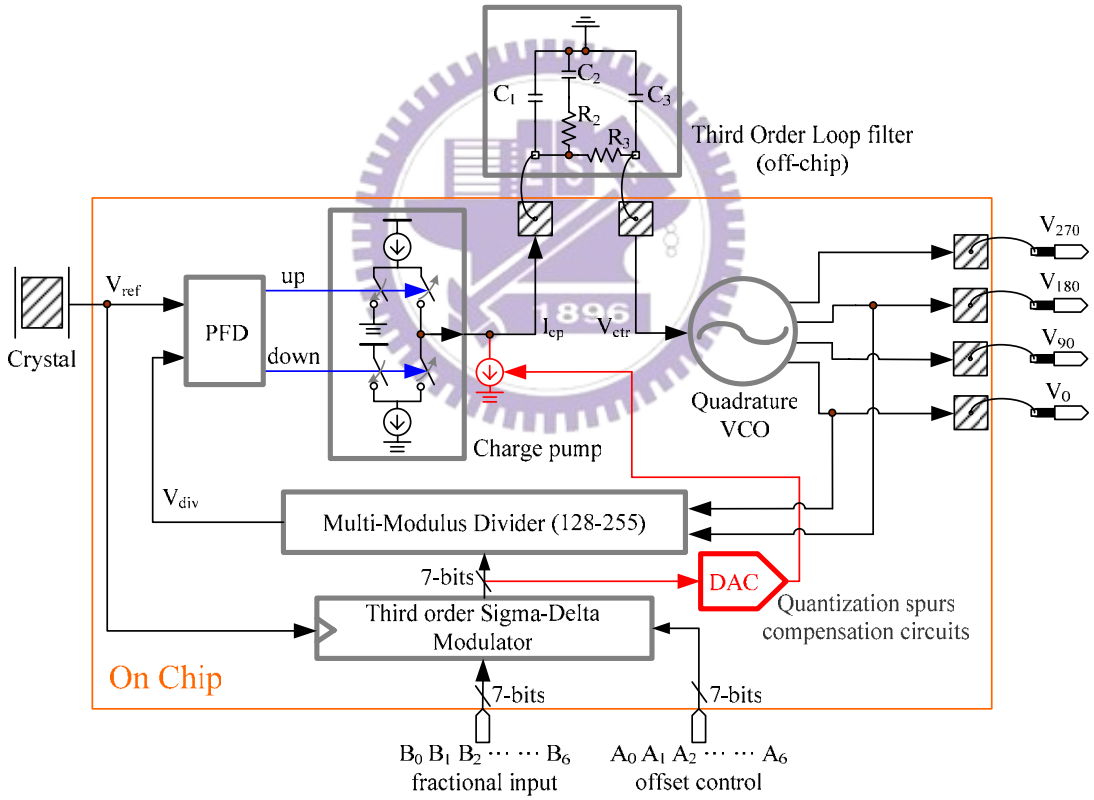


Fig. 5-1 Building blocks of sigma-delta fractional-N frequency synthesizer with spurs compensation technique

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Publication Remarks

International conference papers:

1. Christina F. Jou, Kuo-Hua Cheng, **Wei-Cheng Lien**, Chun-Hsien Wu, and Chin-Hsien Yen, “A 2.45 GHz / 5.25 GHz Concurrent Dual-Band Receiver Front-End Using 0.18um CMOS,” *IEEE Transaction on Microwave Theory and Techniques Mini-Special Issue on: Papers of Asia-Pacific Microwave Conference (APMC 2004)*, New Delhi, India, December, 15-18, 2004.

2. Christina F. Jou, Kuo-Hua Cheng, and **Wei-Cheng Lien**, “Design of a Low-Power and Wide Tuning Range SiGe VCO,” *IEEE Transaction on Microwave Theory and Techniques Mini-Special Issue on: Papers of Asia-Pacific Microwave Conference (APMC 2004)*, New Delhi, India, December, 15-18, 2004.