High-Performance Programmable AC Power Source with Low Harmonic Distortion Using DSP-Based Repetitive Control Technique

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***Abstract*— This paper proposes a new control scheme based on a two-layer control structure to improve both the transient and steady-state responses of a closed-loop regulated pulse-width-modulated (PWM) inverter for high-quality sinusoidal ac voltage regulation. The proposed two-layer controller consists of a tracking controller and a repetitive controller. Pole assignment with state feedback has been employed in designing the tracking controller for transient response improvement, and a repetitive control scheme was developed in synthesizing the repetitive controller for steady-state response improvement. Design procedure is given for synthesizing the repetitive controller for PWM inverters to minimize periodic errors induced by rectifier-type nonlinear loads. The proposed control scheme has been realized using a single-chip digital signal processor (DSP) TMS320C14 from Texas Instruments. A 2-kVA PWM inverter has been constructed to verify the proposed control scheme. Total harmonic distortion (THD) below 1.4% for a 60-Hz output voltage under a bridge-rectifier *RC* load with a current crest factor of 3 has been obtained. Simulation and experimental results show that the DSP-based fully digital-controlled PWM inverter can achieve both good dynamic response and low harmonics distortion.**

I. Introduction

In RECENT years, closed-loop regulated pulse-width-modulated (PWM) inverters have enjoyed extensive application in many types of ac power conditioning systems such as uninterruptible power supply (UPS), automatic voltage regulator (AVR), and programmable ac source (PACS). In these applications, the PWM inverters must maintain a sinusoidal output waveform under various types of loads, and this is achievable only by employing feedback control techniques.

Extensive research has focused on the closed-loop regulation of PWM inverters employing various feedback control schemes to achieve excellent dynamic response and low harmonic distortion [1]–[3]. However, most research was concentrated on improving the transient response through using instantaneous feedback control either by analog or microprocessor-based digital control techniques. In the deadbeat control approach [4], the control signal depends on a precise PWM inverter load model, and the performance of the system is sensitive to parameter and load variations. Another drawback of the deadbeat control scheme is that it requires a larger actuating signal to achieve the deadbeat effect.

Sliding mode control (SMC) with feedforward nonlinear compensation has been developed for the closed-loop regulation of a PWM inverter [5]. Although the SMC-controlled PWM inverter can achieve fast dynamic response and is insensitive to parameter and load variations, locating a satisfactory sliding surface is extremely difficult. Also, its performance degrades under a limited sampling rate. Applying fuzzy control [6] and optimal state feedback with pole assignment [7] improves the system's transient responses and its robustness to load variations. Although satisfactory results have been obtained for step-load disturbances, periodic distortions in the output waveform still remain when a rectifier-type of load is connected.

In most ac power conditioning systems, phase-controlled nonlinear loads are major sources of waveform distortion. Due to the periodic characteristics in voltage regulation, this type of nonlinear load results in periodic distortion in its output waveform. Repetitive control theory [8]–[9], which originates from the internal model principle [10], provides a solution to eliminate periodic errors in a nonlinear dynamic system. A number of modified repetitive control schemes have been developed for use in various industrial applications [11]–[14]. Repetitive control theory has also been applied to a PWM inverter employed in UPS systems to generate high-quality sinusoidal output voltage [15]. However, that investigation did not address the synthesis of the repetitive controller, and it has also been limited to fixed-frequency applications. In this study, we present a new control strategy based on the repetitive control theory to minimize the periodic distortion induced by the rectifier-type loads of a programmable ac power source.

The rest of this paper is organized as follows. In Section II, we introduce a DSP-controlled programmable ac power source. The structure and operational principles of the two-layer control strategy are then described. In Section III, the discrete-time model of the PWM inverter with an *LC* filter and a resistive load is derived. On the basis of the developed sampled-data model using state feedback control technique, a tracking controller with minimum step-tracking error is synthesized. Section IV describes the proposed repetitive control scheme. The design procedure, with a given design example, is also illustrated therein. Section V describes the implementation of the two-layer controller using a single-chip DSP

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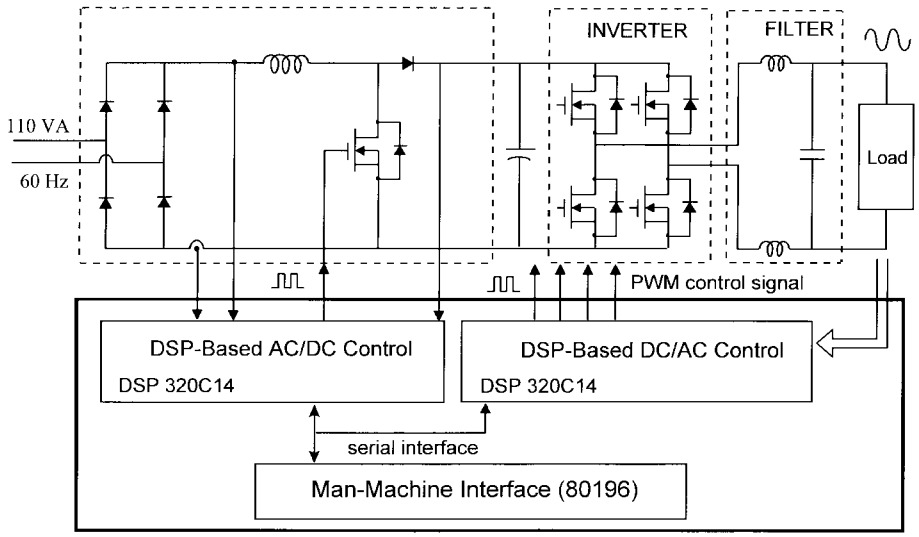


Fig. 1. Block diagram of the proposed DSP-controlled programmable ac power source.

TMS320C14 provided by Texas Instruments [16]. Simulation and experimental results are also given in this section. Section VI is the conclusion.

II. Two-Layer Control Scheme

A PACS is required to provide adjustable sinusoidal output voltage with low waveform distortion under various loading conditions. Therefore, the design specifications of PACS systems are much more stringent than those of VAR or UPS systems. A typical specification for a UPS system for voltage regulation is that its total harmonic distortion (THD) for a 60-Hz line output at a rated load with a current crest factor of 3 should be below 5.0%. The crest factor is defined as the ratio of peak to the rms value of a periodic waveform. With the same loading condition, a PACS system is usually required to output a waveform with a THD below 3.0%. Additionally, its output frequency can be increased to 500 Hz. Moreover, a PACS system should generate adjustable and prescribed output voltage waveforms. Therefore, to satisfy these stringent requirements, the closed-loop regulation of a PACS system needs more advanced control techniques.

Fig. 1 illustrates the block diagram of a proposed hierarchical DSP-controlled PWM inverter for a PACS system. The PACS consists of an ac/dc converter and a dc/ac converter. Each converter is controlled by a single-chip DSP (TMS320C14) from Texas Instruments. A single-chip microcontroller (80196KC) serves as the host controller. The host controller performs functions such as man-machine interface, system monitoring, and task coordination. It also has a serial interface to the DSP controller. Utility power is first rectified by a full-bridge rectifier and then boosted through a switching dc–dc converter with power factor control and dc voltage regulation. A full-bridge PWM inverter is employed for the dc–ac conversion. A higher switching frequency is usually desirable to minimize the size of the output filter, and this, in turn, results in a faster dynamic response for output regulation. However, the switching frequency is also constrained by the switching losses of the power devices. Selecting a proper switching frequency therefore becomes a compromise between these considerations. In the designed PACS system, both the booster and the PWM inverter are switched at 45 kHz. Owing to the limited space in this paper, only the digital control of the PWM inverter is addressed.

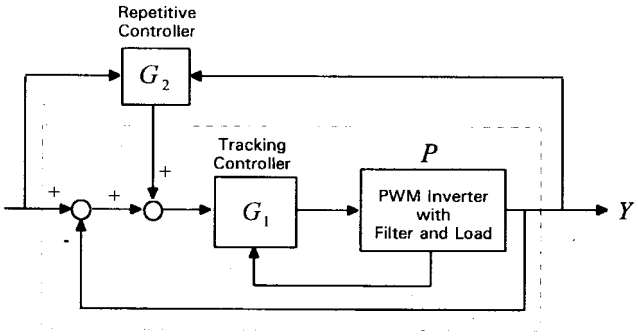


Fig. 2. Basic servo plant P_B. Proposed two-layer controller for ac voltage regulation.

In the PWM inverter subsystem, the inductor current and output voltage are sensed as feedback variables, the reference is read from a programmable RAM, and the DSP computes the required pulsewidths for the PWM inverter so that its output voltage will track a programmed reference waveform at each sampling. Fig. 2 depicts the proposed two-layer control scheme for the closed-loop regulation of the PWM inverter. Two controllers are included in the control loops: a tracking controller G_1 and a repetitive controller G_2. The function of the tracking controller is to improve the transient response, while the repetitive controller serves to eliminate the periodic errors resulting from periodic disturbances. Essentially, these two controllers are coupled and influence each other. However, the appropriate tuning of the convergent rate of the repetitive controller minimizes the coupling effect. In the proposed design procedure, these controllers are designed on the basis of the same nominal plant model. Any control method that guarantees the stability of the closed-loop-controlled plant within the specified operating bound is applicable for synthesizing the

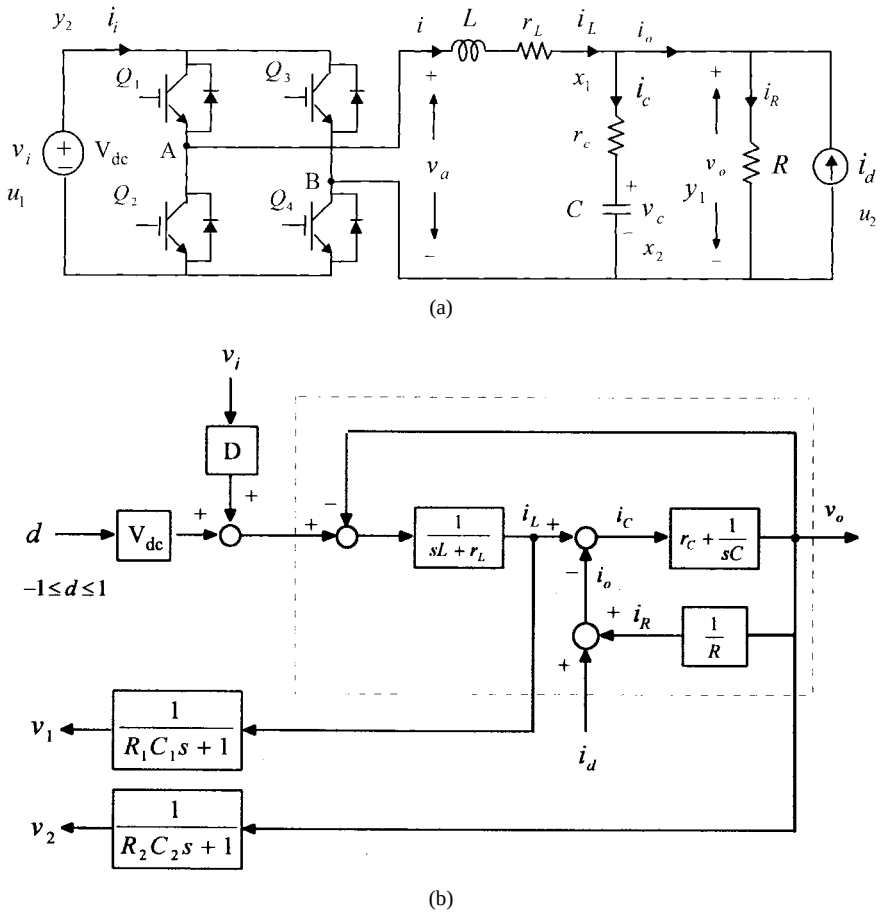


Fig. 3. (a) Equivalent circuit of the PWM inverter with output filter and load and (b) its block diagram representation.

tracking controller. In this paper, partial state feedback with the least squares error fitting of specified time response is adopted in the design of the tracking controller, and a design procedure is developed for synthesizing the repetitive controller to guarantee asymptotic stability for periodic disturbances.

III. Tracking Controller Design

A. Modeling the PWM DC/AC Converter

Fig. 3(a) illustrates the equivalent circuit of the PWM inverter with an *LC* output filter and an unknown load. Fig. 3(b) is a block diagram representing a PWM inverter system. The output voltage v_o and the inductor current i_L are selected as state feedback variables, and the load current i_d is treated as an external disturbance. In designing a digital-controlled PWM switching converter, two switching frequencies require careful selection, i.e., the PWM switching frequency of the power converter and the sampling frequency of the digital controller. When the sampling frequency is increased, current and voltage ripples resulting from the switching of the power converter become more prominent, and this will deteriorate the control performance. Therefore, low-pass filters must be added between the sensing signals and analog-to-digital (A/D) converters. The cutoff frequencies of these feedback sensing filters may no longer be much larger than the sampling frequency. Therefore, the filter dynamics must be included in the plant dynamics. The dynamic equation of the PWM inverter filter-load with state feedback sensing filters can be expressed as

$$\frac{dt}{d}\mathbf{x}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t), \quad y(t) = \mathbf{c}\mathbf{x}(t) + \mathbf{d}\mathbf{u}(t) \tag{1}$$

where

$$\mathbf{x}(t) = [i_L \quad v_c \quad v_1 \quad v_2]^T(t) \tag{2}$$

$$y(t) = v_o(t) \tag{3}$$

$$\mathbf{u}(t) = [v_i \quad i_o]^T(t) \tag{4}$$

$$\mathbf{A} = \begin{bmatrix} -\dfrac{r_L + r_C}{L} & -\dfrac{1}{L} & 0 & 0 \\ \dfrac{1}{C} & 0 & 0 & 0 \\ \dfrac{1}{R_1C_1} & 0 & -\dfrac{1}{R_1C_1} & 0 \\ \dfrac{r_C}{R_2C_2} & \dfrac{1}{R_2C_2} & 0 & -\dfrac{1}{R_2C_2} \end{bmatrix} \tag{5}$$

$$\mathbf{B} = \begin{bmatrix} \dfrac{r_C}{L} & \dfrac{-1}{C} & 0 & \dfrac{-r_C}{R_2C_2} \\ \dfrac{1}{L} & 0 & 0 & 0 \end{bmatrix}^T \tag{6}$$

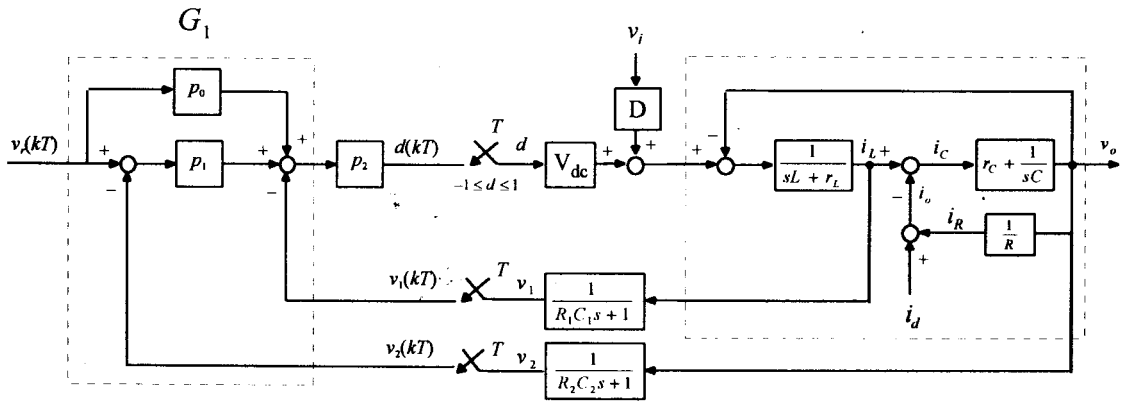


Fig. 4. Digital tracking controller: feedforward with state feedback control.

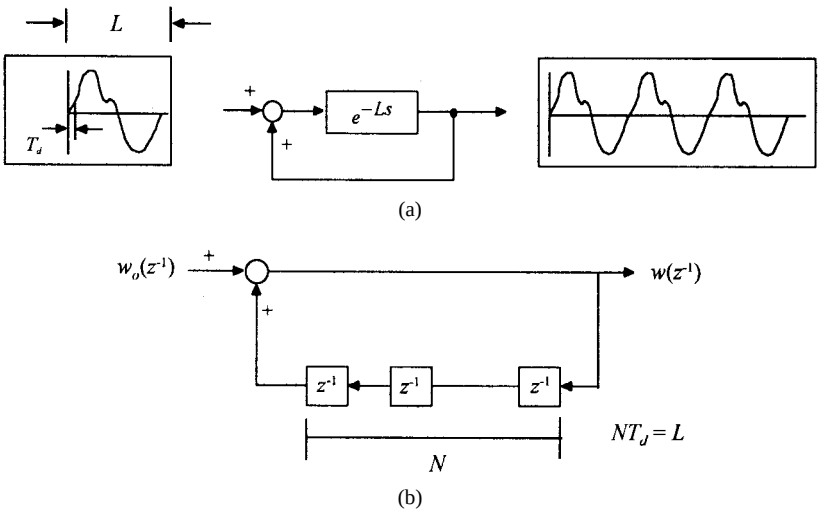


Fig. 5. Generation of periodic signal in (a) continuous-time domain and (b) discrete-time domain: unit time delay with period T_d.

$$\mathbf{c} = [r_c \quad 1 \quad 0 \quad 0] \tag{7}$$

$$\mathbf{d} = [0 \quad -r_C]. \tag{8}$$

If the PWM inverter switching frequency is much higher than the natural frequency of the output *LC* filter, only the inverter average output $\overline{v}_o(t)$ needs consideration, and here, it is assumed to be $v_o(t) = \overline{v}_o(t)$. In the given design example, the PWM switching frequency is set at 45 kHz, and the natural resonant frequency of the *LC* filter is about 3.57 kHz. The discrete-time model of the PWM inverter filter-load dynamics can be derived from its continuous counterpart and can be expressed as

$$\mathbf{x}[k+1] = \mathbf{G}\mathbf{x}[k] + \mathbf{H}u[k], \quad y[k] = \mathbf{c}\mathbf{x}[k] + \mathbf{d}\mathbf{u}[k] \tag{9}$$

where

$$\begin{aligned} \mathbf{G} &= e^{\mathbf{A}T} = \mathbf{I} + \mathbf{A}T\Psi \\ \mathbf{H} &= \Psi T\mathbf{B} \\ \Psi &= \mathbf{I} + \frac{\mathbf{A}T}{2!} + \frac{\mathbf{A}^2T^2}{3!} + \cdots \end{aligned} \tag{10}$$

and T is the sampling period. The Ψ can be calculated by an iterative power series

$$\Psi \approx \mathbf{I} + \frac{\mathbf{A}T}{2}\left(\mathbf{I} + \frac{\mathbf{A}T}{3}\left(\cdots \frac{\mathbf{A}T}{N-1}\left(I + \frac{\mathbf{A}T}{N}\right)\right)\cdots\right) \tag{11}$$

which has better numerical properties than the direct series of powers. A discussion of the selection of N and a technique for computing Ψ for a comparatively large T is found in [17]. In practical applications, a selection of $N = 10$ is suitable for most situations.

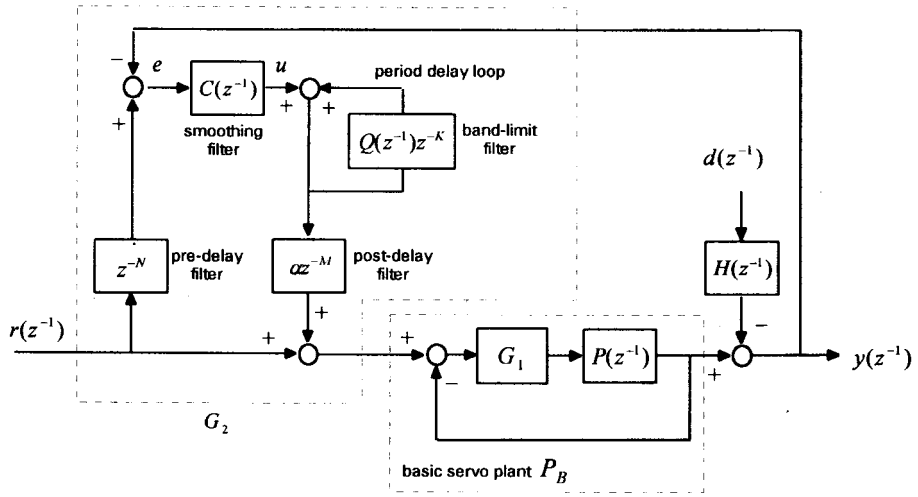
B. Design of the Tracking Controller

In the author's previous work [7], state feedback with feedforward control is employed to regulate the PWM inverter for sinusoidal waveform synthesis. Fig. 4 illustrates its detail by a block diagram. The state feedback and feedforward gains can be determined by fitting a specified step response with the least squares errors employing the steepest descent method. The control parameters in Fig. 4 can be transformed to a feedback gain matrix defined as [7]

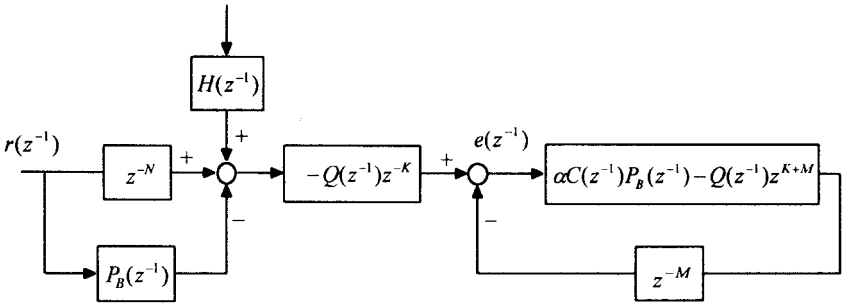
$$\mathbf{k} = [0 \quad 0 \quad k_1 \quad k_2] \tag{12}$$

the dynamic equation of the basic servo plant can be expressed as

$$\begin{aligned} \mathbf{x}[k+1] = \left(\mathbf{G} - \mathbf{H}\begin{bmatrix}\mathbf{k}\\ \mathbf{0}\end{bmatrix}\right)\mathbf{x}[k] + \mathbf{H}\begin{bmatrix}k_0 V_{ref}[k]\\ 0\end{bmatrix} \\ + \mathbf{H}\begin{bmatrix}0\\ i_o[k]\end{bmatrix} \end{aligned} \tag{13}$$



(a)



(b)

Fig. 6. (a) Block diagram of the proposed repetitve control system and (b) the simplified block diagram.

and the output can be expressed as

$$y(z^{-1}) = [P_B(z^{-1}) \quad -H(z^{-1})]\mathbf{u}(z^{-1}) \tag{14}$$

where $P_B(z^{-1})$ is the reference-to-output transfer function and $H(z^{-1})$ represents the output impedance.

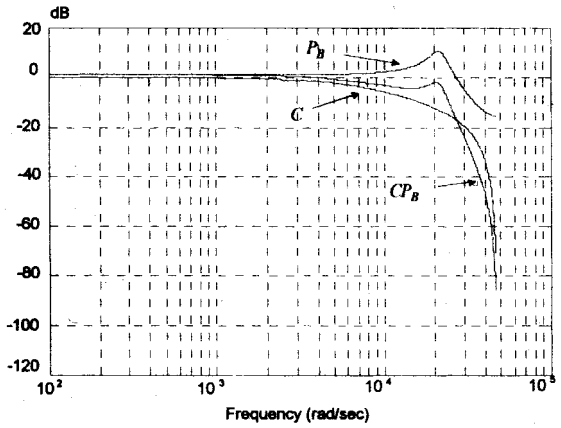
IV. Repetitive Controller Design

The basic concept of *repetitive control theory* originates from the *internal model principle* [10]. This principle states that controlled output tracks a set of reference inputs without steady-state error if the model that generates these references is included in the stable closed-loop system. For example, if a closed-loop control system is required to have a zero steady-state error to a step input, then the model of the step function, i.e., $1/s$, should be included in its loop transfer function. Similarly, if the system is required to have a zero steady-state error to a sinusoidal input, then the model of the sinusoidal function i.e., $\omega_n^2/s^2 + \omega_n^2$, where ω_n is the oscillating frequency, should be included in its stable loop transfer function. In practical applications, a periodic input or disturbance may consist of many high-order harmonics. With the limited system bandwidth, completely eliminating these periodic errors within a control system is practically impossible. This constraint becomes an important consideration factor in synthesizing the repetitive controller to minimize low-order harmonic distortion.

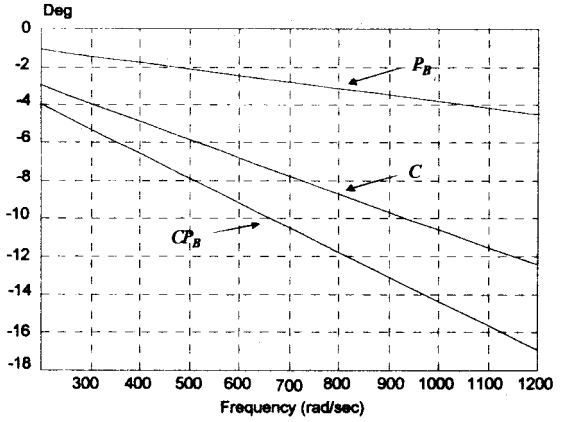
TABLE I
Parameters of the PWM Inverter System

Item	Symbol	Nominal value	Unit
Sampling rate	f_s	15 k	Hz
Filter inductor	L	0.6	mH
Filter capacitor	C	3.3	μF
Inductor ESR	r_L	0.5	Ω
Capacitor ESR	r_C	1.0	Ω
Nominal load	R	40	Ω
DC link voltage	V_{dc}	300	V
Output voltage	v_o	110	$V_{(rms)}$
Switching frequency	f_{sw}	45 k	Hz

In implementing a repetitive control system, a periodic actuating signal to eliminate the periodic errors that resulted from periodic reference or disturbance must be generated. As Fig. 5 demonstrates, such a signal can be generated either by analog or digital techniques with a specified initial condition. However, in practice, storing an arbitrary waveform in analog form is extremely difficult. In contrast, a periodic signal generator can be more easily achieved by a software-based digital control technique. If a periodic signal can be synthesized into a feedback system and a compensator designed to achieve asymptotic stability, then it is possible to track a periodic command or reject a periodic disturbance with the same period.

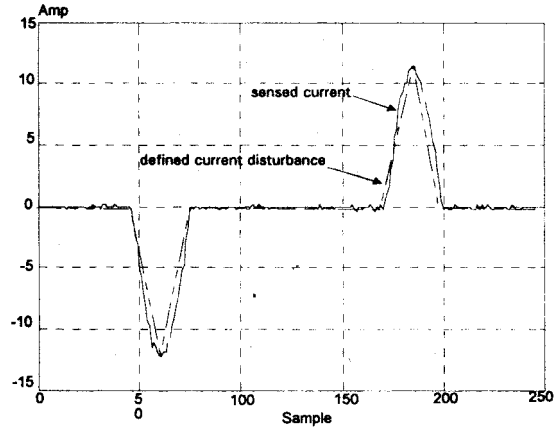


(a)

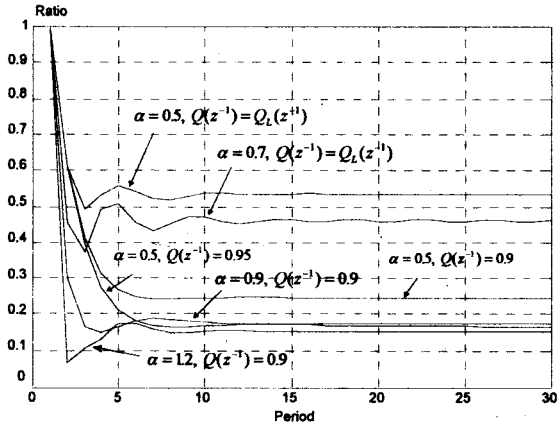


(b)

Fig. 7. The frequency response of $C(z^{-1})$, $P(z^{-1})$, and $C(z^{-1})P_B(z^{-1})$: (a) magnitude and (b) local phase around 800 rad/s.



(a)



(b)

Fig. 8. (a) The defined current disturbance and (b) error-convergence of the repetive control system at various parameter settings.

The proposed repetitive control scheme is illustrated in Fig. 6(a), where $C(z^{-1})$ is the *compensator* for the repetitive control loop, $P(z^{-1})$ is the basic servo plant that has already been closed-loop-regulated by a tracking controller, $H(z^{-1})$ represents the model from the disturbance to the output, and $Q(z^{-1})$ is a *band-limit filter*. A *predelay filter*, z^{-N}, is added at the beginning of the repetitive control path, where N represents the required number of delays. The predelay filter compensates for the corresponding phase delay of the basic servo plant at a specified output frequency. A *postdelay filter*, αz^{-M}, is added at the end of the repetitive control path, where M represents the required number of delays and α is a tuning gain. The postdelay filter compensates for the corresponding phase delay resulting from the basic servo plant and the loop compensator $C(z^{-1})$.

The compensator $C(z^{-1})$ is used to stabilize the repetitive control loop. Its particular function is to attenuate possible resonant peaks resulting from the basic servo plant. The band-limit filter $Q(z^{-1})$ within the period delay loop relieves the stringent requirement of the repetitive controller to eliminate periodic error completely. The low-pass characteristics of $Q(z^{-1})$ allow the repetitive controller to place more weight on minimizing the low-order harmonics of the periodic error. In the period delay loop, K represents the number of samples within a period of the repetitive controller, T is the sampling period of the repetitive controller, and KT is equal to the period of a periodic reference or disturbance.

In the proposed control scheme, the repetitive controller functions as an auxiliary controller that modifies the reference command by adding a periodic compensation signal. For a periodic reference or disturbance, the period delay loop will attenuate its effect on the nominal control loop. The purpose of including a postdelay filter in the repetitive control path is that the controller will not react until the effect of the disturbance appears on the plant output. When a long delay occurs within the repetitive control loop, it will significantly deteriorate the loop dynamics [18]. If the synthesized periodic correcting signal is required to lead several sampling intervals in the next repetitive cycle, M should be smaller than K.

In synthesizing a repetitive control system, a compromise between control actions for periodic and a periodic reference or disturbance must be made. Carefully selecting the controller parameters is a compromise between the convergent rate and relative stability of the repetitive control system. Some related parameters of the constructed PWM inverter system are given in Table I. As presented in the following, a practical design example demonstrates the effectiveness of the design procedure.

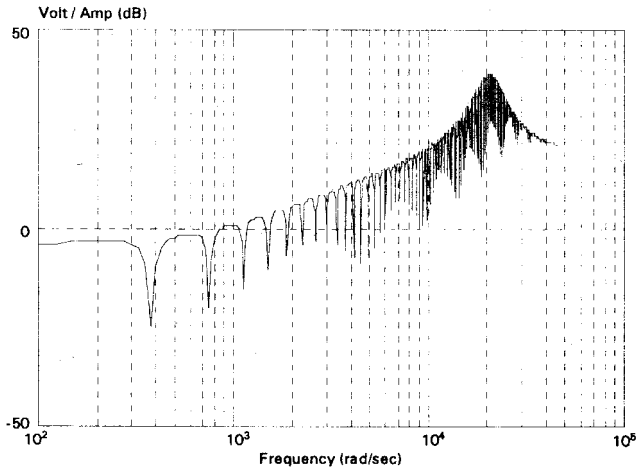


Fig. 9. Output impedance of the repetitive-controlled PWM inverter under a 60-Hz periodic disturbance.

A. Basic Servo Plant

In considering the filter dynamics, the PWM inverter is closed-loop regulated by means of a partial state feedback control scheme. The control parameters are determined by a parameter plane optimization technique with a stable region constraint [7], and $k_1 = -0.9$ and $k_2 = -0.15$ are the design results of the given example [19]. The closed-loop reference-to-output transfer function of the basic servo plant is

$$P_B(z^{-1}) = \frac{0.8045z^{-1} + 0.5069z^{-2} - 0.1044z^{-3} + 0.0043z^{-4}}{1 - 0.4289z^{-1} + 0.7741z^{-2} - 0.1344z^{-3} + 0.0044z^{-4}} \tag{15}$$

and the closed-loop output impedance is

$$H(z^{-1}) = \frac{1 + 11.45z^{-1} - 14.53z^{-2} + 1.53z^{-3} + 0.021z^{-4}}{1 - 0.4289z^{-1} + 0.7741z^{-2} - 0.1344z^{-3} + 0.0044z^{-4}}. \tag{16}$$

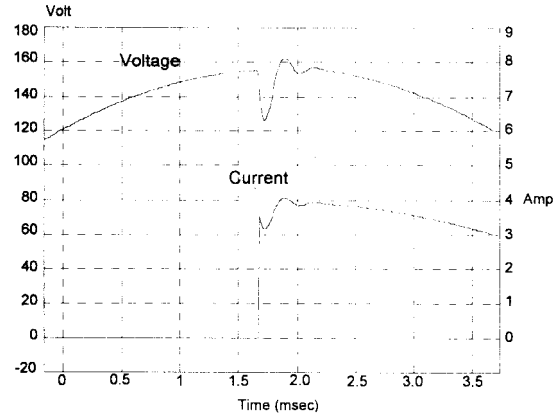
B. Compensator

The compensator for the repetitive control loop is designated as a low-pass filter whose function is to attenuate the resonant peak of $P_B(z^{-1})$ below unit so that the tuning of α can be normalized to unit. With respect to the frequency response featured in Fig. 6(a), the magnitude of $C(z^{-1})P_B(z^{-1})$ can be kept equal to or less than unit if the loop compensator $C(z^{-1})$ is adequately designed. In the given design example, a second-order low-pass filter was synthesized as the compensator

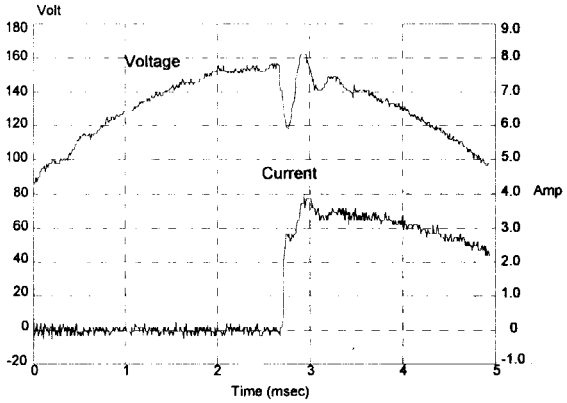
$$C(s) = \frac{(1.9 \cdot 10^4)^2}{s^2 + 2 \cdot (1.6)(1.9 \cdot 10^4)s + (1.9 \cdot 10^4)^2}. \tag{17}$$

This low-pass filter has a damping ratio of 1.6, and its magnitude decays to 0.3125 at a frequency of $1.9 \cdot 10^4$rad/s. The discrete form of this filter, using *bilinear transformation* [20] at a sampling frequency of 15 kHz, is

$$C(z^{-1}) = \frac{0.117 + 0.234z^{-1} + 0.117z^{-2}}{1 - 0.3494z^{-1} - 0.183z^{-2}}. \tag{18}$$



(a)



(b)

Fig. 10. (a) Simulation and (b) experimental current and voltage waveforms of the basic servo plant under large-load variation.

C. Phase-Delay Compensation

Fig. 7 illustrates the frequency responses of $C(z^{-1})$, $P_B(z^{-1})$, and $C(z^{-1})P_B(z^{-1})$. The postdelay filter compensates for the phase delay resulting from $C(z^{-1})P_B(z^{-1})$. This phase delay is a function of the output frequency of the programmable ac power source. The following are defined:

$$M = K - \left[\frac{PH_{delay}}{\frac{360}{K}}\right] \tag{19}$$

$$N = \left[\frac{PH_{plant}}{\frac{360}{K}}\right] \tag{20}$$

where PH_{delay} and PH_{plant} denote the phase delay at a specified output frequency of the frequency response of $C(z^{-1})P_B(z^{-1})$ and $P_B(z^{-1})$, respectively. The bracket "[ ]" denotes the *round function* that rounds its element to the nearest integer. In (19) and (20), $360/K$ represent an "approximate phase lag per sample" of the corresponding plant when there are K samples in one period for the repetitive control. Fig. 7(b) displays the corresponding phase responses of $C(z^{-1}), P_B(z^{-1})$, and $C(z^{-1})P_B(z^{-1})$, from 200 rad/s (32 Hz) to 1200 rad/s (191 Hz). For an output frequency range from 60 to 150 Hz, Fig. 7(b) indicates that the predelay

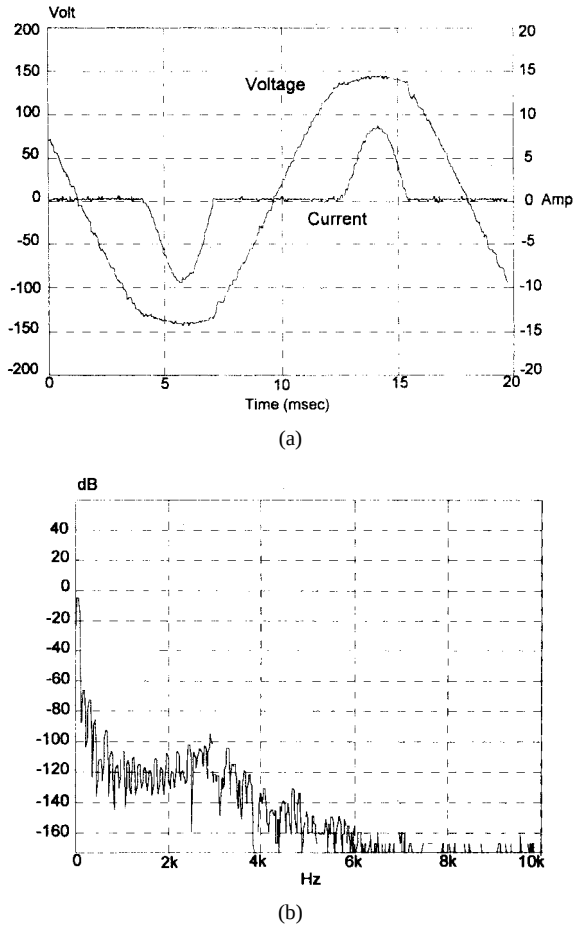


Fig. 11. (a) The 60-Hz output waveforms of the basic servo plant under rectifier load at a current crest factor of 3 and (b) its corresponding power spectrum.

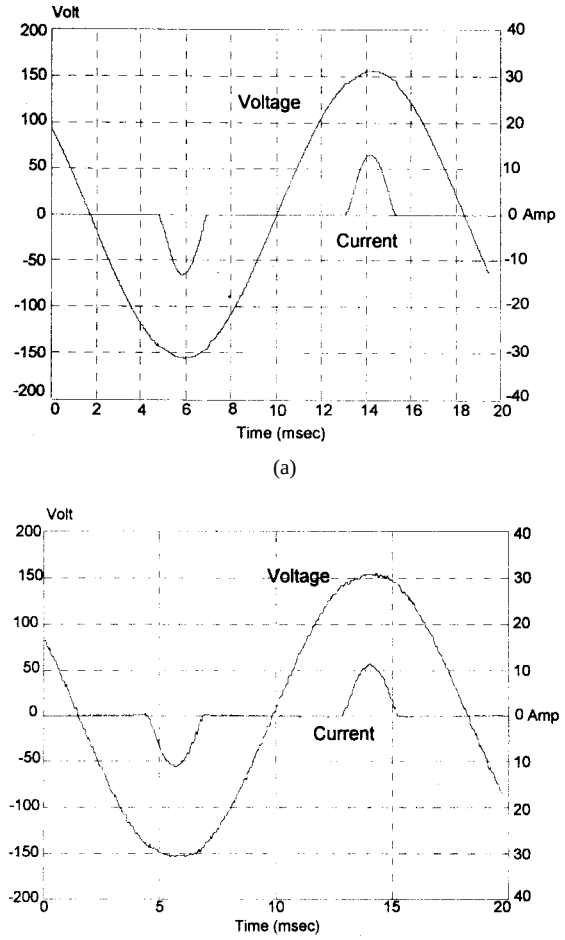


Fig. 12. Output voltage and current waveforms under 60-Hz rectifier load when $Q(z^{-1}) = 0.95$: (a) simulation and (b) experimental.

number N can be approximated by one. Similarly, Fig. 7(b) illustrates the phase responses from which it can be observed that $M = K - 3$ works well during the entire frequency spectrum.

D. Band-Limit Filter and Postdelay Filter

Synthesizing the band-limit filter and the postdelay filter depends on sufficient conditions of stability and the error-convergence rate [19]. Steady-state analysis shows that if the band-limit filter $Q(z^{-1})$ is unit, no steady-state error occurs. Unfortunately, the Nyquist criterion reveals that it is not possible to establish a stable system when $Q(z^{-1}) = 1$. With this constraint, the choice lies in setting either $Q(z^{-1})$ a little smaller than unit, for example 0.95, or in adding a low-pass filter to decrease the magnitude of $Q(z^{-1})z^{-K+M}$ at a higher frequency and keeping $Q(z^{-1})$ equal to unit at a lower frequency.

In determining the postdelay filter gain and the band-limit filter $Q(z^{-1})$, a measured output current waveform with the current crest factor of 3, which Fig. 8(a) indicates, was considered as an exogenous periodic disturbance. Without losing generality, a triangular shape was employed to approximate such a periodic disturbance, and its corresponding output voltage responses can then be calculated at various control parameters.

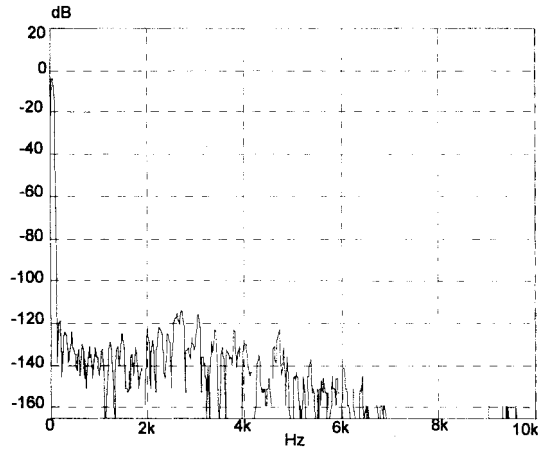
To investigate the effect of the band-limit filter and postdelay filter gain on the error convergence,

$$Q_L(z^{-1}) = \frac{0.4z + 0.4}{z - 0.2} \tag{21}$$

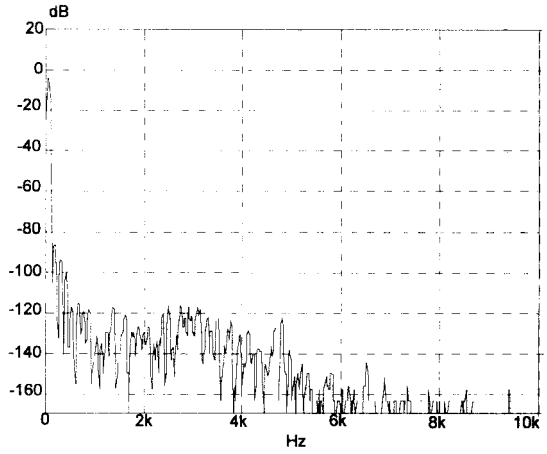
serves as a low-pass filter for $Q(z^{-1})$ and is compared with different settings of $Q(z^{-1})$ and α. Fig. 8(b) illustrates the error convergence curves at various settings of band-limit filter and postdelay gain. These curves were recorded from their maximal error at the peak of the waveform. Fig. 8(b) exemplifies the compromise between the convergent rate and stability by choosing $Q(z^{-1}) = 0.95$ and $\alpha = 0.5$ for the given design example. Fig. 9 displays the output impedance of the PWM inverter using a repetitive control technique subjected to a 60-Hz periodic disturbance. According to that figure, the output impedance has been to a minimum value at integral multiples of 60 Hz.

V. Simulation and Experimental Results

A single-chip DSP TMS320C14 provided by Texas Instruments was used to implement the proposed digital controller for PACS voltage regulation. This DSP has many good features, thereby allowing a sophisticated control algorithm to be

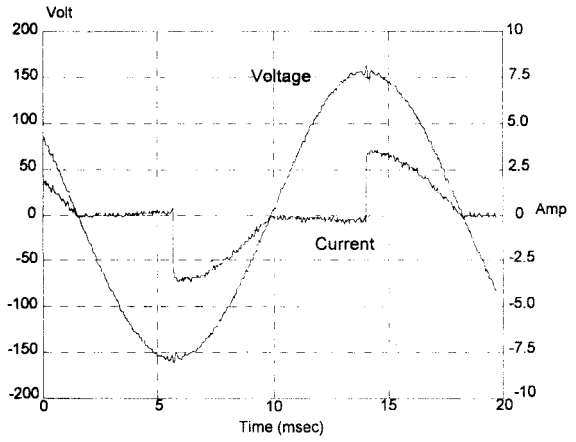


(a)

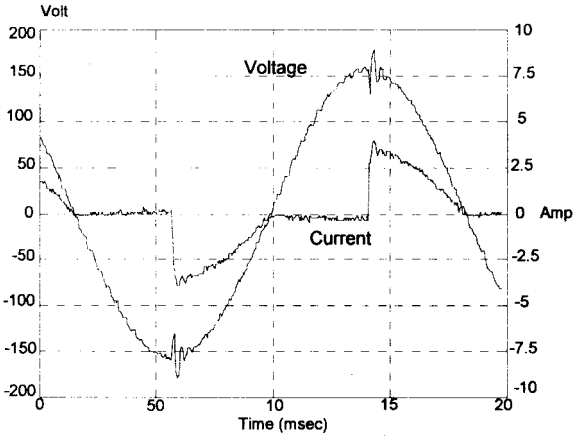


(b)

Fig. 13. Power spectrum when the repetitive control system is under the (a) resistive load and (b) rectifier load.



(a)



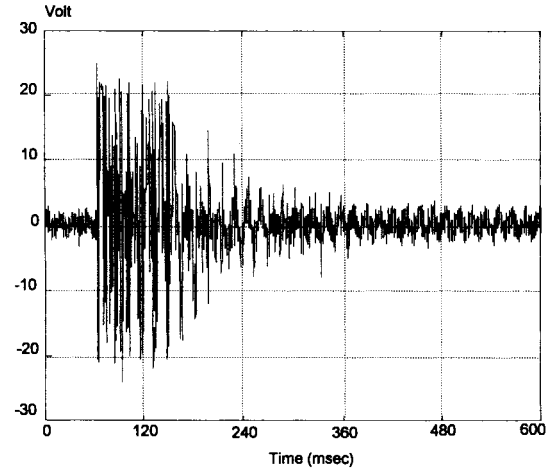
(b)

Fig. 14. 60-Hz output voltage and current waveform operating from no load to resistive load when the band-limit filter is (a) a constant $Q(z^{-1}) = 0.95$ and (b) a low-pass filter $Q(z^{-1}) = Q_L(z^{-1})$.

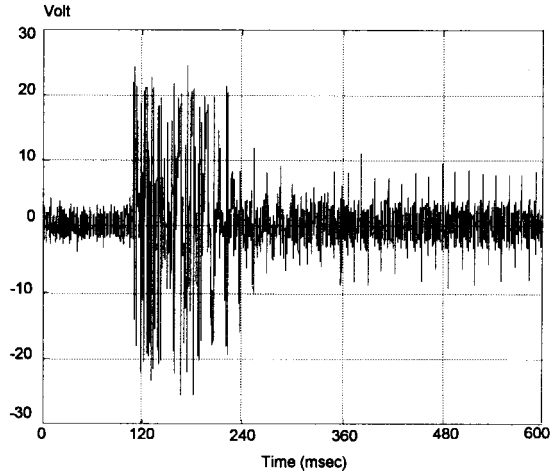
implemented for power converting systems. They include a 200-ns instruction cycle, a 16-b parallel multiplier, multiple independent programmable timers, and some on-chip RAM and ROM [16]. However, it does not possess any on-chip A/D or D/A converters. The hardware circuit of the proposed DSP-based digital controller consists of a 16-b TMS320C14 single-chip DSP, a six-channel multiplexed 12-b A/D converter, a 4K-word external program memory, and an RS232 computer interface. The TMS320C14 also comprises some on-chip peripherals necessary for industrial control. These include four 16-b timers, two general-purpose timers, a watchdog timer, a baud-rate generator, a 16-b programmable I/O, a serial port, and an event manager with a six-channel PWM output. The event manager consists of a six-output-compare subsystem and a four-input-capture subsystem. The PWM output waveform can be adjusted from 8 b of resolution at 100 kHz to 14 b at 1.6 kHz.

The constructed DSP-based fully digital-controlled 2-kVA PWM inverter operates at a switching frequency of 45 kHz and a sampling frequency of 15 kHz. Some key parameters of the constructed system are listed in Table I. Synthesizing the repetitive controller and simulation of the PACS was achieved by the software packages MATLAB and SIMULINK.

Fig. 10 shows the simulation and experimental results of the output voltage and the current waveforms of the digital-controlled PWM inverter without the repetitive controller with a step-load change from no load to a 300-W resistive load. The modeling of the digital-controlled PWM inverter can be verified from the close similarity of the experimental and simulation results, as shown in Fig. 10. The settling time of the digital-controlled PWM inverter for a step disturbance is about 560 μs. Fig. 11(a) summarizes the experimental results when the inverter's output was connected to a 60-Hz rated bridge rectifier *RC* load with a current crest factor of 3. Fig. 11(b) illustrates that its corresponding voltage harmonic spectrum and its THD is -28 dB (5%). Under the same testing conditions, Fig. 12 summarizes the simulation and experimental results when the repetitive control scheme is applied. This figure indicates that the output voltage waveform can still maintain a sinusoidal output under a rectifier *RC* load. Fig. 13 illustrates the harmonics spectrum of the output voltage waveform under a resistive load and a rectifier load. The THD is -40 dB (1.0%) for a resistive load and -37 dB (1.4%) for a rectifier load. These results prove that the designed repetitive controller can effectively eliminate integer

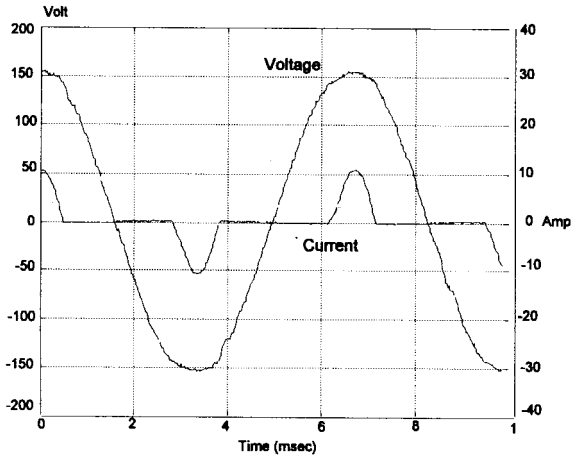


(a)

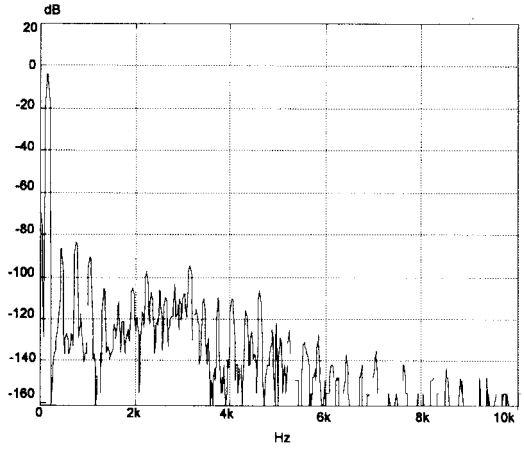


(b)

Fig. 15. The convergence of output voltage error under repetitive control: (a) $Q(z^{-1}) = 0.95$ and $\alpha = 0.5$ and (b) $Q(z^{-1}) = Q_L(z^{-1})$ and $\alpha = 0.7$.



(a)



(b)

Fig. 16. (a) Output waveforms under 150-Hz rectifier load and (b) the corresponding power spectrum with THD $= -36$ dB (1.6%).

harmonic disturbances within its system bandwidth, even at different loads.

Fig. 14 illustrates the transient responses when the band-limit filter is set at different values. The output was connected to a phase-controlled resistive load. The band-limit filter Q, displayed in Fig. 14(a), is just a scaler and is set at 0.95; the settling time is 380 μs, and the maximum voltage distortion is 6 V. Fig. 14(b) illustrates the band-limit filter that is set as the defined low-pass filter (21); the settling time is 540 μs and the maximum voltage distortion is 23 V.

Fig. 15 shows the convergence of the PWM inverter output voltage error induced by a bridge-rectifier *RC* load under repetitive control at different settings of the band-limit filter. These periodic errors can be reduced from 12.5 to 25% of its original value within 120–180 ms. While faster convergence results in a larger steady-state error, slower convergence expectedly results in a smaller steady-state error. Experimental results reveal that designing the band-limit filter calls for a compromise between the rate of error convergence and steady-state error.

Fig. 16(a) illustrates the output voltage and current waveforms at 150 Hz under the defined rectifier *RC* load. The harmonic spectrum of the output voltage is shown in Fig. 16(b). The THD of the output voltage is -36 dB (1.6%), which is much smaller than what can be achieved by conventional control techniques. These experimental results confirm that the proposed repetitive control scheme effectively improves the steady-state performance of an ac voltage regulator and, at the same time, maintains its transient dynamics.

VI. Conclusion

In this paper, we have presented a two-layer control strategy to improve both the transient and steady-state responses of a closed-loop regulated PWM inverter for sinusoidal ac voltage generation. The two-layer controller consists of a servo controller and a repetitive controller. The servo controller serves to improve the load disturbance rejection capability and is designed by using an optimal state-feedback control technique. The repetitive controller serves to eliminate the periodic error induced by a nonlinear load and is synthesized based on the repetitive control theory. These two controllers are designed separately to achieve excellent dynamic response and low harmonic distortion for a high-quality ac power source when operating at 110 V, 15 A, and 60 Hz. The output voltage error for a step-rated load change can be reduced to 5% within

0.3 ms. A total harmonic distortion (THD) below 1.4% of a rated rectifier *RC* load at a current crest factor of 3 is feasible. Experimental results show the proposed repetitive control scheme can effectively eliminate the periodic errors induced by a bridge-rectifier *RC* load. Although the given design example is based on a nominal bridge-rectifier *RC* load, using the proposed repetitive control scheme imposes no constraint on the connected load. The proposed control scheme with the DSP-realization technique reveals that by applying modern control techniques, high-performance DSP can significantly improve the control quality of a power converting system.

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