Chapter 1

Introduction

1.1 Motivation

MEMS (MicroElectroMechanical Systems) have been regarded as the most leading technology in the incoming decades. Combining mechanical elements with electronic circuits, MEMS devices provide a variety of possibilities in many different fields, including aero-space, medical care, and consumer electronics. Low cost, tiny MEMS devices will enter and change our daily life.

However, these changes do not happen as fast as expected. One of the major challenges for MEMS device commercialized is packaging. There are some differences between IC packaging and MEMS packaging. The main goal of IC packaging is to provide a physical support, electrical connections, and thermal path and to isolate it from environments. MEMS packaging, on the contrary, can not totally isolated from surroundings. In order to provide specific functionalities, MEMS devices have to work closely with environments. At least one of the none-electrical signals becomes necessary input or output parameter. Due to this reason, MEMS packaging has to provide specific way for none-electrical signal input/output while isolates unwanted ones.

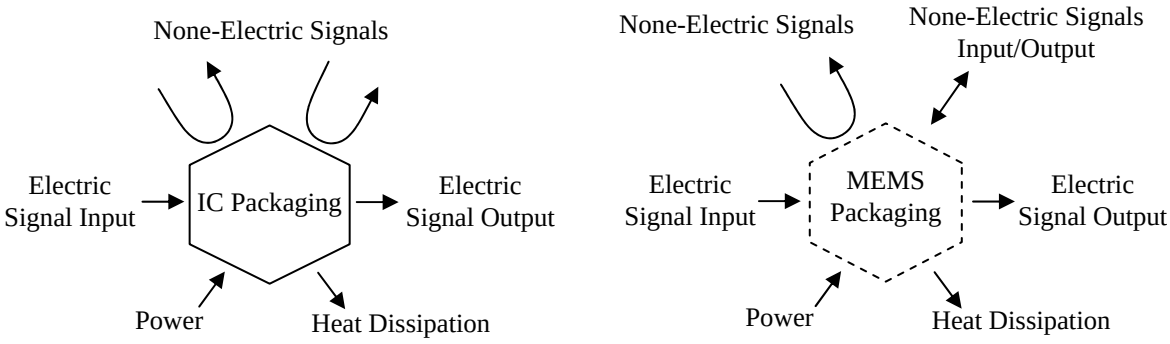


Fig.1 Difference between IC packaging and MEMS packaging

Another challenge of MEMS packaging is the freestanding microstructures. Again, in order to achieve specific functionalities, many MEMS devices contain freestanding microstructures. These freestanding microstructures are obtained by using surface micromachining technique called “Sacrificial Layer”.

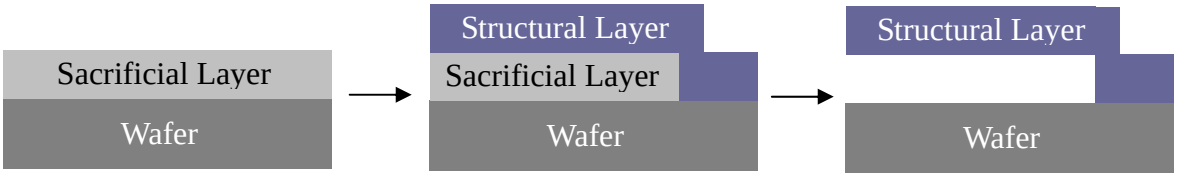
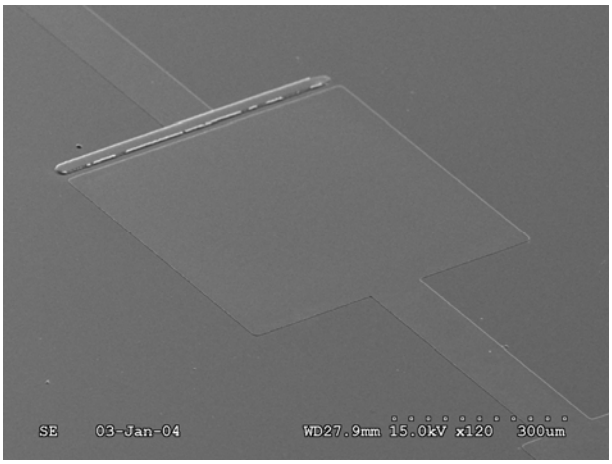


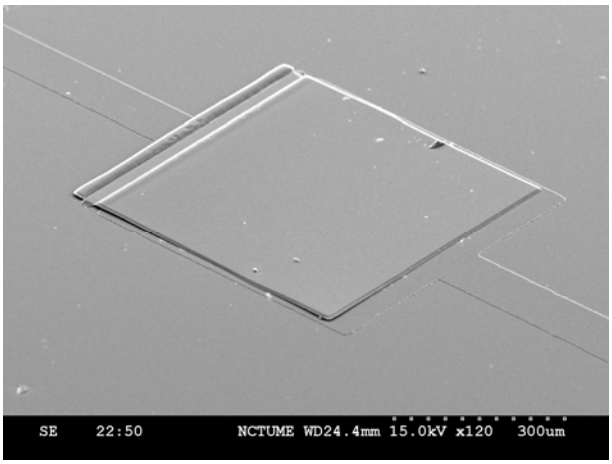
Fig.2 Sacrificial layer technique

First, sacrificial layer such as silicon dioxide, is deposited on silicon substrate. After anchor is patterned, structural layer such as polysilicon is also deposited and patterned over sacrificial layer. Finally, sacrificial layer is removed by etchant, leave the freestanding microstructures.

It is clear, however, these freestanding microstructures are extremely fragile and almost impossible to survive in the following wet dicing process. Cooling water jet may damage structure; surface tension force of water may cause structure stiction, as shown in the pictures.



Upper electrode of overlapping parallel capacitor is washed out by cooling water jet



Structural stiction due to surface tension force of water

Fig.3 MEMS device without protection after dicing operation

These problems can be solved simply by remove sacrificial layer die by die after dicing operation. But this solution is quite time consuming and troublesome, which increases the cost of manufacture. Also, released dice cannot pick-and-place by using traditional vacuum pick-up since there are freestanding microstructures on top. New facilities must be developed for MEMS dice handling.

The packaging problems mentioned above have made many MEMS products too expensive to be commercialized. The cost of MEMS packaging can vary from 20% to as high as 95% of total cost of final products [1]. Besides, final products are always too bulky after packaging, which eliminates the benefits of MEMS devices originally expected. To meet the requirements between cost, performance and size, the post-process packaging concept is introduced. All of the MEMS devices are fabricated, released, and packaged at the same time in wafer level. This approach can protect fragile microstructures from possible damages or contaminations in the following process such as dicing or wire-bonding. Capping freestanding microstructures with bulk material such as glass also provides the compatibility for the use of traditional vacuum pick-up.

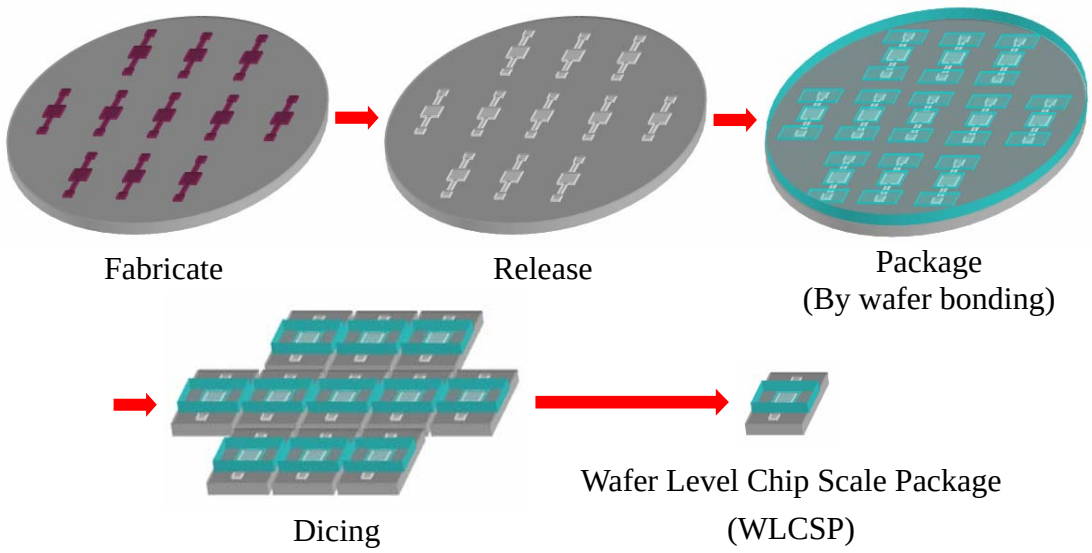


Fig.4 Basic concept of post-process package

In the post-process packaging, the most crucial step is wafer bonding technique. Wafer bonding encapsulates fragile freestanding microstructures within controlled atmosphere such as vacuum, inert gas, or particle less, provides safety working space and environment for MEMS devices in a batch way, effectively cut down the cost of packaging.

1.2 Related Researches

Wafer bonding techniques had been developed for many years. Each of them was developed for specific requirements. All of these wafer bonding techniques will be introduced in the following sections.

1.2.1 Fusion Bonding

Fusion bonding, sometimes calls direct bonding, usually uses in silicon-on-insulator (SOI) technology or cavity seal [2]. Fusion bonding can bond bare silicon wafers or oxidized silicon wafers together. Up to 5 layers fusion bonding has been reported [3]. Wafer surface to be bonded must be well polished and completely particle free, any impurities remain will cause bonding to fail locally. At beginning, wafers must undergo hydration process, usually done by soaking wafers in H_2O_2-H_2SO_4 mixture or boiling nitric acid [4]. After hydration treatment, hydroxyl groups are formed on the surfaces, making two wafers hydrophilic. Then two polished wafer surfaces are brought into contact at room temperature, weak hydrogen bonds are established at the contact surface, as shown in Fig.5. The establishment and voids can be observed under IR-microscope (Fig.6) or ultrasonic. [5]

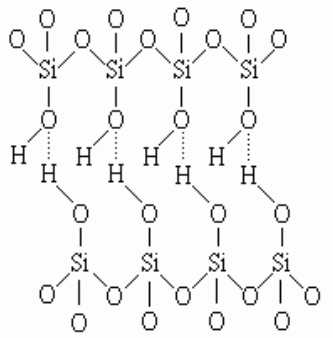


Fig.5 Weak hydrogen bonds forms when hydrophilic surfaces are brought into contact

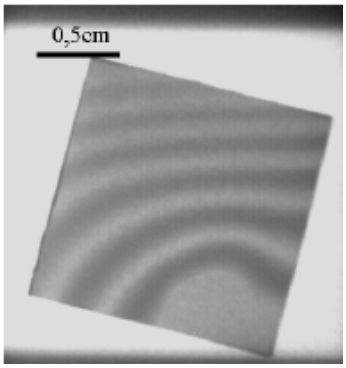


Fig. 6 IR transmission image immediately after contact [5]

The second step is a high temperature annealing to increase the bonding strength. Molecular water is eliminated and covalent bonds are created between surfaces. The whole reaction is shown in Fig.7.

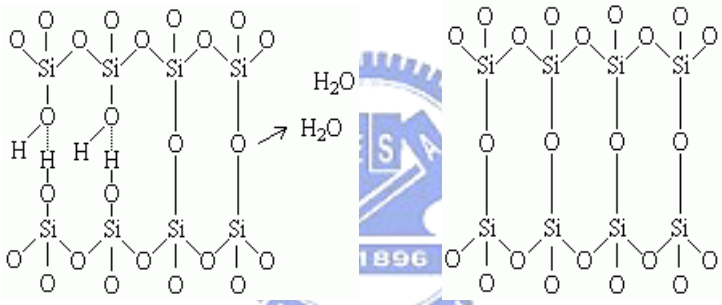


Fig. 7 Molecular water is driven out by high temperature

When annealing in 1000°C or greater, oxygen will be eliminated by diffusion and Si-Si bonds forms. Bonding strength of fusion bonding can up to 20 MPa. [6]

1.2.2 Anodic Bonding

Anodic bonding, also known as field assisted bonding, was used in high vacuum seals for vacuum tubes in the early beginning. Pomerantz showed that metal-glass bonding could be achieved in much lower temperature whole applying high electric fields [7]. The theory of anodic bonding is still unclear, but some believe that positive mobile ions (Na^+) in the glass drift toward cathode under high electric field and elevated temperature [4]. The migration of sodium ions producing huge

electrostatic force at silicon/glass interface.

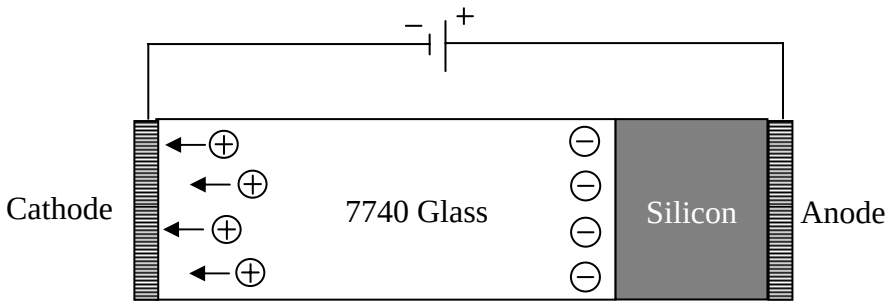


Fig.8 Sodium ions migrate to cathode, negative ions in the glass form a space charge layer adjacent to the silicon surface

This electrostatic force pulls two surfaces together, reducing the high temperature needed for silicon/glass bonding. Normally, silicon and glass are heated to 400°C while 1000V electric potential is applied. At these temperature and high electric field, chemical reaction is presumed to occur and two surfaces are bonding together.

The major difficulties of silicon/glass anodic bonding are the mismatch of coefficient of thermal expansion, or called CTE. CTE mismatch will cause serious residual thermal stress, which causes glass or silicon substrate cracking or shifting of device performance. Corning 7740, Hoya SD-2, and Schott 8330 are the most frequently used glasses for anodic bonding which have the closest CTE to single crystal silicon.

1.2.3 Eutectic Bonding

By taking the advantage of solid solubility of silicon and other materials, it is possible to bond two substrates together at eutectic temperature, this method called eutectic bonding. The most common material used in eutectic bonding is gold. Gold-silicon binary system has the eutectic temperature about 363°C, this

characteristic is especially welcome for temperature sensitive material bonding.

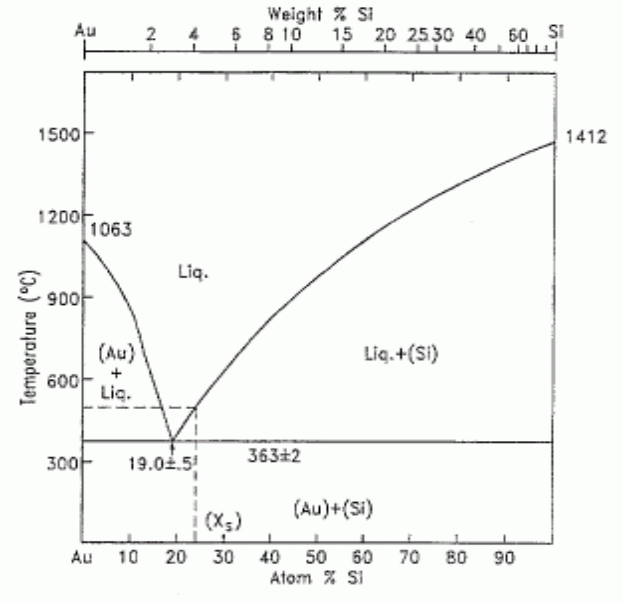


Fig.9 Silicon-Gold phase diagram [8]

About 19% silicon is dissolved in the eutectic silicon-gold compound at 363°C, After cooling, a reliable bond is obtained, bringing two substrates into direct contact. This technique is widely used in die bonding. [8]

1.2.4 Solder Bonding

Solder bonding utilizes alloys with low melting point to bonding two different surfaces together. With sufficient heating, these alloys melt into liquid and join two different substrates together. Sn based alloys such as In/Sn, Au/Sn, Pb/Sn are the must common material for solder bonding. Other low melting point metal such as aluminum is also used for wafer bonding.

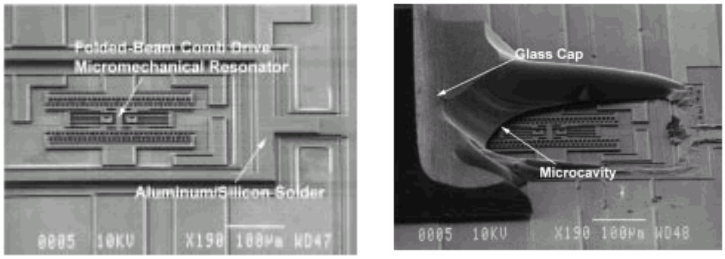


Fig.10 Solder bonding using aluminum by localized heating [15]

1.2.5 Adhesive Bonding

Adhesive bonding utilizes epoxy or photoresist to bond two substrates. These polymers are applied to the substrate through spin coating, and then patterns are defined by ordinary exposure and development process. With proper heat treatment and pressure, polymer is cured and forms strong bonds between two substrates. Normally, adhesive bonding can be performed under much lower temperature than most bonding procedures, often below 300°C.

Many polymers are used for wafer bonding. Epoxy or Teflon type materials are also used, such as SU-8 negative photoresist, BCB (bisbenzocyclobutene) of Dow Corning, and CYTOP of Asahi Chemical. These materials show good resistance toward heat and various chemicals.

1.3 Present Approach

Fusion bonding shows excellent hermeticity and bonding strength. But high processing temperature have made it unsuitable in many applications. Due to thermal budget limitation, high temperature annealing process is undesired for most electric circuit. Anodic bonding can be done under much lower temperature, but high voltage bias during the bonding process may induce dielectric breakdown, circuits need well isolation before anodic bonding. Also, both fusion and anodic bonding are quite surface roughness sensitive [9], surface roughness must less than a few angstroms to avoid bonding fail locally. This characteristic makes some features like interconnections are almost impossible.

For gold eutectic bonding, one of the major problems is large area bonding. Any native oxide on silicon surface will cease eutectic bonding to exist. Another

trouble is that gold is unwelcome in active devices. Gold will result in severe reduction of the minority carrier lifetime in integrated circuits. [8]

Solder bonding can be achieved under lower temperature and less surface roughness sensitive. However, many metals do not intimate with silicon or silicon dioxide, additional adhesion promoter or adhesion layer is necessary. Another problem is the reflow of liquid metal. When solder melts to liquid phase, it may flow toward unexpected region and damage device. Well constraints for solder may need.

Adhesive bonding by using UV definable polymers can solve many bonding problems. This bonding procedure is surface roughness insensitive, low temperature, less reflow during annealing. It is a good choice for low temperature, quasi hermeticity packaging. But must of the adhesives contain solvents, and they will outgas during curing process. Also, the links between monomers is weak than metal bonds, these two characteristic made it unsuitable when vacuum package is necessary. Adhesive bonding still needs to heat to above 130°C[], this temperature still too high for biochemical materials or plastic.

Bonding Techniques	Advantages	Drawbacks	
Fusion	Hermetic, Strong Bonding	High Temp.	Surface Roughness Sensitive
Anodic		High Voltage	
Eutectic	Strong Bonding	Flat, clean surface required	
Solder	Hermetic, Strong Bonding	Solder flow possible	
Adhesive	Low Temp.	Poor long term reliability	

Table 1. Comparisons of different bonding process

Here, a novel wafer bonding technique by using UV curable adhesive will be investigated. Unlike must adhesives cure by heating, UV curable adhesive, on the other hand, cures through UV light exposure with correct wave length and dosage. This process needs no heating, eliminates all of the drawbacks induce by heat, such as thermal stress problems. This feature will especially welcome for temperature sensitive materials, for example, plastic or biochemical compound. Also, by increasing UV light intensity, curing process can be done in seconds. Fast and low processing temperature characteristics have made these polymers more and more attractive in many fields. For example, protective coating of CD-ROM disks, medical syringe needle sealing and DVD disk bonding. High through put, low temperature wafer level package by using UV curable adhesive provides an alternative choice for MEMS package.