國 立 交 通 大 學

材料科學與工程學系

碩 士 論 文

研究藉由氧化鋁為閘極絕緣層來改善成長於矽基板上之氧化鋁鎵/氮化鎵高電子遷移率電晶體之線性度

Study of AlGaN/GaN MOS-HEMTs on Silicon Substrate with Al$_2$O$_3$ Gate Insulator for Device Linearity Improvement

研 究 生：陳玉芳

指導教授：張翼　博士

中 華 民 國 一 百 年 十 月

研究藉由氧化鋁為閘極絕緣層來改善成長於矽基板上之氧化鋁鎵/氮化鎵高電子遷移率電晶之線性度

Study of AlGaN/GaN MOS-HEMTs on Silicon Substrate with Al_2O_3 Gate Insulator for Device Linearity Improvement

研究生: 陳玉芳　　　　　　　　　　　指導教授: 張翼　博士

國立交通大學材料科學與工程學系

摘要

近年來，氮化鎵高電子移動率電晶體具有優越的特性使其在高功率，高溫，高崩潰偏壓以及高頻應用有很大的潛力。然而在高功率無線通訊遇到關鍵性難題，就是以複雜調變技術來達成高速率傳輸的目的時，此調變技術會導致動態訊號的產生，進而造成訊號失真，因此在射頻功率放大器中，元件線性度成為無線通訊系統中一項非常重要的參數。在本研究中，金氧半氮化鎵高電子移動率電晶體與一般傳統的蕭基閘極氮化鎵高電子移動率電晶體相較，擁有較好的元件線性度特性與較高的通道飽和電流。本研究成功製作出 1.5 微米閘極線寬的三氧化二鋁金氧半氮化鎵高電子移動率電晶體，並且將其電性分析與一般傳統的蕭基閘極氮化鎵高電子移動率電晶體相比，證實元件在線性度上有顯著的改善。本論文研究顯示，三氧化二鋁金氧半氮化鎵高電子移動率電晶體能有效的增進元件之線性度，有效地應用在無線通訊系統中的射頻功率放大器。

Study of AlGaN/GaN MOS-HEMTs on Silicon Substrate with Al$_2$O$_3$ Gate Insulator for Device Linearity Improvement

Student: Yu-Fang Chen   Advisor: Dr. Edward Yi Chang

Department of Materials Science and Engineering

National Chiao Tung University

Abstract

Superior properties of AlGaN/GaN HEMTs are promising contenders for high-power, high-temperature, high-breakdown, and high-frequency applications and have attracted much attention recently. However, one of the key issues for using AlGaN/GaN HEMTs for high-power radio-frequency (RF) applications is the quality of the transiting signals. For the modern wireless communication, here are many users, and the neighboring frequencies are usually located closely to each other. Hence, it is important to suppress the signal distortions for the device used in the communication system could not induce signal distortions. A among all intermodulation distortions, third-order intermodulation distortion (IM3) usually cannot be filtered out by the filter; therefore, IM3 dominates the linearity performance of the device and is the most important linearity criteria for wireless communication system. In this study, it's found that MOS-HEMT exhibits better linearity and higher channel saturation current compared to the HEMTs with Schottky-gate. In this paper, we present the linearity characteristics of the Al$_2$O$_3$ AlGaN/GaN MOS-HEMTs on Si substrates with gate length 1.5μm, and compare it with the regular AlGaN/GaN HEMTs devices for device linearity improvement in this study.

誌謝

碩士班兩年的時光，有開心瘋狂大笑，也有遇到挫折低潮到真思考休學，回頭想想，真慶幸我熬了過來。在張翼老師的帶領下，我們猶如在業界，快速的學習與成長，學了製程所需的所有機台，體驗到團體生活。從不熟陌生，到熟稔，這些是在別的實驗室無法獲得與體會的。一路過來，謝謝幫助過我的人，謝謝曾經有的挫折，謝謝張翼老師努力不懈研究爭取實驗室資源，還有耐心的幫我們即將畢業的學生一頁頁修改我們的論文。謝謝林岳欽學長一路以來的指導與幫助，陪我們熬夜量測，事事替我們著想，還犧牲假日來當我的口試委員。也謝謝 Fiaz 的幫助讓我成功的換組，沒有你我想我應該碩班當博班念吧...更謝謝一路一起奮鬥過來的黃大頭跟阿澤，沒有你們的陪伴與幫助，我想我做實驗真的會很無聊跟孤單。尤其謝謝明明已經畢業的黃大頭有情有義留下來，幫我與阿澤，幫我們改論文、量測、畫圖，還一起熬夜。我真的非常非常感謝你唷!謝謝阿澤一路上的包容與耐心，雖然你後來見色忘友的很厲害，我還是很謝謝你唷~謝謝幫我長氧化層的 Dang，如果不是你精湛的長成技術，我是無法有如此好得數據可以畢業。也謝謝我以前的指導教授倪澤恩老師，沒有你，我真的無法考上交大，謝謝你在我最低潮的時候總是耐心的開導我，告訴我該如何做。謝謝王人正學長，當初大學時候研究訓練，與高壓下的學習，總是刀子嘴豆腐心的帶領我們，真的萬般的感激你！你結婚的時候我一定會包大包一點啦!謝謝我的正妹室友林妍君，沒有你的陪伴與貼心的關懷，我想我真的會悶到爆炸!希望你早日找到如意郎君!謝謝我的家人一路上無條件的相挺與包容我的壞脾氣，還讓我無後顧之憂的念書，我會趕快出去賺錢回饋你們的^^!謝謝劉臭臭一路上包容我的壞脾氣，還耐心聽我抱怨與帶我去出飯，即使我在怎麼任性還是會願意挺我與聽我抱怨。謝謝老皮、阿伯當初的教導，沒有你們那兩個月紮實的訓練，我無法成為機台小天后!謝謝林芝羽總是無條件的挺我替我擔心，我真得很高興能夠遇到你這樣的麻吉!我們再一起去土地公還願吧!以後還是可以常打給我唷!要堅強不要傻傻被欺負唷~謝謝阿韋賤賤的關懷與貼心叮嚀、謝謝宗運學弟的體貼與諒解，讓我無後顧之憂的專心

弄論文。謝謝長褲學弟的幫忙與協助，讓我跟阿澤可以專心的準備口試。謝謝一路玩耍瘋狂的婉儀、林緯、佑誠，沒有你們，我碩一生活無法如此的精彩與快樂、謝謝哲榮一路上的相挺與關懷，明明是學長，卻總是被我兇…謝謝已經畢業的凱麟與培維，與你們相處的時光真的很歡樂。凱麟的包容與冷靜的解析給我意見，恭喜你交到人生第一個女朋友!好感謝電子所418陪我走過來的所有人，謝謝你們總是忍受我聒噪吵鬧。謝謝張俊彥校長，默默的縱容我與關心。謝謝張嘉華學長，總是幫忙我預約量測、沒我聊天打屁、在我口試前一天晚上還幫忙我修改投影片與畫圖。謝謝延儀每次都在我報告的時候幫我修改英文文法，還有忍受我三不五十的找麻煩。謝謝大家雖然總是嗆我、損我、卻又總是在我傷心難過的時候，無條件的挺我與幫我。謝謝總是被我機車態度激到快發瘋其實很貼心又細心的谷銘、謝謝細心與貼心總是笑笑的庭維、謝謝一臉認真講話很好笑的智翔，謝謝看起來臉臭臭可是很讚的學弟宗運，我真的沒有覺得你很不好啦!你們真得很乖唷!颱風天還願意來學習。以後要好好加油努力喔!謝謝我的麻吉黃老人，總是在我低潮難過陪我聊天，還努力幫我物色好男人。謝謝太多要謝謝的人，謝謝你們！如果沒有被我提出來，不代表我沒有謝謝你們喔!不要生氣呢!!謝謝大家~我終於終於可以下台一鞠躬囉~喔耶喔耶!!!!

Contents

Chapter 1

Introduction

Chapter 2

AlGaN/GaN Metal-Oxide-Semicomductor HEMTs

Chapter 3

Fabrications of AlGaN/GaN MOS-HEMTs with Al_2O_3 High-K Gate Oxide

Chapter 4

Fundamentals of HEMT Electrical Characteristics

Chapter 5

Study of AlGaN/GaN MOS-HEMTs on Silicon substrate with Al$_2$O$_3$ Gate

Insulator for Device Linearity Improvement

Chapter 6

Conclusion

Table Captions

Figures Caption

Chapter 3

Chapter 4

Chapter 5

Chapter 1

Introduction

1.1 General Background and Motivation

The wide spread communication systems such as third-generation (3G) mobile systems, wireless LAN, electronic toll collection system (ETC), and global positioning system (GPS). Recently, wide band-gap semiconductors have attracted considerable attentions as the next generation materials for RF power electronic applications such as mobile, satellites, and cable TV systems[1] for power transmitter applications. In the mobile communication applications, the next generation cell phone need, widen bandwidth and higher efficiencies; also, the development of satellites communication and TV broadcasting systems also require amplifiers which can operate at higher frequencies and higher power. Because of these demands, the outstanding properties of AlGaN/GaN HEMTs make them most promising candidate for microwave power applications in the wireless communication. Some of the commercial and military markets that are targeted by GaN devices are shown in Fig. 1.1.

However, for the microwave monolithic integrated circuits (MMICs) for power applications, a major problem is to increase the operating frequency. One of the major factors limited the performance of the GaN HEMT devices is the high gate leakage current due to the surface defects of the devices and finite barrier height of the Schottky gate. This gate leakage problem becomes more serious when dealing with high-power and high-temperature RF applications. For this reason, to improve the device high frequency performance, the lowest

possible gate leakage current level must be achieved. The use of high-k gate insulator for AlGaN/GaN MOS-HEMT can significantly suppress the direct-tunneling gate current.

In the past few years, many studies regarding of about the III-V/high-k interface issues have been published. It is well known that the surface pretreatment including sulfide and ammonia solution treatments could eliminate the undesired particles and native oxides. Furthermore, the surface of III-V material could be passivated by the treatment to prevent the surface exposed to air. With the progress of advanced deposition technologies, many passivation methods had been reported including Gd_2O_3/Ga_2O_3 or SiN_x as gate insulators, the Al_2O_3 growth by atomic layer deposition (ALD) [2-4]. Among all the deposition technologies, the ALD shows superior characteristics for oxides deposited. ALD has several advantages over other techniques due to the actual mechanism used to deposit the films. ALD is especially advantageous when film quality or thickness is critical. ALD is also quite effective to be deposited at coating ultra high aspect ratio substrates or substrates that would be difficult to coat with other thin film techniques. It can achieve the high purity level than any other deposition technologies. In this study, the ALD system was used for the high-k oxide deposition.

The main purpose of this study is to establish the AlGaN/GaN MOS-HEMT devices technology with low leakage current for high power, high frequency applications. The technology include the applications of ALD Al_2O_3 with a high insulator constant (8.6-10) and a high breakdown field (5~10 MV/cm) for the gate insulators for AlGaN/GaN MOS-HEMTs. The RF and DC performances of the AlGaN/GaN HEMTs with gate oxide in this study will be evaluated in this thesis.

1.2 Organization of the Thesis

This thesis is comprised of six chapters including conclusions. After background introduction, the GaN material properties and operation principle of HEMTs will be introduced in chapter 2. The AlGaN/GaN MOS-HEMTs device fabrication process is introduced in chapter 3. In Chapter 4, the electrical characterization methods for AlGaN/GaN MOS-HEMTs are described. Chapter 5 is the experiment results and discussion of the performance AlGaN/GaN MOS-HEMTs on Si substrate compared to regular HEMT. Finally, the conclusions will be given in chapter 6.
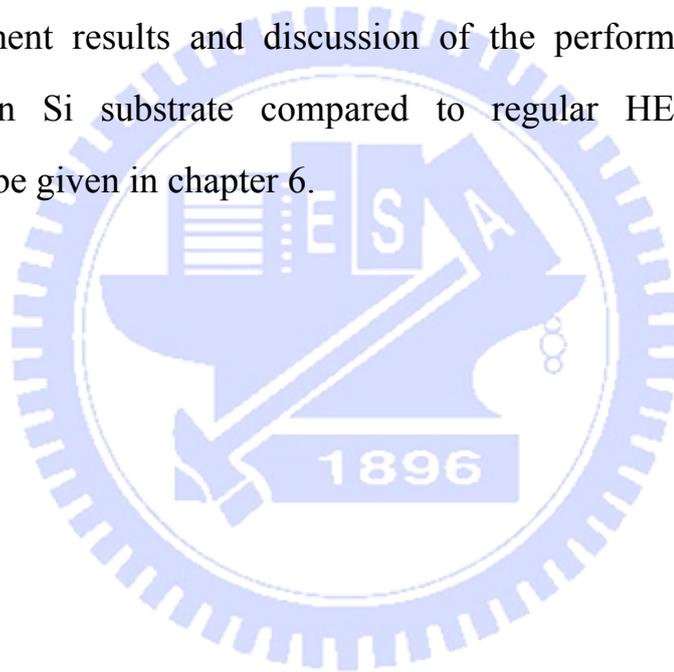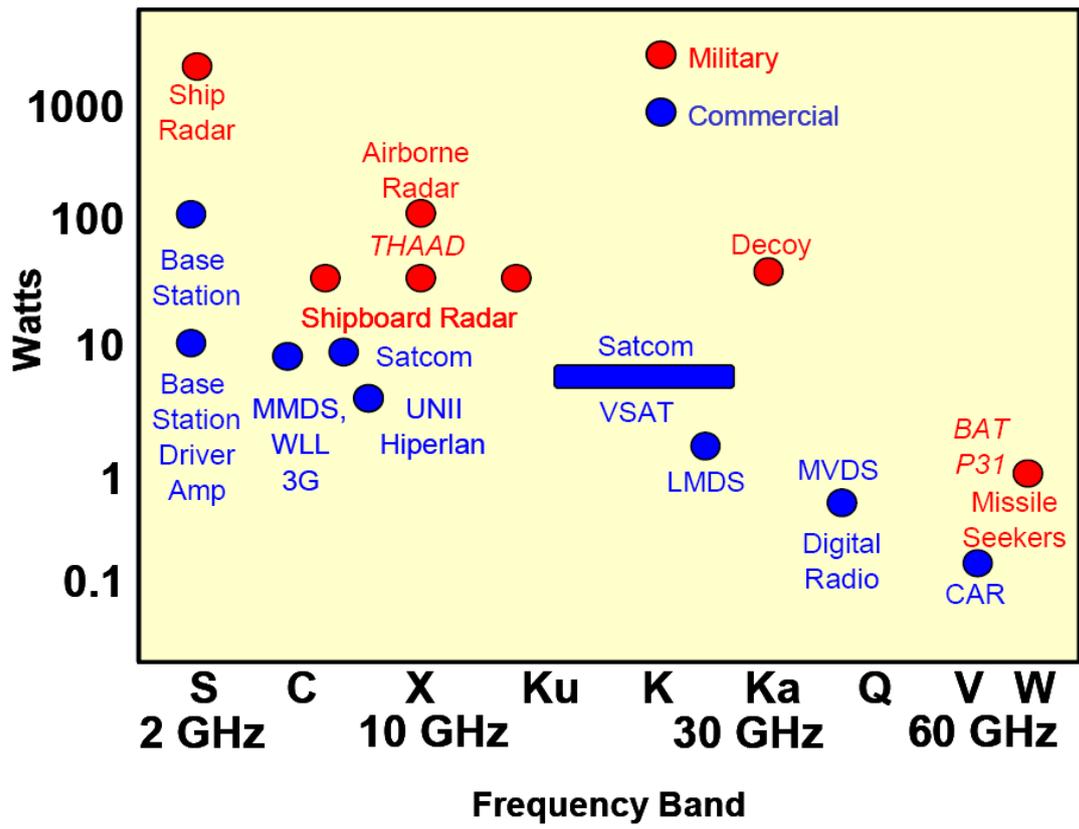
Fig. 1.1 Commercial and military markets targeted by GaN.

Chapter 2

AlGaN/GaN Metal-Oxide-Semiconductor HEMTs

An overview on GaN material and AlGaN/GaN HEMTs will be presented in this chapter. Material properties of GaN, especially the unique characteristics for electronic applications are introduced first. This is followed by a brief description of the polarization effect of GaN, along with AlGaN/GaN HEMTs. Thereafter, the AlGaN/GaN MOS HEMT, which is the focus of this study, is discussed. The historical approaches for the gate insulator of GaN MOS devices are reviewed and the device advantages of MOS-HEMTs over Schottky-gate HEMTs are highlighted. Finally, the basic operation and the non-ideal phenomena of MOS HEMTs are introduced.

2.1. Material properties of GaN

GaN-based materials, GaN, indium nitride (InN), and aluminum nitride (AlN), are wide bandgap semiconductors. They are the candidates for next generation high power devices. These materials have several advantages, such as high band gap, high electron velocity and high breakdown electric field. The bandgaps of GaN, InN, and AlN are respectively 3.4 eV, 1.89 eV and 6.2 eV, as shown in Fig 2.1. The figure not only shows the wide range of energies of III-V nitride materials, but also shows the wavelengths from the visible-light to the ultraviolet (UV) regions if they are used for optical devices. Thus, three-nitrides are good candidates for optoelectronic devices, such as light emission diodes (LEDs), laser diodes (LDs), detectors, and so on.

Compared with other III-V semiconductor materials, GaN gains a considerable attention for the RF power application. Fig. 2.2 compared the power vs. frequency performance of GaN in comparison with other semiconductors, and it indicates that III-V nitrides materials. GaN are promising candidates for the RF power application. Besides, due to the strong bonding energy between the Ga and N, GaN has a high breakdown field at about 3.3 MV/cm, which means the GaN devices can withstand high operating voltage. Although GaN has the lower room temperature electron mobility around 1500cm^2/Vs than that of GaAs, GaN has very high electron saturation velocity about 3×10^7 cm^2/s. This suggests the high frequency applications of the GaN-based devices. Moreover, GaN has a high thermal conductivity around 1.3 W/cmk, this makes it possible to operate at high temperatures. The benefits of GaN for electronic applications are listed in Table 2.1. Table 2.2 and Fig 2.3 show the material properties and figures of merit of GaN compared with the competing material such as 4H-SiC, GaAs and Si. According to the outstanding material properties of GaN, GaN-based devices are the good candidates in high-power, high-frequency, high speed, and high-temperature applications.

2.2 Polarization effect of GaN

The polarization effects in GaN are due to two types, one is strain-induced piezoelectric polarization, and the other is spontaneous polarization. The strain-induced piezoelectric polarization is resulted from the lattice mismatch, and the spontaneous polarization is due to the noncentrosymmetry of the wurtzite GaN and large iconicity of the covalent GaN bonds. The crystal

structure induced polarization of GaN, then the strain-induced piezoelectric and spontaneous polarization, will be described in next section.

2.2.1 Crystal structure and piezoelectric polarization [5]

GaN-based materials have two crystal structure, hexagonal wurtzite structure and cubic zinc blends, as shown in Fig 2.4. Since there is no native GaN substrate, GaN-based materials are grown on the other substrate, such as sapphire and silicon carbide. Recently, GaN growth on Si substrate is well-explored. SiC and sapphire are hexagonal structure, and Si is diamond cubic structure. In general, if noncentrosymmetric compound crystals have two different sequences of the atomic layering in the two opposing directions parallel a certain crystallographic axes; crystallographic polarity along these axes can be observed. In early 90's, the role of nucleation layer was discovered, and (0001) GaN was growth on (0001) sapphire. After that, hexagonal GaN-based materials are widely used in LED and HEMT structure. These are two different growth directions lead GaN to nonequivalent surfaces of Ga- or N-faced. In Ga-face, the Ga atoms are on the top position of bilayers, corresponding to the [0001] polarity. On the other hand, in N-face, the N atoms are located on the surface of {0001}, corresponding to the [0001] polarity. Fig 2.5 shows two different crystal planes of hexagonal GaN lattice structure. According to the specific crystallographic polarities, GaN exhibits different chemical and physical properties.

2.2.2 Strain-induced piezoelectric and spontaneous polarization [5]

7

In case of Ga-face of GaN shown in Fig. 2.5, the spontaneous polarization P_{SP} direction is downward to the substrate. In the other word, the polarization in N-face of GaN in Fig. 2.5 is in opposite direction to Ga-face. In addition, GaN has piezoelectric spontaneous polarization P_{PE} result from the lattice mismatch between AlGaN and GaN. The P_{PE} can be calculated by piezoelectric constants e_{33} and e_{31}, elastic constants c_{13} and c_{33}, and the lattice parameters a_0, is given by equation.

$$P_{PE} = 2 \frac{a-a_0}{a_0} \left(e_{31} - e_{33} \frac{c_{13}}{c_{33}} \right) \tag{2-1}$$

where a is the lattice constant of GaN along a-axis, and a_0 is equilibrium value of lattice constant. $(a- a_0)/a$ represents the in-plan strain along a-axis. Since $\left[e_{31} - e_{33} \frac{c_{13}}{c_{33}} \right]$ is less than zero. For AlGaN, over the whole range of compositions, piezoelectric polarization is positive for compressive and negative for tensile barriers. On the other hand, the spontaneous polarization of GaN and AlN is negative. Fig 2.6 shows the directions of the spontaneous and piezoelectric polarization in Ga- and N- face strained and relaxed AlGaN/GaN heterostrucutre.

2.3 AlGaN/GaN HEMTs

2.3.1 Hetero-epitaxial growth of AlGaN/GaN HEMTs

Due to the lack of large-size and low-cost commercial-grade substrate, GaN materials are usually grown on the foreign substrates such as sapphire, Si or SiC. Table 2.2 shows some of the material properties of these substrates as compared

to the GaN and AlN layers. Generally, the lattice constants and thermal expansion coefficients of these substrates differ significantly (except SiC) from that of GaN. The first successful epitaxial layer layers of GaN were grown on Sapphire. However, the very large lattice mismatch (14.8%) and the difference in the thermal expansion coefficient between GaN and sapphire substrate cause the huge challenges in the grown of nitrides. As a result of these mismatches, large amount of dislocations are generated in the GaN film. The quality of the GaN film is therefore critically dependent on the ability of the transition layer (buffer layer) used to accommodate the stress generated from these mismatches. The commonly used buffer layers include low temperature GaN [6-7], AlN [8-10] or their variations [11-13]. Dislocations generated in GaN are mainly screw, edge and mixed TDs. In addition to the buffer layers, other approaches are also used to improve the crystal quality of GaN film such as the insertion of AlN interlayers [14] or Si delta-doping layer [15].

High crystalline quality GaN materials are usually grown by metal-organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) methods. MOCVD is famous for growing the LED-quality GaN and is also used to grow GaN materials for HEMT applications lately. The main advantages of MOCVD, as compared to MBE, are the high growth rate and high crystal quality even for the direct growth of GaN layers on the foreign substrates. Besides, MBE has also proven to be a promising technique to grow GaN materials for HEMT devices application [16-18]. The benefits of growing GaN by MBE include real-time monitoring of crystal growth with reflection high-energy electron deflection (RHEED), a carbon-free and hydrogen-free growth environment, a smooth surface, sharp interfaces and low point defect density. These attributes are important for achieving high quality materials for

9

HEMT devices. Table 2.3 lists some important developments on the electrical properties of AlGaN/GaN structure grown by MOCVD and MBE techniques.

Although these difficulties have been solved, the low thermal conductivity is still an unneglectable problem. Compared with sapphire, SiC has less lattice mismatch (4%) with GaN and very good thermal properties, which is nearly 10 times more than that of sapphire. Therefore, SiC is rather popular substrate. Yet, SiC is too expensive for commercialization. Recently, GaN HEMTs grown on Si substrate was been widely investigated due to lower material cost and compatible with Si technology for circuit integration.

2.3.2 The Basic Structure and Operation of AlGaN/GaN HEMTs

GaN materials for HEMT fabrication consists of a higher bandgap material, such as AlGaN [19] or AlInN [20], grown on the top of the GaN film as the barrier layer. The discontinuity in conduction bands between the two materials forms a 2-dimentional electron gas (2DEG) channel at the hetero-interface. Basic GaN HEMT structure and band diagrams are shown in Fig. 2.7. AlGaN/GaN HEMT 2DEG formation is totally different from GaAs HEMT. In AlGaAs/GaAs HEMT, the channel electrons come from the surface states in the AlGaAs. The electrons in the AlGaAs where driven into the GaAs layer, because the hetero-junction created by different band-gap materials. The formation mechanism of GaN HEMT 2DEG is due to the strong polarization effect and large amount of surface states. High electron density ($\sim 1.5 \times 10^{13}$ cm^{-2}) can be induced at the 2DEG by AlGaN barrier layer with Al~25%, and high electron mobility (~ 2000 cm^2/V*s) can be achieved on an AlGaN/GaN heterostructure. Therefore, AlGaN/GaN HEMT does not require intentional

doping in the barrier to provide carrier in the 2DEG channel. The 2DEG enables better electron confinement and less carrier scattering. Due to both high mobility and high carrier density, AlGaN/GaN HEMT device of high current density (>2 A/mm) has been demonstrated [21].

2.3.3 Issues of High Gate Leakage Current AlGaN/GaN HEMTs

Despite the impressive device performance, the potential of AlGaN/GaN HEMTs for commercial application have not been fully realized as yet. The RF power expected from fundamental nitride material properties significantly exceeds the experimental data. One of the key problems limiting the HEMT RF power is the high Schottky-gate leakage current, which results in the degradation of DC/RF parameters. At positive gate bias, high forward gate current can shunt the gate-channel capacitance, thus limiting the maximum drain current. At negative gate bias, high voltage drop between the gate and drain results in premature breakdown and the maximum applied drain voltage is restricted [22]. In addition, gate leakage currents increase the device sub-threshold currents, which decrease the achievable amplitude of the RF output. All these limitations become even more severe at high ambient temperatures. Mechanisms of the high gate leakage current in AlGaN/GaN HEMTs have been investigated and possible solutions to suppress the leakage have been explored in the past few years. Through numerical simulations and DC electrical measurements, Miller et al. reported, found that vertical tunneling through the gate area is the dominant mechanism for gate leakage in AlGaN-barrier HEMTs, while additional leakage current mechanisms such as lateral tunneling and defect-assisted tunneling also contributed to the total gate leakage [23]. To suppress the high gate current,

Miller et al. proposed an enhanced-barrier HEMT structure, in which a GaN cap layer was grown on the top of the standard AlGaN barrier. Owing to the strong polarization effects in the nitrides, the peak barrier height in the new GaN/AlGaN/GaN HEMT was increased, thus decreasing the tunneling gate leakage current. Mizuno et al. compared the gate leakage current of a GaN-based HEMT with a GaAs-based HEMT [24]. They observed both a two to three orders of magnitude larger gate leakage of the GaN-based HEMTs as compared to that of the GaAs-based HEMTs, and the temperature-independence for the gate leakage current in GaN-based HEMTs. Considering that AlGaN has a larger Schottky barrier height (1.4 eV) than GaAs HEMTs (~1.0 eV), the authors attributed tunneling to be the main leakage mechanism instead of the thermionic emission. They also found that surface treatment with CF_4 plasma prior to the gate metal deposition was able to reduce the gate leakage current by two to three orders of magnitude. A possible explanation of such leakage suppression is that the plasma treatment introduces deep acceptors to compensate the high-density positive charge on the AlGaN surface. Thus, the depletion layer thickness under the gate increases, and gate leakage current due to electron tunneling becomes small.

2.4 AlGaN/GaN MOS HEMTs

2.4.1 Introduction

As described above, device performance of conventional Schottky gate AlGaN/GaN HEMT device suffers from high gate leakage current. As a result,

the drain current collapse when operating at high-frequency and poor long-term reliability of Schottky gate. In order to reduce the gate leakage current, a concept of high-k insulators layers between gate metal and semiconductor were investigated in the past years. A schematic comparison between HEMT and MOS-HEMTs for AlGaN/GaN is illustrated in Fig. 2.8.

2.4.2 The requirements of high-k insulators oxide

(A) Insulator constant

Insulator constant is the most important parameter for oxide material used in the MOS structure. Due to the reduction of chip's size in the future, the horizontal electrical field is increased and the gate modulation ability is decreased. In order to solve these problems, the capacitance per unit area must be improved to decrease the effect of undesired electrical field.

$$C = \frac{Q}{V}$$ (2-2)

where C is capacitance, Q is charges, and V is turned on voltage.

$$C = \varepsilon_0 \varepsilon \frac{A}{d} \quad , \varepsilon \propto C$$ (2-3)

where ε is the insulator constant of oxide, A is cross section area, and d is the distance between the two plates. According to Eq. (2-2), the devices with larger accumulation capacitance can be turn on more easily by a smaller voltage. Using smaller operating voltage will result in higher device efficiency and cost saving. According to the Eq. (2-3), the MOS device which using oxide material with larger insulator constant as its gate insulator will have larger accumulation capacitance. So, the high-k oxide is desired for III-V MOS devices technology. The energy band gap versus insulator constants of different oxide materials is

plotted depicted in Fig. 2.9.

(B) Energy band gap

The energy band gap of oxide materials is an important factor which influences the leakage current of the MOS devices. The oxide with smaller energy band gap causes the carrier tunneling more easily; it will induce undesired leakage current and influence the devices performance. The oxide with larger energy band gap can prevent the carriers tunneling. But, the oxide with higher insulator constant will have the smaller energy bandgap. So, it is important to find the suitable oxide to improve the MOS devices performance. Several gate oxide candidates are listed in Table 2.4. Besides, the **band offset** of oxide on semiconductor material is also needed to be considered, the value must exceed 1 eV so that the oxide can serve an effective insulator[18].

ALD Al_2O_3 is introduced in this study due to its relatively high band gap (about 8.7 eV) and remains amorphous under typical processing conditions. In addition, Al_2O_3 also possesses high breakdown electric field (5~20 MV/cm), high thermal stability (up to 1000℃) and strong adhesion with dissimilar materials [25]. With well-controlled thickness and uniformity for the Al_2O_3 layer deposited by ALD technology by the good insularity of Al_2O_3 layer, ALD Al_2O_3 is the leading candidate for the gate insulators in MOS-HEMT device.

Table 2.1 Advantages of GaN material for electronic applications.

Material property	Advantages
Wide bandgap 3.42 eV	■ Great endurance for high device operating temperature ■ Suitable for high power applications. ■ Working under high temperature environment
+High breakdown field 4×10^6 V/cm	■ Larger power density
High thermal conductivity ~1.3W/cm* K	■ Better heat dissipation, enhanced device performance ■ Easier device packaging
High saturate electron velocity ~2.7×10^7 cm/sec	■ Suitable for high frequency applications

Table 2.2 Material properties and figure of merit (FOM) of GaN, 4H-SiC, GaAs and Si at 300K for microwave power device applications. All FOMs are normalized with respect to those Si.

Material	Bandgap Energy (eV)	Breakdown field (MV/cm)	Thermal conductively (W/K*cm)	Electron mobility (cm²/V*s)	High-field Peak velocity (x10⁷cm/s)
GaN	**3.40**	**4.0**	**1.3**	**1350**	**2.7**
4H-SiC	3.26	3.0	4.9	800	2.0
GaAs	1.42	0.4	0.5	6000	2.0
Si	1.12	0.25	1.5	1300	1.0

Table 2.3 Comparison of 2DEG mobility and sheet carrier concentration of AlGaN/GaN structure grown by MOCVD and MBE on different substrates. The carrier mobility and concentration are measured at 300, 77, 4.2 or 0.3 K unless specify in the bracket; x is the Al content in AlGaN layer.

Growth Method	substrate	Al content x	2DEG mobility (cm^2/Vs) (Sheet carrier concentration (n$_s$ (cm^{-2})))				Reference
			300K	77K	4.2K	0.3K	
MOCVD	SiC	0.2	2000 (1×10^{13})	9000 (8×10^{12})	11000 (7×10^{12})		Gaska *et al.*, (1999) [23]
	SiC	0.4	1990 (1.4×10^{13})				Higashiwaki *et al.*, (2008) [24]
	Sapphire	0.18				10300 (1.5K) (6.9×10^{12})	Wang *et al.*, (1999) [25]
	Sapphire	0.3	1300 (9.84×10^{12})				Liu *et al.*, (2006) [26]
	Sapphire	0.2	1700 (8.4×10^{12})				Tülek et al., (2009) [27]
	Silicon	0.26	1500 (8.2×10^{12})				Selvaraj et al., (2009) [28]
	Silicon		1800 (1×10^{13})				Arulkumaran et al., (2010) [29]
MBE	SiC	0.3	1500 (1×10^{13})				Corrion el al., (2006) [16]
	Sapphire	0.19	1500 (9×10^{12})	10310 (6×10^{12})		12000	Li *et. el.*, (2000) [12]
	Sapphire	0.3	1310 (1×10^{13})				Manfra et al., (2002) [10]
	Silicon	0.25	1500 (7.9×10^{12})				Dumka et al., (2004) [30]
	MOCVD-GaN/ sapphire	0.09		24000 (2.5×10^{12})	60000 (4K) (2.25×10^{12})		Elsass *et. al.*, (2000) [31]
	MOCVD-GaN/ sapphire	0.28	2039 (1×10^{13})				Cordier *et al.*, (2007) [32]
	HVPE-GaN/ sapphire	0.06				80000 (1.75×10^{12})	Manfra *et. al.*, (2004) [33]
	Dislocation free-GaN/ sapphire	0.1	2500 (2.6×10^{12})			109000	Skierbiszewski el al., (2005) [34]

Table 2.4 Comparison of the gate oxide's properties

Material	Dielectric Constant	Energy Band Gap(eV)	Crystal Structure
SiO_2	3.9	8.9	Amorphous
Si_3N_4	7	5.1	Amorphous
Al_2O_3	9	8.7	Amorphous
Y_2O_3	15	5.6	Cubic
HfO_2	25	5.5	Mono. , tetrag. , cubic
ZrO_2	25	7.8	Mono. , tetrag. , cubic
Ta_2O_5	26	4.5	Orthorhombic
La_2O_3	30	4.3	Hexagonal, cubic
TiO_2	80	3.5	Tetrag.
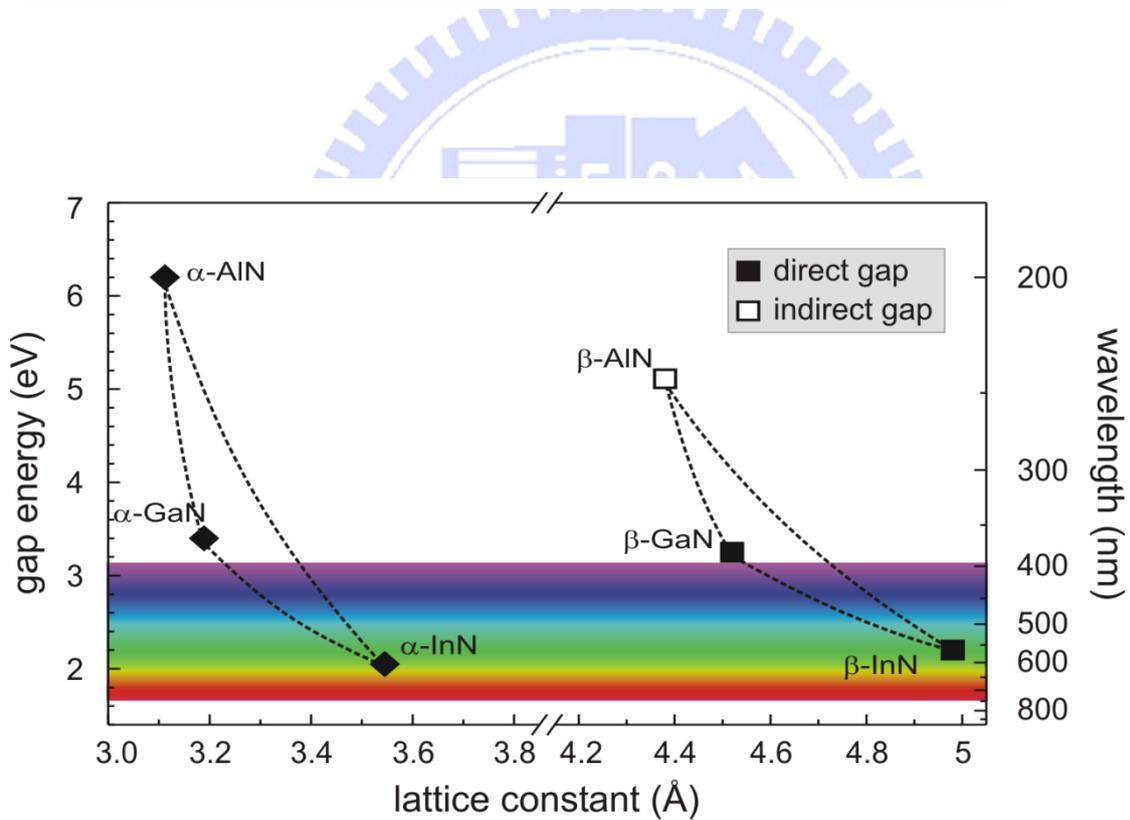
Fig. 2.1 Band gap (E_g) versus lattice constant at 300 °K for wurtzite (α-phase) and zincoblende (β-phase) GaN, InN, and AlN. The right-hand scale gives the light wavelength, corresponding to the band gap energy.

17
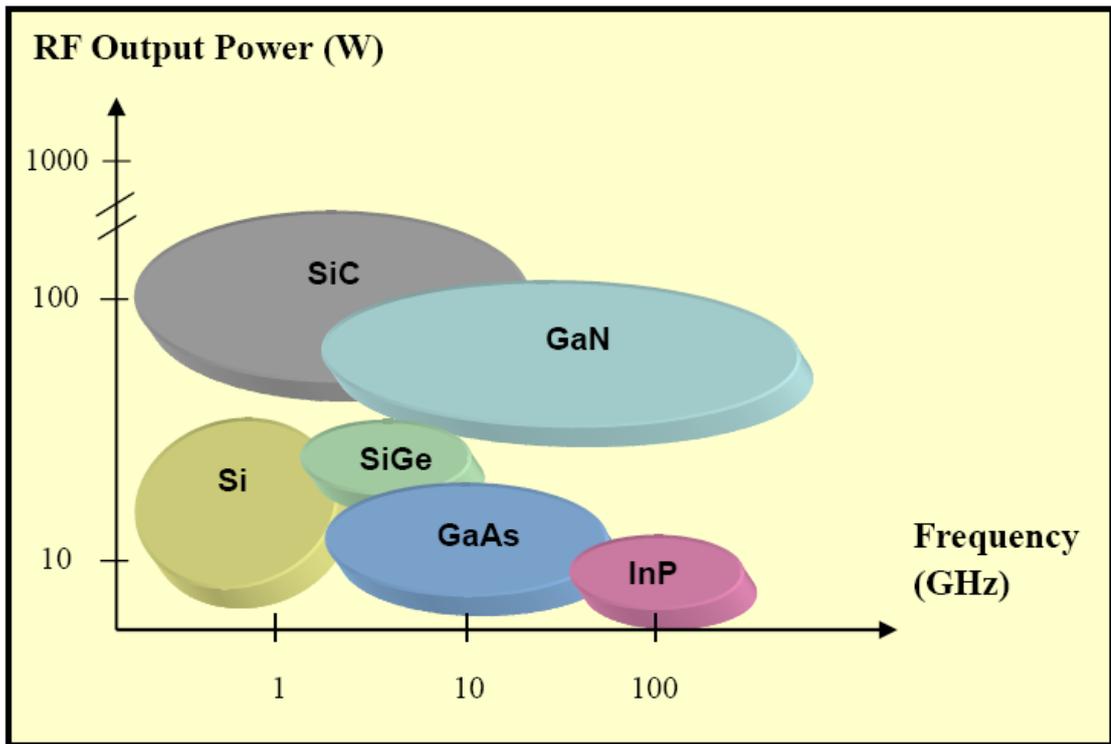
Fig. 2.2 Semiconductor materials for RF applications.
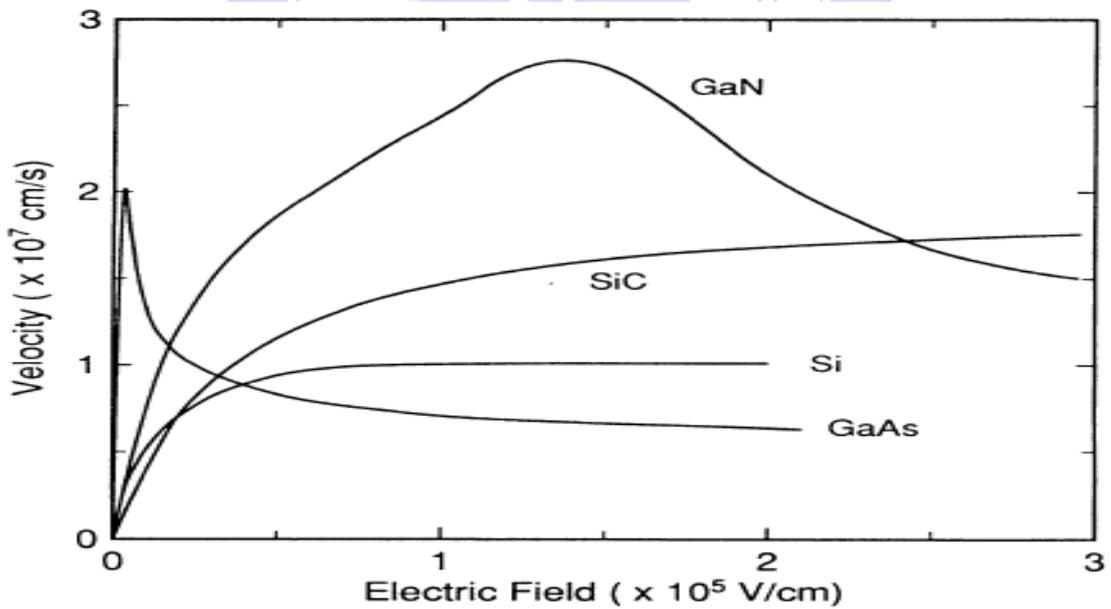
Fig. 2.3 Electron drift velocity of GaN, SiC, Si and GaAs at 300 K computed using the Monte Carlo technique.
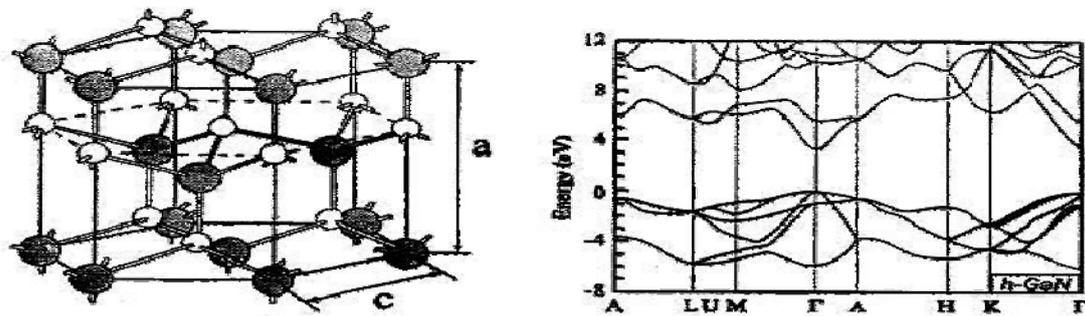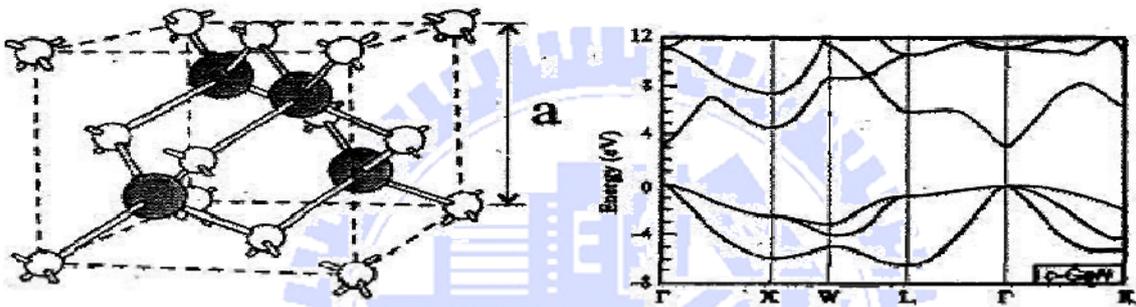
Fig. 2.4 Schematic drawing of the crystal and energy band structure of wurtzite GaN and Zinc Blende GaN.
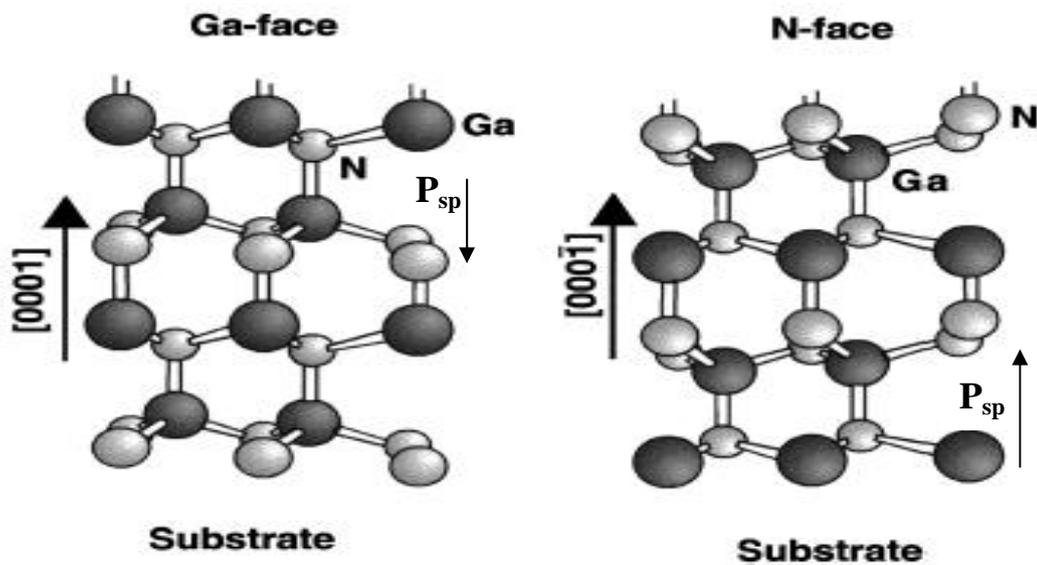
Fig. 2.5 Schematic of the crystal structure of wurtzite Ga-face and-face GaN. The spontaneous polarization (P_{sp}) direction is also shown.
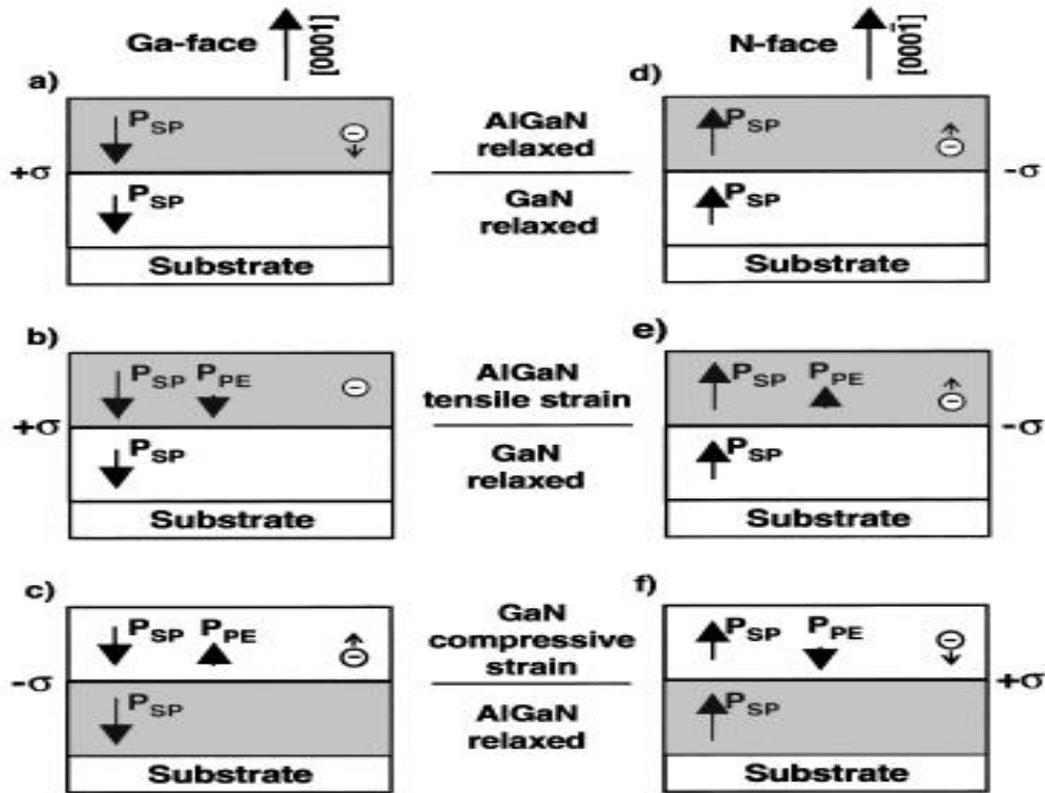
Fig. 2.6 Polarization induced sheet density and directions for the spontaneous and piezoelectric polarization in Ga- and N-face AlN/GaN heterostructures.
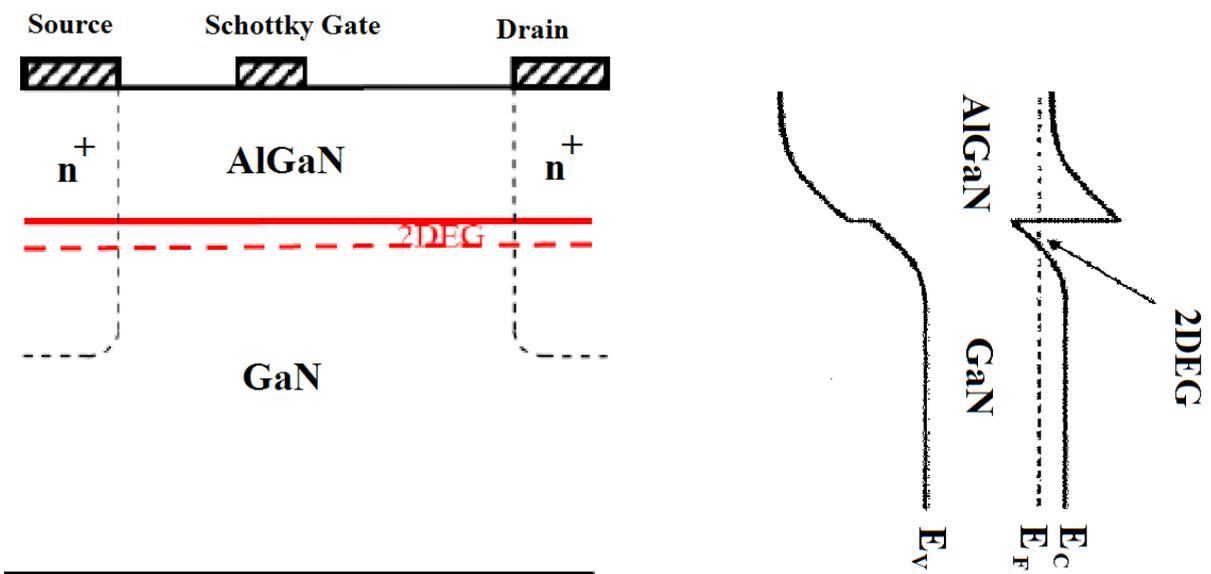
Fig.2.7 Basic structure and its band diagram AlGaN/GaN HEMT.
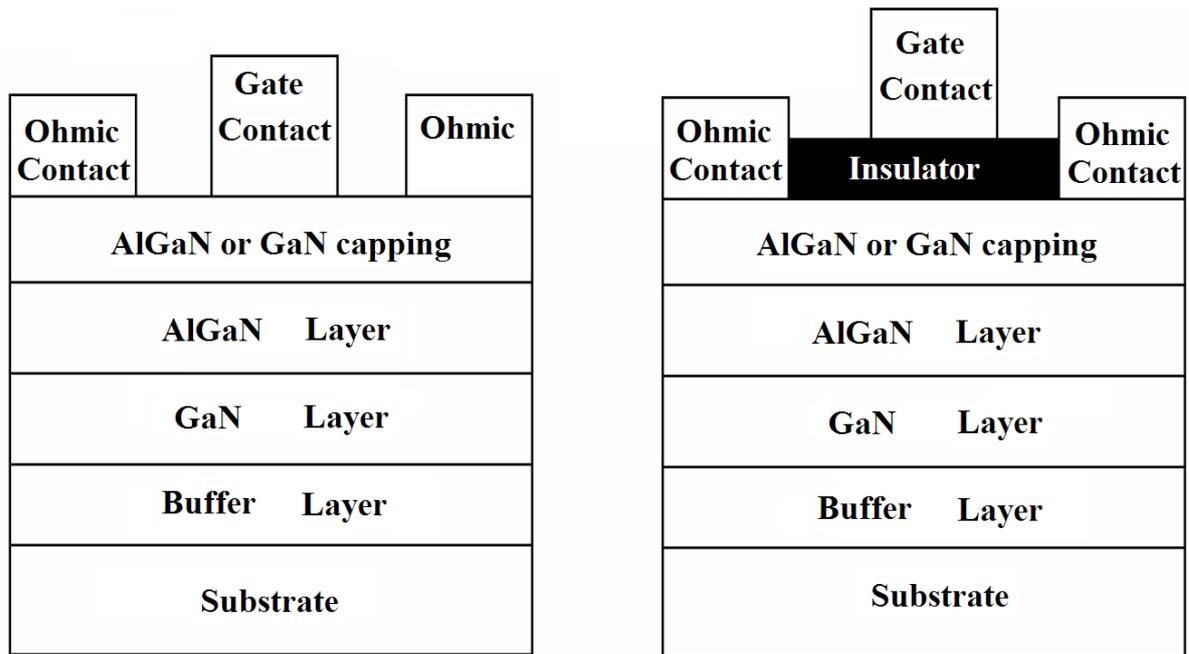
Fig. 2.8 Structure comparisons between AlGaN/GaN HEMT (on the left) and Al$_2$O$_3$ HEMT (MOS-HEMT) (on the right).
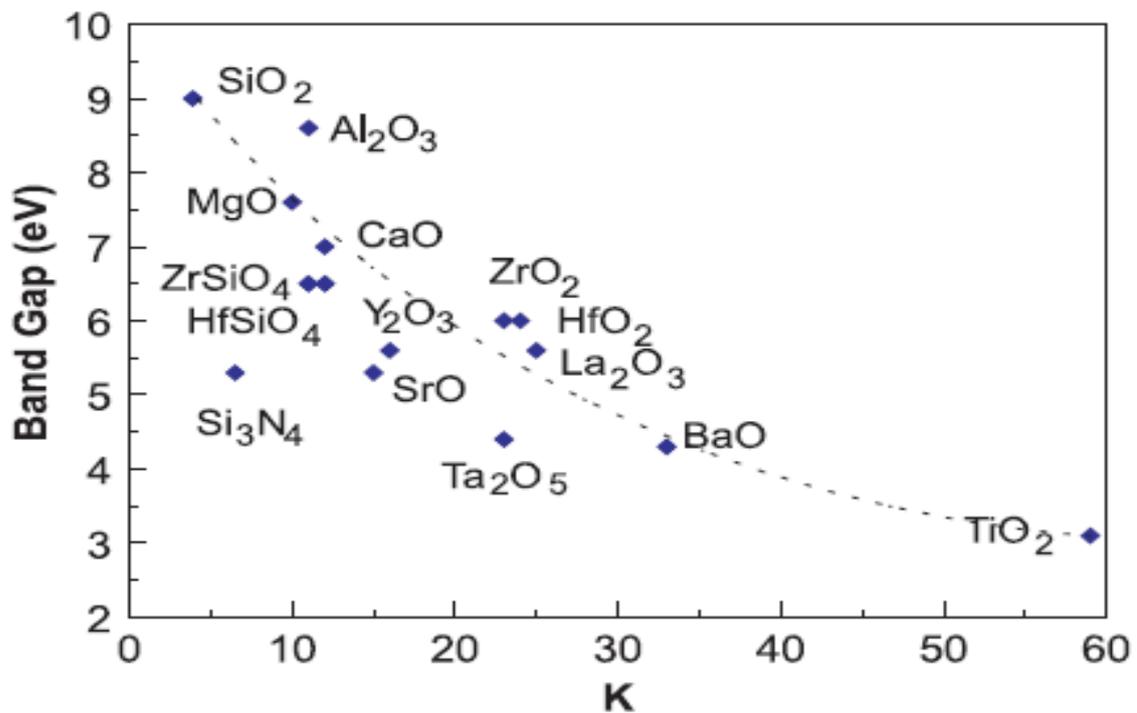
Fig. 2.9 Energy band gap versus Insulator constant diagram of oxides.

Chapter 3

Experimental Methods of AlGaN/GaN MOS-HEMTs with Al$_2$O$_3$ High-K Gate Oxide

The fabricated AlGaN/GaN MOS-HEMT with Al$_2$O$_3$ high-k gate oxide in this study brings together a novel design to enhance the electronic properties of the devices, the process flow of AlGaN/GaN MOS-HEMT with Al$_2$O$_3$ high-K gate oxide fabrication in this study includes several steps as shown in Fig 3.1, and they are:

1. Ohmic contact formation
2. Active region definition (Mesa isolation)
3. Atomic layer deposition (ALD) Al$_2$O$_3$
4. Gate formation

3.1 Ohmic Contact Formation

An ohmic contact is a low resistance junction formed in between metal and semiconductor. The purpose of an ohmic contact on semiconductor is to allow the electrical current to flow in and out of the semiconductor. A good ohmic contact is important for a better device performance such as lower power consumption, low noise and so on. An ohmic contact should obey the ohms law; that is, it should have a linear I-V characteristic either under forward or reverse bias. Therefore, to obtain a low resistance ohmic contact, we have to create a

heavily doped interface between metal and semiconductor. In addition, an ohmic contact not only should be stable over time and temperature, but also should have as small resistance.

First, the negative photoresist AZ5214E and I-line aligner were used to define the ohmic metal pattern after wafer cleaning by using ACE and IPA. Unlike the Si-based devices, the lift-off process is used for III-V based device because of the lack of appropriate etching selection between ohmic metals and III-V materials. The undercut profile of the negative photoresist AZ5214E will benefit the metal lift-off process. Then, the wafers underwent O_2 plasma descum to remove residual photoresist and the dipped in $HCl:H_2O$ (1:4) solution for 15 s to remove the native oxide on the GaN surface before Ohmic metallization. ohmic metal was composed of Ti/Al/Ni/Au from the bottom to the top, and it was deposited by e-gun beam evaporation system. Finally, tcontacts were annealed by rapid thermal annealing (RTA) at 850℃ for 30s in N_2 atmosphere after metal lift-off process as shown in Fig 3.1. The specific contact resistance was checked by the transmission line method (TLM) in the process control monitor (PCM). It containing a linear array of metal contacts with various spacings between them. The distances between TLM electrodes are 3 μm, 5 μm, 10 μm, 20 μm, and 36 μm, respectively in this study. In general, the typical measured contact resistance must be less than 1 x 10^{-5} Ω-cm^2.

3.2 Mesa isolation

For III-V devices, the mesa isolation is to isolated devices from each other. In these specific areas, the current flow is restricted to the desired path. In addition,

parasitic capacitance, parasitic resistance, and leakage current can all be reduced with effective isolation. A successful isolation provides sufficient insulating area to form passive elements such as transmission lines, capacitors, pads, etc.

First, the active areas were masked by Shipley S1818 photoresist, and then the dry etch process was conducted by inductive couple plasma (ICP) with Cl_2 in Ar ambient. After the dry etch process, the etching depth should reach the buffer layer as shown in Fig 3.3. Finally, the photoresist was striped by ACE. According to the device structure, the mesa was etched to the buffer layer to provide good device isolation. Finally, the etching depth was approximately 2500Å measured by p-10 surface profiler after the strip of photoresist, and the etching profile was carefully checked by scanning electron microscopy (SEM).

3.3 Atomic layer deposition (ALD) Al_2O_3

In this study, the Al_2O_3 was deposited by ALD system. ALD developed in Finland by T. Suntolan in 1974, and this method is considered as an advanced variant of the CVD technique.

Before the Al_2O_3 deposition, the chemical surface treatment was used to remove the surface native oxides. Firstly, the wafers were immersed by HCl : H_2O (1:4) solution to remove the native oxides, and followed by rinsing in the water for 30 s and blowing dry by N_2 gas. Then, the wafer was directly immersed in $(NH_4)_2S$ solution for 15 min at room temperate, and also rinsed for 30 s in water and blown dry by N_2 gas after $(NH_4)_2S$ treatment. After the chemical surface treatments, the wafer was loaded into the ALD chamber. The Al_2O_3 films (TMA/N_2/H_2O/N_2 with periods of 0.2s/5s/0.2s/5s) were deposited

over 50 cycles and the thickness Al_2O_3 was about 10 nm as shown in Fig 3.4. Finally, the post deposition annealing (PDA) was used to improve the interface quality. The PDA was performed at 400℃ for 5 min in N_2.

3.4 Gate Formation

Schottky barrier gate is one of the most important elements of the HEMTs. Both the dimension length and placement of the gate are very critical. For high speed and high frequency applications, short gate length is desired. Decreasing gate length (L_g) can increase the electronic field under the gate so as to accelerate the transport property of channel electron.

In this study, the 1.5 μm gate length was defined by AZ 2020 photoresist, and then the remnant photoresist was removed by ICP with Ar and O_2 ambient. Beside, the wafer was dipped into the $HCl:H_2O$ (1:4) solution for 15 s to remove the negative oxidation before the gate metal deposition. Here, the multilayer gate metals Ti/Pt/Au were deposited by the e-gum system. Finally, the wafer was immersed into the ACE for 30 min to lift –off the undesired metal, and the ICP was used to clean the wafer as shown in Fig 3.5.
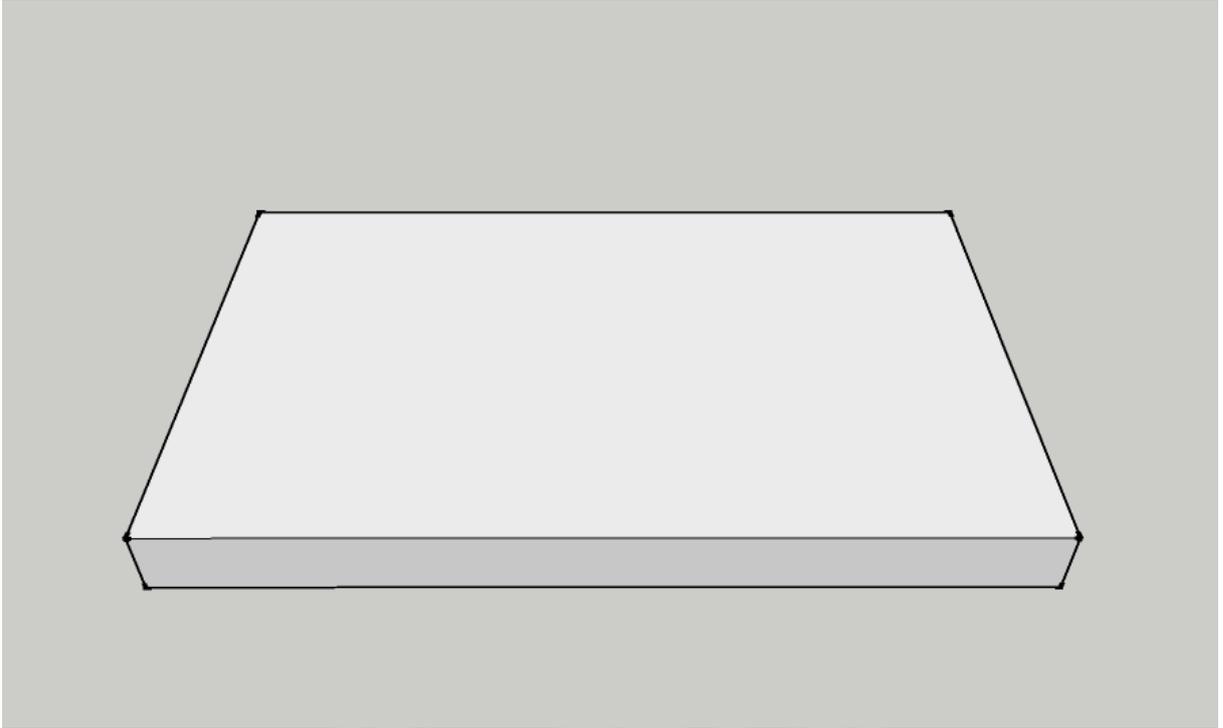
Fig. 3.1 the whole wafer
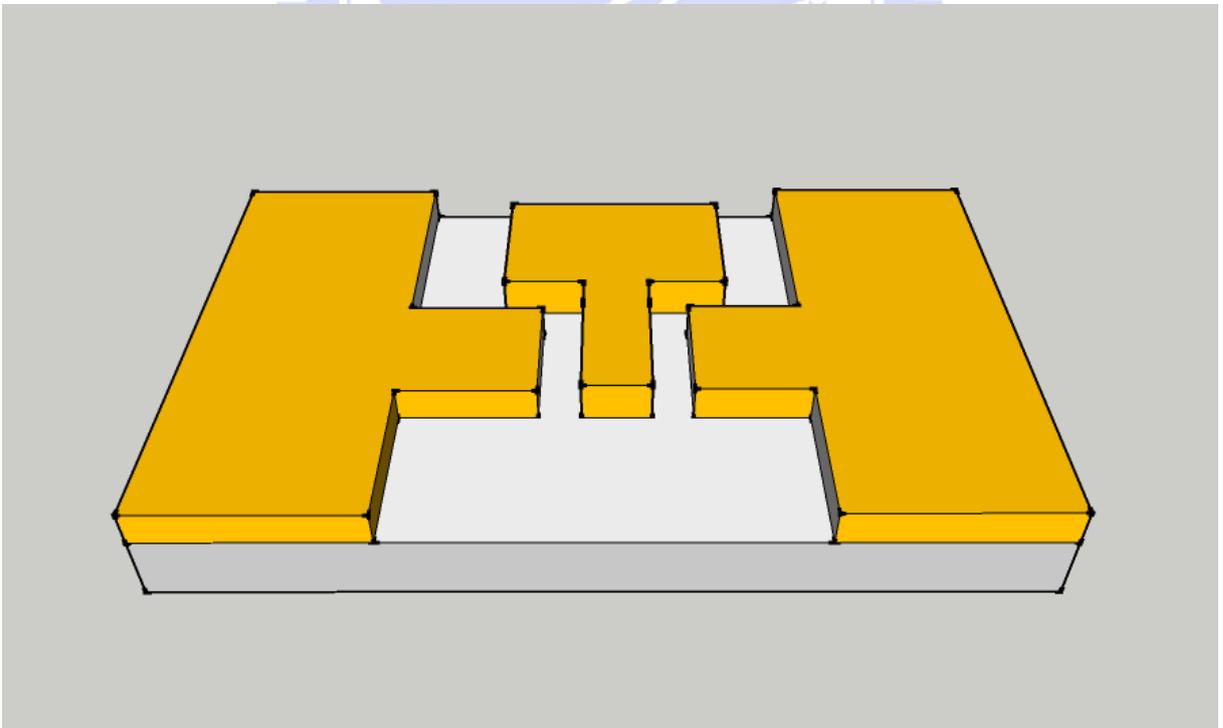
Fig. 3.2 Ohmic contact formation
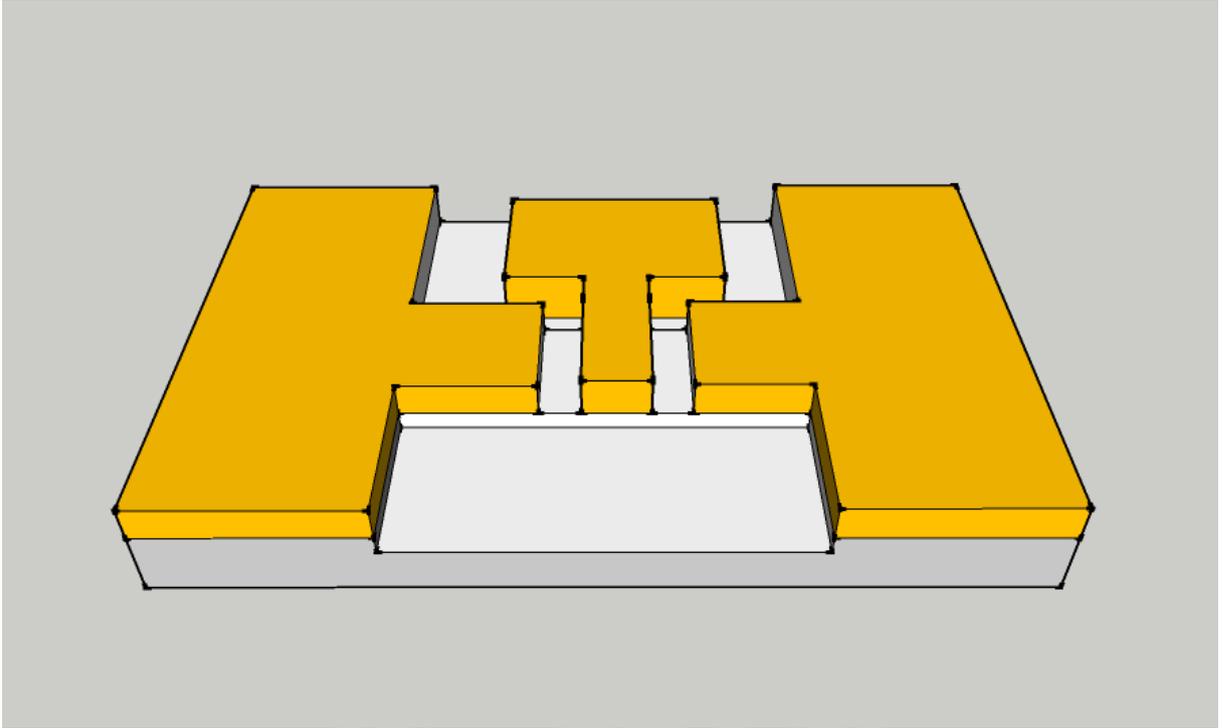
Fig. 3.3 Mesa isolation
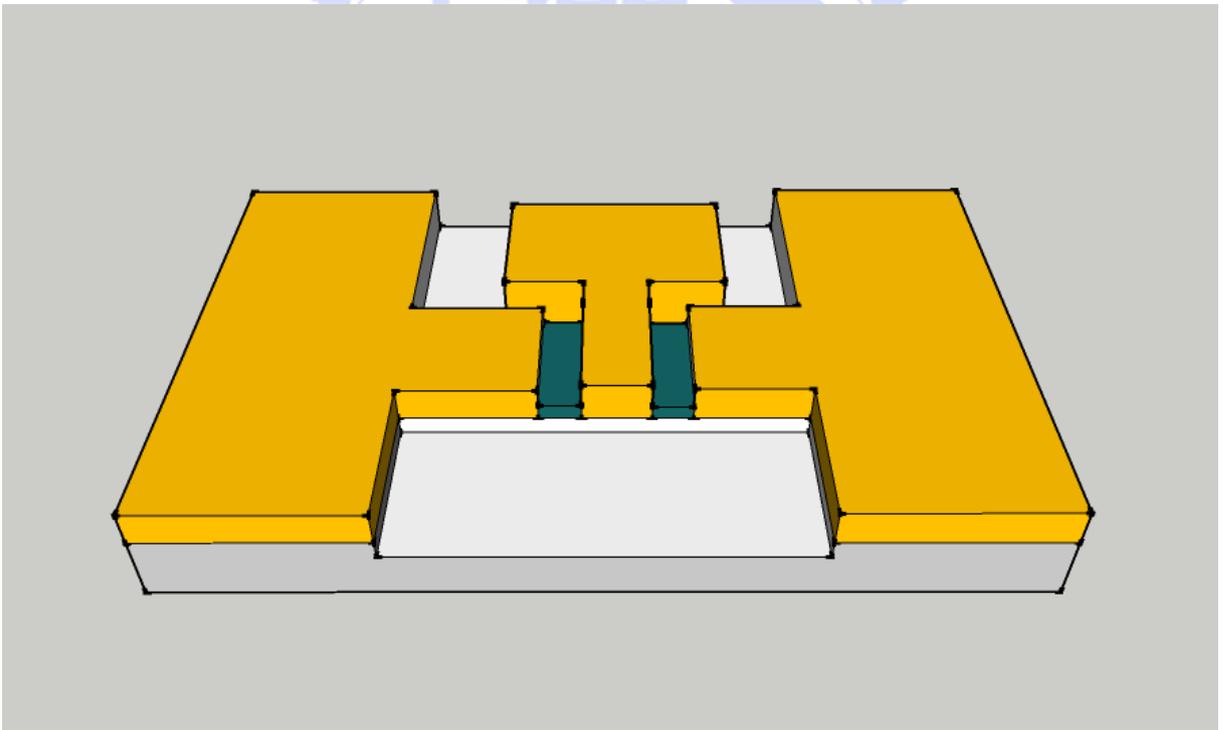
Fig. 3.4 Atomic layer deposition (ALD) Al$_2$O$_3$
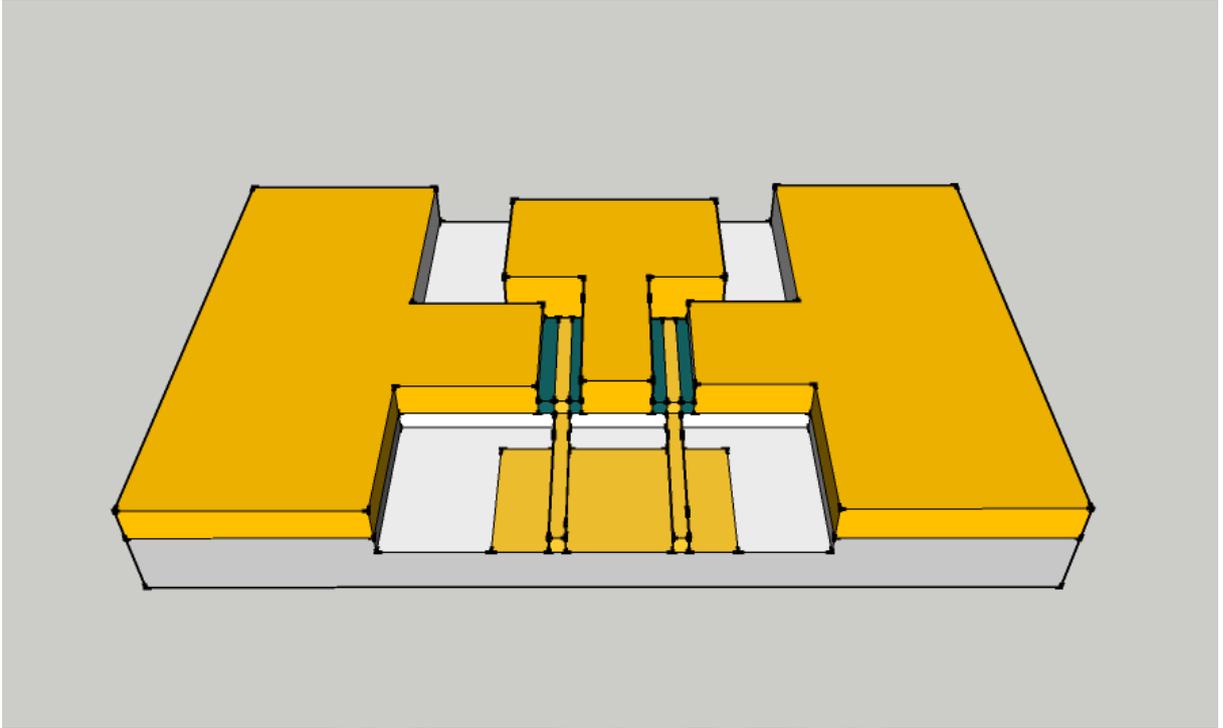
Fig. 3.5 Gate formation

Chapter 4

Fundamentals of Electrical Characteristization

After the device fabrication, DC and RF performances of the AlGaN/GaN HEMT and MOS-HEMT were evaluated by using on-wafer measurement. For the DC measurement, the I-V characteristics were obtained by using an HP4142B Modular DC source/monitor and SUSS PA200 semi-auto probe station. The TLM method was used for determining specific contact resistance was by the 4-wires measurement. The S-parameters were measured by HP8510XF vector network analyzer using on-wafer GSG probes from Cascade MicroTech. However, evaluating the RF behaviors of a device on a wafer was a complicated process. For conventional RF measurement of a packaged device, the wafer needs to be diced and then an individual die should be mounted into a text fixture. Discriminating between the die's and the fixture's responses became an issue. Furthermore, fixturing die was a time-consuming process, making it impractical for high-volume screening. On-wafer RF characterization can simplify the process [26].

The method of characterization of the AlGaN/GaN HEMT and MOS-HEMT devices are stated in the following section. In this study, de-embedding which must also be performed to obtain the true RF performance of the device is also performable.

4.1 DC Characteristics Measurment [27]

Before RF performance analysis, DC measurement was performed to

evaluate the device characteristics, including the saturation drain current (Id_{ss}), threshold voltage (V_{th}), transconductance (G_m), breakdown voltage (V_{BK}). For I_{DS}-V_{DS} curve, the drain voltage sweeps from 0 to 10V, and the gate voltage is from 1 to pinch-off voltage with a step of -1V. For I_{DS}-V_{GS} curve, the gate voltage sweeps from 6V to pinch-off voltage such as -8V for MOS-HEMT and -6 for Schottky-gate HEMT, and the drain voltage is from 4 to 15V. The measured breakdown voltage in this study is off-state breakdown voltage. The gate bias is pinch-off voltage, and the drain bias sweep from 0 to a specific value.

4.2 TLM Method

The specific contact resistance between contact metal and cap layer can be extracted by the TLM method [28]. The TLM pattern, as illustrated in Fig. 4.1, was designed in the process control monitor (PCM). In this particular approach, a linear array of contacts pad is fabricated with various spacing in between them. The distances between TLM electrodes are 3, 5, 10, 20, and 36 μm, respectively. The resistance between the two adjacent electrodes can be plotted as a function of the space between electrodes and is expressed by the following equation

$$R = 2R_c + R_s L/W, \qquad (4\text{-}11)$$

where R is measured resistance, R_C is contact resistance, R_S is sheet resistance of channel region, W is electrode width, and L is the space between electrodes. As Fig. 4.2 shows, extrapolating the data to L=0, one can calculate a value for the term RC. And the specific contact resistance ρ_C can be further extracted by the following formula.

$$\rho_C = \frac{W^2 R^2}{R_s} \qquad (4\text{-}12)$$

4.3 Linearity

Linearity of amplifiers is often assessed by the third-order intercept point (IP3). If an amplifier is presented with two signals closely spaced in frequency, and a perfectly linear amplifier would simply amplify the two signals. However, the real amplifier is never with perfectly linearity, and nonlinearity will result in additional output signals. A nonlinear amplifier will have a transfer function that can be approximated as：

$$P_o = a_1 P_{in} + a_2 P^2_{in} + a_3 P^3_{in} + \dots \tag{4-13}$$

where P_{in} and P_o are the input and output power, and a_i are coefficients. A linear amplifier would have $a_i = 0$ for $i > 1$. Consider an input signal with two closely spaced frequencies, f_1 and f_2：

$$P_{in} = P_1 \sin(2 \pi f_1 t) + P_2 \sin(2 \pi f_2 t) \tag{4-14}$$

If Eq. (4-14) were substituted into Eq. (4-13), we can use elementary algebra and trigonometric identities to show that the output power (P_o) contains the following components：

$a_1 P_1 \sin 2\pi f_1 t$

$a_1 P_2 \sin 2\pi f_2 t$ (fundamentals)

$\dfrac{1}{2} a_2 P_1^2 \sin 2\pi (2 f_1) t$

$\dfrac{1}{2} a_2 P_2^2 \sin 2\pi (2 f_2) t$ (second-order products)

$\dfrac{3}{4} a_3 P_1^2 P_2 \sin 2\pi (2 f_1 \pm f_2) t$

$$\frac{3}{4}a_3 P_1^2 P_2 \sin 2\pi(2f_1 \pm f_2)t \qquad \text{(third-order products)}$$

$$\vdots$$

Assuming $P_1 = P_2$, second-order product power is proportional to the square of the input signal power, third-order product power is proportional to the cube of the input signal power, and so on. But only the odd and greater than third-order terms have greater attribution to the fundamental signal. So we usually consider the fundamental signal and the third-order product signal only. Fig. 4.3 is the output power diagram of the fundamental and the third-order product signals. From Fig. 4.3, we can identify the third-order intercept point (IP3). The P_{in} value of IP3 is also called IIP3, which is important for low noise amplifier. From the fundamental diagram of microwave front-end device (Fig. 4.4), the low noise amplifier is used to receive signals. So a higher IIP3 value results in a higher linearity of the amplifier, and the less distortion of the input signals.

4.4 Breakdown Voltage (BV$_{gd}$)

Breakdown mechanisms and models have been discussed in many articles. One of the models showing it is dominated by the thermionic filed emission (TFE) / tunneling current from the Schottky gate. This model predicts that the two-terminal breakdown voltage is lower at higher temperature because tunneling current increases with the temperature. Higher tunneling current occurs at higher temperature because carriers have higher energy to overcome the Schottky barrier. Other model suggests that impact-ionization determines the

final two-terminal breakdown voltage, because the avalanche current decreases with increasing temperature. Lower avalanche current occurs at higher temperature because phonon vibrations as well as carrier-carrier scattering increase with increasing temperature. Either model is incomplete since coupling exists between TFE and impact ionization mechanisms. In addition, different devices may suffer from different breakdown mechanisms, depending on the details of the device design (insulator thickness, recess, channel composition, and so forth). In this study, the gate-to-drain breakdown voltage BV_{gd} is defined as the gate-to-drain voltage when the gate current is 1mA/mm.

4.5 Extrinsic Transconductance (g_m)

The transconductance of the HEMTs indicates the ability of the gate voltage on the control of the drain current. It can be defined as：

$$g_m = \frac{dI_D}{dV_G} = \frac{\varepsilon_2}{d_2} Z_G v_{sat}$$

(4-15)

where the v_{sat} is the electron velocity of the "two dimensional electron gas" (2-DEG).

The measurement requires specification of the initial gate voltage, the gate voltage step, and the drain voltage at which the measurement is made. Because of the nonlinear behavior of source-drain current as a function of gate voltage, g_m typically will become less as the bias approaches pinch-off approaches. This also means that a smaller voltage step will yield a higher transconductance. The extrinsic transconductance is a function of the total gate width of the device, so the width must also be given. Besides, g_m may also be normalized to a unit gate

width, usually mS/mm.

4.6 Scattering Parameters [3-2]

Generally, the Scattering parameters, which referred to as S-parameters, are fundamental to microwave measurement. S-parameters are a way of specifying return loss and insertion loss or insertion gain. Fig. 4.5 shows the equivalent two-port network schematic at high frequency. The relation of the microwave signals and s-parameters are defined as follows:

$$\begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{bmatrix} s11 & s12 \\ s21 & s22 \end{bmatrix} * \begin{bmatrix} a1 \\ a2 \end{bmatrix} \tag{4-16}$$

S signals going into or coming out of the input port are labeled by a subscript 1. Signals going into or coming out of the input port are labeled by a subscript 2. The electric field of the microwave signal going into the component ports is designated a; that leaving the ports is designated b. Therefore,

a_1 is the electric field of the microwave signal entering the component input.

b_1 is the electric field of the microwave signal leaving the component input.

a_2 is the electric field of the microwave signal entering the component output.

b_2 is the electric field of the microwave signal leaving the component output.

By definition, then,

$$s11 = \frac{b1}{a1} \bigg|_{a2=0}$$

$$s21 = \frac{b2}{a1} \bigg|_{a2=0}$$

$$s12 = \frac{b1}{a2}\bigg|_{a1=0}$$

$$s22 = \frac{b2}{a2}\bigg|_{a1=0} \tag{4-17}$$

Consequently, s_{11} is the electric field leaving the input divided by the electric field entering the input, under the condition that no signal enters the output. Because b_1 and a_1 are electric fields, their ratio is a reflection coefficient. Similarly, s_{21} is the electric field leaving the output divided by the electric field entering the input, when no signal enters the output. Therefore, s_{21} is a transmission coefficient and is related to the insertion loss or the gain of the device. s_{22} is similar to s_{11}, but looks in the other direction into the device.

4.7 Current-Gain Cutoff Frequency (f_T) and Maximum Oscillation Frequency (f_{max})

The intrinsic device model for the HEMT device is shown in Fig. 4.6. If we only consider the intrinsic part, the current can be expressed as：

$$
\begin{aligned}
i_1^{'} &= y_{11}^{'}V_1^{'} + y_{12}^{'}V_2^{'} \\
i_2^{'} &= y_{21}^{'}V_1^{'} + y_{22}^{'}V_2^{'}
\end{aligned} \tag{4-18}
$$

assume $(\omega C_{gs}R_i)^2 \ll 1$, then we can get：

$$y_{11}' = \omega^2 C_{gs}^{\;2} R_i + j\omega(C_{gs} + C_{gd})$$

$$y_{12}' = -j\omega C_{gd}$$

$$y_{21}' = G_m - j\omega(C_{gd} + C_{gs} G_m) \qquad\qquad (4\text{-}19)$$

$$y_{22}' = G_d + j\omega(C_{gd} + C_{ds})$$

$$\frac{i_2'}{i_1'} = \frac{y_{21}'}{y_{11}'} = \frac{G_m - j\omega(C_{gd} + C_{gs} R_i G_m)}{\omega^2 C_{gs}^{\;2} R_i + j\omega(C_{gs} + C_{gd})}$$

assume $\quad \begin{array}{l} G_m \gg |\,\omega(C_{gd} + C_{gs} R_i G_m)\,| \\ \omega(C_{gs} + C_{gd}) \gg \omega^2 C_{gs}^{\;2} R_i \end{array}$

f_T is defined as the frequency when current gain $\dfrac{i_2'}{i_1'} = 1$, and can be

expressed as：

$$f_T \cong \frac{G_m}{2\pi(C_{gs} + C_{gd})} \qquad\qquad (4\text{-}20)$$

f_{max} can be obtained by using unilateral gain：

$$\begin{aligned} U = G_{U\,max} &= \frac{|\,y_{21}' - y_{12}'\,|^2}{4\,\mathrm{Re}(y_{11}')\,\mathrm{Re}(y_{22}')} \\ &= \frac{1}{4}\frac{1}{f^2}\left(\frac{G_m}{2\pi C_{gs}}\right)^2 \frac{1}{R_i G_d} \qquad\qquad (4\text{-}21) \\ &= \frac{1}{4}\frac{f_T^2}{f^2}\frac{1}{R_i G_d} \end{aligned}$$

when U=1, f_{max} can be expressed as：

$$f_{max} = \frac{f_T}{2\sqrt{R_i G_d}} \qquad\qquad (4\text{-}22)$$

If we further consider gate resistance R_g, ohmic contact resistance R_s and R_d, then the small signal equivalent circuit is shown as Fig. 4.7.

assume $\;(\omega C_{gs} R_i)^2 \ll 1$

$$G_m >> | \omega(C_{gd} + C_{gs} R_i G_m) |$$

$$\omega(C_{gs} + C_{gd}) >> \omega^2 C_{gs}{}^2 R_i$$

$$G_m >> | G_d + j\omega(C_{gd} + C_{ds}) |$$

then $\quad | Y^{'} | = y_{11}{}^{'} y_{22}{}^{'} - y_{12}{}^{'} y_{21}{}^{'} \cong j\omega C_{gd} G_m$

Transfer y parameter into Z parameter：

$$Z_{11} = \frac{y_{22}{}^{'}}{| Y^{'} |} + R_g + R_s$$

$$Z_{12} = \frac{-y_{12}{}^{'}}{| Y^{'} |} + R_s$$

$$Z_{21} = \frac{-y_{21}{}^{'}}{| Y^{'} |} + R_s$$

$$Z_{22} = \frac{y_{11}{}^{'}}{| Y^{'} |} + R_d + R_s$$

and $\quad | Z | = Z_{11} Z_{22} - Z_{12} Z_{21}$

$$\frac{i_2}{i_1} = \frac{y_{21}}{y_{11}} = \frac{\dfrac{Z_{21}}{| Z |}}{\dfrac{Z_{22}}{| Z |}} = \frac{-y_{21} + R_s | Y |}{y_{11} + (R_d + R_s) | Y |}$$

$$= \frac{-G_m + R_s \left\{ [j\omega(C_{gs} + C_{gd})][G_d + j\omega(C_{gd} + C_{ds})] + j\omega C_{gd} G_m \right\}}{j\omega(C_{gs} + C_{gd}) + (R_d + R_s)\left\{ [j\omega(C_{gs} + C_{gd})][G_d + j\omega(C_{gd} + C_{ds})] + j\omega C_{gd} G_m \right\}}$$

$$\frac{i_2}{i_1} \cong \frac{G_m}{j\omega(C_{gs} + C_{gd}) + (R_d + R_s)\left\{ [j\omega(C_{gs} + C_{gd})] G_d + j\omega C_{gd} G_m \right\}}$$

$$f_T \cong \frac{G_m}{2\pi \left\{ (C_{gs} + C_{gd})[1 + (R_d + R_s) G_d] + C_{gd} G_m (R_d + R_s) \right\}} \qquad (13)$$

and we can get f_{max} [28]：

$$f_{max} = \frac{f_T}{\sqrt{4 \dfrac{G_d}{G_m}(G_m R_i + \dfrac{R_s + R_g}{1/G_m + R_s}) + \dfrac{4}{5}\dfrac{C_{gd}}{C_{gs}}(1 + \dfrac{2.5 C_{gd}}{C_{gs}})(1 + G_m R_s)^2}} \qquad (14)$$

f_T and f_{max} are parameters often used to indicate the high frequency capability of the transistors.
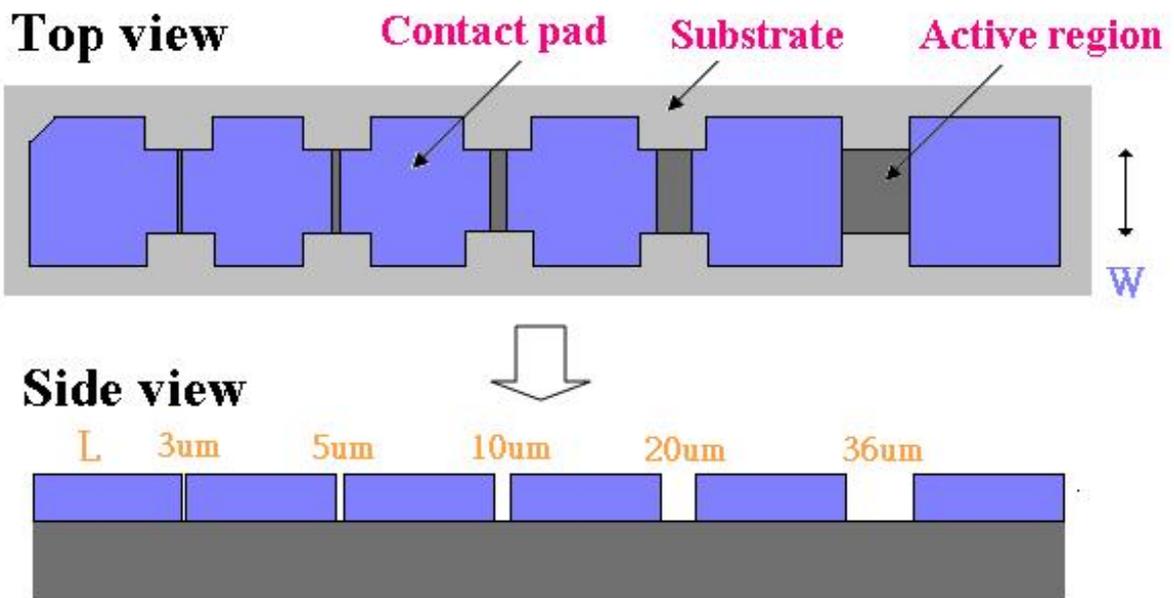
Fig. 4.1 The Transmission Line Method (TLM) pattern.
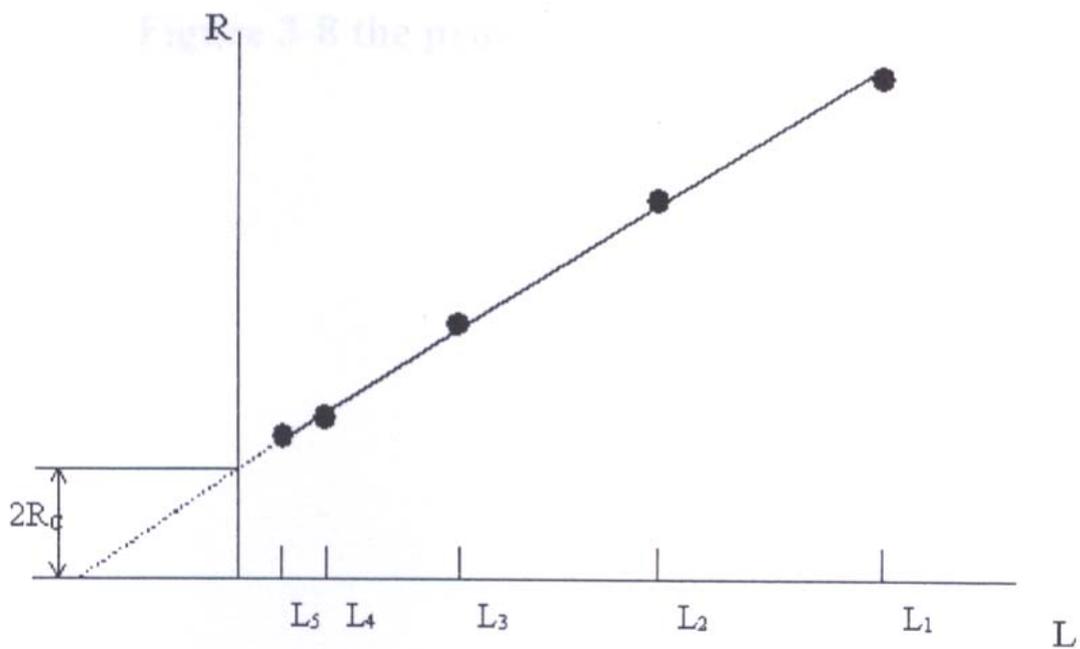
Fig. 4.2 The illustration of utilizing TLM to measure ohmic contact resistance
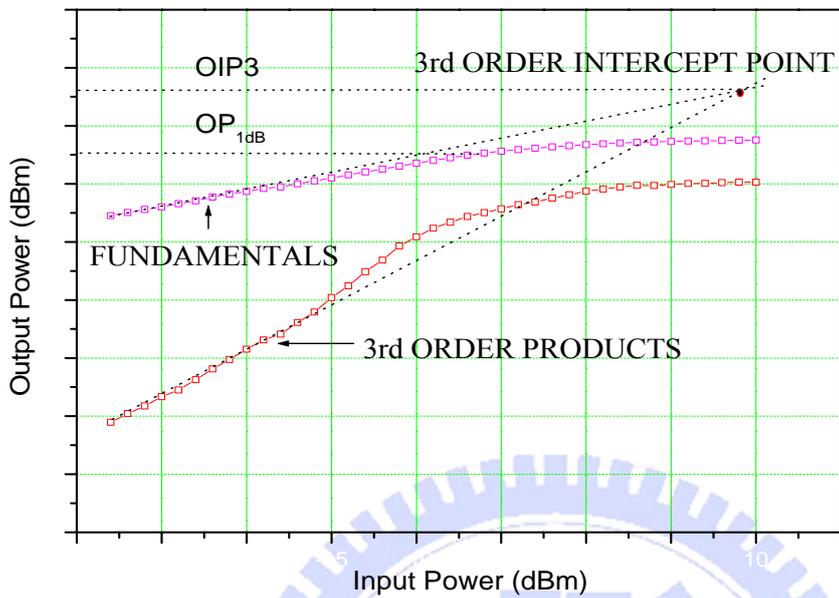
Fig. 4.3 Output power diagram of fundamental andthird-order product signals.
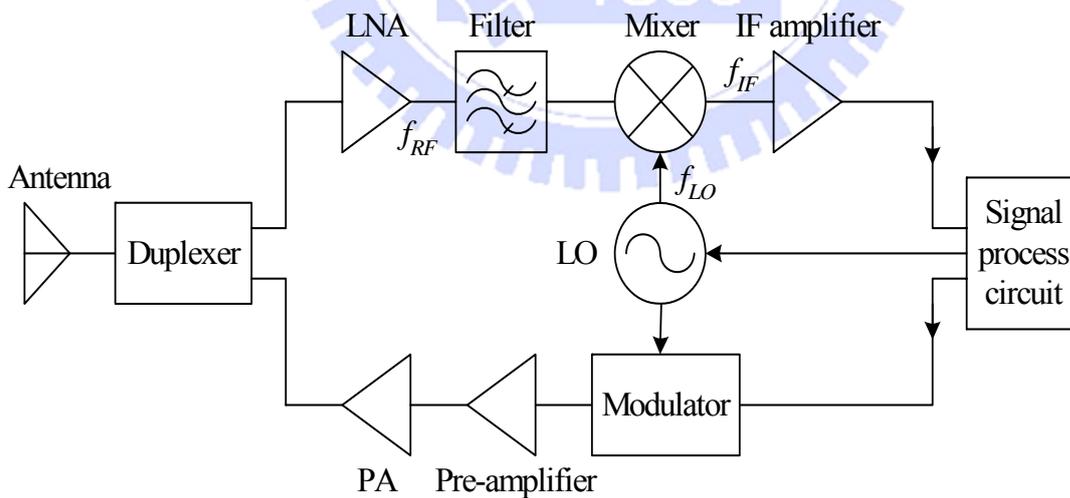
Fig. 4.4 Fundamental diagram of the microwave front-end device.
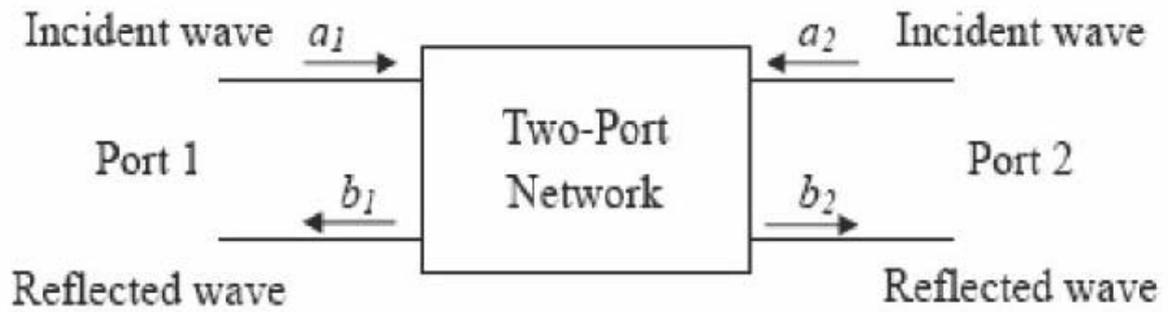
Fig. 4.5 The equivalent two-port network schematic at high frequency.
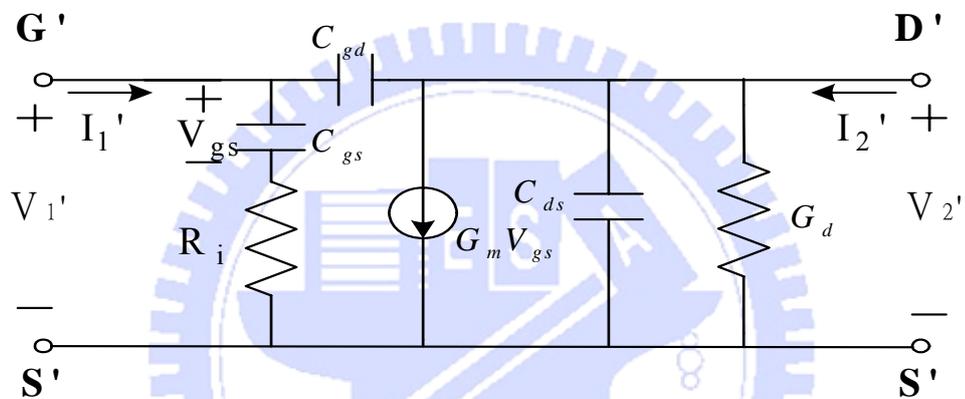
Fig. 4.6 AlGaN/GaN HEMT intrinsic device model.
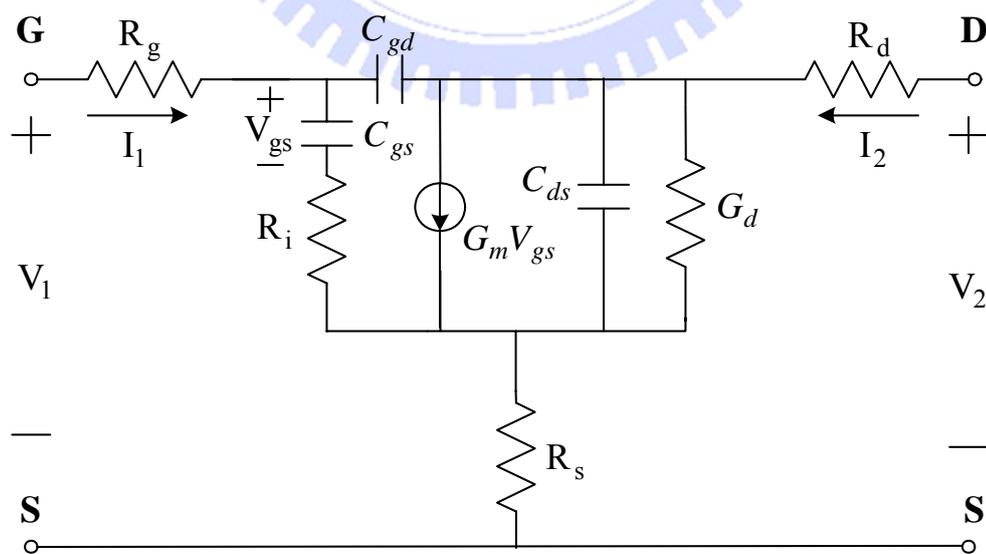
Fig. 4.7 AlGaN/GaN HEMT small signal equivalent circuit.

Chapter 5

Study of AlGaN/GaN MOS-HEMTs on Silicon substrate with Al$_2$O$_3$ Gate Insulator for Device Linearity Improvement

As shown in chapter 2, device performance of conventional Schottky-gate AlGaN/GaN HEMTs suffers from high gate leakage current. Also, the drain current collapses occurs when operating at high bias voltage resulting in poor long-term reliability of the Schottky gate. To improve the leakage characteristics of the conventional Schottky-gate AlGaN/GaN HEMTs devices, the fabrication and characterization of the 1.5-μm AlGaN/GaN MOS-HEMTs with 10 nm Al$_2$O$_3$ high-k gate oxide grown by ALD on Si substrate was investigated. Compared to regular HEMT devices of similar geometry, little degradation of the drain current and gate control ability was observed. The result indicates that AlGaN/GaN MOS-HEMTs were the gate leakage currents several orders of magnitude lower than those of regular HEMTs, and exhibit better linearity, higher channel saturation current with improved higher power performance.

5.1 Introduction

Recently, with the rapid development of wireless communication system, the transmission speeds of next-generation wireless mobile networks, including Mobile Worldwide Interoperability for Microwave Access (WiMAX) and long term evolution (LTE) networks will be several tens of megabits per second. Higher speeds will require increased output power, leading to increased power

consumption by transmission amplifiers, so base stations will require significantly higher power and more physical space. Therefore, there is a need to develop compact base stations that offer easy implementation and low operation costs. To make possible a small base station with lower power consumption, high-efficiency power amplifiers are currently being developed using gallium nitride high electron mobility transistors (GaN-HEMTs). The superior properties of AlGaN/GaN HEMTs promising contenders for high-power, high-temperature, high-breakdown, and high-frequency applications.

However, one of the key problems limiting the performance and reliability of AlGaN/GaN HEMTs for high-power RF applications is the high Schottky-gate leakage current, which results in the degradation of DC/RF parameters. At positive gate bias, high forward gate current can shunt the gate-channel capacitance, thus limiting the maximum drain current. At negative gate bias, high voltage drops between the gate and drain resulting in premature breakdown and the maximum applied drain voltage is restricted. Besides, gate leakage current increase resulting in the device sub-threshold currents, which decrease the achievable amplitude of RF output. All these limitations become the most important key factors to be solved for the development of the advanced wireless communication system.

To overcome this problem, several groups have been trying to integrate the MOS structure into conventional Schottky-gate HEMT by looking for proper gate insulators for AlGaN/GaN based HEMT. Al_2O_3 has been used as the gate insulator to reduce the gate leakage, which allows the application of high positive gate voltage to further increase the sheet electron density in 2D channel. It also offers additional benefits of a wide band gap (about 8.7eV), high breakdown electric field (5~20 MV/cm), high thermal stability (amorphous up to

at least 1000°C) and chemical stability compared to AlGaN. With well-controlled thickness and uniform Al_2O_3 layer deposited by ALD technology which employs surface saturation reaction technique, ALD Al_2O_3 is the leading candidate for the gate insulators in MOS-HEMT device.

On the other hand, in the advanced wireless communication system, multichannel transmissions are extensively used to transmit signals. As transiting signals, there are many operating frequencies with the neighboring frequencies located closely to each other, so it is important to consider that the device used in the communication system would not induce signal distortions. However, among all intermodulation distortions, third-order intermodulation distortion (IM3) can't be filtered out by the filter; therefore, IM3 dominates the linearity performance of the device and is the most important linearity criteria for wireless communication system [29]. Therefore, in this research, we study the linearity characteristics of the Al_2O_3 AlGaN/GaN MOS-HEMTs on Si substrates, and compare it with the regular AlGaN/GaN HEMTs devices for device linearity improvement in this study.

5.2 Device Fabrication

The AlGaN/GaN HEMTs structure was grown on Si substrate using MOCVD technology. Electron mobility of 1600 $cm^2V^{-1}s^{-1}$ and sheet carrier density of 1×10^{13} cm^{-2} were measured by hall measurement. The device processing started with ohmic contact formation. Ohmic metal Ti/Al/Ni/Au was evaporated by e-gun system, and then annealed at 800°C for 1min in N_2. The spacing between source and drain is 5μm. After Ohmic contact fabrication, mesa

isolation was attained through dry etch process was controlled by inductive couple plasma (ICP) with Cl_2 in Ar ambient. A 10nm amorphous Al_2O_3 oxide layer was deposited onto the wafer by atomic layer deposition (ALD) at 300ºC prior to the gate formation. The ALD technique allows high-quality ultra-thin material deposition with atomic layer accuracy. After gate photolithography, a Ti/Pt/Au electrode was evaporated. A schematic comparison between HEMT and MOS-HEMT are fabrication as shown in Fig. 5.1.

5.3 Results and Discussion

Ohmic contact with contact resistance of 2.8×10^{-6} (Ohm-cm^2) was evaluated by TLM method. Fig. 5.2 shows the typical output current-voltage (I-V) characteristics of the 1.5μm gate length AlGaN/GaN HEMT and Al_2O_3 MOS-HEMT. The Schottky-gate device has a maximum drain current of 404 mA/mm at $V_{GS} = 0$, while the MOS-HEMT devices have 544.2 mA/mm drain currents, respectively. Besides, the HEMTs and MOS-HEMTs were completely pinch-off at a gate voltage of -5 and -6.7V, respectively. The negative shift in the V_{th} was attributed to the decrease gate barrier capacitance. The experimental V_{th} for both HEMTs and MOS-HEMTs were in good agreement with the values obtained from Eq. (5-1), neglecting the residual doping in the AlGaN barrier layer [6]:

$$V_{th} = \frac{en_s}{C_b}.$$
(5-1)

Where e is the electronic charge, n_s is the sheet charge density and C_b is the total unit area capacitance of the barrier layer and dielectric.

Fig. 5.3 shows the I_{DS} versus V_{GS} curves of HEMT and MOS-HEMT devices. From a comparison of these device performances, it can be seen that the

HEMTs have lower I_{DS} of 747 mA/mm at V_{GS} = 3.6 V, but for MOS-HEMTs, its reaches 880 mA/mm at 6 V gate bias. In this sense, the good quality of both Al_2O_3 insulator and Al_2O_3/HEMT interface has rendered a higher applicable gate bias, which result in a higher driving current capacity of MOS-HEMTs compared to HEMTs. Moreover, the drain current at the same gate bias is also higher for MOS-HEMT. This difference arises, thereby making the MOS-HEMT channel depletion for the same gate voltage smaller than that for the HEMT. In Fig. 5.4, a slight transconductance decrease in MOS-HEMTs compared to HEMTs from 171 to 132 mS/mm was observed, which is consistent with a further separation between the control gate and the 2-DEG channel with the presence of an additional Al_2O_3 layer in MOS-HEMTs. However, due to the high dielectric constant of Al_2O_3, the degradation in $g_{m,max}$ of MOS-HEMT is only 22.8% relative to that of HEMT, much better than the serve transconductance deterioration in MOS-HEMTs using low-k gate dielectrics such as SiO_2 (27.2%), Si_3N_4 (35.7%). This is in agreement with an estimated reduction of 20% by (5-1), assuming drift velocity saturation (at L_g = 1.5μm) with V_{sat} = 5×10^6 cm/s. In additional, the gate voltage swing (GVS), defined as the 10% drop from the $g_{m,max}$ increase from 0.3V for HEMTs to 3.1 V for MOS-HEMTs. The larger GVS suggests a better linear behavior for MOS-HEMTs compared to Schottky-gate HEMTs, from which a smaller intermodulation distortion, a smaller phase noise and a larger dynamic range could be expected, thus desirable for practical amplifier application.

Fig. 5.5 shows the gate leakage performance of the both HEMTs and MOS-HEMTs with the same device dimensions, from which the leakage current of MOS-HEMTs is found to be significantly lower than that of the Schottky-gate HEMTs. The gate leakage current density of MOS-HEMTs is almost 3 orders of

magnitude lower than that of the HEMTs. Such a low gate leakage current should be attributed to the large band offsets in the Al_2O_3/HEMT and a good quality of both the reactive-sputtered Al_2O_3 dielectric and the Al_2O_3/HEMT interface. This leads to an increase of the two terminal reverse breakdown voltage (about 25%) and of the forward breakdown voltage (about 30%). This confirms that the Al_2O_3 dielectric thin film acts as an efficient gate insulator. To investigate the breakdown behavior of Al_2O_3-insulated gate device, the off-state three-terminal drain-source breakdown characteristics of the HEMT and Al_2O_3 MOS-HEMT were measured, the results are as shown in Fig. 5.6; the devices were measured at gate voltage Vgs of -8V. The breakdown voltage BV_{DS} is defined as the drain voltage at a gate current of 1ma/mm, which is consistent with the rapidly increased currents caused by avalanche breakdown. The Al_2O_3 MOS-HEMT with 1.5μm gate length shows a higher breakdown voltage, while the conventional HEMT. The high breakdown voltage is related to the utilization of the Al_2O_3 gate insulator to reduce the leakage current.

Fig 5.7 shows I_{DS} vs. V_{GS} transfer curves for Al_2O_3-insulated gate and Schottky-gate AlGaN/GaN HEMTs with the different drain voltages from 4 to 7 V. With increasing the drain voltage, both of the HEMT and MOS-HEMT devices have higher maximum drain current, except the HEMT at V_{DS} is 7 V. In addition, at forward gate bias beyond +2V, high drain current drops for the Schottky-gate HEMT was observed as compare to the MOS-HEMT. This is because the high Schottky-gate leakage current of HEMT, with results in the degradation of the I_D. On the other hand, the slope of I_D curve of MOS-HEMT is lower than regular HEMT; however, when increasing the gate bias to the positive voltage, the drain current increases at a stable rate in a large gate bias region. This is because Al_2O_3 gate insulator with larger bandgap that can afford much higher forward gate bias.

The characteristics of the G_m dependence on the gate-bias of Al$_2$O$_3$-insulated and Schottky-gate AlGaN/GaN HEMTs with the different drain voltages from 4 to 7 V are shown in Fig. 5.8. With the increase of the drain voltage, both of the HEMT and MOS-HEMT devices show almost have the similar maximum transconductance. The maximum drain current depends G_m versus V_{GS} curve, the MOS-HEMT device has a lower maximum Gm value, but a flatter Gm distribution as compared to that of regular HEMT. It represents that the drain current increased in a stable rate in a wider range of gate bias region, this may be due to that the gate leakage current was suppressed in the MOS-HEMT. As mentioned before, a lower IM3 level can be achieved by increasing the flatness of the G_m distribution across the gate-bias region, in our current case, it indicate, that MOS-HEMT may have better device linearity performance.

For linearity assessment, nonlinear transfer function based analysis method is used. Previously published results revealed that, the G_m were to remain constant over the operating range of gate bias for minimizing third-order distortion. Hence, improving the flatness of the extrinsic G_m profile will result in lower IM3 levels and higher third-order intercept point (IP3), and thus improve the device linearity [30]. Eq. (5-2) shows the relationship between Gm and drain-source current (I_{DS}). To maintain Gm constant with different gate-source voltage (V_{GS}), the I_{DS} as a function of V_{GS} should be straight and large.

$$Gm = \frac{dI_{DS}}{dV_{GS}}$$
(5-2)

To further investigate the linearity performance of the three devices, polynomial curve fitting technique was applied to the transfer characteristic functions of these devices as equation (5-2).

$$G_m(V_{GS}) = \frac{\partial I_{DS}(V_{GS})}{\partial V_{GS}} = a_1 + 2a_2V_{GS} + 3a_3V_{GS}^2 + 4a_4V_{GS}^3 + 5a_5V_{GS}^4 + ... \qquad (5\text{-}3)$$

Hence, the relationship between IM3, IP3 and Gm, Gds are shown in equation (5-3) and (5-4) [31-33].

$$IM3 \propto \frac{\left(G_m^"\right)^2}{G_{ds}^2 \cdot R_L} \cdot A^6 \qquad (5\text{-}4)$$

$$IP3 \propto \frac{\left(G_m\right)^3}{G_m^" \cdot G_{ds}^2 \cdot R_L} \qquad (5\text{-}5)$$

In order to improve the device linearity, I_{DS} should increase linearly with V_{GS}. Therefore, a_1 should be larger and the higher order constants, while a_3 and a_5 should be minimized [34-35]. Table 5.1 shows the coefficients of HEMT and MOS-HEMT devices. It shows that the MOS-HEMT device has higher a_1 of 6.64×10^{-3}, while regular HEMT device has lower a_1 of 5.53×10^{-3}. In addition, the lower a_3 is 1.5646×10^{-4} and the lower a_5 is 4.33061×10^{-6} from MOS-HEMT device. From the data analysis, the devices linearity improvement can be achieved by using MOS-HEMT with the Al_2O_3 as gate insulator approach.

To evaluate the device linearity, the measurement of IM3 and IP3 of these devices were necessary. The IM3 and IP3 measurements were carried out by injecting two signals with the same amplitude but at two different frequencies: 2.0 GHz and 2.001GHz with the devices biased at V_{DS} = 7V, and adjust the I_{DS} to get the IP3 vs. I_{DS} curve. Furthermore, the load impedance was firstly tuned for maximum gain in input side and maximum power in output side for each individual device. The measurement results of the IP3 versus I_{DS} curves for these three different 80nm × 50μm devices are shown in Fig.5.11. It shows that

MOS-HEMT devices possess higher IP3 value, and wider high IP3 region versus different I_{DS}. The tuning at Γsource and Γload of MOS-HEMT and HEMT devices were Γsource = $33.5\angle88.71^{o}$ and $74.8\angle89.47^{o}$, and Γload = $12.22\angle86.62^{o}$ and $12.22\angle86.62^{o}$, respectively. From the data in Fig. 5.11 and Table 5.1, it can be concluded that Al_2O_3-insulated gates can achieves flatter Gm distribution versus V_{GS} bias and thus lower overall IM3 and higher IP3 of these devices even though Schottky-gate gate device exhibits higher peak G_m.

5.4 Conclusions

The linearity characteristics of the AlGaN/GaN HEMT and Al_2O_3 MOS-HEMT on Si substrates are investigated in this study. Although the MOS-HEMT device demestrated gigher maximum G_m of 132 mS/mm at V_{DS}= 7V, flatter G_m distribution was achieved for the MOS-HEMT device. To further investigate the linearity performance of the two devices, polynomial curve fitting technique was applied to the transfer characteristic functions. It shows that the MOS-HEMT device has highest a_1 and lowest a_3 and a_5, as compared with the regular HEMT. Therefore, the devices linearity improvement can be achieved by using Al_2O_3 insulated-gate.

The AlGaN/GaN HEMTs on Si substrates with Al_2O_3 gate insulator to improve the device linearity is demonstrated. The reduction of gate leakage current in MOS-HEMT results in the improvement of the G_m vs. V_{GS} curve flatness, and leads to lower overall IM3 and higher IP3 for MOS-HEMT devices, even though the regular HEMT device exhibits higher peak G_m. These DC characteristics lead to higher IP3 levels and lower IM3 for the MOS-HEMT device as compared to the regular HEMT devices studied. The experimental

results in this work show that Al_2O_3 insulated-gate can be practically used on GaN HEMT devices for the development of high linearity devices for wireless communication applications.
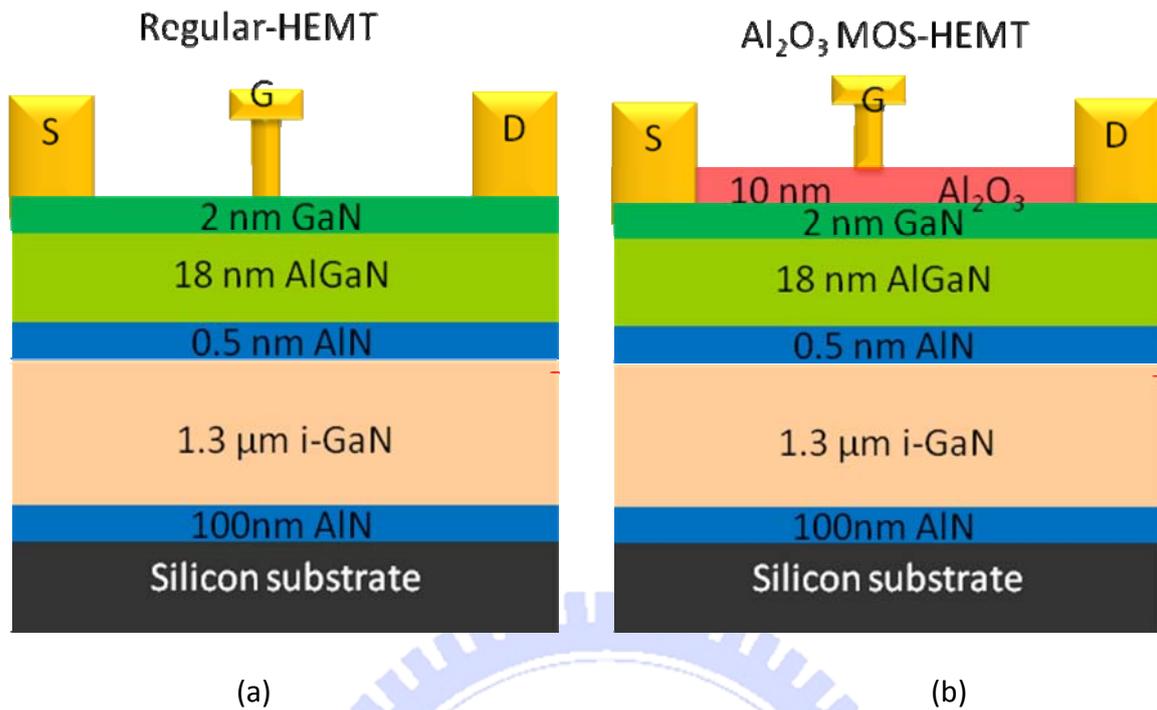
Fig. 5.1 Cross section of the (a) 1.5μm a Schottky-gate AlGaN/GaN HEMT (b)

MOS-HEMT with 10nm Al_2O_3.
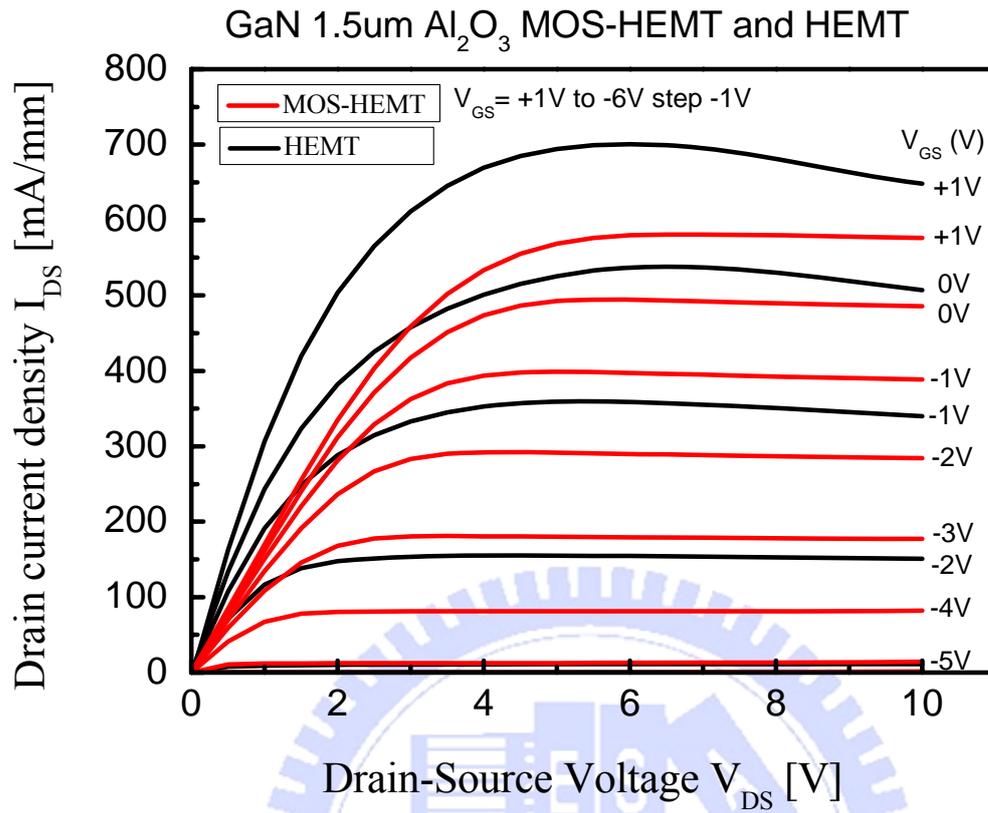
Fig. 5.2 DC I_D versus V_{DS} characteristics at V_{GS}= 1 to -6 V of the AlGaN/GaN

HEMT and Al_2O_3 MOS-HEMT.
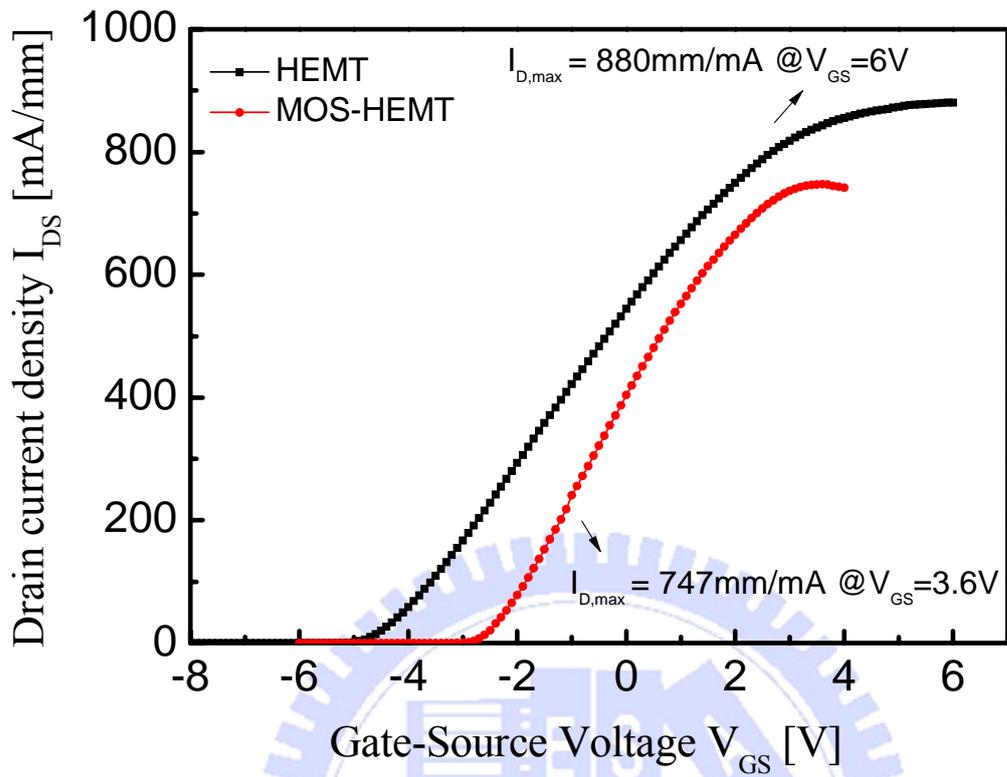
Fig. 5.3 I_{DS} versus V_{GS} curve for the AlGaN/GaN HEMT and Al_2O_3 MOS-HEMT at the V_{DS} bias is 7 V.
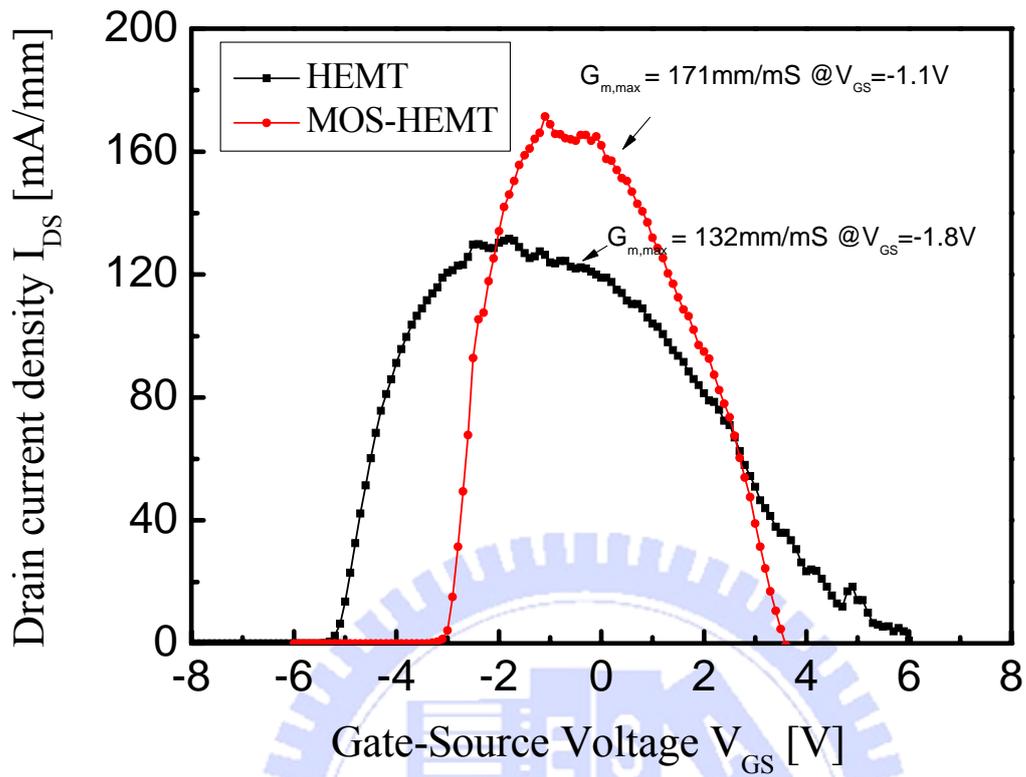
**Fig. 5.4** Transconductance gm versus gate-source bias V_{GS} at the same drain bias

Vds = 7V in the saturation region for the AlGaN/GaN HEMT and Al_2O_3

MOS-HEMT with gate length =1.5μm.
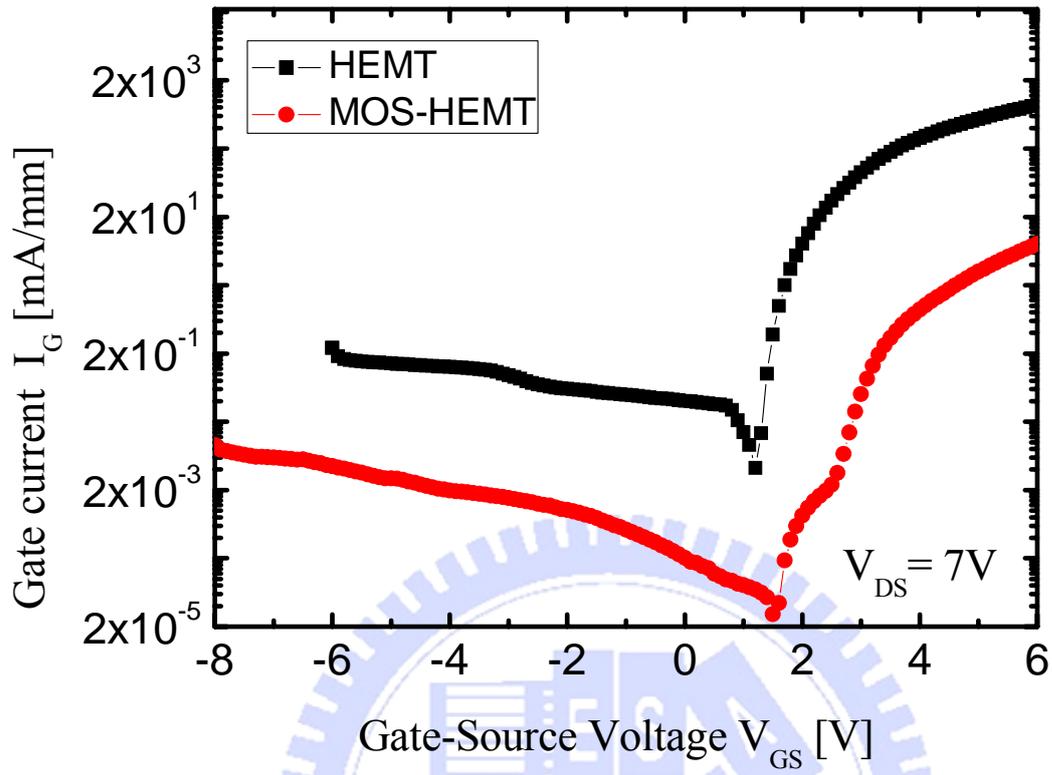
Fig. 5.5 Gate leakage currents for the AlGaN/GaN HEMT and Al_2O_3 MOS-HEMT with the same device dimensions.
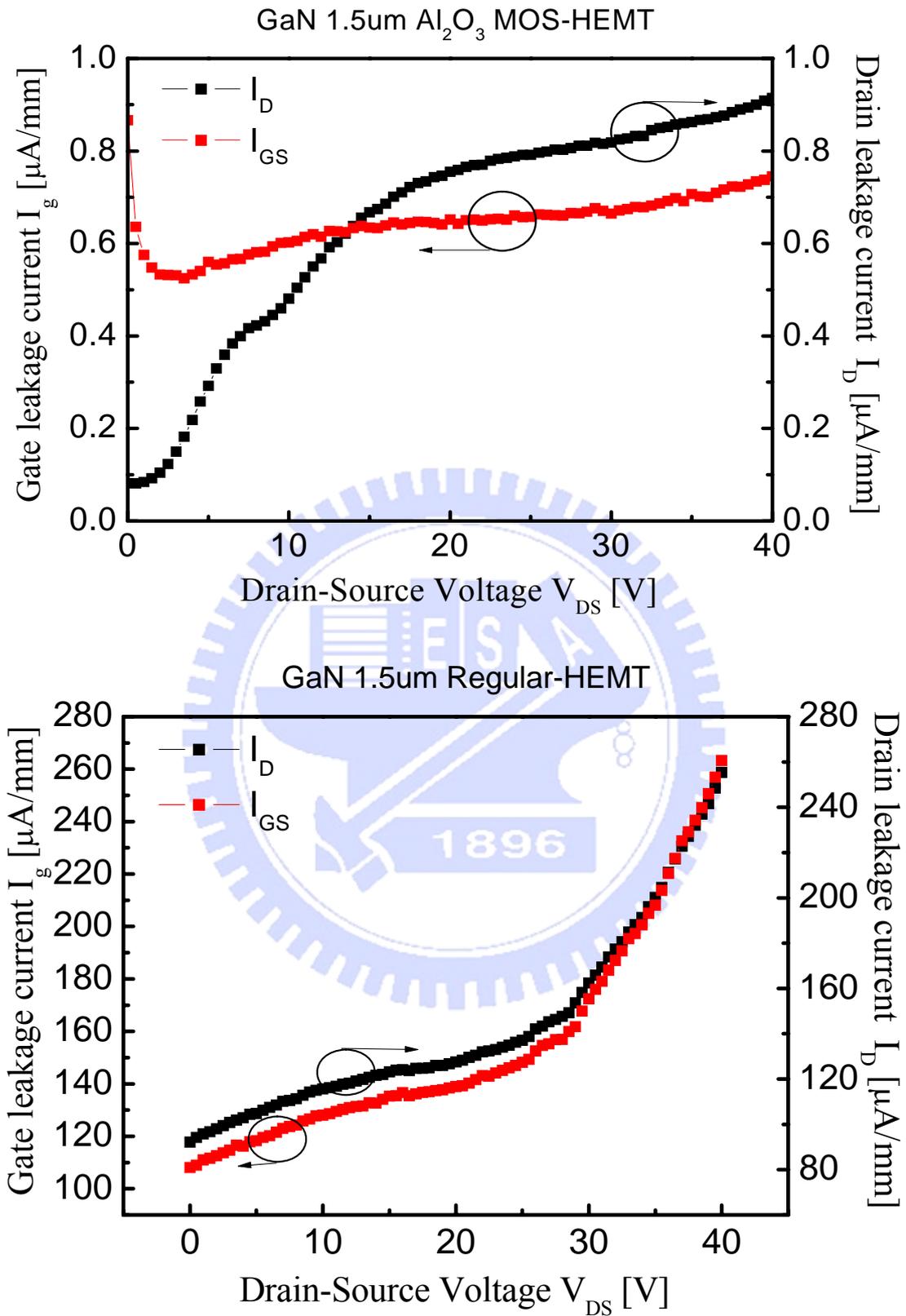
Fig. 5.6 Off-state drain-source breakdown characteristics of Al$_2$O$_3$ MOS-HEMT

and regular-HEMTs.
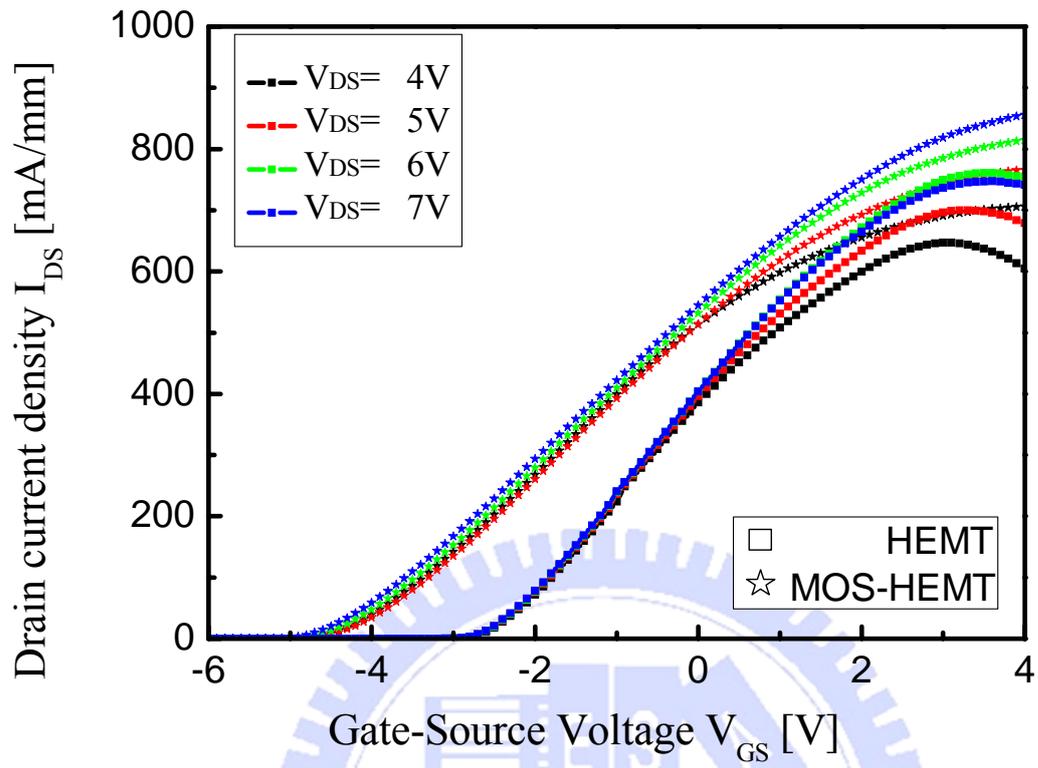
Fig. 5.7 I_{DS} versus V_{GS} curve for the AlGaN/GaN HEMT and Al_2O_3 MOS-HEMT at the V_{DS} bias is from 4 V to 7 V.
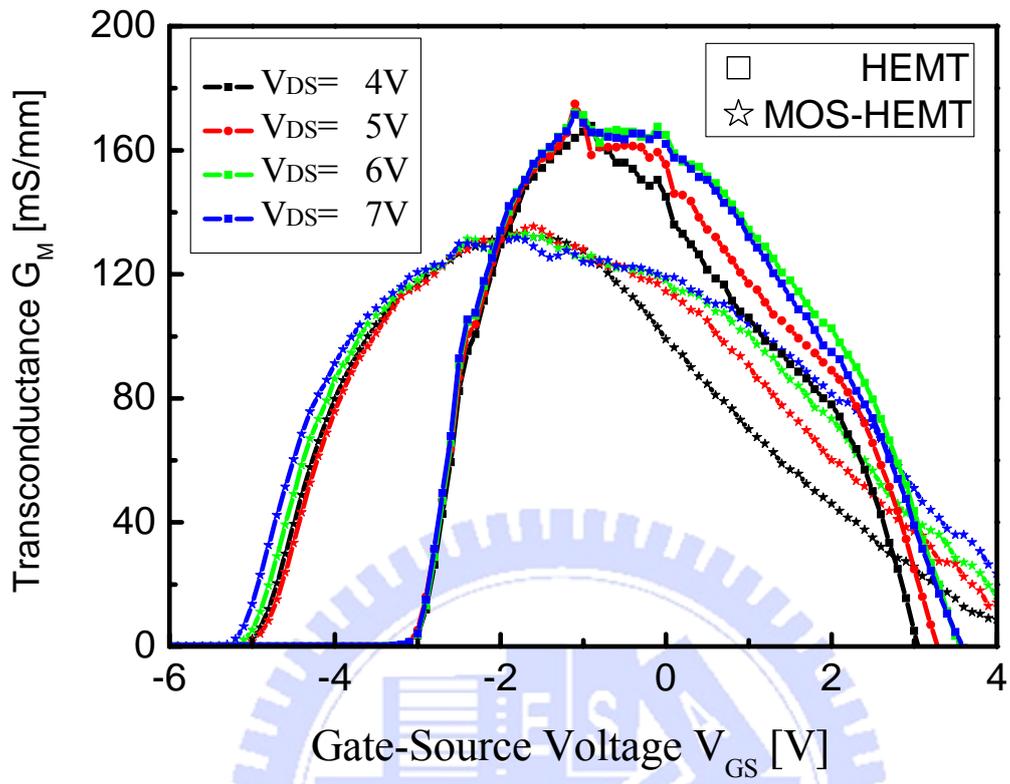
Fig. 5.8 G_m versus V_{GS} curve for the AlGaN/GaN HEMT and Al_2O_3 MOS-HEMT at the V_{DS} bias is from 4 V to 7 V.
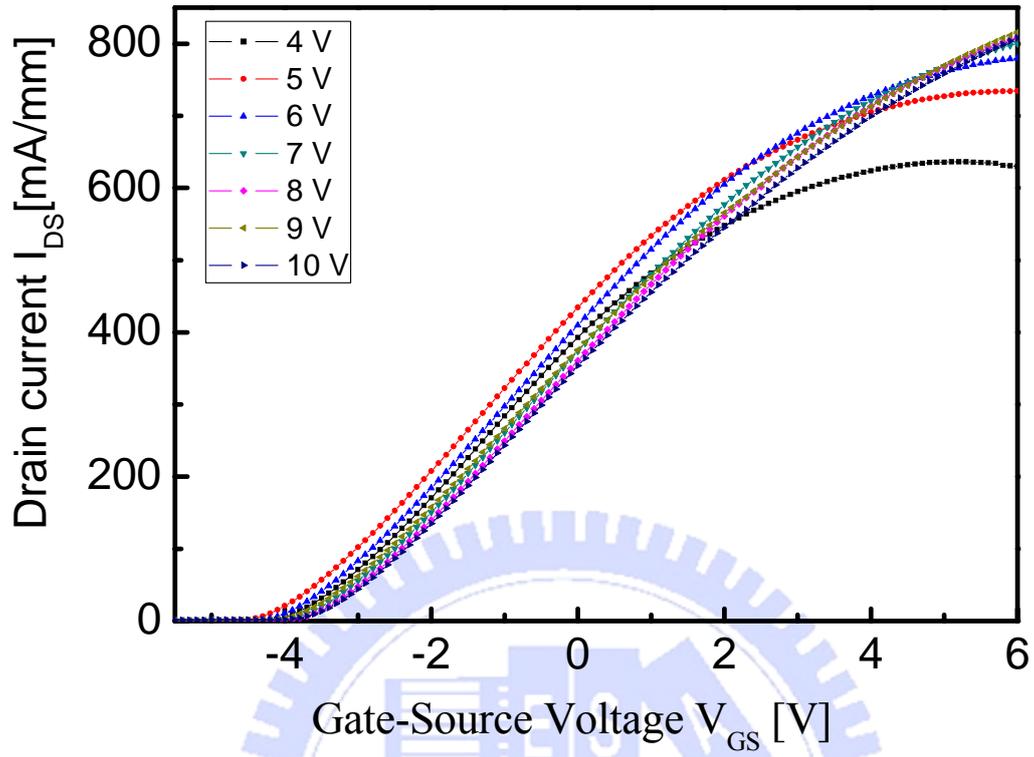
Fig. 5.9 I_{DS} versus V_{GS} curve for the Al_2O_3 MOS-HEMT at the V_{DS} bias is from 4 V to 10 V.
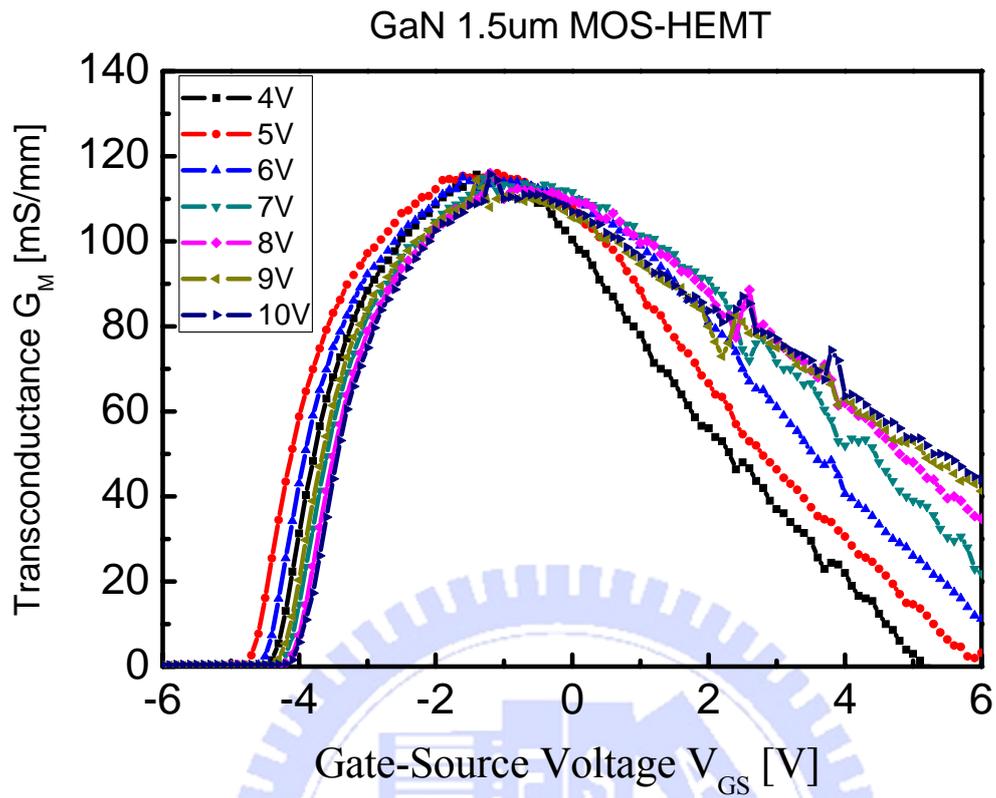
Fig. 5.10 G_m versus V_{GS} curve for the Al_2O_3 MOS-HEMT at the V_{DS} bias is from

4 V to 10V.
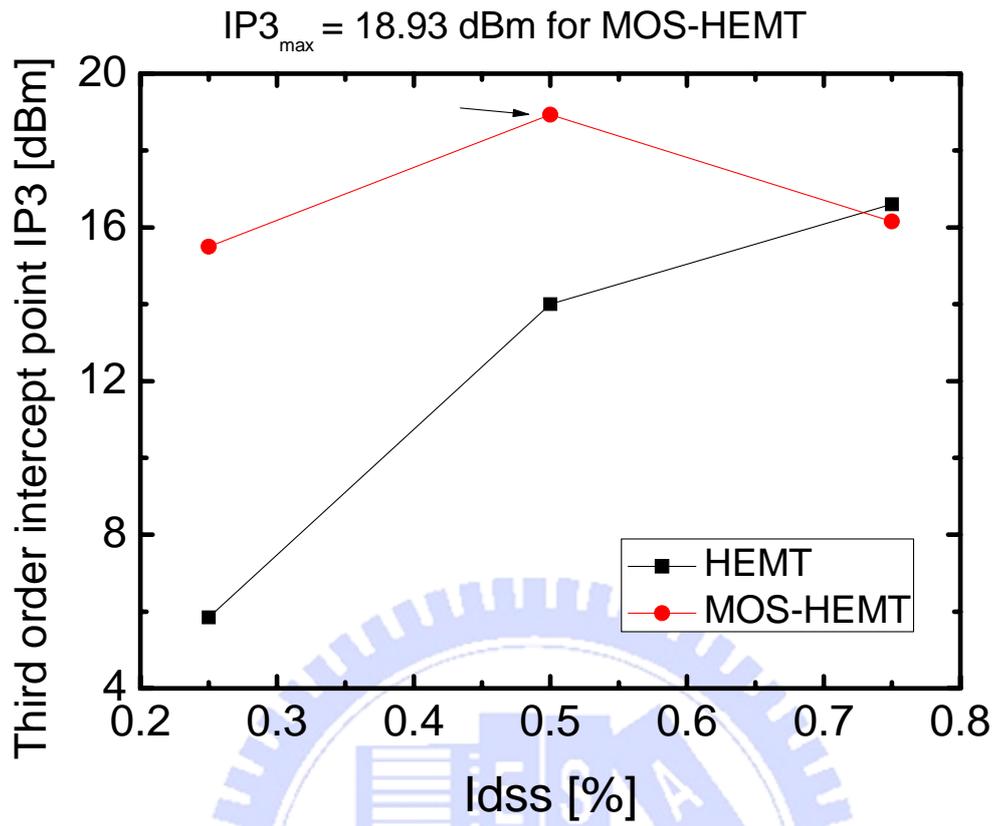
Fig. 5.11 IP3 versus IDS curve of the the AlGaN/GaN HEMT and Al_2O_3 MOS-HEMT, and the test frequency is 2GHz and V_{DS} =7V.

Table 5.1 Comparison of the IP3 of Al_2O_3 MOS-HEMT and HEMT device at drain bias is 7V.

	MOS-HEMT	HEMT
a_0	$1.619*10^{-2}$	$2.368*10^{-2}$
a_1	$6.64*10^{-3}$	$5.53*10^{-3}$
a_2	$6.94732*10^{-5}$	$1.62*10^{-3}$
a_3	$1.5646*10^{-4}$	$4.786*10^{-4}$
a_4	$3.33471*10^{-5}$	$9.2108*10^{-5}$
a_5	$4.33061*10^{-6}$	$9.54367*10^{-5}$
a_6	$1.27578*10^{-6}$	$1.7857*10^{-7}$
a_7	$1.10918*10^{-7}$	$5.2013*10^{-6}$
a_8	$1.51595*10^{-8}$	$8.7903*10^{-8}$
a_9	$1.38391*10^{-9}$	$9.8594*10^{-8}$
a_3 / a_1	$9.66*10^{-3}$	$8.6*10^{-2}$
a_5 / a_1	$6.52*10^{-4}$	$1.72*10^{-2}$

Chapter 6

Conclusion

In this dissertation, 1.5-µm-length Al_2O_3 AlGaN/GaN MOS-HEMTs and HEMTs grown on Silicon substrate were successfully fabricated and the DC and RF characteristics were evaluated. The maximum I_{DS} of 810 mA/mm and peak extrinsic G_m of 747 mS/mm were obtained for the GaN HEMT fabricated. However, the AlGaN/GaN HEMT suffers from high leakage current. In order to solve this problem, an insulated Al_2O_3 gate was applied to the device to suppress the high gate leakage current. The innovative MOS-HEMT technique not only reduces the leakage current but also successfully improved the linearity characteristics of the AlGaN/GaN HEMTs on Si substrate. It is found that MOS-HEMT effectively reduced the high electric field, in the forward bias, it enables the electrons to maintain a stable electron velocity under the gate domain and further to suppress high gate leakage current. The MOS-HEMT devices demonstrates increased drain current and maintain stable G_m value under a larger gate bias domain; the MOSHEMTs also demonstrated improvement in the G_m vs. V_{GS} curve flatness and thus leads to lower overall IM3 and higher IP3 for even through the regular HEMT exhibits higher peak G_m. For the MOS-HEMT, the maximum third order intermodulation point (IP3) of 18.93 dBm was achieved in the MOS-HEMT devices. The IP3 was higher them the regular HEMT device.

In addition, the third order intermodulation points of the MOS-HEMT and Schottky-gate device under the different gate biases are also compared in this study. By polynomial curve fitting technique, It successfully demonstrate that

the multi-gate device have the higher IP3 in the larger I_{DSS} % region. Therefore, it indicated that multi gate technique could effectively improve the linearity performance.

In conclusion, the experimental results in this study shows that, in the future, the AlGaN/GaN HEMTs with Al_3O_3-insulated gate have great potential to be used in the RF power amplifier, with improved linearity for the modern wireless communication system.

References

[1] U. K. Mishra, Linkun Shen, T. E. Kazior, and Y.-F. Wu,"GaN-Based RF Power Devices and Amplifiers," *Proceedings of the IEEE* ,vol. **96**, no. 2, pp.287-305, Feb. 2008.

[2] Y. Ando, Y. Okamoto, H. Miyamoto, T. Nakayama, T. Inoue, and M. Kuzuhara, "10-W/mm AlGaN-GaN HFET with a field modulating plate," *IEEE Electron Device Lett.*, vol. **24**, no. 5, pp. 289-291, May 2003.

[3] Y. F. Wu, M. Moore, A. Saxler, T. Wisleder, and P. Parikh, "40 W/mm double field-plated GaN HEMTs," *in Proc. Dig. Device Res. Conf.*, pp. 151–152, Jun. 2006.

[4] Y. F.Wu, A. Saxler,M.Moore, R. P. Smith, S. Sheppard, P.M. Chavarkar, T.Wisleder, U. K.Mishra, and P. Parikh, "30-W/mm GaN HEMTs by field plate optimization," *IEEE Electron Device Lett.*, vol. **25**, no. 3, pp. 117-119, Mar. 2004.

[5] Y. Pei, et. al, "Recessed Slant Gate AlGaN/GaN High Electron Mobility Transistors with 20.9W/mm at 10GHz " *Jpn. J. Appl. Phys.*, Vol. **46**,pp. L1087-L1089,2007.

[6] Wu, Y.Q., Y. Xuan, T. Shen, P.D. Ye, Z. Cheng, and A. Lochtefeld, "Enhancement-mode InP n-channel metal-oxide-semiconductor field-effect transistors with atomic-layer-deposited Al_2O_3 dielectrics." *Appl. Phys. Lett.*, vol. **91,** no. 2, 2007.

[7] Huang, M.L., Y.C. Chang, C.H. Chang, Y.J. Lee, P. Chang, J. Kwo, T.B. Wu, and M. Hong, "Surface passivation of III-V compound semiconductors using atomic-layer-deposition-grown Al_2O_3." *Appl. Phys. Lett.*, vol. **87,** no. 25, 2005.

[8] Xuan, Y., H.C. Lin, P.D. Ye, and G.D. Wilk, "Capacitance-voltage studies on enhancement-mode InGaAs metal-oxide-semiconductor field-effect transistor using atomic-layer-deposited Al_2O_3 gate dielectric." *Appl. Phys. Lett.*, vol. **88**, no. 26, 2006.

[9] O. Ambacher,a) J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy,W. J. Schaff, and L. F. Eastman," Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *Journal of Applied Physics,* vol. 85, no. 6 ,15 ,1999

[10] S. Nakamura, "GaN Growth Using GaN Buffer Layer," *Jpn. J. Appl. Phys.*, vol. **30**, pp. L1705-L1707, 1991.

[11] D. Kapolnek, et al., "Structural evolution in epitaxial metalorganic chemical vapor deposition grown GaN films on sapphire," *Appl. Phys. Lett.*, vol. **67**, pp. 1541-1543, 1995.

[12] L. Zhou, et al., "Effect of Al/N flux ratio during nucleation layer growth on the microstructure of GaN films grown by molecular-beam epitaxy," *Appl. Phys. Lett.*, vol. **88**, p. 011916, 2006.

[13] J. C. Zhang, et al., "The influence of AlN buffer layer thickness on the properties of GaN epilayer," *J. Crys. Growth*, vol. **268**, pp. 24-29, 2004.

[14] D. G. Zhao, et al., "Surface morphology of AlN buffer layer and its effect on GaN growth by metalorganic chemical vapor deposition," *Appl. Phys. Lett.*, vol. **85**, pp. 1499-1501, 2004.

[15] L. Meshi, et al., "The reduction of threading dislocations in GaN using a GaN nanocolumn interlayer," Phys. Status Solidi (c), vol. **5**, pp. 1645-1647, 2008.

[16] M. J. Manfra, *et al.*, "Dislocation and morphology control during

molecular-beam epitaxy of AlGaN/GaN heterostructures directly on sapphire substrates," *Appl. Phys. Lett.,* vol. **81**, pp. 1456-1458, 2002.

[17] K. Uchida, et al., "Characterization of Double-Buffer Layers and Its Application for the Metalorganic Vapor Phase Epitaxial Growth of GaN," *Jpn. J. Appl. Phys*., vol. **37**, pp. 3882-3888, 1998.

[18] L. K. Li, et al., "High electron mobility AlGaN/GaN heterostructures grown on sapphire substrates by molecular-beam epitaxy," *Appl. Phys. Lett.*, vol. **76**, pp. 742-744, 2000.

[19] Y. B. Pan, et al., "Reduction of threading edge dislocation density in n-type GaN by Si delta-doping," *J. Crys. Growth*, vol. **286**, pp. 255-258, 2006.

[20] A. Corrion, et al., "Review of Recent Developments in Growth of AlGaN/GaN High-Electron Mobility Transistors on 4H-SiC by Plasma-Assisted Molecular Beam Epitaxy," *IEICE Trans Electron* vol. E89-C, pp. 906-912, 2006.

[21] J. P. Ibbetson*, et al.*, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," *Appl. Phys. Lett.,* vol. **77**, pp. 250-252, 2000.

[22] M. Miyoshi, et al., "Metalorganic Chemical Vapor Deposition and Material Characterization of Lattice-Matched InAlN/GaN Two-Dimensional Electron Gas Heterostructures," *Appl. Phys. Express*, vol. **1**, p. 081102, 2008.

[23] A. Chini, et al., "2.1 A/mm current density AlGaN/GaN HEMT," *Electron. Lett*., vol. **39**, pp. 625-626, 2003.

[24] S. L. Rumyantsev, N. Pala, M. S. Shur, M.E. Levinshtein, R. Gaska,M. Asif Khan and G. Simin, "Generation-Recombination Noise in GaN-based Devices", in: "GaN-based materials and devices, Selected topics in electronics and systems" - v.33, eds. M.S.Shur and R.F. Devis, World Scientific, 2004, ISBN 981-238-844-3.

[25] E.J. Miller, X.Z. Dang, H.H. Wieder, P.H. Asbeck, E.T.Yu, G.J. Sullivan, and J.M. Redwing, "Trap characterization by gate-drain conductance and capacitance dispersion studies of an AlGaN/GaN heterostructure field-effect transistor," *Jpn. J. Appl.*, vol. **87**, 8070, 2000.

[26] Shinya MIZUNO, Yutaka OHNO, Shigeru KISHIMOTO, Koichi MAEZAWA and Takashi MIZUTANI, *Jpn. J. Appl. Phys.*, vol. **41,** no. 8, pp. 5125-5126 Part 1, August 2002.

[27]Kim, H.S., I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, J.C. Lee, P. Majhi, N. Goel, W. Tsai, C.K. Gaspe, and M.B. Santos, "A study of metal-oxide-semiconductor capacitors on GaAs, $In_{0.53}Ga_{0.47}As$, InAs, and InSb substrates using a germanium interfacial passivation layer." *Appl. Phys. Lett.*, **93**(6)(2008).

[28] Ok, I., H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, D. Garcia, P. Majhi, N. Goel, W. Tsai, C.K. Gaspe, M.B. Santos, and J.C. Lee, "Self-aligned n-channel metal-oxide-semiconductor field effect transistor on high-indium-content $In_{0.53}Ga_{0.47}As$ and InP using physical vapor deposition HfO2 and silicon interface passivation layer." *Appl. Phys. Lett.*, **92**(20)(2008).

[29] Zhao, H., H.S. Kim, F. Zhu, M. Zhang, I. Ok, S.I. Park, J.H. Yum, and J.C. Lee, "Metal-oxide-semiconductor capacitors on GaAs with germanium nitride passivation layer." *Appl. Phys. Lett.*, **91**(17) (2007).

[30] Oktyabrsky, S., V. Tokranov, M. Yakimov, R. Moore, S. Koveshnikov, W. Tsai, F. Zhu, and J.C. Lee, "High-k gate stack on GaAs and InGaAs using in situ passivation with amorphous silicon." *Mater. Sci. Eng. B-Solid State Mater. Adv. Technol.*, **135**(3): P.272-276 (2006).

[31] Zhao, H., J.H. Yum, Y.T. Chen, and J.C. Lee, "$In_{0.53}Ga_{0.47}As$ n-metal-oxide-semiconductor field effect transistors with atomic layer deposited

Al$_2$O$_3$, HfO$_2$, and LaAlO$_3$ gate dielectrics." *J. Vac. Sci. Technol. B*, **27**(4): P.2024-2027 (2009).

[32] Xuan, Y., Y.Q. Wu, T. Shen, T. Yang, and P.D. Ye, "High performance submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al$_2$O$_3$, HfO$_2$, and HfAlO as gate dielectrics." *IEEE New York* Vols 1 and 2, p.637-640 (2007).

[33] O'Connor, E., R.D. Long, K. Cherkaoui, K.K. Thomas, F. Chalvet, I.M. Povey, M.E. Pemble, P.K. Hurley, B. Brennan, G. Hughes, and S.B. Newcomb, "In situ H2S passivation of In$_{0.53}$Ga$_{0.47}$As/InP metal-oxide-semiconductor capacitors with atomic-layer deposited HfO2 gate dielectric." *Appl. Phys. Lett.*, **92**(2)(2008).

[34] S. M. SZE, Semiconductor devices, physics and technology 2nd edition, Wiley (2002)

[35] T. Ytterdal, Y. Cheng and T. A. Fjeldly, Devices Modeling for analog and RF CMOS Circuit Design, John Wiley and Sons(2003)

Devices, **55**(2): P.547-556 (2008).

Wiley(2007)