Chapter 1

Introduction

1-1 Overview and research motivation

GaN-based electron device have been widely investigated for RF and microwave power amplifiers due to their high breakdown field, high electron saturation velocity, and high operating temperature in the last decade. Recently, AlGaN/GaN high electron mobility transistors (HEMTs) have lately attracted considerable attentions as next generation device for RF power electronics application such as cell phone, satellites, and TV broadcasting [1-1]. In the mobile communication applications, the next generation cell phone need wilder bandwidth and higher efficiency; the development of satellites communication and TV broadcasting require amplifiers which can operate at higher frequencies and higher power. Because of these need, the outstanding property of AlGaN/GaN HEMTs is a very promising candidate for microwave power application in the wireless communication [1-2, 1-5].

As the amplifiers used in modern wireless communication, linearity of amplifier devices is one of the most important parameters. In the advanced wireless communication system, multichannel transmissions are extensively used to transmit signals. As transiting signals, there are many operating frequencies which the neighboring frequencies are located closely to each other, so it is important to consider that the device used in the communication system will produce the distortions. Among all intermodulation distortions, third-order intermodulation distortion (IM3) dominates the linearity performance of the device. Therefore, IM3 is the most important criteria of linearity for wireless communication system [1-6].

For the assessment of linearity, a nonlinearity transfer-function-based analysis method was used. The study of the linearity performance have been reported that , for reducing the

third-order intermodulation distortion (IM3), the transconductance need to be a constant during the wide operating range of the gate bias. It indicated the flatter transconductance profile led to a lower IM3 levels and a higher third order intercept point IP3. Therefore, the linearity of device is improved. The relationship between Gm and the drain-to- source current (I_{DS}) is shown in the equation (1)

$$Gm = \frac{dI_{DS}}{dV_{GS}} \qquad (1)$$

This thesis represented the method of improving the linearity of GaN HEMTs by using the multi-gate modulation. Firstly, we present the electrical and reliability characteristics of 80 nm multi-gate AlGaN/GaN HEMTs fabricated on Si substrates. The DC characteristic such as I_D-V_D curve and transconductance (Gm) are measured, while the specific contact resistance between contact metal and cap layer can be extracted by the transmission line model (TLM) method. All of the results show that the linearity performance of device could be improved by multi-gate modulation.

1-2 Organization of the thesis

This thesis consists of six chapters and conclusion. After introduction, the GaN material properties and high electron mobility transistors will be introduced in chapter 2. Chapter 3 focuses on the basic intermodulation of RF power amplifier. The GaN device fabrication process is introduced in chapter 4.Chapter 5 is the experiment results and discussion of the 80-nm AlGaN/GaN HEMTs on Silicon Substrate, while chapter 6 is the study of device linearity improvement for the 80-nm AlGaN/GaN HEMTs on silicon substrate by using multi-gate process. Finally, a conclusion is purposed in Chapter 7.

Chapter.2

GaN-based High Electron Mobility Transistors

2-1 Material properties of GaN

Compared with III-V semiconductor materials, the material properties of GaN, makes it become a very attractive material to produce RF power devices and amplifiers. Table 1 shows the material properties of GaN compared the competing material. In III-V materials, it can be seen in Fig.2-1 that GaN possesses very large energy band gap at room temperature (~3.4eV). The wide energy band gap property makes it excellent thermal stability. In addition, due to the strong bonding energy between the Ga and nitrogen gas, GaN has a high breakdown field (3.3 MV/cm) which means the GaN devices can withstand high operating voltage. Although GaN has the lower room temperature electron mobility of around 1500cm^2/Vs than the GaAs, but GaN has very high electron saturation velocity ($\sim 3\times10^7$ cm^2/s) ,as shown in Fig.2-2, suggesting the high speed potential of GaN-based device. Moreover, GaN has a great thermal conductivity of around 1.3 W/cm-k. The thermal property makes it can be operated at high temperature. According to the outstanding material properties of GaN, GaN-based devices are the good candidates in high-power, high-speed, and high-temperature application [2-1, 2-2].

2-2 Polarization effect

2-2-1 Crystal structure and polarization [2-3, 2-4]

GaN have two kinds of crystal type, wurtzite and zinc blende, as shown in Fig. 2-3. In

general, if noncentrosymmetric compound crystals have two different sequences of the atomic layering in the two opposing directions parallel to certain crystallographic axes, crystallographic polarity along these axes can be observed. For GaN epitaxial layers and GaN- based heterostructure, the atoms arranged in bilayers are commonly normal to the (0001) basal plane. These bilayers formed by cations and anions results in the polar face. Therefore, the basal surface of GaN should be either Ga- or N- faced. In Ga-faced, the gallium atoms are on the top position of bilayers, corresponding to the [0001] polarity. On the other hand, in N-face, the nitrogen atoms are located on the surface of {0001}, corresponding to the [0001] polarity, as shown in Fig.2-4. According to the specific crystallographic polarities, GaN exhibits different chemical and physical properties.

2-2-2 Spontaneous and piezoelectric polarization [2-3, 2-4]

Due to the spontaneous polarization P_{SP} and piezoelectric polarization P_{PE} of AlGaN and GaN, the undoped AlGaN/GaN heterostructure could achieve a very high sheet carrier density at the interface. For AlGaN/GaN heterostructure, the spontaneous polarization is $P_{SP}=P_{SP}\mathbf{z}$ (along the c-axis). On the other hand, the piezoelectric polarization can be calculated by

$$P_{PE} = 2\,\frac{a - a_0}{a_0}\left(e_{31} - e_{33}\frac{c_{13}}{c_{33}}\right) \qquad (1)$$

Where e_{33} and e_{31} are the piezoelectric coefficient, c_{13} and c_{33} are elastic constants, and a_0 is the lattice parameters.

For AlGaN, over the whole range of compositions, piezoelectric polarization is positive for compressive and negative for tensile barriers. On the other hand, the spontaneous polarization of GaN and AlN is negative. Fig.2-5 shows the directions of the spontaneous and piezoelectric

polarization in Ga- and N- face strained and relaxed AlGaN/GaN heterostrucutre.

At an interface of the AlGaN/GaN or GaN/AlGaN heterostructure, the polarization can decrease or increase within a bilayer which causes a polarization sheet charge density. The polarization sheet charge density can be defined by

$$\begin{aligned} \sigma &= P(\mathrm{top}) - P(\mathrm{bottom}) \\ &= \{P_{SP}(\mathrm{top})\} - \{P_{sp}(\mathrm{bottom}) + P_{PE}(\mathrm{bottom})\}. \end{aligned} \tag{2}$$

For the AlGaN/GaN and GaN/AlGaN, the amount of the polarization induced sheet charge density at interfaces is dependence on the Al-content x of the Al_xGaN layer. In order to calculate the polarization induced sheet charge density, the following set of linear interpolations between the physical properties of GaN and AlN is needed.

$$a(x) = (-0.077x + 3.189)10^{-10} \tag{3}$$

elastic constants:

$$C_{13}(x) = (5x + 103)\ \mathrm{GPa} \tag{4}$$

$$C_{33}(x) = (-32x + 405)\ \mathrm{GPa} \tag{5}$$

Piezoelectric constant:

$$e_{31}(x) = (-0.11x - 0.49)\ \frac{C}{m^2} \tag{6}$$

$$e_{33}(x) = (0.73x - 0.73)\ \frac{C}{m^2} \tag{7}$$

Spontaneous polarization:

$$P_{SP}(x) = (-0.052x - 0.29)\ \frac{C}{m^2} \tag{8}$$

Finally, the amount of the polarization induced sheet charge density for the undoped pseudomorphic N-face GaN/AlxGaN/GaN heterostructure is calculated:

$$|\sigma(x)| = |P_{PE}(Al_xGa_{1-x}N) + P_{SP}(Al_xGa_{1-x}N) - P_{SP}(GaN)|,$$

$$|\sigma(x)| = \left|2\ \frac{a(0)-a(x)}{a(x)}\left(e_{31}(x) - e_{33}(x)\frac{c_{13}(x)}{c_{33}(x)}\right) + P_{SP}(x) - P_{SP}(0)\right| \tag{9}$$

Fig.2-6 shows as the Al-content increasing, the piezoelectric and spontaneous polarizations of AlGaN are increasing. It means that sheet charge density caused by the different polarizations of AlGaN and GaN is also increasing.

2-3 GaN-based High Electron Mobility Transistors

2-3-1 Basic GaN HEMT operation principle [2-5]

AlGaN/GaN HEMT two dimension electron gas (2DEG) formation is totally different with GaAs HEMT. In AlGaAs/GaAs HEMT, the channel electrons come from the n-type AlGaAs. The electrons doped in the n-type AlGaAs drop into the GaAs layer, because the hetero-junction created by different band-gap materials. It forms the 2DEG channel where

electrons can move quickly without colliding with other atoms. However, the formation mechanism of GaN HEMT 2DEG is different from that in GaAs. Because the strong polarization field across the AlGaN/GaN heterojunction, the 2DEG could have sheet carrier density up to 10^3 /cm^2 without any doping. Actually, the spontaneous and piezoelectric polarizations lead to an altered energy band diagram and the electron distribution of AlGaN/GaN heterostructure. Basic GaN HEMT structure and band diagrams are shown in Fig. 2-7.

Similar to the traditional AlGaAs/GaAs HEMTs, in the operation of GaN HEMTs, a voltage signal applied to the gate electrode controls the current flow between the source and the drain electrodes. The small voltage variation on the gate causes the large changes in the external circuit.

2-3-2 GaN cap layer

In order to achieve high power, high efficiency, and high-reliability operation, GaN HEMT structure need to be optimized. An n-GaN cap layer on the top of AlGaN/GaN HEMTs has many effects improving the device performance and reliability. Firstly, n-GaN cap layer can suppress the current collapse and gate leakage current [2-6]. Fig.2-8 shows the simulation result of the electrostatic potential distribution in GaN HEMTs without an n-GaN cap layer. Compared with on-state and off-state, the high electric potential and strong electric field near the gate edge is observed in the off-state. The strong electric field might cause gate leakage current. Fig.2-9 is the simulation result of the electric field distribution around the gate region of undoped AlGaN-cap case and n-type GaN cap layer case. It shows the n-type GaN cap layer could effectively reduce the electric field around the gate edge in the off-state. Therefore, the gate leakage current can be reduced. In addition, the n-GaN cap layer could also improve the surface roughness and suppresses the surface oxidation that originates from Al [2-6].

2-3-3 Substrate choice

So far, the main reason that GaN could not be commercialized is also due to the substrate issue. Therefore, the selection of the suitable substrate is very important. For now, the common substrates for GaN HEMTs are SiC, sapphire and Si. Generally, high-power GaN HEMTs are fabricated on sapphire and SiC because of the potential for high-power high-frequency applications and confirmed the high current drivability [2-7]. The first successful epitaxial layer layers of GaN were grown on Sapphire. However, the very large lattice mismatch (14.8%) and the difference in the thermal expansion coefficient between GaN and sapphire substrate cause the huge challenges in the grown of nitrides. Although the challenges have been solved, the low thermal conductivity is still an unneglectable problem. Compared with sapphire, SiC has less lattice mismatch (4%) with GaN and very good thermal properties, which is nearly 10 times more than that of sapphire. Therefore, SiC is more and more popular. Yet, SiC is too expensive to be commercialized. Recently, GaN HEMTs grown on silicon substrate can reduce material expenses and to be compatible with Si technology which is more possible to be commercialized. [2-2][2-5]

Material	Band Gap Energy (eV)	Breakdown voltage (MV/cm)	Thermal Conductivity (W/cm*K)	Mobility ($cm^2/V*s$)	Saturated Velocity ($*10^7$ cm/s)
Si	1.1	0.3	1.5	1300	1.0
GaAs	1.4	0.4	0.5	8500	2.0
GaN	3.4	3.3	1.3	800	2.7

Table.1 Material properties of GaN, GaAs and Si at 300 K for microwave power device applications.

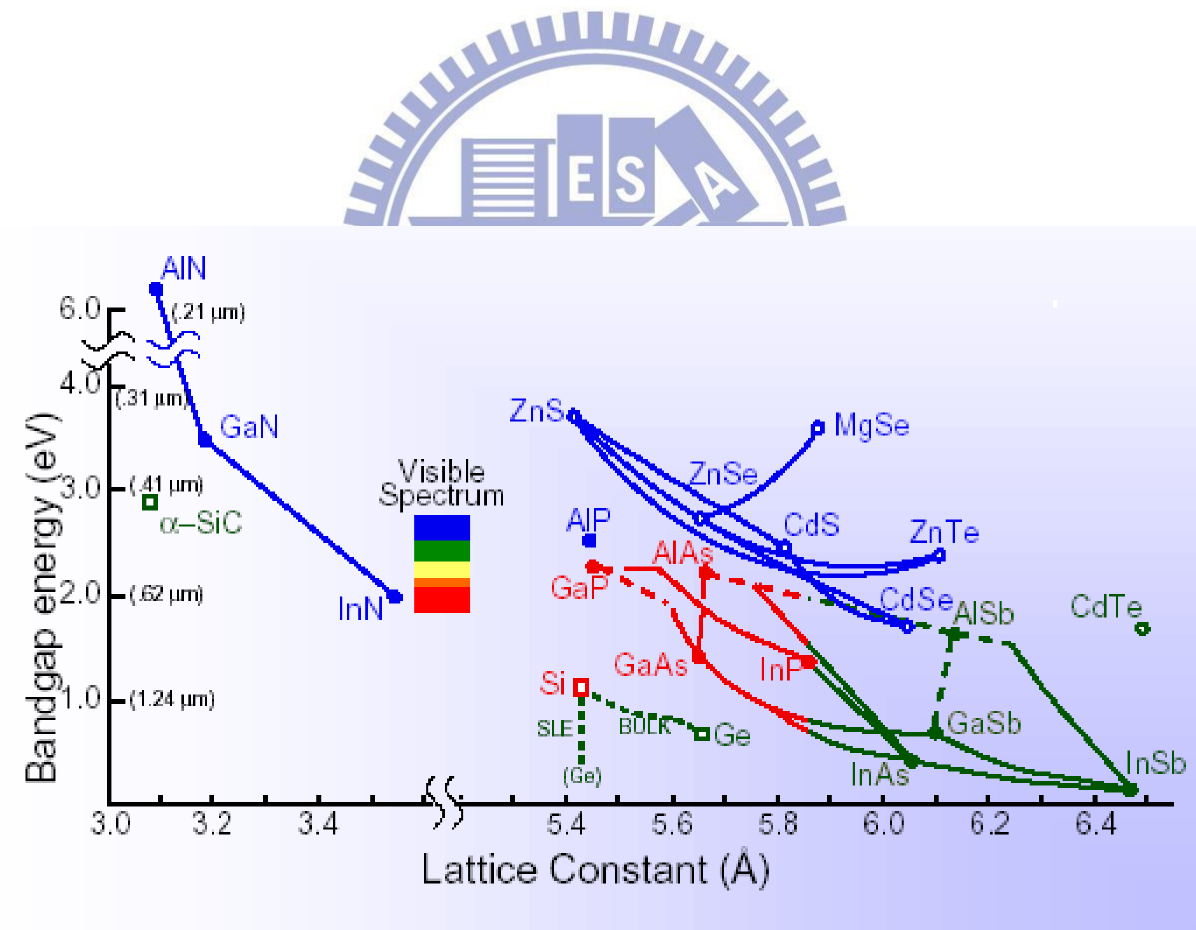


Fig. 2-1 Band gap (E_g) versus lattice constant for semiconductor materials.

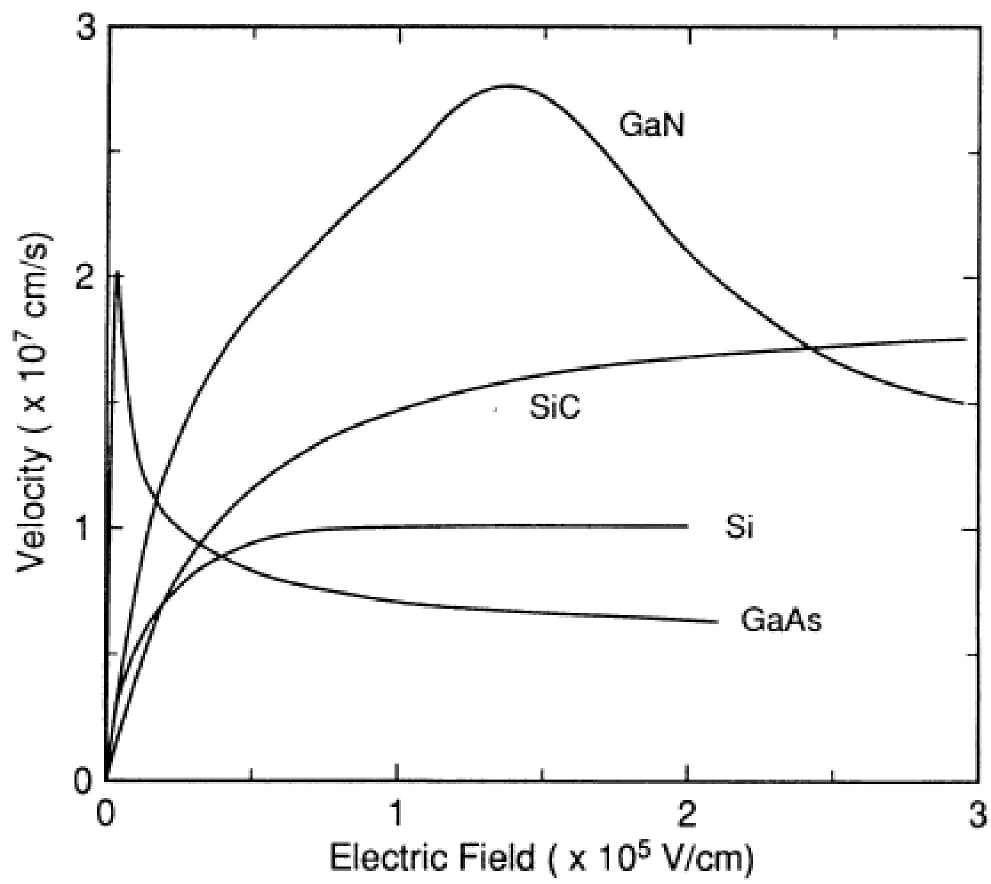
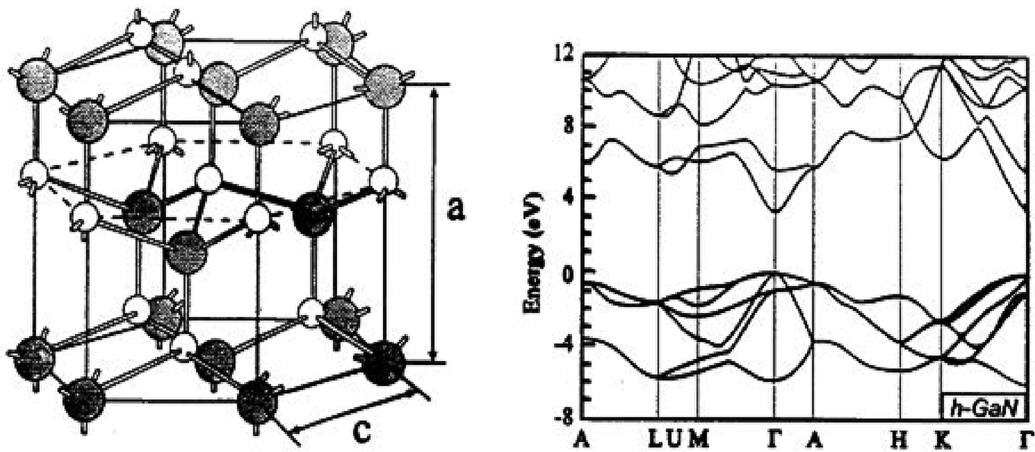


Fig.2-2 Electron drift velocity o f GaN, SiC, Si and GaAs at 300 K computed using the Monte Carlo technique [3].

GaN Wurtzite



GaN Zinc Blende

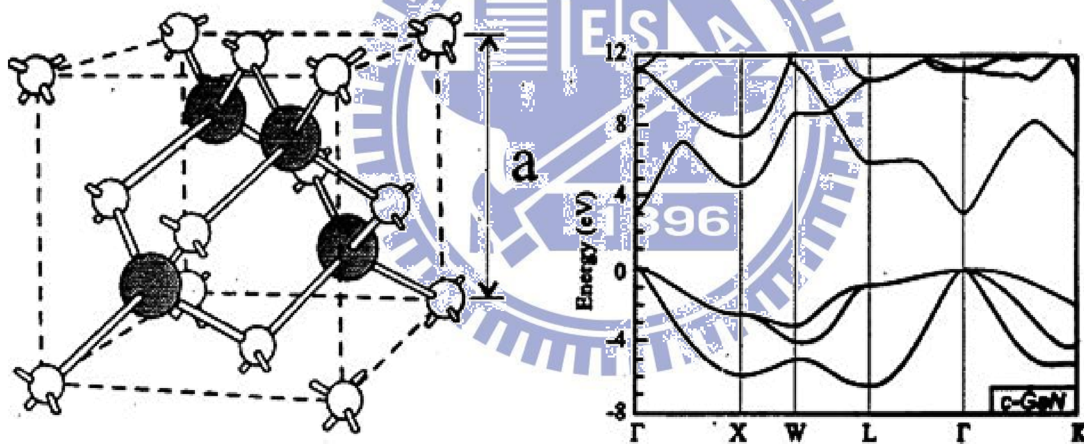


Fig.2-3 Schematic drawing of the crystal and energy band structure of wurtzite GaN and Zinc Blende GaN [3].

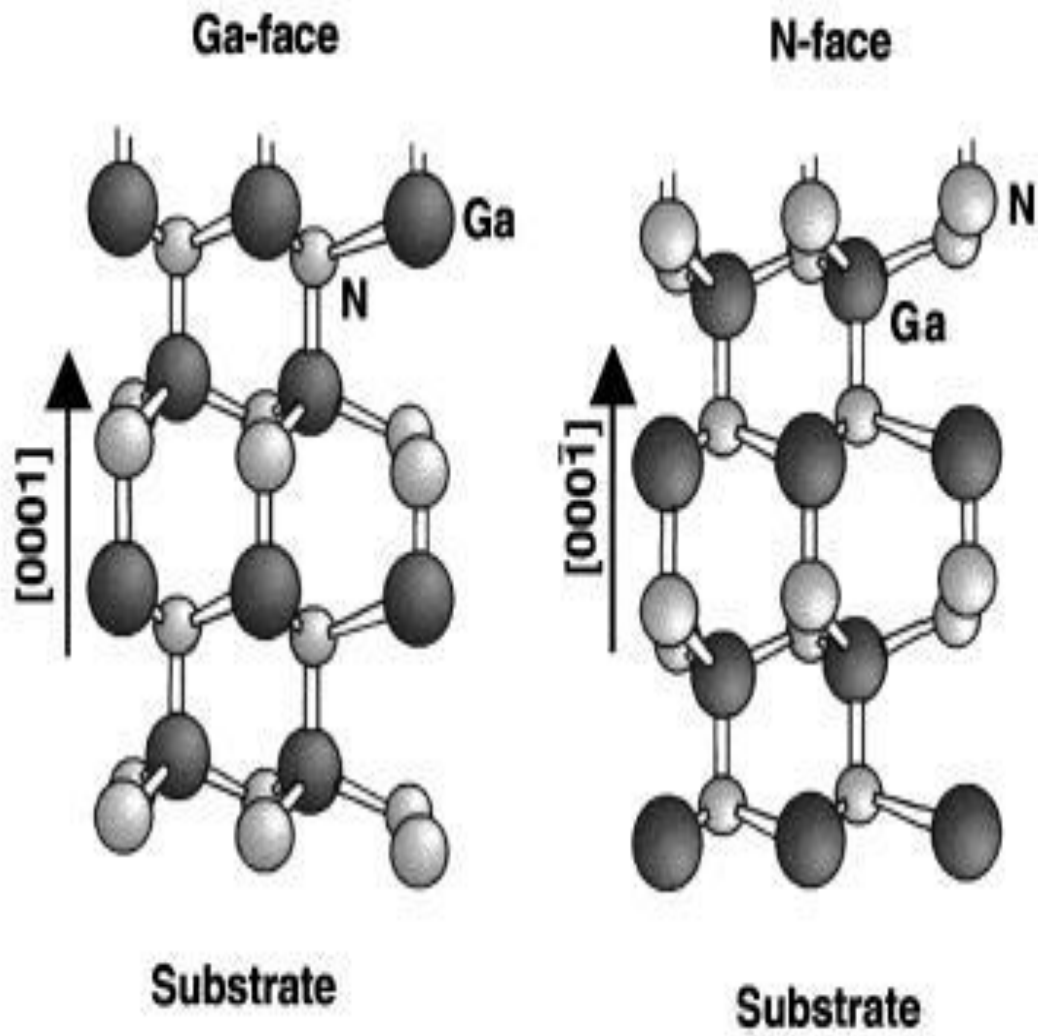


Fig.2-4 Schematic drawing of the crystal structure of wurtzite Ga-face and-face GaN [3].

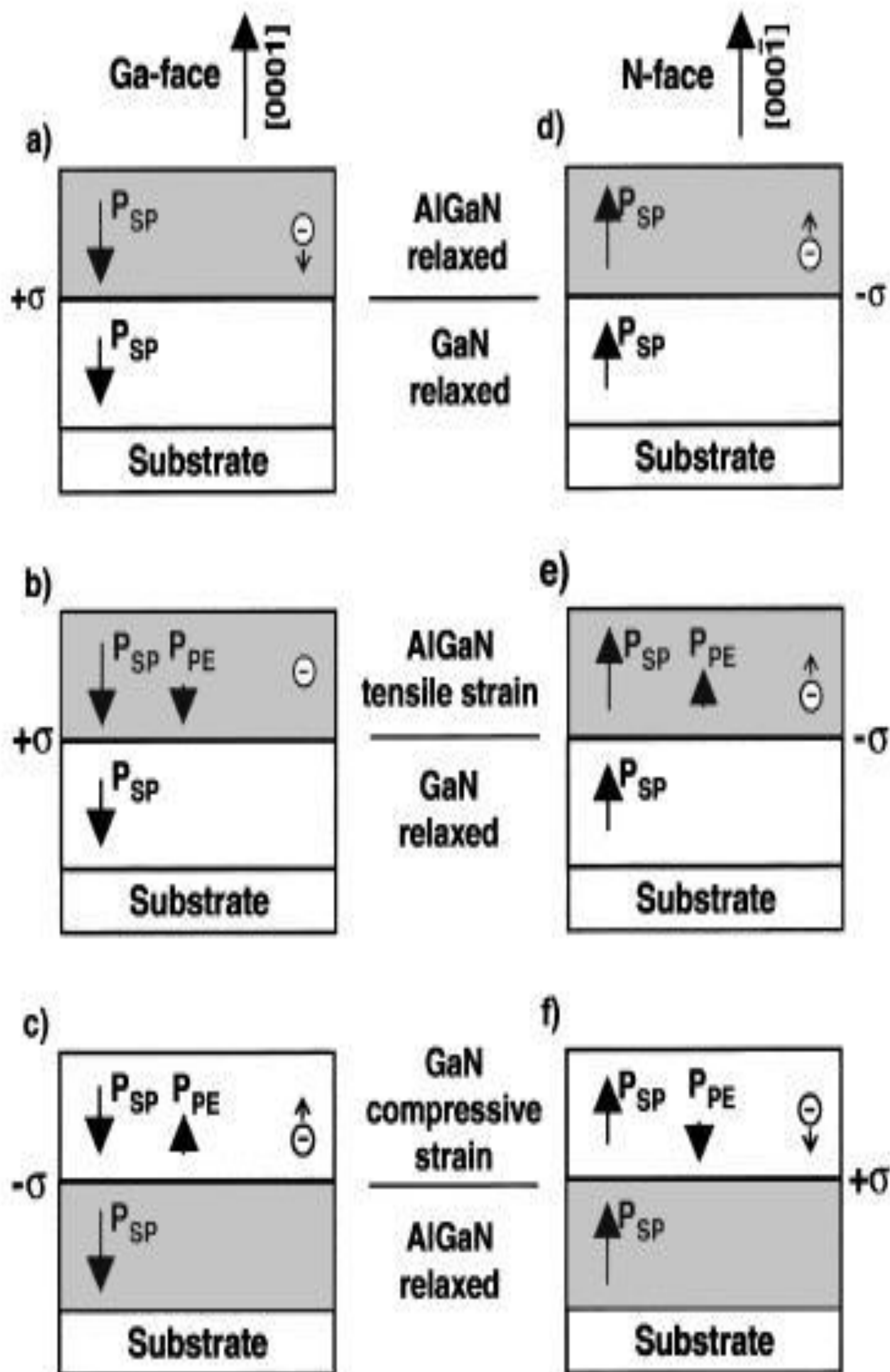


Fig.2-5 Polarization induced sheet charge density and directions of the spontaneous and piezoelectric polarization in Ga- and N-face strained and relaxed AlGaN/GaN heterostructures [3].

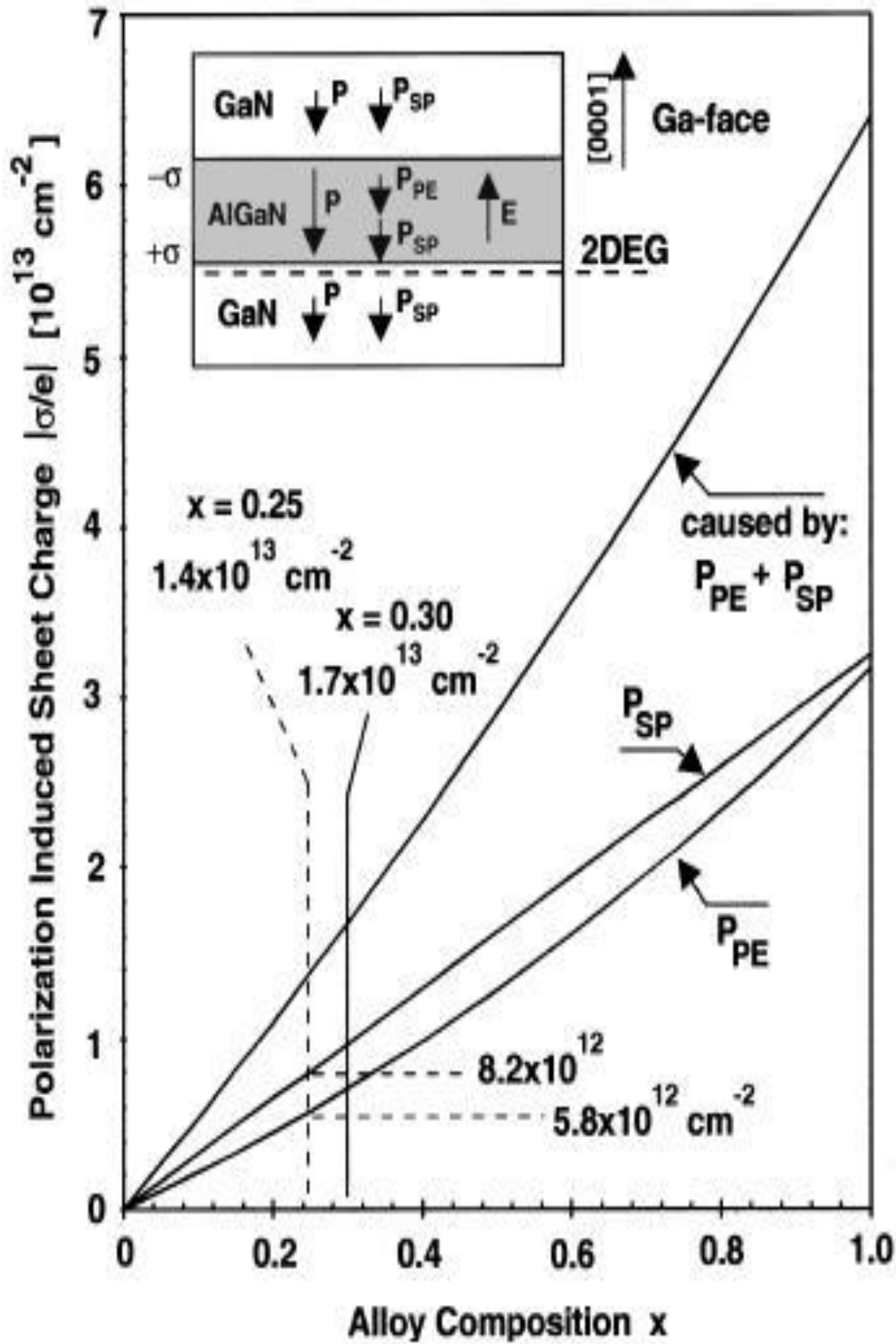
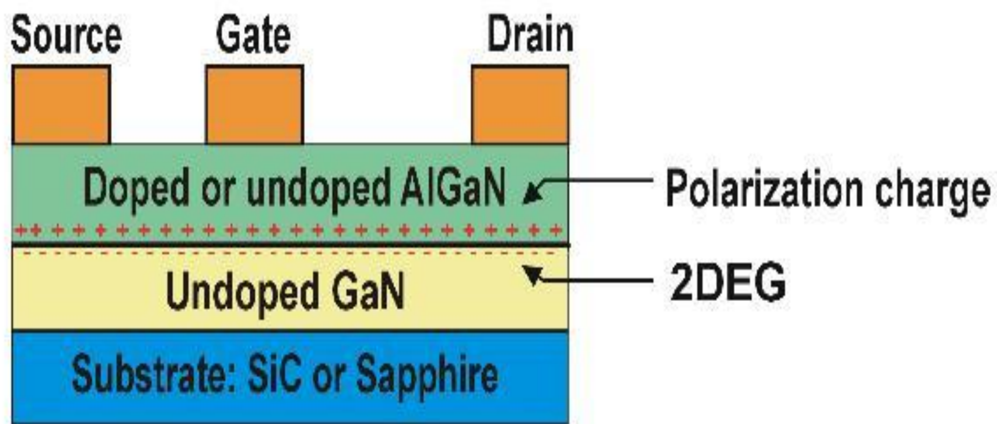


Fig.2-6 Calculated sheet charge density caused by spontaneous and piezoelectric polarization at the lower interface of a Ga-face GaN/AlGaN/GaN heterostructure vs. alloy composition of the barrier [3].



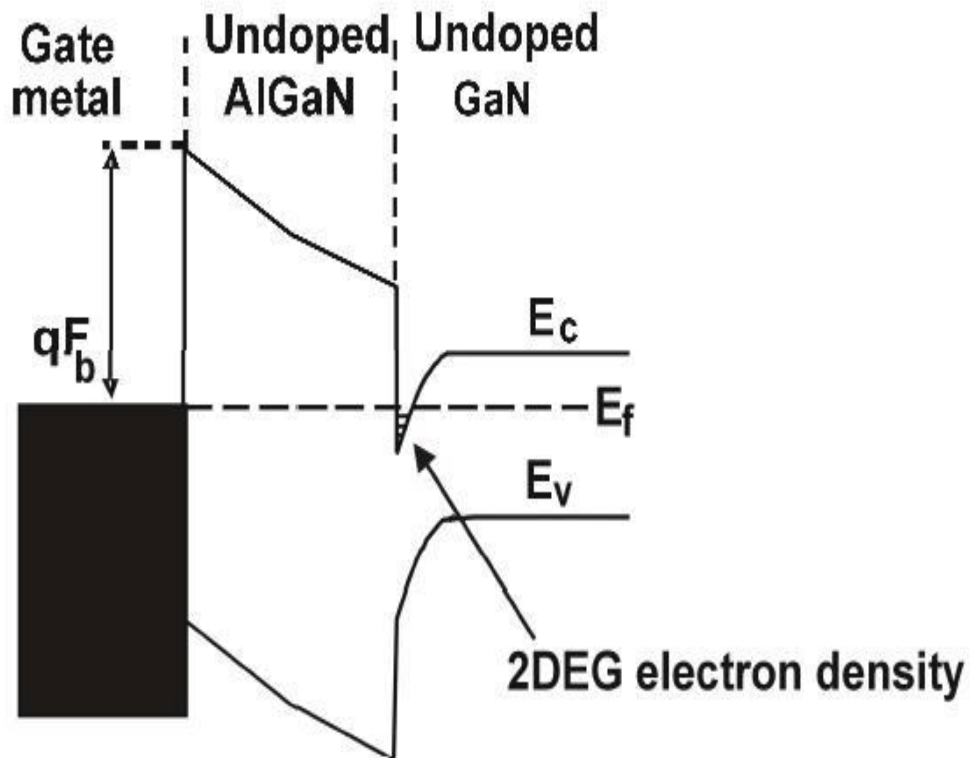


Fig.2-7 Basic structure and its band diagram AlGaN/GaN HEMT [5].

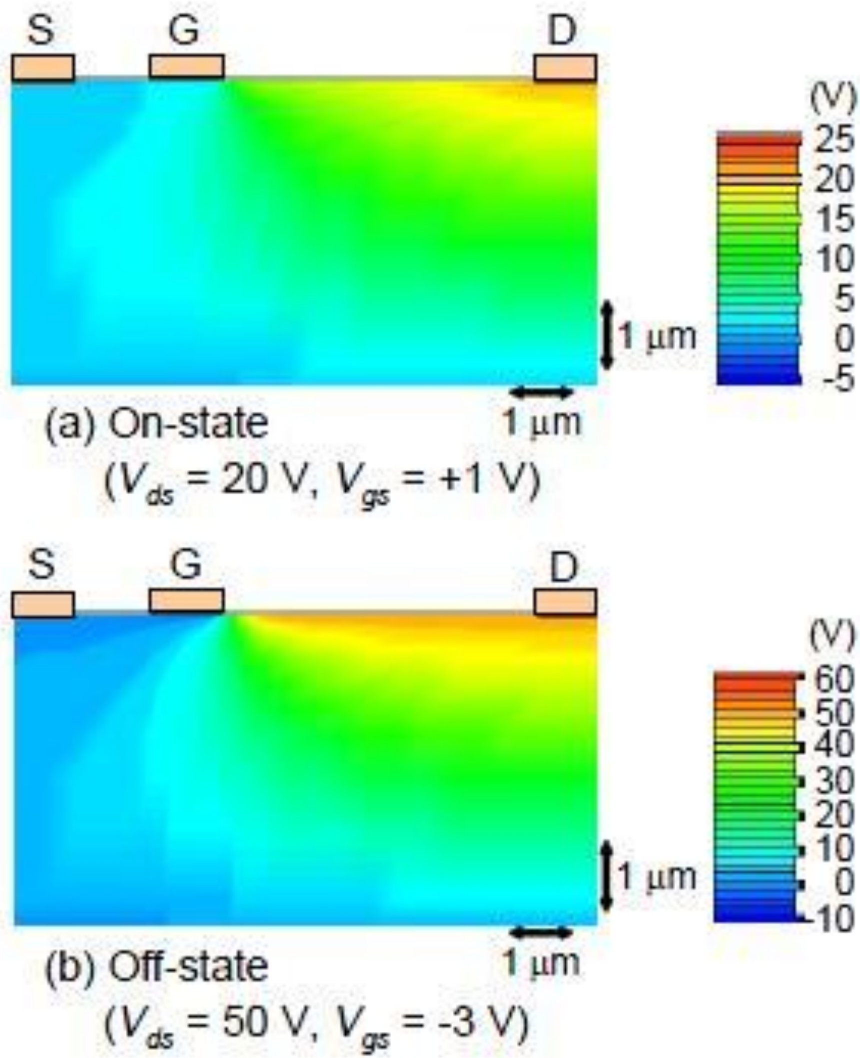


Fig.2-8 Device simulation results of the electrostatic potential distribution of a GaN HEMT without a GaN cap layer under (a) on-state and (b) off-state conditions [6].

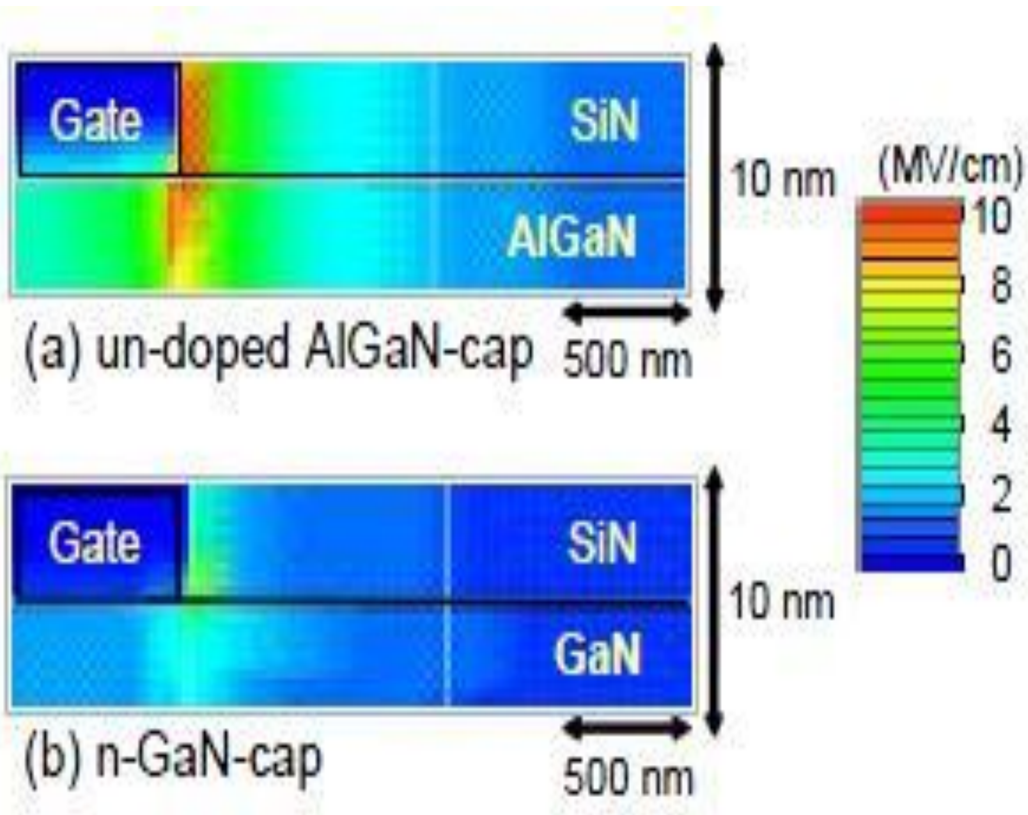


Fig.2-9. Device simulation results of the distribution of electric field magnitude on the edge of the gate nearest the drain for (a) the undoped AlGaN-cap case and (b) the n-GaN-cap case. These devices are simulated under pinched-off conditions [6].

Chapter 3

Basic Intermodulation of RF Power Amplifier

Nonlinear distortion

In an ideal condition, when the information is transferred across a medium, there are not any losses or interferences. In fact, the desired information is often added unwanted signals, such as random noise and distortion. The random noise is not correlated with the information, while distortion is a strong function of information carrying signal. Thus, intermodulation distortion plays an important role in microwave and RF amplifier. Distortion comes from the communication subsystem, such as antennas, amplifiers, mixers and converters. These active devices are nonlinear. The nonlinearity characteristics of active devices cause the distortion [3-1].

There are some merits for linearity of active devices.

(1)Gain compression/P_{-1dB} point

(2)Harmonic distortion

(3)Phase distortion

(4)Intermodulation distortion

(5)Third order intercept point (IP3/ TOI)

(6)Adjacent channel power ratio (ACPR)

These merits are introduced in the following:

3-1 Gain compression / P_{-1dB}

Transistors can be an active device to amplify the electrical signal. In ideal, these devices could amplify the input signal with a constant gain. In fact, the real devices have an input versus output characteristic as shown in Fig. 3-1 which is different with the perfect linear amplifier.

From the Fig.3-1, gain decreases after a specific input or output power. As the gain is 1dB less than the linear gain, the output power is defined as P_{-1dB}.

3-2 Harmonic distortion

Harmonic distortion is defined as a single-tone distortion product caused by device non-linearity [3-2]. In ideal case, the frequency of output power is the same as the input signal frequency. However, due to the nonlinearity, the amplifier generates spurious output signals as the non-linear device is stimulated by a signal at frequency f_1. When additional frequency is multiples of the signal frequency ($2f_1$,$3f_1$, $4f_1$,…..Nf_1), the specific frequency components are called harmonic distortion. The order of the distortion product is defined by the multiplier; for example, the second harmonic is a second order product. Fig. 3-2 shows the Harmonic distortion.

3-3 Intermodulation distortion

Intermodulation distortion is a multi-tone distortion product that results generated when two or more signals are present at the input of non-linear device [3-2]. In reality, all transistors exhibit a degree of non-linearity that caused the spurious products which related to the original input signals. In order to simplifying the analysis, it commonly limits the analysis to two-tones. The frequencies of the two-tone intermodulation products can be expressed as:

$Mf_1 + Nf_2$, where $M, N = 0,1,2, \ldots ....$

The order of the product is the sum of M+N. For example, the second order intermodulation products of two signals at f_1 and f_2 are f_1+f_2, f_2-f_1, $2f_2$ and $2f_1$ as how in Fig.3-3.

3-4 Third order intercept point [3-1]

The output of harmonically related products will change at a rate exponential to the change of the input signal. For an amplifier, the output curve is the function of the input curve which can be expressed by Taylor series as:

$$v_0 = a_0 + a v_i^2 + a_2 v_i^2 + a_3 v_i^3 + \cdots \qquad (1)$$

When applying a pure sine wave into an amplifier, the output signal will consist of the amplifier signal and higher harmonics. Among all of the harmonic distortion, the second order products can be filtered out by a filter. However, for a modulated signal, the output signal will contain the mixing products which fall in pass band and can’t be filtered out. The mixing products are called intermodulation distortion products.

The simplest modulated signal is a two-tone signal which can be written as:

$$x = A(\sin f_1 t + \sin f_2 t) \qquad (2)$$

Therefore, we can replace the input voltage V_{in} by the two-tone signal. Fig.3-4 shows the output spectrum of a device excited with two-tone signal. Among all intermodulation distortions, third-order intermodulation distortion (IM3) which at $(2f_1-f_2)$, $(2f_2-f_1)$ dominates the linearity performance of the device due to falling inside the Pass band. If the input signal

is increased by a factor x, the IM3 products would increase by x^3.It means the slope if the third order component is three times than the slope of input versus output power. If we can increase the input power while maintaining the slope, the IM3 curve will intercept with the curve at a certain point. This point is called third order intercept point (IP3).In addition, the out power of IP3 is defined as TOI or OIP3 and the input power of IP3 is defined as IPP3, as shown in Fig.3-5. The IP3 is an important criteria of defining the device linearity. Intercept point of any order can be expressed as:

$$\mathrm{IP_n[dB]} = \mathrm{P_{out(fund.)}[dB]} + \frac{\mathrm{(Supression)_n}}{\mathrm{(n-1)}}\mathrm{[dB]} \qquad (3)$$

Where

$$\mathrm{(Suppression)_n[dB]} = \mathrm{P_{out(fund.)}[dBm]} - \mathrm{P_{out(IM_n)}[dBm]} \qquad (4)$$

For n=3, the IP3 would be expressed as:

$$\mathrm{IP_3[dbm]} = \mathrm{P_{out(fund.)}[dBm]} + \frac{\mathrm{P_{out(fund.)}} - \mathrm{P_{out(IM3)}}}{2}\mathrm{[dBm]} \qquad (5)$$

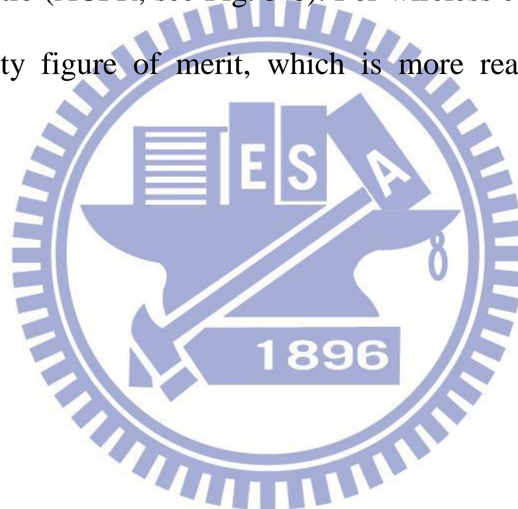
Moreover, the real difference between the output power of the fundamental tone and IM3 tone is defined as carrier to intermodulation (C/I) ratio. Thus, the TOI could be expressed as:

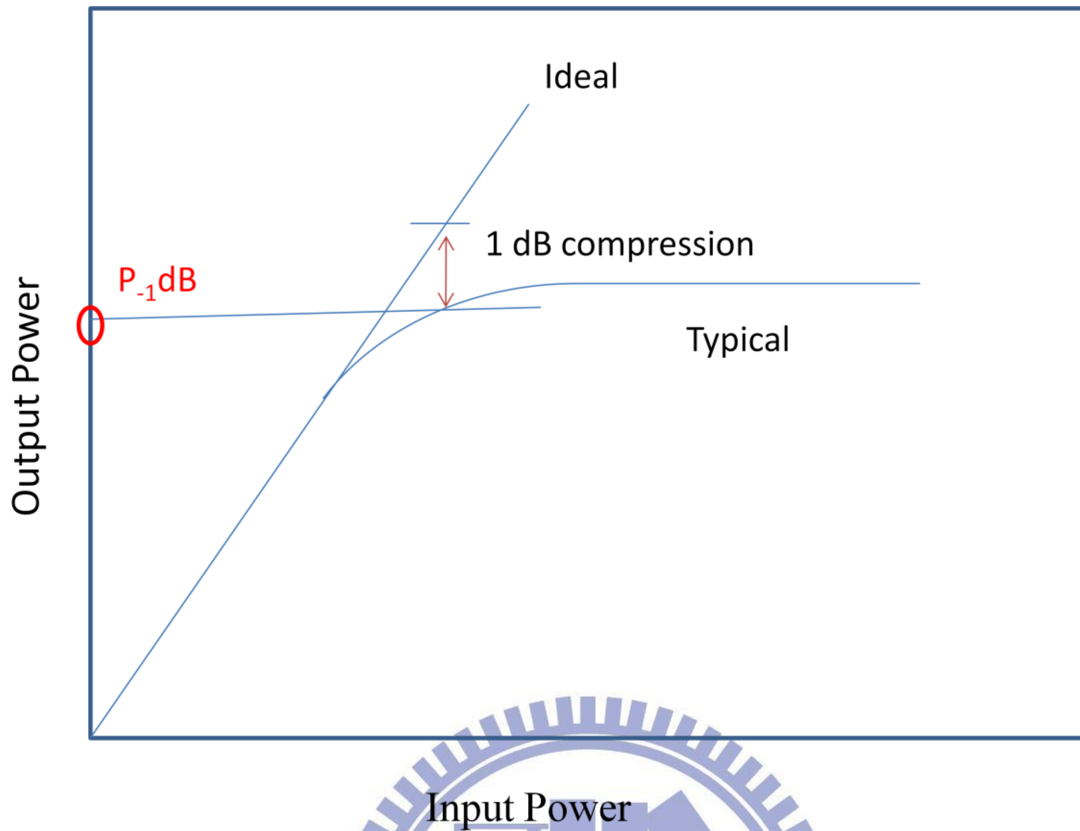
$$\mathrm{TOI[dBm]} = \mathrm{P_{out(fundamental)}[dBm]} + \frac{1}{2}\left(\mathrm{C}/_{\mathrm{I}}\right)\mathrm{[dB]} \qquad (6)$$

where, $\mathrm{C}/_{\mathrm{I}}\,\mathrm{[dB]} = \mathrm{P_{out(fundamental)}[dBm]} - \mathrm{P_{out(IM3)}[dBm]}$

3-5 Adjacent channel power ratio (ACPR)

The most common way to measure the intermodulation distortion products is the two-tone signal measurement. The amplitude of two-tone signal is modulated like signal with suppressed carrier. If we excite the device with a multi-tone signal, a broad spectrum of the distortion product can be observed. Fig.3-6 shows an output spectrum of an amplifier excited with multi-tone signal and wide band signal. When the channels are defined, we can measure the ratio of total power in the signal and the power in the side band. The measurement is adjacent channel power ratio (ACPR, see Fig. 3-6). For wireless communication applications, ACPR provides a linearity figure of merit, which is more realistic than intermodulation distortion [3-1].





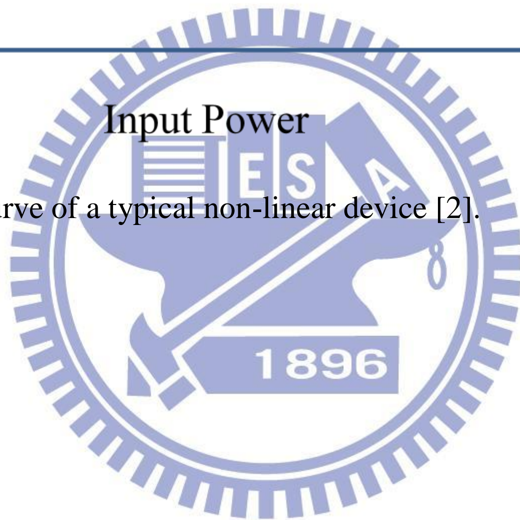


Fig.3-1 Input vs. output curve of a typical non-linear device [2].

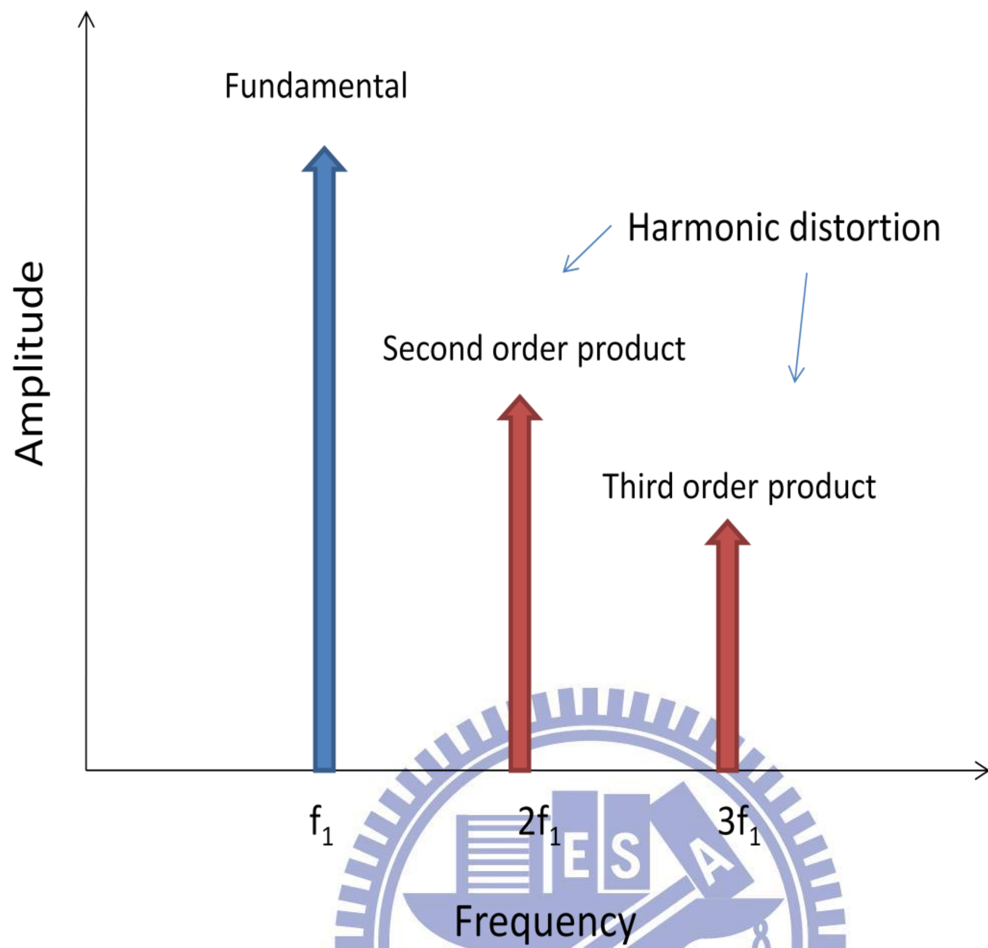


Fig.3-2 The harmonic distortion of a typical non-linear device [2].

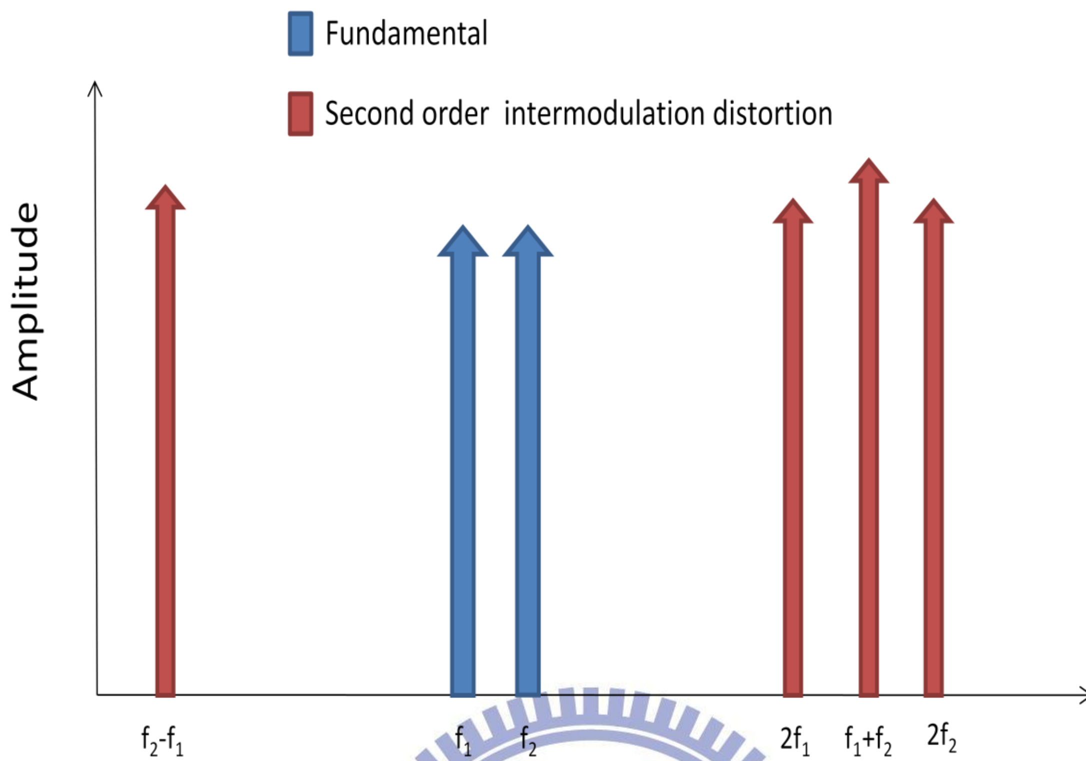
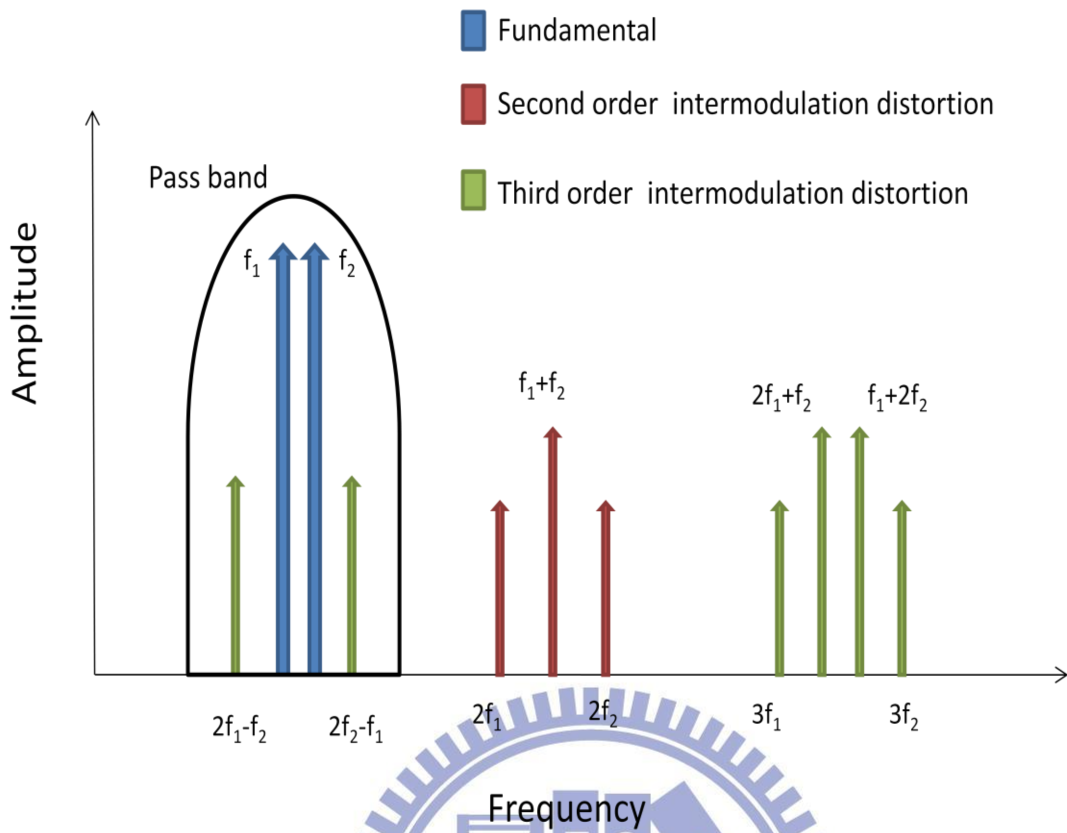


Fig.3-3 Second order intermodulation distortion [2].



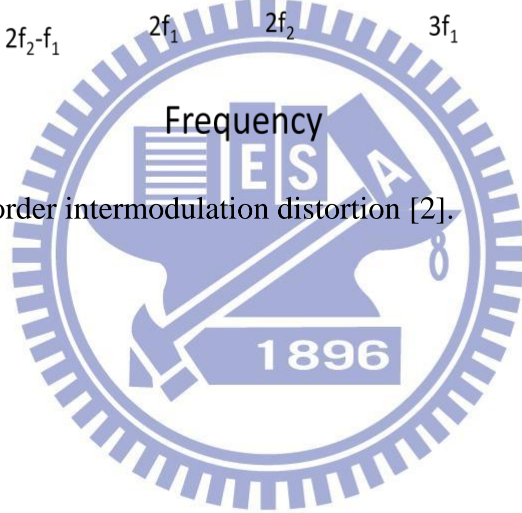


Fig.3-4 Second and third order intermodulation distortion [2].

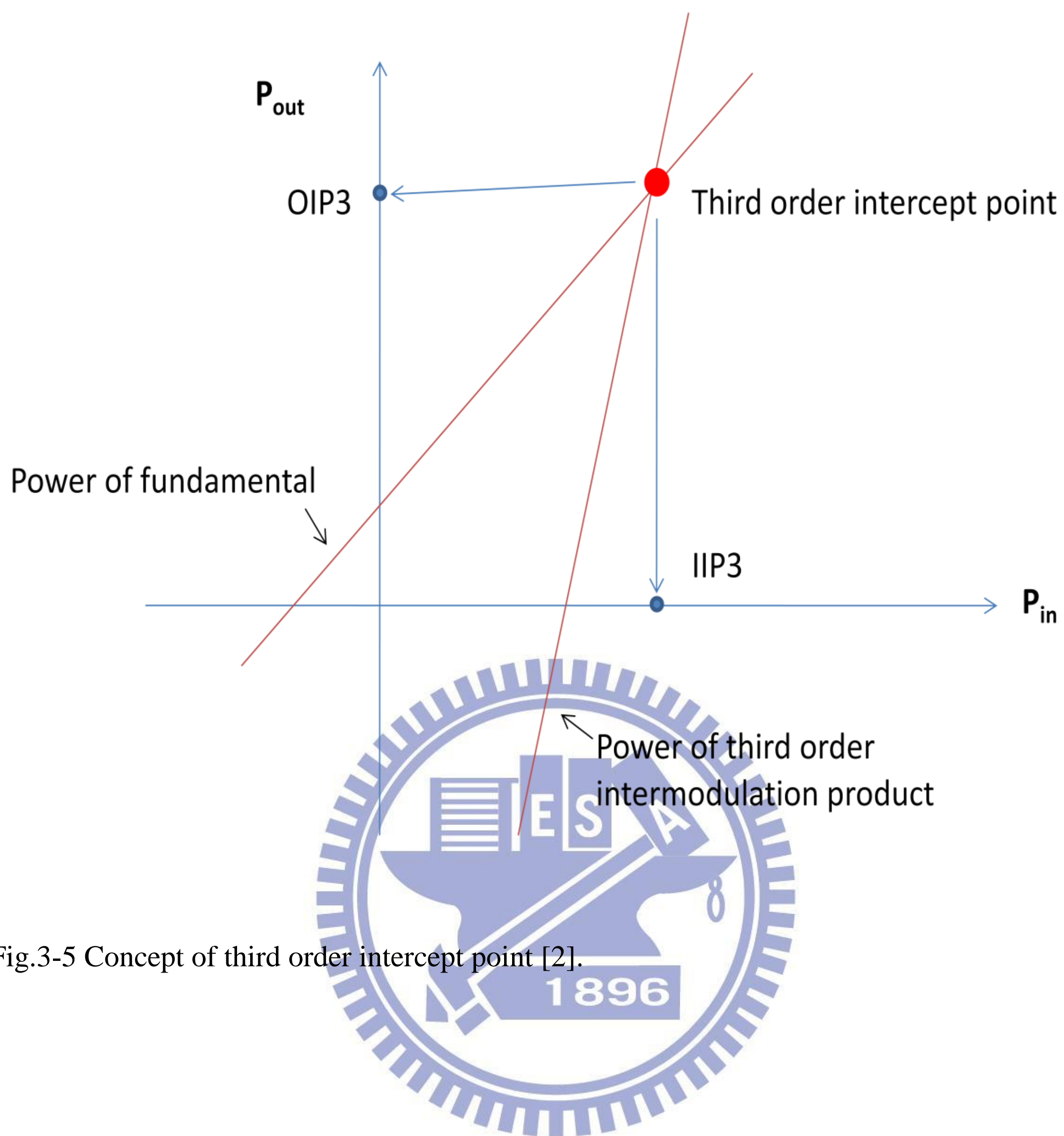
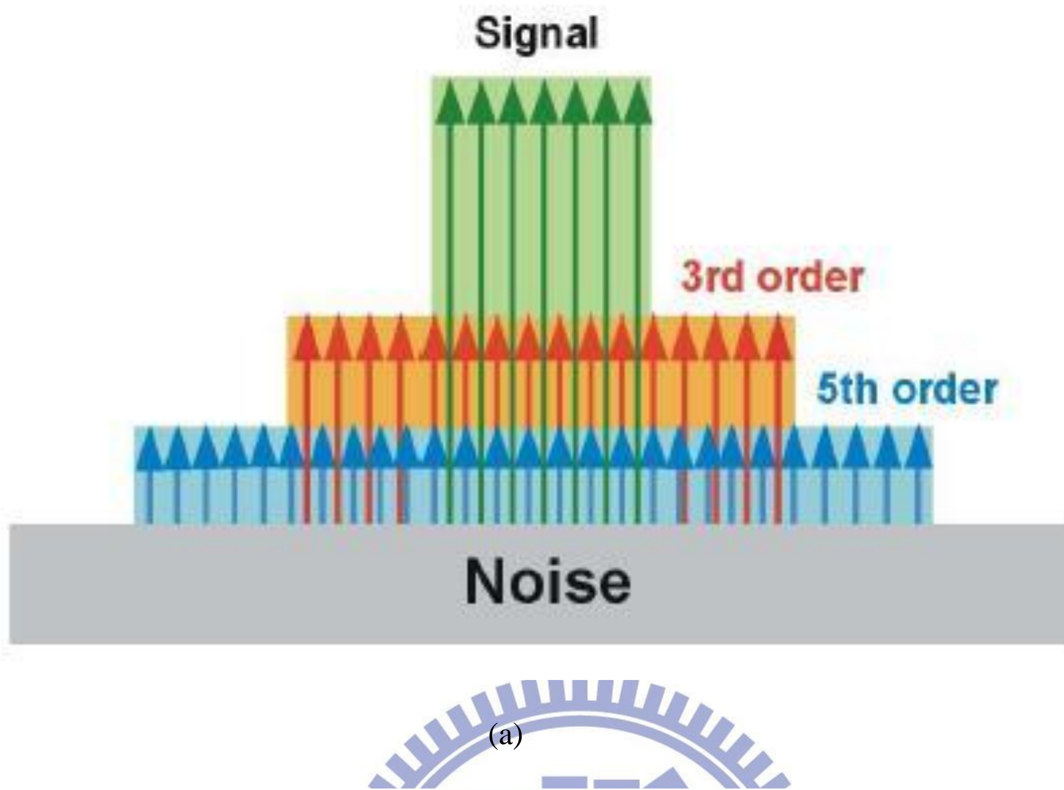
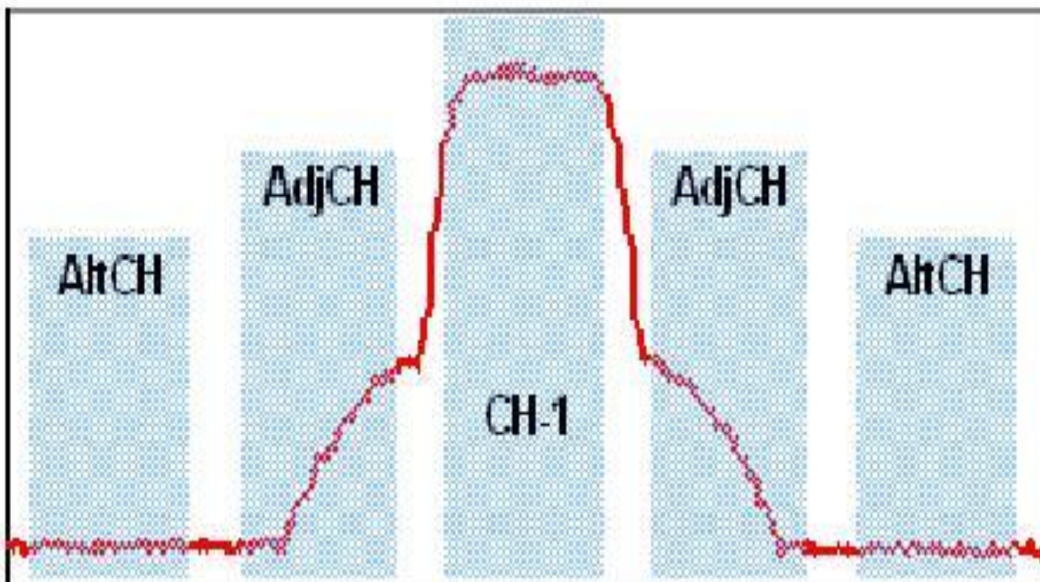


Fig.3-5 Concept of third order intercept point [2].



(a)



(b)

Fig.3-6 The output spectrum of a device excited with (a) multi-tone signal (b) wide band signal where the abscissa and ordinate correspond to frequency and power accordingly.[1]

Chapter 4

Fabrication of AlGaN/GaN high Electron Mobility Transistors

Device fabrication

The device processing started with ohmic contact formation. Ohmic metal Ti/Al/Ni/Au was evaporated by e-gun system, and then annealed at 800℃ for 1min in N_2. After that, active region of the device was defined by the mesa isolation process, and dry etch process was controlled by inductive couple plasma (ICP) with Cl_2 in Ar ambient. Then, electron beam (EB) lithography with tri-layer photoresists was applied for the fabrication of T-shaped gate. The Ti/Pt/Au T-gate was centered in the source/drain space. A 100 nm thick Si_3N_4 passivation film was deposited by plasma-enhanced chemical vapour deposition (PECVD) at 300℃. Finally, the nitride via was opened by CF_4 RIE etching.

4-1 Source and drain formation (Ohmic contact formation)

Firstly, the GaN wafer was immersed in ACE and IPA. This step was used to remove the surface particles and contaminates, as shown in Fig.4-1. Secondly, the photoresist AZ5214E and I-line aligner were used to define the ohmic region [4-1]. According to the characteristic of AZ5214E, the undercut profile which benefits the metal life-off process could be easily fabricated. Before the ohmic metal deposition, HCl: H_2O = 1: 10 solution was used to remove the native oxidation on the GaN surface. Then, ohmic multilayer Ti/Al/Ni/Au was evaporated by e-gun system, and then wafer was dipped in ACE for lift-off process (see Fig.4-2). After lift-off process, multilayer ohmic metal was annealed at 800℃ for 60 sec in N_2. The metal contact becomes ohmic after the RTA process. Finally, the specific contact resistance could be

extracted by the transmission line method.

4-2 Active region formation (mesa isolation)

The active region of the device was defined by the mesa isolation process, as shown in Fig.4-3. The positive photoresist S1818 was used to masked the active region, and then dry etch process was controlled by inductive couple plasma (ICP) with Cl_2 in Ar ambient. After the dry etch process, the etching depth which should reach the buffer layer and measured by α-step. Finally, the photoresist was striped by ACE.

4-3 Gate formation (Electron Beam lithography for nanometer gate)

The electron beam (EB) lithography with tri-layer photoresists was applied for the fabrication of T-shaped gate. T-shaped gate structure was the most common approach for achieving low gate resistance and a small gate foot [4-1]. Before the gate metal deposition, the remnants photoresist was remove by the ICP with Ar and O_2 ambient, and then the wafer was immersed in $HCl:H_2O=1:4$ to remove the negative oxidation. Finally, the multilayer Ti/Pt/Au (200Å /400Å /1800Å) metals were deposited, as shown in Fig.4-4.

4-4 Device passivation

The surface passivation process was used to protect device from the mechanical damages and environmental contaminates. For GaN, SiN passivation layer can also eliminate the surface trapping effects that produce the frequency-dependent current [4-2]. Before the passivation, device was dipped in ACE and IPA to clean the surface. There are also some

pretreatments for GaN, such as dipping in the NH_4OH-based solution. And then, PECVD system with process pressure of 900 mtorr, process temperature of 300℃, process time of 15 min, and process gases of silane, ammonia, and nitrogen was used for depositing the silicon nitride film. After the passivation process, the nitride via was opened by CF_4 RIE etching.

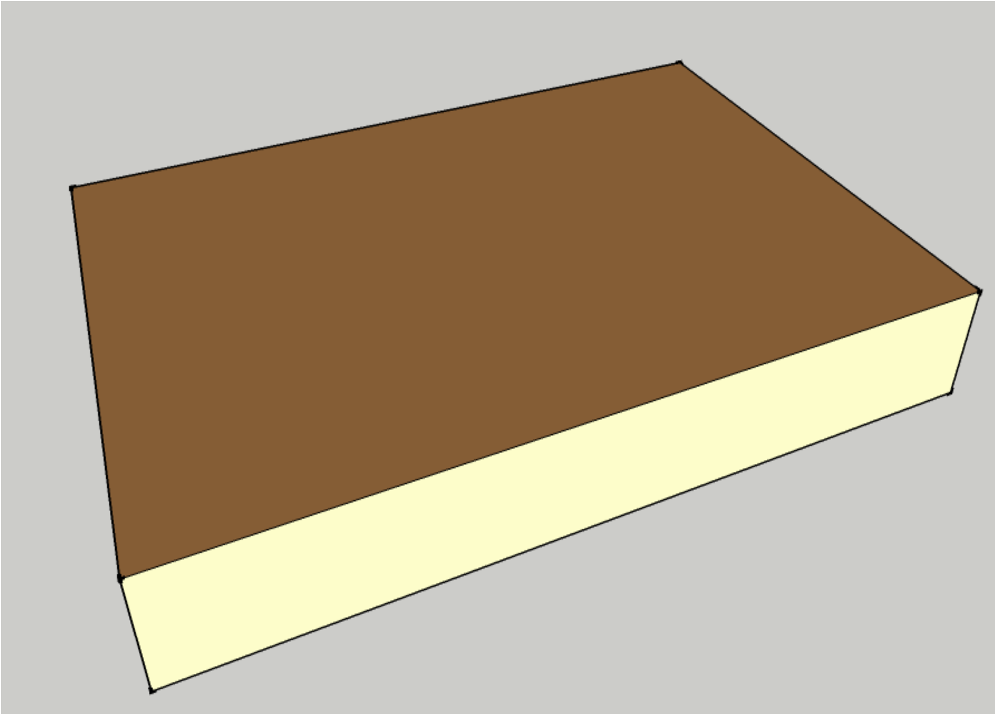


Fig.4.1 The whole wafer

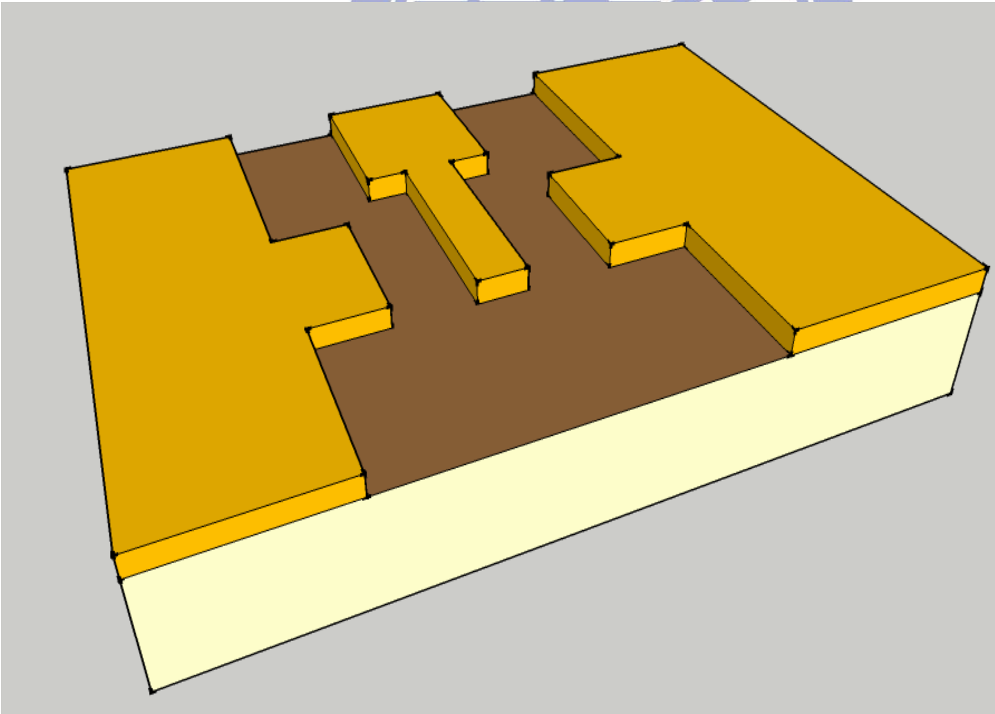


Fig.4.2 Ohmic formation

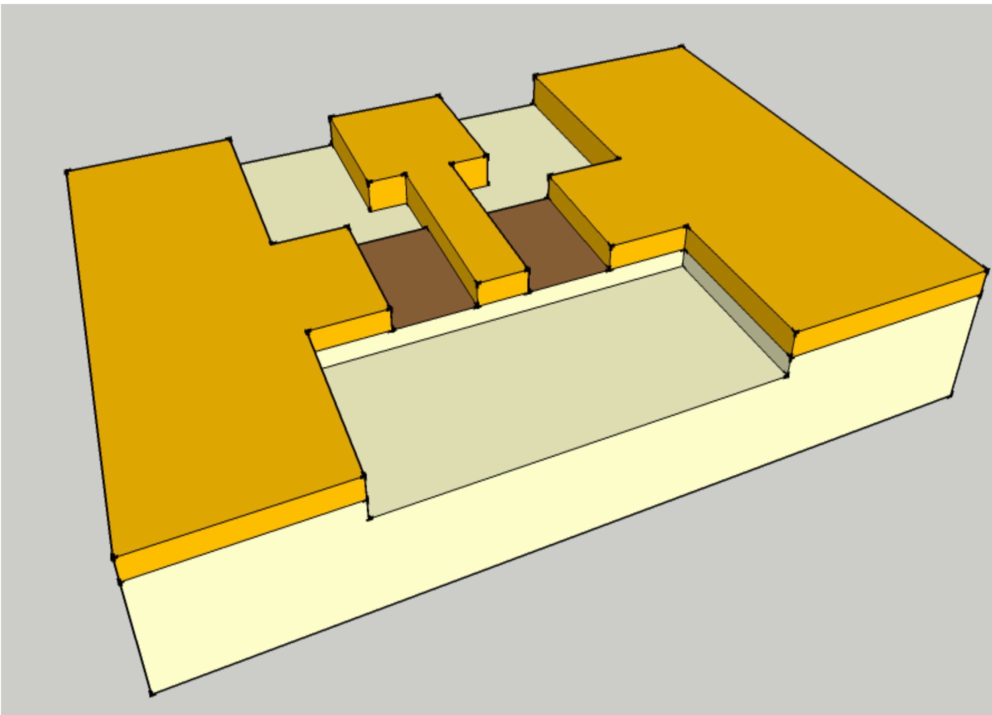


Fig.4.3 Mesa isolation

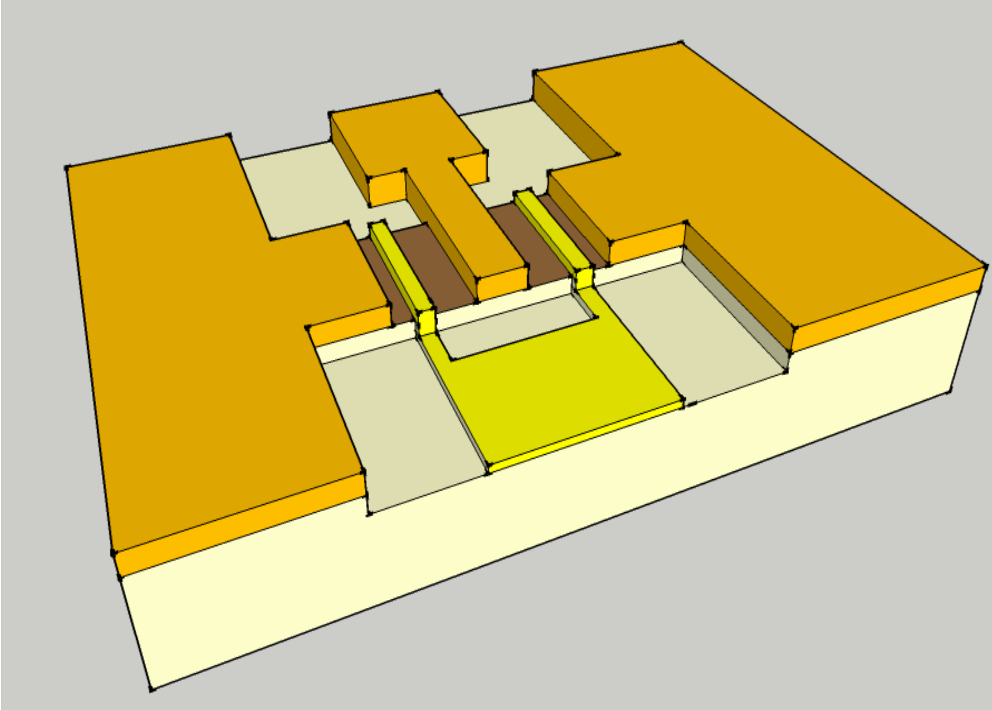
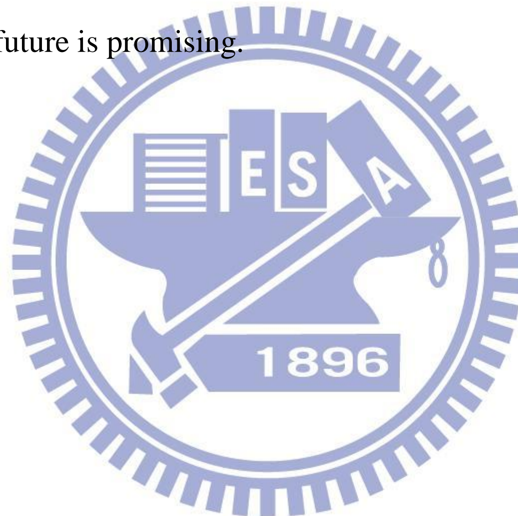


Fig.4.4 Gate formation

Chapter 5

An 80-nm AlGaN/GaN High Electron Mobility Transistors (HEMTs) on Silicon Substrate

We report on the high frequency characterization of 80 nanometer gate length AlGaN/GaN High Electron Mobility Transistors (HEMTs) on silicon substrate. The device achieves a maximum drain current 810mA/mm, and a maximum transconductance (Gm) 265mS/mm, while a cutoff frequency is 36 GHz when V_{DS} is 5V. The outstanding results show that AlGaN/GaN HEMTs grown on silicon to reduce material cost and to be compatible with Si technology in the future is promising.



5-1. Introduction

Due to the rapid development of the RF power electronics, the demand of a high output power density and high input impedance transistor is inevitable. GaN-based high-electron-mobility transistors which can operate at high power and high frequency meet the needs of personal mobile communication, TV broadcasting and satellites in the future [5-1]. Generally, high-power GaN HEMTs are fabricated on sapphire and SiC because of the potential for high-power high-frequency applications and confirmed the high current drivability [5-2]. However, GaN HEMTs grown on silicon substrate can reduce material expenses and to be compatible with Si technology which is more possible to be commercialized [5-1, 5-5].

In this study, we present the electrical and reliability characteristics of 80 nm AlGaN/GaN HEMTs fabricated on Si substrates. The DC characteristic such as I-V curve and transconductance (g_m) are measured, while the specific contact resistance between contact metal and cap layer can be extracted by the transmission line model (TLM) method. In addition, the off-state breakdown is showed to demonstrate that the short-channel effect influences the device performance. Finally, the cutoff frequency is deduced from S-parameter measurement and clearly discussed.

5-2 Device Fabrication

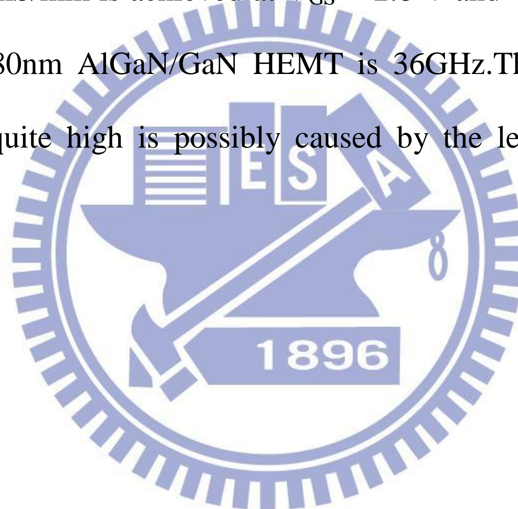
AlGaN/GaN HEMTs grown on Si substrate using molecular beam epitaxial technique were fabricated. Hall measurement shows that an electron mobility about 1600 $cm^2V^{-1}s^{-1}$ and a sheet carrier density of 1×10^{13} cm^{-2}. Device processing started with ohmic contact formation that the photoresist AZ5214E and I-line aligner were used to define the ohmic

metal pattern. Hydrochloric acid based solution was used to remove the native oxide before depositing ohmic metal Ti/Al/Ni/Au which was evaporated by e-gun system. The ohmic contact was improved by annealing at 800℃ for 1min in N_2. Then, the mesa isolation process is used for the definition of active region. Using Shiply S1818 photoresist to protect the active region, the dry etch process was controlled by inductive couple plasma (ICP) with Cl_2 and Ar ambient. In next step, electron beam lithography with tri-layer photoresists was applied for the T-shape gate. The 80nm Ti/Pt/Au T-gate were centered in a 5μm source/drain space, as shown in Fig.5-1. A 100 nm thick Si_3N_4 passivation film was deposited by plasma-enhanced chemical vapour deposition at 300℃ [5-6]. After the passivation process, the nitride via was opened by CF_4 RIE etching for interconnections. The devices are 2 x 50 μm gate width with drain-gate spacing about 2.46 μm, and gate length of 80nm.

5-3 Results and Discussion

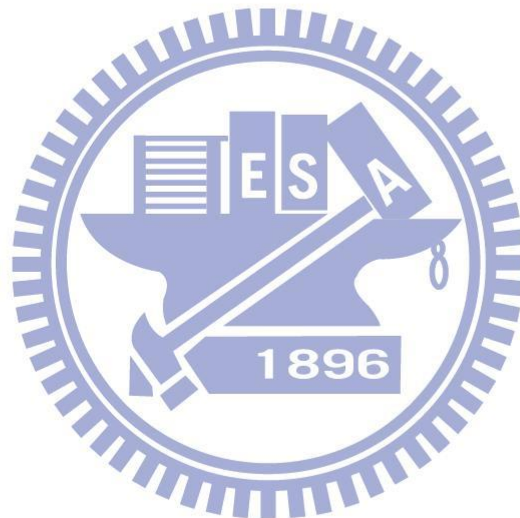
According to transmission line method measurement, the ohmic resistance is about 2.8×10^{-6} Ohm-cm^2. Fig.5- 2 shows the representative current-voltage (I-V) characteristics of 80nm gate length HEMT. The static output characteristics were measured for the range V_{DS}=0 to 10 V with V_{GS}=0 to -5 V, while a maximum drain current of 810mA/mm is obtained and the channel pinch-off is achieved at V_{DS}=10 and V_{GS}= -5V. As seen from Fig.5-3, there are some evidences of short-channel effects. The residual channel current is 0.9 mA/mm at V_{DS}=10 V and V_{GS}= -5 V. The research of short channel effect of AlGaN/GaN has been reported that when the aspect ratio of the gate length L_g to the AlGaN barrier-layer thickness d_{AlGaN}(L_g/d_{AlGaN}) is less than 5, the G_{mmax}, f_T, and threshold voltage (V_g) are degraded [5-7] [5-8]. From Fig.5-1, the ratio of L_g and d_{AlGaN} is approximately 4 which demonstrate that the source to drain leakage current resulted from the short channel effect. However, Fig.5-2

shows that the residual channel current is still less than 1mA/mm which is the definition of the gate-drain breakdown voltage at V_{DS}=10 V. From Fig.5-4, the gate leakage current density is 0.4 mA/mm at V_{DS}=10 and V_{GS}=0 V. There are many researches in the gate leakage current mechanisms in AlGaN/GaN heterostructure field-effect transistors. It demonstrates that the gate leakage current comes from the vertical tunneling and the lateral tunneling. However, vertical tunneling is the dominant mechanism in the AlGaN/GaN HEMTs without cap layer and both vertical and lateral tunneling are important in the AlGaN/GaN with cap layer[5-9,5-12]. In addition, the gate leakage can be reduced by the recessed gate which is under the extremely low recess etching rate [5-12]. Fig.5-5 shows the maximum extrinsic transconductance of 265 mS/mm is achieved at V_{GS}= -2.8 V and V_{DS}= 5V. Fig.5-6 shows the cutoff frequency of the 80nm AlGaN/GaN HEMT is 36GHz.The reason that Si substrate cutoff frequency is not quite high is possibly caused by the leakage current from the Si substrate [5-13].



5-4 Conclusions

An 80-nm-length T-gate AlGaN/GaN HEMTs grown on Silicon substrate were fabricated; simultaneously, the DC and RF devices characteristics were clearly discussed. The maximum I_{DS} of 810mA/mm and peak extrinsic Gm of 265 were obtained, while a cutoff frequency is 36 GHz when the V_{DS} is 5V. These DC and RF characteristics demonstrate the potential of AlGaN/GaN HFETs on silicon substrate for high-frequency applications. Moreover, the outstanding results also show the AlGaN/GaN HEMTs grown on silicon to reduce material cost and to be compatible with Si technology is promising in the future.



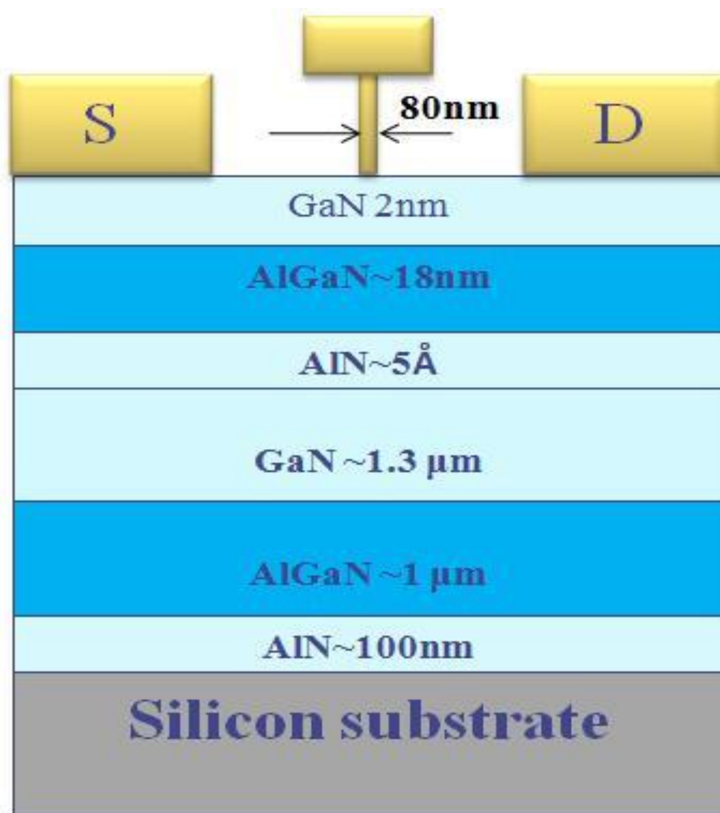


Fig.5-1 Cross section of the 80nm AlGaN/GaN HEMT

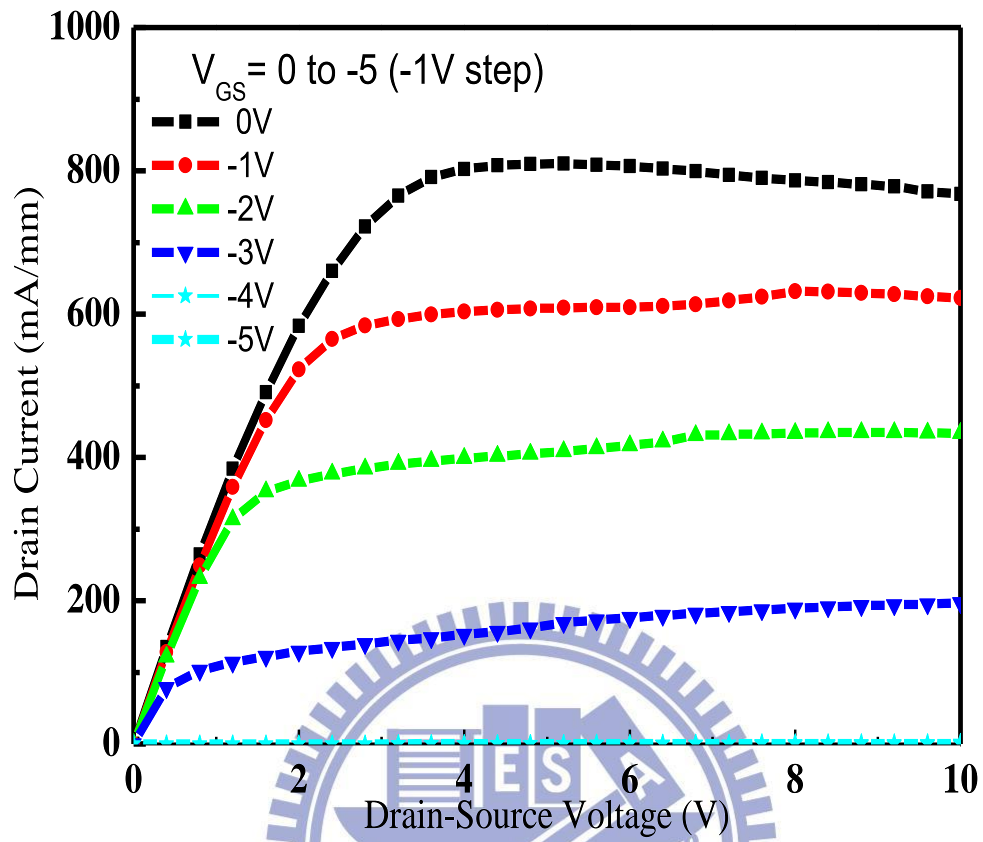


Fig.5-2 Drain-source current versus drain-source voltage curves of 80nm AlGaN/GaN HEMT with Si_3N_4 passivation.

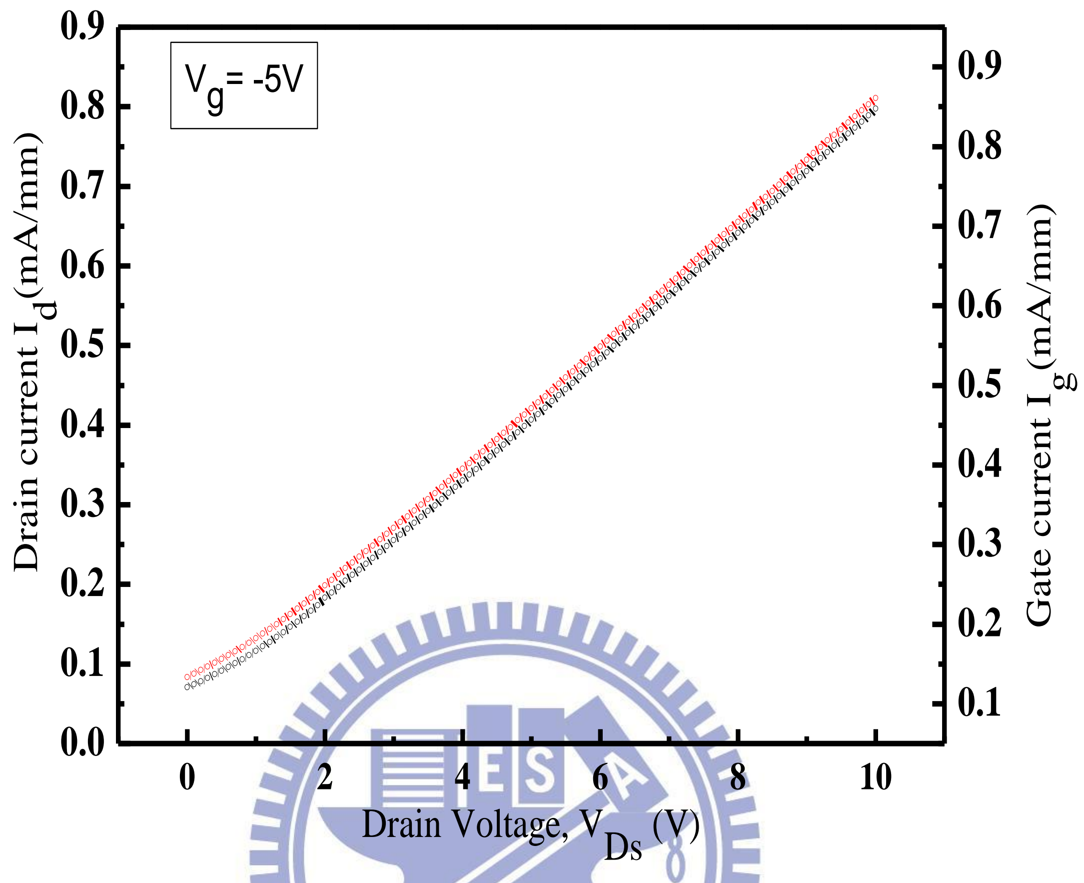


Fig.5-3 Drain leakage current in the off-state

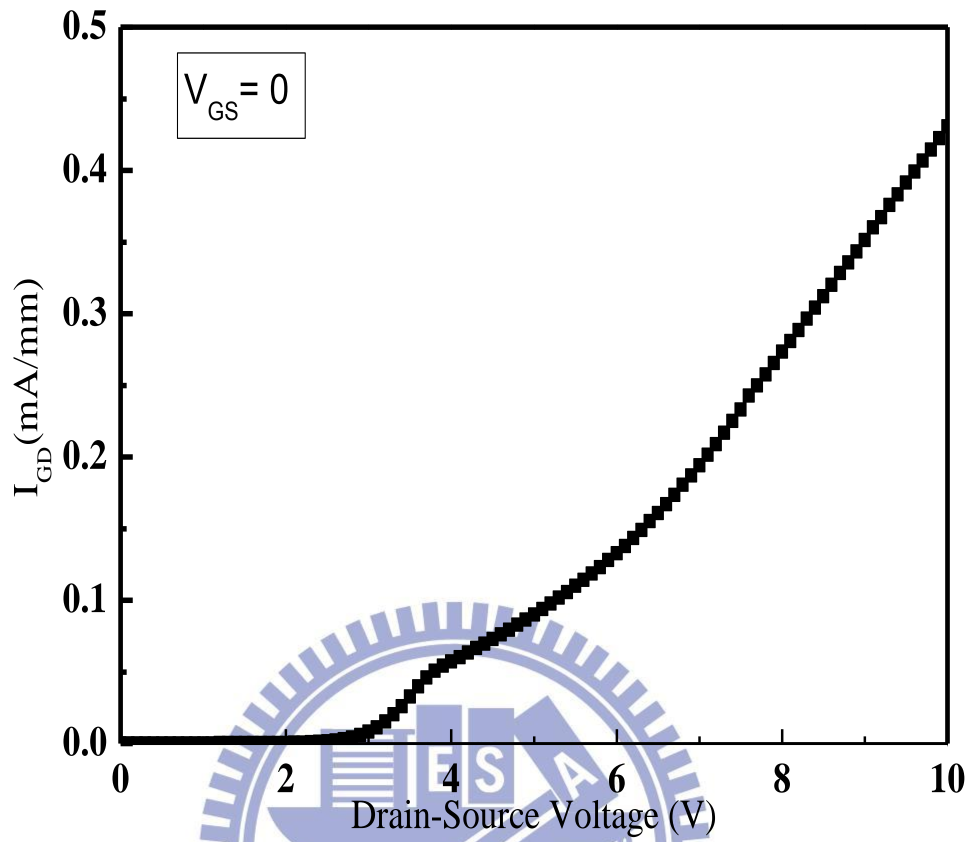


Fig.5-4 Gate leakage current density during the device operation

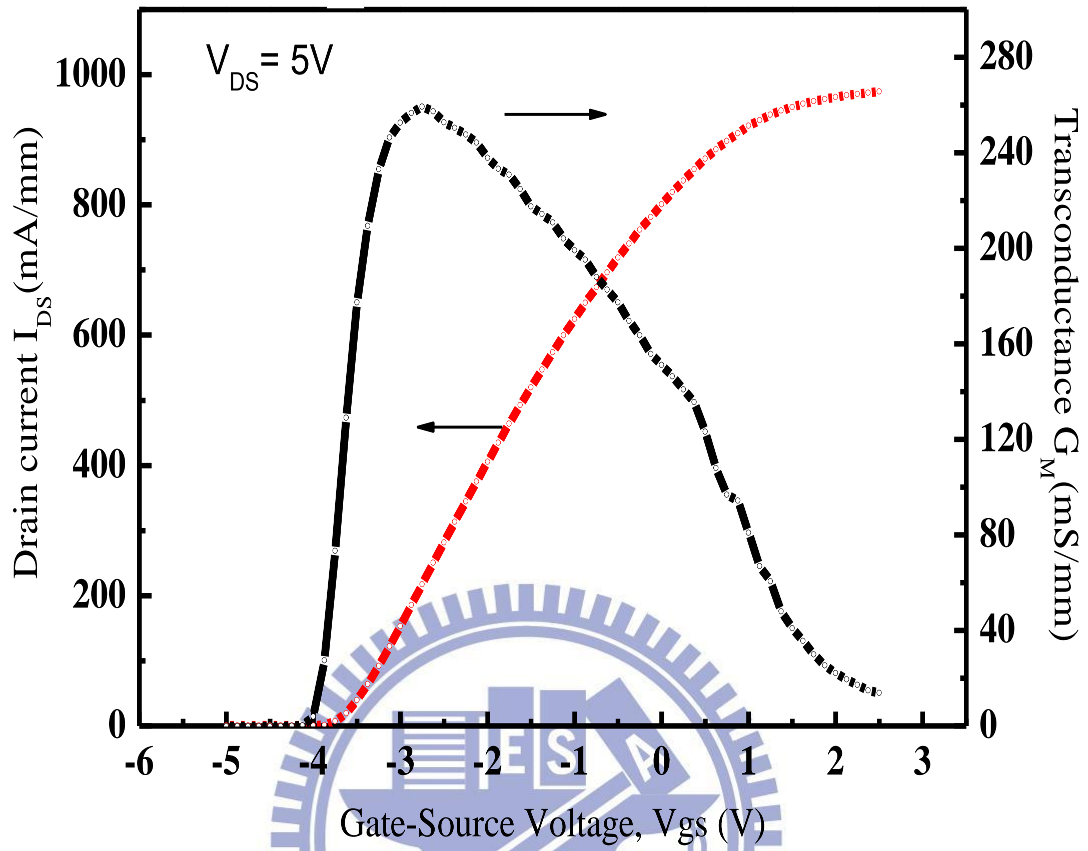


Fig.5-5 Transconductance versus gate-source voltage of 80 nm AlGaN/GaN HEMT with Si_3N_4 passivation

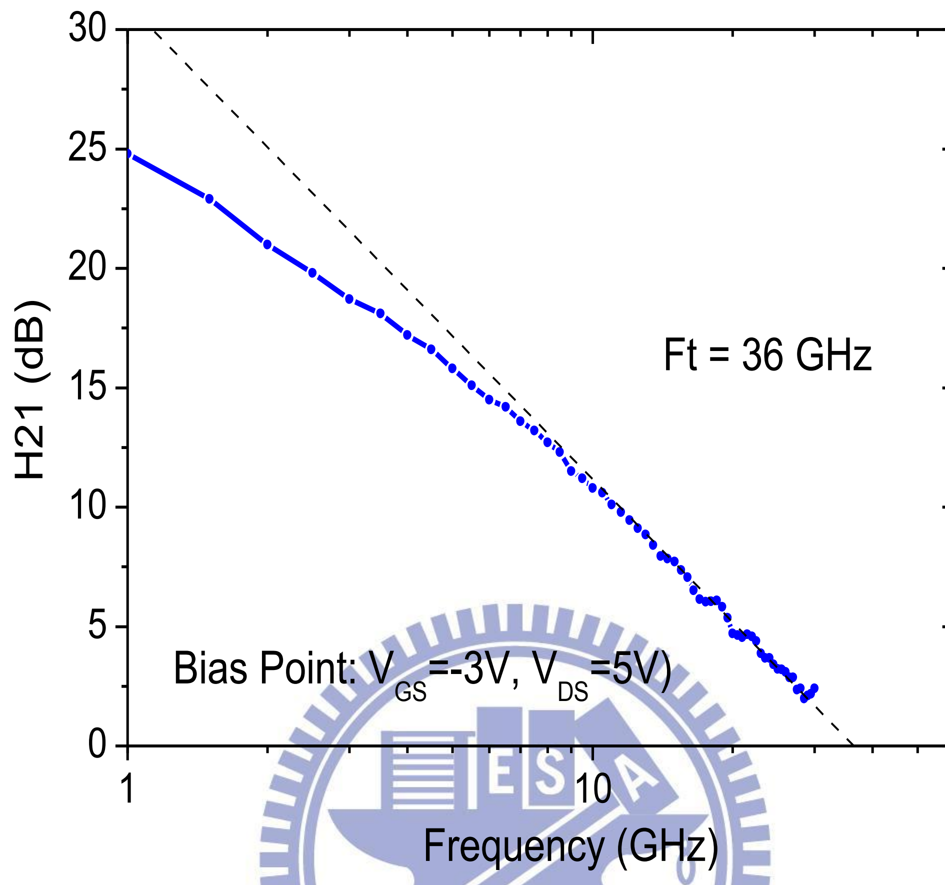


Fig.5-6 Cutoff frequency of the 80nm AlGaN/GaN HEMT

Chapter 6

Study of Device Linearity Improvement for the 80-nm AlGaN/GaN HEMTs on Silicon Substrate by Using Multi-Gate Process

An 80-nm AlGaN/GaN high-electron-mobility transistor (HEMT) on silicon substrate with multi gates is investigated for device linearity improvement. The single, dual and triple gates devices were fabricated, and the DC characteristics, IM3 and IP3 of these devices were tested for obtaining the relationship between device linearity and gate fingers, and found that the AlGaN/GaN HEMTs with multi-gates will improve the flatness of the Gm distribution under different gate bias conditions and thus achieve lower IM3 and higher IP3 with small scarification in the peak Gm value. Overall, the triple gates with gate length of 80-nm AlGaN/GaN HEMTs on Silicon Substrate demonstrated best linearity performance among these three different types of devices studied with highest IP3 level, lowest IM3.

6-1 Introduction

Recently, with the rapid development of wireless communication system, the video telephony, high quality audio and video transfer could be realized in our life. However, because of the huge amount of users, the available frequency spectrum is heavily crowed. In order to reduce the cost in the expensive frequency spectrum, the maximum data transfer rate in the minimum bandwidth is necessary. Therefore, we need to use the complex modulation techniques to get the maximum data transfer rate. But, the modulation techniques, such as Quqdrature Phase Shift Keying (QPSK), lead to the dynamic signal and signal distortion. Therefore, the linearity of the RF power amplifier is one of the most important parameter in the modern wireless communication system.

In the advanced wireless communication system, multichannel transmissions are extensively used to transmit signals. As transiting signals, there are many operating frequencies with the neighboring frequencies located closely to each other, so it is important to consider that the device used in the communication system could not induce signal distortions. However, among all intermodulation distortions, third-order intermodulation distortion (IM3) can't be filtered out by the filter; therefore, IM3 dominates the linearity performance of the device and is the most important linearity criteria for wireless communication system [6-1].

R

For linearity assessment, nonlinear transfer function based analysis method was used. Previously published results revealed that transconductance is required to remain constant over the operating range of gate bias for minimizing third-order distortion. Hence, improving the flatness of the extrinsic transconductance (Gm) profile will result in lower IM3 levels and higher third-order intercept point (IP3), and thus improve the device linearity [6-2]. Equation

(1) shows the relationship between Gm and drain-source current (I_{DS}). For remaining Gm constant with different gate-source voltage (V_{GS}), the I_{DS} as a function of V_{GS} should be straight and large.

$$Gm = \frac{dI_{DS}}{dV_{GS}} \qquad (1)$$

Generally, high-power GaN HEMTs are fabricated on sapphire and SiC because of the potential for high-power high-frequency applications and confirmed the high current drivability [6-3]. However, GaN HEMTs grown on silicon substrate can reduce material expenses and to be compatible with Si technology which is more possible to be commercialized [6-3, 6-7]. Therefore, we present the linearity characteristics of the multi-gates AlGaN/GaN HEMTs on Si substrates, and compare it with the regular AlGaN/GaN HEMTs devices for device linearity improvement in this study.

6-2 Device Fabrication

The AlGaN/GaN HEMTs structure was grown on Si substrate using molecular beam epitaxy (MBE) technology. Electron mobility of 1600 $cm^2V^{-1}s^{-1}$ and sheet carrier density of 1×10^{13} cm^{-2} were measured by hall measurement for. The device processing started with ohmic contact formation. Ohmic metal Ti/Al/Ni/Au was evaporated by e-gun system, and then annealed at 800℃ for 1min in N_2. After that, active region of the device was definite by the mesa isolation process, and dry etch process was controlled by inductive couple plasma (ICP) with Cl_2 in Ar ambient. Then, electron beam (EB) lithography with tri-layer photoresists was applied for the fabrication of T-shaped gate. The 80nm Ti/Pt/Au T-gate were centered in the 5μm source/drain space. Single, dual and triple gate devices are fabrication as shown in Fig.6-1. The 100 nm thick Si_3N_4 passivation film was deposited by plasma-enhanced chemical vapour deposition (PECVD) at 300℃. Finally, the nitride via was opened by CF_4

RIE etching.

6-3 Results and Discussion

Ohmic contact with contact resistance of 2.8×10^{-6} (Ohm-cm^2) was evaluated by transmission line method (TLM). Figure.6-2 shows the current-voltage (I-V) characteristics of the 80nm gate length AlGaN/GaN HEMT with single, dual and triple gates. The single gate device has a maximum drain current of 854 mA/mm at V_{GS} = 0, while the dual gate and triple gate devices have 816 and 781 mA/mm drain currents, respectively. The reason that multi gate has lower I_{DS} is the total gate length of the multi gate is larger than the single gate. The study of the relationship between the gate length and drain current has been reported. As the area of schottky contact metal is increased, the 2DEG carrier concentration is decreased [6-8]. The reason is some 2DEG electrons under the schottky contact metal are extracted to the void surface donor state as the schottky contact metal is deposited on strained AlGaN/GaN heterostructure. Due to the larger total gate length of multi gate, the area of schottky contact metal of multi gate is more than the single gate. The electrons under the multi-gate domain are be extracted to the surface states, so it represents that the 2DEG carrier concentration of multi gate is less than the single gate; thus, the multi gate has the lower drain current.

Figure.6-3 shows the I_{DS} versus V_{GS} curve for the three different types of devices. From a comparison of these devices, it can be seen that the single gate device has the higher pinch off voltage of -4.2V and the multi gate devices have the lower pinch off voltage of -3.9 V and -3.7 V .However, the maximum current of the three different type of devices reach the almost the same value at V_{GS} = 4 V with V_{DS} = 5 V. The results indicated that the multi gate significantly decreased the pinch of voltage but did not influence the maximum drain current. The finding of the decreased pinch-off voltage is in agreement with other literatures which had reported that the lower pinch-off voltage with the larger gate length [6-9, 6-10]. In

addition, in the submicrometer gate length, the distribution of electric field under the gate domain causes more electrons travel ballistically [6-11]; therefore, the velocity overshoots effect become very important. In Fig.6-3, the devices were operated at V_D=5V and V_{GS}=-5V to 3.5V. It can be observed that the slope of the I_D curve of single gate device is higher than multi-gate devices at V_{GS}= -5V to -4V. This is due to the electron overshoot effect dominated the device performance at submicrometer gate length. Because of the high electric field at the edge of gate, the high velocity electrons reduce the transit time and lead to higher drain current and transconductance [6-11, 6-12]. It caused the single gate device has a sharper I_D curve at high drain to gate bias. However, when increasing the gate bias to the positive voltage, there is no velocity overshoot owing to the lower drain to gate bias [6-12]. It caused the degradation of the drain current and I_D curve of single gate device. In the multi-gate devices, the spacing of gate is 0.3μm and the gate length is 80 nm, as shown in Fig.6-1. The second or third gate could effectively reduce the electric field; further, it can suppress the electron overshoot effect. Thus, it can be seen in Fig.6-3 that the slope of I_D curve of multi gate is lower than single gate; however, when increasing the gate bias to the positive voltage, the drain current can increase with a stable rate in a large gate bias region. This is a result of the suppression of velocity overshoot effect by the multi gate. One may notice that the maximum current of the three different type of devices reached the almost same value at V_{GS} = 4V. According to the study of electric distribution in GaN/AlGaN, the high electron field was located at the domain near the drain side at a positive gate bias [6-13]. This result predicts that electrons use the same velocity transverse the gate domain of the different three type devices. It means that the multi gate devices could achieve the same maximum drain current as same as single gate device.

The characteristic of the transconductance dependence on the gate-bias are shown in Fig.6-4. Compared to multi-gate devices, single gate device acquired the maximum transconductance at V_{GS}= -3V and V_D=5 V. There is a good agreement with the I_D versus V_{GS}

curve. The high transconductance attributed to the high electron velocity and the strong electric field. On the other hand, the multi gate device obtained a lower maximum Gm value, but a flatter Gm distribution as compared to that of single gate. It represented that the drain current increased in a stable rate in a large variety of gate bias region, since the multi gates suppressed the electron velocity overshoot effect. As mentioned before, a lower IM3 level can be achieved by increasing the flatness of the Gm distribution across the gate-bias region which indicated that multi gate have the potential to lead to an excellent linearity performance.

To further investigate the linearity performance of the three devices, polynomial curve fitting technique was applied to the transfer characteristic functions of these devices as equation (1).

$$G_m(V_{GS}) = \frac{\partial I_{DS}(V_{GS})}{\partial V_{GS}} = a_1 + 2a_2V_{GS} + 3a_3V_{GS}^2 + 4a_4V_{GS}^3 + 5a_5V_{GS}^4 + \ldots\ldots(2)$$

Hence, the relationship between IM3, IP3 and Gm, Gds are shown in equation (3) and (4) [1, 14, and 15].

$$IM3 \propto \frac{\left(G_m''\right)^2}{\mathrm{G}_{\mathrm{ds}}^2 \cdot R_L} \cdot A^6 \qquad (3)$$

$$IP3 \propto \frac{\left(G_m\right)^3}{G_m'' \cdot G_{ds}^2 \cdot R_L} \qquad (4)$$

In order to improve the device linearity, I_{DS} should increase linearly with V_{GS}. Therefore, a_1 should be larger and the higher order constants, while a_3 and a_5 should be minimized [6-1, 6-14]. Table 6-1 shows the coefficients of these multi-gate devices and the comparison of the dc characteristics of these three device extracted from the I_D versus V_{GS} curve with V_{DS} =5 V. It shows that the triple gate device has highest a1 of 0.00868 ,while

single device has lowest a_1 of 0.00704. In addition, the lowest a_3 is 2.32×10^{-5} from the triple gate device and the lowest a_5 is 1.4×10^{-5} from the dual gate device. From the data analysis, the devices linearity improvement can be achieved by using multi gates approach.

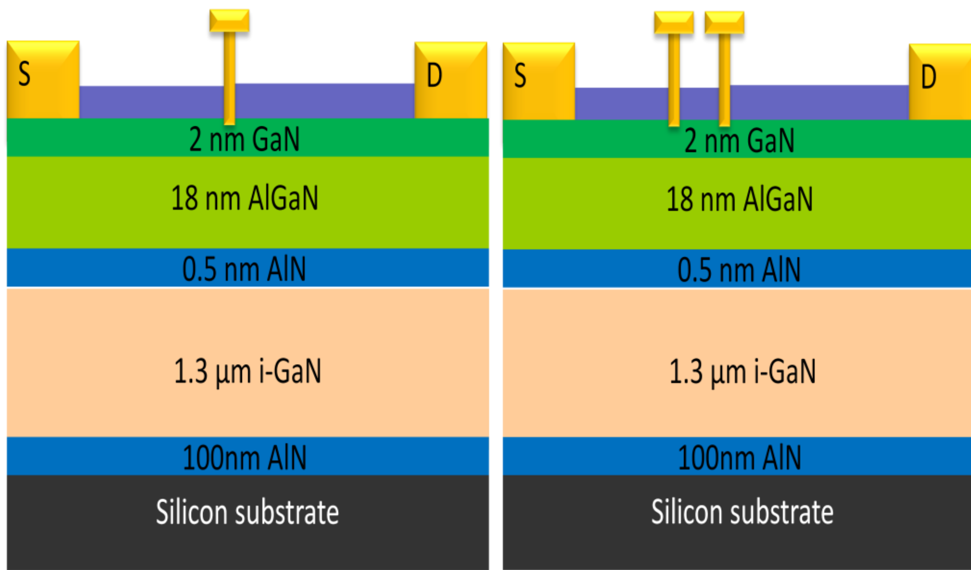
To evaluate the device linearity, the measurement of IM3 and IP3 of these devices were necessary. The IM3 and IP3 measurements were carried out by injecting two signals with the same amplitude but at two different frequencies: 2.0 GHz and 2.001GHz with the devices biased at V_{DS} = 5V, and adjust the I_{DS} to get the IP3 vs. I_{DS} curve. Furthermore, the load impedance was firstly tuned for maximum gain in input side and maximum power in output side for each individual device. The measurement result of the IP3 versus. I_{DS} curves for these three different 80nm × 100μm devices are shown in Fig.6-5. It shows that multi gates devices possess higher IP3 value, especially tripe gates, and wider high IP3 region versus different I_{DS}. IP3 is proportional to the Gm^3 and the reciprocal of the G_m'', and the maximum IP3 derived from the equation (4) can be obtained at $G_m'' = 0$. To further investigate the maximum IP3, the Gm^3 versus gate-source voltage and the I_{DS} at $G_m'' = 0$ were calculated as shown in Fig.6-6. The result indicated that two maximum IP3 points will appear on the both sides of the maximum transconductance, and it can be extracted the I_{DS} value of this two points. The single, dual and triple gate device possess two maximum IP3 points at 0.54% I_{dSS} and 53.8% I_{dSS}, 0.72% I_{dSS} and 66% I_{dSS}, and 2.09% I_{dSS} and 71.1% I_{dSS}. It clarified the degradation of device linearity at high I_{dss} condition. Owing to the smallest available operating bias, the IP3 value of single gate device drops significantly at the high Idss region. Compared to the single gate, multi gate device possess relatively large available operating bias that demonstrated the degradation of multi gate in high I_{dss} region is less than single gate. The measured maximum IP3 of these devices are listed in Table 6-2 and the tuning at Γ_{source} and Γ_{load} of single gate, dual gates and triple gates devices are Γ_{source} = 199.26∠71.13°, 124.2∠77.52° and 201.69∠71.07°, and Γ_{load} = 181.87∠62.58°, 260.07∠43.20° and 179.68∠58.97°,

respectively. The triple gates device shows highest IP3 of 30.54 dBm, higher Δ(IP3-P1dB) of 17.68 dB, and higher IP3 to DC power consumption ratio (IP3/PDC) of 16.71. Overall, the triple gates device has highest value of figure of merit for device linearity. From the data in Fig.6-5 to Fig.6-7, it can be concluded that multi gates either dual gate or triple gates can achieves flatter Gm distribution versus V_{GS} bias and thus lower overall IM3 and higher IP3 of these devices even though the single gate device exhibits higher peak Gm.

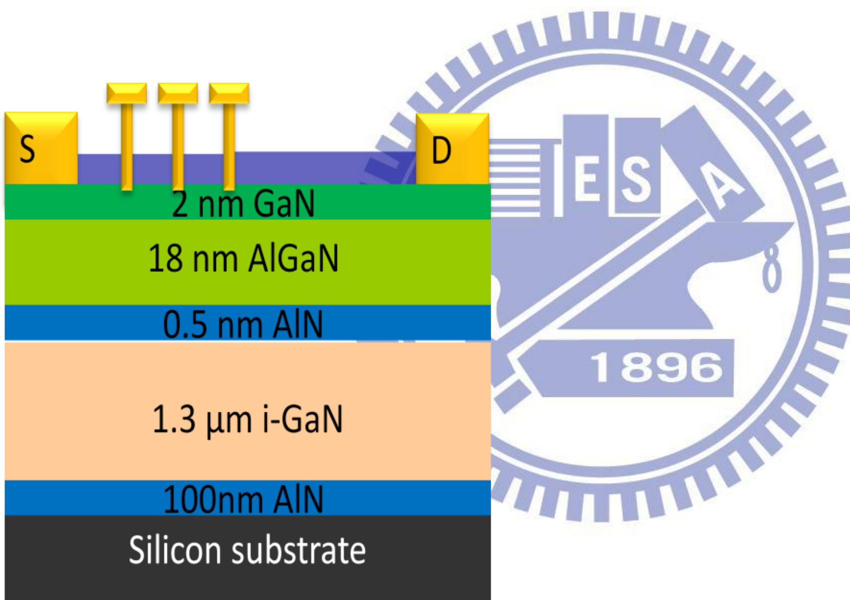
6-4 Conclusions

The linearity characteristics of the multi-gate AlGaN/GaN HEMTs on Si substrates is investigated in this study. Although the single gate device has the maximum Gm of 265 mS/mm at V_{DS}= 5V, the flatter Gm distribution was achieved for the triple gates device. To further investigate the linearity performance of the three devices, polynomial curve fitting technique was applied to the transfer characteristic functions. It shows that the multi gate device has highest a_1 and single gates device has lowest a_1. In addition, the multi gates device has the lowest a3 and a5, especially triple gates device. Therefore, the devices linearity improvement can be achieved using multi gates approach.

The AlGaN/GaN HEMTs on Si substrates with multi gates process to improve the device linearity is demonstrated. The gate increased in a device results in the improvement of the Gm vs. V_{GS} curve flatness and thus leads to lower overall IM3 and higher IP3 for these devices, even though the single device exhibits higher peak Gm. With the three different gate fingers devices studied, it demonstrated the multi gates did not influence the maximum drain current, but the triple gates device has flattest G_m versus V_{GS} curve. These DC characteristics lead to higher IP3 levels and lower IM3 for the triple gates device as compared to the other devices studied. The experimental result in this work shows that multi gates can be practically used for the development of high linearity devices for wireless communication applications.

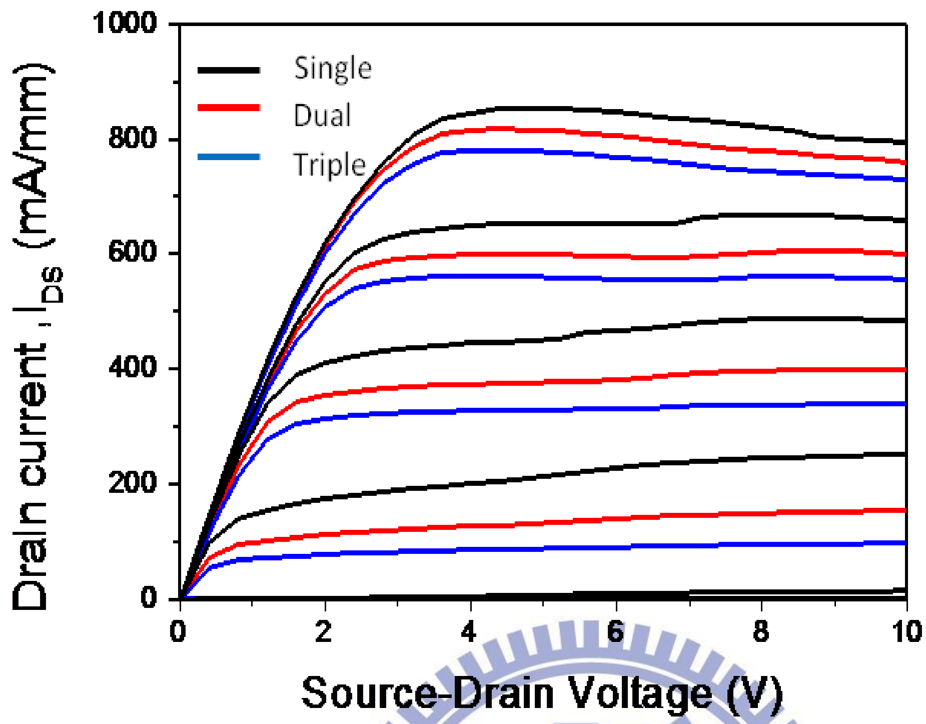


(a) (b)



(c)

Fig.6-1 Cross section of the 80nm AlGaN/GaN HEMT (a) single gate (b) dual gate (c) triple gate



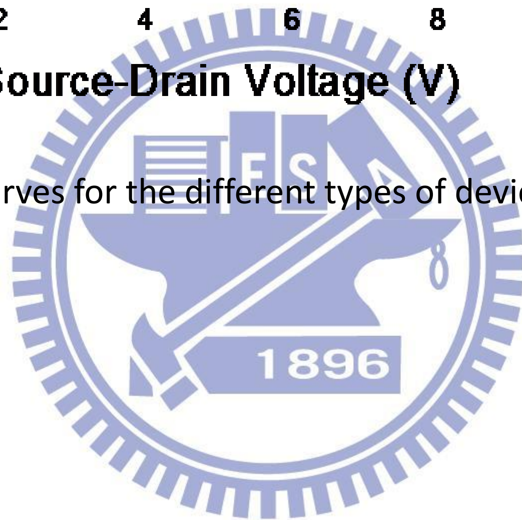
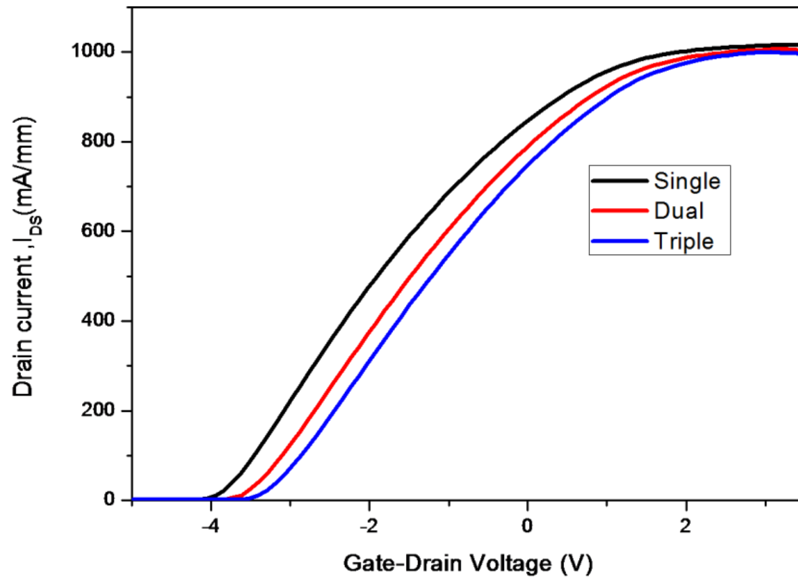


Fig.6-2 I_D versus V_{DS} curves for the different types of devices at V_{GS}= 0 to -5V



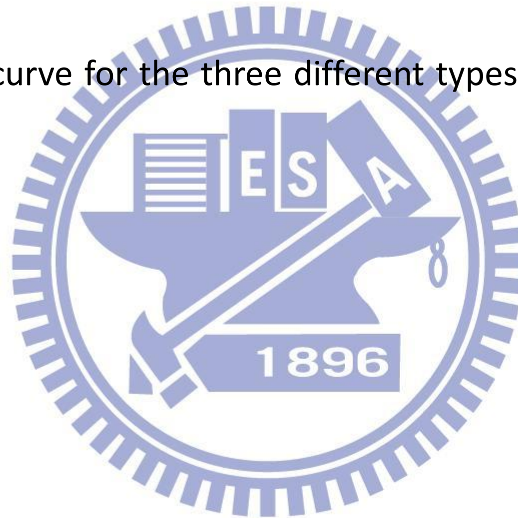


Fig.6-3 I_{DS} versus V_{GS} curve for the three different types of devices and the V_{DS} bias is 5 V

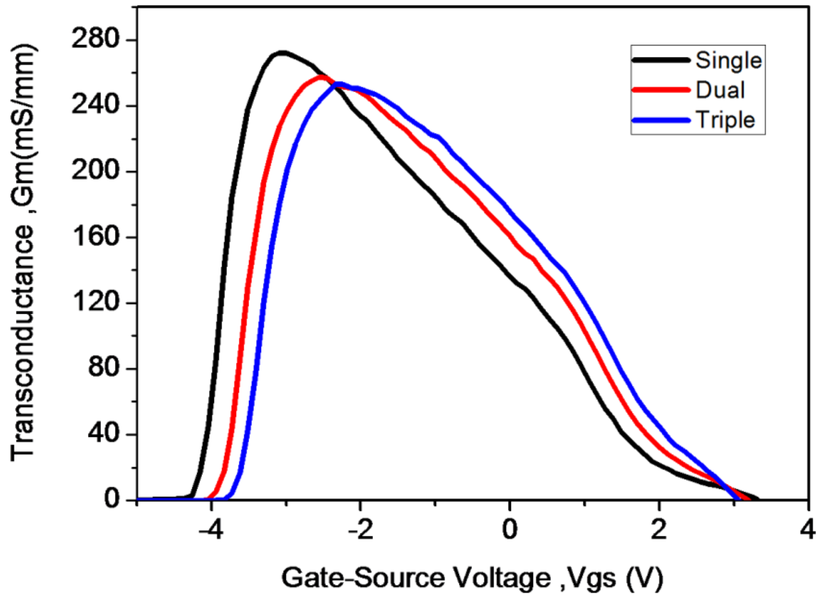
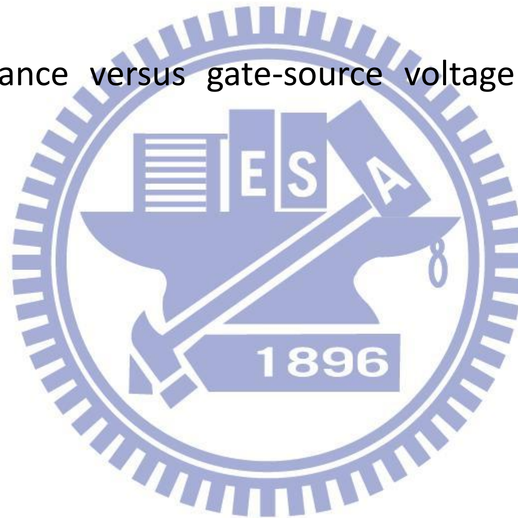


Fig.6-.4 Transconductance versus gate-source voltage of different types of devices



Device type	**Single gate**	**Dual gate**	**Triple gate**
I_{DSmax} (mA/mm)	1015.4	1005.72	999.8
G_{mmax} (mS/mm)	272.5	251.86	253.08
I_{DS}-V_{GS} polynomial 1st order coefficient a1	0.00704	0.00809	0.00868
I_{DS}-V_{GS} polynomial 2nd order coefficient a_2	-0.00134	-0.00103	-8.80E-04
I_{DS}-V_{GS} polynomial 3rd order coefficient a_3	-2.9613×10^{-5}	-1.5917×10^{-4}	-2.3232×10^{-5}
I_{DS}-V_{GS} polynomial 4rd order coefficient a_4	2.93×10^{-7}	-1.41×10^{-4}	-1.93×10^{-4}
I_{DS}-V_{GS} polynomial 5rd order coefficient a_5	5.6394×10^{-5}	-1.3995×10^{-5}	-2.2566×10^{-5}
I_{DS}-V_{GS} polynomial 6rd order coefficient a_6	-2.13×10^{-7}	1.86×10^{-5}	2.66×10^{-5}
a_3/a_1	0.0420	0.0197	0.0087
a_5/a^1	8.01×10^{-3}	1.72×10^{-3}	2.50×10^{-3}

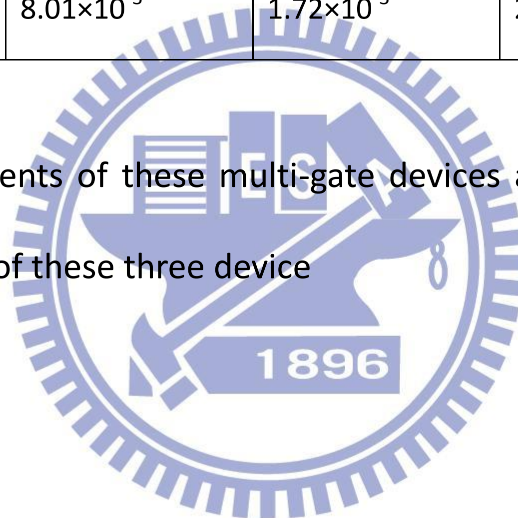
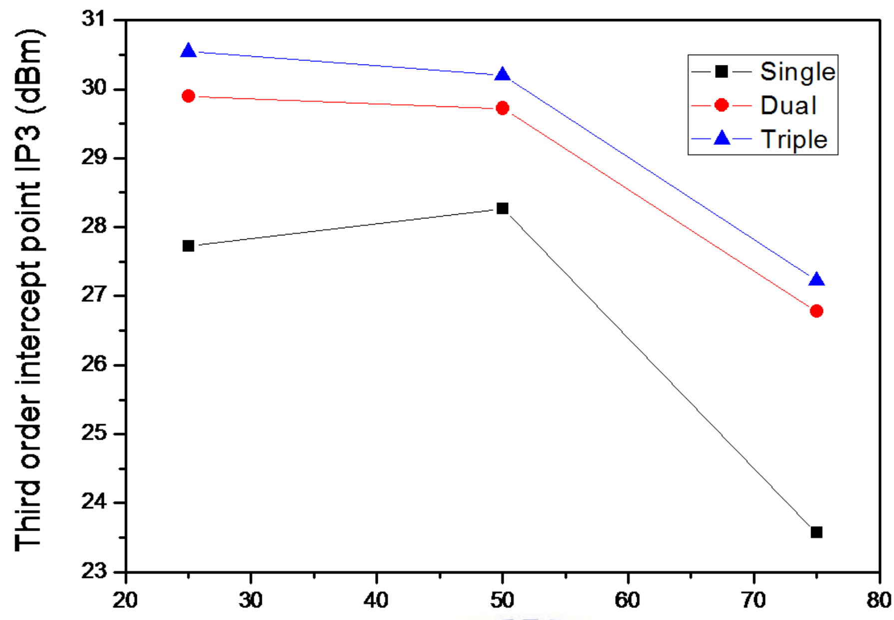


Table 6-1 The coefficients of these multi-gate devices and the comparison of the dc characteristics of these three device



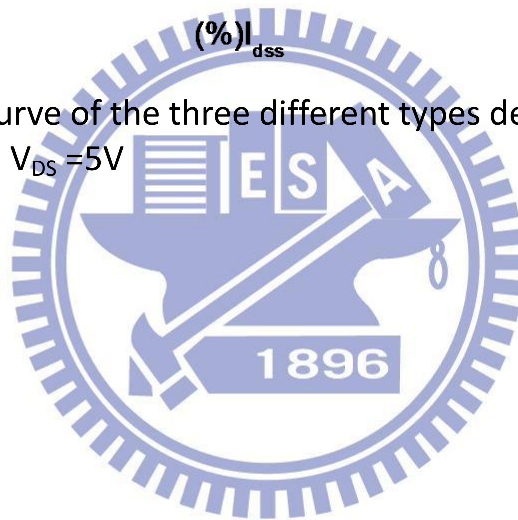
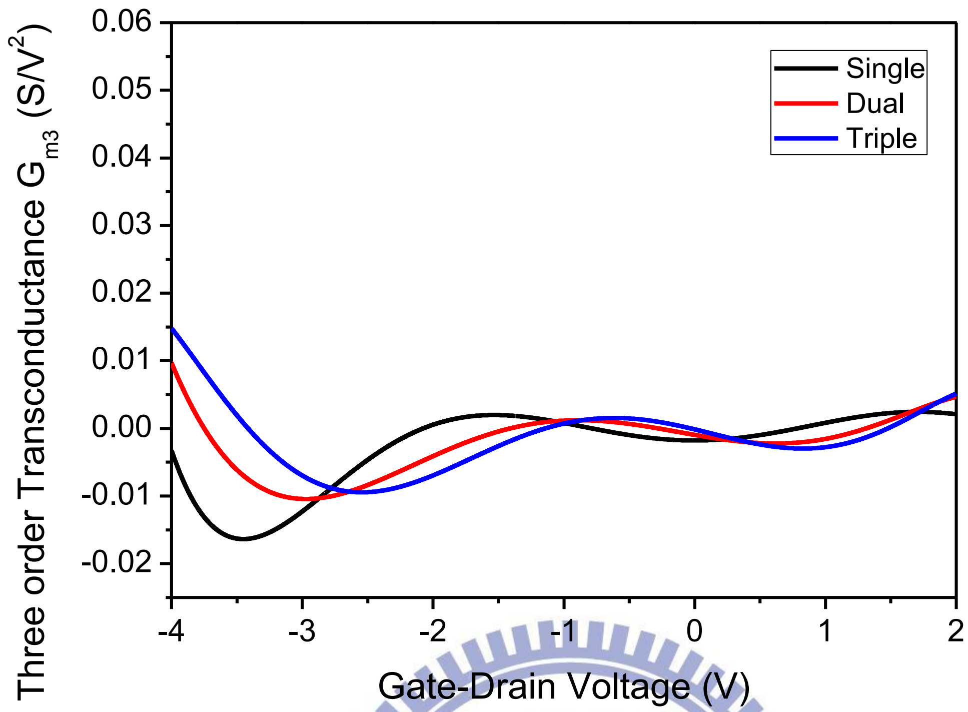


Fig.6-5 IP3 versus I_{DS} curve of the three different types devices, and the test frequency is 2GHz and V_{DS} =5V



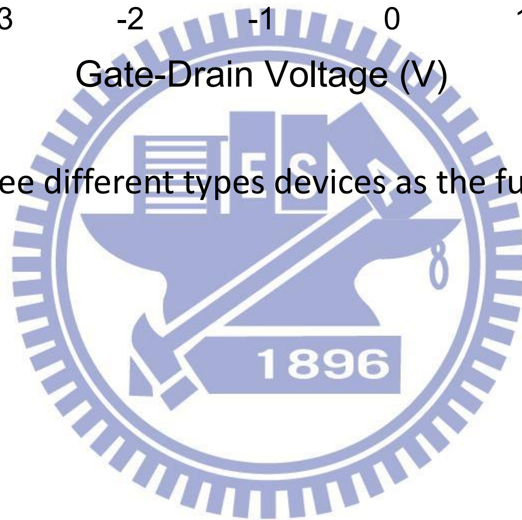


Fig.6-6 Gm3 of the three different types devices as the function of gate-source voltage

Device Type	DC bias point VDS = 5V				
	I_{DS} bias point	Operation frequency : 2 GHz			
		P1dB(dBm)	IP3(dBm)	IP3-P1dB (dBm)	IP3/PDC
Single gate	25% Ids	9.75	27.72821	13.58	3.21
	50% Ids	12.19	28.27246	16.08	7.42
	75% Ids	6.52	23.57	17.05	0.79
Dual gate	25% Ids	12.73	29.89436	17.17	5.86
	50% Ids	13.68	29.7221	16.04	11.13
	75% Ids	10.35	26.77599	16.42	1.89
Triple gate	25% Ids	13.63	30.5401	16.91	8.38
	50% Ids	12.51	30.19896	17.68	16.71
	75% Ids	11.5	27.22508	15.72	2.81

Table 6-2 Comparison of the IP3 of the three different types of device

Chapter 7

Conclusion

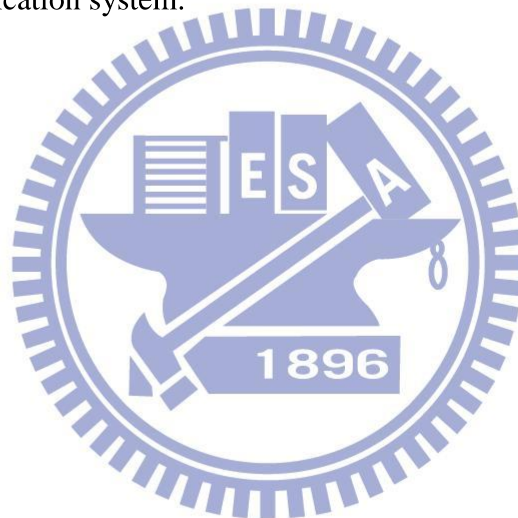
In this thesis, an 80-nm-length T-gate AlGaN/GaN HEMTs grown on Silicon substrate were successfully fabricated; simultaneously, the DC and RF characteristics were clearly discussed. The maximum I_{DS} of 810mA/mm and peak extrinsic G_m of 265 were obtained. However, the short channel effect led to the high leakage current. After the discussion, this phenomenon could be improved by using the gate recess technique to suppress the short channel effect and gate leakage current. In addition, the current-gain cut-off frequency is 36 GHz at the V_{DS} = 5V. These DC and RF characteristics showed the potential of AlGaN/GaN HEMTs on silicon substrate for RF power amplifier. Moreover, the outstanding results also indicated that the AlGaN/GaN HEMTs grown on silicon to reduce material cost and to be compatible with Si technology is promising in the future.

Although the 80nm single gate devices showed the excellent electrical characteristic, the velocity overshoot phenomena may occur and degrade the linearity performance. In this thesis, the single, dual and triple gate devices were fabricated and investigated. The innovative multi-gate technique successfully improved the linearity characteristics of the AlGaN/GaN HEMTs on Si substrate. It could be found that multi-gate effectively reduced the high electric field. It made the electron possessed a stable electron velocity under the gate domain and further to suppress the velocity overshoot effect. The multi-gate devices could stably increase the drain current and maintain the transconductance value under a larger gate bias region; the gate increased in a device results in the improvement of the Gm vs. V_{GS} curve flatness and thus leads to lower overall IM3 and higher IP3 for multi-gate devices, even though the single device exhibits higher peak Gm. Furthermore, multi-gate devices possessed the electrical characteristic as same as the nanometer gate length device. After the measurement, the

maximum third order intermodulation point (IP3) of 30.54 dBm could be achieved in the triple-gate devices. It shown that multi gate could effectively improve the linearity of devices.

In addition, the third order intermodulation points of the multi-gate and single gate device under the different gate bias are also compared in this study. By polynomial curve fitting technique, It could successfully demonstrate that the multi-gate device have the higher IP3 in the larger I_{DSS} % region. Therefore, it indicated that multi gate technique could effectively improve the linearity performance.

In conclusion, these experimental results demonstrated that, in the future, the multi-gate AlGaN/GaN HEMTs have the great potential to be the RF power amplifier applied in the modern wireless communication system.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Reference

Chapter 1

[1-1] Umesh K. Mishra, Linkun Shen, Thomas E. Kazior, and Yi-Feng Wu,"GaN-Based RF Power Devices and Amplifiers," Proceedings of the IEEE 96, 2(2008).

[1-2] Jean-Claude Gerbedoen, Ali Soltani, Sylvain Joblot, Jean-Cluade De jaeger, Christophe Gaquiere, Yvon Cordier, and Fabrice Semond,"AlGaN/GaN HEMT on (001) Silicon Substrate With Powe Density Performance of 2.9 W/mm at 10GHz," IEEE Trans. Electron Device 57, 7 (2010).

[1-3] L.Wang, W.D.Hu, X.S. Chen, and W. Lu," The Role of Ultrathin AlN in the Reduction in the Hot Electron and Self-Heating Effects for GaN-Base Double Heterojunction High Electron Mobility Transistors," Journal of Applied Physics 108,054501(2010)

[1-4] Haifeng Sun, Andreas R. Alt, Hansruedi Benedickter, C. R. Bolognesi, Eric Feltin, Jean-Francois Carlin, Marcus Gonschorek, Nicolas Grandjean,"Ultrahigh-Speed AllnN/GaN high Electron Mobility TransistorsGrown on (111) High-Resistivity Silicon with FT=143," Applied Physics Express 3, 094101 (2010).

[1-5] T.Palacio, A. Chakrabotry, S. Rajan, C. Poblenz, S. Keller, S.P. DEnBaars, J.S. Speck, and U.K. Mishra,"High-Power AlGaN/GaN HEMTs for Ka-Band Application," IEEE Electron Device Letters 26, 11(2005).

[1-6] Yueh-Chin Lin, Edward Yi Chang, Hiroshi Yamaguchi, Wei-Cheng Wu, and Chun-Yen Chang, "A δ-Doped InGaP/InGaAs pHEMT With Different Doping Profiles for Device-Linearity Improvement," IEEE Transaction on Electron Devices, vol. 54, no. 7, July 2007.

Chapter 2

[2-1] U.K. Mishra, P. Parikh, Y.F. Wu, "AlGaN/GaN HEMTs: An overview of device operation and applications," Processdings of The IEEE, Vol. 90,No.6, June 2002.

[2-2]Chien-chi Lee,"GaN-Based Heterostructure Field Effect Transistors " June 2006

[2-3] O. Ambacher,a) J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy,W. J. Schaff, and L. F. Eastman," Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," Journal of Applied Physics Volume 85, Number 6 ,15 March, 1999

[2-4] J. A. Garrido, J. L. Sa´nchez-Rojas, A. Jime´nez, and E. Mun˜oz, F. Omnes and P. Gibart," Polarization fields determination in AlGaN/GaN heterostructure field-effect transistors from charge control analysis," Applied Physics Letters Volume 75, Number 16, 18 October 1999.

[2-5]Vorgelegt von,M.Sc. Eng.,Ibrahim Khalil,and Barisal, Bangladesch," Intermodulation Distortion in GaN HEMT,"17.07.2009

[2-6] Toshihiro Ohki, Toshihide Kikkawa, Yusuke Inoue, Masahito Kanamura, Naoya Okamoto,Kozo Makiyama, Kenji Imanishi, Hisao Shigematsu, Kazukiyo Joshin, and Naoki Hara," Reliability of GaN HEMTs:Current Status and Future Technology," IEEE 47th Annual International Reliability, Physics Symposium, Montreal, 2009

[2-7] Jean-Claude Gerbedoen, Ali Soltani, Sylvain Joblot, Jean-Cluade De jaeger, Christophe Gaquiere, Yvon Cordier, and Fabrice Semond,"AlGaN/GaN HEMT on (001) Silicon Substrate With Powe Density Performance of 2.9 W/mm at 10GHz," IEEE Trans. Electron Device 57, 7 (2010).

Chapter 3

[3-1]Vorgelegt von,M.Sc. Eng.,Ibrahim Khalil,and Barisal, Bangladesch," Intermodulation

Distortion in GaN HEMT,"17.07.2009

[3-2] Microwave Measurements Division • 490 Jarvis Drive • Morgan Hill, CA 95037-2809, "Intermodulation Distortion Measurements Using the 37300 Series Vector Network Analyzer Application Note/GIP-G"

Chapter 4

[4-1]Chien-Ying Wu,"Study of High and Low Voltage InAs-Channle Quantum Well Field Effrct Transistors for RF and Logic Applications," July 2009.

[4-2]Bruce M. Green, Student Member, IEEE, Kenneth K. Chu, E. Martin Chumbes, Student Member, IEEE, Joseph A. Smart, James R. Shealy, Member, IEEE, and Lester F. Eastman, Life Fellow, IEEE," The Effect of Surface Passivation on the Microwave Characteristics of Undoped AlGaN/GaN HEMT's," IEEE Electron Device Letters, Vol. 21, No. 6, June 2000

Chpater 5

[5-1] Umesh K. Mishra, Linkun Shen, Thomas E. Kazior, and Yi-Feng Wu,"GaN-Based RF Power Devices and Amplifiers," Proceedings of the IEEE 96, 2(2008).

[5-2] Jean-Claude Gerbedoen, Ali Soltani, Sylvain Joblot, Jean-Cluade De jaeger, Christophe Gaquiere, Yvon Cordier, and Fabrice Semond,"AlGaN/GaN HEMT on (001) Silicon Substrate With Powe Density Performance of 2.9 W/mm at 10GHz," IEEE Trans. Electron Device 57, 7 (2010).

[5-3] L.Wang, W.D.Hu, X.S. Chen, and W. Lu," The Role of Ultrathin AlN in the Reduction in the Hot Electron and Self-Heating Effects for GaN-Base Double Heterojunction High Electron Mobility Transistors," Journal of Applied Physics 108,054501(2010)

[5-4] Haifeng Sun, Andreas R. Alt, Hansruedi Benedickter, C. R. Bolognesi, Eric Feltin,

Jean-Francois Carlin, Marcus Gonschorek, Nicolas Grandjean,"Ultrahigh-Speed AllnN/GaN high Electron Mobility TransistorsGrown on (111) High-Resistivity Silicon with FT=143," Applied Physics Express 3, 094101 (2010).

[5-5] T.Palacio, A. Chakrabotry, S. Rajan, C. Poblenz, S. Keller, S.P. DEnBaars, J.S. Speck, and U.K. Mishra,"High-Power AlGaN/GaN HEMTs for Ka-Band Application," IEEE Electron Device Letters 26, 11(2005).

[5-6]Chien-Ying Wu,"Study of High Speed and Low Voltage InAs-channel Quantum Well Field Effect Transistors for RF and Logic Applications," (2009)

[5-7] Gregg H. Jessen, Robert C. Fitch, Jr., , James K. Gillespie, Glen Via, Antonio Crespo, Derrick Langley, Daniel J. Denninghoff, Manuel Trejo, Jr. , and Eric R. Heller," Short-Channel Effect Limitations on High-Frequency Operation of AlGaN/GaN HEMTs for T-Gate Devices," IEEE Trans. Electron Device

[5-8] Toshihide IDE_, Mitsuaki SHIMIZU, Akira NAKAJIMA, Masaki INADA, Shuichi YAGI, Guanxi PIAO,Yoshiki YANO1, Nakao AKUTSU1, Hajime OKUMURA, and Kazuo ARAI," Gate-Length Dependence of DC Characteristics in Submicron-Gate AlGaN/GaN High Electron Mobility Transistors," Japanese Journal of Applied Physics 46, 4B(2007).

[5-9] I. Adesida, "High performance recessed gate AlGaN–GaN HEMTs on sapphire," in Proc. TWHM, Jan. 2003, pp. 102–103.

[5-10] Y. Ando, Y. Okamoto, K. Hataya, T. Nakayama, H. Miyamoto, T. Inoue,and M. Kuzuhara, "12 W/mm recessed-gate AlGaN–GaN heterojunction field-plate FET," in IEDM Tech. Dig, 2003, pp. 563–566.

[5-11] E. J. Miller, X. Z. Dang and E. T. Yua," Gate leakage current mechanisms in AlGaN/GaN heterostructure field-effect transistors," Journal of Applied Physics 88, 10 (2000).

[5-12] Chia-Ta Chang, Heng-Tung Hsu, Edward Yi Chang, Chien-I Kuo, Jui-Chien Huang, Chung-Yu Lu, and Yasuyuki Miyamoto, "30-GHz Low-Noise Performanceof

100-nm-Gate-Recessed," IEEE Electron Device Letters 31, 2(2010).

[5-13] Masataka HIGASHIWAKI1, Takashi MIMURA1;2 and Toshiaki MATSUI1," 30-nm-Gate AlGaN/GaN Heterostructure Field-Effect Transistors with a Current-Gain Cutoff Frequency of 181 GHz," Japanese Journal of Applied Physics 45, 42(2006).

Chapter 6

[6-1] Yueh-Chin Lin, Edward Yi Chang, Hiroshi Yamaguchi, Wei-Cheng Wu, and Chun-Yen Chang, "A δ-Doped InGaP/InGaAs pHEMT With Different Doping Profiles for Device-Linearity Improvement," IEEE Transaction on Electron Devices, vol. 54, no. 7, July 2007.

[6-2] K. Y. Hur, K. T. Hetzler, R. A. McTaggart, D. W. Vye, P. J. Lemonias and W. E. Hoke, "Ultralinear double pulse doped AlInAs/GaInAs/InP HEMTs," Electronics Lett., vol. 32, no. 16, pp. 1516-1517, 1996.

[6-3] Jean-Claude Gerbedoen, Ali Soltani, Sylvain Joblot, Jean-Cluade De jaeger, Christophe Gaquiere, Yvon Cordier, and Fabrice Semond,"AlGaN/GaN HEMT on (001) Silicon Substrate With Powe Density Performance of 2.9 W/mm at 10GHz," IEEE Trans. Electron Device 57, 7 (2010).

[6-4] Umesh K. Mishra, Linkun Shen, Thomas E. Kazior, and Yi-Feng Wu,"GaN-Based RF Power Devices and Amplifiers," Proceedings of the IEEE 96, 2(2008).

[6-5] L.Wang, W.D.Hu, X.S. Chen, and W. Lu," The Role of Ultrathin AlN in the Reduction in the Hot Electron and Self-Heating Effects for GaN-Base Double Heterojunction High Electron Mobility Transistors," Journal of Applied Physics 108,054501(2010)

[6-6] Haifeng Sun, Andreas R. Alt, Hansruedi Benedickter, C. R. Bolognesi, Eric Feltin, Jean-Francois Carlin, Marcus Gonschorek, Nicolas Grandjean,"Ultrahigh-Speed AllnN/GaN high Electron Mobility TransistorsGrown on (111) High-Resistivity Silicon with F_T=143,"

Applied Physics Express 3, 094101 (2010).

[6-7] T.Palacio, A. Chakrabotry, S. Rajan, C. Poblenz, S. Keller, S.P. DEnBaars, J.S. Speck, and U.K. Mishra,"High-Power AlGaN/GaN HEMTs for Ka-Band Application," IEEE Electron Device Letters 26, 11(2005).

[6-8] Zhaojun Lin and Wu Lu, "Inflluence of Ni Schottky Contact Area on Two-Dimensional Electron-Gas Sheet Carrier Concentration of Strained AlGaN/GaN Heterostructures," Journal of Applied Physics 99, 014504 (2006).

[6-9] A. T. Ping, Q. Chen, J. W. Yang, M. Asif Khan, and I. Adesida ," DC and Microwave Performance of High-Current AlGaN/GaN Heterostructure Field Effect Transistors Grown on p-Type SiC Substrates," IEEE Electron Device Letters, VOL. 19, NO. 2, FEBRUARY 1998.

[6-10] Toshihide IDE, Mitsuaki Shimizy, Akira Nakajima, Masaki Inada, Shuichi YAGI, Guanxi Piao, Yoshiki Yano1, Nakao Akutsu1, Hajime Okumura, and Kazuo ARAI, "Gate-Length Dependence of DC Characteristics in Submicron-Gate
AlGaN/GaN High Electron Mobility Transistors," Japanese Journal of Applied Physics
Vol. 46, No. 4B, 2007, pp. 2334–2337.

[6-11] Yuji Awano, Makoyo Kosugi, Kinjiro Kosemura, Takashi Mimura, and Masayuki ABE , "Short-Channel Effects in Subquarter-Micrometer-Gate HEMT's: Simulation and Experiment," IEEE Transaction on Electron Devices, VOL. 36, NO. 10, OCTOBER 1989.

[6-12]Madahusudan Singh, Yuh-Renn Wu, and Jasprit Singh,"Velocity Overshoot Effects and Scaling Issues in III-V Nitrides," IEEE Transaction on Electron Devices, vol. 52, no. 3, March 2005.

[6-13] Toshihiro Ohki, Toshihide Kikkawa, Yusuke Inoue, Masahito Kanamura, Naoya Okamoto,Kozo Makiyama, Kenji Imanishi, Hisao Shigematsu, Kazukiyo Joshin, and Naoki Hara ,"Reliability of GaN HEMTs: Current Status and Future Technology," IEEE CFP09RPS-CDR 47th Annual International Reliability Physics Symposium, Montreal, 2009.

[6-14] H. C. Chiu, S. C. Yang, F. T. Chien, and Y. J. Chan, "Improved device linearity of

AlGaAs/InGaAs HFETs by a second mesa etching," IEEE Electron Device Lett., vol. 23, no. 1, pp. 1-3, Jan. 2002.

[6-15] N. B. de Carvalho and J. C. Pedro, "Lager- and small-signal IMD behavior of microwave power amplifiers," IEEE Trans. Microw. Theory Tech., vol. 47, no. 12, pp. 2364-2374, Dev. 1999.