國 立 交 通 大 學

電子物理學系

碩士論文

隱藏式選擇性閘極結構之薄膜電晶體記憶體元件研究

A Study on Wrapped-Select-Gate SONOS-type Thin Film Transistor Memory Devices

指導教授：趙天生 博士

研 究 生：薛芳昌

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研 究 生 ：薛芳昌　　Student : Fang-Chang Hsueh

指導教授 ：趙天生 博士　Advisor : Dr. Tien-Sheng Chao

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摘要

我們首先提出一種新穎的隱藏式選擇性閘極結構薄膜電晶體記憶體元件，它的製程條件不僅簡單，也能與傳統的標準 CMOS 製程相容，特別適合嵌入式非揮發性記憶體的應用。在本篇論文中，我們首次在薄膜電晶體記憶體元件中嘗試更為有效的電子注入之源極端注入方式(Source-Side-Injection)來做寫入，以及能帶到能帶穿隧產生之熱電洞(BTBTHH)的機制來作為電子抹除的操作。此外，我們也同時驗證可消除二位元效應以及可在單一位元胞進行二位元的操作。值得注意的是，薄膜電晶體記憶體所需較大的操作偏壓會造成較嚴重的偏壓干擾現象，包括閘極干擾和汲極干擾。不同於分離式的電荷儲存元件，懸浮閘極結構的薄膜電晶體記憶體在寫入以及抹除操作中，面臨了可能威脅到免於二位元效應特性的懸浮閘極電壓耦合效應問題。

與單純由氮化矽組成的電子捕捉層和懸浮閘極結構的元件相比，在氮化矽中加入內嵌式矽奈米晶體作為電子捕捉層的元件，經過耐久度測試後的元件，都能夠有較佳的電子保存能力(約 6-8%的漏電改善)，尤其是在高溫的電子保存性量測中更為明顯。在耐久可靠度測試中，氮化矽元件以及在氮化矽中加入內嵌式矽奈米晶體作為電子捕捉層的元件有嚴重的電子電洞不匹配的問題以及在氧化矽中造成許多缺陷，這些造成元件的記憶體窗有關閉的傾向。然而對於懸浮閘極結構的記憶體元件而言，即使寫入狀態和抹除狀態的閥值電壓都會隨著測試次數增加而上升，仍然不會發生記憶體窗關閉的現象。

A Study on Wrapped-Select-Gate SONOS-type Thin Film Transistor Memory Devices

Advisor : Dr. Tien-Sheng Chao **Student : Fang-Chang Hsueh**

Abstract

For the first time, we proposed the novel Wrapped-Select-Gate (WSG) SONOS-type thin film transistor (TFT) memory device. The fabrication process of WSG structure memory device is not only simple but also compatible to conventional standard CMOS technology which fits for embedded non-volatile memory applications. In this thesis, we firstly apply source-side-injection (SSI) mechanism to three kinds SONOS-type thin film transistor memory and perform erase operation with Band-to-Band Tunneling Hot-Hole (BTBTHH). Furthermore, the elimination of 2^{nd} bit effect and 2 bit per cell operation are also demonstrated in the same time. It is worth to note that higher operation voltage in TFT memory causes serious disturb phenomena including word-line disturbance and bit-line disturbance. Unlike to discrete charge trapping devices, TFT memory cell with floating gate structure have floating gate coupling concerns in every program or erase operation which may threaten the immunity to 2^{nd} bit effect.

Compared to pure nitride trapping layer and floating gate structure, nitride with embedded silicon nanocrystals (Si-NCs) as trapping layer material always has better retention characteristics (6-8% improvement) when device already suffers 10k times P/E cycle, especially in high temperature retention test. In endurance characteristics, Nitride cell and Nitride_Dot cell suffer charge mismatch problem and generation of oxide defects which gives rise to window closure phenomenon while Floating gate cell still can maintain memory window even though both threshold voltage of program state and erase state keep on a rise.

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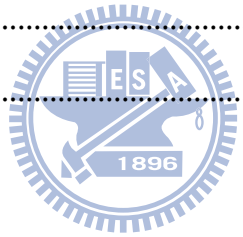


Figure caption

Chapter 1

Chapter 2

Chapter 3

Chapter 4

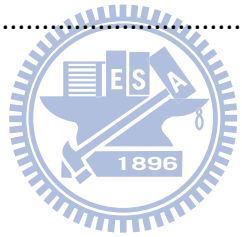


Table caption

Chapter 1

Chapter 2

Chapter 3

Chapter 1

Introduction

1.1 Overview of memory device and its challenges

Due to the explosive growth of portable devices in recent years, the urgent demand of large data storage that do not vanish when the power of device is turned off has attracted a lot of attention. The rapid-increasing development of non-volatile memory (NVM) can be attributed to the ubiquitous presence of MP3 player, digital still camera (DSC), USB, iPod, etc. [1.1]. There are two major types of Flash memory application – the code storage provided by the NOR architecture, and the data storage by the page access architecture of NAND type Flash, as shown in Fig. 1.1, Fig. 1.2. Flash memory revenues have reached > $20.4 billion dollars in 2008, $11.4 billion for NAND and $9 billion for NOR respectively, nearly 7.8% of annual semiconductor industry market.

In 1967, there is a epoch-making innovation in memory technology invented by D. Kahng and S. M. Sze, the first floating gate (FG) non-volatile memory using metal-insulator-metal-insulator-semiconductor (MIMIS) structure [1.2]. Generally, non-volatile memory (NVM) device have to keep the programmed state and the erased state for 10 years, which is defined by high state is “1” and low state is “0”, as shown in Fig. 1.3. However, the charges stored in floating gate (FG) give rise to a built-in field which empowers charges to tunnel back to channel [1.3]. Flash memories, inevitably must face severer reliability problems deriving from the continuous scaling of the past years. According to International Technology Roadmap for Semiconductor (ITRS), as shown in Table 1.1, the tunnel oxide have to be thick enough (> 8nm) to avoid an unacceptable reduction of retention and endurance

characteristics due to leakage current [1.4].

In the last years, several structures and materials have been reported for the purpose of getting over the scaling limitation of floating gate flash memory [1.5]. In order to ameliorate drain-induced-turn-on effect, floating gate coupling effect, and data retention capability, silicon-oxide-nitride-oxide-silicon (SONOS) Non-volatile Memory, Nanocrystal memory (NCM), MRAM, FeRAM, and Ovonic Unified Memory (OUM) are proposed to be candidates of the next generation memory technology.

1.2 Brief Introduction of SONOS Flash Memory Device

The SONOS Flash memory, as shown in Fig.1.4, has recently drawn attention for applications in electrically erasable and programmable read-only memories due to the advantages of lower operation voltage, better data retention, and faster program/erase speed. The cell consists of a single transistor, is immune to over-erase problem and exhibits satisfactory reliability characteristics. Moreover, most importantly, it has simpler fabrication process compatible with conventional CMOS technology, fit for embedded application. In addition to nitride trapping layer, people make a good effort to tunneling oxide engineering [1.6]. Because we choose silicon nitride as trapping layer material which has localized, and discrete trapping sites, we can have tunneling oxide to scale down to 4~5nm. In this way, we successfully suppress the tough situation resulting from stress-induced-leakage-current (SILC), Frenkel-Poole tunneling and trap-assisted tunneling (TAT). So, compared to the floating gate structure, we can make a breakthrough in the scaling of flash memory.

The programming and erase time usually are in the range of 10^{-6} -10^{-3} sec due to the tunneling mechanism. Programming is usually performed by three program

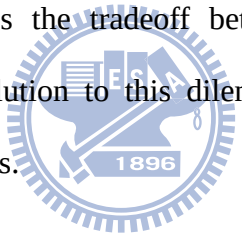
techniques: Fowler-Nordheim (FN) tunneling [1.7], channel hot electron (CHE) injection [1.8], and source-side injection (SSI) [1.9]. Besides, Fowler-Nordheim (FN) tunneling and band-to-band tunneling hot hole (BTBTHH) erase [1.10] are responsible for erasing process.

1.3 Brief Introduction of Nanocrystal Memory Device

Conventional floating gate flash has been the dominant and is the most widespread in nonvolatile memory (NVM) technology for the past three decades. However, the most serious issue of floating gate memory is the scaling of the tunnel oxide thickness around 7-10nm. Further thinning of this layer could give rise to an unacceptable leakage current. Consequently, there are considerable research efforts devoted to such flash memory utilizing discrete charge trapping site. Charge trapping devices such as nanocrystal memory (NCM), as shown in Fig. 1.5, has been considered as a candidate to replace conventional floating gate memory due to its superior scalability stemming from high defect tunneling immunity. Moreover, ease of integration is the most attracting factor in favor of charge trapping devices. In order to obtain memory devices with faster operating speed and lower peripheral voltage bias, Tiwari and his coworkers were the first to report that embedded Si nanocrystals (Si-NCs) in the gate oxide allows further scaling of the tunnel oxide [1.11]. Changes in threshold voltage are achieved by injecting charge into silicon nanocrystal dots that are placed between tunneling oxide and blocking oxide. Because of limited size, density, and capacitance of nanocrystal dots, Coulomb blockade effect may be very important in this structure. Also, various metal materials as nanocrystal layer have been widely discussed due to their different work function value [1.12]. Because issues with semiconductor-based nanocrystals are not large enough work function,

work function lowering effect related to quantum-confinement and poor control ability to its size and density.

In NCMs, the charge stored in silicon NCs layer instead of continuous polysilicon floating gate. Thus, NCM exhibits better retention characteristics than that of floating gate structure. It also features immunity to drain-turn-on effect and simple fabrication process compatible to conventional CMOS technology. Despite these advantages, NCMs still have three major challenges for the mass production. First of all, we still have no effective ways to precisely control the uniformity of NCs formation. In order to achieve better data retention time, we should devote more effort to obtaining well-ordered high density NCs. Secondly, although metal NC enhance program efficiency, the accompanied contamination problem can evoke the degraded characteristics. The last issue is the tradeoff between program/erase speed and retention time. One possible solution to this dilemma situation can be to choose high-k materials as gate dielectrics.



1.4 Brief Introduction of Thin-Film Transistor Memory

Nonvolatile memories (NVMs) with high density, large memory window, and excellent data retention ability have attracted much attention in electronic products in these days. Especially, thin-film transistor (TFT) memory have been successfully fabricated for applications such as system-on-panel (SOP) and system-on-chip (SOC) technologies. Owing to battery saving issue for novel electronics products, the power consumption of system have already made further progress with the help of built-in memory. Moreover, nonvolatile integrated memory can offer people additional functionality. For these reasons, a number of thin-film transistors with special structures have been an emphasized investigating research area in recent years. Lin *et*

al. proposed a nonvolatile polycrystalline silicon channel thin-film transistor memory using three different kinds of high permittivity as charge trapping layer which is annealed at 600^{o}C after their deposition processes. They exhibited millisecond program and erase time and achieved 2-bit operation without significant disturbance for SOP [1.13]. Chiang *et al.* reported a novel P-N-Diode structure SONOS-type thin film transistor memory with embedded silicon nanocrystals. The larger memory window (12V) and longer data retention time (only 12% charge loss for 10^{8} s) enables PND-TFT memory to be a promising candidate for multilevel operation and system-on-chip application [1.14]. With the development of 3D integration, Yin *et al.* first demonstrated an experimental device with 3-D fin-like channel structure for system on panel and embedded memory applications. By applying a special operation mode, backside FN program and erase, they showed millisecond P/E characteristics with threshold voltage shift of 1.41V, and acceptable endurance and retention characteristics [1.15]. In order to integrate multi-functional and advanced circuits on SOP or SOC, there still a lot of efforts need to be made to scale down device size and to minimize the operation voltage for power consumption issue.

1.5 Motivation

In recent years, many people are gradually conscious that SONOS-type Flash EEPROMs are gaining prominence because they have smaller bit size, absence of floating-gate coupling effect as well as simple fabrication process, provide low power consumption, and multi-bit per cell or multi-level cell capability which is based on localized charge trapping properties. As floating gate structure memories run into the scaling challenge that over-scaled tunneling oxide may give rise to a stress-induced-leakage-current (SILC) problem, all of us are looking forward a device

with not only faster operation speed but also better data retention characteristics. Therefore, SONOS-type Flash has been extensively discussed for a long time. Conventional planar SONOS-type structure memories, however, still have some concerns in developing into multi-bit cell which we called 2^{nd} bit effect [1.3]. Any interference between two bits of a cell may lead us to unacceptable memory state misidentification. In this work, we investigate wrapped-select-gate structure with three kinds of electron trapping layer materials which are pure nitride, nitride with embedded silicon dots and N^+ floating gate. The experimental results can offer us a choice to developing a device combining most of advantages we mentioned before.

1.6 Organization of the thesis

The organization of the thesis is separated into five chapters. Following a brief introduction of various memory devices in chapter 1, the fabrication process of Wrapped-Select-Gate SONOS-type thin film transistor memory device and experimental measurement setup is explicitly discussed in chapter 2 which also exhibits the operation mode and the disturbance of memory device. In chapter 3, we will show basic characteristics and 2^{nd} bit effect of memory device. The reliability of WSG-SONOS-type TFT memory will be discussed in chapter 4. Lastly, conclusions will be presented in chapter 5.

NOR Array

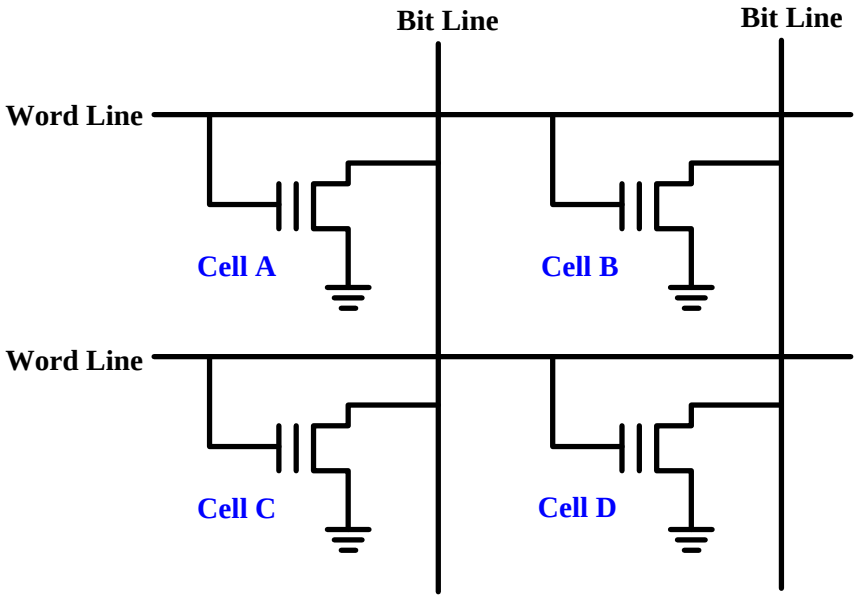


Fig. 1. 1 The equivalent circuit schematic of NOR architecture.

NAND Array

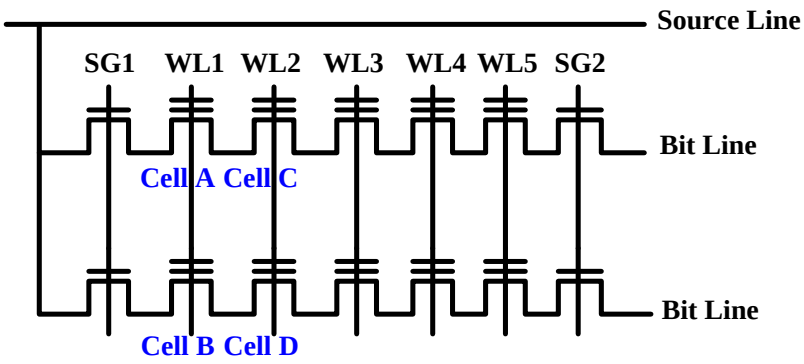


Fig. 1. 2 The equivalent circuit schematic of NAND architecture.

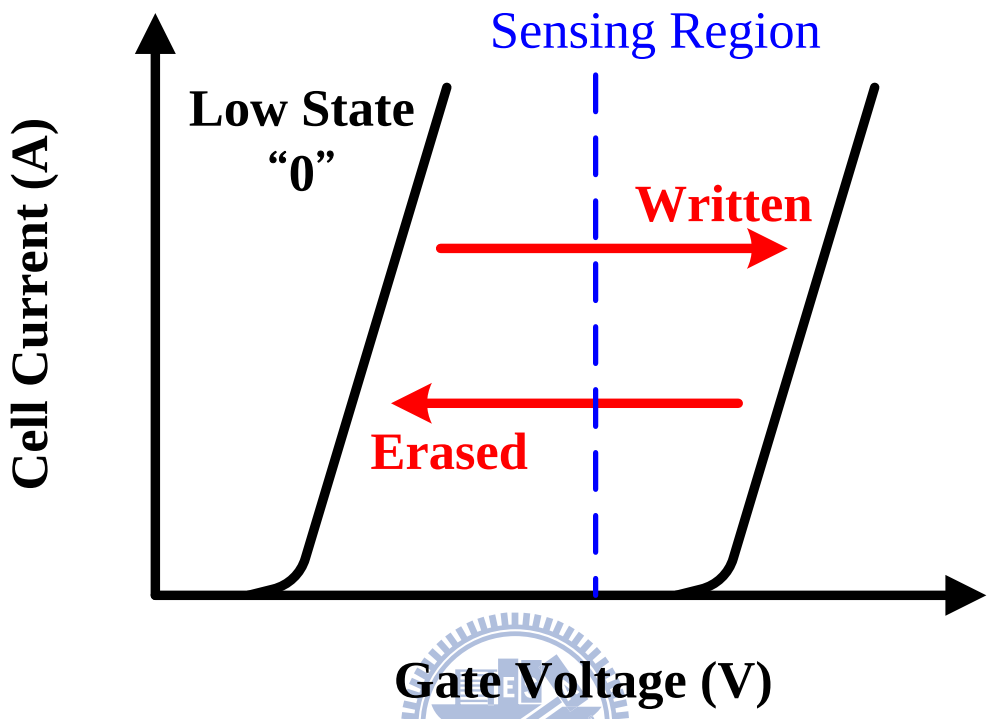


Fig. 1. 3 Definition of "1" and "0" state in Id-Vg curve

Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
NOR Flash technology – F (nm)	**45**	**40**	**35**	**32**	**28**	**25**	**22**	**20**	**18**
A. Floating gate NOR Flash									
Cell size—area factor a in multiples of F^2	**9-11**	**9-11**	**9-11**	**9-11**	**9-11**	**9-11**	**10-13**	**10-13**	**10-13**
Gate length L_g, physical (nm)	**110**	**100**	**100**	**90**	**90**	**90**	**?**	**?**	**?**
Tunnel oxide thickness (nm)	**8–9**	**8–9**	**8–9**	**8**	**8**	**8**	**?**	**?**	**?**
Interpoly dielectric material	**ONO**	**ONO**	**ONO**	**High-κ**	**High-κ**	**High-κ**	**High-κ**	**High-κ**	**High-κ**

Table 1. 1 Non-volatile Memory Technology Requirements for NOR Flash in ITRS 2010 Edition _ Process Integration, Devices, and Structures [1.4].

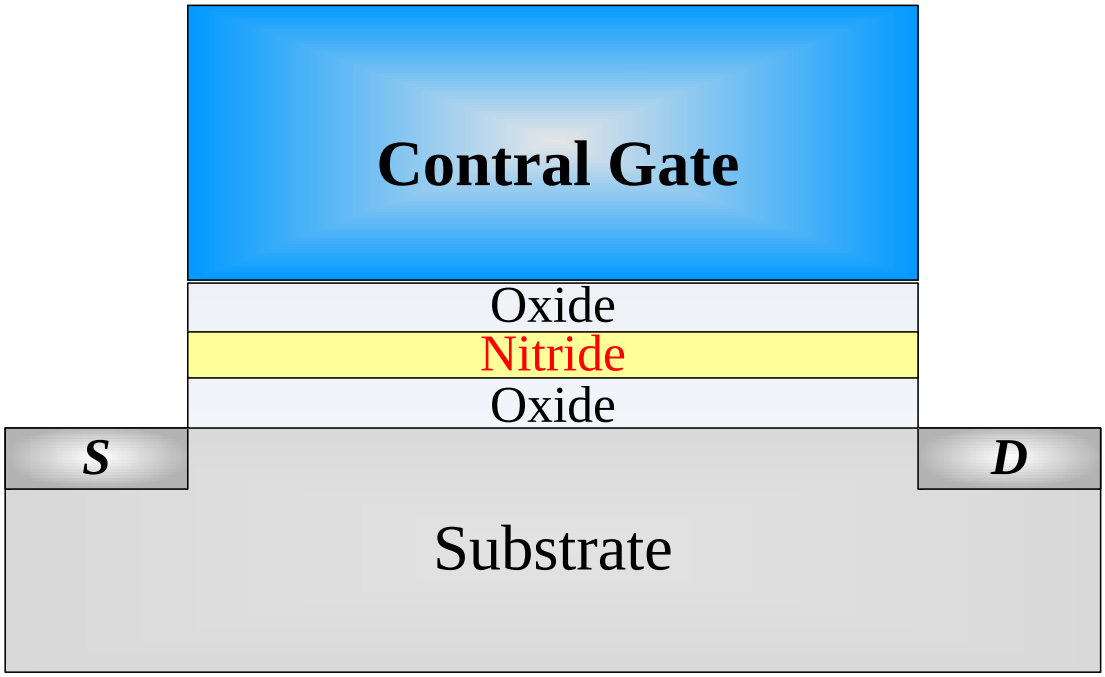


Fig. 1. 4 Schematic of conventional SONOS-type NVM device

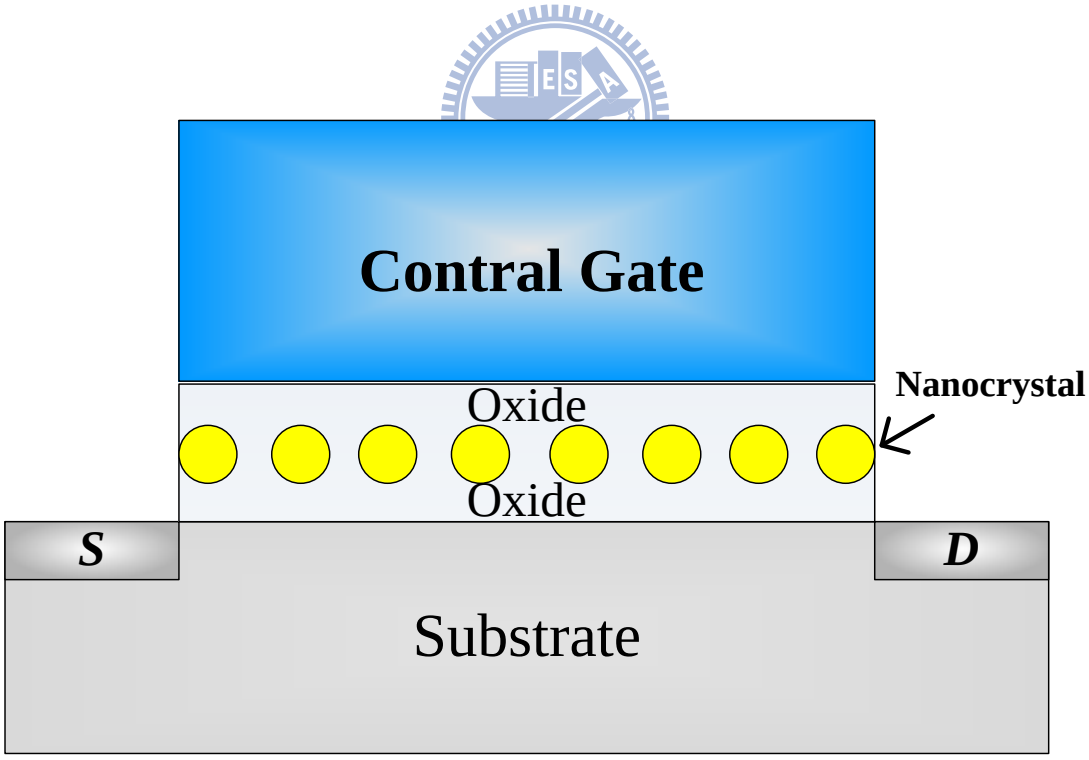


Fig. 1. 5 Schematic of nanocrystal memory device

Chapter 2

Device Fabrication and Experimental Setup

2.1 Introduction

With the evolution of nonvolatile memory (NVM) from floating gate structure to charge trapping device, SONOS-type flash memory have been extensively discussed due to its excellent data retention and fast operation speed. As tunneling oxide of SONOS-type flash memory is scaled down to 3nm, the average time for programming and erase is usually in the range of microsecond and millisecond. On the other hand, in order to integrate additional functionality into system-on-panel (SOP) and system-on-chip (SOC), thin film transistor memory have been an emphasized investigating research area in recent years. In this chapter, we report a thin film transistor memory device using wrapped-select-gate structure with different electron trapping layer materials, nitride, nitride with embedded silicon nanocrystals and N^+ floating gate, based on conventional ONO-type structure. Besides, we will also introduce the mechanism during program, erase and read operation. Finally, drain disturbance and gate disturbance phenomena will be carried into brief discussion respectively.

2.2 Experimental Procedure

Unlike most conventional two-bit memory devices, as shown in Fig.2.1, our SONOS-type memory has two polycrystalline silicon gates, select gate and word-line gate. Fig. 2.2 shows the former gate is wrapped with oxide-trapping material-oxide

layer above channel film and subsequently covered by word-line gate. Compared to other novel memory device, its simpler fabrication procedure is totally compatible with traditional CMOS process flow.

It is the first time we successfully fabricated Wrapped-Select-Gate SONOS-type memory on simulated glass substrate to be a thin-film-transistor (TFT) memory, First of all, silicon wafer with 5500 Å wet oxide were used as starting substrate. Then, a 500 Å amorphous Si (a-Si) film for the channel region was deposited at 500 ^{o}C by low-pressure chemical vapor deposition (LPCVD) and patterned by plasma dry etching. The deposited a-Si films were recrystallized by solid-phase-crystallization (SPC) at 600 ^{o}C for 24hr. To form inner assistant gate, we deposited 180 Å TEOS oxide, 1000 Å in-situ N^{+} ploy-Si layer, and 1000 Å nitride. The thick nitride layer above select gate is served as isolation between select gate and word-line gate. Subsequently lithography and etching was performed. After pattering select-gate structure, the tunnel oxide/trapping layer/blocking oxide stack layer was deposited as ONO-type dielectric layer. These thin film thickness are 180 Å, 120Å and 235Å respectively. In this experiment, trapping layer materials are pure nitride, nitride with embedded silicon nanocrystals [2.1] and N+ floating gate. Following the 2000 Å poly-Si deposition and word-line gate patterning, gate implant and source/drain region were formed by self-alignment technique. The cross-section of WSG-SONOS thin film transistor (TFT) memory device (a) Nitride cell (b) Nitride_Dot cell (c) Floating gate cell and examples of basic operation bias are shown in Fig. 2.3-2.5 and Table 2.1.

2.3 Measurement and Equipment Setup

Fig. 2.6 shows the connection of each measurement apparatus for I-V curve and threshold voltage characteristics which is composed of semiconductor

characterization system (KEITHLEY 4200), two channel pulse generator (Agilent 81110A), low leakage current switch mainframe (KEITHLEY 708A) and the probe station. Stable measuring environments provide us accurate electrical characteristics extraction.

The timing diagrams of program and erase operation are shown in Fig. 2.7. KEITHLEY 4200 equipped with programmable source-monitor unit (SMU) and a high resolution current amplifier with pico-ampere range is the main control system here which is responsible for electrical characteristics measurement. Besides, Agilent 81110A with two pulse channels can not only offers us a high timing resolution pulse for P/E cycling in ordinary flash memory endurance test but also be used in every program and erase pulse. In order to obtain excellent ability to precisely control the pulse level and pulse timing of Agilent 81110A, the triggered pattern mode is used by the GPIB baseband between Agilent 81110A and KEITHLEY 4200. In our measurements, the duty cycle is 50% and the pulse period is set larger than100ns for better square pulse, while the both edge of rising time and falling time are larger than 25-50ns to prevent under-shoot and over-shoot from happening. Moreover, the C^{++} language is applied to take control of different equipment such as the low leakage current apparatus KEITHLEY 708A with 10-input and 12-output switching matrix which can automatically switch the signals to the device under test. That is why this measurement system empowers us to investigate different program/erase/read techniques in novel Wrapped-Select-Gate SONOS-type thin film transistor memory.

2.4 Operation of Program/Erase/Read

The WSG SONOS-type TFT memory was programmed and erased by applying source side injection [1.9] and band-to-band tunneling hot hole injection mechanism

respectively. The hot electrons were accelerated by high electric field in the gap region between word line gate and select gate. Under high word line gate bias, electrons which were accelerated due to horizontal electric field have larger injection efficiency to trapping layer compared to conventional channel hot electron injection, as shown in Fig. 2.8. The program condition is set at V_{WL} = 18V, V_{BL} = 8V, V_{SG} = 0.6V. Secondly, the band-to-band tunneling hot hole injection mechanism is employed to neutralize electrons trapped in our different trapping layer materials. Under a reverse bias of the p-n junction, excess holes are generated and then are accelerated by lateral field. By gaining enough energy from electric field, these hot holes could easily overcome potential barrier height, jump into electron storage layer, and then recombine with electrons in trapping layer, as shown in Fig. 2.9. In the read mode, the sweeping voltage of word line gate is from -4V~9V, in the meanwhile, V_{BL} and V_{SG} remain 6V and 4V respectively for better second bit effect characteristic. In order to perform two bit operation, forward read and reverse read are applied to confirm the state of Bit 1 and Bit 2, as shown in Fig. 2.10 and Fig. 2.11. In this work, threshold voltage (V_T) is defined as the applied word line gate voltage when the sensing current is 10^{-7} A in read mode. Memory window is defined as the V_T shift between program state and erase state.

2.5 Disturbance Characteristics

Fig. 2.12 shows two types disturbance of memory array during programming which called gate (word-line) disturbance and drain/source (bit-line) disturbance [2.2]-[2.3]. When Cell A is programmed, gate disturb takes place in Cell B and the drain disturb takes place in Cell C. Operation bias applied to neighboring un-selected cells might result in high electric field across gate dielectrics helping electrons to trap

or de-trap. The tunneling of electrons in these neighboring cells causes significant threshold voltage shift. Besides, there also exists another type of disturbance when we are reading a specific memory cell in the array which we called read disturbance [2.4]. These disturbance characteristics may restrain the feasibility of multi-level operation.

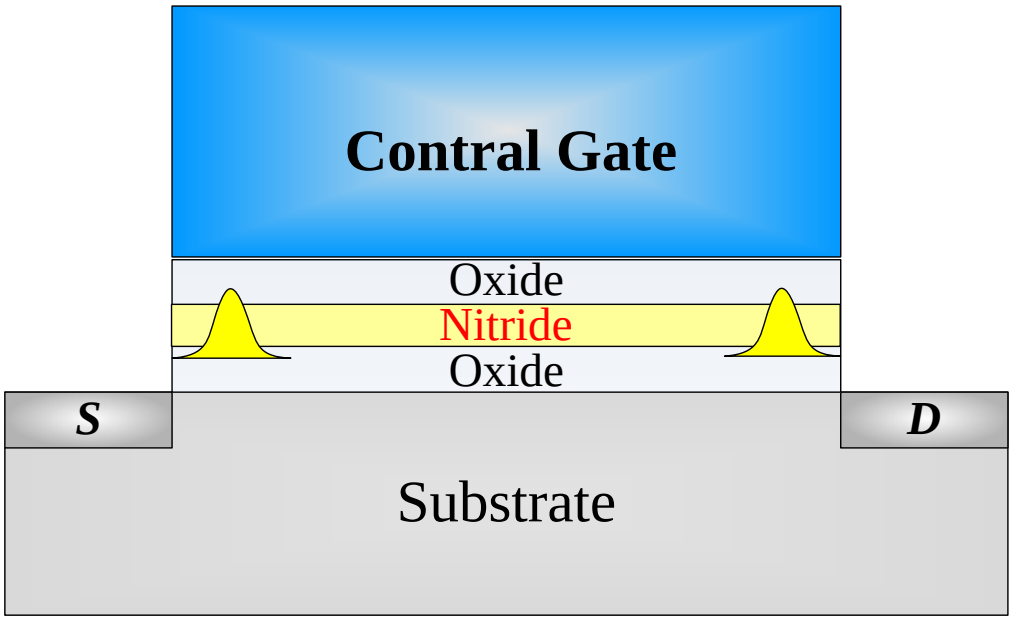


Fig. 2. 1 Schematic of conventional two-bit SONOS-type memory

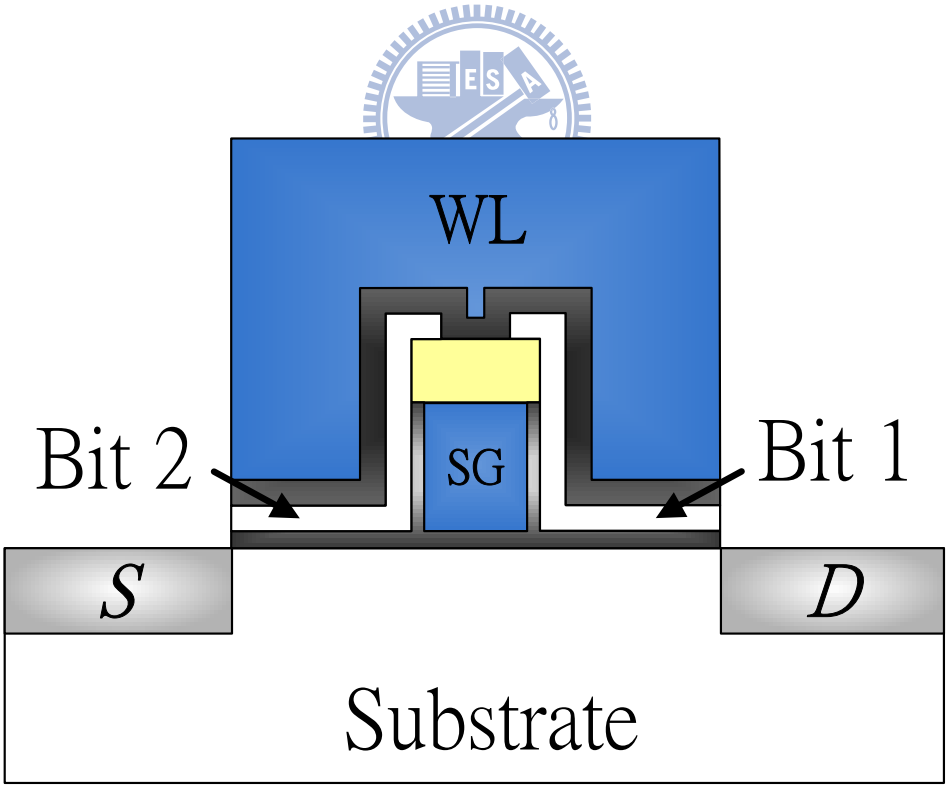


Fig. 2. 2 Schematic of two-bit WSG SONOS-type memory

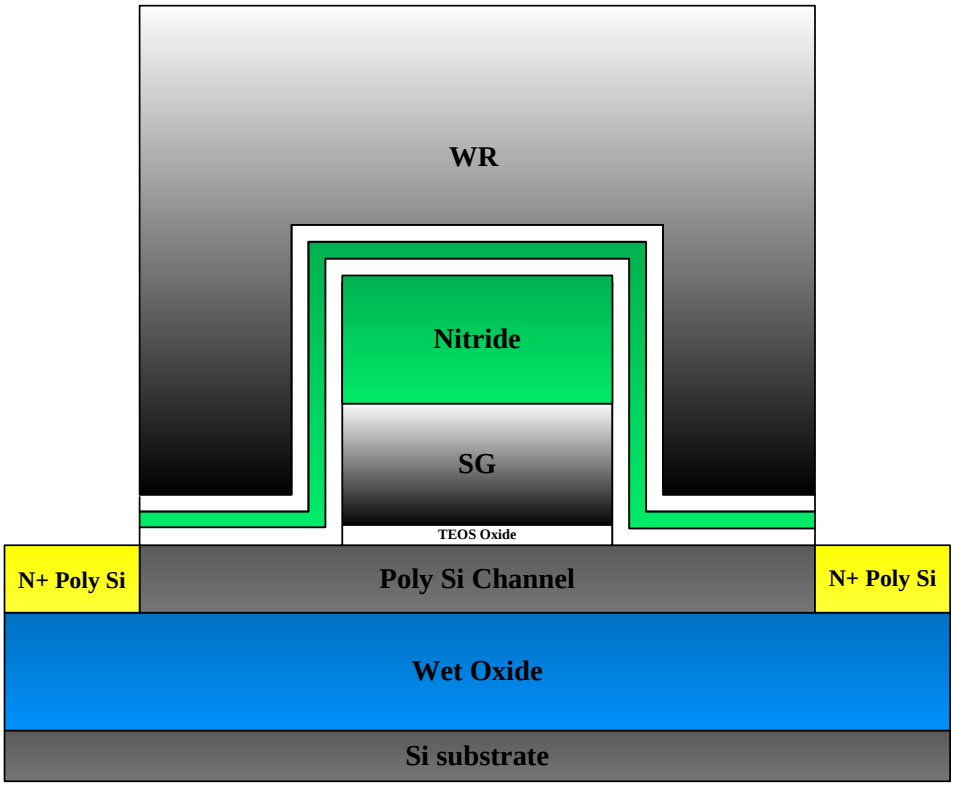


Fig. 2. 3 Schematic of WSG SONOS-type TFT memory (a) Nitride cell

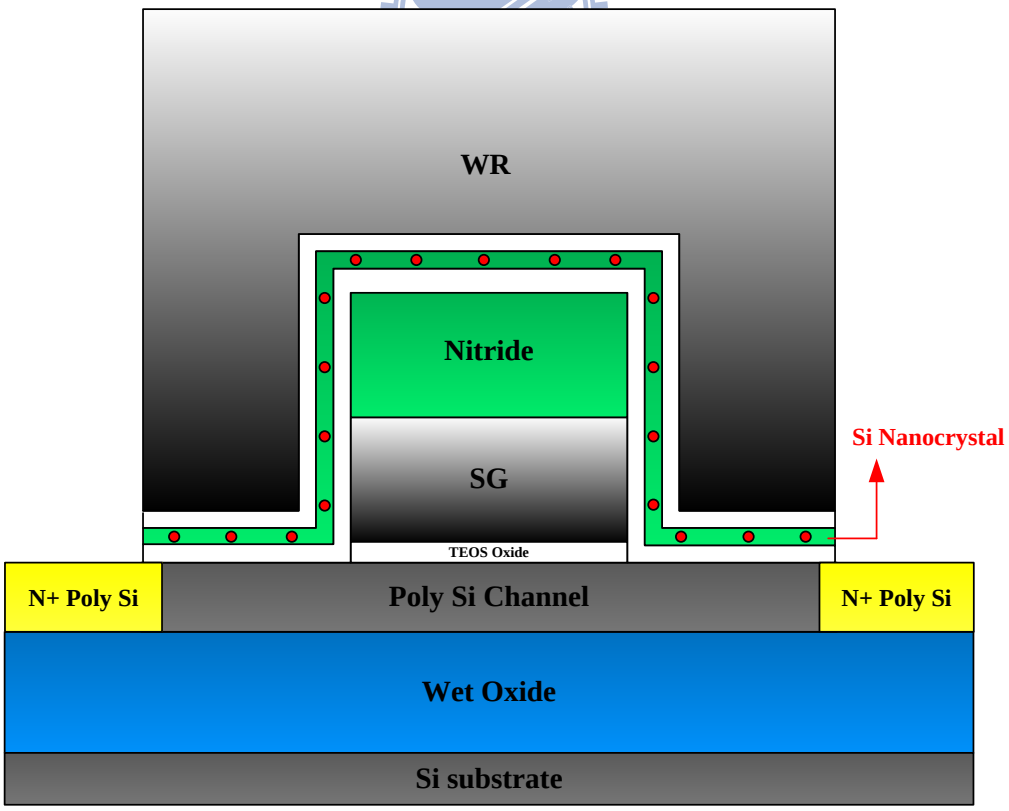


Fig. 2. 4 Schematic of WSG SONOS-type TFT memory (b) Nitride_Dot cell

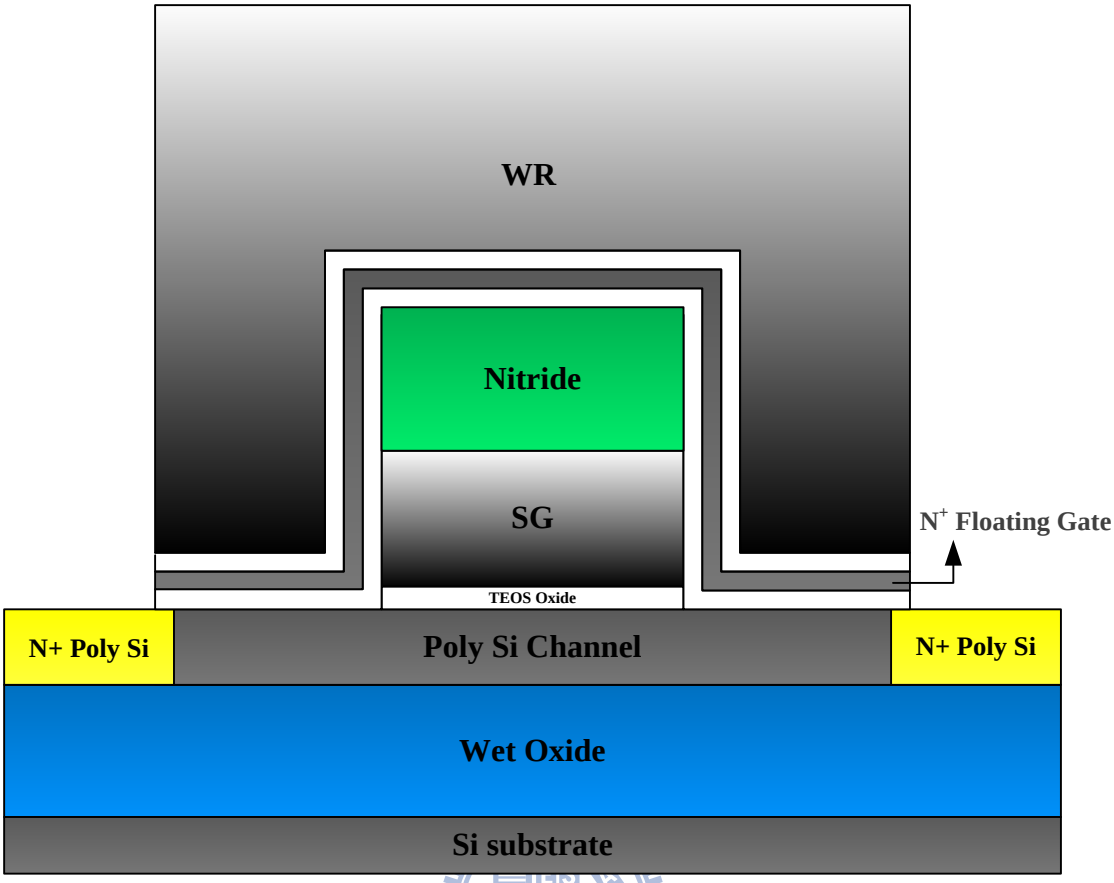


Fig. 2. 5 Schematic of WSG SONOS-type TFT memory (c) Floating gate cell

WSG SONOS TFT Memory		Program	Erase
Bit 1	V_{WL}	18V	-8V
	V_D	8V	18V
	V_{SG}	0.6V	0V
Bit 2	V_{WL}	18V	-8V
	V_S	8V	18V
	V_{SG}	0.6V	0V

Table 2. 1 Bias condition of WSG SONOS-type TFT memory operation.

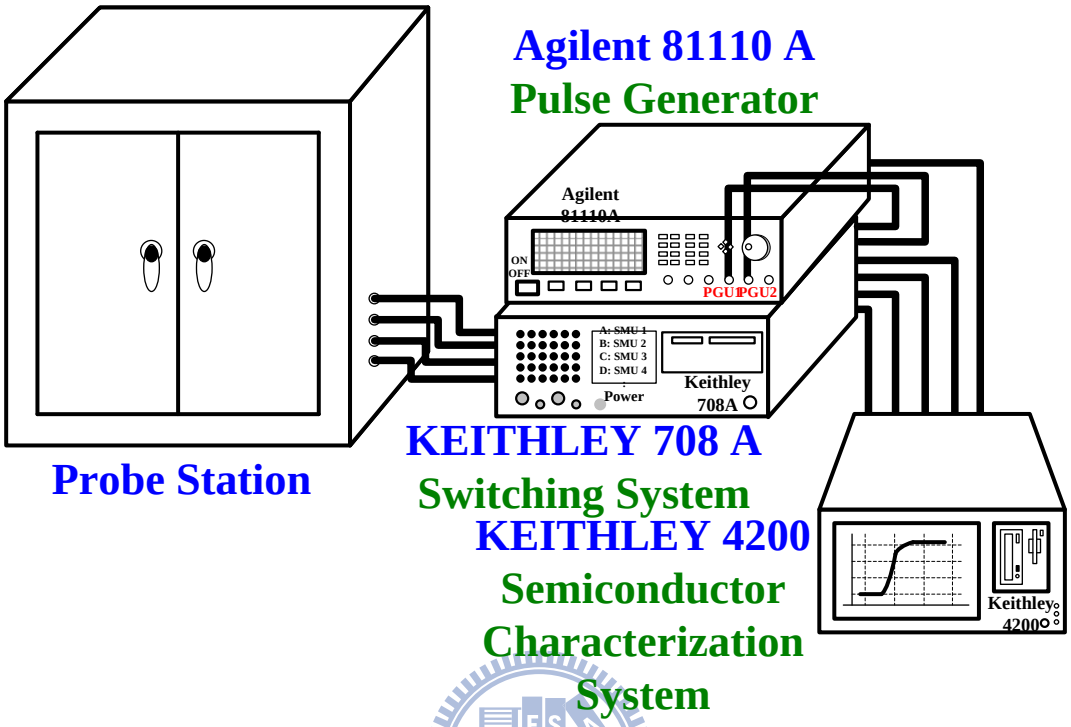


Fig. 2. 6 The experimental setup of each apparatus for pulse generator and I-V characteristics measurement of memory cell.

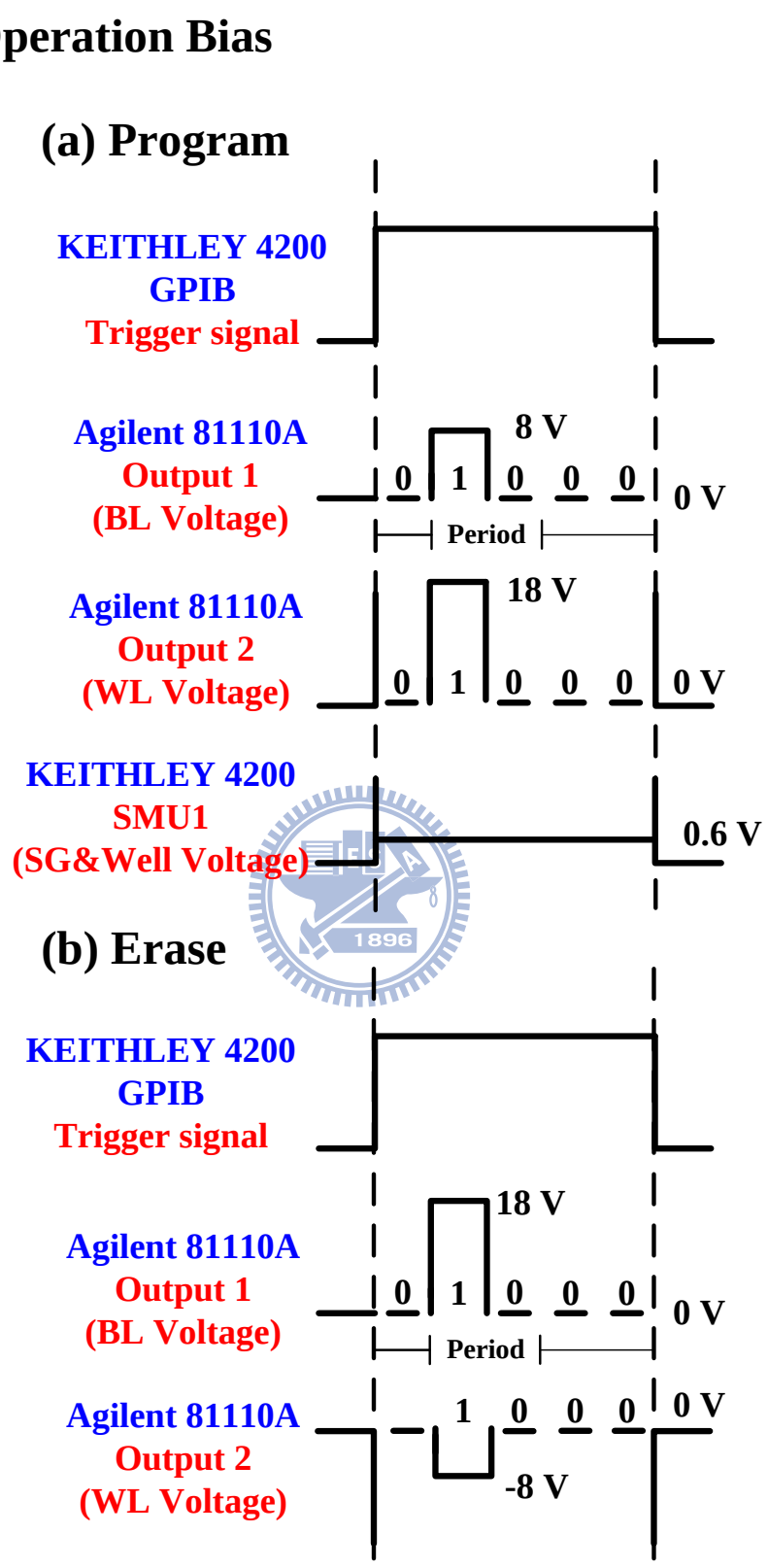


Fig. 2. 7 The timing diagrams of the two-pulse generator, Agilent 81110A, during (a) program and (b) erase.

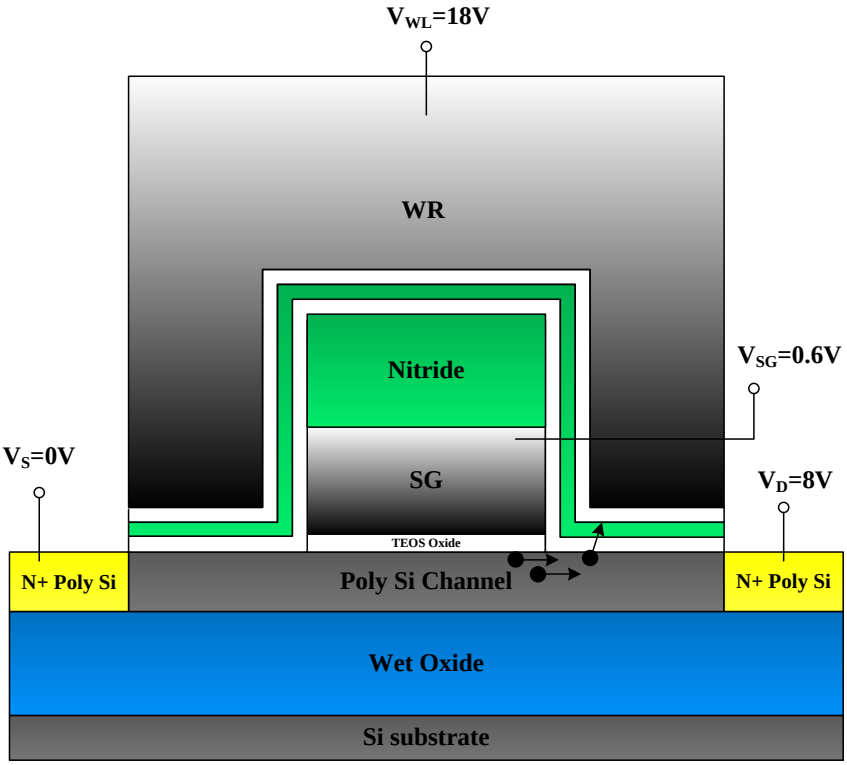


Fig. 2. 8 Cross-sectional scheme of WSG-TFT memory during programming

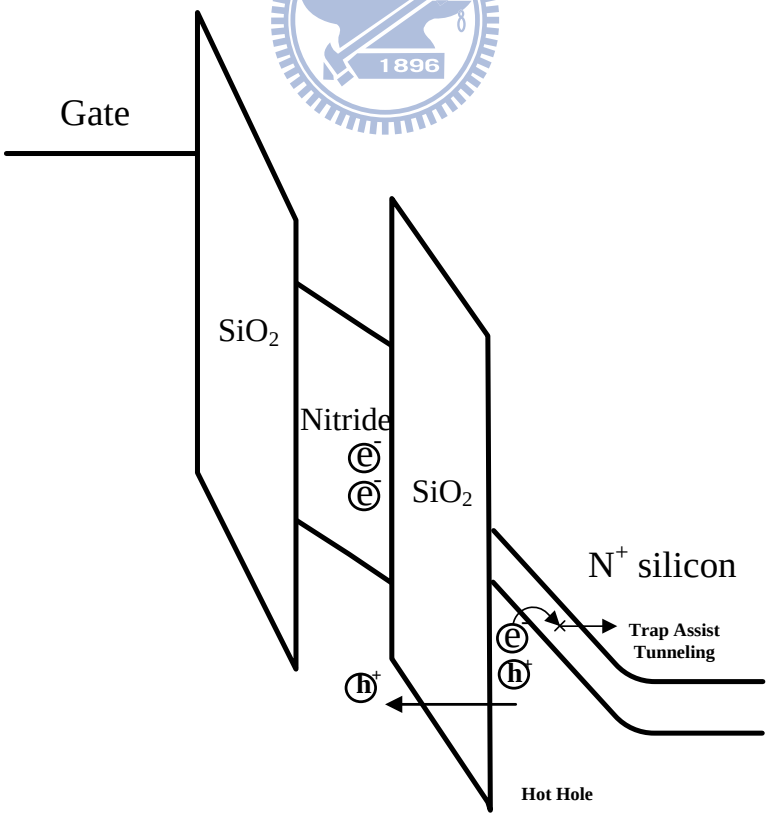


Fig. 2. 9 The energy band diagram of band-to-band tunneling hot hole injection

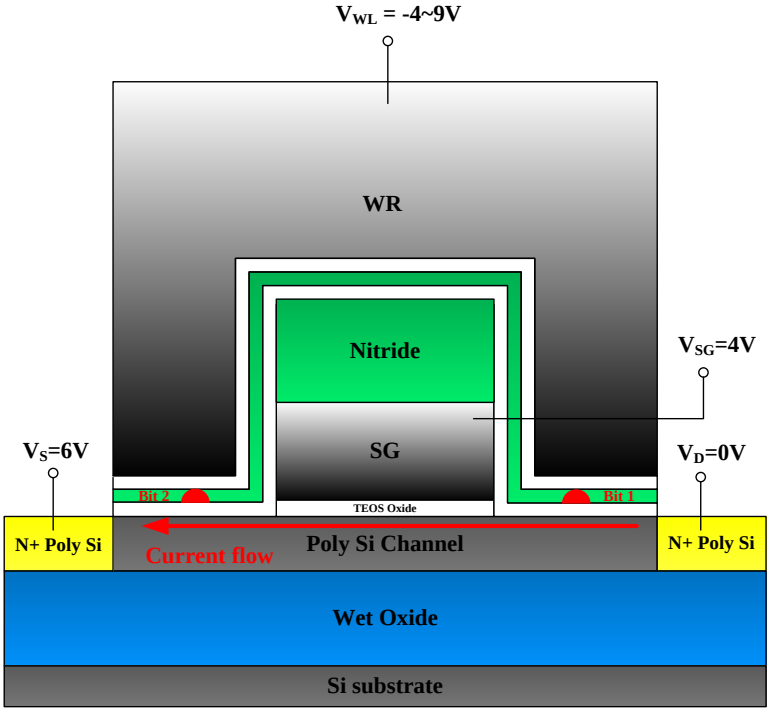


Fig. 2. 10 The operation of reverse read Bit 1 in WSG-SONOS TFT memory cell.

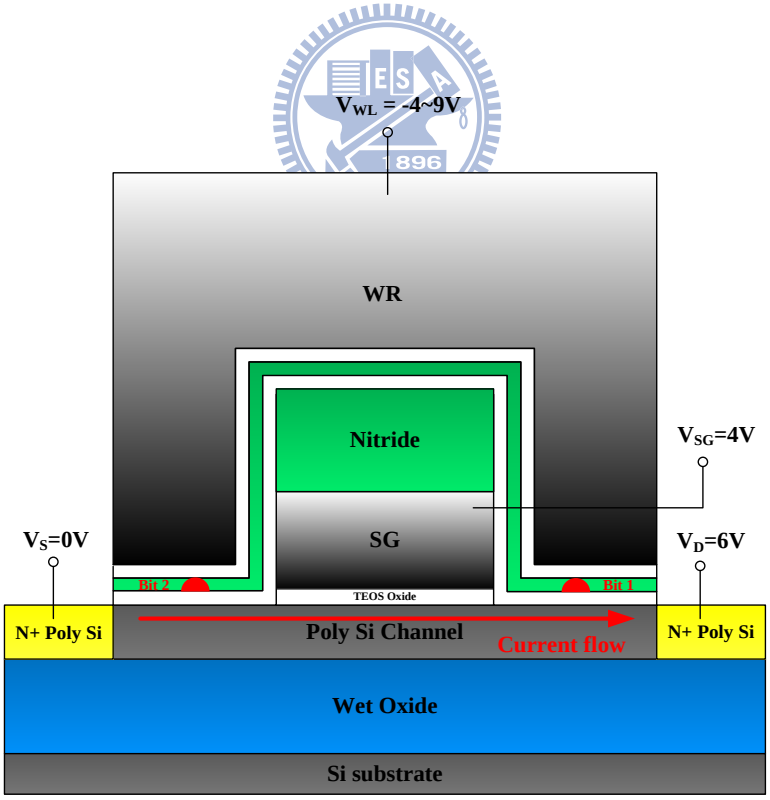


Fig. 2. 11 The operation of reverse read Bit 2 in WSG-SONOS TFT memory cell.

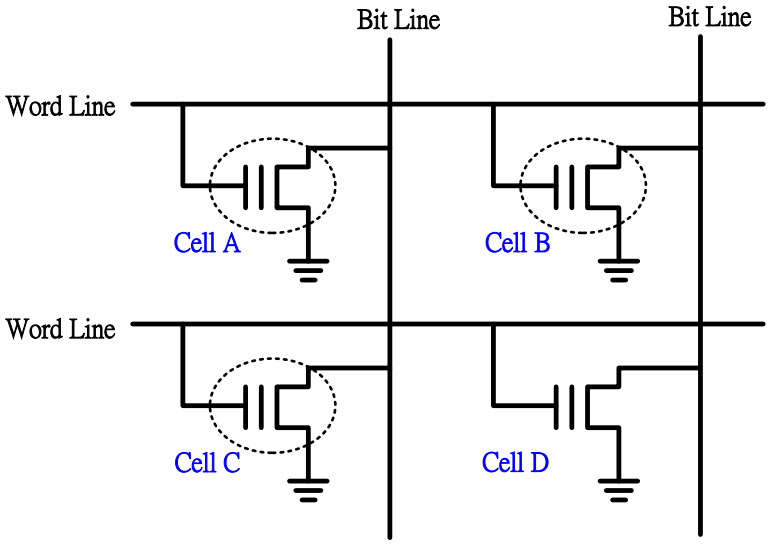


Fig. 2. 12 The circuit schematic of memory cells. When Cell A is programmed, gate disturb occurs in Cell B and the drain disturb occurs in Cell C.

Chapter 3

Characteristics of WSG-SONOS-type TFT memory

3.1 Introduction

In order to meet the emerging demand of portable electric products, we need a flash memory device with faster program speed, faster erase speed, smaller cell size, higher density, and the most importantly, reasonable sell prices. For this reason, high performance memory device and two bits per cell technique have been studied for a long time [3.1]-[3.3]. The main idea of this novel technique is that we have charges localized trapping in discrete storage trapping site near source side and drain side. Moreover, we can precisely determine two bit states in a flash memory cell by using reverse read technique.

In this chapter, we will discuss the mechanism of program and erase of wrapped-select-gate structure memory cell. Conventional schematic of program speed and erase speed is attained for different bias condition. Additionally, we find that V_{SG} also plays an important role in programming process of wrapped-select-gate thin film transistor memory device. Then we discuss the problems and challenges of 2^{nd} bit effect by measuring in forward read and reverse read. The above discussions are carried into three types of trapping layer in our experiments.

3.2 Results and Discussions

For wrapped-select-gate SONOS-type TFT memory, we have two transistor characteristic in one cell which were controlled by word-line gate and select gate respectively. Fig. 3.1 - Fig. 3.3 show basic I_D-V_{WL} characteristics for three types of

WSG TFT memory. On the other hand, Fig. 3.4 - Fig. 3.6 show inner $I_D V_{SG}$ characteristics of Nitride-based (Nitride) cells, Nitride with Si dot (Nitride_Dot) cells, and N^+ floating gate (Floating gate) cells. They have similar on/off ratio and threshold voltage in low drain voltage measurement. We additionally observe that Floating gate cell have serious floating gate coupling problem in Fig. 3.6. The off current is rise when V_{SG} is larger than 8V.

As mentioned before, split gate structure can offer a more effective way for electrons to tunnel into trapping layer that we called source side injection [3.4]. Fig. 3.7 shows program speed characteristics of Nitride cell with different word-line gate voltage. We can observe that V_{WL}=18V case has the fastest speed for programming. 3V memory window can be achieved in few micro-second. The same results also occur in Nitride_Dot cell and Floating gate cell, as shown in Fig.3.8 and Fig. 3.9. Although having faster speed in short programming time, Floating gate cell cannot separate program operation for bit1 and bit2 due to floating gate coupling. That is to say, in this operation bias, Floating gate cell no longer has two bit per cell operation characteristics. So we also exhibit another operation bias for program in Fig. 3.10 which apparently has slower speed and acceptable 2nd bit effect with 2V memory window. In order to make it clear to understand where is the main injection location for electron tunneling by source-side-injection mechanism, the simulated electric field is performed both laterally and vertically, as shown in Fig.3.11 and Fig.3.12.. Channel region ranges from x=-0.5μm to x=0.5μm and voltage bias are set to be V_{WL}=16~18V, V_{BL}=8V, and V_{SG}=2V. We find that V_{WL}=18V case has both strongest lateral and vertical electric field in ONO gap between word-line gate and select gate. By increasing word-line gate voltage, the voltage difference between word-line gate and inversion layer increases. Thus, we have larger vertical electric field. At the same time,

the bit-line voltage becomes easier to couple into gap region by inversion region. In this way, higher voltage difference between two inversion regions gives rise to larger lateral electric field. That is why V_{WL}=18V case shows the fastest program speed and largest memory window.

Let's talk about the influence of bit-line voltage in program speed measurement. Voltage bias are set to be V_{WL}=17V, V_{BL}=7~9V, and V_{SG}=0.6V. As shown in Fig. 3.13 to Fig. 3.15, the larger bit-line voltage is applied, the faster program speed we have. In order to attain acceptable two bit operation, junction breakdown injection mechanism was performed to single side programming, as shown in Fig. 3.16. Also, the results of simulated lateral and vertical electric field are shown in Fig. 3.17 and Fig. 3.18. When we increase bit-line voltage, higher voltage difference between word-line inversion and select gate inversion regions gives rise to larger lateral electric field. Besides, the voltage difference between word-line gate and its inversion region decreases which suppress vertical electric field of gap region.

In wrapped-select-gate structure memory, not only word-line gate voltage and bit-line voltage but also select gate voltage can control the programming current and electric field during program speed measurement. The following measurements are divided into two parts, large V_{SG} (V_{SG}=1, 2, 3 V) and small V_{SG} (V_{SG}=0, 0.4, 0.8 V). Fig. 3.19 shows that large V_{SG} could result in the suppression of electron tunneling from channel to nitride trapping layer. However, in small V_{SG} measurements, three cases exhibit comparable program speed characteristics, as shown in Fig. 3.20. Without the suppression of electric field, programming current becomes dominant in these tests. We find that V_{SG}=0V case still have equal programming current compared to V_{SG}=0.8V case due to large operation bias like V_{WL}=18V and V_{BL}=8V. The same results are repeated in Nitride_Dot cell and Floating gate cell, as shown in Fig. 3.21 to

Fig. 3.24. Regarding the single side programming for Floating gate cell by junction breakdown injection mechanism, programming current no longer plays a key role in these measurements, as shown in Fig. 3.25 and Fig. 3.26. When select gate voltage is increased, both lateral and vertical are suppressed which give rise to slower program speed. The simulations of electric field are also carried out to demonstrate the influence of select gate voltage, as shown in Fig. 3.27 and Fig. 3.28.

In this thesis, we use reverse read and forward read techniques to determine the states of bit1 and bit2. However, traditional SONOS memory device exists the interference between two states we called 2nd bit effect [3.5]-[3.7]. Fig. 3.29 shows the interference between programmed bit1 and erased bit2 of WSG TFT memory Nitride cell. Threshold voltage variation of bit2 is smaller than 1V under applying V_{BL}=6V and V_{SG}=4V. In this way, we indeed have memory window larger than 4V. Fig. 3.30 also shows the interference between programmed bit1 and erased bit2 of WSG TFT memory Nitride_Dot cell. Under reading voltage V_{BL}=6V and V_{SG}=4V operation, Nitride_Dot still exhibits acceptable V_T variation of bit2 although bit1 is programmed to larger memory window. Based on single side programming, Floating gate cell also shows 2V memory window in spite of serious floating gate coupling effect, as shown in Fig. 3.31.

Erase operation is performed by band-to-band tunneling hot hole injection and junction breakdown mechanism. Holes are accelerated by large positive bit-line voltage and tunnel into trapping layer. Fig. 3.32 shows erase speed of WSG TFT memory Nitride cell with V_{WL}=-6~-8V. We observe that V_{WL}=-8V, V_{BL}=18V, V_{SG}=0V case exhibits the fastest erase speed due to the largest tunneling opportunity resulting from vertical electric field. Fig. 3.33 shows the influence of V_{BL} in erase speed measurements. We know that larger junction reverse bias would generate more holes

around junction region. As we expected, among three cases of V_{BL}=16, 17, 18V, V_{BL}=18V shows the greatest erase ability, about 6V in one second. Fig. 3.34 and Fig. 3.35 show erase speed characteristics of WSG TFT memory Nitride_Dot cell with various word-line voltages and bit-line voltages. Compared to the results of Nitride cell, they have comparable erase speed in both measurements. For Floating gate cell, owing to floating gate coupling, they have faster erase speed in short erase time, as shown in Fig. 3.36 and Fig. 3.37. After measurement with different word-line bias and bit-line bias, we still need to confirm the hot holes injection location during erase. We observe that both lateral and vertical direction have large electric field peak right in the overlapped region of word-line gate and drain region, as shown in Fig. 3.38 and Fig. 3.39. However, operation bias of BTBTHH may lead to unwanted situation that bit 1 and bit 2 are erased at the same time. In order to achieve two bit operation, single side junction breakdown mechanism with smaller operation voltages is performed again with V_{WL}=-8V, V_{BL}=15V, and V_{SG}=0V. Fig. 3.40 and Fig. 3.41 shows slower erase characteristics of Floating gate cell with acceptable 2^{nd} bit effect.

In the end of this chapter discussion, all programming and erase mechanism of different cells are listed in Table 3.1. Speed, 2^{nd} bit effect, and endurance to 10K time P/E cycle are carried to comparison sheet.

3.3 Summary

Owing to the development of portable electronic devices, people are looking forward memory devices with fast program speed, fast erase speed, and high density characteristics. Wrapped-select-gate structure memory devices show excellent P/E speed with source-side injection and BTBTHH injection mechanism. Moreover, WSG structure memory devices also perform two bit operation exhibiting good immunity to

2^{nd} bit effect. We also observe that the increase of word-line gate voltage will enhance both lateral and vertical electric field during programming. On the other hand, the increased bit-line voltage will enhance lateral electric field but suppress vertical electric field at the same time. For erase operation, bit-line voltage is responsible for generation of excess holes while word-line voltage take charge of tunneling efficiency. Among three types of WSG TFT memory, Floating gate cell suffers serious floating gate problems. Nitride cell and Nitride_Dot cell show great potential to scaling down and outstanding P/E characteristics.

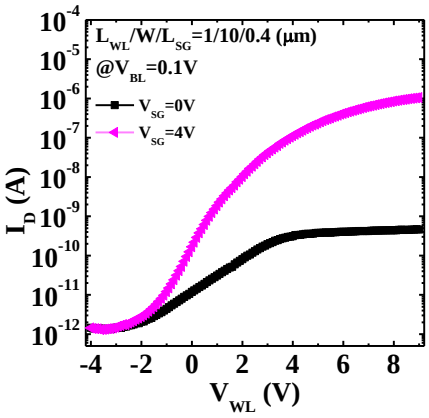


Fig. 3. 1 The I_D-V_G characteristics of WSG SONOS-type TFT memory with Nitride trapping layer on the different select gate voltage

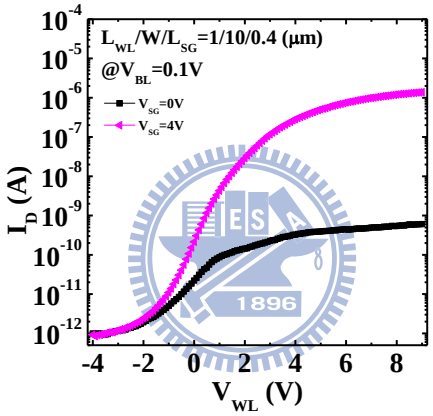


Fig. 3. 2 The I_D-V_G characteristics of WSG SONOS-type TFT memory with Nitride + Si dot trapping layer on the different select gate voltage

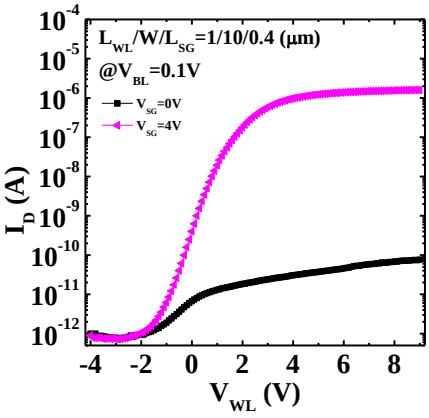


Fig. 3. 3 The I_D-V_G characteristics of WSG SONOS-type TFT memory with N^+ floating gate trapping layer on the different select gate voltage

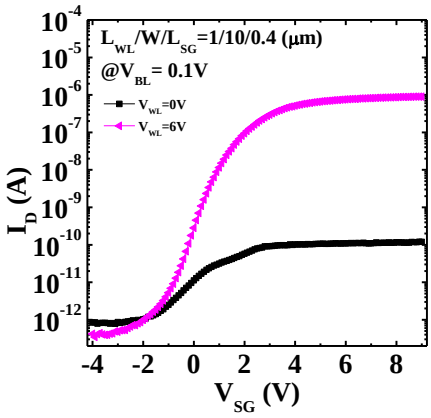


Fig. 3. 4 The I_D-V_{SG} characteristics of WSG SONOS-type TFT memory with Nitride trapping layer on the different select gate voltage

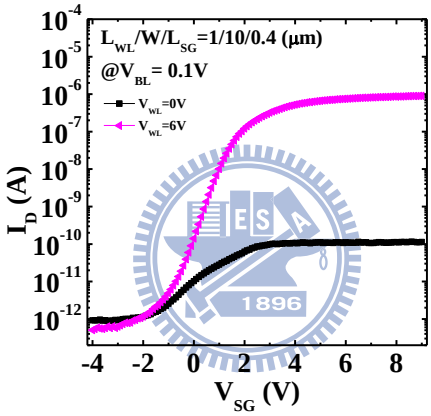


Fig. 3. 5 The I_D-V_{SG} characteristics of WSG SONOS-type TFT memory with Nitride + Si dot trapping layer on the different select gate voltage

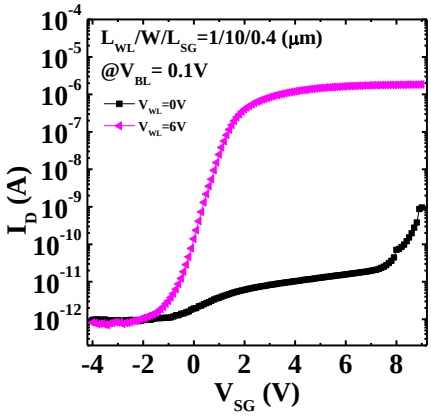


Fig. 3. 6 The I_D-V_{SG} characteristics of WSG SONOS-type TFT memory with N^+ floating gate trapping layer on the different select gate voltage

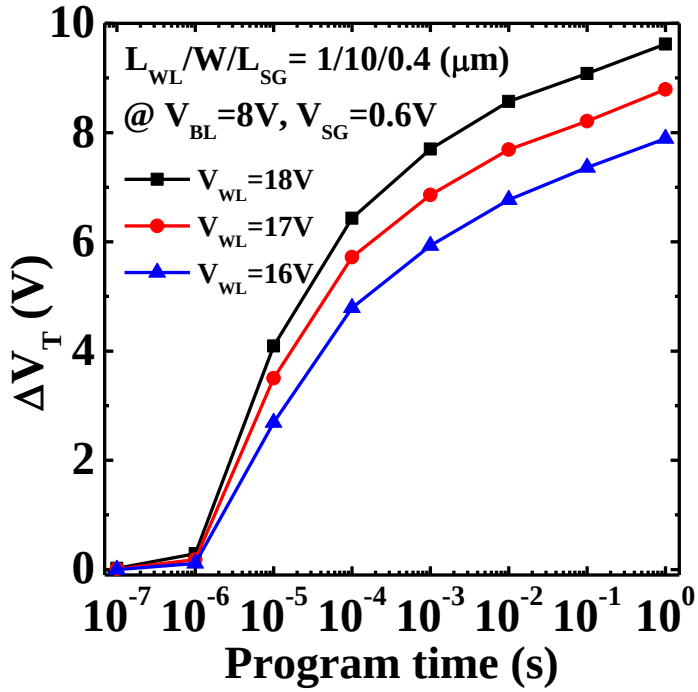


Fig. 3. 7 Program speed characteristics of WSG SONOS-type TFT memory with Nitride trapping layer on the various word line bias

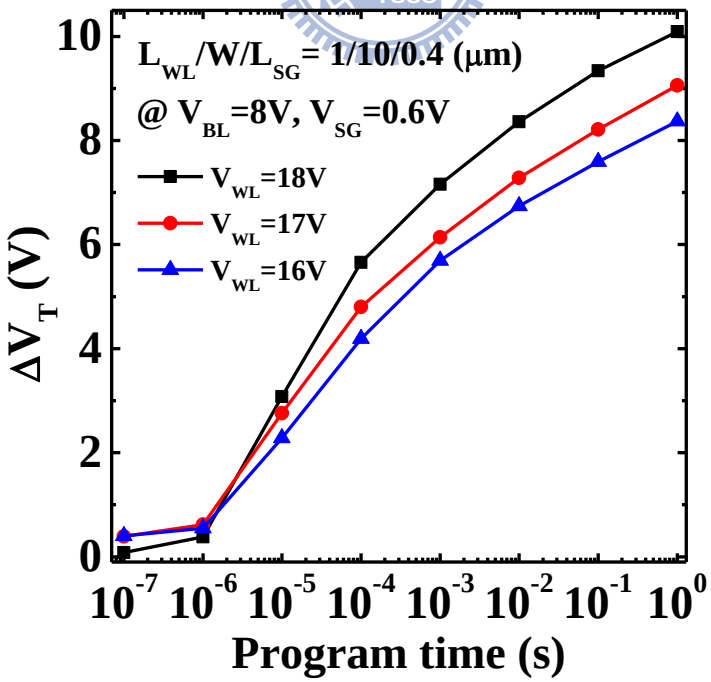


Fig. 3. 8 Program speed characteristics of WSG SONOS-type TFT memory with Nitride + Si dot trapping layer on the various word line bias

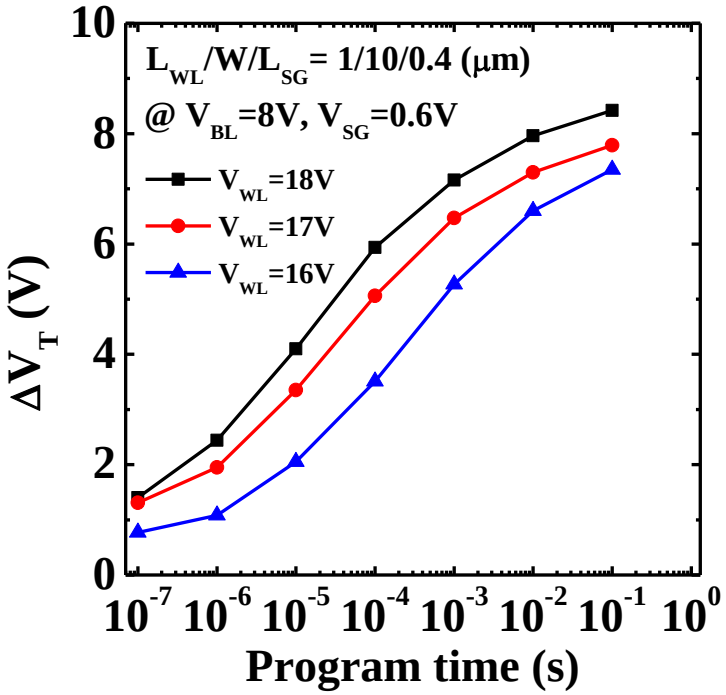


Fig. 3. 9 Program speed characteristics of WSG SONOS-type TFT memory with N^+ floating gate trapping layer on the various word line bias

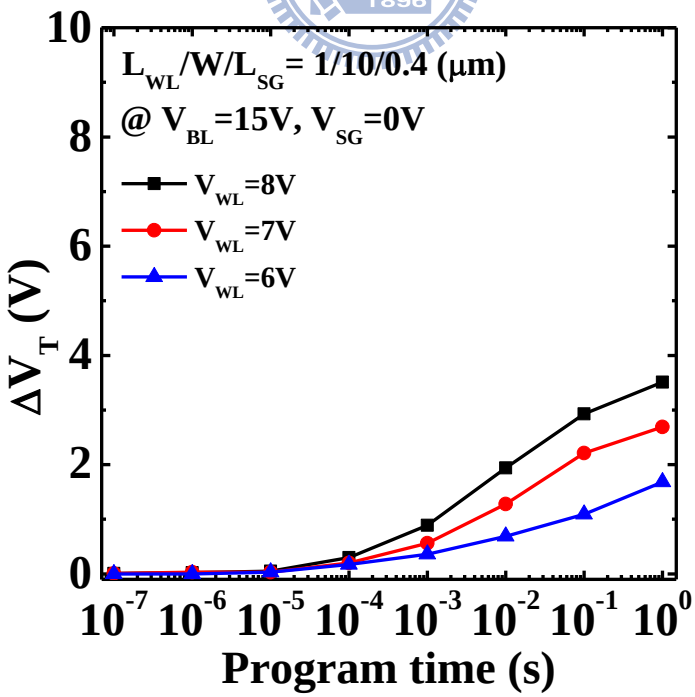


Fig. 3. 10 Program speed characteristics of WSG SONOS-type TFT memory Floating gate cell on the various word line bias exhibiting acceptable 2nd bit effect

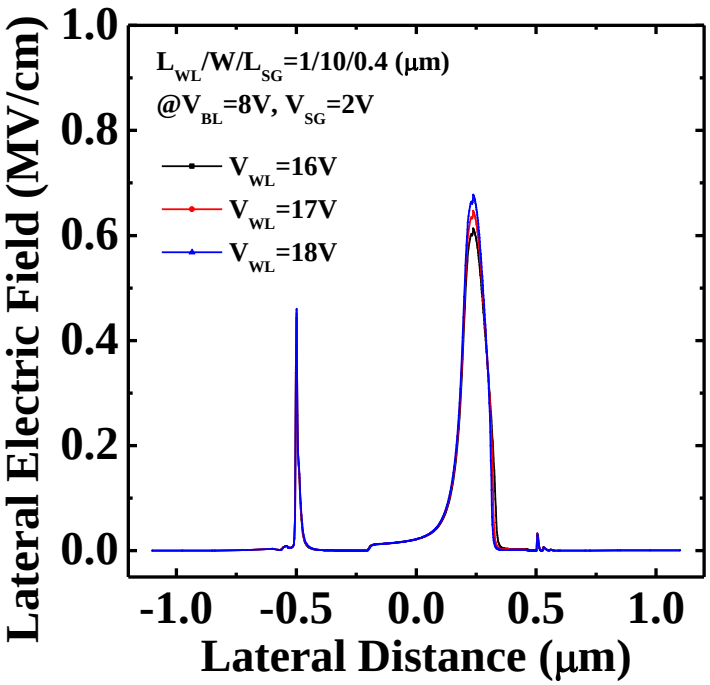


Fig. 3. 11 The simulated results of lateral electric field start from V_{WL}=16V to V_{WL}=18V in the channel of WSG SONOS TFT memory device

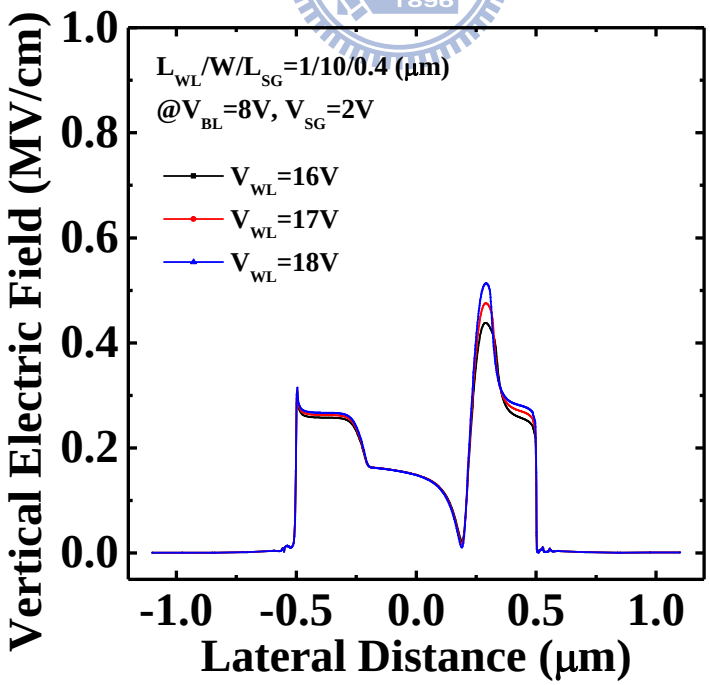


Fig. 3. 12 The simulated results of vertical electric field start from V_{WL}=16V to V_{WL}=18V in the channel of WSG SONOS TFT memory device

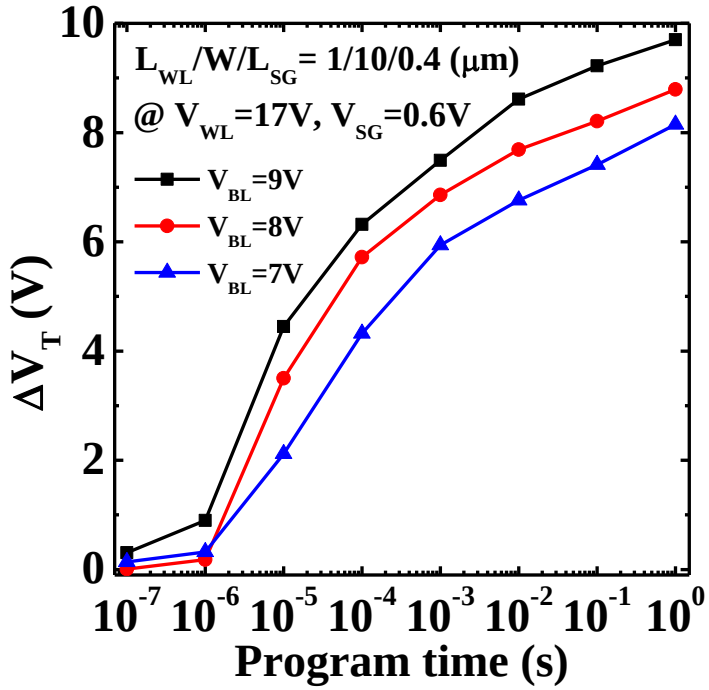


Fig. 3. 13 Program speed characteristics of WSG SONOS-type TFT memory with Nitride trapping layer on the various bit line bias

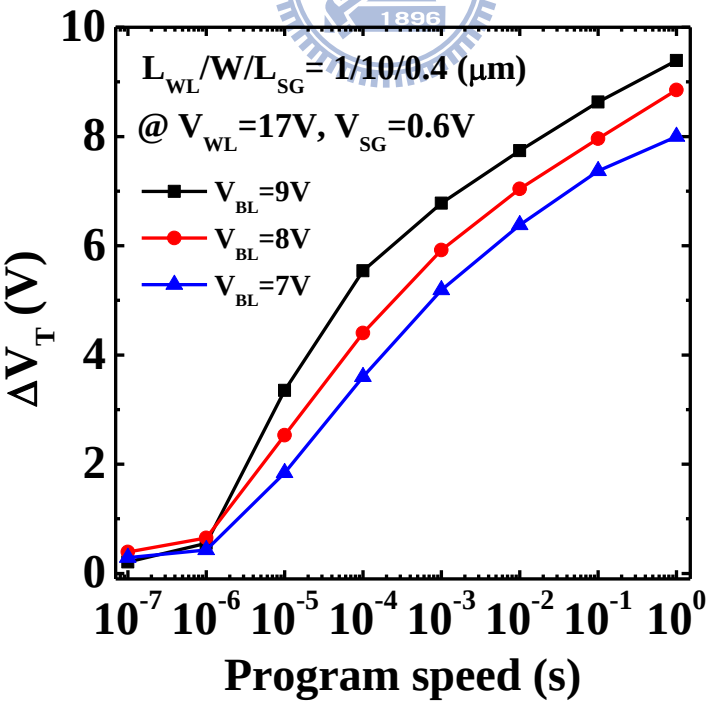


Fig. 3. 14 Program speed characteristics of WSG SONOS-type TFT memory with Nitride + Si dot trapping layer on the various bit line bias

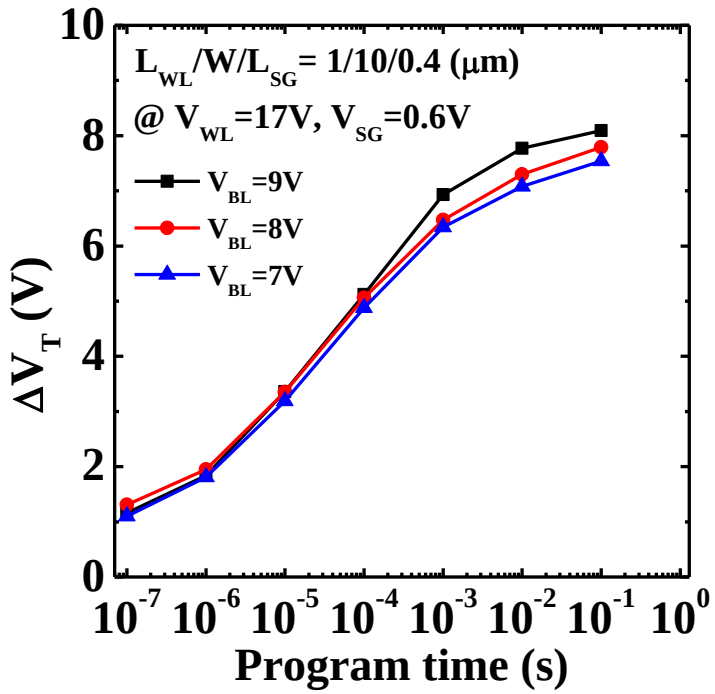


Fig. 3. 15 Program speed characteristics of WSG SONOS-type TFT memory with N^+ floating gate trapping layer on the various bit line bias

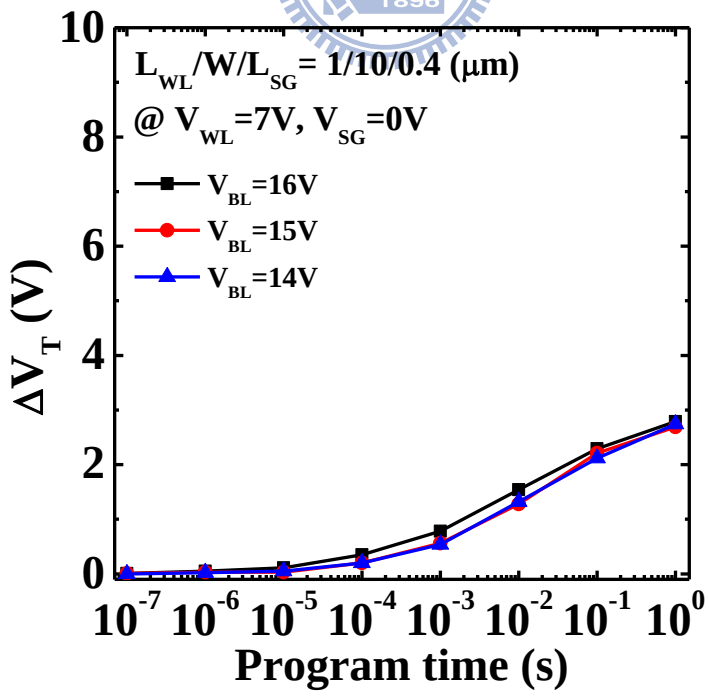


Fig. 3. 16 Program speed characteristics of WSG SONOS-type TFT memory Floating gate cell on the various bit line bias exhibiting acceptable 2nd bit effect

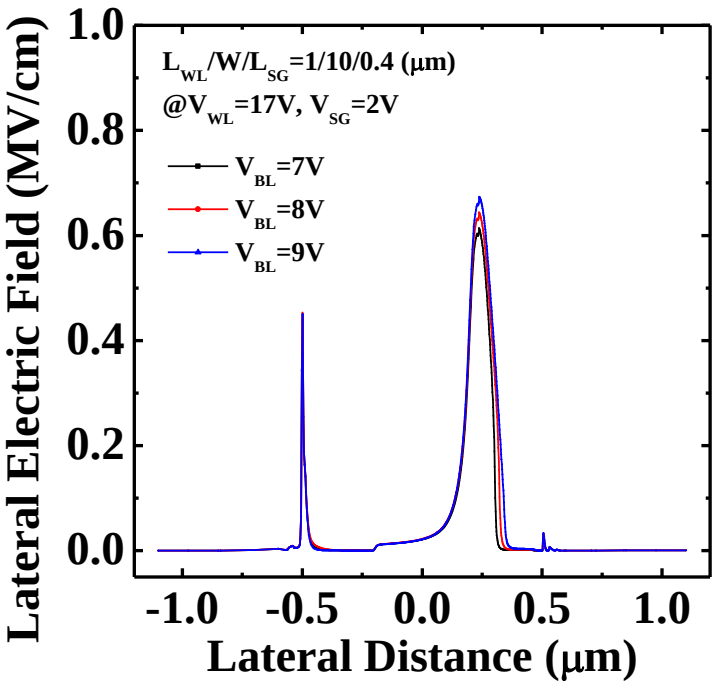


Fig. 3. 17 The simulated results of lateral electric field start from V_{BL}=7V to V_{BL}=9V in the channel of WSG SONOS TFT memory device

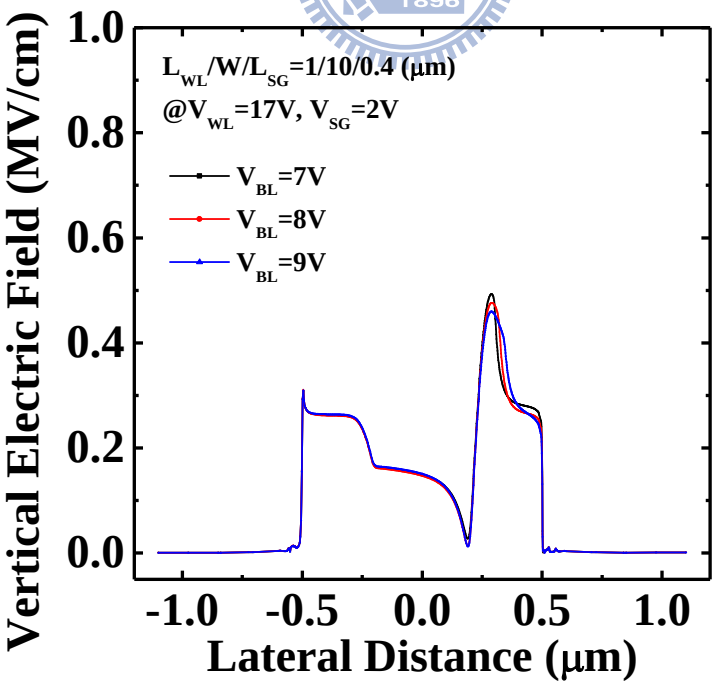


Fig. 3. 18 The simulated results of vertical electric field start from V_{BL}=7V to V_{BL}=9V in the channel of WSG SONOS TFT memory device

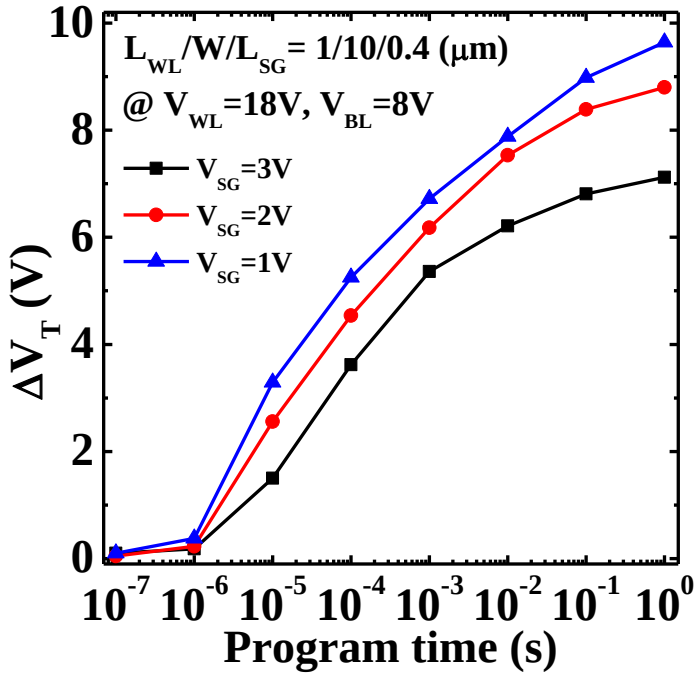


Fig. 3. 19 Program speed characteristics of WSG SONOS-type TFT memory with Nitride trapping layer on the large select gate bias

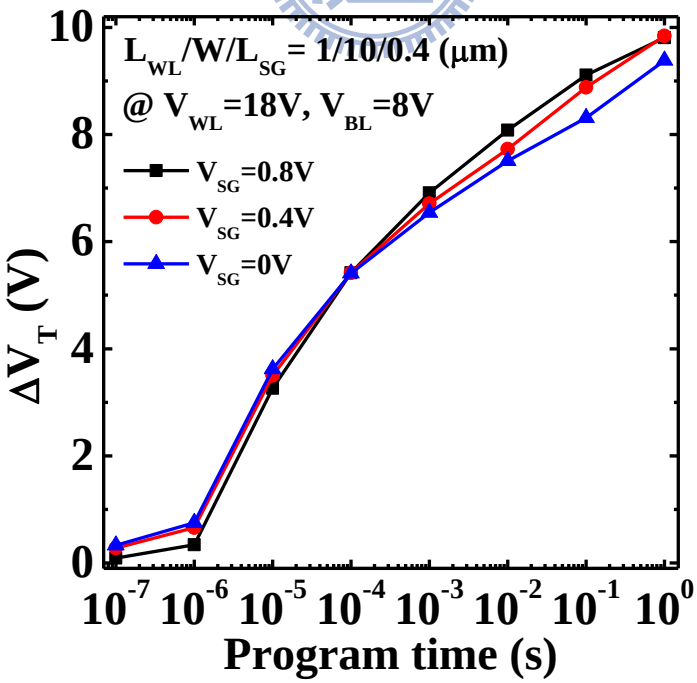


Fig. 3. 20 Program speed characteristics of WSG SONOS-type TFT memory with Nitride trapping layer on the small select gate bias

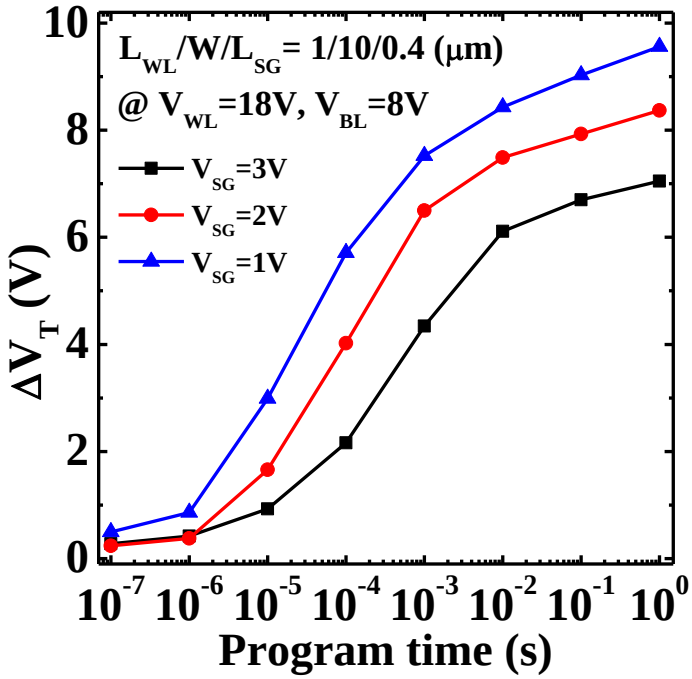


Fig. 3. 21 Program speed characteristics of WSG SONOS-type TFT memory with Nitride + Si dot trapping layer on the large select gate bias

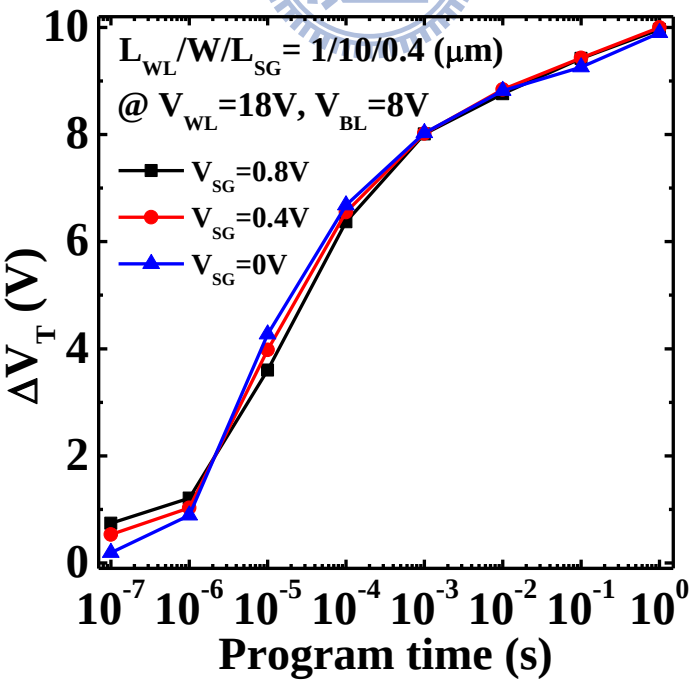


Fig. 3. 22 Program speed characteristics of WSG SONOS-type TFT memory with Nitride + Si dot trapping layer on the small select gate bias

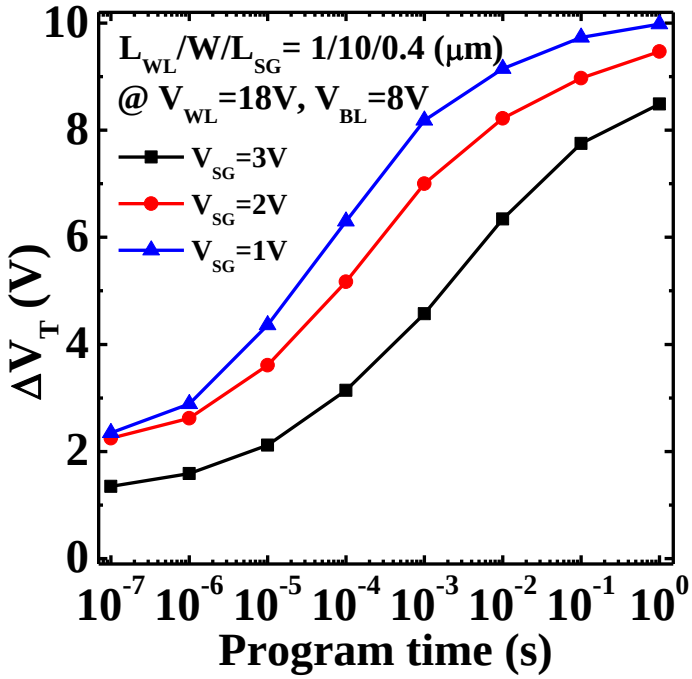


Fig. 3. 23 Program speed characteristics of WSG SONOS-type TFT memory with N^+ floating gate trapping layer on the large select gate bias

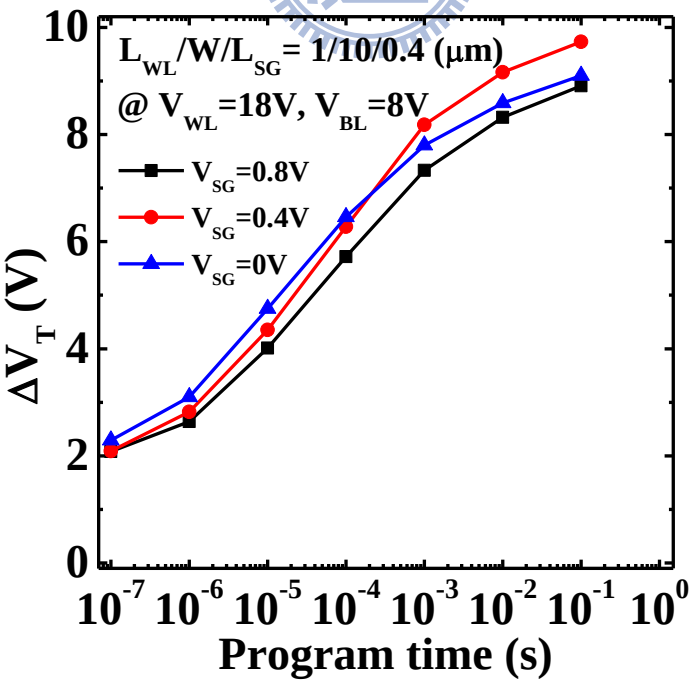


Fig. 3. 24 Program speed characteristics of WSG SONOS-type TFT memory with N^+ floating gate trapping layer on the small select gate bias

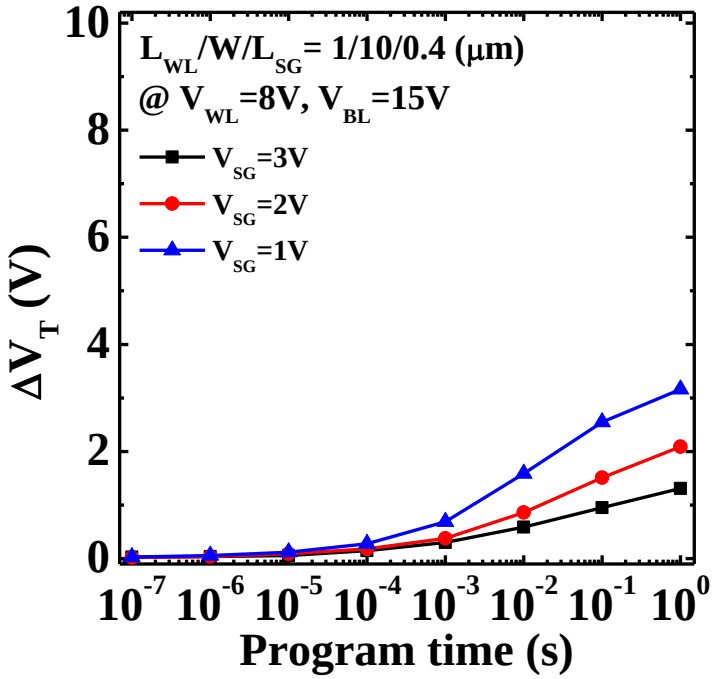


Fig. 3. 25 Program speed characteristics of WSG SONOS-type TFT memory Floating gate cell on the large select gate bias exhibiting acceptable 2nd bit effect

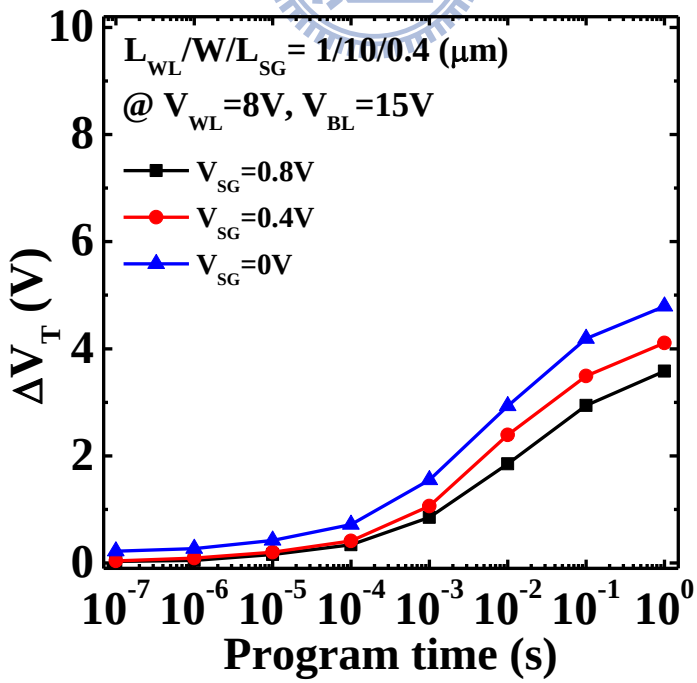


Fig. 3. 26 Program speed characteristics of WSG SONOS-type TFT memory Floating gate cell on the small select gate bias exhibiting acceptable 2nd bit effect

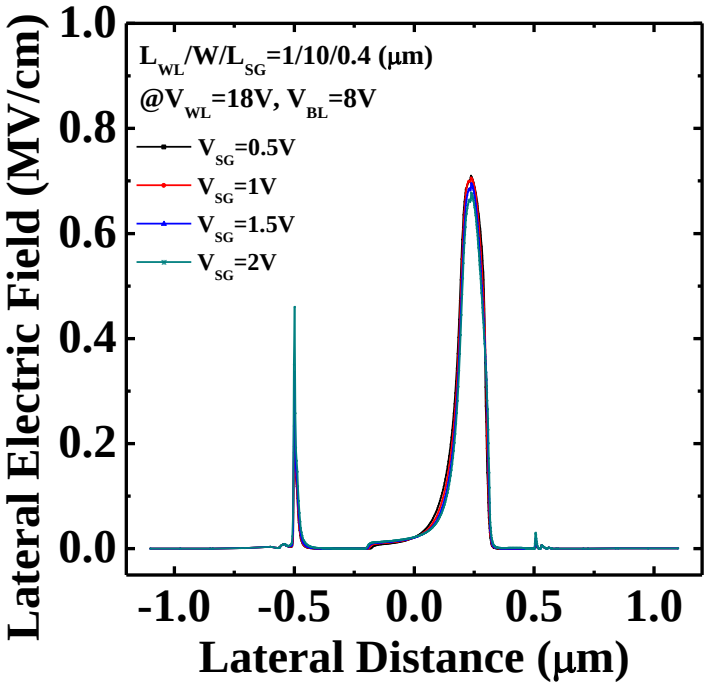


Fig. 3. 27 The simulated results of lateral electric field start from V_{SG}=0.5V to V_{SG}=2V in the channel of WSG SONOS TFT memory device

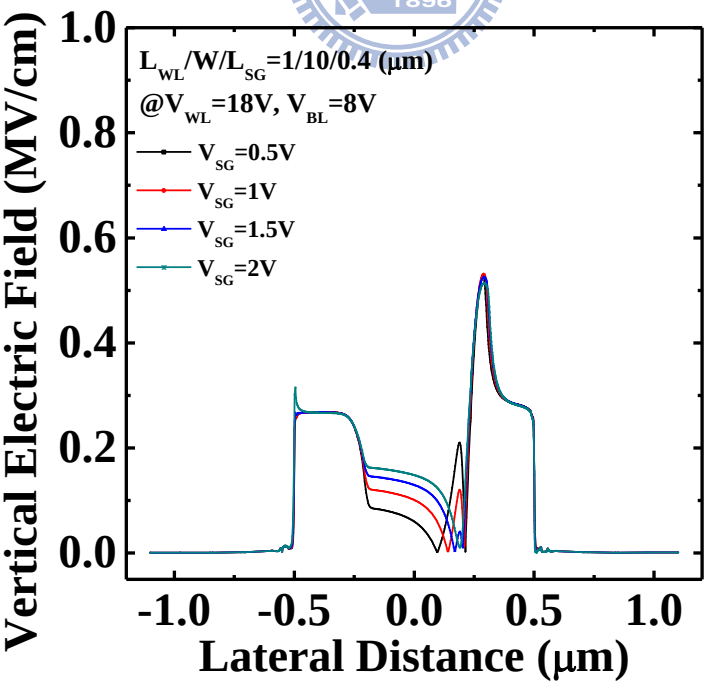


Fig. 3. 28 The simulated results of vertical electric field start from V_{SG}=0.5V to V_{SG}=2V in the channel of WSG SONOS TFT memory device

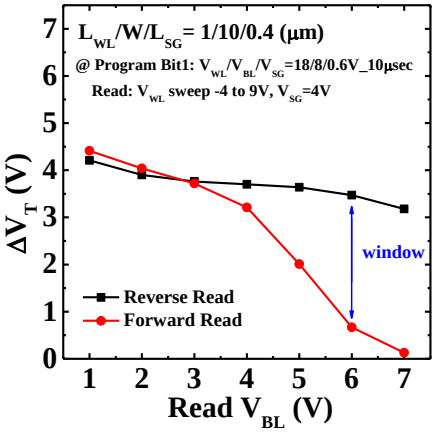


Fig. 3. 29 The schematic of 2nd bit effect of WSG TFT memory Nitride cell

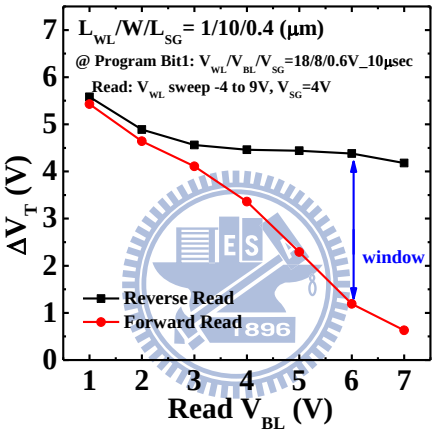


Fig. 3. 30 The schematic of 2nd bit effect of WSG TFT memory Nitride_Dot cell

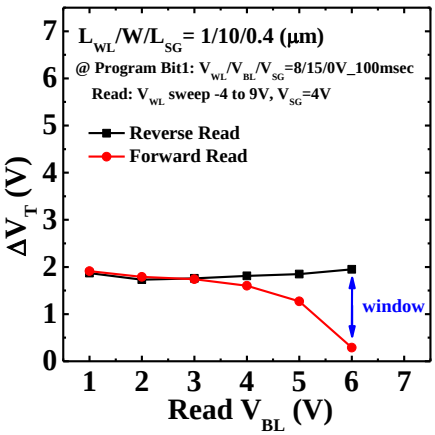


Fig. 3. 31 The schematic of 2nd bit effect of WSG TFT memory Floating gate cell

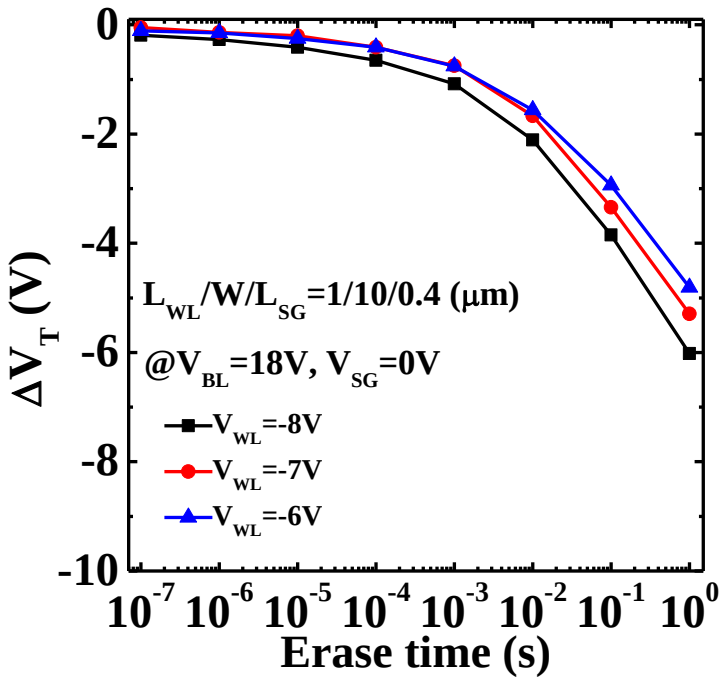


Fig. 3. 32 Erase speed characteristics of WSG SONOS-type TFT memory with Nitride trapping layer on the various word line bias

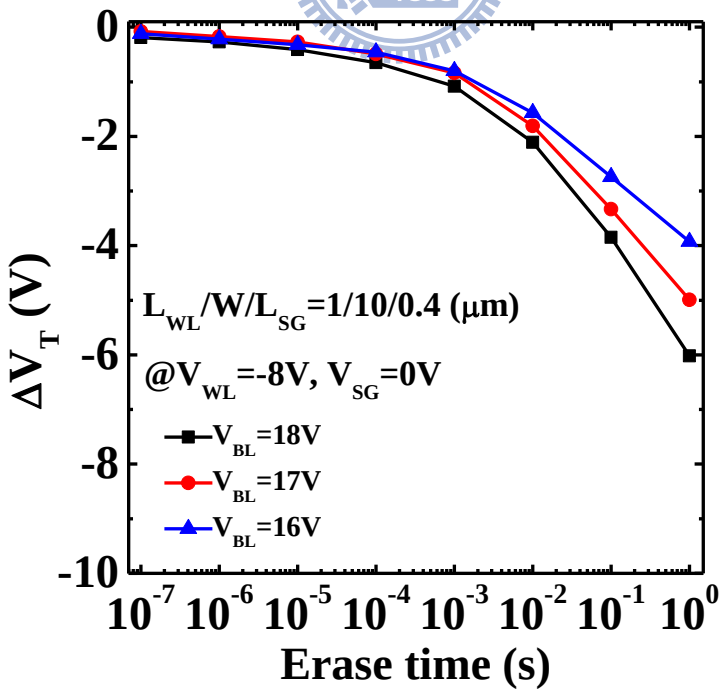


Fig. 3. 33 Erase speed characteristics of WSG SONOS-type TFT memory with Nitride trapping layer on the various bit line bias

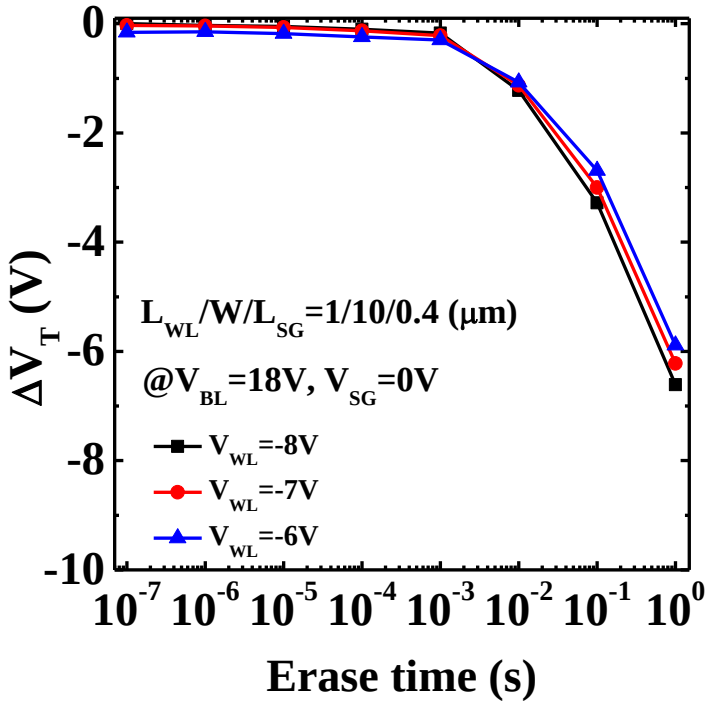


Fig. 3. 34 Erase speed characteristics of WSG SONOS-type TFT memory with Nitride + Si dot trapping layer on the various word line bias

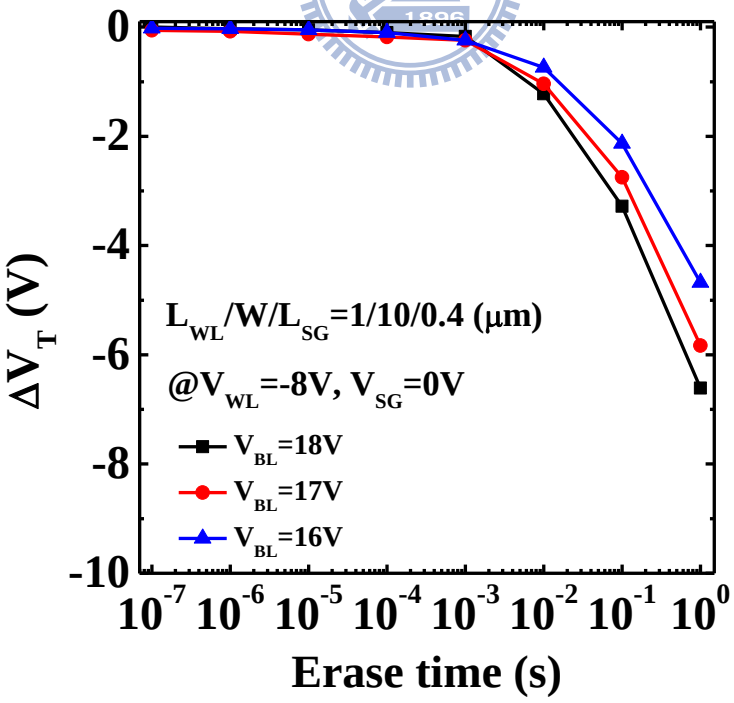


Fig. 3. 35 Erase speed characteristics of WSG SONOS-type TFT memory with Nitride + Si dot trapping layer on the various bit line bias

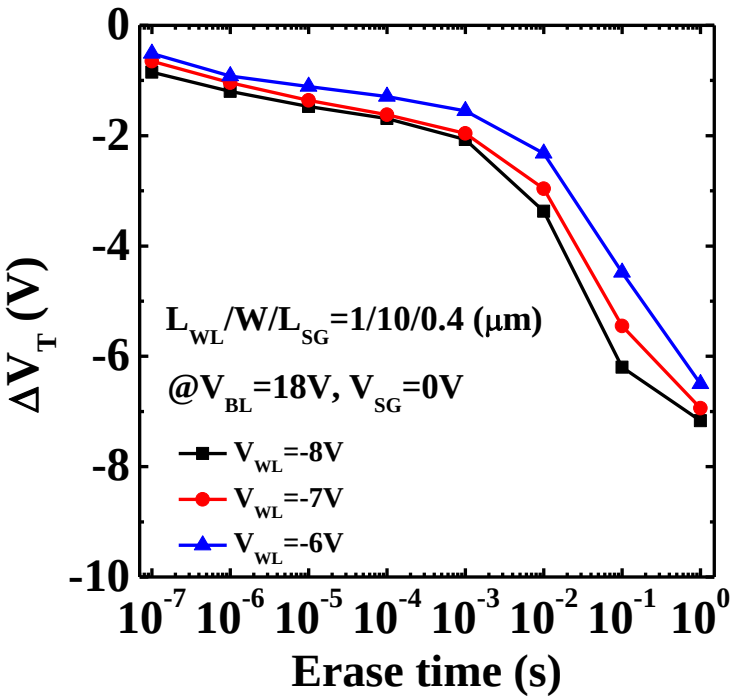


Fig. 3. 36 Erase speed characteristics of WSG SONOS-type TFT memory with N^+ floating gate trapping layer on the various word line bias

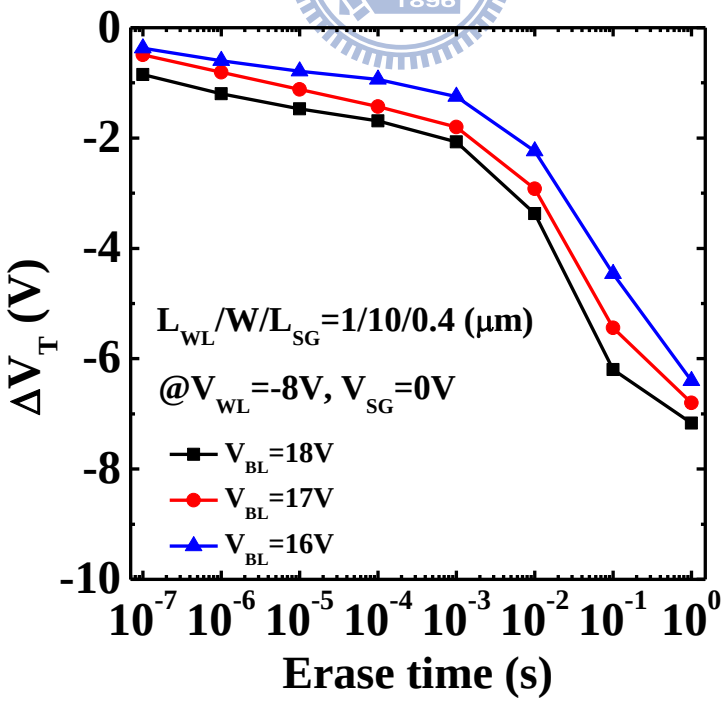


Fig. 3. 37 Erase speed characteristics of WSG SONOS-type TFT memory with N^+ floating gate trapping layer on the various bit line bias

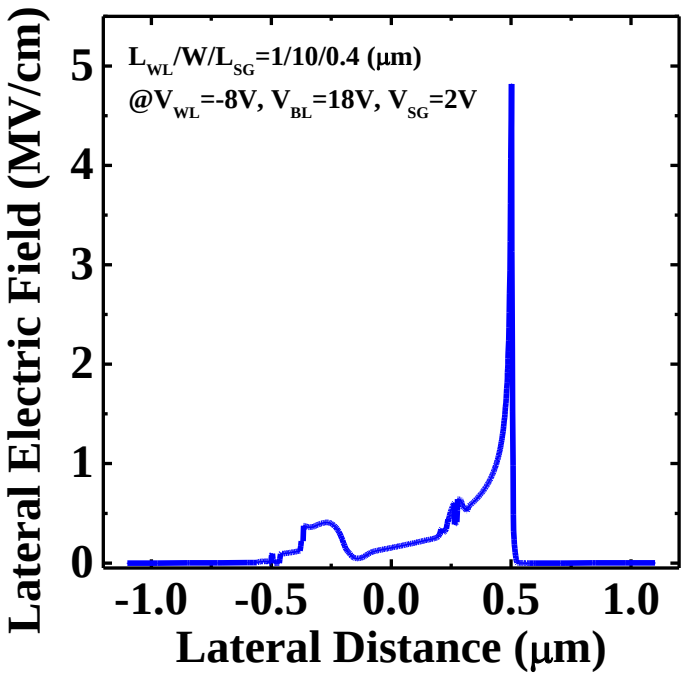


Fig. 3. 38 The simulated results of lateral electric field with bias V_{WL}=-8V, V_{BL}=18V, and V_{SG}=2V in the channel of WSG SONOS TFT memory device

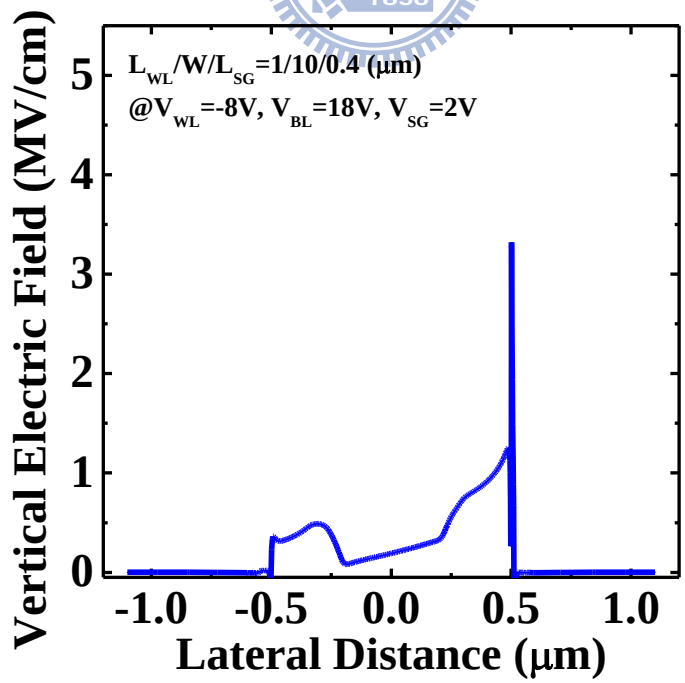


Fig. 3. 39 The simulated results of vertical electric field with bias V_{WL}=-8V, V_{BL}=18V, and V_{SG}=2V in the channel of WSG SONOS TFT memory device

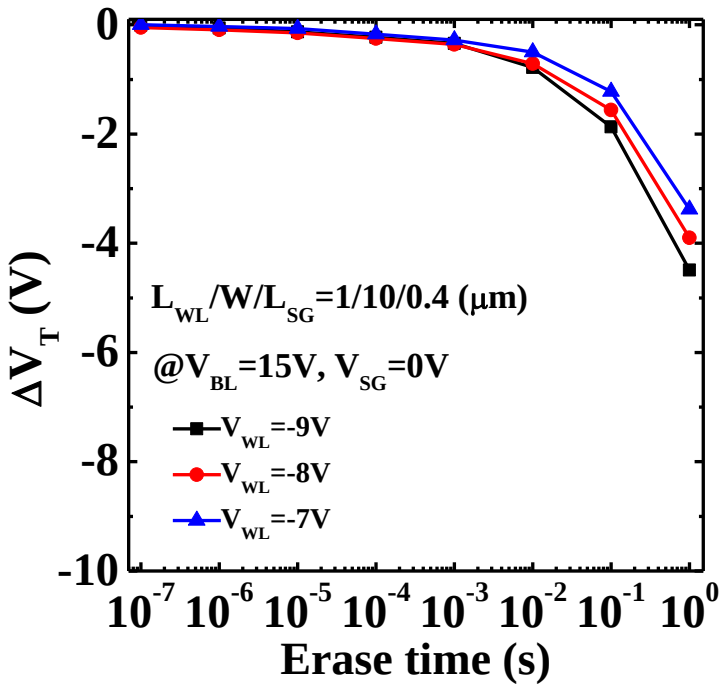


Fig. 3. 40 Erase speed characteristics of WSG SONOS-type TFT memory Floating gate cell on the various word line bias exhibiting acceptable 2nd bit effect

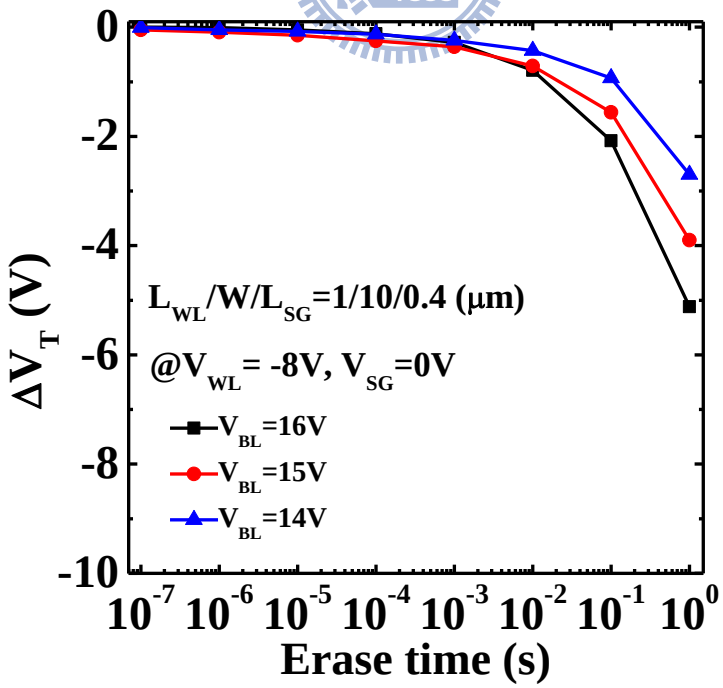


Fig. 3. 41 Erase speed characteristics of WSG SONOS-type TFT memory Floating gate cell on the various bit line bias exhibiting acceptable 2nd bit effect

Operation	$V_{WL}/V_{BL}/V_{SG}$	Cell	Speed	2^{nd} Bit Effect	Endurance
Program	18/8/0.6V Source Side Injection	Nitride	O	O	O
		Nitride_Dot	O	O	O
		Floating gate	O	×	×
	8/15/0V Junction Breakdown	Floating gate	Δ	Δ (2V window)	O
Erase	-8/18/0V BTBTHH + Junction Breakdown	Nitride	O	O	O
		Nitride_Dot	O	O	O
		Floating gate	O	×	×
	-8/15/0V BTBTHH + Junction Breakdown	Floating gate	Δ	Δ (2V window)	O

Table 3. 1 Comparison sheet of operation bias of WSG SONOS-type TFT memory

Chapter 4

Reliabilities of WSG-SONOS-type TFT memory

4.1 Introduction

Besides struggling for better performance characteristics of memory device, the reliabilities of memory device are still concern issues as scaling down. The most frequently mentioned reliabilities include gate disturbance, drain disturbance, data retention, and P/E endurance [4.1]-[4.3]. The scaling down of conventional floating gate memory devices has met limitations beyond 60-nm node technology. Further scaling of tunneling oxide below 7nm may face challenges including stress induced leakage current (SILC), short channel effect, floating gate coupling effect, and drain-induced turn on effect, etc. [4.4]-[4.6]. Storing charges in discrete trapping sites layer can offer us an excellent immunity to above serious problem. Moreover, we can have two bit operation and better data retention characteristics. When we apply program or erase operation in a memory array, the neighboring un-selected cell may suffer word-line disturb or bit-line disturb. Hence, in this chapter, we will discuss disturbance phenomena, P/E cycle endurance, and date retention at different temperature values in detail.

4.2 Results and Discussions

We have discussed the program and erase mechanism in detail in previous chapter. According to the results of discussions before, Wrapped-Select-Gate structure memory cells exhibit fast program speed and erase speed. However, disturbance phenomena always happen in memory array operation. In order to make an

investigation of word line disturb and bit line disturb, Nitride-based (Nitride) cells, Nitride with Si dot (Nitride_Dot) cells, and N^+ floating gate (Floating gate) cells are programmed to memory window of 3V, 3V, 2V, respectively. First of all, Fig. 4.1 shows word line disturbance characteristics of a Nitride cell with stress bias, 16V, 17V, and 18V. The normalized window axis means the remaining window over initial window after a period of stress time. We find that all three positive word line biases give rise to charge loss by gate leakage. Trapped electrons tunnel to word line gate away from channel and then amount of negative threshold voltage shift (0.33V) is observed in long disturb time. On the other hand, bit line disturb biases are applied to Nitride cell, as shown in Fig. 4.2. Trapped electrons tunneling through bottom oxide result in much severer charge loss problem in disturb test. The worst case is that about 0.7V threshold voltage shift under 18V bit line stress bias.

Similarly, two kinds of disturb bias are applied to Nitride_Dot cells, as shown in Fig. 4.3 and Fig. 4.4. The results different to those of Nitride cells are word line disturb phenomena. Nitride_Dot cells seem to have severer word line disturb problem than Nitride cells because of the existence of Si nanocrystals in trapping layer. Under overall positive word line bias, electrons trapped in Si nanocrystals may accumulate on the upper side and have larger chance to tunnel through blocking oxide compared to bulk nitride trap. As for bit line disturb of Nitride_Dot cells, regardless of thinner tunneling oxide layer, because only partial trapping region are directly affected by V_{BL}, charge loss slightly decrease when lower bit line voltage is applied.

Fig. 4.5 shows the word line disturb phenomena of Floating gate cells. Due to smaller operation biases of Floating gate cells, memory states are almost unaffected until long stress period time. Unlike to previous discussions, floating gate coupling in word line disturb test causes electron trapping. Electrons of N^+ source/drain region go

to floating gate by Fowler-Nordheim tunneling mechanism and then raise the threshold voltage of device. It is worth to note that V_{WL}=6V is not enough to make electron tunneling happen. Therefore, the normalized window remains constant even longest stress time is reached. Because of inferior trapping capability, however, Floating gate cells still have comparable charge loss with lower bit line voltage in disturbance test, as shown in Fig. 4.6.

In order to achieve two-bit or multi-bit operation, hot electron injection and band-to-band tunneling induced hot hole erase have been widely used for a long time. However, endurance and retention are still two concerns related to repeat P/E stress [4.2]. Memory window closure with program/erase cycling especially in thin film transistor memory devices is a serious reliability concern in novel discrete charge trapping devices. Window closure is believed to arise from build-up of permanent excess electrons trapped in ONO stack and defect generation [4.7]. Fig. 4.7 shows the endurance characteristic of a Nitride cell. The trend of window narrowing is observed due to increasing V_T of erase state and, at the same time, decreasing V_T of program state. When cycling times is rising, more and more defects are generated in channel grain boundaries and TEOS oxide interface. The other reason may be attributed to long channel length. Accumulated electron in trapping layer didn't recombine with hot holes which results in programming efficiency lowering. In the meanwhile, excess holes are ejected to the overlap region between word line gate and drain. Once these holes didn't recombine with trapped electrons, they have limited capability of reducing threshold voltage of memory device. That is why 3.5V window is left to be less than half of initial window after 10k times P/E cycling. Although bit 1 underwent repeated P/E stress, we can find that these operations of bit 1 completely do not carry

any influence on bit 2 state. In other words, wrapped-select-gate structure memory device has excellent immunity to second bit effect.

Fig. 4.8 shows the endurance characteristic of a Nitride_Dot cell. Under the same bias condition, Nitride_Dot cell have larger initial memory window. However, as cycling time increases, the threshold voltage of program state and erase state become closer to each other. This phenomenon can be attributed to the poor quality of TEOS tunneling oxide and mismatch of electrons and holes. More and more charges pile up in tunneling oxide and trapping layer which hinders P/E operation. As mentioned before, we can observe that only about 1.6V memory window is left over after 10k P/E cycling times. There also have no interference between bit1 state and bit2 state in endurance test. That is to say, in wrapped-select-gate structure Nitride_Dot cell, it shows great potential in multi-bit operation because of outstanding immunity to 2^{nd} bit effect.

We can see the endurance characteristics of wrapped-select-gate structure Floating gate cell in Fig. 4.9. Unlike to Nitride cell and Nitride_Dot cell, Floating gate cell have no charge mismatch problem that suppress the happening of window closure. However, poor quality of TEOS tunneling oxide still brings influence on defect generation and interface state issue. We find that both threshold voltage of program state and erase state keep on a rise as cycling times increases. Owing to the lack of ability to stop charges moving from bit 1 to bit 2 in program state, we can observe that when bit1 is programmed, bit2 state V_T has large range of variation.

In order to study the impact of different electron injection location by SSI and conventional channel hot electron (CHE) Injection, endurance test was also performed with V_{WL}=12V, V_{BL}=12V, and V_{SG}=0V programming bias in Nitride_Dot cell, as shown in Fig. 4.10. More serious window closure problem occurs because of repeated

tunneling by hot electrons during programming and hot holes during erase in the same place. This operation process may cause much more defects generated near the overlap region of word-line gate and drain region. Fig 4.11 and Fig. 4.12 again demonstrate the electron injection location of CHE is near the drain side. Because we have major electric field both laterally and vertically near the drain region.

The other serious concern is long-tern retention of cycled charge trapping device. First of all, Fig. 4.13 shows data retention characteristics of 1 cycled WSG SONOS-type TFT memory device Nitride cell with various temperatures, 25^{o}C, 55^{o}C, and 85^{o}C. Due to a lot of original defects in TEOS tunneling oxide, long-term 85^{o}C retention case has more than 20% charge loss in Nitride cell of 3V window. However, 10k cycled Nitride cell exhibits worse data retention characteristics in all three temperature cases, as shown in Fig. 4.14. The degraded retention characteristic refers to accumulated oxide damage from P/E cycling.

Despite high temperature and oxide defects enhance the opportunity of charge detrapping, Nitride_Dot cell still shows better retention characteristics in both 1 cycle and 10k cycled case, as shown in Fig. 4.15 and Fig. 4.16. All of these improvements may be attributed to deeper trap state of Si nanocrystal. Charges trapped in Si nanocrystal rather than bulk nitride native trap have less chances to tunnel out, especially in long-term data retention measurement. However, there one thing we might need to note is that electron injection location has great influence on retention characteristics of cycled devices. Repeat P/E operation in the same region (CHE/Drain Avalanche Hot Carrier program and BTBTHH erase) generates excess defects in tunneling dielectric which causes extra charge loss in high temperature retention measurement.

Fig. 4.17 shows data retention characteristics of 1 cycled WSG SONOS-type TFT memory device N^+ floating gate with cell various temperatures. Inferior to charge trapping devices in data retention characteristics, the existence of defect offer a tunneling path of charge and high temperature may speed up the velocity of charge loss. All charges in floating gate can move to the easiest tunneling path, however, charges in charge trapping device cannot move randomly. For 1 cycled Floating gate cell with 2V memory window, long-term 85^{o}C retention case has more than 40% charge loss. This phenomenon reminds us it is very important to control the quality of tunneling oxide for floating gate memory device. As for 10k cycled Floating gate cell, as shown in Fig. 4.18, it is an extremely tough mission to keep charges staying in floating gate device with excess defects and oxide damage. Both short-term and long-term retention suffer serious charge loss problem.

4.3 Summary

In this chapter, we discuss the characteristics of word line disturb, bit line disturb, P/E cycle endurance, and date retention. We observe that Nitride cell has better word line disturb performance than Nitride_Dot cell. Floating gate cell has no gate leakage issue in word line disturb due to floating gate coupling phenomenon. Regarding bit line disturb performance, Nitride_Dot cell shows better performance than Nitride cell under the same stress bias.

On the performance of endurance test, Nitride cell and Nitride_Dot cell have comparable characteristics. Both of them suffer from electron/hole mismatch problem which results in obvious window closure phenomena. Because of the absence of the disadvantage charge trapping device, charges can move around in floating gate. So no window closure problem is observed in endurance measurement of Floating gate cell.

In the last part of this chapter is the discussion about data retention characteristics. All three types of memory device has serious charge loss problem due to poor quality of TEOS tunneling oxide. Nevertheless, Nitride_Dot cells still exhibit the greatest performance of date retention characteristic among three types of devices. Compared to 10k-cycled Nitride cell, 10k-cycled Nitride_Dot cell has 6-8% improvement on high temperature retention measurement.

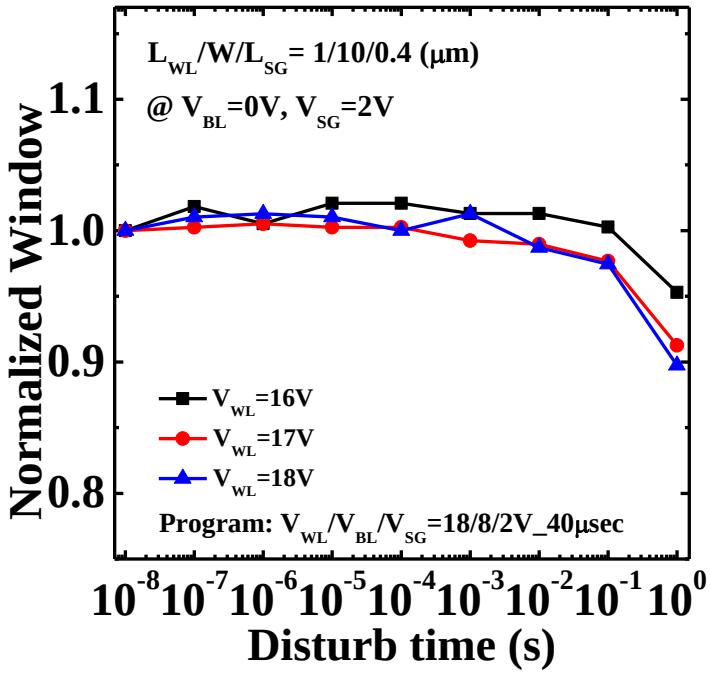


Fig. 4. 1 Word line disturbance characteristics of WSG SONOS-type TFT memory with Nitride trapping layer on the various stress bias

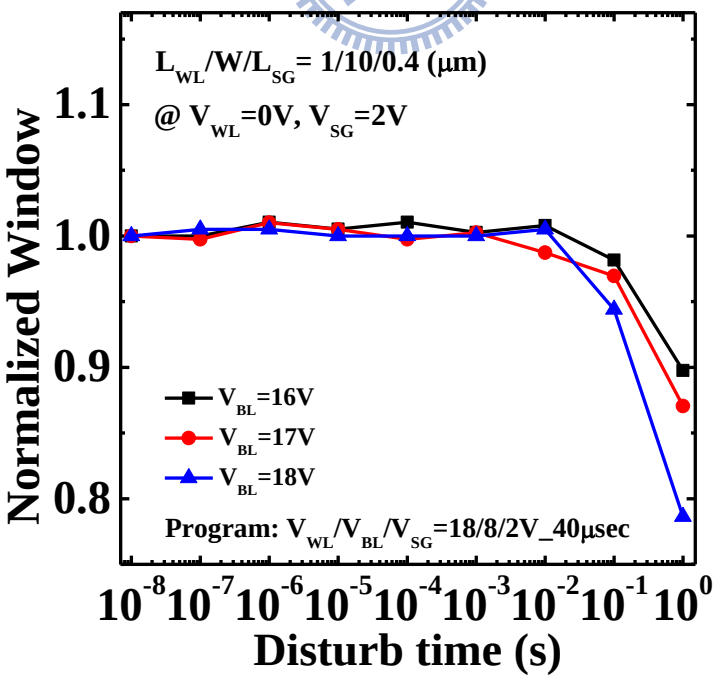


Fig. 4. 2 Bit line disturbance characteristics of WSG SONOS-type TFT memory with Nitride trapping layer on the various stress bias

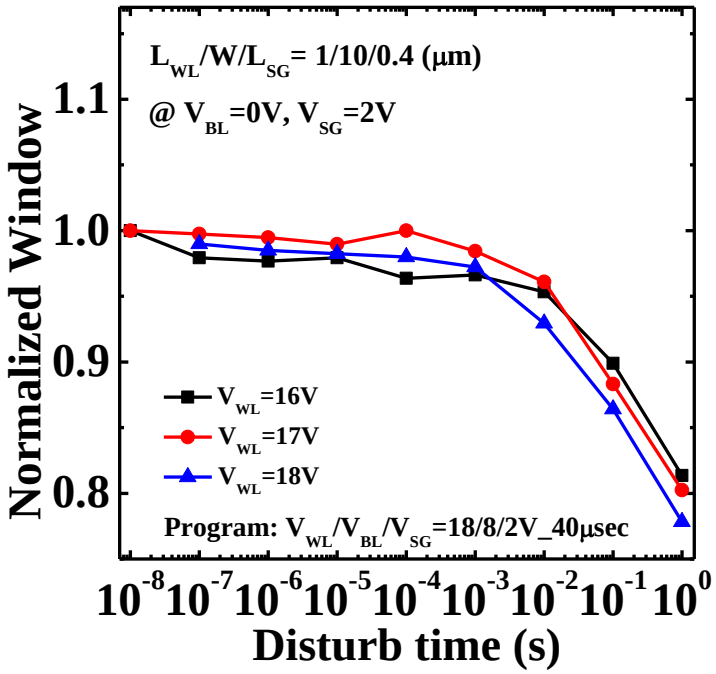


Fig. 4. 3 Word line disturbance characteristics of WSG SONOS-type TFT memory with Nitride + Si dot trapping layer on the various stress bias

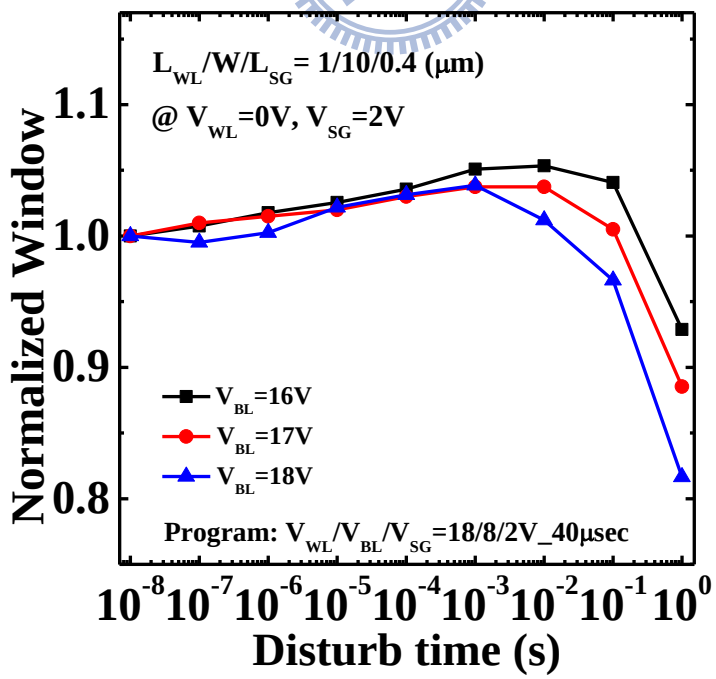


Fig. 4. 4 Bit line disturbance characteristics of WSG SONOS-type TFT memory with Nitride + Si dot trapping layer on the various stress bias

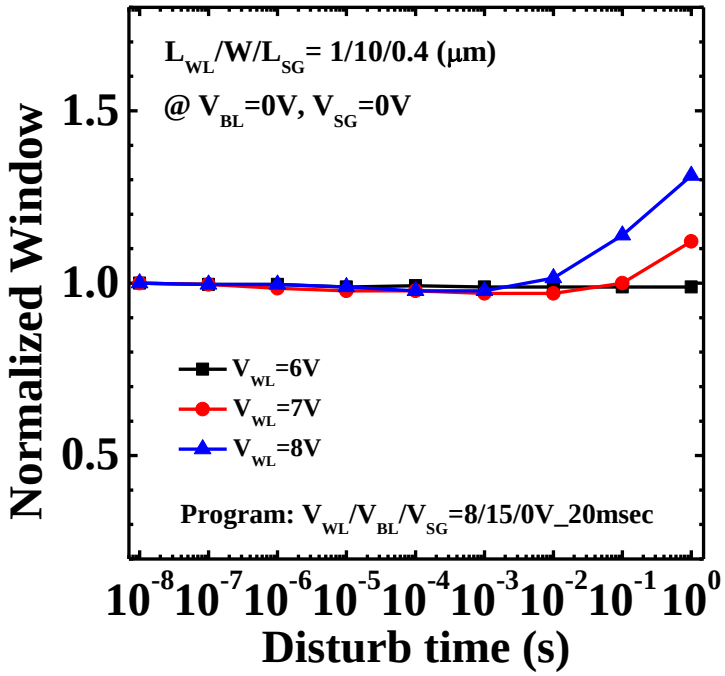


Fig. 4. 5 Word line disturbance characteristics of WSG SONOS-type TFT memory with N^+ floating gate trapping layer on the various stress bias

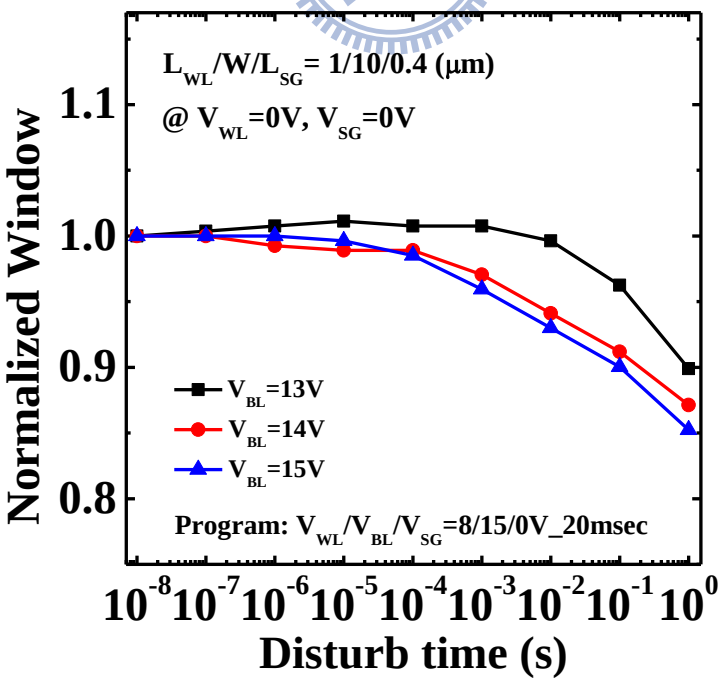


Fig. 4. 6 Bit line disturbance characteristics of WSG SONOS-type TFT memory with N^+ floating gate trapping layer on the various stress bias

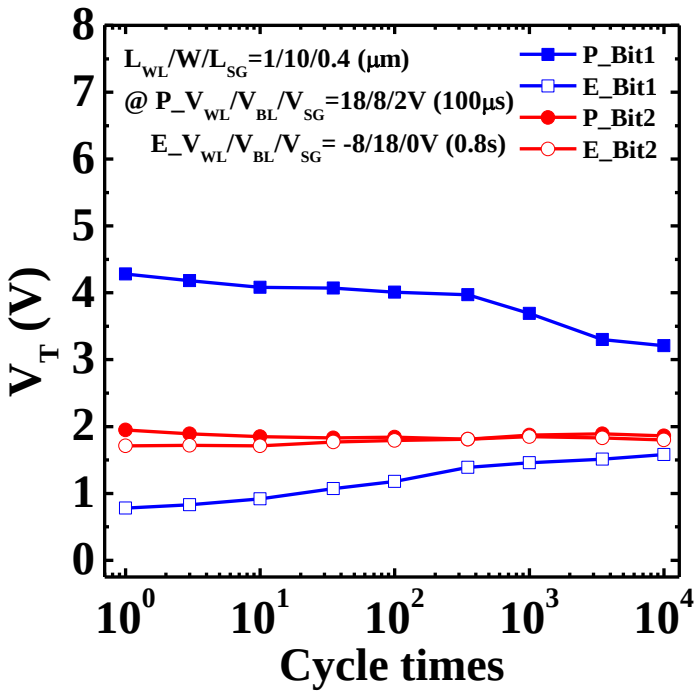


Fig. 4. 7 Endurance characteristics of WSG SONOS-type TFT memory with Nitride trapping layer

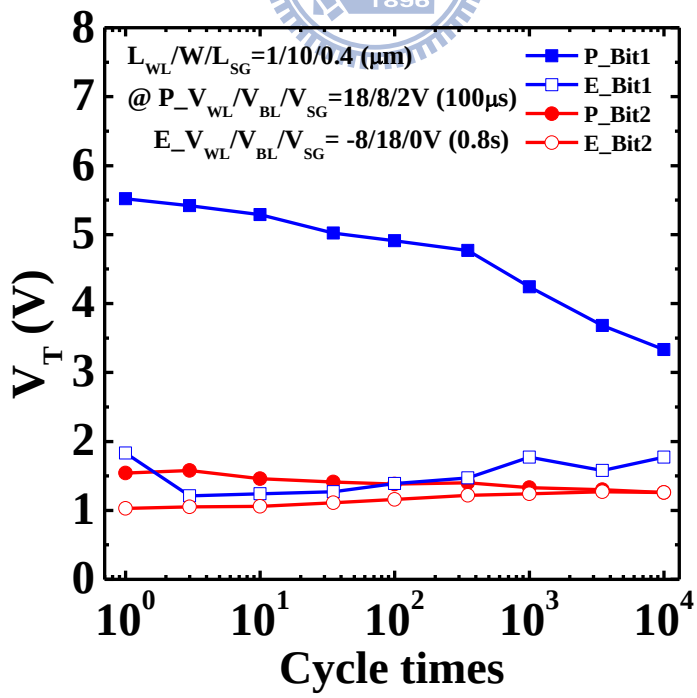


Fig. 4. 8 Endurance characteristics of WSG SONOS-type TFT memory with Nitride + Si dot trapping layer

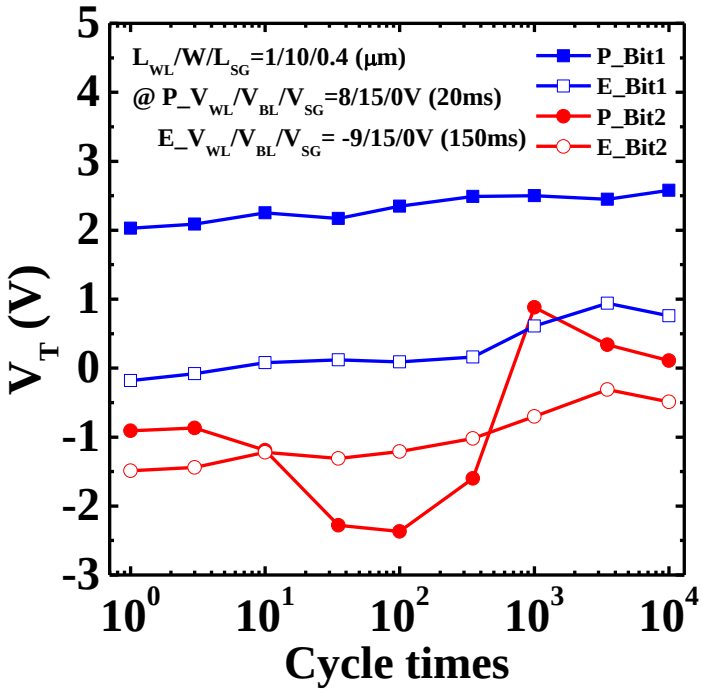


Fig. 4. 9 Endurance characteristics of WSG SONOS-type TFT memory with N^+ floating gate trapping layer

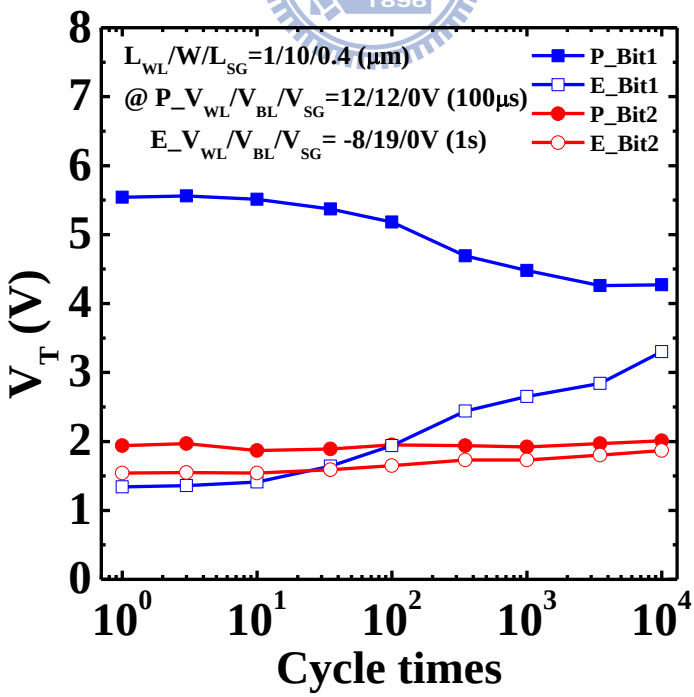


Fig. 4. 10 Endurance characteristics of WSG SONOS-type TFT memory with Nitride + Si dot trapping layer by CHE/DAHC injection

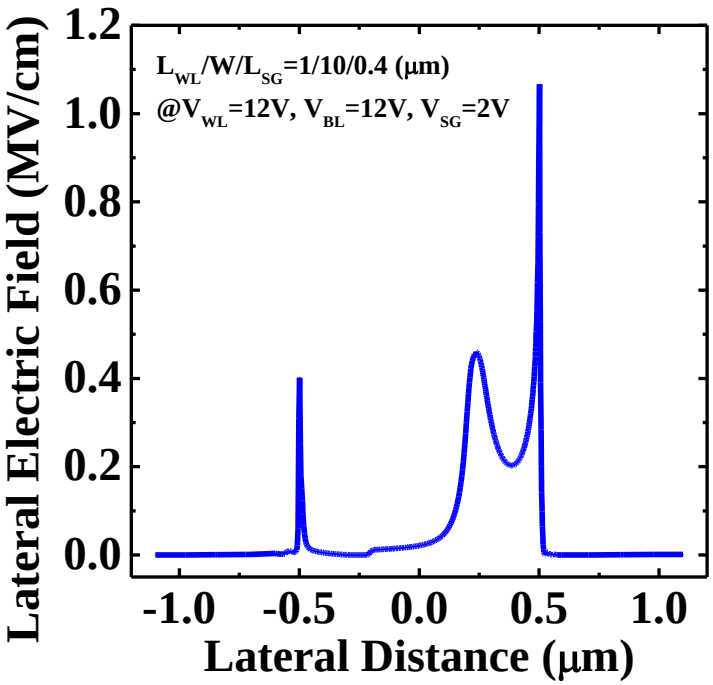


Fig. 4. 11 The simulated results of lateral electric field with bias V_{WL}=12V, V_{BL}=12V, and V_{SG}=2V in the channel of WSG SONOS TFT memory device

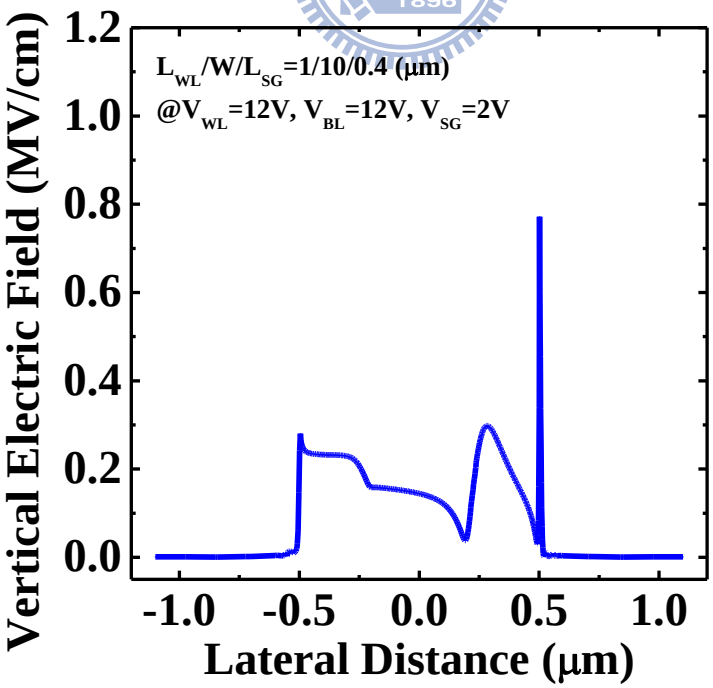


Fig. 4. 12 The simulated results of vertical electric field with bias V_{WL}=12V, V_{BL}=12V, and V_{SG}=2V in the channel of WSG SONOS TFT memory device

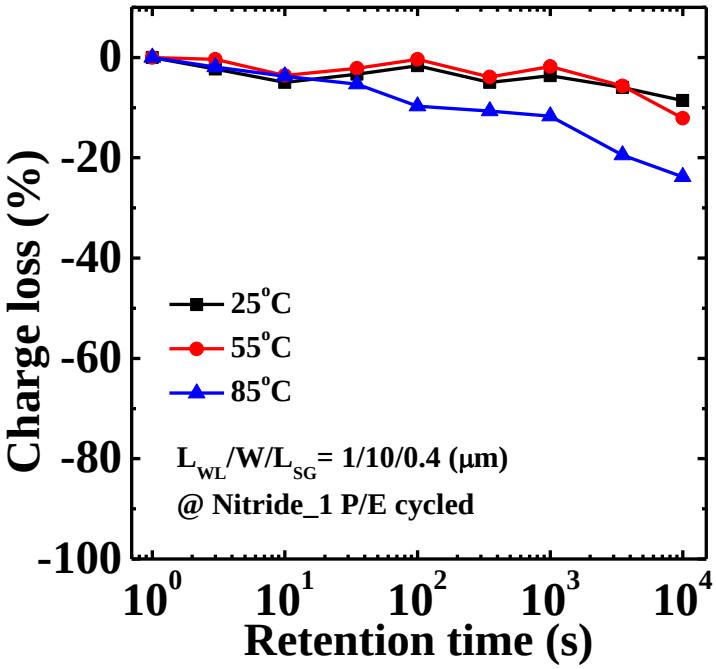


Fig. 4. 13 Data retention characteristics of 1 cycled WSG SONOS-type TFT memory device with Nitride trapping layer on the various temperatures

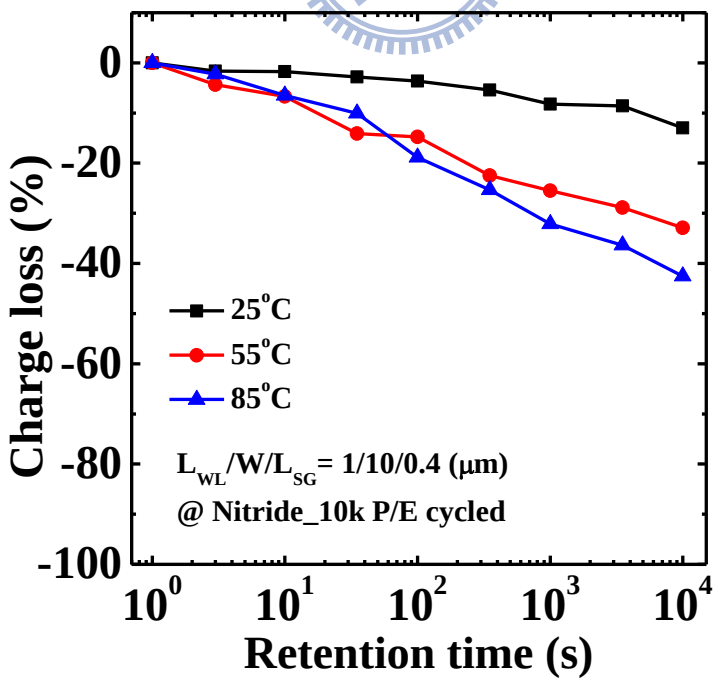


Fig. 4. 14 Data retention characteristics of 10k cycled WSG SONOS-type TFT memory device with Nitride trapping layer on the various temperatures

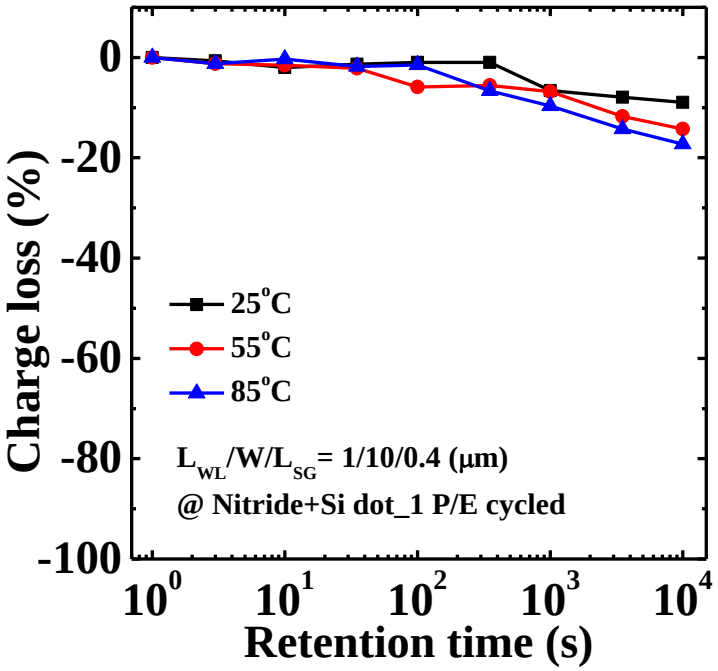


Fig. 4. 15 Data retention characteristics of 1 cycled WSG SONOS-type TFT memory device with Nitride + Si dot trapping layer on the various temperatures

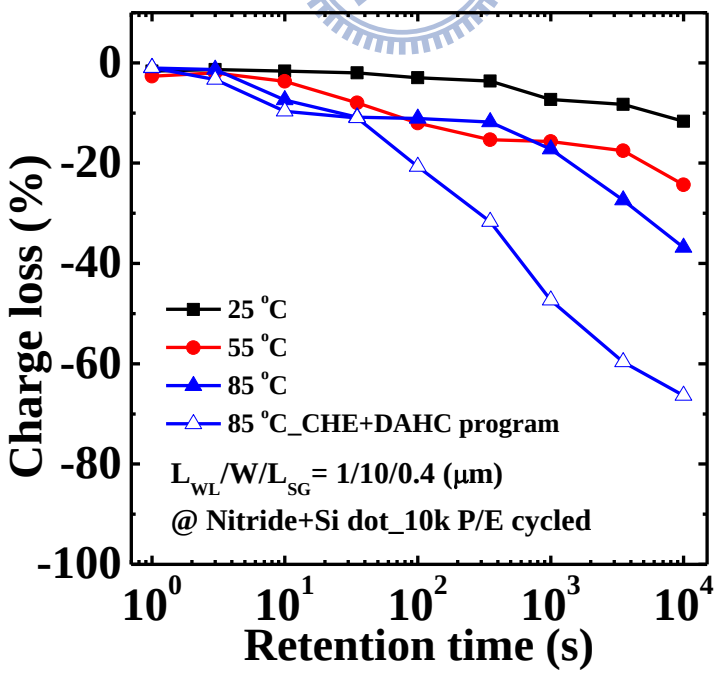


Fig. 4. 16 Data retention characteristics of 10k cycled WSG SONOS-type TFT memory device with Nitride + Si dot trapping layer on the various temperatures

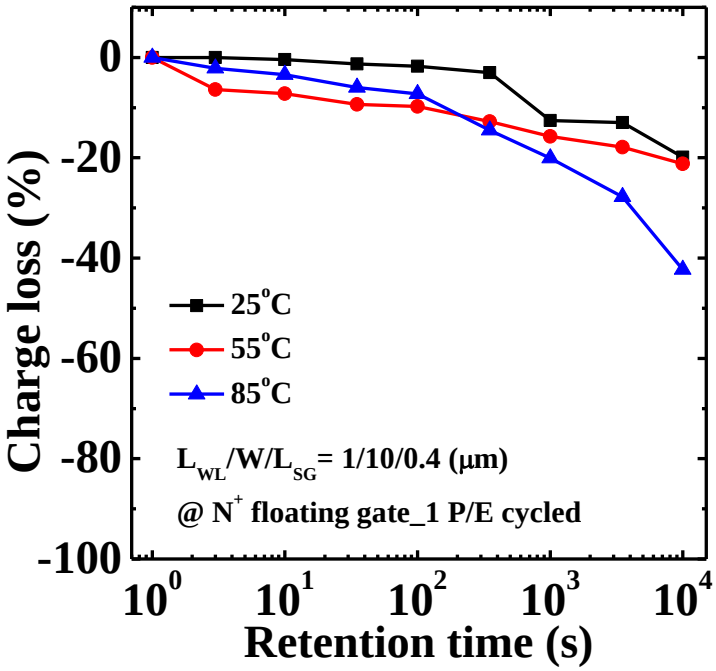


Fig. 4. 17 Data retention characteristics of 1 cycled WSG SONOS-type TFT memory device with N^+ floating gate trapping layer on the various temperatures

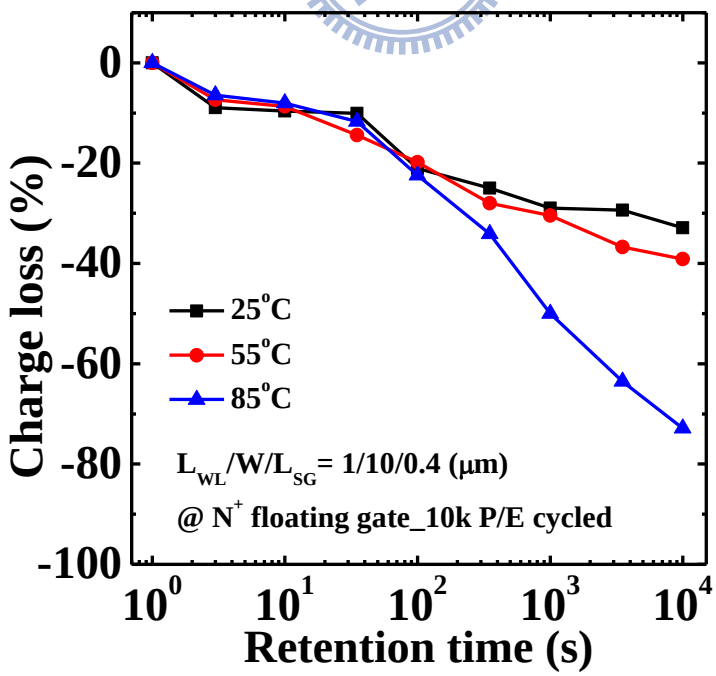


Fig. 4. 18 Data retention characteristics of 10k cycled WSG SONOS-type TFT memory device with N^+ floating gate trapping layer on the various temperatures

Chapter 5

Conclusions

5.1 Conclusions

In this thesis, we talk about the advantages and challenges of SONOS-type flash memories. SONOS memory is usually considered as a promising candidate of memory technology during the interim period from floating gate structure memories to the next generation memories. For the first time, we have successfully demonstrated the feasibility of applying wrapped-select-gate structure to thin film transistor memory. Besides, fabricating embedded Si-NCs in nitride trapping layer using *in-situ* deposition method and the idea of replacing nitride trapping layer with floating gate are also carried out in this WSG SONOS-type TFT memory experiment.

For the performance part of WSG SONOS-type TFT memories, Nitride cell and Nitride_Dot cell have comparable program speed and memory window. While Floating gate cell have floating gate coupling issue which limits the operation bias or it may lead to losing of two bit per cell characteristics. During programming, we find that the increase of word-line gate voltage will result in the enhancement of both lateral and vertical electric field during programming. However, it is still a serious trade-off concern between the enhancement of lateral and vertical electric field in conventional channel hot electron program. On the other hand, the increased bit-line voltage will enhance lateral electric field but suppress vertical electric field at the same time. For erasing mechanism, negative word-line gate voltage enhance tunneling efficiency of holes and positive bit-line voltage for N^+ source/drain region as reverse bias is responsible for generating excess holes. Combining negative word-line gate voltage and positive bit-line voltage, we can apply BTBTHH and junction breakdown

as erasing mechanism for WSG SONOS-type TFT memory.

For the reliability part of WSG SONOS-type TFT memories, thermal emission and trap assisted tunneling are responsible for charge loss in data retention. Fowler-Nordheim tunneling and trap assisted tunneling are regarded as main causes of leakage current of Nitride cell and Nitride_Dot cell in disturb stress. As for Floating gate cell, there exist a serious gate coupling effect for every operation containing large word line bias. In the end, discrete charge trapping devices of TFT memory like Nitride cell and Nitride_Dot cell have charge mismatch problem in P/E endurance test. The operation of SSI and BTBTHHI separate the injection location of carriers which can ease the pressure of defect generating in tunneling layer. Nevertheless, it is quite urgent to find a better dielectric material to take the place of poor-quality TEOS oxide for improvement of reliability characteristics. In the end, we find Nitride_cell has 6-8% charge loss improvement in high retention test over Nitride_cell.

5.2 Future work

In this work, we have investigated different trapping layer material memories with wrapped-select-gate structure. Among these experiments, nitride with embedded silicon nanocrystals (Si-NCs) cell shows better reliability characteristics than others. In order to go further in the development of device performance, blocking oxide could be substituted for high-k materials like aluminum oxide. As for floating gate cell, we can further use more advanced lithography equipment to cut off N^+ floating gate region. In this way, we can divide floating gate layer into two parts, and the interference between two bits will be greatly improved.

Concerning further scaling down of electronic devices, 3D-like structure has been widely studied for a long time. According to the latest news of semiconductor industry, Intel announced a historic innovation in 22nm-based microprocessors using FinFET structure. It is feasible to combine wrapped-select-gate structure and FinFET structure to get better performance characteristics.

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作者簡歷 Vita

姓名：薛芳昌

性別：男

生日：中華民國 76 年 7 月 26 日

籍貫：台灣 台中市

住址：台中市大安區松雅里松九街 76 號

學歷：國立台中第二高級中學

2002 年 9 月– 2005 年 6 月

國立臺灣師範大學物理學系

2005 年 9 月– 2009 年 6 月

國立交通大學電子物理學系碩士班

2009 年 9 月– 2011 年 6 月

論文題目：

隱藏式選擇性閘極結構之薄膜電晶體記憶體元件研究

A Study on Wrapped-Select-Gate SONOS-type Thin Film Transistor Memory Devices