非晶態氧化銦鎵鋅薄膜電晶體其幾何結構對表面能態影響的整合

Integration of Surface State and Geometry Effects on Amorphous IGZO Thin-Film Transistors

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摘要

目前氧化物薄膜電晶體所使用的四種元件結構類似於非晶矽薄膜電晶體。其中值得注意的地方為不同的元件結構會對元件的電性產生明顯的改變，例如臨界電壓及次臨界擺幅等等。因此對於設計元件結構來說，考慮幾何結構對其元件電性上的影響是很重要的。

本研究採用逆交錯型(inverted-staggered)和逆共面型(inverted-coplanar)結構去調查及模型化表面能態對於非晶態氧化銦鎵鋅薄膜電晶體的影響。逆交錯型結構有者較少的表面能態及較低的接觸電阻，因此表現出更好的元件電性和穩定性。基於實驗的結果，逆交錯型表現出較高的載子移動率及較好的電壓應力下的穩定度，因此適合作為高性能非晶態氧化銦鎵鋅薄膜電晶體的元件結構。

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Abstract

For oxide based TFTs, the device structures are employed for four types which similar to a-Si TFTs. Noteworthy, the different structures result in distinct electrical properties including threshold voltage (V_{th}), sub-threshold swing (S) and so forth. Therefore, the geometry effect is important for designing device structures that varies the electrical performances seriously.

In this study, we investigate and model the influence of surface state effects of a-IGZO TFTs by adopting the inverted-staggered and inverted-coplanar structures. The inverted-staggered TFTs with less surface states and lower contact resistance show improved electrical and stable performances compared to inverted-coplanar TFTs. Based on our results, the inverted-staggered structure with higher mobility and better stability under voltage stressing is suitable as high-performance a-IGZO TFTs.

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Chapter 1

Introduction

1.1 Background of Thin Film Transistors

1.1.1 Basic Concepts

A thin-film transistor, TFT, fabricated by evaporation of all components on to an insulating substrate is first proposed by Weimer in 1962 [7]. Conventional TFTs are composed of semiconductor layer, gate insulator, and electrode terminals. The TFTs are particular form of field-effect transistors by depositing the active layer with a thin film semiconductor. A TFT device consisted of three terminals is shown in Fig. 1-1(a). The gate (G) terminal acts as a switch to control the transistor to open or close in a circuit. The TFTs are categorized to n-type and p-type semiconductors, and the majority carriers are electrons in n-type channel. On the other hand, the majority carriers are holes in p-type channel. In a n-type TFT, the current flows from drain (D) to source (S) which is originated from the drift of electron carriers.

Recent years, TFTs are became critical electronic switch components in active matrix array techniques for driving the pixels turn-on and turn-off, such as liquid crystal displays (LCDs), active-matrix organic light-emitting diodes (AMOLEDs), and other consumer electronics

[1-3]. The benefit of TFTs technique is utilized independent transistor for each pixel in the display. Fig. 1-1 (b) shows the equivalent circuit of the active-matrix LCDs. Once a particular row is scanned on by a electrical pulse, the proper TFT is switched on, and then a charge is sent down the correct data line to charge both of the LC and the storage capacitor. Since the scan line and the TFT are switched off, the capacitor is able to hold the charge until the next refresh cycle. This active-matrix driving technique provides a brighter, screen faster and more colorful display than the passive-matrix technique.

Furthermore, in the concepts of the active layer material, TFTs based on amorphous silicon or polycrystalline silicon (poly-Si) have been widely used in flat panel displays (FPDs) recently. However, future displays demand fast response time, large panel size, transparency, and low power consumption. Conventional hydrogenated amorphous silicon (a-Si:H) [4] TFTs are limited in performances such as low field-effect mobility and sensitivity of visible light. The low field-effect mobility becomes a limitation for a driving high response time display. Although poly-Si TFTs exhibit large field-effect mobility, the grain boundary issue limits their application only in small panel size. Lately, based on large area uniformity, high field-effect mobility and room temperature (RT) deposited process, TFTs using metal oxide semiconductors as a channel layer have attracted much attention for manufactures. In particular, amorphous indium gallium zinc oxide (a-IGZO) TFTs with superior electrical properties such as flexible, visible light transparency and high field-effect mobility are widely

developed [5-6].

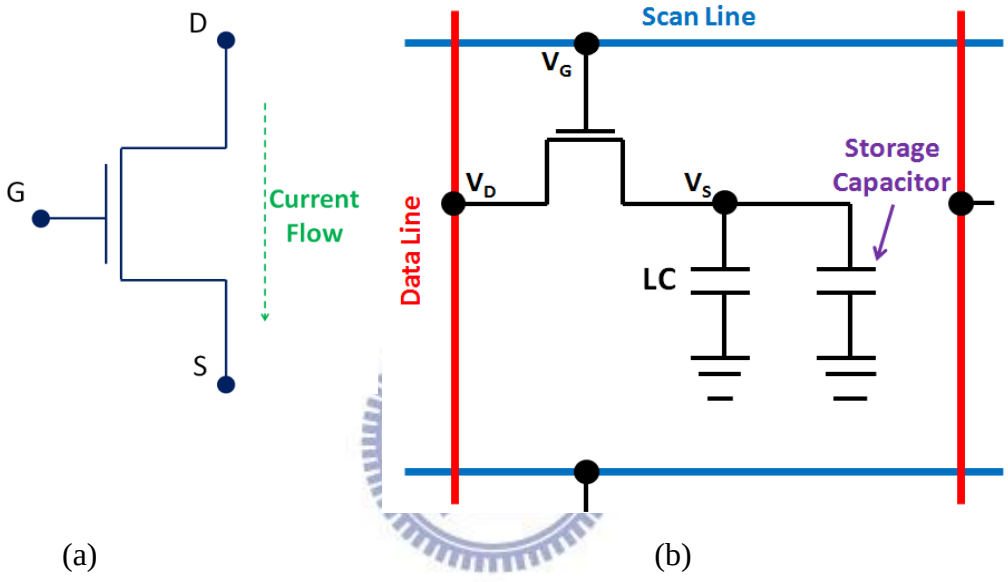


Fig. 1-1 (a) The schematic of a TFT and (b) the equivalent circuit for AMLCDs, respectively

1.1.2 Device Structure of TFTs

For the developments of TFTs structures, there were four types of TFTs structures deposited by a-Si as the active layer as shown in Fig. 1-2 [6]. The classification of the structures is convenient to define by the stacked order of the gate electrode, dielectric, active layer, and source/drain electrodes. To elaborate on the classification, first the device structures can be divided into two types called normal or inverted structure. The bottom gate contact named inverted structure is the gate electrode as the first layer deposited on the substrate, while the normal structure has the top gate contact form oppositely. Besides, another classification is depended on whether the source/drain contacts and gate are formed in the same or opposite side of the active layer called coplanar or staggered structure, respectively. Different configurations results in different device fabrications, and thus causes distinct electrical performance. Typically, a-Si TFTs use the inverted type structures due to the easy fabrications and give them better electrical performance. Contrasting to the poly-Si TFTs, the devices typically fabricate in normal type structures which are the nearest thin film analog of the crystalline Si MOSFETs. A flat and continuous Si thin film without other layers beneath is a better choice for laser irradiation re-crystallization process to convert the a-Si to poly-Si.

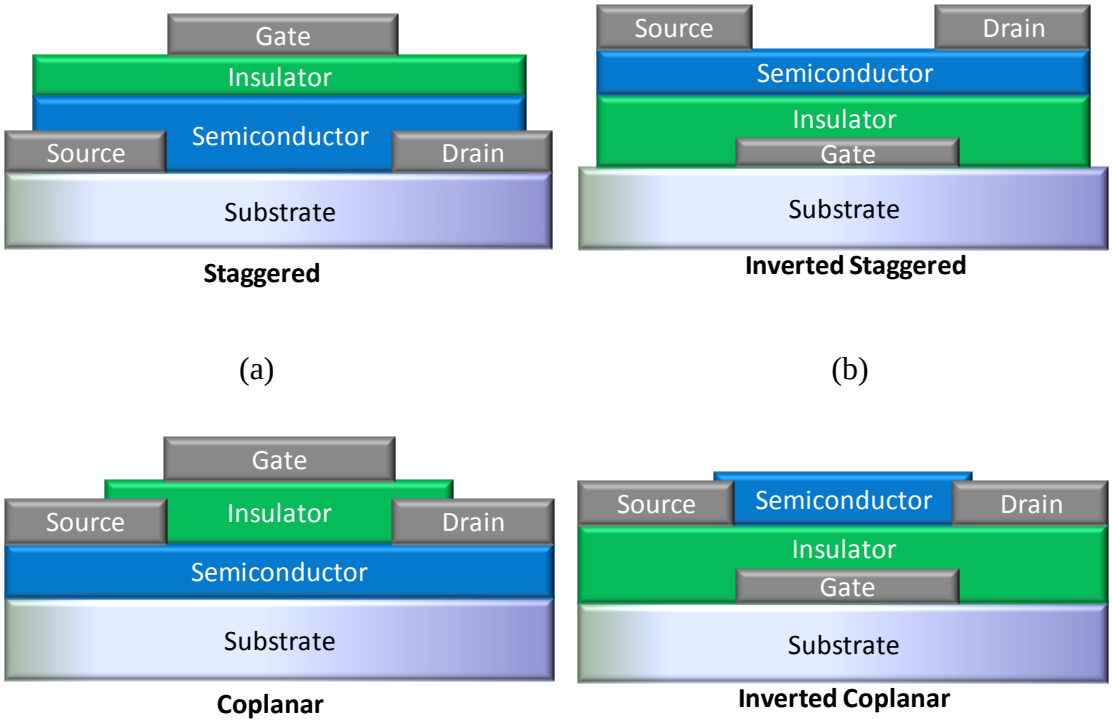


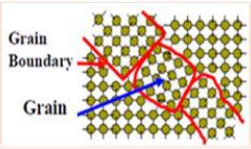
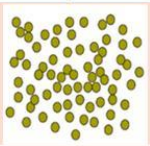
Fig. 1-2 Four kinds of TFTs configurations: (a) staggered, (b) inverted-staggered, (c) coplanar, and (d) inverted-coplanar

1.2 Development of Metal Oxide TFTs

Among the thin film materials, the transparent metal oxide such as SnO_2, In_2O_3, ZnO, CdO, and their alloys with high electrical conductivity received much attention because of their important applications [8]. In particular, the indium tin oxide (ITO) is a well-known material used in display industry. These metal oxide materials also have semi-conductive property to be used as the active layer of TFTs [9].

In recent research, these metal oxide TFTs exhibit field effect mobility above 10 cm^2/Vs even in the amorphous state, which is more than one order of magnitude compared to traditional a-Si TFTs [10]. The field effect mobility of amorphous metal oxide semiconductors is similar to the corresponding crystalline phase, even under the room temperature deposition process. Furthermore, a conventional metal oxide semiconductor, zinc oxide (ZnO), is polycrystalline state in nature even at room temperature. The grain boundary of such metal oxides affects device properties including uniformity and stability over large areas. However, the ZnO compound semiconductors such as In-Zn-O, Zn-Sn-O and In-Ga-Zn-O can be amorphous state at room temperature and have been proposed as the active layer in TFTs [11-12]. These amorphous metal oxide compound TFTs overcome the drawbacks of a-Si:H and poly-Si TFTs in flat panel displays and can be one of the promising candidates for the increase in the size of the flat panel display because of high mobility and good uniformity. The comparisons of amorphous metal oxide and conventional silicon TFTs are summarized in Tab. 1-1.

Tab. 1-1 The characteristics of poly-Si, a-Si, and a-metal oxide materials

Characteristic	poly-Si	a-Si	a-metal oxide
			
Stability	**Excellent**	Good	Good
Uniformity	**Bad(grain boundary)**	**Good**	
Mobility (cm^2/Vs)	**>80**	<1	**>10**
I_{off}	High	Low	**Lowest**
Profits	High cost (7-9 masks)	**Low cost (3-5masks)**	
Processing Temperature	High	**Low**	

1.3 Technology of a-IGZO

1.3.1 Electron Transport Characteristics

In order to describe the electron transport characteristics of a-IGZO, an In_2O_3-Ga_2O_3-ZnO ternary system is modeled. For the ternary system of In_2O_3-Ga_2O_3-ZnO, the electron transport characteristics are deeply related to each fraction. As shown in Fig. 1-3, the highest mobility around $40cm^2/Vs$ is obtained when the fraction of In_2O_3 is the primary contents in the thin films, because the In^{+3} conform to the criterion for electronic configuration $(n-1)d^{10}ns^0$ ($n \geq 5$) of heavy post transition metal cation [12]. Fig. 1-4 illustrates the effect of oxygen pressure during the deposition procedure upon the carrier concentration in a-IGZO and a-IZO. It is clear that the carrier concentrations of a-IZO do not show any distinct variation when the

partial oxygen pressure shifts from 0 to 10 Pa. The incorporation of Ga^{3+} suppresses the generation of electron carriers effectively. The Ga^{3+} attracts the oxygen ions tightly due to its small ionic radius which results in high ionic potential, and thereby suppresses electron injection which is caused by oxygen ion escaping from the thin film [13].

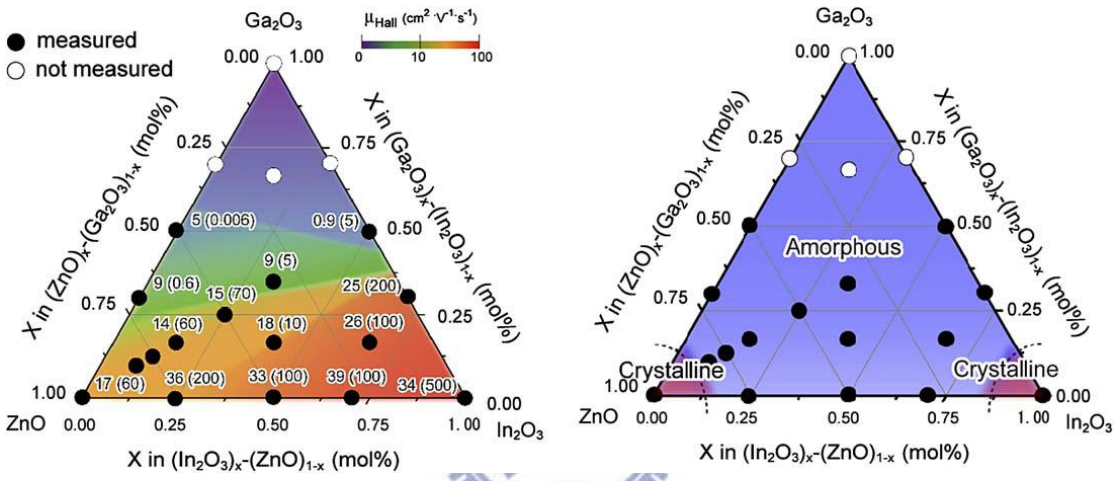


Fig. 1-3 The amorphous formation region (right) and the electron mobility and concentrations evaluated from the Hall effects for the amorphous thin films (left) in the In_2O_3–Ga_2O_3–ZnO system, respectively. The thin films were deposited on a glass substrate by pulse laser deposition under deposition atmosphere of P_{O2} = 1 Pa. Number in the parenthesis denotes carrier electron concentration ($x10^{18}$ cm^{-3}) [13]

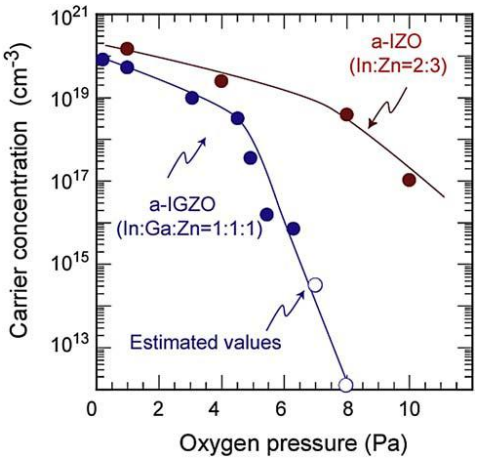
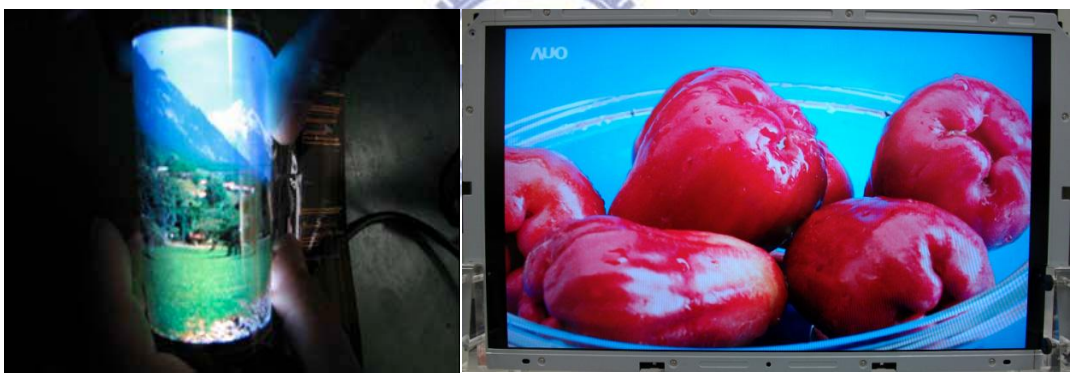


Fig. 1-4 The carrier concentration as a function of O_2 pressure during the deposition in a-IGZO and a-IZO [13]

1.3.2 Developments of a-IGZO TFTs

Since a-IGZO thin film transistors are first described by Nomura et al. in 2004 [12], many groups have joined the development of oxide TFTs and proposed various methods to enhance the stability or the electrical performances of a-IGZO TFTs. For instance, the means of plasma treatment on a-IGZO thin film was adopted to reduce the contact resistance between active layer and S/D electrodes [14-15]. Besides, several novel gate dielectric materials such as HfO_2 Al_2O_3, and Y_2O_3 were also investigated to substitute the traditional dielectric SiO_2 or SiN_x which effectively enhance the interface issue between the gate insulator and the active layer [16-18]. Moreover, TFTs with passivation layer upon the back channel reveal stable electrical properties in ambient than the prototype TFTs structure [19-21].

Different products using oxide TFTs have been demonstrated as shown in Fig. 1-5. Samsung Mobile Display reported a 6.5 inch flexible AMOLED driven by a-IGZO TFTs. The TFTs deposited on polyimide plastic substrate shows no deterioration while bending down to radius (R) = 3mm [22]. In SID 2010, AU Optronics Corporation demonstrated a 32 inch LCD by using a-IGZO TFTs. The coplanar type TFTs exhibited field-effect mobility of 5.16 cm^2/Vs, threshold voltage of 0.5 V, sub-threshold swing of 0.38 V/decade, and I_{on}/I_{off} higher than 10^8 [23]. These prior arts indicated that a-IGZO TFTs can be the next generation displays.



(a) (b)

Fig. 1-5 Photographs of (a) 6.5 inch flexible full-color top emission AMOLED panel with a-IGZO TFTs as back plane and (b) 32-inch TFT-LCD driven by a-IGZO TFTs

1.4 Motivation and Objective

For oxide based TFTs, the device structures are employed for inverted-staggered and inverted-coplanar structures which similar to a-Si TFTs. In research, the most common structures for a-IGZO TFTs are inverted-staggered and inverted-coplanar types due to the easily use of silicon oxide or silicon nitride as the gate insulator. Noteworthy, the different structures result in distinct electrical properties including threshold voltage (V_{th}), sub-threshold swing (S) and so forth [24-25]. Therefore, the geometry of the TFTs leads to vary the electrical performances seriously.

For the purpose of achieving a high performance a-IGZO TFT, we concentrate on investigating and modeling the electrical properties with the surface state influences in the interface of insulator, active layer, and bulk TFTs by employing the inverted-staggered and inverted-coplanar as the device configuration, respectively. We aim to offer a standard reference to select the suitable structure of the a-IGZO TFTs.

1.5 Thesis Organization

The organization of this thesis as follows: The background, operation principle, and the extraction method of TFTs device parameters are described in **Chapter 2**. The experiment and equipment details are presented in **Chapter 3**. In **Chapter 4**, the discrepancies of the transfer characteristics and the DC bias stressing between inverted-staggered and inverted-coplanar structures are discussed. The simulations of the surface state effects in different structures are also proposed. Finally, the conclusions and future works are summarized in **Chapter 5**.

Chapter 2

Principles and Theory

2.1 Introduction

In this chapter, the principles of TFTs are introduced first. Second, the extraction method of electrical parameters including threshold voltage (V_{th}), sub-threshold swing (S), field-effect mobility (μ), and I_{on}/I_{off} are defined. Finally, the source/drain contact resistance and the density of states are described.

2.2 Operation Principle of TFTs

The operation principle and the structure of TFTs are similar to the metal-oxide-semiconductor field-effect transistors (MOSFETs) which are widely used in single crystal silicon as the semiconductor. Different from MOSFETs, TFTs are three terminal devices with a source terminal (injecting carriers), a drain terminal (extracting carriers) and a gate terminal (for controlling the concentration of carriers in channel region).

To realize the operation mechanism, a bottom gate with top contact (inverted-staggered)

TFTs structure is shown in Fig. 2-1. As with the n-type MOSFETs, there are two operational regimes in the n-type TFTs: linear region and saturation region. In the linear region ($V_{DS} \ll V_{GS} - V_{th}$), the drain current is directly proportional to the drain voltage and can be written as:

$$I_{DS} = \frac{1}{2} \mu_{FE} C_{ox} \left(\frac{W}{L}\right) [(V_{GS} - V_{th}) V_{DS} - V_{DS}^2] \quad (2.1)$$

where C_{ox} is the capacitance per unit area of the gate insulator. V_{th} is denoted as the smallest applied gate voltage that causes a non-negligible increase in drain current for a given drain voltage. W and L are represented the TFTs channel width and length, respectively. A more thorough description of the electrical parameters relative to V_{th} and μ_n is described in next section. When the drain voltage increases and exceeds the relational expression of $V_{DS} \equiv V_{GS} - V_{th}$, the drain current is constant with increasing the drain voltage and this condition is called the saturation region. The formula of the drain current can be expressed into Eq. 2.2.

$$I_{DS} = \frac{1}{2} \mu_{FE} C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{th})^2 \quad (2.2)$$

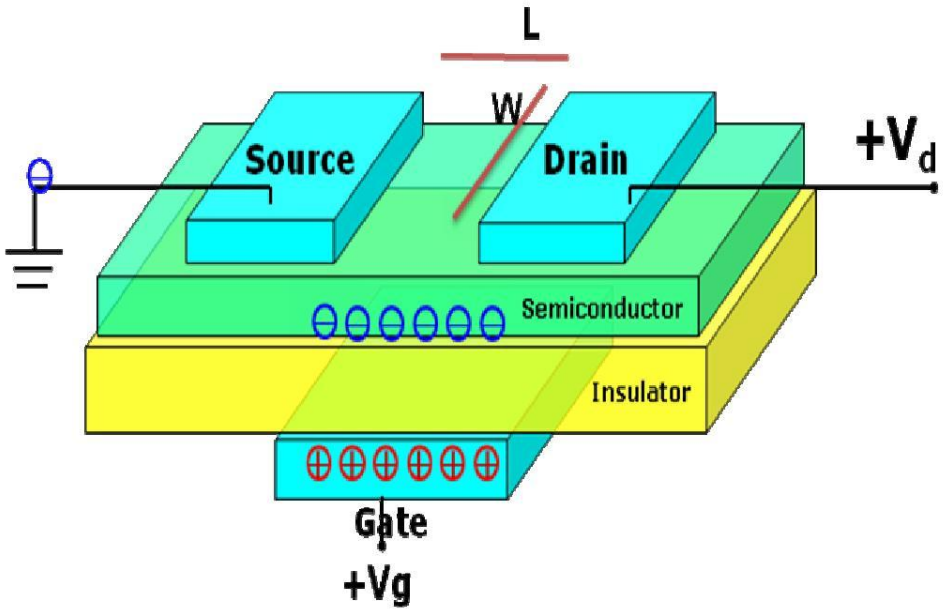
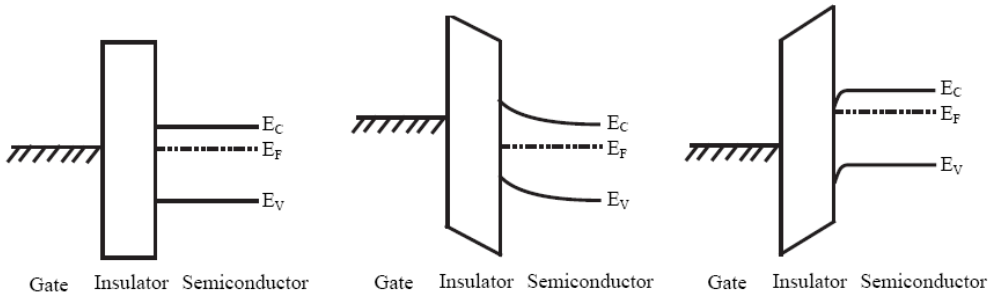


Fig. 2-1 A bottom-gate-top-contact TFT structure

In addition, the TFTs can be classified into two operational modes: the depletion-mode and the enhancement-mode. The classification is based on when the drain current flows through TFTs, whether the gate voltage is applied or not. For the depletion-mode TFT, the device is on when there is no voltage applied to the gate electrode. It needs an extra applied voltage (negative voltage for n-type, and positive voltage for p-type) to turn off the device. On the other hand, without the gate applied voltage, the device is off and only leakage current flows through is called enhancement-mode TFT. This TFTs mode needs to apply the threshold voltage to turn on the channel.

The energy band diagrams of an n-type enhancement-mode TFTs are shown in Fig. 2-2 to illustrate the energy band condition under operation. When no gate voltage is applied, the

energy band keeps in an equilibrium state. Once a negative voltage is applied to the gate, delocalized electrons in the channel are repelled from the semiconductor/insulator interface to create a depletion region of positive charge. The bending of conduction band and valance band near the insulator are represented the channel with depletion state as shown in Fig. 2-2 (b). As a positive voltage is applied to the gate terminal, delocalized electrons in the channel region are attracted to the semiconductor/insulator interface. This phenomenon creating electron accumulation at the interface, as indicated by the negative curvature in the conduction and valence bands in Fig. 2-2 (c).



(a) (b) (c)

Fig. 2-2 Energy band diagrams as viewed through the gate of the TFT. Energy band diagram when the gate with (a) no applied voltage, (b) a negative voltage, and (c) a positive voltage is applied

2.3 Method of Parameter Extraction

The general electrical parameters of TFTs such as V_{th}, S value, and the I_{on}/I_{off} are usually deduced from the transfer characteristics, where I_{DS} is plotted against V_{GS} for various V_{DS} as shown in Fig. 2-3. The extraction method will be introduced in detail below.

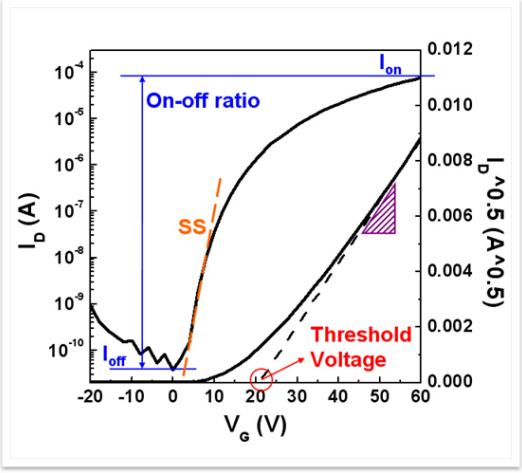


Fig. 2-3 Conventional n-type TFTs transfer characteristics

(1) Threshold Voltage (V_{th})

There are a lot of methods to extract the V_{th} at present which is one of the most important parameter in the voltage driving system. We adopts the constant drain current method in which the voltage at a specific drain current I_{ND} is taken as V_{th}, where I_{ND} denotes normalized drain current. The I_{ND} is expressed as the Eq. 2-3, which is used to remove the effect of the device dimensions.

$$I_{ND} = \frac{I_D}{W/L} \quad (2\text{-}3)$$

When the V_{DS}=0.1V, a particular value which drain current approximately reached 10^{-8}A is taken as V_{th}. When the V_{DS}=5V, a particular value which drain current approximately reached 10^{-7}A is taken as V_{th}. The constant current method is popular adopted in most studies of TFTs.

(2) Sub-threshold Swing (S)

The S value is a typical parameter to describe the control ability of gate toward channel which reflects the value of V_{GS} required obtaining a 10 times larger I_{DS} in the sub-threshold region. Theoretically, the S is independent of drain voltage and gate voltage. However, the S is still influenced by the short channel effects such as charge sharing, avalanche multiplication and punch through-like effect. The sub-threshold swing is also related to the gate voltage due to undesirable factors such as resistance and interface state. The S is evaluated from the TFTs transfer characteristic in the sub-threshold region, using the following equation:

$$S = \left(\frac{\partial \log(I_D)}{\partial V_{GS}}\right) \quad (2\text{-}4)$$

(3) Field-effect Mobility (μ_{FE})

At present, there are lots of methods to calculate the field-effect mobility μ_{FE}. In this thesis, the μ_{FE} is induced by the transconductance (g_m) at a low drain voltage (V_{DS} = 0.1V) [26]. The μ_{FE} is derived from the transfer characteristic in Eq. 2-1 at beginning. When V_D is much

smaller than $V_G - V_{th}$ or $V_G > V_{th}$, drain current can be approximated as:

$$I_{DS} = \mu_{FE} C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{th}) V_{DS} \quad (2\text{-}5)$$

Transonductance is defined as

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_{D=const.}} = \mu_{FE} C_{ox} \frac{W}{L} V_{DS} \quad (2\text{-}6)$$

Thus, μ_{FE} is obtained from Eq. 2-6:

$$\mu_{FE} = \frac{L}{W V_{DS} C_{ox}} g_m \quad (2\text{-}7)$$

(4) I_{on}/I_{off}

I_{on}/I_{off} is another important factor of TFTs. The high I_{on}/I_{off} ratio represents not only the large turn-on current but also the small off current (leakage current). The practical method to determine I_{off} is defined the maximum leakage current as off state current when the drain voltage is applied at 4.5V. I_{on}/I_{off} affects gray levels (the numbers of bright to dark state) of the AMLCDs directly and I_{on} is particularly important for current-driving devices such as OLEDs. However, there are many dominant factors that affect I_{on}/I_{off} such as carrier concentration, dimension of channel width/length, interface state, ohmic contact, etc.

2.4 Contact Resistances

The complete analysis of the TFTs electrical performance also involves the extraction of the source and drain contact resistances. They are estimated by the well-known transmission line method (TLM) [27] using a series of TFTs with different channel lengths. The total TFT ON-resistance is:

$$\mathbf{R_T = \frac{V_{DS}}{I_{DS}} = r_{ch}L + 2R_{SD}} \quad (2\text{-}8)$$

where r_{ch} is the channel resistance per channel-length unit and $2R_{SD}$ is the total (source + drain) contact resistances, respectively.

The a-Si:H TFT model of TLM is illustrated in Fig. 2-4, the extraction of the TFT source and drain contact resistances is rather straightforward using a series of TFTs with different channel lengths. At first, the total TFT ON-resistance as a function of the TFT channel length for different gate voltages are plotted, ensuring that the TFT is in accumulation regime. Fitting the experimental data to linear lines and this step lets us to obtain the TFT total contact resistances from the *y*-intercepts and the channel resistance per channel length unit (r_{ch}) from the slopes in the figure [28]. The TLM also has been used for a-IGZO TFTs to extract the S/D contact resistances [29].

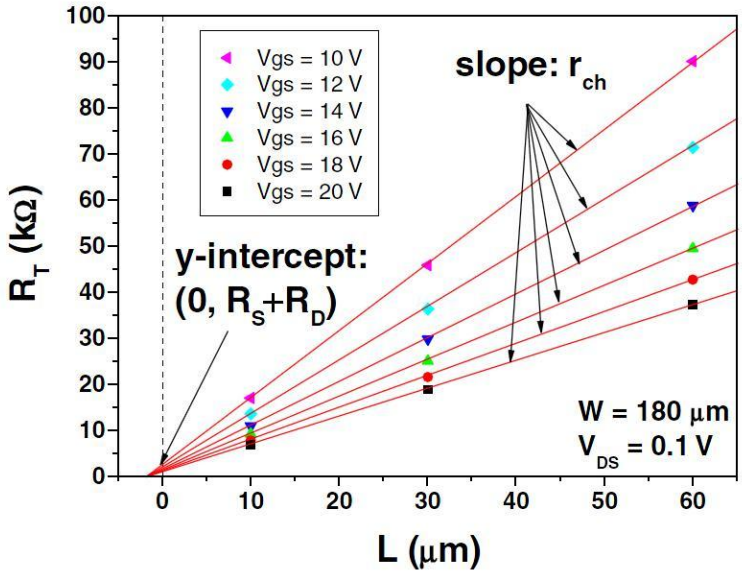


Fig. 2-4 The total TFT ON resistance (R_T) versus channel length (L). The TFT channel resistance per unit length (r_{ch}) and contact resistance ($R_S + R_D$) are extracted from the slope and y intercept of the plots for different V_{GS}, respectively [30]

2.5 Density of States

The density of states (DOS) governs many physical properties and consequently plays an important role in solid state physics. In solid state and condensed matter physics, the DOS describes the number of states per interval of energy at each energy level that are available to be occupied. Different from isolated systems, the density distributions are not discrete like a spectral density but continuous in gas phase of atoms or molecules. A high DOS at a particular energy level means that there are many states available for occupation. At a zero

DOS, there are no states can be occupied at that energy level. In general, the DOS is an average over the space and time domains occupied by the system.

Recently, a density-of-states model proposed by Fung et al. can simulate the a-IGZO TFTs electrical properties to conform to the experimental results precisely [31]. Fig. 2-5 illustrates the DOS of a-IGZO, the conduction band-tail states are thought to originate from the disorder of metal ion *s*-bands, while the oxygen *p*-band disorder mainly contributes to the valence band-tail states. The DOS model provides a better understanding on the physical properties of a-IGZO TFTs.

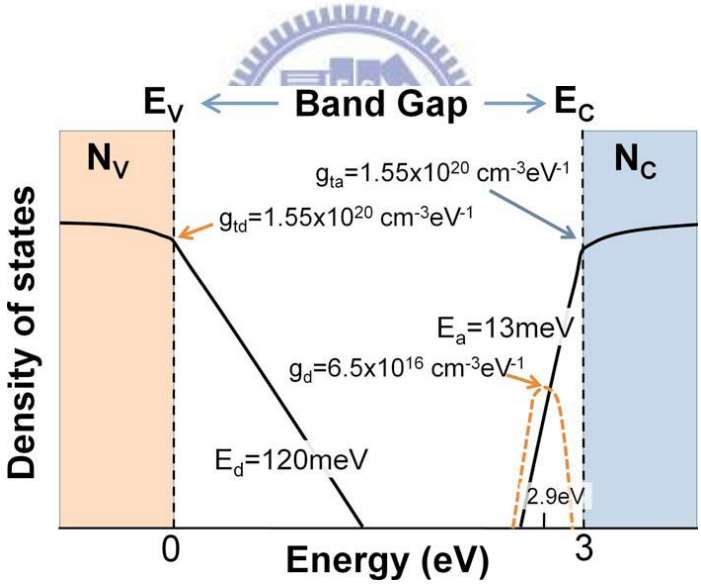


Fig. 2-5 Proposed DOS model for *a*-IGZO where E_C and E_V are conduction and valence band edge energies, respectively. Solid curves within the band gap represent the exponentially distributed band-tail states, while the dash curve near the conduction band edge represents the Gaussian-distributed donor-like oxygen vacancy states [31]

2.6 Summary

The a-IGZO thin film shows the promising property and the feasibility of room temperature (RT) deposition. The principles and theory of the a-IGZO TFTs are also investigated thoroughly. For practical application, the suitable structure of the a-IGZO must be studied by finding out the geometry and the surface states effects.

Chapter 3

Experimental Methods

3.1 Introduction

The major deposited method in this thesis is the sputtering system. Therefore, the principle of sputtering system including the RF sputtering and the DC sputtering will be described in this chapter. Besides, the fabrication flow of a-IGZO TFTs, fabrication facilities, materials and analyzers for electrical and thin films properties will also be introduced.

3.2 Process Design and Schemes

To study the geometry and the surface states effects of a-IGZO TFTs, the arrangement of the experiment is shown in Fig. 3-1. First, two kinds of a-IGZO thin films with different compound ratio are deposited by the sputtering system. The Auger electron spectroscopy (AES) is adopted to determine the atomic ratio of deposited thin films. Then the comparisons of geometry effect are presented by the measurement of I-V curves and DC voltage stressing.

Furthermore, the contact resistance and CV characteristics are adopted to explain the variation of device performance. On the other hand, the properties of surface states are modeled and investigated by a simulation method.

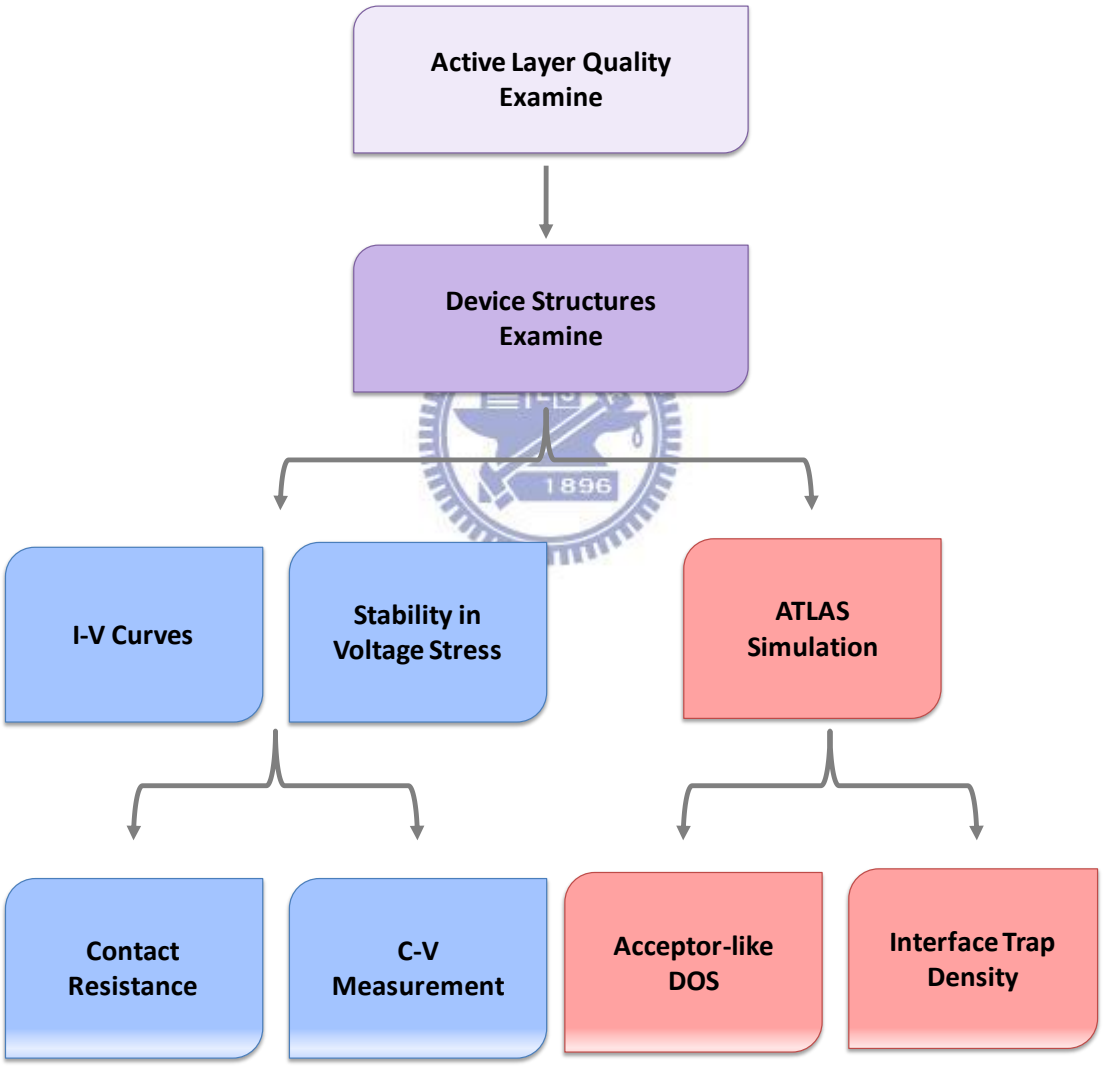


Fig. 3-1 Flowchart of the study

3.3 Principle of Sputter System

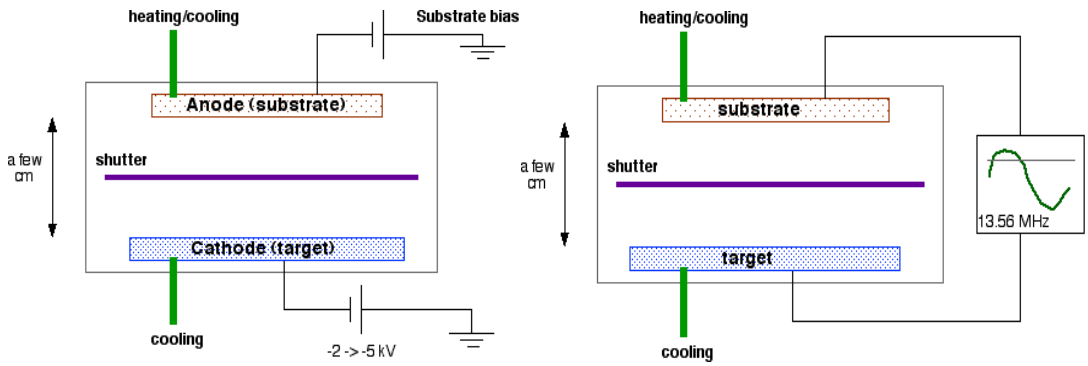
The sputter system is usually divided into two operation types, DC (direct current) and RF (radio frequency), which are classified by the power supply. The description in detail is below:

(1) RF sputtering

The RF sputtering uses the radio frequency power supply and operates at 13.56 MHz to generate plasma. The plasma creates ions which can be accelerated toward the target by a negative DC bias on the target. The ions hit the target with enough energy to dislodge the target atoms and then deposit onto the substrate. The RF sputtering is performed under vacuum, typically between 1mtorr and 50mtorr. A lower working pressure increases the mean free path which results in the deposited species having more energy to diffuse along the substrate surface in order to find the lowest energy state possible. The RF sputtering can be used to sputter both insulator and conductive targets, since charge does not build up on the surface of the target. The major disadvantages of the RF sputtering are the cost and deposited rate.

(2) DC sputtering

The major change from the RF to the DC sputtering is the power supply. In the DC sputtering, a direct current power supply is used to create the plasma. The physics of the sputtering process is identical. The DC sputtering allows higher deposited rates and low cost than the RF sputtering. Conventional DC sputtering is only used for sputtering conductive targets. The electron flux from the DC supply causes charge to build-up on the surface of an insulating target and renders the plasma unstable so that it eventually extinguishes. A pulsed DC source method is used in order to sputter insulating targets by DC sputtering system. When using a pulsed DC source, the voltage is periodically pulsed positive for a very short time to remove the charge on the insulating target. This positive pulse duration is a very small fraction of the entire period and results in a higher sputter rate than the RF sputtering.



(a) (b)

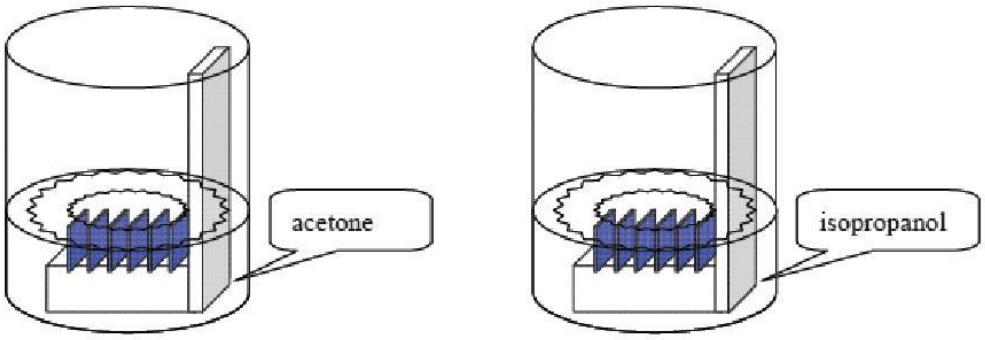
Fig. 3-2 (a) DC and (b) RF mode of sputter system

3.4 Device Fabrication Procedure

In this experiment, a n-type (antimony doping) silicon wafer with 100nm thick thermal SiO_2 was selected to represent the gate electrode and insulator layer, respectively. The a-IGZO active layer was deposited by the DC magnetron sputtering at RT. ITO as source and drain electrodes were deposited by the RF sputtering. The flowchart of the fabrications is shown in Fig. 3-6 and the deposition details of each procedure are described in the following section.

(1) Substrate Cleaning

The dimensions of Si wafer substrate are 3cm x 3cm. At first, the wafer is cleaned by detergent and DI water in succession. Next, the wafer is placed into the Teflon holder, and put them into a container with acetone. 30 minutes of ultrasonic vibration was carried out to remove the organic contamination. Afterward, wafer in placed into another container with isopropanol (IPA) and 30 minutes of ultrasonic vibration was performed to remove acetone. Sequentially, the N_2 jet was adopted to purge dry the wafer and then the water was baked at 120° C. Fig. 3-3 shows the procedure of ultrasonic vibration.



(a) (b)

Fig. 3-3 Schematic diagrams of container with (a) acetone and (b) IPA for ultrasonic vibration

(2) Active Layer Deposition

The high vacuum sputter system in NCTU with background pressure about 3×10^{-6} torr was placed in class 10K clean room as shown in Fig. 3-4. Vacuum system composes of rotary pump and cryo pump, which work for different pressure range. Power system consists of several DC and RF power modules with 6 sputtering guns and the purified gas sources of argon, nitrogen, and oxygen gas. The substrate planetary rotation system can bring high uniformity by rotating the sample disk and holders.

The a-IGZO active layer with 40nm in thick was deposited upon the silicon wafer with 100nm thickness of thermal SiO_2 by DC magnetron sputtering with an $InGaZnO_4$ target at RT. The deposition was done at DC power = 100W without any intentional substrate heating, working pressure = 3mtorr and argon flow rate = 10sccm.

Fig. 3-4 The Sputter system in NCTU

(3) Electrodes Deposition

The 50nm thick ITO as source and drain electrodes were patterned by means of shadow mask in RF magnetron sputter system with the background pressure about 3×10^{-6}torr. The deposition was done at RF power = 50W without any intentional substrate heating, working pressure = 3mtorr and argon flow rate = 10sccm.

(4) Annealing Process

Finally, the device was annealed in nitrogen ambience at 450 ° C for 1 hour by atmospheric anneal furnace to rearrange the a-IGZO and the passivation lattice again. After annealing

process, the electrical characteristics of the device are better than the device without annealing.

Fig. 3-5 shows the instrument of atmospheric anneal furnace.

Fig. 3-5 atmospheric anneal furnace

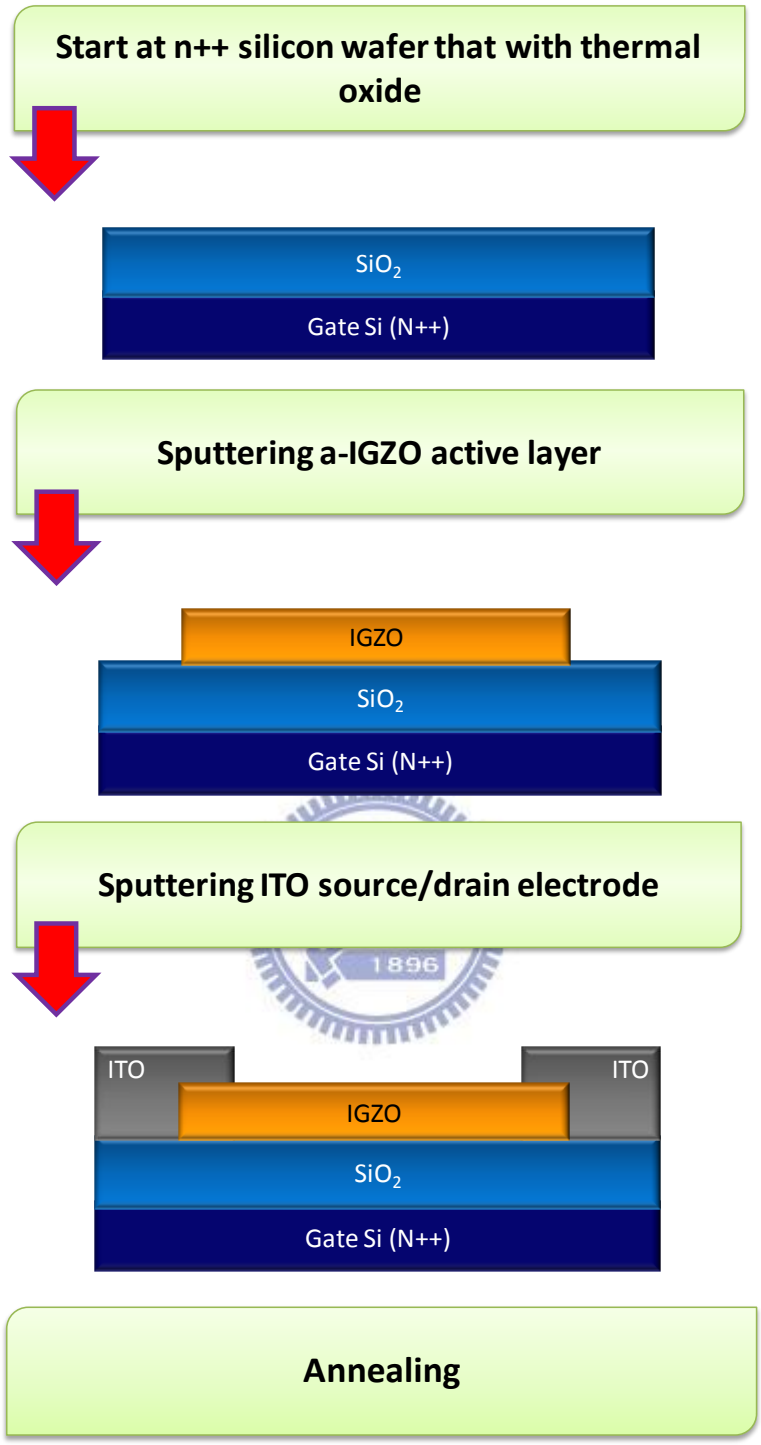


Fig. 3-6 Flowchart of a-IGZO devices fabrication

3.5 Devices Measurement and Analysis

(1) Measurement of Electrical Characteristics for a-IGZO TFTs

The device electrical properties, transfer and output characteristics, were measured by a semiconductor parameter analyzer (Keithley 4200) in the dark at room temperature (RT). In the output characteristic (I_{DS}-V_{DS}), the V_{DS} are conventionally swept from 0 to 40V at the step V_{GS} (step = 0.4V) to measure the corresponding I_{DS}. In the transfer characteristic (I_{DS}-V_{GS}), V_{GS} are conventionally swept from -10 to 30V. In voltage stressing measurement, V_{GS} and V_{DS} were set at +20V and the stress time is 5000 second. At each 500 second, the transfer characteristics were measured.

(2) Measurement of Capacitance-Voltage Characteristics

The procedure for the C-V measurements involves the application of DC bias voltages across the capacitor while taking the measurements with an AC signal as shown in Fig. 3-7. The source and drain electrodes are connected each other to form a terminal. Commonly, AC frequencies used for these measurements are from 1kHz to 10MHz. The bias is applied as a DC voltage sweep that drives the TFT devices from depletion into the accumulation region.

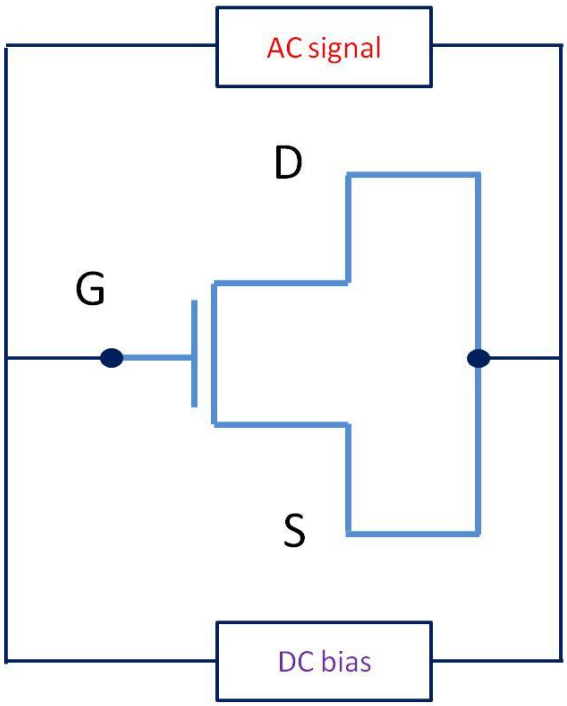


Fig. 3-7 Circuit of C-V measurement

(3) Thin Film Analysis

The surface chemistry and the material science of thin films common adopt a special analytical technique, which named Auger electron spectroscopy (AES). The Auger effect was discovered independently by both Lise Meitner and Pierre Auger in the 1920s. The Auger effect occurs when an incident electron removes a core state electron from an inner energy level and creates a core hole in the 1s level as illustrated in Fig. 3-8. An electron from the 2s level fills in the 1s hole and the transition energy is imparted to a 2p electron which is emitted. The emitted electron is called Auger electron and the energy is expressed as Eq. 3-1.

$$KE = E_K - E_L - E_M \quad (3\text{-}1)$$

The final atomic state thus has two holes, one in the 2s orbital and the other in the 2p orbital. The Auger electron emitted by different atom has its particular energy. Therefore, the element can be determined by using the AES to probe the particular energy of the Auger electron which is emitted from that element.

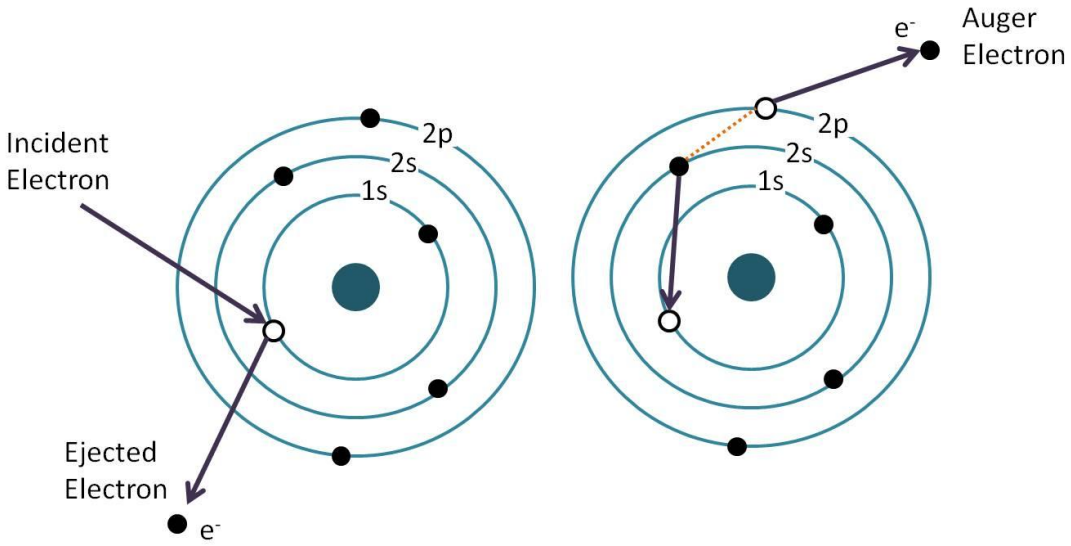


Fig. 3-8 Illustrates the steps of Auger process

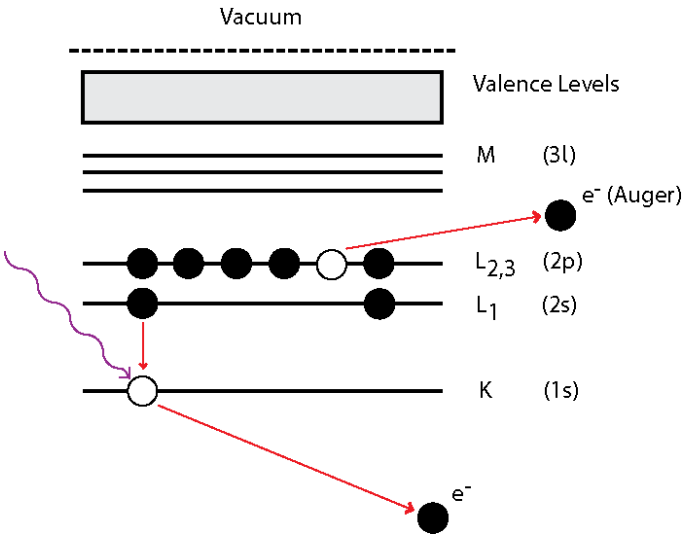


Fig. 3-9 Illustrates the same process using spectroscopic notation

3.6 Simulation Model

The ATLAS simulation based on DOS model in 2-D is employed to describe the electrical properties of the a-IGZO TFTs. The representative inverted-staggered a-IGZO structure used for ATLAS simulation is shown in Fig. 3-10. The a-IGZO active layer and SiO_2 gate insulator layer are 40nm and 100nm, respectively. To facilitate the analysis, the 2-D structure is

decomposed into mesh structure. The spaces (resolution) between grid points for different regions were optimized for computing time and best fit to experimental data. The contacts between source/drain electrodes and a-IGZO channel are either assigned as Schottky or ohmic contact in nature in this work.

The increasing structural disorder within amorphous material can induce electron scattering and eventually localized wave-functions. Such phenomenon can be approximately represented as localized tail states within band gap, near the band edges. In this study, band tail states of a-IGZO are represented as a function of energy (E) by following expressions:

$$g_{CBa} = g_{ta}\exp[(E - E_C/E_a)] \quad (3\text{-}1)$$

$$g_{VBd} = g_{td}\exp[(E_V - E/E_d)] \quad (3\text{-}2)$$

where E_C and E_V are conduction and valence band edge energy, g_{ta} and g_{td} are density of acceptor and donor like states at $E=E_C$ and $E=E_V$, and E_a and E_d are characteristic slopes of conduction and valence band tail states, respectively. Moreover, the peak values of Gaussian-distributed for acceptor-like and donor-like deep-gap states are used to represent the properties of a-IGZO thin films. The DOS model can accurately simulate the properties of measured transistors [32].

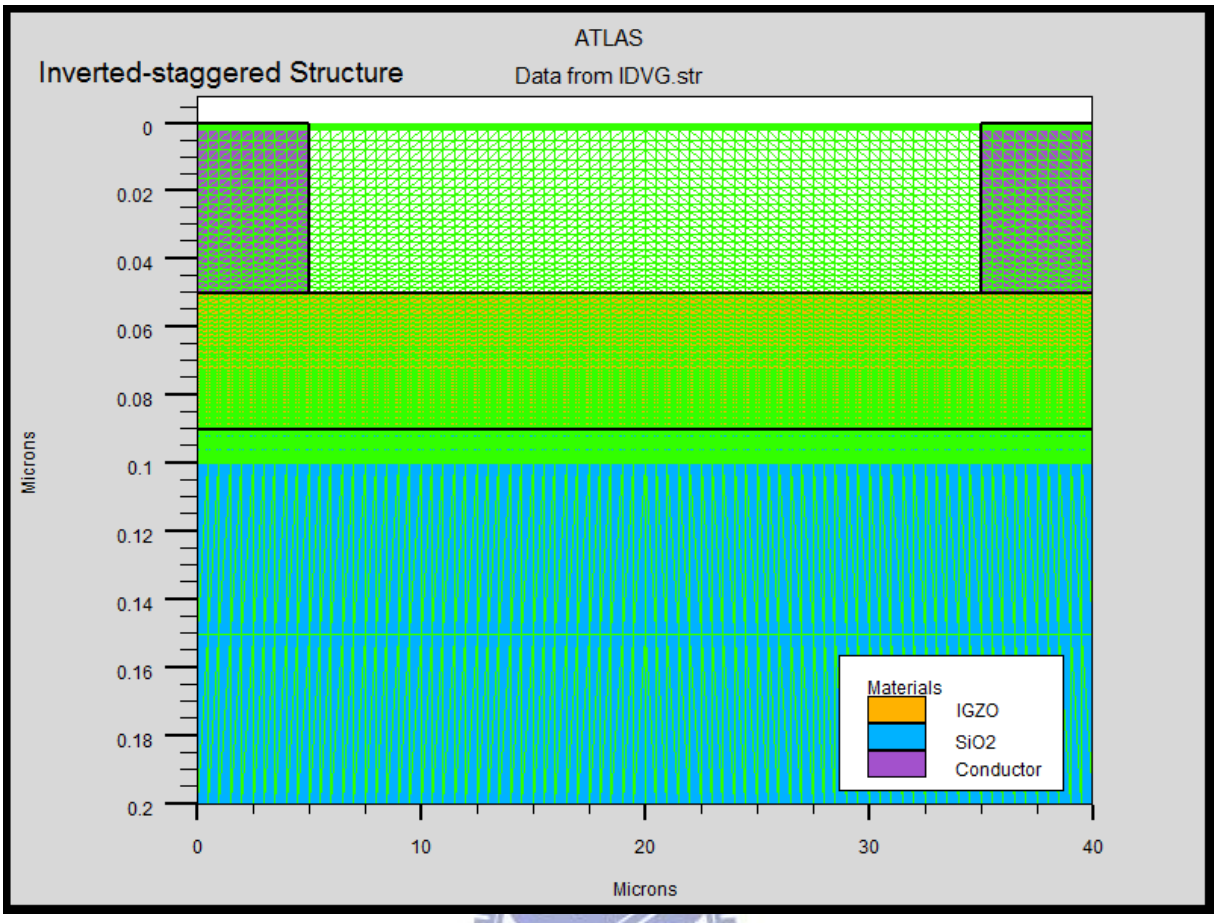


Fig. 3-10 Cross-sectional view of inverted-staggered a-IGZO TFTs

3.7 Summary

The inverted-staggered and inverted-coplanar structures of a-IGZO TFTs are fabricated. The properties of active layer were examined by AES. The performances and stabilities of different device structures are investigated by the Keithley 4200 semiconductor analyzer. The surface states properties of these devices are modeled by the ALTAS simulation tool. All of the experimental results and discussions will be given in Chapter 4.

Chapter 4

Results and Discussion

4.1 Introduction

The atomic ratios and properties of the a-IGZO semiconductor are discussed first. Then the electrical characteristics of inverted-staggered and inverted-coplanar structures of a-IGZO TFTs are compared and discussed. The characteristics of contact resistance and capacitance-voltage are employed to describe the variation of device performance. Afterward, the stability under bias stress is discussed. Finally, the simulation results are presented.

4.2 Analysis of the a-IGZO Thin Films

Because the IGZO is a multi-component material, the performance such as electrical properties and device stability are depended its the chemical composition. In this study, the growths of the a-IGZO thin films are deposited by DC and RF magnetron sputtering methods with different composition of sputtering targets, respectively. The DC and RF sputtering used the polycrystalline $InGaZnO_4$ and $In_2Ga_2ZnO_7$ targets, respectively. The sputtering condition of the $InGaZnO_4$ target is deposited at Ar flow rate equal to 10sccm, but the $In_2Ga_2ZnO_7$

target is deposited in a mixed Ar/O_2 (10:0.6 at sccm) gas environment.

The analysis of the thin film properties was carried out by AES and the results are shown in Tab. 4-1. The thin films deposited by DC target reveal more Ga content than RF target. As mentioned in the previous section, the Ga is effectively to suppress the electron carrier generation. Thereby, TFTs adopt the polycrystalline $InGaZnO_4$ target as the active layer by DC sputtering system will result in lower field effect mobility. Nevertheless, the TFTs with higher Ga content show more stable performance against the bias stress. The Ga has the highest binding energy with oxygen among the three metal components, thus the concentration of the weak bonds in the overall active layer seems to be suppressed by the increase of Ga content [33]. The V_{th} shift of transfer curve of TFTs is considered to contain more oxygen vacancies due to lower Ga content. Therefore, we choose the DC sputtering target to fabricate the a-$InGaZnO_4$ TFTs, which have better device stability.

Tab. 4-1 Atom ratios of a-IGZO thin films for different sputtering methods

Atom	At. % / DC target	At. % / RF target
In	18.88	18.90
O	46.75	44.09
Zn	17.56	22.70
Ga	16.81	14.30

4.3 Analysis of the Electrical Properties

After selecting the suitable sputtering target for active layer, the device structures are examined. The different structures and deposited procedures result in the distinct electrical properties including V_{th}, S value, etc. Therefore, the comparisons of the electrical properties are essential.

4.3.1 Output and Transfer Characteristics

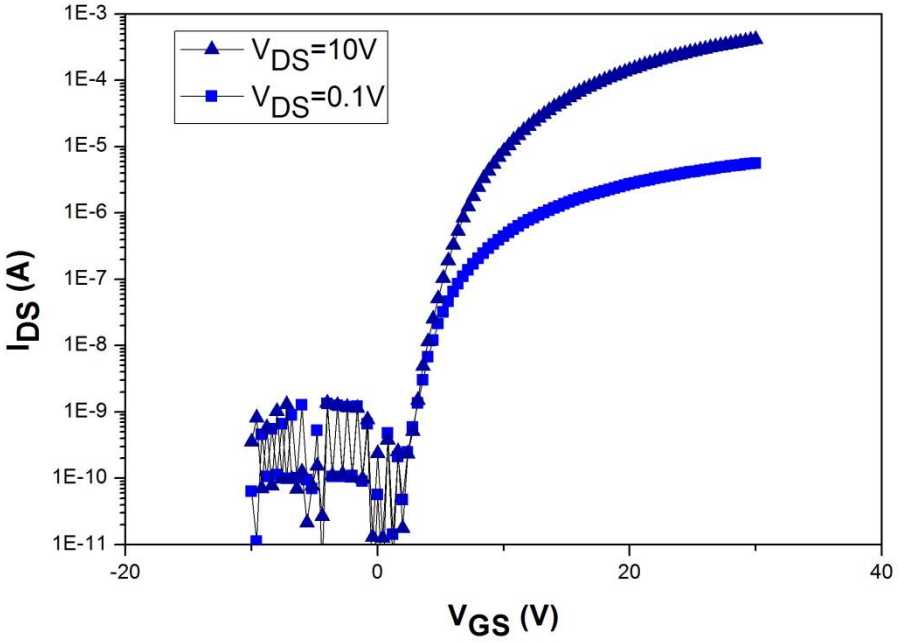
The transfer characteristics of a-IGZO TFTs for inverted-staggered and inverted-coplanar structures are shown in Fig. 4-1. The inverted-coplanar a-IGZO TFTs exhibit a V_{th} of 1.61V, a μ_{FE} of 5.97cm^2/Vs, a S value of 1.52V/decade, and a I_{on}/I_{off} of 1.34×10^6. In contrast, the inverted-staggered TFTs show a V_{th} of 3.96V, a μ_{FE} of 8.29cm^2/Vs, a S value of 0.91V/decade, and a I_{on}/I_{off} of 4.21×10^6. Fig. 4-2 shows the comparison of transfer and output curves between the inverted-staggered and inverted-coplanar TFTs, respectively. All of the parameters are summarized in Tab. 4-2.

Tab. 4-2 Extracted electrical parameters of a-IGZO TFTs with different structures

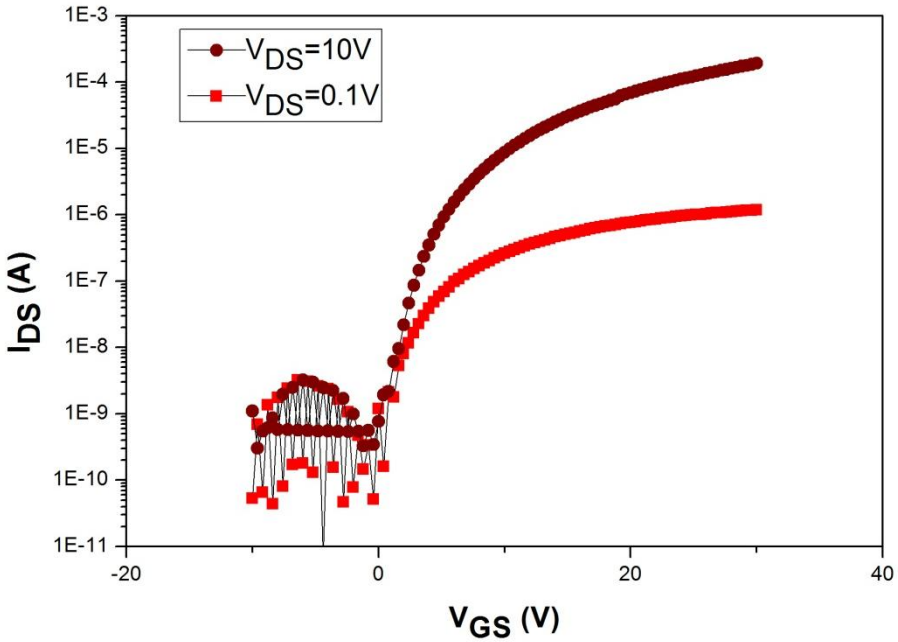
Structure	μ_{FE} (cm^2/Vs)	V_{th} (V)	S value (V/decade)	I_{on}/I_{off}
Inverted Staggered	8.29	3.96	0.91	4.21×10^6
Inverted Coplanar	5.97	1.61	1.52	1.34×10^6

4.3.2 Discussion

The results show that the inverted-staggered structure exhibits a better electrical performance compared to the inverted-coplanar device such as mobility, I_{on}/I_{off} and sub-threshold swing. These improvements are attributed to two major factors: the lower energy barrier between the channel and source/drain electrodes; and the defect creation at the dielectric/semiconductor interface during the source/drain electrodes deposition. Therefore, the contact resistance between S/D electrodes and active layer and C-V characteristic are employed to evaluate these two factors.

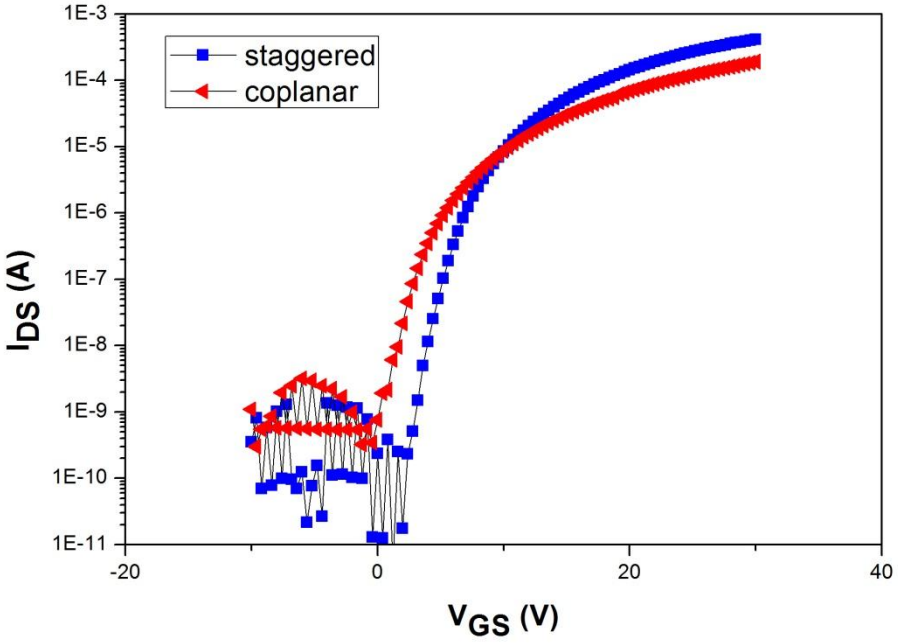


(a)

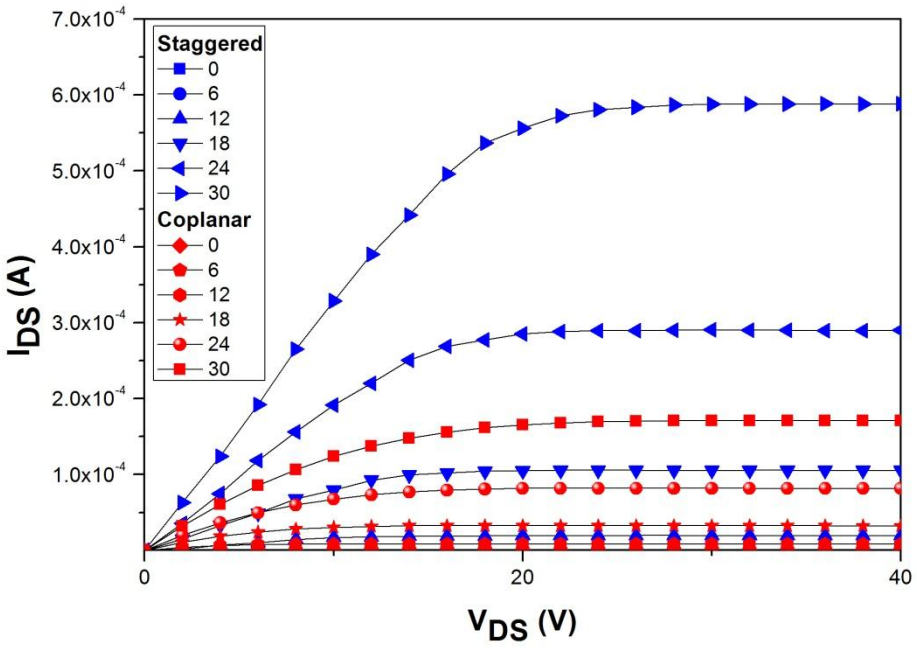


(b)

Fig. 4-1 I_{DS}-V_{GS} curves of a-IGZO TFTs of (a) inverted-staggered and (b) inverted-coplanar structures



(a)



(b)

Fig. 4-2 Comparison of the inverted-staggered and inverted-coplanar for (a) I_{DS}-V_{GS} and (b) I_{DS}-V_{DS} characteristics

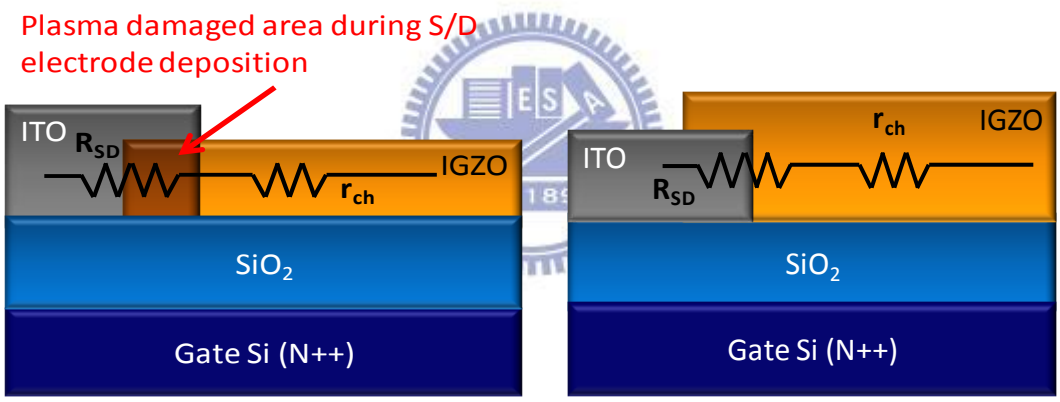
4.4 TFTs Source/Drain Contact Resistance

In order to investigate the contact effect for inverted-staggered and inverted-coplanar structures of a-IGZO TFTs, the TLM method is employed to measure the contact resistance. Fig. 4-3 illustrates the cross-section of the total resistances for inverted-staggered and inverted-coplanar structures. Fig. 4-4 shows the total resistances as a function of channel length. The contact resistances are obtained from the y-interception of the fitting linear line. The contact resistances of inverted-staggered and inverted-coplanar structures are approximately $1.056\times10^{5}\Omega$ and $2.822\times10^{5}\Omega$, respectively.

According to the sputtering operation, the energetic Ar ions bombard the surface of a-IGZO films during the electrodes deposition in the inverted-staggered procedure. The physical momentum transfers between the ions in the plasma and the atoms on the a-IGZO surface. Therefore, the oxygen on the films surface is preferentially dissociated by the Ar ion bombardment due to its relatively light atomic weight. Consequently, the inverted-staggered structure reveals smaller contact resistance than the inverted-coplanar structure due to the creation of electrons on the plasma damaged surface during the electrodes deposition. Therefore, the better contact effect leads the inverted-staggered structure to perform improved electrical properties such as μ_{FE}, I_{on}/I_{off}, and S value.

In terms of the channel resistance, r_{ch} is extracted from the slopes in Fig. 4-4. The

inverted-staggered structure shows a smaller r_{ch} than inverted-coplanar device. For inverted-coplanar structure, the surface of the gate dielectric is damaged by the RF sputtering during the S/D electrodes deposition. This damage induces the defect creation at the dielectric/semiconductor interface and increases r_{ch}. Therefore, the preferable dielectric/semiconductor interface for inverted-staggered structure also leads the device to exhibit improved performance.



(a) (b)

Fig. 4-3 Schematic cross-sectional diagram of the total TFTs ON-resistance in a-IGZO TFTs with (a) inverted-staggered and (b) inverted-coplanar structures

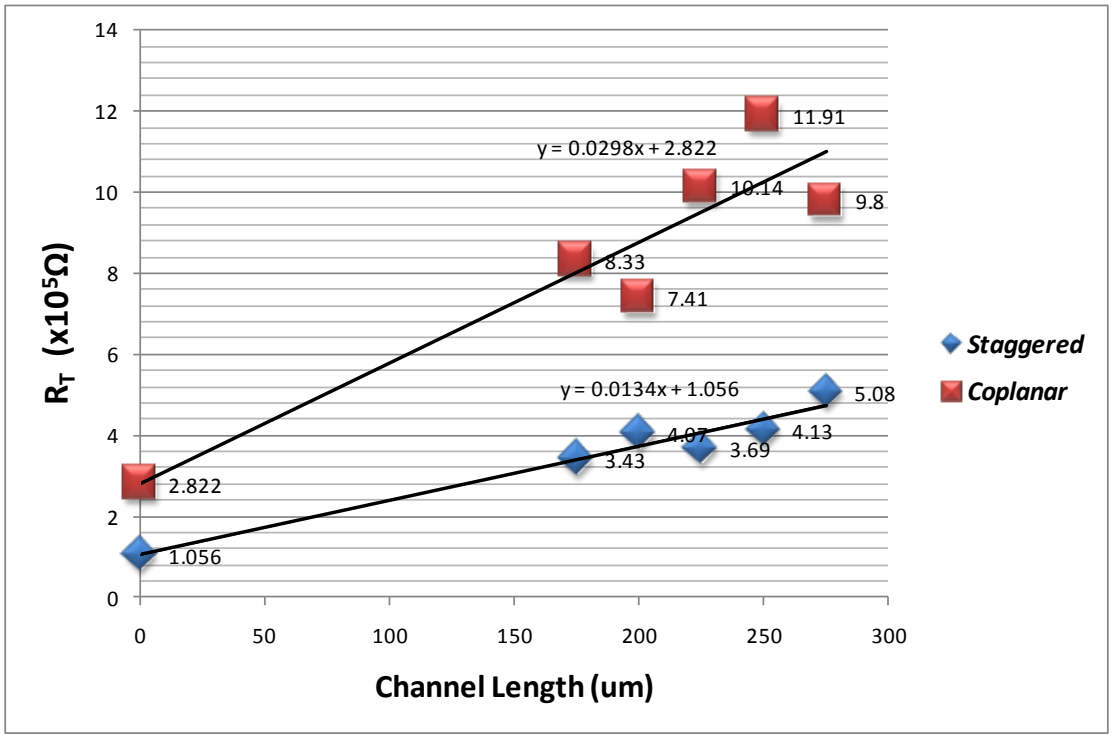


Fig. 4-4 Total TFTs ON-resistance as a function of the channel length at V_{GS}=26V for inverted-type staggered and coplanar structures of a-IGZO TFTs with ITO electrodes

4.5 Dielectric/Channel Interface Trap Density

The trap density in a-IGZO TFTs affects the electrical characteristics of transistor into non-ideal condition. Therefore, the effect of trap density is a concerned issue. In this thesis, we employ a C-V measurement and an equivalent trap density (N_t) equation to analyze and extract the effect of trap density at the dielectric/channel interface.

4.5.1Capacitance-Voltage Characteristic

The C-V method to detect the trap density is operated in a low measurement frequency to get a thermal equilibrium condition where the spatial profile of the electric potential and carrier density in the active layer is uniform and the trapping ratio is saturated [34]. Fig. 4-5 shows the measurement results of the C-V for inverted-staggered and inverted-coplanar TFTs at applied frequency of 10kHz, respectively. It is observed that $C_{g(s+d)}$ becomes smaller at negative V_{GS} due to that the electrons are depleted in the a-IGZO thin films. In the positive V_{GS} region, the $C_{g(s+d)}$ becomes larger as the increasing of V_{GS} because the electrons in the a-IGZO thin films are accumulated at the front channel.

In estimating the capacitance of the devices, the interface trapped charges are usually neglected. In fact, the interface trapped charges between the dielectric and active layer affect the capacitance. The interface trapped charges create an interface-trap capacitance (C_{it}), and the C_{it} connects to the silicon oxide capacitance (C_{ox}) in series, as shown in Fig. 4-6. Therefore, the existence of C_{it} decreases the whole capacitance of a device. In contrast, the inverted-coplanar structure exhibits higher total capacitances than the inverted-staggered structure. Because the capacitances are in series connection, the higher total capacitances indicate the larger series C_{it}. Thus, it is reasonable to assume that the inverted-staggered structure has minor interface trapped charges effect.

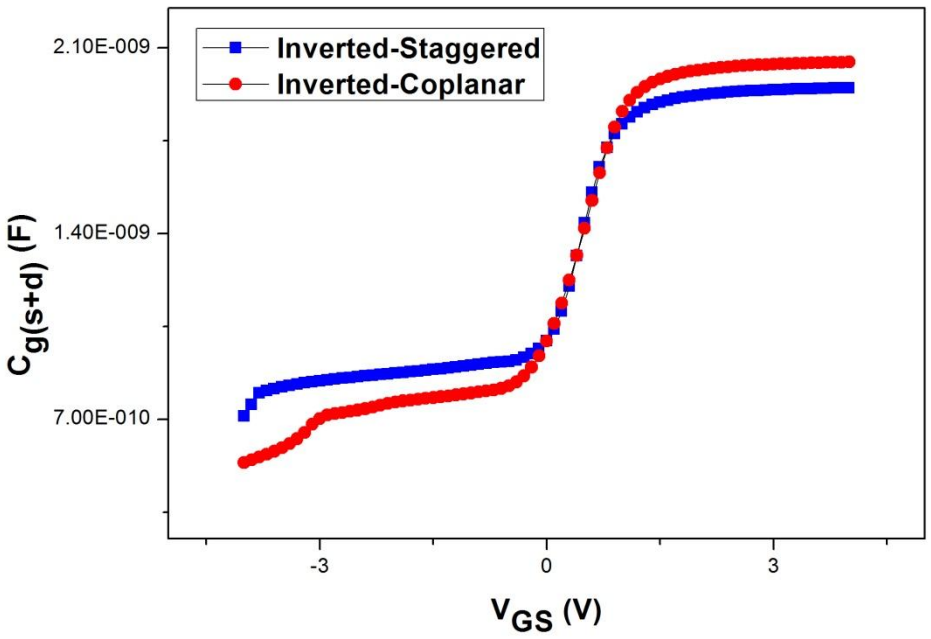


Fig. 4-5 Measured results of C-V characteristics of inverted-staggered and inverted-coplanar structures

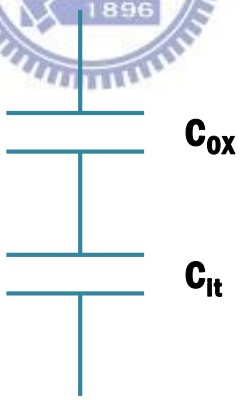


Fig. 4-6 Existence of the C_{it} results in series connection and reduces the whole capacitance

4.5.2 Equivalent Trap Density

The variation of sub-threshold slope may be due to the higher density of traps contained in the dielectric layer. Near the interface of dielectric and active layer, the traps would trap or scatter the carriers in the front channel region. To determine the trap density at the interface of dielectric/channel, an equivalent trap density (N_t) method [35] is adopted and extracted from the S value using the following equation:

$$N_t = \left(\frac{S}{2.3 k_B T / q} - 1 \right) \frac{C_i}{q} \qquad (4\text{-}1)$$

where k_B denotes the Boltzmann constant, T the temperature, q the elementary electric charge, and C_i the capacitance per unit area of the gate dielectric. The extracted N_t are about $3.08 \times 10^{16} cm^{-2}/eV$ and 5.29×10^{16} cm^{-2}/eV for inverted-staggered and inverted-coplanar structures, respectively. The surface of the gate dielectric layer is damaged by the RF sputtering of S/D electrodes for inverted-coplanar structure. Hence, the inverted-coplanar has more trap defects at the dielectric/channel interface and the result is consistent with the C-V characteristic.

Furthermore, the interface traps trap the carriers on dielectric/channel interface in the TFTs operation and it decreases the migration ability of the carriers in the front channel. As a result, the inverted-staggered structure with minor interface trapping effect reveals higher mobility than inverted-coplanar device. Meanwhile, the interface traps also behave like the internal

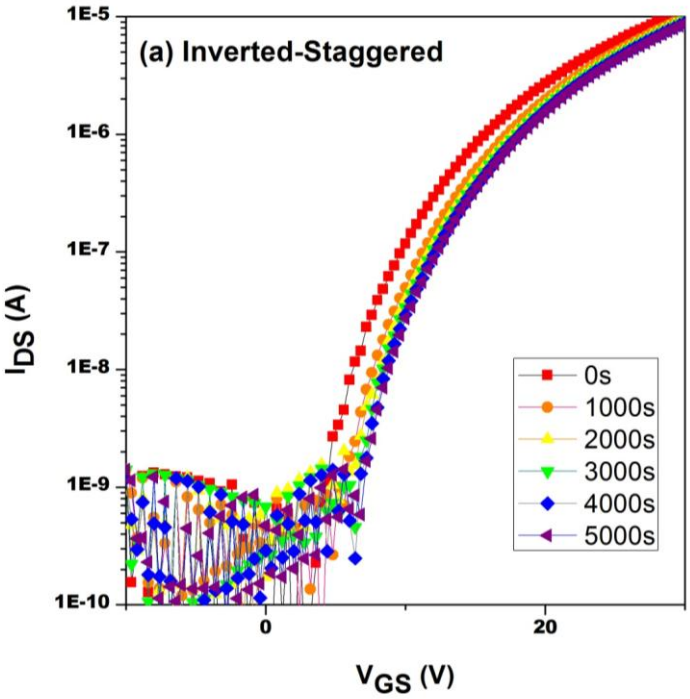
positive charges and these traps attract the electrons in semiconductor to accumulate in the front channel when there is no applied voltage. Therefore, the inverted-coplanar TFTs exhibit smaller turn-on voltage than those of inverted-staggered devices.

4.6 Stability of Geometry Structures

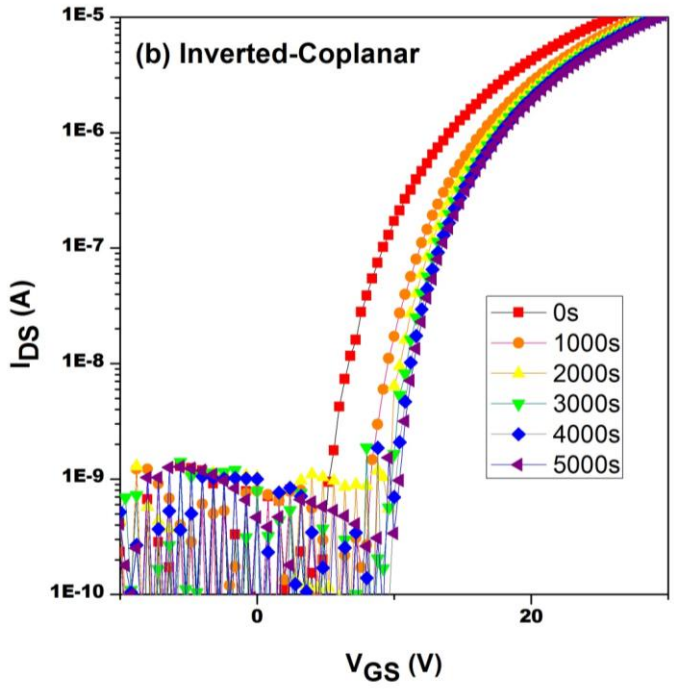
The TFTs electrical stability is a key issue in device applications. The bias induced V_{th} shift limits the application of a-IGZO TFTs especially critical in the case of current driven OLED displays because it leads to variations in the respective pixel brightness. Therefore, a DC bias stressing is adopted to examine the bias induced instability on V_{th} shift in geometry structures of a-IGZO TFTs.

4.6.1 Transfer Characteristic under Bias Stressing

To characterize the stable performances of inverted-staggered and inverted-coplanar structures, the DC bias stressing is adopted to investigate the geometry effect of a-IGZO TFTs. V_{GS}=V_{DS}=20V of bias voltage, 5000 seconds of stressing time, and Δt=1000s of interval are chosen for stressing conditions. The periodic measurements of the V_{th} under DC bias stressing for inverted-staggered and inverted-coplanar structures are shown in Fig. 4-7. The comparison of V_{th} shift are 2.5V and 4.8V of 5000s stressing time for inverted-staggered and inverted-coplanar, respectively.



(a)



(b)

Fig. 4-7 Transfer curves of a-IGZO TFTs as a function of DC bias stressing for (a) inverted-staggered and (b) inverted-coplanar structures

4.6.2 Discussion

Previous studies [36-37] reported that the dominant mechanism in the V_{th} shift under bias stressing is the interface charge trapping effect between active layer and gate dielectric. In the TFTs operation, the interface trapped electrons form the screening effect so that the effective gate voltage is smaller than actually applied gate voltage. Fig. 4-8 shows the corresponding variation of the V_{th} shift in different device structures. In the device deposition procedures, the electrodes of inverted-coplanar TFTs were deposited earlier than the channel layer, therefore the reserved dielectric region for the channel was bombarded from the sputtering. This plasma bombardment produced excess interface charge trapping on the dielectric/channel surface which deteriorated the performances of TFTs. In the C-V characteristic, the inverted-coplanar is also confirmed that serious C_{it} effect is existed in this kind of configuration. The electrical stability is considered strongly depending on the dielectric/channel interface properties in TFTs, consequently the inverted-coplanar TFTs have obvious degraded performances compared to the inverted staggered devices under DC bias stressing.

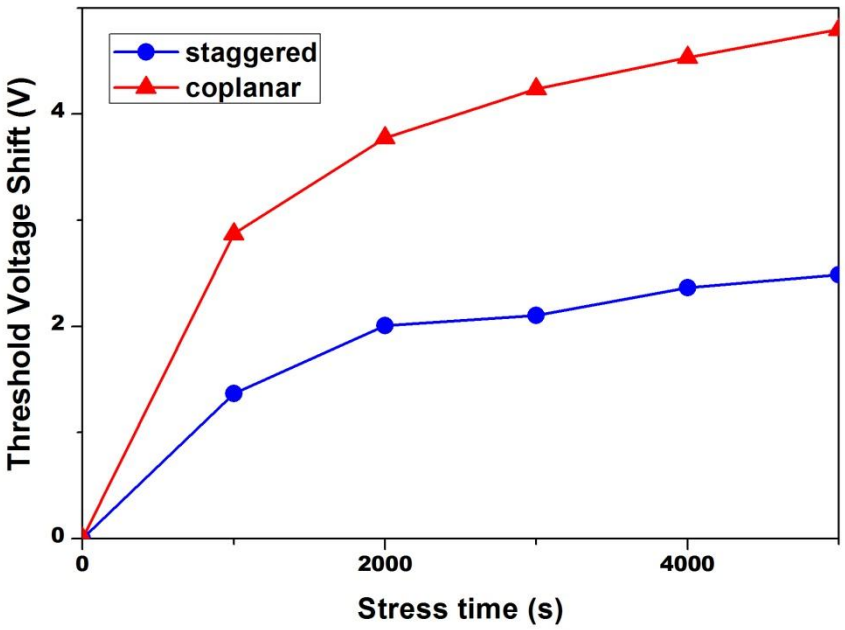


Fig. 4-8 Time dependence of ΔV_{th} in geometry structures

4.7 Surface States Simulation

As mentioned before, the a-IGZO film of the inverted-coplanar device was deposited after patterning the S/D electrodes. This procedure elicits the change of surface states at the interface of channel and gate dielectric. Among the variation of surface states, a main change is the interface trap density between active layer and gate dielectric. Besides, the point defects will increase the bulk DOS at or near the semiconductor/gate insulator surface. Because the variation of the transfer curves is strongly affected by the surface state effect, the quantification of surface states is essential.

4.7.1 Interface Trap Density and Acceptor-Like DOS

The interface charge effect and variation of DOS are modeled by a simulation tool (ATLAS). The physical based model of a-IGZO TFTs can reproduce accurate output, transfer and sub-threshold characteristics. By fitting the transfer characteristic of the simulation with the experimental results, the interface charge density is set as 10^{16} and $10^{25}cm^{-2}eV^{-1}$ for inverted-staggered and inverted-coplanar structures, respectively. Meanwhile, a large number of acceptor-like DOS in inverted-coplanar structure is observed during the simulation. From the experimental results, the inverted-staggered TFTs exhibit better inverse slope in the sub-threshold region. In order to adjust the transfer characteristic of the simulation to conform to the experiment, the inverted-staggered shows smaller peak value of acceptor-like DOS ($8\times10^{12}cm^{-3}eV^{-1}$) than inverted-coplanar ($7\times10^{17}cm^{-3}eV^{-1}$) in the setting of simulation. Therefore, the parameter of acceptor-like DOS in the a-IGZO active layer is considered the origin of the sub-threshold slope.

As shown in Fig. 4-9, the linear transfer I_{DS}-V_{GS} curves from simulation agree well with experiments. The simulation results indicate that the dominant surface state mechanism for the degradation of sub-threshold swing is the increase of acceptor-like DOS near the conduction band of the a-IGZO TFTs. Because the point defect is caused by the sputtering of S/D electrodes, the severe interface charge density and acceptor-like DOS are existed in the

inverted-coplanar structure. The parameters of the surface states and simulation in ATLAS are listed in Tab. 4-3 and Tab. 4-4, respectively.

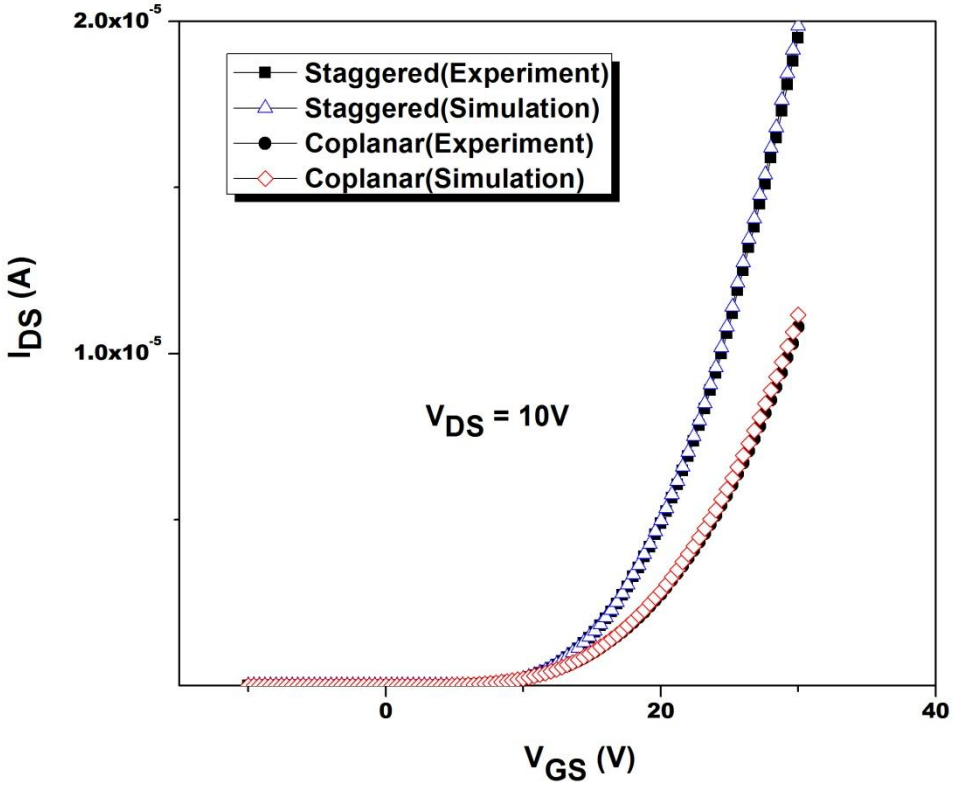


Fig. 4-9 Linear I_{DS}-V_{GS} characteristic of simulation and experimental results

Tab. 4-3 Simulation of Surface States of a-IGZO TFTs for different structures

Structure	Interface Charge Density ($cm^{-2}eV^{-1}$)	Peak Value of Acceptor-like DOS ($cm^{-3}eV^{-1}$)
Inverted Staggered	**$1x10^{16}$**	**$8x10^{12}$**
Inverted Coplanar	**$1x10^{25}$**	**$7x10^{17}$**

Tab. 4-4 Device Simulation Parameters in ATLAS

	parameter	Symbol	value	Unit	description
gate	k		4.1		gate electrode
dielectric	SiO_2 THK		100	nm	thickness
	k		3.9		dielectric constant
electrode	ITO		4.65		workfunction / Universal schottky tunneling model ohmic contact with resistance
IGZO	NTA	g_{ta}	$6.5x10^{20}$	cm^{-3}	density of state at $E_T=E_C$
(ATLAS DOS setting)	NTD	g_{td}	$1x10^{21}$	cm^{-3}	density of state at $E_T=E_V$
	NGA	d_a	$8x10^{12}$	cm^{-3}	peak value of gaussian-distributed acceptor-like deep-gap states
	NGD	d_d	$1x10^{16}$	cm^{-3}	peak value of gaussian-distributeddonor-like deep-gap states
	EGA	λ_a	0.1	eV	mean value of gaussion-distributed acceptor-like deep-gap states
	EGD	λ_d	0.1	eV	mean value of gaussion-distributed donor-like deep-gap states
	WTA	E_a	0.015	meV	conduction-band-tail slope
	WTD	E_d	0.12	meV	valence-band-tail slope
	WGA	σ_a	0.05	eV	variance of gaussion-distributed acceptor-like deep-gap states
	WGD	σ_d	0.1	eV	variance of gaussion-distributed donor-like deep-gap states
	SIGTAE		$1x10^{-17}$	cm^2	electron capture cross-section for the acceptor tail
	SIGTDE		$1x10^{-15}$	cm^2	electron capture cross-section for the donor tail
	SIGGAE		$2x10^{-16}$	cm^2	electron capture cross-section for the gaussion acceptor states
	SIGGDE		$2x10^{-15}$	cm^2	electron capture cross-section for the gaussion donor states
	SIGTAH		$1x10^{-15}$	cm^2	hole capture cross-section for the acceptor tail
	SIGTDH		$1x10^{-17}$	cm^2	hole capture cross-section for the donor tail
	SIGGAH		$2x10^{-15}$	cm^2	hole capture cross-section for the gaussion acceptor states
	SIGGDH		$2x10^{-16}$	cm^2	hole capture cross-section for the gaussion donor states
IGZO	Nc		$6.5x10^{20}$	cm^{-3}	conduction band carrier concentration
	Nv		$1x10^{22}$	cm^{-3}	valance band carrier concentration
	Eg		3.20	eV	bang gap
	Ne				carrier concentration
	ϕ		4.6		affinity
	μ_n		15.11	cm^2/Vs	band mobility n
	μ_p		0.1	cm^2/Vs	band mobility p
	mc		0.3		conduction band effective mass
	t		40	nm	film thickness

4.7.2 Discussions

There are several researches use simulation tools to model the characteristics of a-IGZO TFTs and their DOS. The donor-like and acceptor-like states are usually utilized to describe the density of states at band edge. The simulation technique can be a useful tool for investigating the device operation and physical properties. In this study, we use the ATLAS simulation to analyze the characteristics of a-IGZO TFTs in inverted-staggered and inverted-coplanar structures and integrate with the contact resistance and C-V characteristic. Comparison of the studies with inverted-staggered and inverted-coplanar structures is shown in Tab. 4-5.

Tab. 4-5 Comparison of the studies with inverted-staggered and inverted-coplanar structures

	NCTU'11	*SID 2010 LG Display*
TFT Structures	inverted-staggered & inverted-coplanar	inverted-staggered & inverted-coplanar
Active Layer Deposition Method	Sputtering	Solution
Stressing Condition	DC Stressing	DC Stressing
Quantification of Surface States	Simulation	None
Analysis Method	**Contact Resistance + CV Characteristic + ATLAS Simulation**	Contact Resistance

4.8 Summary

The electrical properties and stability of inverted-staggered and inverted-coplanar TFTs are presented and discussed. The inverted-staggered TFTs exhibit improved performance such as mobility, I_{on}/I_{off}, and S value due to the lower contact resistance and less surface state effects. Under the bias stressing, the V_{th} shift of inverted-staggered and inverted-coplanar TFTs are 2.5 and 4.8V, respectively. Because the charge trapping effect in the interface of dielectric/channel with an inverted-coplanar structure is more severe, the inverted-staggered TFTs exhibit improved device stability. To quantitate of surface states, the ATLAS simulation shows that the inverted-staggered structure has smaller interface charge density and acceptor-like DOS due to the preferable dielectric/semiconductor interface.

Chapter 5

Conclusions and Future Works

5.1 Conclusions

The surface state and geometry effects are investigated and compared by introducing the inverted-staggered and inverted-coplanar device structures. In contrast, the inverted-staggered TFTs show a μ_{FE} of 8.29cm^2/Vs, a S value of 0.91V/decade, and a I_{on}/I_{off} of 4.21×10^6. These improved performances are attributed to the lower contact resistance, less interface trap density, and acceptor-like DOS. The interface traps behave like the internal positive charges and attract the electrons in semiconductor to accumulate when there is no applied voltage. Therefore, the V_{th} for inverted-staggered and inverted-coplanar structures are 3.96V and 1.61V, respectively.

The inverted-coplanar structure shows a serious deterioration in V_{th} shift under bias stressing which is attributed to the charge trapping at the interface between gate dielectric and channel layers. The dominant mechanism of S value degradation is the increase of acceptor-like DOS in the active layer. The decay of device performance implies that the surface states effects in the inverted-coplanar structure are more severe. The interface traps

and acceptor-like DOS in inverted-staggered and inverted-coplanar structures are quantitated by the ATLAS simulation. The interface charge density and acceptor-like DOS for inverted-staggered structure are $10^{16}cm^{-2}eV^{-1}$ and $8\times10^{12}cm^{-3}eV^{-1}$, respectively, and $10^{25}cm^{-2}eV^{-1}$ and $7\times10^{17}cm^{-3}eV^{-1}$ for inverted-coplanar structure, respectively. A list of parameters for representative TFTs is summarized in Tab. 5-1.

In our research, we integrated the contact resistance method, C-V characteristic, and ATLAS simulation to evaluate the surface state and geometry effects. This study has shown that the inverted-staggered structure with improved mobility, sub-threshold swing, I_{on}/I_{off}, and bias stress stability is a promising configuration for a-IGZO TFTs.

Tab. 5-1 Comparison of the electrical properties, stability, and surface states of inverted-staggered and inverted-coplanar structures, respectively

Structure	Inverted Staggered	Inverted Coplanar
μ_{FE} (cm^2/Vs)	8.29	5.97
V_{th} (V)	3.96	1.61
S (V/decade)	0.91	1.52
I_{on}/I_{off}	$4.21x10^6$	$1.34x10^6$
Contact Resistance (Ω)	$1.06x10^5$	$2.82x10^5$
ΔV_{th} (V) ($@V_{GS}=V_{DS}=20V$, 5000s)	2.5	4.8
Interface Charge Density ($cm^{-2}eV^{-1}$)	$1x10^{16}$	$1x10^{25}$
Peak Value of Acceptor-like DOS ($cm^{-3}eV^{-1}$)	$8x10^{12}$	$7x10^{17}$

5.2 Future Works

5.2.1 Homojunction Structure

To further improve the device performance, we focus on the inverted-staggered structure and try to fabricate a homojunction between the active layer and S/D electrodes. For the application of a-IGZO TFTs to active-matrix backplanes, there are still issues to be solved. One of the essential issues is that it is difficult to form good electrical contacts between the a-IGZO channel and S/D electrodes. Previous study reported that a highly conductive a-IGZO buffer layer helped to form a good ohmic contact between the a-IGZO channel and S/D electrodes [38-39]. The TFTs performance varies with the contact resistance between a-IGZO and S/D metals. Therefore, it is necessary to increase the carrier concentration at the contact interface of the a-IGZO layer by depositing a highly conductive a-IGZO buffer layer in order to obtain a good ohmic contact.

Fig. 5-1 shows the fabrication flowchart of the further improvement. The first step is patterned the SiO_2 channel protection before the deposition of SiN_X barrier layer. The SiN_X deposition induces the hydrogen effect onto the area of the a-IGZO layer without the SiO_2 channel protection and forms a highly conductive a-IGZO layer. The highly conductive a-IGZO region is contacted to the a-IGZO channel in plane and acted as the S/D. This fabrication process not requires expensive doping techniques such as ion implantation or

diffusion of impurities. Sato et al. reported that contact resistance was improved about 30% by a similar homojunction structure and the TFTs exhibited good performances such as μ_{FE}=9.5cm^2/Vs, V_{th}=0.13V, and S=0.13Vdecade^{-1} [40]. The proposed structure and fabrication process can solve the contact issue between the metal and semiconductor materials and then achieve a high performance a-IGZO TFTs.

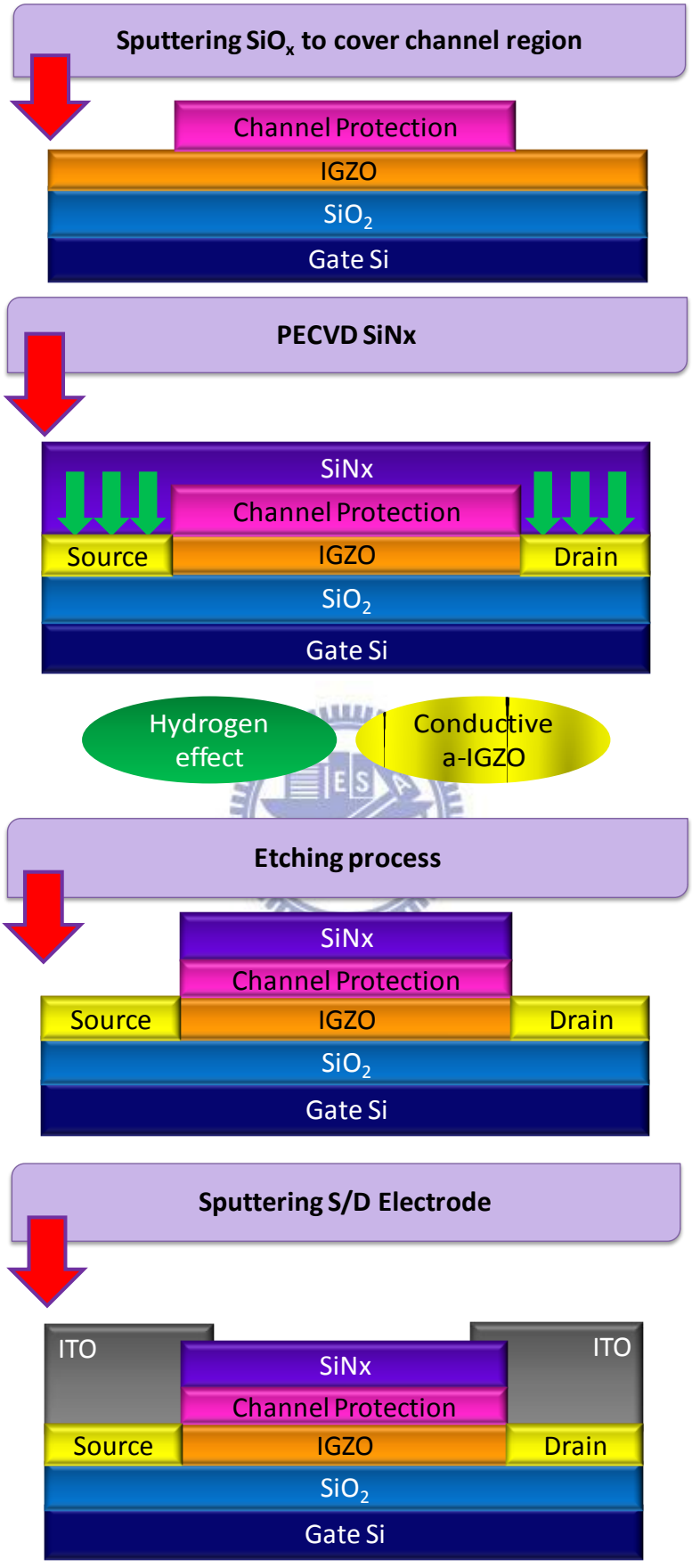


Fig. 5-1 Deposition flowchart of the further improvement

5.2.2 a-IGZO Thin Films

Because the IGZO is an In_2O_3-Ga_2O_3-ZnO ternary system, the thin film properties greatly depend on its chemical composition. However, it is hard to maintain the proportion of the In_2O_3, Ga_2O_3, and ZnO for each area in the fabrication process. Besides, the electron transport mechanism of the IGZO is attributed to the oxygen vacancies. Therefore, the difficult control of the metal oxide content indicates that it is hard to estimate the quantity of oxygen vacancies in the IGZO thin films.

To improve the uniformity of the TFTs characteristics, we will further study the wet O_2 annealing. For the a-IGZO thin films, the absorption of oxygen at the backchannel can affect the oxygen vacancies in the thin films. The adsorbed oxygen will fill in the oxygen vacancies and capture electrons as shown in Fig. 5-2. This implies that the wet O_2 annealing is more effective to reduce the oxygen deficiencies than the annealing at air or N_2 atmosphere. Overall, the wet O_2 annealing is a good topic for attaining the equal oxygen vacancies in large deposition area that can improve the uniformity of a-IGZO TFTs characteristics.

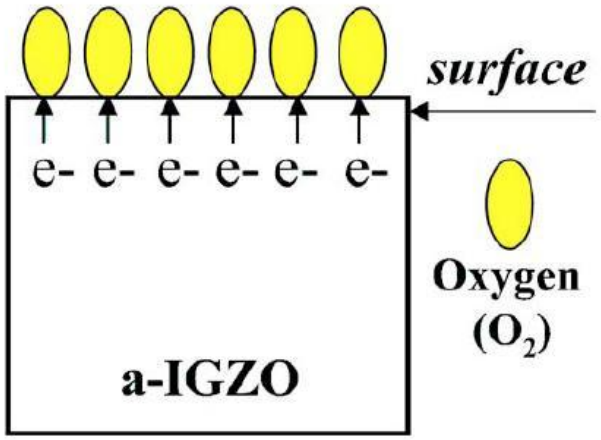


Fig. 5-2 The schematic diagram showing the role of oxygen as an electron acceptor onto a-IGZO surface [26]

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