The Lambda Bipolar Phototransistor—Analysis and Applications

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Abstract —An analytic model for the I-V characteristic of the lambda bipolar phototransistor (LBPT) is developed in which the characteristic parameters, such as the peak voltage, peak current, differential negative resistance, valley voltage, and valley current, are expressed in terms of the known device parameters and photocurrent. It is shown that the valley current of the new device in the dark is much smaller than the saturation dark current of the conventional bipolar phototransistor and the differential negative resistance region can be varied for wide range by controlling the fabrication processes. Comparisons between the characteristics of the fabricated devices and the developed model have been made and satisfactory agreement has been obtained. Moreover, some interesting applications of this new device in photodetection are also presented and discussed. In addition, the frequency limit of the LBPT and the improvement methods are also discussed.

I. Introduction

THERE ARE several kinds of semiconductor photodetectors, such as photoconductor, photodiodes, phototransistors, and charge-couple device, available in commercial for optical signal detection. All of these devices are based on the principle that one of their electrical parameters, such as conductivity, voltage, current, or stored charges, may vary with the spectral intensity of the incident light. Recently, a new photodevice—the lambda bipolar photo-transistor (LBPT)—has been proposed by Wu et al. [1], which will exhibit the voltage-controlled differential negative resistance characteristic when this device is exposed to light. The basic integrated structure of the LBPT consists of a simultaneous integration of an n(p)channel enhancement mode MOSFET and a merged n-p-n (p-n-p) bipolar phototransistor, which is identical to that of the lambda bipolar transistor (LBT) originally proposed by Wu et al. [2] except that no base driving current is needed for the LBPT and design considerations are slightly different.

In this paper, a quantitative analysis for the I-V characteristic of the LBPT is presented, which is very essential for us to understand the physical operation and photocharacteristics of the LBPT and, further, to design a suitable LBPT for circuit applications. Based on the developed analytic model, the important characteristic parameters of the LBPT, such as the peak voltage, peak current, photoinduced differential negative resistance, valley voltage, and valley current, are analytically expressed in terms of the

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known device parameters and photocurrent. Design considerations and fabrication techniques are also discussed by using the developed model. Moreover, comparisons between the developed model and the experimental results of the fabricated LBPT's are also made and satisfactory agreement between these comparisons has been obtained. In order to show the applicability of this new device, some rather interesting applications of the LBPT are presented and discussed.

II. THEORETICAL ANALYSIS

The basic integrated structure of an n-p-n LBPT is shown in Fig. 1(a) where an n-channel enhancement-mode MOSFET is fabricated in the base region of the n-p-n bipolar transistor, the base region of the n-p-n bipolar phototransistor serves as the substrate of the n-channel MOSFET, and the emitter region of the bipolar transistor serves as the source region of the n-MOSFET. Furthermore, the gate and collector, and the drain and the base are electrically connected by metallization, respectively. The equivalent circuit of an n-p-n LBPT device is shown in Fig. 1(b) and the I-V characteristic of an n-p-n LBPT device under a constant illumination is shown in Fig. 2. According to the operating points of the separate devices, the I-Vcharacteristic curve can be divided into five regions as indicated in Fig. 2. In order to simplify the analysis, the terminal characteristics of the bipolar phototransistor can be written as [3]

$$I_{E} = I_{ES} \left[\exp \left(\frac{qV_{BE}}{k_{B}T} \right) - 1 \right]$$

$$- \alpha_{I} I_{cs} \left[\exp \left(\frac{qV_{BC}}{k_{B}T} \right) - 1 \right]$$

$$I_{C} = - I_{cs} \left[\exp \left(\frac{qV_{BC}}{k_{B}T} \right) - 1 \right]$$

$$+ \alpha_{N} I_{ES} \left[\exp \left(\frac{qV_{BE}}{k_{B}T} \right) - 1 \right] + I_{PH}$$
(2)

where $I_{ES}(I_{cs})$ is the reverse saturation current of the emitter (collector) junction with the collector (emitter) electrode shorted to the base electrode; $\alpha_I(\alpha_N)$ is the inverse (normal) current gain in the common-base configuration; and I_{PH} is the photocurrent across the base-collector photodiode. Note that the second-order effects of the bi-

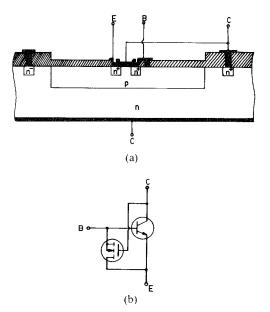


Fig. 1. (a) Schematic structure for the n-p-n LBPT. (b) The equivalent circuit.

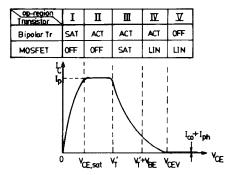


Fig. 2 The I-V characteristic of the n-p-n LBPT under a constant illumination and the operating region of each constituent device.

polar phototransistor, such as the Early effect and high current effects, are all neglected for simplicity.

The I-V characteristic of the n-channel MOSFET can be approximately expressed by

$$I_{D,NS} = \beta_M \left[(V_{GS} - V_T') V_{DS} - \frac{1}{2} V_{DS}^2 \right],$$
for nonsaturation region (3)
$$I_{D,S} = \frac{\beta_M}{2} (V_{GS} - V_T')^2,$$
for saturation region (4)

where $\beta_M = (W/L)C_o\mu_n$ is the gain factor of the n-channel MOSFET; L is the channel length; W is the channel width; C_o is the gate oxide capacitance per unit area; μ_n is the electron mobility in the surface inversion layer; and V_T' is the threshold voltage of the n-channel MOSFET with an applied substrate bias V_{DS} , which can be expressed by

$$V'_{T} = \phi_{Ms} + 2|\phi_{fp}| - \frac{Q_{ss}}{C_{o}} + \frac{1}{C_{o}} \left[2K_{s}\epsilon_{o}qN_{AS}(2|\phi_{fp}| - V_{DS}) \right]^{1/2}$$
 (5)

where ϕ_{Ms} is the metal-semiconductor work function difference: ϕ_{fp} is the potential difference between the Fermi level and the intrinsic Fermi level in neutral substrate; $K_s \epsilon_o$ is the permittivity of the semiconductor; N_{As} is the surface doping concentration of the base diffusion; and Q_{ss} is the interface fixed-charge density of the MOS gate. Note that the short channel effect and subthreshold leakage current are all neglected for simplicity.

For the interconnection shown in Fig. 1(a), we have $V_{Ds} = V_{BE}$ and $V_{Gs} = V_{CE}$. Based on the above simplified expressions, the I-V characteristic of the LBPT device can be derived as follows.

Region I: When the emitter-collector voltage V_{CE} is smaller or equal to the saturation voltage $V_{CE,sat}$ of the bipolar phototransistor, the bipolar phototransistor is in saturation and the n-channel MOSFET is off. The I-V characteristic may be obtained from (1) and (2) and is written as

$$V_{CE} = V_t \ln \left| \frac{I_{cs} [I_c (1 - \alpha_I) + \alpha_I I_{PH}]}{I_{Es} [I_{PH} - I_C (1 - \alpha_N)]} \right| + I_c (\gamma_{sE} + \gamma_{sc}) \quad (6)$$

where γ_{sE} and γ_{sc} are the series resistances of the emitter and collector regions, respectively; V_t is the equivalent thermal voltage, $V_t = k_B T/q$.

Region II: When $V_{CE,sat} < V_{CE} < V_T'$, the n-channel MOSFET is still in the cutoff region, but the bipolar phototransistor is operated in the active region. The collector current in this case can be calculated and is expressed as

$$I_c = (1 + \beta_N)(I_{co} + I_{PH}) \tag{7}$$

where $\beta_N = \alpha_N/(1-\alpha_N)$; I_{co} is the reverse saturation current of the collector junction with the emitter open-circuited, which is equal to $I_{cs}(1-\alpha_I\alpha_N)$.

Similarly, the emitter-base voltage V_{BE} can be expressed by

$$V_{BE} = V_t \ln \left[\frac{(1 + \beta_N)(I_{co} + I_{PH})}{I_{ES}} \right] = V_{Ds}.$$
 (8)

Note that V_{BE} in (8) is a function of illumination, and in this region $I_c = I_p$, $V_{BE} = V_{BEP}$.

Region III: When V_{CE} exceeds V_T' , the n-channel MOSFET will be operated in the saturation region because the channel near the drain is pinched off. The upper limit of this region is given by the onset voltage of strong inversion near the drain, i.e., $(V_T' + V_{RE})$.

The current-voltage characteristic in this region can be solved by the following simultaneous equations:

$$I_{D,S} = \frac{\beta_M}{2} (V_{CE} - V_T')^2$$

$$V_T' = \phi_{MS} + 2|\phi_{fp}| - \frac{Q_{ss}}{C_o}$$

$$+ \frac{1}{C_o} \left[2K_s \epsilon_o q N_{AS} (2|\phi_{fp}| - V_{BE}) \right]^{1/2}$$
(10)

$$V_{BE} = V_{t} \ln \left[\frac{(1 + \beta_{N})(I_{co} + I_{PH} - I_{D,S})}{I_{ES}} \right]$$
(11)

$$I_c = (1 + \beta_N)(I_{PH} + I_{co}) - \beta_N I_{D,S}.$$
 (12)

It is clearly seen that using (9) and (11), V_T' in (10) can be solved for any given V_{CE} by using the iterative method. Then, the output current-voltage characteristic in this region can be expressed as

$$I_c = (1 + \beta_N)(I_{PH} + I_{co}) - \frac{\beta_N \beta_M}{2} (V_{CE} - V_T')^2.$$
 (13)

Note that V_T' is increased with increasing V_{CE} , so I_c in (13) is decreased much slower than the square law. The differential negative resistance in this region can be easily obtained by (13) and is expressed as

$$R_{N} = -\left[\beta_{N}\beta_{M}(V_{CE} - V_{T}')\left(1 - \frac{dV_{T}'}{dV_{CE}}\right) + \frac{\beta_{N}}{2}(V_{CE} - V_{T}')^{2}\frac{d\beta_{M}}{dV_{CE}}\right]^{-1}.$$
 (14)

In general, the electron mobility in the inversion layer is a function of the applied gate voltage, which can be expressed by

$$\mu_n = K(V_{CE} - V_T')^{-r} \tag{15}$$

where K and r are the empirical constants which can be determined experimentally.

Using (15) the differential negative resistance in (14) can be further simplified and is expressed as

$$R_{N} = -\left[\beta_{N}\beta_{M}(V_{CE} - V_{T}')\left(1 - \frac{dV_{T}'}{dV_{CE}}\right)\left(1 - \frac{r}{2}\right)\right]^{-1}$$
 (16)

where

$$\frac{dV_{T}'}{dV_{CE}} = \left[1 + \left(\frac{2C_{o}}{V_{t}\beta_{M}} \right) \left(\frac{2|\phi_{fp}| - V_{BE}}{2K_{s}\epsilon_{o}qN_{As}} \right)^{1/2} \cdot \frac{\left(I_{co} + I_{PH} - I_{D,S} \right)}{\left(1 - \frac{r}{2} \right) (V_{CE} - V_{T}')} \right]^{-1} .$$
(17)

Note that r < 0 and $dV_T'/dV_{CE} < 1$, so that the differential negative resistance always exists in the region.

Region IV: When $V_{CE} > V_T' + V_{BE}$, the n-channel MOSFET is operated in the nonsaturation region. The current-voltage characteristic in this region can be obtained by solving the simultaneous equations as the method described in Region III except that (9) is replaced by the expression in the nonsaturation region. The drain current in nonsaturation region can be written as

$$I_{D, Ns} = \beta_M \left[(V_{CE} - V_T') V_{BE} - \frac{1}{2} V_{BE}^2 \right]$$
 (18)

and the collector current in this region can also be written

$$I_{c} = (1 + \beta_{N})(I_{co} + I_{PH}) - \beta_{N}\beta_{M}[(V_{CE} - V_{T}')V_{BE} - \frac{1}{2}V_{BE}^{2}].$$
 (19)

Similarly, the differential negative resistance in this region can be calculated by (19). After some algebra manipulations and rearrangements we can easily obtain the following compact form:

$$R_N =$$

$$-\frac{1+\frac{\beta_{M}V_{t}(V_{cE}-V_{T}'-V_{BE})}{(I_{co}+I_{PH}-I_{D,Ns})}}{\beta_{N}\beta_{M}\left(1-\frac{dV_{T}'}{dV_{CE}}\right)\left[(1-r)V_{BE}+\frac{r}{2}(V_{CE}-V_{T}')^{-1}V_{BE}^{2}\right]}$$
(20)

where

$$\frac{dV_T'}{dV_{CE}} = \left[1 + \left(\frac{2C_o}{V_t \beta_M}\right) \left(\frac{2|\phi_{fp}| - V_{BE}}{2K_s \epsilon_o q N_{As}}\right)^{1/2}\right]$$

$$\frac{\left(I_{co} + I_{PH} - I_{N,Ds}\right) + V_{t}\beta_{M}(V_{CE} - V_{T}' - V_{BE})}{(1 - r)V_{BE} + \frac{r}{2}(V_{CE} - V_{T}')^{-1}V_{BE}^{2}}\right]^{-1}.$$
 (21)

Note that $R_N < 0$ is always valid in this region because $I_{co} + I_{PH} > I_{D,Ns}$ and $dV_T'/dV_{CE} < 1$. However, when the condition $I_{co} + I_{PH} = I_{D,Ns}$ is satisfied, R_N becomes an infinity, then the slope (dI_c/dV_{CE}) becomes zero. This condition implies that the current across the collector junction is completely taken out by the n-channel MOSFET and does not pass through the emitter-base junction to obtain the current amplification. It is quite interesting that when the illumination is off, the reverse saturation current across the collector junction I_{co} is forced to pass through the n-channel MOSFET, so the total leakage current of the LBPT is only equal to I_{co} which is much smaller than that of the conventional bipolar phototransistor by a factor $(1+\beta_N)$. This remarkable feature enables the LBPT to be operated with extremely low standby power.

Region V: When $V_{CE} > V_{CEV}$, the n-p-n bipolar transistor is in the cutoff region, and the n-channel MOSFET is operated in the nonsaturation region, then the collector current will be equal to the sum of the reverse saturation current of the collector junction with the emitter opened and the photoinduced current, i.e., $I_c = I_{co} + I_{PH}$. From the moment that the n-p-n bipolar transistor is in the cutoff region, the collector current will be equal to the drain current I_D in the nonsaturation region, i.e.,

$$I_{D} = \beta_{M} \left[(V_{CE} - V_{T}') V_{BE} - \frac{1}{2} V_{BE}^{2} \right]$$

$$= I_{co} + I_{PH}. \tag{22}$$

Based on the derived condition, i.e., $I_{co} + I_{PH} = I_{D, Ns}$, we may easily define the valley voltage of the LBPT. Using (18), (15), and (10) the valley voltage can be calculated and is expressed by

$$V_{CEV} = \left[\frac{L(I_{co} + I_{PH})}{WC_o V_{BE, \text{cut-in}}} + \frac{1}{2} V_{BE, \text{cut-in}} \right]^{1/(1-r)}$$

$$+ \phi_{Ms} + 2|\phi_{fp}| - \frac{Q_{ss}}{C_o}$$

$$+ \frac{1}{C_o} \left[2K_s \epsilon_o q N_{As} \left(2|\phi_{fp}| - V_{BE, \text{cut-in}} \right) \right]^{1/2}. \quad (23)$$

If the peak voltage of the LBPT (V_{CEP}) is defined as the magnitude of the emitter-collector voltage at which the collector current starts to decrease and the differential negative resistance begins, then the peak voltage will be equal to V_T' and can be expressed as

$$V_{CEP} = \phi_{Ms} + 2|\phi_{fp}| - \frac{Q_{ss}}{C_o} + \left[2K_s\epsilon_o qN_{As}(2|\phi_{fp}| - V_{BEP})\right]^{1/2}.$$
 (24)

The voltage range of the differential negative resistance ΔV_t can be written as

$$\Delta V_{t} = V_{CEV} - V_{CEP}$$

$$= \left[\frac{L(I_{co} + I_{PH})}{WC_{o}KV_{BE, \text{cut-in}}} + \frac{1}{2}V_{BE, \text{cut-in}} \right]^{1/(1-r)}$$

$$+ \frac{(2K_{s}\epsilon_{o}qN_{As})^{1/2}}{C_{o}} \left[(2|\phi_{fp}| - V_{BE, \text{cut-in}})^{1/2} - (2|\phi_{fp}| - V_{BEP})^{1/2} \right]. \tag{25}$$

From (25) it is clearly seen that the voltage range of the differential negative resistance region ΔV_t may be varied with the device parameters and the photoinduced current.

It should be noted that the condition $I_D = I_{co} + I_{PH}$ may also be satisfied in Region III. In this situation, Region IV does not exist; then the valley voltage can be calculated by using (9) and is expressed by

$$V_{CEV} = \left[\frac{2L(I_{co} + I_{PH})}{WC_o K} \right]^{1/(2-r)} + \phi_{Ms} + 2|\phi_{fp}| - \frac{Q_{sv}}{C_o} + \frac{1}{C_o} \left[2K_s \epsilon_0 q N_{As} \left(2|\phi_{fp}| - V_{BE, cut-in} \right) \right]^{1/2}.$$
 (26)

III. EXPERIMENTAL RESULTS AND THEORETICAL COMPARISONS

In order to fabricate the LBPT's as described in the previous section, a set of testing patterns was designed and the metallization pattern of the designed mask is shown in Fig. 3. The layout parameters of the testing patterns are listed in Table I where the aspect ratio (W/L) of the

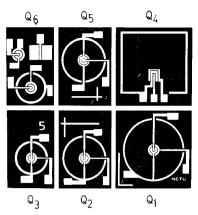


Fig. 3. The photograph of the design patterns (metallization mask).

TABLE I
GEOMETRIC PARAMETERS OF THE DESIGNED MASK

LBPT Parameters	o ₁	Ω2	Q ₃	Ω ₄	Q ₅
Effective base area(mm ²)*	0.628	0.33	0.154	1.033	0.33
Aspect ratio of the MOSFET (W/L)	19.7	19.7	28.2	26	26

* Effective base area = (base area)-(source area)-(drain area)
-(metallization area)

TABLE II PROCESS STEPS OF THE LBPT

- . Strictly clean the silicon wafer surface (n or n/n+
- . Thermally grow a layer of ${\rm SiO_2}$ about ${\rm 8000A^\circ}$
- . Use the 1st mask to define the base diffusion region
- . Boron predeposition (950°C), Boron drive-in (1200A°) and oxide growth
- . Use the 2nd mask to define the emitter and collector windows of the npn thrasistor and the drain window of the n-channel MOSFET
- . Phosphorus deposition (1000°C), phosphorus drive-in (1050°C) and oxide growth
- . Use the 3rd mask to define the gate oxide region
- . Thermally grow the gate oxide
- . Use the 4th mask to define the contact windows
- . Al-metallization
- . Use the 5th mask to define the metallization patterns
- . Sintering

circular MOSFET's in the center of the pattern is calculated by using the expression $2\pi/\ln(r_1/r_2)$ and $r_1(r_2)$ is the outer (inner) radius of the channel.

Note that two smaller patterns in the upper left corner are two MOSFET's which are used to measure the threshold voltage and other characteristic parameters. The masking steps are similar to those of the double-diffused n-p-n transistor except that an additional mask is designed to remove the gate oxide of the n-channel MOSFET. The fabrication sequences of the LBPT's are the same as those of the LBT's [2], [4] and are listed in Table II. A typical surface morphology of the fabricated LBPT(Q5) is shown in Fig. 4, where the electrodes are also marked for clarity.

The I-V characteristic of the fabricated device (Q5) is shown in Fig. 5, where three different kinds of illumination

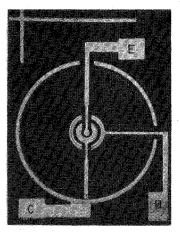


Fig. 4. The surface morphology of the fabricated n-p-n LBPT(Q5).

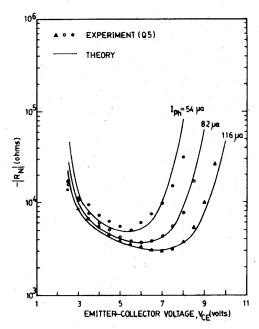


Fig. 6. Comparisons between the measured differential negative resistance of the fabricated n-p-n LBOT(Q5) and the results of the developed model.

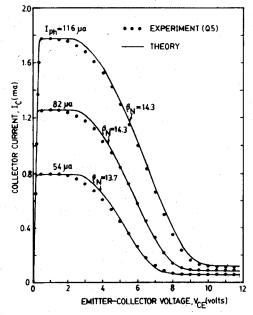


Fig. 5. Comparisons between the measured I-V characteristic of the fabricated n-p-n LBPT(Q5) and the results of the developed model.

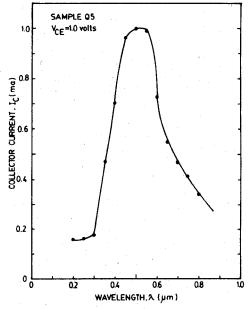


Fig. 7. Spectral response of the fabricated n-p-n LBPT(Q5) operated with $V_{CE} = 0.1 \text{ V}$.

TABLE III PARAMETERS USED FOR SIMULATIONS (Q5)

Paremeter LBPT	N _{As} (cm ⁻³)	Q _{ss} /q	φ _{fp} (volt)	I _{Es} (amp)	$\beta_{\text{mo}} = (\frac{W}{L}) C_{\text{o}} K$ (amp/volt^2)	C _o (forad/cm ²)	r	r _{sc} +r _{SE} (ohms)
Q5	3.5 x 10 ¹⁷	3.0 x 10 ¹¹	0.44	3.86 x 10 ⁻¹⁶	3.0 x 10 ⁻⁶	3.4 x 10 ⁻⁸	-0.72	60 y

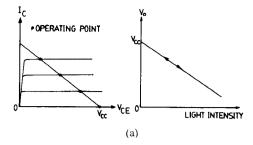
intensity are used. Comparisons between the developed model and the experimental I-V characteristic are also plotted in Fig. 5 and the parameters used for simulations are listed in Table III. It is shown that excellent agreement has been obtained. Similarly, the differential negative resistance as a function of applied terminal voltage (V_{CF}) for three different illumination intensities is shown in Fig. 6, where the parameters used for simulations are the same as those listed in Table III. Again, good agreement between comparisons has been obtained. Therefore, the developed model is shown to accurately describe the operation of the fabricated lambda bipolar phototransistor. The spectral response of the fabricated device (Q5) is shown in Fig. 7, where the peak response is located at $\lambda \approx 5000$ Å. It has been shown that the peak location of spectral response will shift to longer wavelength as the base junction depth becomes deeper. This consequence is the same as that of conventional bipolar phototransistor because longer wavelength will penetrate more deeply in the silicon materials. Note that there are five different patterns shown in Table I; however, their differential negative resistance characteristics are similar except the characteristic parameters defined in Section II are slightly different due to different device dimensions.

IV. APPLICATIONS

The LBPT described in the previous sections not only possesses all the properties of the conventional bipolar phototransistor, but also offers extra characteristics, which can be used in switching, oscillator, modulator, and memory applications.

The LBPT can be used to detect the ON-OFF of an optical signal. Due to the bistable characteristic which existed in the negative resistance region, the LBPT is inherently superior to the conventional phototransistor in driving digital circuit. For example, if the LBPT is biased as shown in Fig. 8(b), two clear states can be easily observed during the gradual change of light intensity. However, for the conventional bipolar phototransistor as shown in Fig. 8(a), a Schmitt triggering circuit must be inserted in order to obtain a clear state. Hence, the LBPT possesses good noise immunity for digital circuit applications. Furthermore, the valley current of the LBPT in the dark is equal to I_{co} , while the dark current of the conventional phototransistor is equal to $(1+\beta)I_{co}$. Therefore, the LBPT will consume much less standby power. These merits enable the LPBT to be used in various digital switching applications, such as perforated-tape readers and punched-card readers as shown in Fig. 9, where an 8-bit digital perforated-tape reader using the LBPT devices is shown. Note that this circuit consumes the standby power of $8I_{co}V_{CE}$, however, the circuit using conventional phototransistors consumes $8(1+\beta)I_{co}V_{cc}$.

Similarly, the regenerative process of the LBPT due to the negative resistance region will facilitate the LBPT to be used as a very sensitive light detector. For example, if the



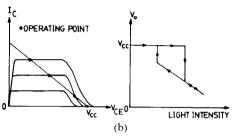


Fig. 8. Operating characteristic and transfer curve of (a) conventional bipolar phototransistor and (b) the n-p-n LBPT.

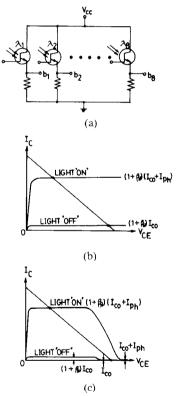


Fig. 9. (a) The circuit diagram of an 8-bit digital perforated-tape reader using the LBPT's. (b) The operating points and characteristics of conventional bipolar phototransistor as a light switch (c) The operating points and characteristics of the LBPT as a light switch.

LBPT is biased with a base current such that the operating point is slightly beyond the valley point, a small disturbance of ambient illumination can be easily detected.

The LBPT may also be biased at the astable point as shown in Fig. 10 where the output of the LBPT is connected in series with a *LC* tank circuit. The output of this circuit will be a well-defined sinusoidal waveform with the

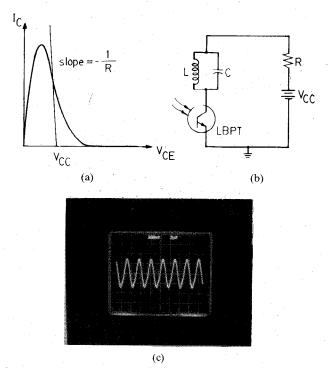


Fig. 10. The n-p-n LBPT used as a photoinduced sinusoidal oscillator.

(a) Load line and operating point. (b) The circuit diagram. (c) The output waveform.

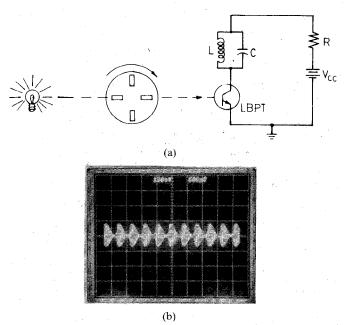


Fig. 11. The n-p-n LBPT used as a photoinduced modulator. (a) Circuit diagram and coded light source. (b) The output waveform.

frequency of $1/2\pi\sqrt{LC}$. Hence, the LBPT may serve as a light sensor and gives a sinusoidal oscillation signal, which can drive a counter to count the duration of the incident light. Similarly, the LBPT can also be used as light signal modulator as shown in Fig. 11, where a coded light signal modulates the amplitude of sinusoidal signal generated by the LBPT and the LC tank circuit.

The LBPT may also be used in the four-quadrant photoposition detector as shown in Fig. 12(a). If the detector is biased as shown in Fig. 12(b), larger output current

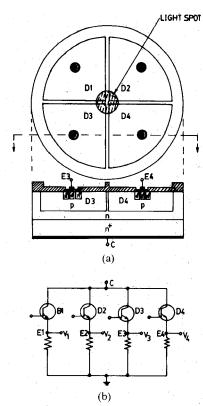


Fig. 12. A four quadrant photoposition detector. (a) The layout structure and the cross-sectional view. (b) The circuit diagram.

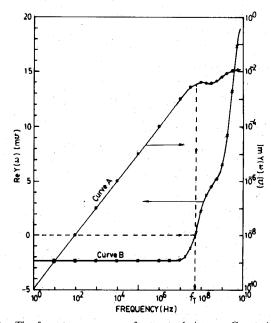


Fig. 13. The frequency response of output admittance. Curve A represents the imaginary part of output admittance. Curve B represents the real part of output admittance.

 $[(1+\beta)(I_{PH}+I_{co})]$ and low dark current (I_{co}) can be obtained. The detected signal and the transformation of position vector to voltage vector are the same as those of conventional four-quadrant photopositive detector [5]. The performance of this application will be presented elsewhere.

The analysis for the frequency response is valuable because the dynamic characteristics the LBPT are closely

related to the applications of this device in oscillators and switching circuits. Using the SPICE [6] circuit simulator. the ac analysis of the LBPT has been carried out. It has been shown that the differential negative resistance will disappear at a certain frequency which is defined as the frequency limit of the LBPT. This feature can be easily seen from the output admittance of the LBPT(O5) shown in Fig. 13, in which curve A shows the imaginary part of the output admittance and curve B shows the real part of output admittance. From Fig. 13, the frequency limit f_T (70 MHz) as marked in the figure indicates that $f < f_T$, the differential negative resistance exists, and both the output capacitance and the differential negative resistance are kept constant for f < 10 MHz. This frequency limit can be increased by increasing the transconductance of the MOSFET and reducing the collector capacitance of the bipolar transistor and the gate-drain overlap capacitance of the MOSFET. Therefore, the frequency limit f_T can be improved by using self-alignment Si-gate technology to reduce the gate and drain overlap capacitance and the channel length. Similarly, the collector capacitance can be reduced by using the lightly doped epilayer on n⁺ substrate as the substrate wafer.

V. CONCLUSION

The LBPT, a new light-sensitive voltage-controlled differential negative device, has been theoretically and experimentally studied. It has been shown that the important characteristic parameters of the LBPT can be varied by controlling the fabrication process and the device geometries. Good agreement between the experimental devices and the developed simple model has been obtained. Some interesting applications of the LBPT have been briefly discussed and demonstrated, which show that the LBPT devices exhibit superior characteristics in optical detection when compared to those using conventional bipolar phototransistor. Moreover, the frequency limit of the LBPT has been simulated by using SPICE circuit simulator and the methods of improving the frequency limit are also discussed.

REFERENCES

[1] C.-Y. Wu, C.-Y. Wu, and H.-D. Sheng, "A new photo-sensitive voltage-controlled differential negative resistance device—The lambda bipolar photo-transistor," *IEEE Electron Device Lett.*, vol.

EDL-1, pp. 81–82, May 1980. C.-Y. Wu and C.-Y. Wu, "An analysis and the fabrication technology of the LAMBDA bipolar transistor," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 414-419, Feb. 1980.

J. J. Ebers and J. L. Moll, "Large signal behavior of junction

J. J. EDETS and J. L. Moll, "Large signal behavior of junction transistor," *Proc. IRE*, vol. 42, no. 12, p. 1761, 1954.

C.-Y. Wu, "A new internal overvoltage protection structure for the bipolar power transistor," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 773, 777, Dec. 1982. 777, Dec. 1983.

G. J. Deboo and C. N. Burrous, Integrated Circuits and Semiconductor Device: Theory and Application. New York: McGraw-Hill, 1977,

A. Vladimirescu, A. R. Newton, and D. O. Pederson, SPICE 2G.1 User's Guide. Berkeley, CA: Univ. of Calif., Oct. 1980.



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