A New Approach to Model CMOS Latchup

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Abstract—Based upon the concept of the λ-type I–V characteristics, CMOS latchup is modeled and latchup criteria are constructed. According to the model and the criteria, conditions which lead to latchup can be expressed in terms of triggering currents, parasitic resistances, and device parameters. Therefore, latchup initiation can be predicted. Both transient simulation results and experimental results coincide with theoretical predictions and calculations. This substantiates the correctness of the proposed model.

LIST OF SYMBOLS

$HC_{1(2)}$ Low-current compensation parameter of the transistor $Q_1(Q_2)$.

I_{AC} Total anode–cathode current of the p-n-p-n structure.

I_{E1} Emitter current of the transistor Q_1.

$I_{P(V)0}$ Peak (valley) current without the triggering current I_1.

$I_{S1(2)}$ Reverse saturation current of the transistor $Q_1(Q_2)$ with high-level injection roll-off effect.

$I_{S1(2)0}$ Reverse saturation current of the transistor $Q_1(Q_2)$ without high-level injection roll-off effect.

$V_{B(E)N}$ Voltage drop across the base (emitter) resistance $R_{BN}(R_{EN})$ of the n-p-n transistor Q_2.

V_T Thermal voltage.

V_Z Collector–emitter voltage of the transistor Q_2 at the zero point.

$\beta_{F1(2)}$ Ideal maximum forward current gain of the transistor $Q_1(Q_2)$.

$\beta_{R1(2)}$ Ideal maximum reverse current gain of the transistor $Q_1(Q_2)$.

$\theta_{1(2)}$ High-level injection roll-off parameter of the transistor $Q_1(Q_2)$.

I. INTRODUCTION

IT IS KNOWN that the inherent p-n-p-n structure in bulk complementary MOS (CMOS) integrated circuits (IC's) can be triggered into the conduction state under certain conditions [1]. Such a parasitic semiconductor-controlled-rectifier (SCR) action, which creates a high current path

between V_{DD} and V_{SS} power supplies and destroys the operation of a CMOS chip, is called latchup. When scaling bulk CMOS to achieve better cost and performance in very-large-scale integration (VLSI), both horizontal and vertical dimensions must be reduced. This enhances the parasitic effects and increases the latchup threat drastically.

Therefore, an efficient and accurate latchup model capable of characterizing and predicting latchup is required as a good design guideline for device/circuit optimization or improvement.

Recently, many latchup models have been proposed [1]–[9]. In these models, latchup is characterized by using the SCR approach which takes the whole parasitic p-n-p-n structure into consideration. Then, the holding and threshold points in the resultant S-type I–V characteristic can be formulated by using various calculation methods. Latchup is considered to be initiated when the threshold point is reached, and is considered to be sustained when the holding point is reached.

In the S-type I–V characteristic, however, current is a multivalue function of voltage. So it can not be modeled by using the popular circuit simulators such as SPICE. Moreover, the negative-resistance region as well as the threshold and holding points in the I–V curve often can not be easily observed or measured. These lead to some difficulties in modeling and predicting the latchup initiation.

In this study, a different approach is proposed to model CMOS latchup. In this approach, the I–V characteristic of the parasitic p-n-p-n structure is modeled as that of the dual-base transistor (DUBAT) [10]. The resultant I–V curve will be of the λ-type [10] rather than the S-type. Section II of this paper is devoted to model development and analysis for the λ-type I–V characteristics of the p-n-p-n structures with different transistor parameters, parasitic resistances, and external triggering currents. SPICE simulation results are also given for comparisons. For simplicity, a one-dimensional lumped equivalent circuit is adopted. Based upon the developed λ-type I–V characteristics, latchup criteria are definitely determined and described in Section III. Verifications of these criteria using SPICE transient simulations are also described in this section. Using these criteria, latchup initiation can be predicted and useful design guidelines can also be formed. In Section IV, experimental results are investigated. General consistency with the model predictions and calculations substantiates the correctness of the proposed model.
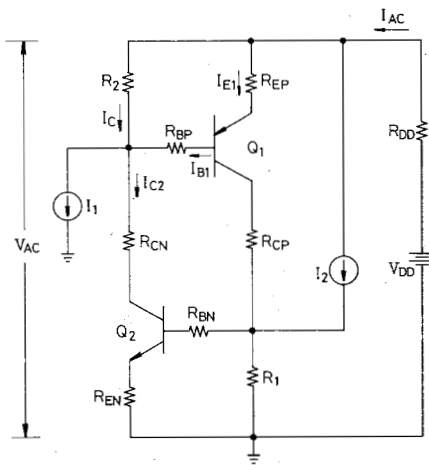
Fig. 1. Complete lumped equivalent circuit of the parasitic p-n-p-n structure.
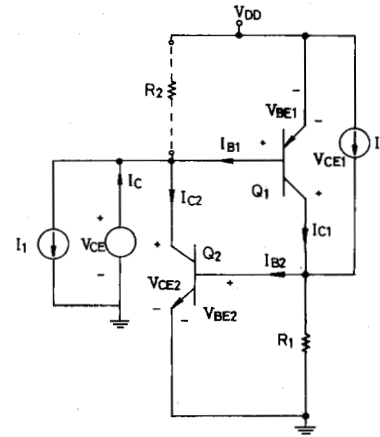

Fig. 2. Simplified lumped equivalent circuit of the p-n-p-n structure together with the voltage source V_{CE}.

II. λ-Type I-V Characteristics of the Parasitic p-n-p-n Structure

A. Simplified Model for I-V Characteristics

Generally, the parasitic p-n-p-n structure in bulk CMOS can be represented by the lumped equivalent circuit of Fig. 1, where the voltage source V_{DD} is the total power supply voltage across the structure and the resistance R_{DD} is the total power supply internal resistance. In the case of bulk p-well CMOS, the p-n-p transistor Q_1 is the p^+-n-substrate-p-well lateral transistor with the equivalent substrate resistance R_2 across its base–emitter junction. The n-p-n transistor Q_2 is the n^+-p-well-n-substrate vertical transistor with the equivalent well resistance R_1 across its base–emitter junction. All other resistances are the terminal series resistances of the transistors. The triggering currents can be effectively represented by two ideal current sources I_1 and I_2, both connected to the base terminals of the transistors.

In order to obtain analytic results and to get an insight into the physical nature of latchup, a simplified lumped equivalent circuit for the p-n-p-n structure is used first. This circuit is shown in Fig. 2, which is obtained from the circuit of Fig. 1 by neglecting all resistances except R_1 and R_2. Later, the effects of these neglected resistances on the I-V characteristics will be considered.

Referring to the circuit of Fig. 2, if the resistance R_2 is temporarily removed, the whole structure becomes similar to the DUBAT device [10]. Therefore, after an independent voltage source V_{CE} is applied between the collector and emitter terminals of the n-p-n transistor Q_2. The resultant I_C-V_{CE} characteristic is of the λ type as shown in Fig. 3 by solid lines. This λ-type I_C-V_{CE} curve can be understood from the analysis of the circuit in Fig. 2.

First, when V_{CE} is small, both transistors are turned on deeply in their saturation regions. In this case, I_{B1} is much larger than I_{C2} and the resultant I_C is negative because it flows into the voltage source V_{CE}. When V_{CE} is increased, the transistor Q_2 is out of saturation and I_{C2} is increased. On the other hand, the base–emitter voltage V_{BE1} of the
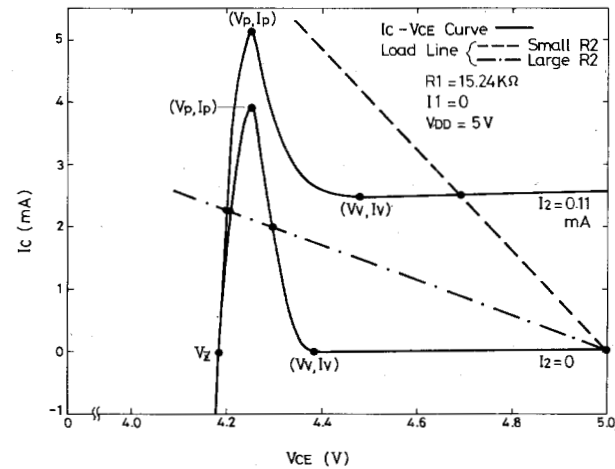

Fig. 3. Typical I_C-V_{CE} characteristics with $I_2 = 0$ and $I_2 = 0.11$ mA.

transistor Q_1 is decreased and I_{B1}, although remaining larger in magnitude then I_{C1}, is thus decreased. This leads to a negative I_C with decreasing magnitude, as shown in Fig. 3.

Further increase of V_{CE} gradually pulls the transistor Q_1 from deep saturation and decreases V_{BE1}. This decreases I_{B1} and increases I_{C1}. The increase of I_{C1} also increases I_{B2} and I_{C2}. Therefore, the magnitude of I_C is decreased. At $V_{CE} = V_Z$, I_{C2} is equal in magnitude to I_{B1} and $I_C = 0$. This point is called the zero point. When I_{C2} becomes larger than I_{B1}, I_C becomes positive, both its magnitude continues to increase until V_{CE} reaches the peak voltage V_P as shown in Fig. 3. At this point, the transistor Q_1 is operated in the active region and I_C reaches its maximum value called the peak current I_P.

After this point, further increase of V_{CE} decreases V_{BE1} of transistor Q_1, which is in the active region. Thus I_{B1} and I_{C1} are decreased. This in turn decreases I_{B2}, I_{C2}, and I_C. The differential negative resistance (DNR) region, therefore, is formed. When V_{CE} finally reaches the valley voltage V_V, the transistor Q_1 is turned off with very small I_{C1} and I_{B1}. Thus I_{B2} is completely generated from the fixed triggering current I_2. This leads to fixed I_{C2} and I_C. Fur-

ther increase of V_{CE} still keeps I_C nearly constant as shown in Fig. 3. Since I_1 is in parallel with the voltage source V_{CE}, applying a fixed I_1 only leads to a constant shift of current in the I–V curve shown in Fig. 3.

It should be noted that this λ-type I–V characteristic can be definitely measured and can be simulated by using the conventional circuit simulators such as SPICE.

As will be verified later, the region between the zero point and the peak point in the λ-type I_C–V_{CE} characteristic is the latchup operation region whereas the region between the valley ponit and the V_{DD} point is the stable operation region. Therefore, latchup can be analyzed by analyzing the λ-type I_C–V_{CE} characteristics.

To characterize the I_C–V_{CE} characteristics, the modified Ebers–Moll equations [11] are used. Taking both the high-level injection effect and the surface-leakage current effect into consideration, the currents I_{B1}, I_{C1}, I_{B2}, and I_{C2} can be expressed. Then the relations between the terminal currents and voltages are formulated according to the equivalent circuit of Fig. 2. Using these equations, current I_C can be expressed in term of V_{CE}. The detailed calculation procedures and the final expressions are listed in Appendix I.

To calculate I_C–V_{CE} characteristics, first the voltage V_{BE2} under fixed V_{CE} is solved from (A12) by numerical iterations. Then, the solved V_{BE2} is substituted into (A13) to solve I_C. The calculated results are plotted in Fig. 3 with typical device parameters and different values of I_2.

In the case that both transistors are operated in their active regions, we have $\exp[(V_{BE2} - V_{CE})/V_T] \ll 1$ and $\exp(V_{BE2}/V_T) \gg 1$. Then (A12) and (A13) in Appendix I can be simplified as

$$I_C = I_{S2}e^{V_{BE2}/V_T} - (I_{S10}/\beta_{F1})\, e^{(V_{DD} - V_{CE})/V_T}$$

$$- HC_1 I_{S10} e^{(V_{DD} - V_{CE})/2V_T} + I_1 \tag{1}$$

$$(I_{S20}/\beta_{F2})\, e^{V_{BE2}/V_T} + HC_2 I_{S20} e^{V_{BE2}/2V_T}$$

$$= I_{S1} e^{(V_{DD} - V_{CE})/V_T} + I_2 - V_{BE2}/R_1. \tag{2}$$

To solve V_Z, one can let $I_C = 0$ and solve V_{CE} from (A12) and (A13) or from (1) and (2).

As will be seen later, the peak and valley points are important in determining the latchup criteria, so they must be definitely characterized. Since the peak point specified by the peak current I_P and the peak voltage V_P is the absolute maximum point in the λ-type I_C–V_{CE} curve, they can be solved from the first derivative of I_C with respect to V_{CE}. The final results are listed in (A15). Solving (A15) and (A12) by numerical iterations, V_P and the corresponding V_{BE2P} can be obtained. Substituting V_P and V_{BE2P} into (A13), the peak current I_P can be calculated.

In most cases, the peak voltage is large and both transistors are operated in their active region. Therefore, (A15) can be simplified as (A12) and (A13). The simplified expression is

$$[(I_{S10}/\beta_{F1} V_T)\, e^{(V_{DD} - V_P)/V_T}]$$

$$\cdot \left[(I_{S20}/V_T) \left(\frac{1}{\beta_{F2}}\, e^{V_{BE2}/V_T} \right. \right.$$

$$\left. + \frac{HC_2}{2}\, e^{V_{BE2}/2V_T} \right) + \frac{1}{R_1} \right]$$

$$+ \{(-I_{S20}\theta_2 e^{3V_{BE2}/2V_T})/[2V_T(1 + \theta_2 e^{V_{BE2}/2V_T})^2]$$

$$+ (I_{S2}/V_T)\, e^{V_{BE2}/V_T}$$

$$- (HC_1 I_{S10}/2V_T)\, e^{V_{BE2}/2V_T}\}$$

$$\cdot \{-(I_{S1}/V_T)\, e^{(V_{DD} - V_P)/V_T}$$

$$+ (I_{S10}\theta_1 e^{2(V_{DD} - V_P)/V_T})$$

$$\cdot /[2V_T(1 + \theta_1 e^{(V_{DD} - V_P)/2V_T})^2]\}\}$$

$$= 0. \tag{3}$$

At the valley point, the transistor Q_1 is nearly cut off because of larger V_{CE}. Thus its collector current I_{C1} is very small and the base current I_{B2} is equal to $(I_2 - V_{BE2V}/R_2)$. In this case, V_{BE2} denoted as V_{BE2V} can be solved from (A3). Substituting the solved V_{BE2V} into (A14) for V_{BE2}, the valley voltage $V_{CE} = V_V$ can be calculated. Using the solved V_{BE2V} and V_V in (A13) for V_{BE2} and V_{CE}, respectively, the valley current I_V can be calculated. In the case of $I_2 = 0$, V_{BE2V} is small and I_V may become negative as may be seen from (A13) or (1).

The simplified expression for V_{BE2V} can be written from (A3) and (A7) as

$$I_2 - V_{BE2V}/R_1 = (I_{S20}/\beta_{F2})\, e^{V_{BE2V}/V_T}$$

$$+ HC_2 I_{S20} e^{V_{BE2V}/2V_T}. \tag{4}$$

Using (4), (1), and (2), V_V and I_V can also be solved.

Fig. 4(a) and (b) shows the calculation results of the peak and valley currents as a function of triggering current I_2 under different values of R_1 and β_{F2}, respectively. Also shown in these figures are the corresponding simulation results by using the SPICE 2 Program [12]. The general agreement is satisfactory.

From Fig. 4, it can be seen that both peak and valley currents are decreased with decreasing I_2 and R_1. When R_1 is small, the shunting effect across the base–emitter junction is large and a considerable part of current I_2 is taken out of the base terminal of the transistor Q_2. Thus the peak and valley currents are decreased as shown in Fig. 4(a). On the other hand, a larger β_{F2} leads to a larger I_{C2} and I_C. Thus the peak and valley currents are increased as shown in Fig. 4(b).

The calculated peak and valley voltages are shown in Fig. 5(a) and (b) where the weak dependence on I_2, β_{F2}, and R_1 leads to nearly constant V_P and V_V. This is because the voltage is a logarithmic function of the current, and thus the gain and the resistance R_1, in bipolar transistors.

As may be seen from (2)–(4), the current I_1 has no effect on the peak and valley voltages. Equation (1) also in-
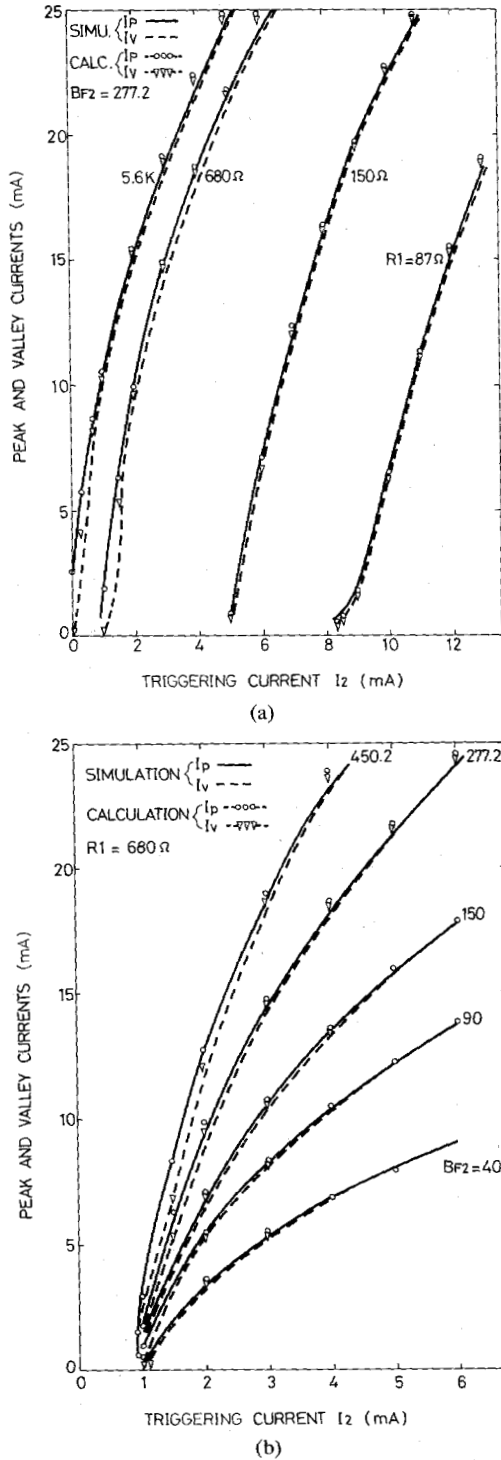
Fig. 4. Peak and valley currents versus triggering current I_2 (a) with R_1 as a parameter and $\beta_{F2} = 277.2$; (b) with β_{F2} as a parameter and $R_1 = 680$ Ω.
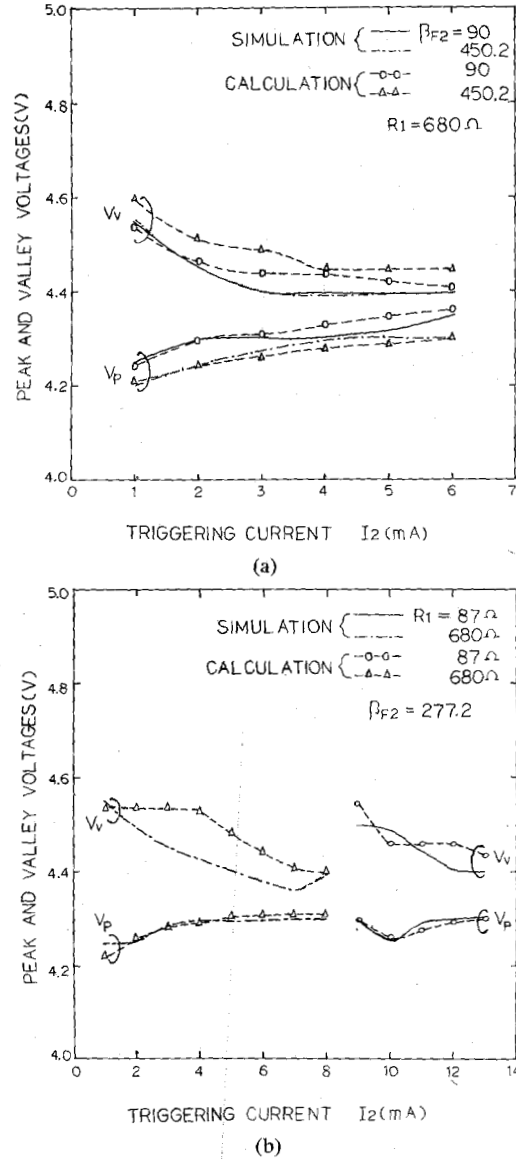

Fig. 5. Peak and valley voltages versus triggering current I_2 (a) with $\beta_{F2} = 90$ and 450.2 and $R_1 = 680$ Ω; (b) with $R_1 = 87$ and 680 Ω and $\beta_{F2} = 277.2$.

dicates that the peak and valley currents are simply increased by a quantity I_1 under I_1 excitation. These observations have been confirmed by SPICE simulations.

In some cases, no DNR region exists, or equivalently, the valley current is equal to the peak current. No DNR region means that the collector current I_{C1} has no contribution to I_{C2} and there is no regeneration path. Generally, too small a current gain in transistor Q_1 or Q_2, as well as

too small R_1, results in these cases. Using the derived theory, these cases can be figured out as shown in Fig. 6(a) and (b), where the ranges of parameters in which the DNR region exists are marked by the boundary lines shaded with hatching. Generally, when β_{F1} or β_{F2} is larger than some threshold values, the same threshold value for R_1 is necessary to generate the DNR region, and this value of R_1 is decreased with increasing I_2.

B. I–V Characteristics with Load Line

With the substrate resistance R_2 added to generate the collector current I_C, the complete characteristics of the latchup equivalent circuit of Fig. 2 can then be described by the I_C–V_{CE} characteristic curve combined with the load line, all shown in Fig. 3 where the load lines are represented by broken lines. The load line equation is

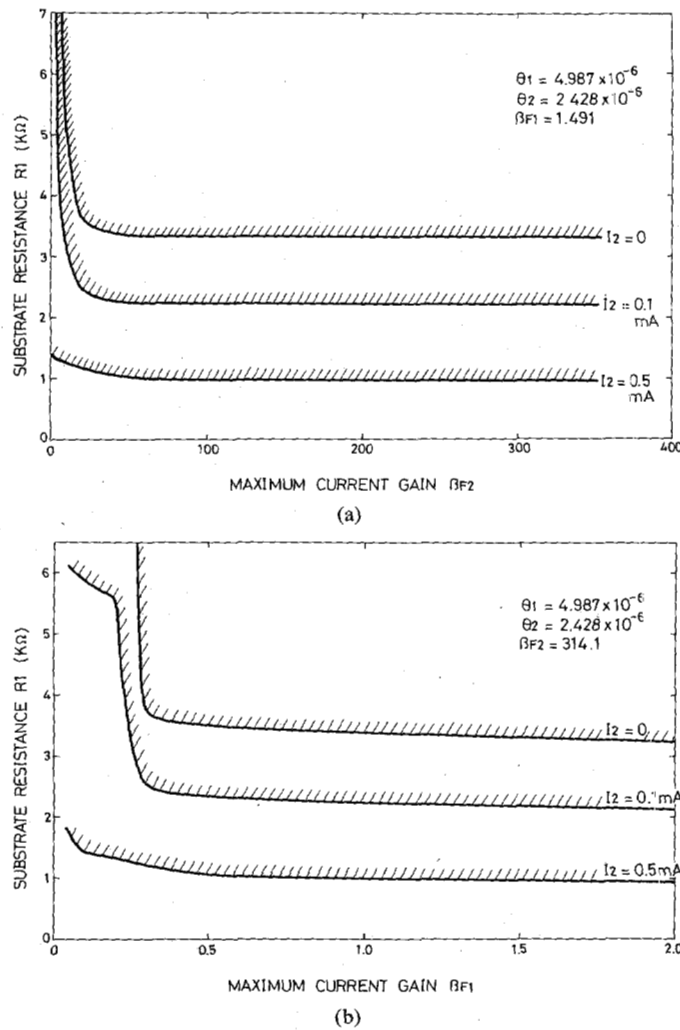$$I_C = (1/R_2) \ (V_{DD} - V_{CE}). \tag{5}$$

$\theta_1 = 4.987 \times 10^{-6}$
$\theta_2 = 2.428 \times 10^{-6}$
$\beta_{F1} = 1.491$

$I_2 = 0$

$I_2 = 0.1$ mA

$I_2 = 0.5$ mA

(a)

$\theta_1 = 4.987 \times 10^{-6}$
$\theta_2 = 2.428 \times 10^{-6}$
$\beta_{F2} = 314.1$

$I_2 = 0$

$I_2 = 0.1$ mA

$I_2 = 0.5$ mA

(b)

Fig. 6. The ranges of R_1 and (a) β_{F2}; (b) β_{F1} in which the differential negative resistance (DNR) region exists.

Fig. 7. Schematic diagram of the lambda lines and load lines in case A.

Fig. 8. Schematic diagram of the lambda lines and load lines in case B.

The intersection points of the $I_C\text{-}V_{CE}$ curve and load line can be determined by solving (A12), (A13), and (5) or simply (1), (2), and (5). Generally, the intersection points whose voltage is smaller than V_P, between V_P and V_V and larger than V_V, are classified as class I, II, and III intersection points, respectively. The classes of intersection points are strongly related to latchup criteria, as will be seen in the next section.

To analytically identify the classes of intersection points, the $I_C\text{-}V_{CE}$ curve in the DNR region is approximated by a straight line called the λ line. This λ line is completely determined by the peak and valley points with the line equation

$$V_{CE} - V_P = m(I_C - I_P)$$

$$= [(V_V - V_P)/(I_V - I_P)] (I_C - I_P) \quad (6)$$

where m is the inverse slope of the λ line and is negative. The intersection point of the λ line and the load line, called the artificial intersection point, can be determined from (5) and (6). Substituting (5) into (6), the voltage V_{CE} at
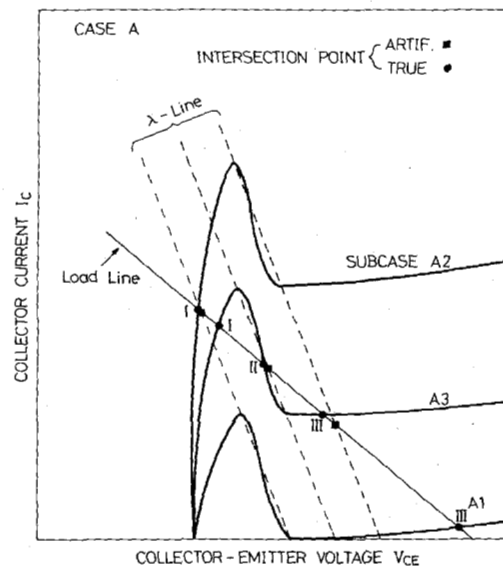
the artificial intersection point, denoted by V_{CEAI}, is solved as

$$V_{CEAI} = [V_P/m + V_{DD}/R_2 - I_P]\bigg/\bigg(\frac{1}{m} + 1/R_2\bigg). \quad (7)$$

From the value of V_{CEAI}, the artificial intersection point can be located and the classes of intersection points can be identified.

According to the magnitude of the slopes of both lines, three different cases must be considered. In each case, there are three subcases corresponding to three different locations of the artificial intersection points. To clearly demonstrate each case, three $I_C\text{-}V_{CE}$ curves, their corresponding λ lines, and the load line have been drawn together. Both artificial and true intersection points have also been indicated. Three such figures are shown in Figs. 7–9. The main features in these three cases have also been

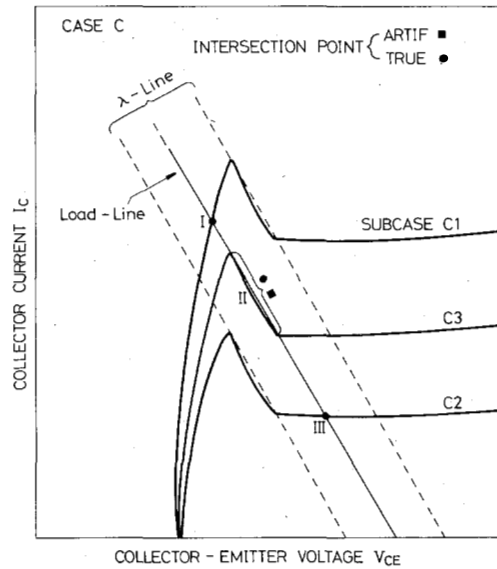Fig. 9. Schematic diagram of the lambda lines and load lines in case *C*.

TABLE I
VARIOUS CASES OF INTERSECTION POINTS AND THEIR CORRESPONDING
LATCHUP FEATURES

Case	Subcase	True intersection point	Artificial intersection point	Latchup condition
	A1	Class III	$V_{CEAI} < V_p$	Stable
A	A2	Class I	$V_{CEAI} > V_v$	Latchup
	A3	Class I II III	$V_p < V_{CEAI} < V_v$	Conditional stable
	B1	Class I	$V_{CEAI} < V_p$	Latchup
B	B2	Class III	$V_{CEAI} > V_v$	Stable
	B3	Class II	$V_p < V_{CEAI} < V_v$	Conditional stable
	C1	Class I	None	Latchup
C	C2	Class III	None	Stable
	C3	Class II	Infinite	Conditional stable

listed in Table I where the latchup conditions will be determined in the next section. In Appendix II, the three cases are analyzed in detail.

C. Effects of Other Resistances

Since the peak point, the valley point, and the intersection points are the most important characteristics in modeling CMOS latchup, the effects of other parasitic resistances on these points, as shown in the circuit of Fig. 1, are considered.

At the valley point, transistor Q_1 is turned off. Therefore, the resistances R_{EP}, R_{BP}, and R_{CP} have negligible effects on the valley point. On the other hand, if R_{CN} and R_{EN} are not so large that the collector–emitter voltage of transistor Q_2 is reduced to $V_{CE,SAT}$, the valley current I_V is nearly independent of R_{CN} and R_{EN}. But when R_{CN} or R_{EN} is too large, the valley current I_V is decreased with the increase of resistance. For the valley voltage V_V, the resistances R_{CN}, R_{EN}, and R_{BN} have no effect on it.

The effect of base resistance R_{BN} on the valley current can be described by the following equation:

$$I_2 - (V_{BE2} + V_{EN})/R_1 = V_{BN}(1/R_{BN} + 1/R_1). \quad (8)$$

If $R_{BN} << R_1$ and transistor Q_2 is in the active region, the base current V_{BN}/R_{BN} will be nearly constant for fixed R_1, as may be seen from (8) by neglecting the term $1/R_1$. This leads to a constant valley current independent of R_{BN}. Otherwise, I_V is decreased with the increase of R_{BN}.

Similarly, if the supply resistance R_{DD} is small, transistor Q_2 can be operated in its active region. Then the effect of R_{DD} is simply to decrease V_V by a quantity of $(I_2 + I_V) R_{DD}$ and the valley current I_V is unchanged. Otherwise, both V_V and I_V will be decreased with the increase of R_{DD}.

With R_{DD}, the load-line equation when $V_{CE} > V_V$ can be written as

$$I_C = \{1/[R_2 + (1 + I_2/I_C) R_{DD}]\} (V_{DD} - V_{CE}). \quad (9)$$

Since $I_2 < I_C$ and $R_{DD} << R_2$, the load characteristic generally is not changed much near the valley point.

The peak current I_P is nearly independent of R_{DD}, R_{EP}, R_{BP}, R_{CP}, R_{BN}, R_{EN}, and R_{CN} if both transistors are operated in the active region. Otherwise, I_P will be decreased. On the other hand, only R_{DD}, R_{EP}, and R_{BP} affect the value of V_P which is decreased by a quantity of $I_{B1}R_{BP} + I_{E1}R_{EP} + I_{AC}R_{DD}$. If both transistors are in the active region, I_{B1}, I_{E1}, and I_{AC} can be approximately expressed by assuming constant gain. The resultant equations are

$$I_{B1} = [\beta_{F2}I_2 + I_1 - I_P - \beta_{F2}V_{BE2}/R_1$$

$$- R_{BN}(I_P - I_1)/R_1 - R_{EN}(\beta_{F2} + 1)$$

$$\cdot (I_P - I_1)/R_1] \Big/ \left[1 + \frac{R_{BN}}{R_1} \right.$$

$$\left. + R_{EN}(\beta_{F2} + 1)/R_1 - \beta_{F1}\beta_{F2} \right] \qquad (10)$$

$$I_{E1} = (\beta_{F1} + 1)\,I_{B1}/\beta_{F1} \qquad (11)$$

$$I_{AC} = I_P + I_{E1} + I_2. \qquad (12)$$

Similarly, the decrease of the voltage V_Z at the zero point due to R_{DD}, R_{EP}, and R_{BP} can be calculated by the same formulas.

The load-line equation is changed by R_{DD}. The general expression can be rewritten as

$$I_C = \{1/[R_2 + (1 + I_2/I_C + I_{E1}/I_C)\,R_{DD}]\}\,(V_{DD} - V_{CE}). \qquad (13)$$

When $V_{CE} > V_V$, $I_{E1} = 0$ and (13) reduces to (9) as expected. As may be seen from (13), the effective load resistance is increased due to R_{DD}.

Generally, the peak and valley points of the complete equivalent circuit of Fig. 1 can be exactly determined from the λ-type I_C-V_{CE} characteristics which are obtained from the SPICE simulations on the circuit with R_2 replaced by a V_{CE} voltage source. These points can also be approximately calculated by using the previously mentioned methods provided both transistors are in the active region. Using the calculated peak and valley points and load-line equation (13), the intersection points can be identified by the methods in Section II-B.

In summary, the effect of the resistances R_{BP}, R_{CP}, R_{EP}, R_{BN}, R_{CN}, and R_{EN} on the λ-type I_C-V_{CE} characteristic is to decrease the voltage and current at the peak and valley points. Therefore, the Class III intersection point is more likely to be generated with such resistances. The effects of R_{DD} are to decrease the voltage and current at the peak and valley points and to increase the load resistance. Therefore, the classes of intersection points are not considerably changed.

D. Relation to the S-type I–V Characteristics

Using the new modeling approach, the S-type I–V characteristic of the p-n-p-n structure can be calculated. From the simplified equivalent circuit in Fig. 2 with the resistor R_2 and the triggering currents I_1 and I_2, the anode–cathode current I_{AC} which is the current of the supply voltage V_{DD} can be expressed as

$$I_{AC} = I_C + I_{B1} + I_{C1} + I_2 \qquad (14)$$

where I_C, I_{B1}, and I_{C1} are expressed in (A8), (A1), and (A2) as functions of V_{CE}, V_{BE2}, V_{CE1}, and V_{BE1}. The supply voltage V_{DD} in this case is the anode–cathode voltage V_{AC}. Using (A12), (A13), (A9), and (A10), V_{CE}, V_{BE2}, V_{CE1}, and V_{BE1} cna be expressed in terms of V_{AC}. Substituting these expressions into (14), current I_{AC} becomes a function of V_{AC}. Then, the S-type I_{AC}-V_{AC} characteristic can be generated by solving V_{AC} for various given values of I_{AC}.

The most important parameters in the S-type I–V characteristic are the threshold current I_{TH}, threshold voltage V_{TH}, holding current I_H, and holding voltage V_H [1]–[9]. The threshold points considered here are those with the triggering currents. These important parameters can be characterized by using the peak current I_P, peak voltage V_P, valley current I_V, and valley voltage V_V of the λ-type I_C-V_{CE} characteristic analyzed in Section II-A.

Since the supply resistance R_{DD} is not considered in the circuit of Fig. 2, the load line is the S-type I_{AC}-V_{AC} characteristic is a vertical line at $V_{AC} = V_{DD}$. If the value of V_{DD} is smaller than the threshold voltage V_{TH} but is larger than the holding voltage H_H, there are three intersection points located in the ON region, negative resistance region, and OFF region of the S-type I–V characteristic. They correspond to the Class I, II, and III intersection points mentioned in Section II-B. In the case where V_{DD} is equal to the threshold voltage V_{TH}, the threshold point is on the load line and further increase of V_{DD} leads to only one intersection point in the ON region. This case corresponds to the case that a suitable voltage $V_{DD} = V_{TH}$ is applied such that the load line in the λ-type I_C-V_{CE} characteristic passes the valley point and further increase of V_{DD} leads to only one intersection point of Class I. Therefore, threshold voltage V_{TH} can be expressed in terms of V_V and I_V as

$$V_{TH} = V_{AC} = V_V + I_V R_2 \qquad (15)$$

where V_V and I_V can be expressed by using the similar method in Section II-A and they are functions of $V_{AC}(=V_{TH})$. By using numerical iterations, V_{TH} can be solved from (15). The corresponding threshold current I_{TH} can be determined from (14) with $I_C = I_V$ and with I_{B1} and I_{C1} calculated at the valley point.

On the other hand, if voltage V_{DD} is equal to holding voltage V_H, the holding point is on the load line and further increase of V_{DD} leads to only one intersection point in the OFF region. This corresponds to the case that a suitable voltage $V_{DD}(=V_H)$ is applied such that the load line in the λ-type I_C-V_{CE} characteristic passes the peak point and further increase of V_{DD} leads to only one intersection point of Class III. Thus holding voltage V_H can be written as

$$V_H = V_{AC} = V_P + I_P R_2 \qquad (16)$$

where V_P and I_P are functions of V_H. The holding voltage V_H thus can be solved from (16) and holding current can

be calculated from (14) by using a method similar to that in the calculations of the threshold point.

Generally, the effect of transistor parasitic terminal resistances on the $I_{AC}-V_{AC}$ characteristic, holding point, and threshold point can also be analyzed in a similar way, based upon the considerations in Section II-C. In an actual CMOS IC, the applied power supply V_{DD} usually has a small R_{DD}. If, however, the p-n-p-n structure is measured on a curve tracer, the resistance R_{DD} becomes the series resistance provided by the equipment. In this case, R_{DD} is large and the load line in the $I_{AC}-V_{AC}$ characteristic is no longer a vertical line. Although the observed S-type curves may be different for different values of R_{DD}, the actual S-type $I_{AC}-V_{AC}$ characteristic is independent of R_{DD}. So R_{DD} is not needed in characterizing the $I_{AC}-V_{AC}$ characteristic, holding point, or threshold point.

It can be concluded from the preceding analysis that threshold current I_{TH}, threshold voltage V_H, and holding current I_H, and holding voltage V_H depend not only on transistor parameters and transistor parasitic terminal resistances, but also on the shunting resistances (R_1 and R_2) and the triggering currents (I_1 and I_2).

III. LATCHUP CRITERIA

From discussions of the DNR region in the previous section, it is concluded that so long as the regeneration paths exist in the parasitic p-n-p-n structure, the DNR region exists in the I_C-V_{CE} characteristic, and vice versa. Therefore, in the case where the DNR region exists, latchup is possible.

For the three classes of intersection points, Classes I and III correspond to two stable states whereas Class II in the DNR region corresponds to an unstable stage.

In the state of Class III, transistor Q_1 is off and transistor Q_2 is driven by triggering current I_2. After all the external triggering currents have been removed, the whole structure remains in its stable OFF state.

In the state of Class I, both transistors are stably and heavily turned on even after the external triggering currents have been removed. Although current I_C in this case is smaller than the peak current I_P, there is another current which flows into the emitter of transistor Q_1. This current is very large, and the resultant total anode–cathode current I_{AC} is also very large. This is latchup.

In the Class II state, it can be switched to the Class I state or the Class III state, depending upon external triggering. Therefore, the Class II state is a conditional stable state.

Based upon the preceding analysis, the criteria for latchup initiation can be stated as

1) the DNR region exists; and
2) only one intersection point of Class I exists (subcases $A2$, $B1$, and $C1$).

It is possible that the latchup criteria are satisfied only when the triggering currents are applied. Thus latchup may be initiated under triggering, but the OFF state will
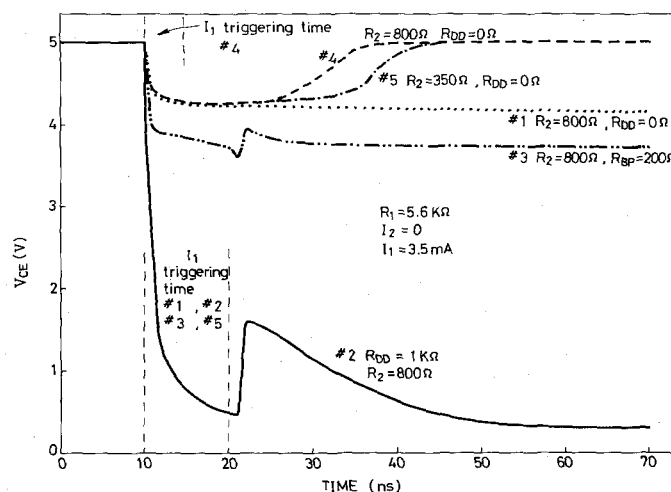

Fig. 10. Latchup transient behavior simulated by using SPICE.

be recovered when the triggering sources are removed. This kind of latchup is called the recoverable latchup. Its criteria are

1) no DNR region exists or only one intersection point of Class III exists (subcases $A1$, $B2$, and $C2$) when triggering sources are removed; and
2) the latchup criteria are satisfied when triggering sources are applied.

On the other hand, latchup which is not recoverable is called irrecoverable latchup.

Applying these criteria, the latchup condition in each subcase mentioned in the previous section can be determined. They are also listed in Table I.

In Section II-C, the effects of transistor terminal resistances and R_{DD} have been analyzed. Applying the latchup criteria, it can be concluded that the effects of transistor terminal resistances are to decrease the latchup threat whereas the resistance R_{DD} causes no considerable change on latchup initiation. Therefore, in the worst case consideration, only R_1 and R_2 are needed to characterize latchup.

To verify the proposed latchup criteria, SPICE transient simulations have been performed. Part of the results are shown in Fig. 10 where V_{CE} as a function of time is plotted. Curves 1, 2, and 3 of Fig. 10 are generated from a p-n-p-n structure in subcase $A3$ with no triggering and in subcase $A2$ under triggering. As may be seen from curve 1, the intersection point is changed to the Class I under enough long-time triggering and remains at the Class I intersection point after the triggering is removed. This is an irrecoverable latchup. If $R_{DD} = 1$ kΩ is added, the voltage at the Class I intersection point is lowered as shown in curve 2. Similarly, if $R_{BP} = 200$ Ω is added, the voltage at the Class I intersection point is also lowered as shown in curve 3.

The latchup criteria described here are valid for enough long-time triggering. If the triggering time is short, an irrecoverable latchup may become a recoverable one, as shown in curve 4. This paper will not deal with such dynamic latchup.
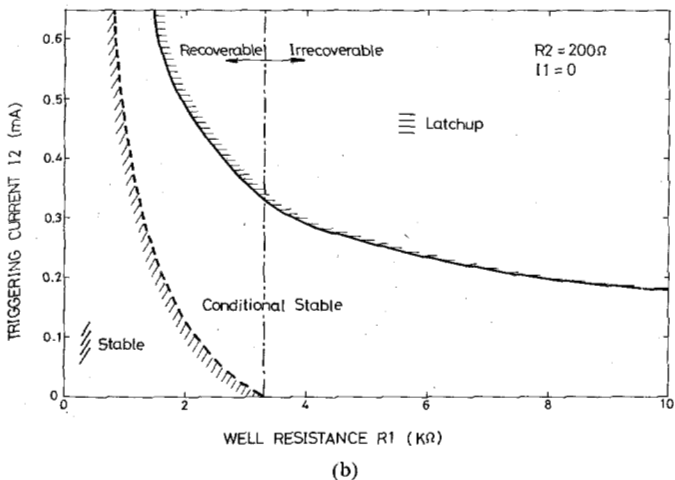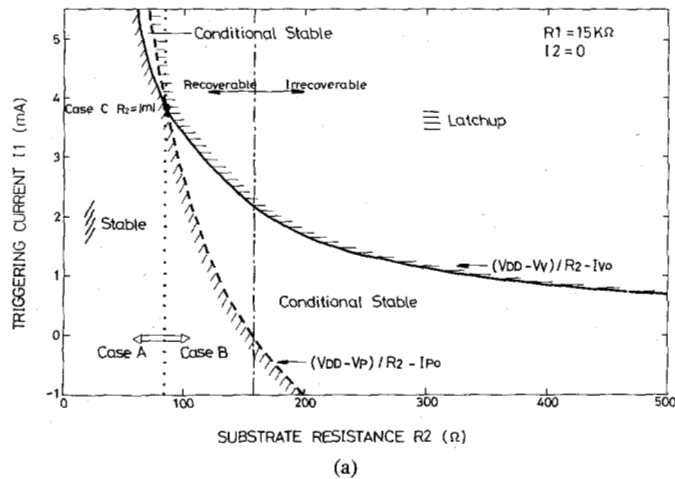
(a)

(b)

Fig. 11. Latchup features under different (a) triggering current I_1 and substrate resistance R_2, and (b) triggering current I_2 and well resistance R_1.

Fig. 12. Cross-sectional view of the test pattern for latchup measurement and investigation.
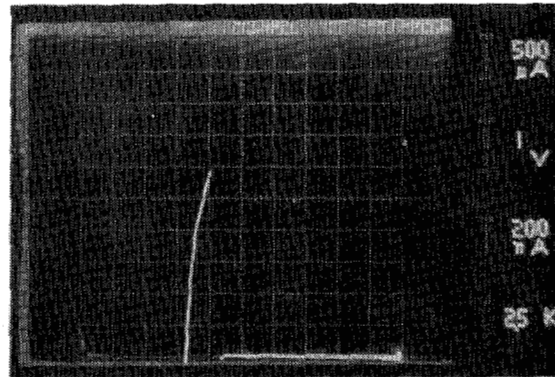
Fig. 13. Typical experimental lambda-type I_C–V_{CE} characteristic observed on the curve tracer.

Curve 5 is for a p-n-p-n structure in subcase $A1$ with no triggering and in subcase $A2$ under triggering. This is a recoverable latchup despite any triggering. Therefore, after the triggering is removed, the intersection point recovers to Class III, as may be seen from curve 5.

Using the latchup criteria and the results in Section II-B, the effect of R_2 and I_1 on latchup can be clearly determined. Fig. 11(a) shows such an effect in the case of $I_2 = 0$ and $R_1 = 15$ kΩ. The two solid lines are plotted from $I_1 = (V_{DD} - V_P)/R_2 - I_{P0}$ and $I_1 = (V_{DD} - V_V)/R_2 - I_{V0}$. Three cases and various latchup conditions are also indicated in this figure. A similar figure can be drawn for R_1 and I_2, as shown in Fig. 11(b). These figures can serve as good design guidelines to avoid latchup.

IV. EXPERIMENTAL RESULTS

An experimental p-n-p-n structure for latchup testing had been designed and fabricated using conventional p-well CMOS technology. A cross-sectional view of the test structure is shown in Fig. 12 where substrate resistance R_2 and well resistance R_1 can be determined from the spacings between the n$^+$ region and the p$^+$ region both connected to V_{DD} in the substrate and both connected to the ground in the p-well region, respectively. The spac-
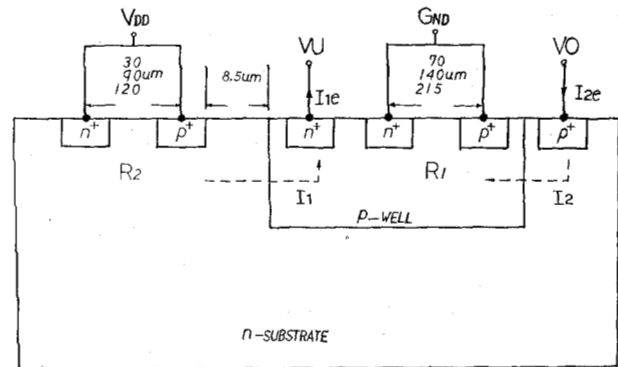
ings between the n$^+$ and p$^+$ regions in the substrate are 30, 90, and 120 μm whereas those in the well region are 70, 140, and 215 μm, as shown in Fig. 12. One extra n$^+$ region in the p-well and one extra p$^+$ region in the substrate serve as the emitters of the triggering transistors.

The λ-type I_C–V_{CE} characteristic can be measured by connecting the n$^+$ and the p$^+$ regions in the p-well to the ground while separating the n$^+$ region in the n-substrate from the V_{DD} connection and applying a variable V_{CE} on it. Therefore, the voltage V_{CE} is applied between the collector region of n-p-n transistor Q_2 (i.e., the base region of p-n-p transistor Q_1) and the emitter region of n-p-n transistor Q_2. Fig. 13 shows a typical λ-type I_C–V_{CE} characteristic obtained on a curve tracer. The power supply voltage V_{DD} in this case is 5 V and both triggering currents are not applied. Voltage V_{CE} is a variable dc voltage provided by the curve tracer under dc mode operation. When tracing V_{CE} from high voltage to low voltage, the λ curve can be clearly seen except in the DNR region. In this region, the curve is so sharp that the tracing time of electron beams is very short and the resultant brightness of the screen is not visible. The peak and valley points, however, can be definitely displayed, as shown in Fig. 13.

The measured currents and voltages at the peak and valley points as well as voltage V_Z at the zero point are listed in Table II for three different p-n-p-n test structures. Also listed in this table are the calculated results of (1)–(4) with independently measured device parameters listed in Table

TABLE II
EXPERIMENTAL AND CALCULATED PEAK AND VALLEY POINTS IN THE
LAMBDA-TYPE I_C–V_{CE} CHARACTERISTICS

R_1	I_p (mA)		V_p (V)		V_p'(V)	I_V (mA)		V_V (V)		V_Z (V)	
(Ω)	exp.	cal.	exp.	cal.	cal.	exp.	cal.	exp.	cal.	exp.	cal.
2.8K	2.94	3.19	4.0	4.25	3.99	-0.2	-0.094	4.25	4.33	3.62	3.67
4.2K	4.23	4.23	4.08	4.25	4.10	-0.1	-0.094	4.30	4.33	3.65	3.64
6.3K	4.67	4.62	4.05	4.24	4.11	-0.05	-0.094	4.35	4.33	3.82	3.58

TABLE III
DEVICE PARAMETERS USED IN THE THEORETICAL CALCULATIONS

Parameters	Q_2 (NPN)	Q_1 (PNP)
I_{SO} (A)	1.4E-15	1.0E-15
β_F	314.1	1.491
β_R	2.0	0.5
θ	2.242E-6	2.025E-6
HC	150	150

III and with different values of R_1. The measurement method of the device parameters is the conventional one [11] whereas the values of R_1 are determined partly by measurements and partly by calculations. Due to the multidimensional nonuniform spreading nature of well resistance R_1, the error in these values of R_1 is inevitable. With the error of R_1 and the error of the lumped latchup model, however, general agreement between the measured and calculated results in Table II still can be obtained.

Note that in calculating the peak voltage denoted by V_p' and the voltage V_Z in Table II, $R_{BP} = 50 \Omega$ has been used and the calculation method introduced in Section II-C has been applied. The resultant values of V_p' and V_Z have a good agreement with the experimental values.

To observe latchup behavior under the triggering of I_1 and I_2, constant voltages denoted by VO and VU were applied to the emitters of the two triggering transistors, as indicatd in Fig. 12. Thus the triggering currents I_1 and I_2 can be generated. Under enough positive voltage of VO or negative voltage of VU, the p-n-p-n structure under test was triggered into the high conduction state with large power supply current and was kept in that state after the voltage VO or VU was taken away. This phenomenon evidently is latchup. The currents I_{1e} and I_{2e} at the emitter nodes of the two triggering transistors which have been recorded at the instant when latchup occurred, are listed in Table IV. To avoid complexity, voltages VO and VU were separately applied.

Also listed in Table IV are the collector–emitter voltages V_{CE} after latchup. These voltages denoted as V_F were measured after voltages VO and VU were taken away.

The values of I_{1e} and I_{2e} can be calculated by first calculating the required I_1 and I_2 for latchup using the methods described in Sections II and III. Then the calculated values of I_1 and I_2, which are collector currents of the triggering transistors, are transformed into the corresponding

TABLE IV
EXPERIMENTAL AND CALCULATED RESULTS OF THE TRIGGERING CURRENTS IN
THE LATCHUP TEST

R_2	R_1	I_{1e} (mA)		I_{2e} (mA)		V_F (V)	
(Ω)	(Ω)	exp.	cal.	exp.	cal.	exp.	cal.
750	2.8K	0.830	0.984	0.525	0.470	3.090	3.830
	4.2K	0.883	0.983	0.214	0.263	3.180	3.812
	6.3K	0.848	0.983	0.110	0.159	3.550	3.768
900	2.8K	0.776	0.836	0.522	0.458	3.041	3.804
	4.2K	0.767	0.835	0.209	0.255	3.010	3.787
	6.3K	0.756	0.835	0.092	0.150	3.551	3.741
1.2K	2.8K	0.701	0.651	0.502	0.434	3.042	3.774
	4.2K	0.709	0.650	0.199	0.248	3.020	3.753
	6.3K	0.701	0.650	0.086	0.147	3.522	3.701

emitter currents I_{1e} and I_{2e}. On the other hand, V_F is calculated approximately from the voltage at the intersection point formed by the straight line between the peak point and the zero point and the load line. This intersection point is just the Class I intersection point mentioned in Section II-C. The device parameters used in these calculations are those listed in Table III whereas the values of R_2 are listed in Table IV. The general agreement between experimental results and theoretical calculations confirms the correctness of the proposed latchup model. Using this model, one can predict latchup initiation when triggering currents I_1 and I_2 are applied.

V. SUMMARY AND DISCUSSION

In this study, a new approach is proposed to characterize CMOS latchup from its λ-type I–V characteristics. Based upon the lumped equivalent circuit, the peak and valley points in the λ-type I–V characteristics are definitely formulated. When combined with the load line, the features of intersection points are determined and then latchup criteria are set. Using the criteria, latchup initiation can be predicted by determining whether the triggering currents exceed their calculated ratings. Furthermore, the effects of various device parameters on latchup can also be visualized. Transient simulations and experiments on latchup have been performed. Their results generally are consistent with the theoretical calculations.

It has been shown in this work that substrate resistance R_2 and well resistance R_1 are the most important parameters in modeling latchup because they represent the worst case consideration and the appearance of all other transistor terminal resistances decreases latchup threat. Resistances R_1 and R_2, however, are difficult to characterize exactly. Since the λ-type I–V characteristics involve only one resistance, and they can be conveniently simulated, modeled, and measured, it is expected that resistances R_1 and R_2 may also be extracted from the λ-type I–V characteristics. This will be one of the topics in our further research.

APPENDIX I

Taking both the high-level injection effect and the surface leakage current effect into consideration, the terminal currents of both transistors can be written as [11]

$$I_{B1} = (I_{S10}/\beta_{F1}) \, (e^{-V_{BE1}/V_T} - 1)$$
$$+ \, (I_{S10}/\beta_{R1}) \, [e^{-(V_{BE1} - V_{CE1})/V_T} - 1]$$
$$+ HC_1 I_{S10} \, (e^{-V_{BE1}/2V_T} - 1) \quad (A1)$$

$$I_{C1} = I_{S1} \cdot e^{-V_{BE1}/V_T} \, (1 - e^{V_{CE1}/V_T})$$
$$- (I_{S1}/\beta_{R1}) \, [e^{-(V_{BE1} - V_{CE1})/V_T} - 1] \quad (A2)$$

$$I_{B2} = (I_{S20}/\beta_{F2}) \, (e^{V_{BE2}/V_T} - 1)$$
$$+ (I_{S20}/\beta_{R2}) \, (e^{(V_{BE2} - V_{CE2})/V_T} - 1]$$
$$+ HC_2 \cdot I_{S20} \, [e^{V_{BE2}/2V_T} - 1] \quad (A3)$$

$$I_{C2} = I_{S2} \cdot e^{V_{BE2}/V_T} \, [1 - e^{-V_{CE2}/V_T}]$$
$$- (I_{S2}/\beta_{R2}) \, [e^{(V_{BE2} - V_{CE2})/V_T} - 1] \quad (A4)$$

$$I_{S1} = I_{S10}/(1 + \theta_1 \cdot e^{-V_{BE1}/2V_T}) \quad (A5)$$

$$I_{S2} = I_{S20}/(1 + \theta_2 \cdot e^{V_{BE2}/2V_T}). \quad (A6)$$

According to the equivalent circuit of Fig. 2, the relations between terminal currents and voltages are

$$I_{B2} = I_{C1} + I_2 - V_{BE2}/R_1 \quad (A7)$$

$$I_C = I_{C2} - I_{B1} + I_1 \quad (A8)$$

$$V_{CE1} = V_{BE2} - V_{DD} \quad (A9)$$

$$V_{BE1} = -V_{DD} + V_{CE2} \quad (A10)$$

$$V_{CE2} = V_{CE}. \quad (A11)$$

Substituting (A9)–(A11) into (A2) and (A3) and then from (A7), we have

$$(I_{S20}/\beta_{F2}) \, (e^{V_{BE2}/V_T} - 1)$$
$$+ (I_{S20}/\beta_{R2}) \, [e^{(V_{BE2} - V_{CE})/V_T} - 1]$$
$$+ HC_2 \cdot I_{S20} \, (e^{V_{BE2}/2V_T} - 1)$$
$$= I_{S1} \, [e^{(V_{DD} - V_{CE})/V_T} - e^{(V_{BE2} - V_{CE})/V_T}]$$
$$- (I_{S1}/\beta_{R1}) \, [e^{(V_{BE2} - V_{CE})/V_T} - 1]$$
$$+ I_2 - V_{BE2}/R_1. \quad (A12)$$

Similarly, (A8) can be rewritten as

$$I_C = I_{S2} \, [e^{V_{BE2}/V_T} - e^{(V_{BE2} - V_{CE})/V_T}]$$
$$- (I_{S2}/\beta_{R2}) \, [e^{(V_{BE2} - V_{CE})/V_T} - 1]$$
$$- (I_{S10}/\beta_{F1}) \, [e^{(V_{DD} - V_{CE})/V_T} - 1]$$
$$- (I_{S10}/\beta_{R1}) \, [e^{(V_{BE2} - V_{CE})/V_T} - 1]$$
$$- HC_1 \cdot I_{S10} \, [e^{(V_{DD} - V_{CE})/2V_T} - 1] + I_1. \quad (A13)$$

Since the peak point specified by the peak current I_P and the peak voltage V_P is the absolute maximum point in the λ-type I_C–V_{CE} curve with fixed I_2, so at $V_{CE} = V_P$, we have

$$dI_C/dV_{CE}|_{V_{CE} = V_P}$$
$$= \partial I_C/\partial V_{CE}|_{V_{BE2} = \text{constant}} + \partial I_C/\partial V_{BE2}|_{V_{CE} = \text{constant}}$$
$$\cdot \partial V_{BE2}/\partial V_{CE}$$
$$= 0 \quad (A14)$$

In (A14), the term $\partial V_{BE2}/\partial V_{CE}$ can be derived from (A12) whereas the other terms can be obtained from (A13). The final expression is

$$(1 + 1/\beta_{R2}) \cdot I_{S2}/V_T \cdot e^{(V_{BE2} - V_P)/V_T}$$
$$+ I_{S10}/\beta_{R1}/V_T \cdot e^{(V_{BE2} - V_P)/V_T}$$
$$+ I_{S10}/\beta_{F1}/V_T \cdot e^{(V_{DD} - V_P)/V_T}$$
$$+ \{- I_{S20} \cdot \theta_2 \cdot e^{V_{BE2}/2V_T}/(2V_T)/(1 + \theta_2 \cdot e^{V_{BE2}/2V_T})^2$$
$$\cdot [e^{V_{BE2}/V_T} - (1 + 1/\beta_{R2}) \cdot e^{(V_{BE2} - V_P)/V_T} - 1/\beta_{R2}]$$
$$+ I_{S2}/V_T \cdot [e^{V_{BE2}/V_T} - (1 + 1/\beta_{R2}) \cdot e^{(V_{BE2} - V_P)/V_T}]$$
$$- I_{S10}/\beta_{R1}/V_T \cdot e^{(V_{BE2} - V_P)/V_T}$$
$$- HC_1 \cdot I_{S10}/(2V_T) \cdot e^{V_{BE2}/2V_T}\} \cdot F/G = 0$$

$$(A15)$$

where

$$F = I_{S20}/(\beta_{R2} \cdot V_T) \cdot e^{(V_{BE2} - V_P)/V_T}$$
$$- I_{S1}/V_T \cdot [e^{(V_{DD} - V_P)/V_T}$$
$$- (1 + 1/\beta_{R1}) \cdot e^{(V_{BE2} - V_P)/V_T}]$$
$$+ \theta_1 \cdot e^{(V_{DD} - V_P)/V_T}/(2V_T)/(1 + \theta_1$$
$$\cdot e^{(V_{DD} - V_P)/2V_T})^2$$
$$\cdot [I_{S10} \cdot e^{(V_{DD} - V_P)/V_T}$$
$$- I_{S10} \, (1 + 1/\beta_{R1})$$
$$\cdot e^{(V_{BE2} - V_P)/V_T} + I_{S10}/\beta_{R1}]$$

$$G = I_{S20}/V_T \cdot [1/\beta_{F2} \cdot e^{V_{BE2}/V_T}$$
$$+ HC_2/2 \cdot e^{V_{BE2}/2V_T}]$$
$$+ I_{S20}/\beta_{R2}/V_T \cdot e^{(V_{BE2} - V_P)/V_T}$$
$$+ I_{S1} \, (1 + 1/\beta_{R1}) + e^{(V_{BE2} - V_P)/V_T}/V_T + 1/R1.$$

APPENDIX II

According to the magnitude of the slopes of both load line and λ line, three different cases must be considered.

1) *Case A:* The magnitude of the slope of the load line is smaller than that of the λ line, i.e., $R_2 >$

$|m|$. This case is indicated in Fig. 7 where according to the value of V_{CEAI}, there are three subcases.

i) Subcase $A1$: $V_{CEAI} < V_P$. As may be seen from the curves of Fig. 7, there is only one true intersection point of Class III. Using (7), the condition $V_{CEAI} < V_P$ can be rewritten as

$$I_1 < (V_{DD} - V_P)/R_2 - I_{P0} \tag{B1}$$

where I_{P0} is equal to $I_P - I_1$ and is independent of I_1.

ii) Subcase $A2$: $V_{CEAI} > V_V$. Only one intersection point of Class I exists. The condition is

$$I_1 > (V_{DD} - V_V)/R_2 - I_{V0} \tag{B2}$$

where I_{V0} is equal to $I_V - I_1$ and is independent of I_1.

iii) Subcase $A3$: $V_P < V_{CEAI} < V_V$. The artificial intersection point is just the true intersection point of Class II. There are two other true intersection points of Class I and Class III. The condition is

$$(V_{DD} - V_P)/R_2 - I_{P0} < I_1 < (V_{DD} - V_V)/R_2 - I_{V0}. \tag{B3}$$

2) Class B: The magnitude of the slope of the load line is larger than that of the λ line, i.e., $R_2 < |m|$. Three different subcases are considered as shown in Fig. 8.

i) Subcase $B1$: $V_{CEAI} < V_P$. There is only one true intersection point of Class I. The condition in subcase $B1$ is

$$I_1 > (V_{DD} - V_P)/R_2 - I_{P0}. \tag{B4}$$

ii) Subcase $B2$: $V_{CEAI} > V_V$. There is only one true intersection point of Class III. The condition is

$$I_1 < (V_{DD} - V_V)/R_2 - I_{V0}. \tag{B5}$$

iii) Subcase $B3$: $V_P < V_{CEAI} < V_V$. The artificial intersection point is just the true intersection point of Class II. Only one such true intersection point exists. The condition in subcase $B3$ is the same as that in subcase $A3$.

3) Case C: The magnitude of the slope in the load line is just equal to that of the λ line, i.e., $R_2 = |m|$. This case is indicated in Fig. 9.

i) Subcase $C1$: There is no artificial intersection point and the peak point is in the upper side of the load line. This results in a true intersection point of Class I, as shown in Fig. 9. The condition in subcase $C1$ is the same as that in subcase $B1$.

ii) Subcase $C2$: There is no artificial intersection point and the peak point is in the lower side of the load line. This results in a true intersection point of Class III. The condition in subcase $C2$ is the same as that in subcase $A1$.

iii) Subcase $C3$: In this subcase, the peak point is just located in the load line. There are infinite number of artificial intersection points which are also the true ones of Class II. The condition for subcase $C3$ can be written as

$$I_1 = (V_{DD} - V_P)/R_2 - I_{P0}. \tag{B6}$$

REFERENCES

[1] D. B. Estreich, "The physics and modeling of latch-up and CMOS integrated circuits," Integrated Circuit Lab., Stanford Univ., Stanford, CA, Tech. Rep. G-201-9, 1980.
[2] R. R. Troutman and H. P. Zappe, "A transient analysis of latchup in bulk CMOS," IEEE Trans. Electron Devices, vol. ED-30, pp. 170–179, Feb. 1983.
[3] W. D. Raburn, "A model for the parasitic SCR in bulk CMOS," in IEDM Tech. Dig., p. 252, Dec. 1980.
[4] R. D. Rung and H. Momose, "Improved modeling of CMOS latchup and VLSI implications," in Dig. Symp. VLSI Tech. (Oiso, Japan), p. 50, 1982.
[5] D. B. Estreich and R. W. Dutton, "Modeling latchup in CMOS integrated circuits," IEEE Trans. Computer-Aided Design of ICAS, vol. CAD-1, pp. 157–162, Oct. 1982.
[6] C. C. Huang, M. D. Hartranft, N. F. Pu, C. Yue, C. Rahn, J. Schrankler, G. D. Kirchner, F. L. Hampton, and T. E. Hendrickson, "Characterization of CMOS latchup," in IEDM Tech. Dig., p. 454, Dec. 1982.
[7] D. N. Pattanayak, G. Kinoshita, J. H. Nelson, and Y. Wong, "Switching conditions for CMOS latchup path with shunt resistances," IEEE Electron Device Lett., vol. EDL-4, pp. 116–119, Apr. 1983.
[8] R. C.-Y. Fang and J. L. Moll, "Latchup model for the parasitic p-n-p-n path in bulk CMOS," IEEE Trans. Electron Devices, vol. ED-31, pp. 113–120, Jan. 1984.
[9] G. J. Hu, "A better understanding of CMOS latchup," IEEE Trans. Electron Devices, vol. ED-31, pp. 62–67, Jan. 1984.
[10] C.-Y. Wu and C.-Y. Wu, "Theoretical and experimental characterization of the dual-base transistor (DUBAT)," Solid-State Electron., vol. 23, pp. 1113–1122, Nov. 1980.
[11] I. Getreu, Modeling The Bipolar Transistor. Beaverton, OR: Tektronix, Inc., 1976.
[12] L. W. Nagel, "SPICE 2: A computer program to simulate semiconductor circuits," Univ. of California, Berkeley, May 1975.