A Simple Punchthrough Voltage Model for Short-Channel MOSFET's with Single Channel Implantation in VLSI

CHING-YUAN WU, MEMBER, IEEE, WEI-ZANG HSIAO, AND HSING-HAI CHEN

Abstract—Based on the step-profile approximation and geometrical analysis, the punchthrough voltage of short-channel enhancement n-channel MOSFET's with single channel implantation has been derived by defining a punchthrough depth. The punchthrough depth, which represents the distance of the two-dimensional potential ridge from the SiO_2–Si interface, is calculated by the surface potential of the punchthrough point. Therefore, the derived punchthrough voltage model is then analytically expressed in terms of device geometries and implant parameters. Comparisons between the developed model and the experimental devices have been made and excellent agreement has been obtained.

I. Introduction

WITH THE ADVENT of fine-line lithographic techniques, MOSFET's can be scaled down to such an extent that they are approaching the physical limits of operating principle [1]–[3]. It is also known that the circuit speed and packing density are much improved if the scaled down MOSFET's are used. It has been shown, however, that many deleterious phenomena will occur, which are hardly observed from larger dimension devices. Among these deterious phenomena, punchthrough and avalanche breakdown have been recognized to be the most important phenomena for short-channel MOSFET's [1]–[6]. The punchthrough breakdown of a MOSFET will limit the operating drain voltage to a small value and result in the unreliable operation of integrated circuits.

A simple one-dimensional analytic model for the punchthrough voltage was first developed by Taylor [7] in which the punchthrough point is assumed to be located at the SiO_2–Si interface. More recently, a more elaborate model based on geometrical analysis has been proposed by Hsu *et al.* [8]. This model, however, is only valid for a uniformly doped substrate which does not exist for present and future MOSFET's. Due to the complexity of analysis, two-dimensional numerical analyses for the punchthrough effect have been carried out by several authors [9], [10], and the punchthrough voltage is defined by a certain current level by considering the effect of drain-induced barrier lowering. Until now, there has not been an analytic model for the punchthrough voltage of channel-implanted MOSFET's, which are the practical devices used in VLSI. In this paper, an analytic model for the punchthrough voltage is presented, in which a channel-implanted profile is approximated by a step profile. Based on simple geometrical analysis, the punchthrough voltage is derived in terms of punchthrough depth and device parameters, and the punchthrough depth is calculated in terms of applied biases through surface potential. Comparisons between the experimental data and the developed model have been made, and good agreement has been obtained. Therefore, the developed model can be used as a design aid for short-channel MOSFET's in VLSI.

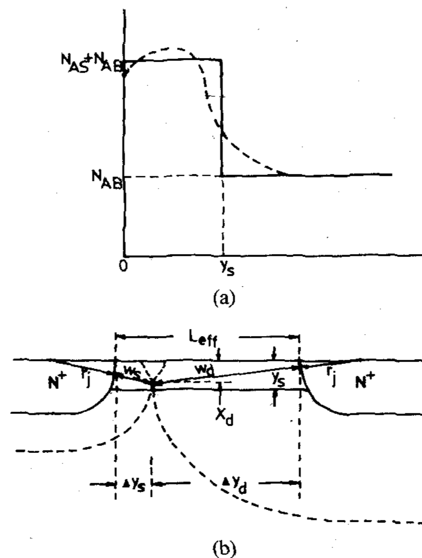

Fig. 1. (a) A double-step profile approximation for single channel implantation; (b) the geometric model for a single channel-implanted MOSFET.

II. Model Development

Assuming a step profile approximation for a single channel-implanted substrate as shown in Fig. 1(a), if the punchthrough point is located in the implanted region as shown in Fig. 1(b), a new definition for the punchthrough condition can be expressed by

$$L_{\text{eff}} - \Delta y_s - \Delta y_d = 0 \tag{1}$$

where L_{eff} is the effective channel length, Δy_s (Δy_d) is the surface distance between the punchthrough point and the edge of source (drain) diffusion island.

Manuscript received November 13, 1984; revised March 11, 1985. This work was supported by the Electronics Research and Service Organization, ITRI, Taiwan, Republic of China.

The authors are with the Institute of Electronics, National Chiao-Tung University, Hsin-Chu, Taiwan, Republic of China.

0018-9383/85/0900-1704$01.00 © 1985 IEEE

Based on geometrical analysis, we may obtain

$$\Delta y_s = [(r_j + W_s)^2 - x_d^2]^{1/2} - r_j \tag{2}$$

$$\Delta y_d = [(r_j + W_d)^2 - x_d^2] - r_j \tag{3}$$

where r_j is the source (drain) junction depth, x_d is the punchthrough depth, and W_s (W_d) is the depletion width of the source (drain) implanted layer junction.

From (2) and (3) it is clearly seen that if $x_d = 0$, i.e., the punchthrough point is located at the SiO_2–Si interface, then $\Delta y_s = W_s$, $\Delta y_d = W_d$. If x_d is increased, Δy_s and Δy_d are decreased, then the applied drain voltage needed to satisfy the punchthrough condition is increased.

If we assume that the source (drain) implanted layer junction can be treated as an abrupt p-n junction, then W_s and W_d can be easily written as

$$W_s = \left[\frac{2\epsilon_s(V_{Bi} + V_{BG})}{qN_S}\right]^{1/2} \tag{4}$$

$$W_d = \left[\frac{2\epsilon_s(V_{Bi} + V_{BG} + V_{DS})}{qN_S}\right]^{1/2} \tag{5}$$

where N_S is the doping concentration in the implanted region, which is equal to $N_{AB} + N_{AS}$, and V_{Bi} is the built-in voltage across the source (drain) implanted layer junction, which can be easily written as

$$V_{Bi} = \frac{k_BT}{q} \ln\left(\frac{N_DN_S}{n_i^2}\right). \tag{6}$$

Note that N_D is the doping concentration in the source (drain) diffusion island and n_i is the intrinsic carrier concentration of silicon.

Putting (2)–(5) into (1), we obtain the punchthrough voltage as

$$\begin{aligned} V_{PT} = \frac{qN_S}{2\epsilon_s} \{&(L_{\text{eff}} + 2r_j)^2 - 2(L_{\text{eff}} + 2r_j) \\ &\cdot [(r_j + W_s)^2 - x_d^2]^{1/2} + 2r_jW_s \\ &+ 2r_j^2 - 2r_j [(L_{\text{eff}} + r_j)^2 \\ &- 2(L_{\text{eff}} + 2r_j)[(r_j + W_s)^2 - x_d^2]^{1/2} \\ &+ 2r_jW_s + W_s^2 + r_j^2]^{1/2}\}. \end{aligned} \tag{7}$$

From (7) it is clearly seen that if $x_d = 0$, (7) can be reduced to

$$V_{PT} = \frac{qN_S}{2\epsilon_s}\left\{L_{\text{eff}} - \left[\frac{2\epsilon_s(V_{Bi} + V_{BG})}{qN_S}\right]^{1/2}\right\}^2 - (V_{Bi} + V_{BG}). \tag{8}$$

It is clearly seen that (8) is the same as that derived by Taylor [7] if $N_s = N_{AB}$.

Since the channel implanted depth becomes deeper for MOSFET's in VLSI, in order to increase the punchthrough voltage, the punchthrough point is assumed to be located in the implanted region for zero back-gate bias. Therefore, the applied gate voltage can be related to the surface potential by the following equation:

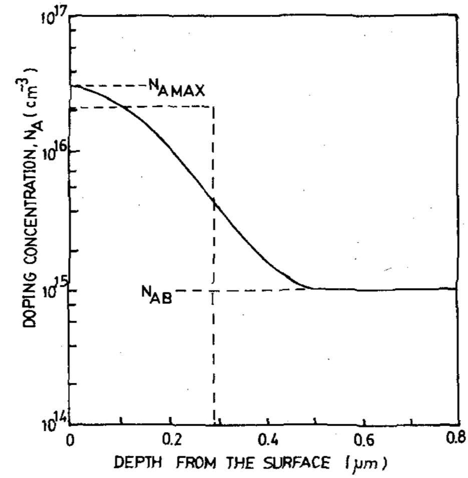

Fig. 2. Doping profile and step profile approximation for single channel implantation used in [10].

$$V_{GS} = V_{FB} + \phi_s + \frac{q(N_{AB} + N_{AS})}{C_o} x_d \tag{9}$$

where V_{FB} is the flatband voltage and C_o is the gate oxide capacitance per unit area.

The punchthrough depth x_d can be calculated by using Poisson's equation. The result is

$$x_d = \left[\frac{2\epsilon_s}{q(N_{AB} + N_{AS})}\right]^{1/2} \cdot \left[\phi_s + V_{BG} + \frac{k_BT}{q} \ln\left(1 + \frac{N_{AS}}{N_{AB}}\right)\right]^{1/2} \tag{10}$$

where $k_BT/q \ln (1 + N_{AS}/N_{AB})$ is the built-in voltage of high–low junction formed by channel implantation.

Combining (9) and (10) we may obtain an explicit form for x_d as follows:

$$x_d = \left[\frac{2\epsilon_s}{q(N_{AS} + N_{AB})}\right]^{1/2} \cdot \left\{A_1 - \frac{r_1}{2}\left[\left(1 + \frac{4A_1}{r_1}\right)^{1/2} - 1\right]\right\}^{1/2} \tag{11}$$

$$A_1 = V_{GS} + V_{BG} - V_{FB} + \frac{k_BT}{q} \ln\left(1 + \frac{N_{AS}}{N_{AB}}\right) \tag{12}$$

$$r_1 = \frac{2q(N_{AS} + N_{AB})\epsilon_s}{C_o^2}. \tag{13}$$

III. Experimental Results and Comparisons

In order to verify the accuracy of our developed model, the experimental results measured by Barnes *et al.* [10] are used to compare with our model. The implant profile used in [10] is shown in Fig. 2 and the process data and parameters used in the step profile are shown in Table I. The I–V characteristic of the measured devices (L_{eff} = 0.79, 0.9, and 1 μm) for $V_{GS} = V_{BG} = 0$ is shown in Fig. 3. Based on the current level definition [10], the punch-

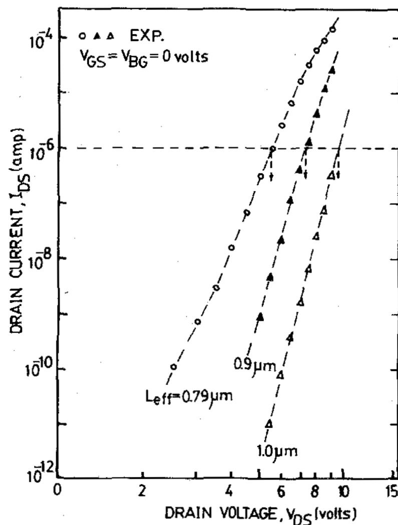

Fig. 3. The *I–V* characteristics of the fabricated short-channel MOSFET's presented in [10].

TABLE I
DEVICE PARAMETERS USED FOR SIMULATIONS

Parameters				Values
Region	Shape	Quantities		
Source and Drain	Gaussian	Maximum Concentration	$N_{SMax}(cm^3)$	1.0×10^{19}
		Standard Deviation	σ_s (μm)	0.065
		Junction Depth	X_j (μm)	0.28
Channel	Gaussian	Maximum Concentration	$N_{AMax}(cm^{-3})$	2.9×10^{16}
		Standard Deviation	σ_c (μm)	0.17
		Range	R_p	0.0
Substrate Doping Concentration			$N_{AB}(cm^{-3})$	1.0×10^{15}
Gate Oxide Thickness			t_{ox} (nm)	40
Simulated parameters (step profile)		V_{FB} (v)		-0.3
		y_s (μm)		0.2942
		$N_{AS}(cm^{-3})$		2.10×10^{16}

through voltages of these three devices are compared with our model and are shown in Fig. 4. It is clearly seen that good agreement between the experimental results and our simple model has been obtained. Moreover, in order to further verify the accuracy of our simple model, short-channel devices were measured which were fabricated on a production line. The basic parameters extracted from the threshold voltage measurements and the process parameters are listed in Table II. The *I–V* characteristic of the measured devices ($L_{eff} \doteq$ 1.20, 1.30, and 1.35 μm) are shown in Fig. 5. Similarly, based on current level definition (10^{-6} A) [10], comparisons between our experimental measurements and the theoretical model are shown in Fig. 6. Again, good agreement between these comparisons has

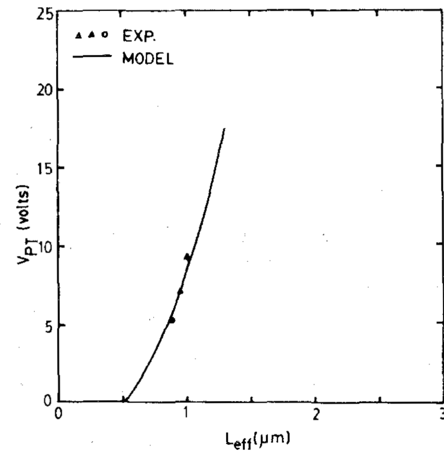

Fig. 4. Comparisons between the measured punchthrough voltage (from Fig. (2)) and the developed model. The parameters used for simulation are cited in Table I.

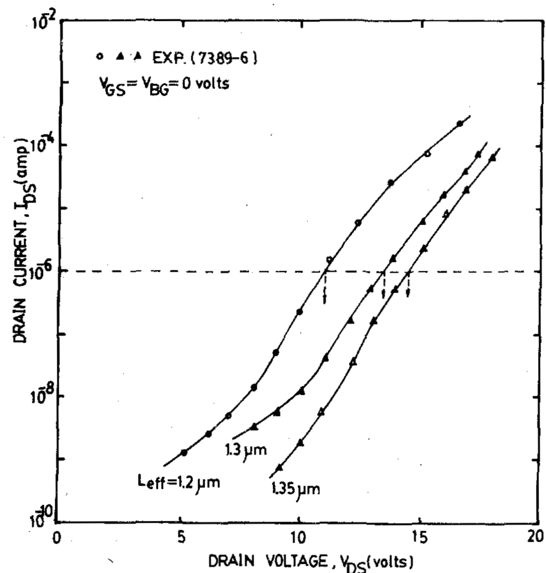

Fig. 5. The *I–V* characteristics of the fabricated short-channel MOSFET's (wafer 7389-6).

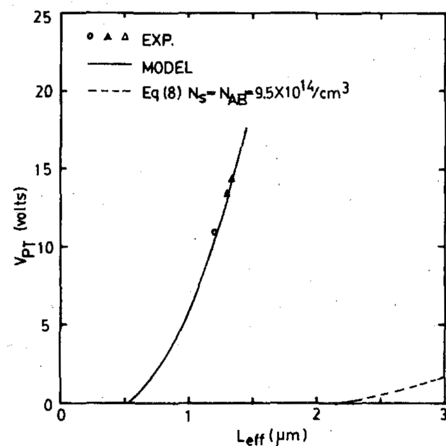

Fig. 6. Comparisons between the measured punchthrough voltage (from Fig. (3)) and the developed model. The parameters used for simulation are cited in Table II.

TABLE II
DEVICE PARAMETERS OF WAFER 7389-6 USED FOR SIMULATIONS

Specification \ Wafer No.		7389-6
Source And Drain Junction Depth (μm)		0.4
Gate Oxide Thickness (A)		602
Substrate Doping Concentration (cm^{-3})		9.50×10^{14}
Effective Channel Width (μm)		48.35
Source And Drain Doping Concentration (cm^{-3})		1.00×10^{20}
Channel Implant (Across Gate oxide)	Energy (Kev)	30
	Dose (cm^{-2})	3.1×10^{11}
Simulated Parameters (Step-Profile)	V_{FB} (Volt)	-0.89
	Y_S (μm)	0.18
	N_{AS} (cm^{-3})	1.67×10^{16}

been obtained, which strongly supports the accuracy of our simple model. Moreover, comparisons between the experimental data and the results of Taylor's model are shown in Fig. 6, in which $N_s = N_{AB} = 9.5 \times 10^{14}/\text{cm}^3$ is used in (8). It is clearly seen that a large discrepancy is obtained by using Taylor's model.

It should be noted that the developed simple model is not valid as the punchthrough point is located in the substrate region. This situation will occur when the back gate is applied. The analysis of this case is slightly complicated and will be presented elsewhere. As the back-gate bias is applied, however, the punchthrough depth becomes deeper and the punchthrough voltage is increased. Therefore, the punchthrough voltage at zero back-gate bias becomes the worst case for the MOSFET's, which is important for a device designer.

IV. CONCLUSION

This paper has presented a simple model for the punchthrough voltage of n-channel enhancement MOSFET's fabricated with single channel implantation. In order to verify the developed model, comparisons between the experimental measurements and the developed model have been made. It is shown that excellent agreement has been obtained. Although the developed model is only valid for the case where the punchthrough point is located in the channel-implanted region, it can be used to predict the worst case of the punchthrough voltage for short-channel MOSFET's (below 1 μm) in VLSI.

REFERENCES

[1] Y. El-mansy. "MOS device and technology constraints in VLSI," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 567–573, Apr. 1982.
[2] B. Eitan and D. Frohman-Bentchkowsky, "Surface conduction in short-channel MOS devices as a limitation to VLSI scaling," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 254–264, Feb. 1982.
[3] H. Y. Yu, A Reisman, C. M. Osburn, and D. L. Critchlaw, "1-μm MOSFET VLSI technology: Part I—An overview," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 240–246, Apr. 1979.
[4] W. Muller, L. Risch, and A. Schutz, "Short channel MOS transistors in avalanche-multiplication regime," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 1778–1784, Nov. 1982.
[5] C. M. Wu and K. W. Yeh, "Safty drain voltage avoiding avalanche breakdown in MOSFET's," *IEEE Electron Device Lett.*, vol. EDL-3, pp. 245-247, Sept. 1983.
[6] E. Sun, J. Berger, and B. Alders, "Breakdown mechanism in short channel MOS transistors," in *IEDM Tech. Dig.*, pp. 478–482, 1978.
[7] G. W. Taylor, "Subthreshold conduction in MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-25, pp. 337–350, Mar. 1978.
[8] F. C. Hsu, R. S. Muller, C. Hu, and P. K. Ko, "A simple punchthrough model for short-channel MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 1354–1359, Oct. 1983.
[9] N. Kotani and S. Kawazu, "Computer analysis of punchthrough in MOSFET's," *Solid-State Electron.*, vol. 22, pp. 63–70, Jan. 1979.
[10] J. J. Barnes, K. Shimohigashi, and R. W. Dutton, "Short-channel MOSFET's in the punchthrough current mode," *IEEE Trans. Electron Devices*, vol. ED-26, no. 4, pp. 446–452, Apr. 1979.