國 立 交 通 大 學

機械工程學系

博 士 論 文

高介電常數介電質金氧金電容應用於動態記憶體與射頻元件之研究

The Research on Metal-Insulator-Metal Capacitor Using High-κ Dielectrics for DRAM/RF Application

研 究 生：鄭淳護

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摘要

隨著超大型積體電路技術的日新月異、元件尺寸的不斷縮微，為配合現今類比、射頻通訊和記憶體元件的發展，金氧金電容(MIM)的研發是刻不容緩的。在各種不同的被動元件中，金氧金電容經常被廣泛的應用在射頻電路裡的阻抗匹配與直流濾波器中；而且它們通常佔據了很大比例的電路面積。因此，為了有效降低晶片的面積與成本，提高單位面積的電容值是極為需要的。為了符合未來記憶體元件的高電容密度需求，高介電系數材料的開發似乎是唯一的選擇，但增加介電常數和減少元件厚度所伴隨而來的高漏電，更是目前研究的主要議題之一。而目前已開發和尚在研究的高介電常數材料包含氧化鋁(Al_2O_3)、氧化鉭(Ta_2O_5)、氧化鋯(ZrO_2)和鈦酸鍶($SrTiO_3$)等。

雖然，鈦酸鍶介電質($SrTiO_3$)具有高介電常數(κ ~50-200)，但小的導帶不連續(conduction band discontinuity)和能帶寬度(bandgap)，將易造成較大的漏電。除此之外，鈦酸鍶介電質必須要有結晶相產生才能有較高的介電常數(κ~150-170)，而要形成奈米結晶 (nano-crysatl)的鈦酸鍶，則需要較高的製程溫

度(>450°C)。

因此，我們針對以上鈦酸鍶介電質所產生的問題，開發出一系列和二氧化鈦相關(TiO_2-based)的材料，其中包括了鉿化鈦氧化物(TiHfO)、鑭化鈦氧化物(TiLaO)和鋯化鈦氧化物(TiZrO)。除了之外，我們也成功的發展出一種雙電漿處理(Dual plasma treatment)下電極的方法，我們藉由這個方法搭配這些高介電質材料，成功的開發出高性能的金氧金電容，不但在漏電上有大幅的改善，更改良了電壓電容係數(Voltage coefficient of capacitance)和的溫度電容係數(Temperature coefficient of capacitance)。最後，我們針對鈦酸鍶介電質進行定電壓應力測試(constant voltage stress test)，去觀察其電性和類比特性上的變化，進而推估元件的可靠度。此一電容可靠度測試的方法將可用來作為未來金氧金電容在動態記憶體及高頻應用上的評估。

The Research of Metal-Insulator-Metal Capacitor Using High-κ as Dielectrics for DRAM/RF Application

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Abstract

According to International Technology Roadmap for Semiconductors (ITRS), the continuous increasing capacitance density ($\varepsilon_0\kappa/t_\kappa$) is required to scale down the device size of Metal-Insulator-Metal (MIM) capacitors that are widely used for Analog, RF and DRAM functions. To meet these requirements, the using higher κ dielectric is the only choice since the decreasing dielectric thickness (t_κ) increases the unwanted leakage current exponentially. To achieve this goal the only choice is to increase the κ value of the dielectrics, which have evolved from Al_2O_3, Ta_2O_5 (κ ~25), ZrO_2 (κ ~30), to $SrTiO_3$ (κ~50-200).

Although $SrTiO_3$ has a large dielectric (κ ~50-200), the small conduction band offset (-0.1eV) and bandgap to lead larger leakage current is an important issue. And $SrTiO_3$ showed higher k values by forming nano-crystals, this only occurs at a high process temperature >450°C.

We have developed successfully a dual plasma treatment on bottom surface to reduce the growth of interracial layer and then adopted high-κ TiO_2 (κ~50-80) to mix medium-κ dielectric with large conduction band offset as a dielectric to improve the electrical and analog characteristic of MIM capacitors. These TiO_2-based dielectrics (κ ~40-50) such as TiHfO, TiLaO and TiZrO exhibit good performance and thermal stability. On the other hand, stress degradation is especially a concern in low-breakdown field and small-bandgap STO materials, which also leads to high leakage currents because of the small conduction band discontinuity (ΔE_C) with respect to Si. Here we describe the stress behavior on electrical and analog characteristics of hi-κ MIM capacitors from low frequencies (100 kHz~1 MHz) to high frequencies (1 GHz~20 GHz). This method will be beneficial to the reliability evaluation of MIM capacitors for DRAM/RF application.

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謹以此論文獻給我最親愛的家人，謝謝你們～

淳護

戊子年於交通大學

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Chapter 1

Introduction

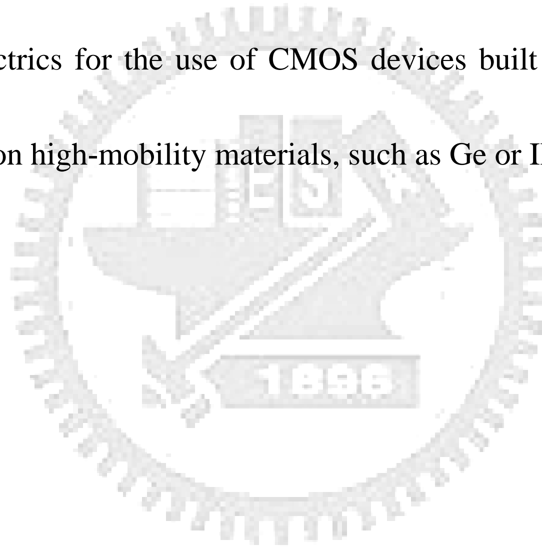
1.1 Motivation to Study High-κ Dielectrics

In the scaling of CMOS devices, reducing the thickness of gate stack with lower leakage current plays an important role. Although the leakage current of the devices with the same gate dielectric reduces with the scaling gate length and width, that leakage current density increases with the scaling of gate dielectrics exponentially. Therefore, the gate leakage current increases as the device size decreases. The larger leakage current will not only cause the higher power consumption but also degrade the reliability of the devices.

Using the material with high dielectric constant (high-κ), the physical thickness of the dielectric in the devices can be increased without sacrificing capacitance density. According to the ITRS (International Technology Roadmap for Semiconductor) [1-1] of SIA as shown in Figure 1-1, the thickness of gate oxide have to be below 1nm after 2009. Moreover, the gate length and bias voltage reduces by 11 % every year while the driving current has to be maintained. Therefore, the continual scaling of gate dielectric is a trend in CMOS technology. Even some high-κ dielectrics show good electrical characteristics at low frequency, the performance of

those at RF region could possibly degrade. Therefore, it is necessary to find out the high-κ dielectrics that can exhibit good analog characteristics for RF application.

After years of research, some high-κ dielectrics (HfO_2, ZrO_2 and TiO_2) have been widely studied and related characteristics and issues of these materials have also been reported. In addition, high-k gate dielectrics and metal gate electrodes has been introduced in 45nm and achieved good performance for both NMOS and PMOS transistors. To build next-generation transistor, it is important to find out the most suitable high-κ dielectrics for the use of CMOS devices built upon conventional Si substrate or non-silicon high-mobility materials, such as Ge or III-V substrates.



1.2 The Background of High-κ Dielectrics used for DRAM and RF Application

The first of the above requirements is that the oxide's κ value should be over 12, preferably 25-30. There is a trade off with the band offset condition, which requires a reasonably large band gap. Figure 1-2 and Figure 1-3 show that the κ of candidate oxides tends to vary inversely with the band gap, so we must accept a relatively low κ value. There are numerous oxides with extremely large dielectric constant, such as $SrTiO_3$ (κ ~50-200) or $BaSrTiO_3$ (κ ~250-350), which are candidates in DRAM capacitors, but these materials have a small conduction band offset and band gap.

According to International Technology Roadmap for Semiconductors (ITRS), the continuous increasing capacitance density ($\varepsilon_0\kappa/t_\kappa$) is required to scale down the device size of Metal-Insulator-Metal (MIM) capacitors that are widely used for Analog, RF and DRAM functions. To meet these requirements, the using higher κ dielectric is the only choice since the decreasing dielectric thickness (t_κ) increases the unwanted leakage current exponentially. To achieve this goal the only choice is to increase the κ value of the dielectrics, which have evolved from TiO_2 (κ~50-80) [1-13], TiHfO (κ~40-50) [1-6], TiTaO (κ~40-50) [1-7]-[1-9] to $SrTiO_3$ (STO; κ~50-200) [1-10]-[1-12].

It has been reported that titanium oxide (TiO_2) exhibits some better properties than other dielectrics in addition to the higher dielectric constant (κ ~50-80). One of

that is the good thermal stability when it was integrated with TiN electrode. It allows TiO_2 shows dielectric characteristics after high temperature process for silicide formation. Besides, the heat conduction rate for TiO_2 is higher than that for SiO_2. With the scaling of integrated circuits, the issue of power dissipation should also be taken into account. Although TiO_2 exhibits the above merits, there are still some other issues that should be considered and overcome such as the higher leakage current than that of other dielectrics with the same effective oxide thickness, lower breakdown voltage and interface oxide layer formation after post implant RTA. However, it has been reported that thickness of the interface oxide layer can be reduced by using NH_3 plasma treatment, but the effect of N^+ plasma for bottom interface is limited beyond 1nm of EOT.

$SrTiO_3$ (STO) has been widely studied as a substrate for high T_C oxide superconductors. Its alloy $BaSrTiO_3$ has been widely studied as a high dielectric constant dielectric for DRAM capacitors. $SrTiO_3$ (STO) well-known perovskite-type structure is a potential candidate to increase the κ value beyond a value of 45. To achieve the high κ value, the STO requires a heat treatment at 450~500^oC under an oxygen ambient for crystallization. Therefore, it also requires a Pt or RuO_2 lower electrode to withstand the high temperature oxidation, but the high cost and availability of noble metals pose concerns for mass production.

The continuous scaling of design rules for DRAM leaves us some difficulties to overcome. From the requirement of stacked capacitor showed in Fig. 1-5 (a) and trench capacitors showed in Fig. 1-5 (b) in ITRS roadmap, the major obstacle in scaling of the DRAM capacitor is scaling of t_{eq} for capacitor dielectrics. According to 2007 ITRS roadmap [1-1], one of the difficult challenges is scaling of the physical dielectric thickness, T_{phy} (physical thickness) while maintaining dielectric constant and leakage current of dielectrics. In general, as the physical thickness of high-κ materials such as $SrTiO_3$ decreases, the dielectric constant decreases and the leakage current increases. This means higher T_{phy} while decreasing $T_{eq.}$. In the G-bit DRAM generation, the memory cell density is so high that the cell space can only allow dielectrics no thicker than 20nm. This requirement of thickness for dielectrics makes it impossible to use quaternary metal oxide such as $SrTiO_3$ or $BaSrTiO_3$ as the dielectric layers. Because of the difficulty of conformal CVD for these quaternary oxide, the high aspect ratio of the trench for DRAM seems to be the other challenge to integrate these dielectrics into G-bit DRAM generation.

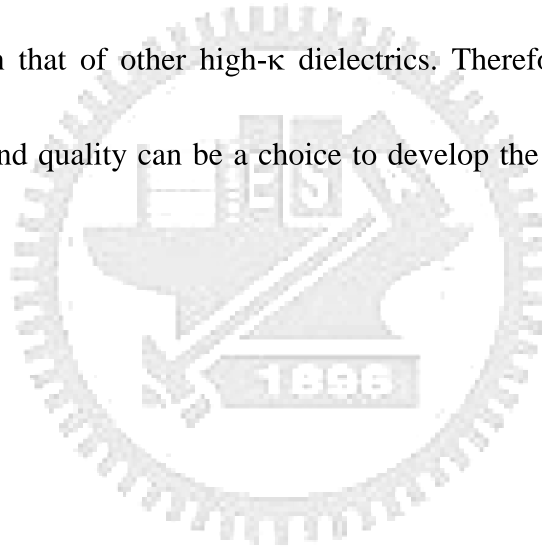
Owing to the high dielectric constant, good step coverage and minimum thickness limit, simple metal oxide such as Ta_2O_5, Al_2O_3, ZrO_2, HfO_2, La_2O_3 and $SrTiO_3$ are thought the promising materials in the application of DRAM. Among the simple metal oxide, HfO_2, ZrO_2 and La_2O_3 exhibit larger conduction band

discontinuity (ΔEc ~1.4-2.3 eV), dielectric constant (κ ~25-30) and bond enthalpy (Figure 1-6) to prevent from higher leakage current and degradation after high temperature process. Similar to high-k/Si CMOSFET, the larger conduction band offsets is the better choice for MIM capacitor.

Due to their moderate permittivity, it is difficult to achieve dielectric structures with an EOT well below 1.0 nm. One approach to increase permittivity is combining it with very high-κ material, such as TiO_2 with a permittivity value of 50-80 due to a contribution from soft phonons. Chiang *et al.* reported that permittivity of approximately 50 have been obtained from physical-vapor deposited TiHfO thin film. Therefore, TiO_2-based material which combined high-κ and large conduction band offset materials will be a good solution for logic devices (metal-gate/high-κ) beyond 32nm node or DRAM technology beyond 60nm node.

To fabricate monolithic microwave integrated circuits successfully, both active and passive components with reliable, repeatable and predictable performance are required. Among them, the capacitor used in filtering, decoupling and network matching plays a significant role in front end or mixed signal circuits. The requirement for capacitors includes high capacitance density, low voltage coefficients, good capacitor matching, precision control of values and low parasitic effects. The method to increase the capacitance density, in other words, to reduce the area

occupied by capacitors, is utilizing thin dielectrics with high dielectric constant. Recently, some kinds of dielectrics and approaches have been proposed to achieve the goal of high capacitance and the other good performance. Instead of SiO_2 with low dielectric constant, Si_3N_4 deposited by plasma enhanced chemical vapor deposition (PECVD) has been studied in the past years. Although Si_3N_4 shows good linearity and reliability, the capacitance density still needs to be increased. However, Si_3N_4 fabricated by PECVD has the minimum thickness limit and the defect density of nitride is higher than that of other high-κ dielectrics. Therefore, high-κ dielectrics with good linearity and quality can be a choice to develop the innovative and useful RF capacitors.



1.3 The Background of Metal Electrodes

MIM structure (metal-insulator-metal) can reduce contact resistance and raise storage charge comparing to MIS structure. MIM capacitors are integrated in the backend process. The maximum temperature of deposition is restricted by the thermal budget of back end processes.

As DRAM density increasing, devices shrinkage and higher charge storage is inevitable. It is difficult for conventional MIS structure to meet the requirements due to high-temperature-process limitation, so MIM structure is expected to apply in trench DRAM process. On the other hand, since high-k material interacts with bottom electrodes during dielectric activation, an interfacial layer will be formed between high-k material and metal electrode. The bottom interface will degrade the property of the dielectrics, such as interface roughness, interface stress, electron barrier height and thermal stability, etc.

Metal electrodes have been applied for CMOS devices as a gate material in 45nm process and for DRAM devices as electrodes in 90nm process. A full MIM structure with high-k dielectric may be required for the DRAM technology of 2009.

The use for electrodes of MIM capacitors, such as TiN, TaN, Ru, Ir, Ni and Pt, are deposited by using CVD, ALD or MOCVD methods. MIM capacitors used for logic-friendly embedded DRAM features require a low-temperature electrode

deposition process (typically less than about 450°C)

1.4 The Deposition method of High-κ Dielectrics

Some methods to deposit ultra thin high-κ dielectrics on substrates have been proposed in recent years and various methods exhibit the merits as well as some other issues that have to be solved.

Among the proposed high-κ dielectrics, HfO_2, La_2O_3 and ZrO_2 show the promising properties and are thought the candidate of the next generation. It has been reported that many process technologies can be used to deposit high quality HfO_2. Atomic layer chemical vapor deposition has attracted much attention due to its self-limit and mono-layer deposition properties. Atomic layer chemical vapor deposition (ALCVD) is the method using MCl_4 (M: Hf, Ti, Zr…) and H_2O as sources to deposit HfO_2 as well as high-κ dielectrics. The precursors are introduced into the heated chamber and substrates. The reaction only happens on the substrate surface instead of the deposited layer and one layer is deposited at a time. Thus, the thickness of dielectrics can be controlled precisely and is dependent on the process cycles linearly. Although the excellent uniformity and initiation of deposition can be achieved on SiO_2 and Si_3N_4, the deposition directly on H-terminated Si substrate can lead to rough surface. However, H-terminated Si substrate is inevitable after HF dipping. Therefore, the improvement of process precursor is the key point to overcome the issues of ALCVD.

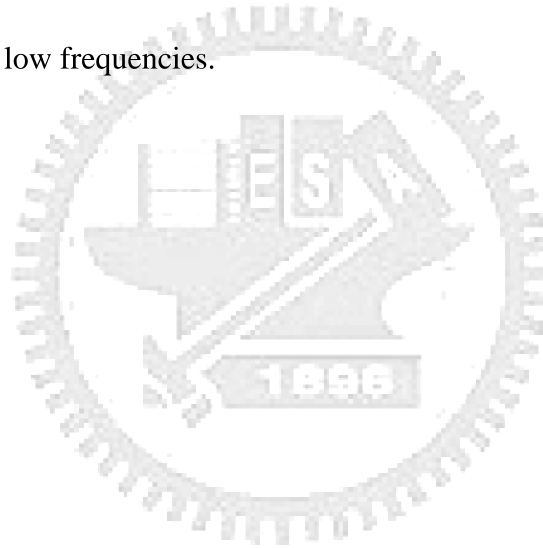
Metalorganic chemical vapor deposition (MOCVD) is the other method

extensively used in VLSI fabrication. The deposition of dielectrics has been carried out using metal organic precursor vapor. The precursors are introduced into low-pressure chamber and the substrate is heated to some suitable process temperature. The uniform and conformal deposition of dielectrics can be obtained. That is the reason why MOCVD process is integrated into fabrication process flow extensively. Although MOCVD suggests many merits, it still exists some issues such as the carbon contamination and the impact of precursors to the environment, health and safety.

Depositing the metal or metal oxide directly on the substrate using PVD method followed by thermal oxidation and annealing is the other method to deposit high quality dielectrics. In the past, many studies on the dielectrics by PVD have been reported and the related process flow was described as the following. The pre-clean Si substrate is loaded into high vacuum chamber immediately to prevent from the formation of native oxide. Then, the bottom electrode was deposited using reactive dc magnetron sputtering with a mixed gas of oxygen and argon. The deposited dielectrics was then followed a full oxygen ambient under 400°C furnace-annealing to finish the dielectric activation. Although the flow is already the standard DRAM process, the poor low-k interlayer and the property for easy-to-crystallize are still the issues that should be solved. By combining an advanced interface-plasma treatment with mixed

dielectrics with a stable thermal property, both of the issues mentioned above can be minimized.

In this study, we used the PVD method to fabricate the high-κ dielectrics. Instead of plasma treatment, we utilized NH_3 plasma treatment to prevent from the formation of interface oxide. The pre-cleaned wafer was loaded in E-beam evaporator under high vacuum condition and then oxidized at 400 ^{o}C in O_2 ambient followed by annealing. The devices using TiHfO, TiLaO, TiZrO and $SrTiO_3$ are fabricated and measured at high and low frequencies.



1.5 The Measurement and Analysis of the MIM Capacitors

To investigate the electrical characteristics of our devices, we measured the leakage current, stress induced leakage current using HP 4156A semiconductor parameter analyzer. Besides, HP4284A precision LCR meter was used to evaluate the capacitance and the conductance ranging from 100 kHz to 1 MHz. Furthermore, to investigate the characteristics of our devices at the frequency above 1 MHz, we measured the scattering parameter using HP8510C network analyzer and the test set. .

	Year in Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
	L_g: Physical gate length for LOP (nm) [1]	45	37	32	28	25	22	20	18	16
	EOT: Equivalent Oxide Thickness [2]									
IS	Extended planar bulk (Å)	14	13	12	11	10	9	9	9	
	UTB FD (Å)							9	9	8
	DG (Å)							9	9	8
	Gate Poly Depletion and Inversion-Layer Thickness [3]									
IS	Extended planar bulk (Å)	6.5	6.5	6.4	6.6	6.7	3.2	3.3	3.2	
	UTB FD (Å)							4	4	4
	DG (Å)							4	4	4
	EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]									
IS	Extended planar bulk (Å)	20.5	19.5	18.4	17.6	16.7	12.2	12.3	12.2	
	UTB FD (Å)							13	13	12
	DG (Å)							13	13	12
	$J_{g,limit}$: Maximum gate leakage current density [5]									
IS	Extended Planar Bulk (A/cm^2)	3.30E+01	4.10E+01	7.80E+01	1.54E+02	1.61E+02	1.10E+02	4.50E+02	6.90E+02	

Fig. 1-1 The International Technology Roadmap of SIA for Semiconductor 2007 [1-1]

	Calculated (eV)	Experiment (eV)	References
SiO_2		3.1	Alay [109]
Ta_2O_5	0.35	0.3	Miyazaki [79]
$SrTiO_3$	0.4	0	Chambers [78]
ZrO_2	1.6	1.4	Miyazaki [79]
		2.0	Afanasev [72]
		1.4	Rayner [85]
HfO_2	1.3	1.3	Sayan [84]
		2.0	Afansev [83]
Al_2O_3	2.4	2.8	Ludeke [81]
		2.2^a	Afansev [83]
a-$LaAlO_3$	1.0	1.8	Edge [87]
La_2O_3	2.3	2.3	Hattori [88]
Y_2O_3	2.3	1.6	Miyazaki [89]

Fig. 1-2 Comparison of the calculated conduction band offset and experimental values for various gate oxides, by various authors [1-13]

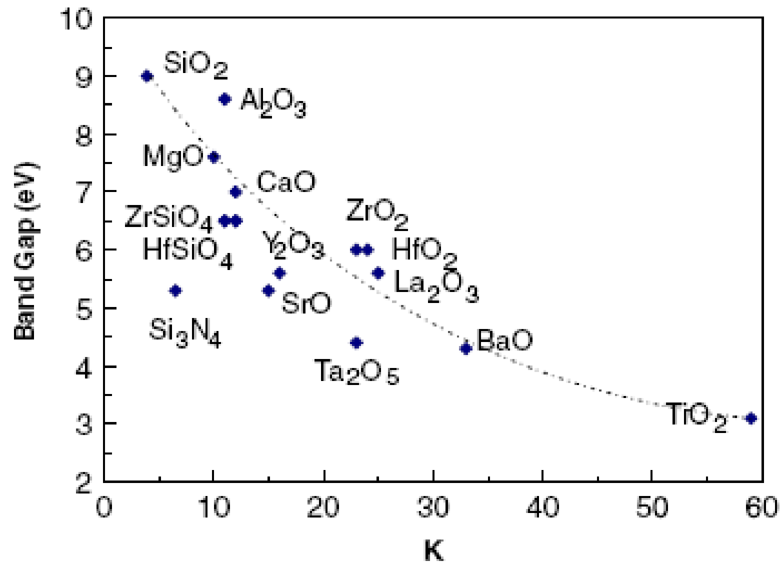


Fig. 1-3 Static dielectric constant versus band gap for candidate gate oxides, after Robertson [1-13]

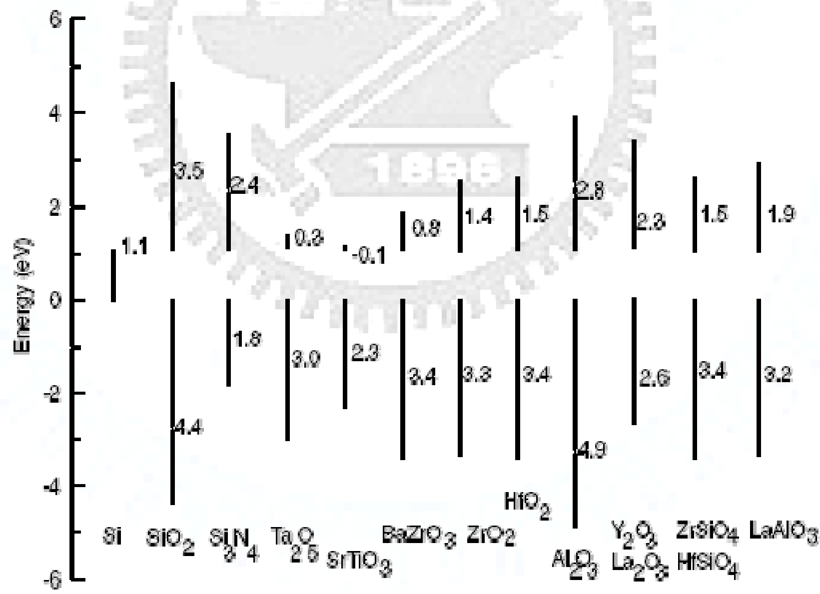


Fig. 1-4 Static dielectric constant versus band gap for candidate gate oxides, after Robertson [1-13]

Table FEP5b DRAM Stacked Capacitor Technology Requirements—Long-term Years

Year of Production	2016	2017	2018	2019	2020	2021	2022
DRAM ½ Pitch (nm) [A]	22	20	18	16	14	13	11
Cell size factor a [B]	6	6	6	6	6	6	6
Cell size (μm^2) [C]	0.003 =0.045x0.068	0.0024 =0.040x0.060	0.0019 =0.036x0.054	0.0015 =0.032x0.048	0.012 =0.028x0.043	0.010 =0.026x0.039	0.007 =0.022x0.033
Storage node size (μm^2) [D]	0.001 =0.023x0.045	0.0008 =0.020x0.040	0.00064 =0.018x0.036	0.00051 =0.016x0.032	0.0004 =0.014x0.028	0.0003 =0.013x0.026	0.0002 =0.011x0.022
Capacitor structure	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM
t_{eq} at 25fF (nm) [G]	0.3	0.3	0.3	0.25	0.2	0.15	0.1
Dielectric constant	91	78	78	70	80	91	98
SN height (μm)	1.6	1.8	2.0	1.9	1.7	1.4	1.1
Cylinder factor [E]	1	1	1	1	1	1	1
Roughness factor	1	1	1	1	1	1	1
Total capacitor area (μm^2)	0.22	0.22	0.22	0.18	0.14	0.11	0.07
Structural coefficient [F]	72.4	90.5	114.3	120.7	120.7	120.7	120.7
t_{phy} at 25fF (nm) [H]	7.0	6.0	6.0	4.5	4.1	3.5	2.5
A/R of SN [I]	74.5	90.2	111.4	117.5	122.8	106.8	99.4
A/R of SN (OUT) for cell plate deposition [I]	204.8	225.4	334.2	267.6	296.7	231.3	182.2
HAC diameter (μm) [J]	0.03	0.02	0.02	0.02	0.02	0.02	0.01
Total interlevel insulator and metal thickness except SN (μm) [K]	0.57	0.55	0.53	0.51	0.49	0.47	0.45
HAC depth (μm) [L]	2.2	2.4	2.5	2.4	2.2	1.9	1.5
HAC A/R	73.6	117.7	126.8	119.5	110.5	92.9	154.3
$V_{capacitor}$ (Volts)	0.7	0.6	0.6	0.6	0.6	0.5	0.5
Retention time (ms) [M]	64	64	64	64	64	64	64
Leak current (fA/cell) [N]	0.41	0.35	0.35	0.35	0.35	0.29	0.29
Leak current density (nA/cm^2)	188.8	161.9	161.9	194.2	242.8	269.8	404.7
Deposition temperature (degree C)	~500	~500	~500	~500	~500	~500	~500
Film anneal temperature (degree C)	<650	<650	<650	<650	<650	<650	<650
Word line R_s (Ohm/sq.)	2	2	2	2	2	2	2

(a)

Table FEP6b DRAM Trench Capacitor Technology Requirements—Long-term Years

Year of Production	2016	2017	2018	2019	2020	2021	2022
DRAM ½ pitch "F" (nm)	22	20	18	16	14	13	11
Cell size factor "a" [A]	8	8	8	8	8	8	8
Cell size (μm^2) [B]	0.0039	0.0032	0.0026	0.0020	0.0016	0.0014	0.0010
Trench structure	bottled	bottled	bottled	bottled	bottled	bottled	bottled
Trench bottle circumference (nm) [C]	183	166	150	133	116	108	92
Trench etch depth (μm) [D]	3.0	2.8	2.6	2.4	2.3	2.2	2.1
Bottled trench depth (μm) [E]	2.5	2.3	2.1	1.9	1.8	1.7	1.6
Storage node size (μm^2) [F]	0.5	0.4	0.3	0.3	0.2	0.2	0.1
Trench surface area enhancement factor (HSG) [G]	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Cell capacitance (fF) [H]	25.0	25.0	25.0	25.0	25.0	25.0	25.0
teq at Cs (nm) [I]	0.6	0.5	0.4	0.3	0.3	0.3	0.2
Trench top opening (nm) [J]	31	28	25	22	20	18	15
Trench etch aspect ratio [K]	97	100	103	107	117	121	136
Capacitor structure	Cup MIM	Cup MIM	Cup MIM	Cup MIM	Cup MIM	Cup MIM	Cup MIM

(b)

Fig. 1-5 The 2007 International Technology Roadmap for Semiconductors for DRAM (a) stacked capacitors and (b) trench capacitors.

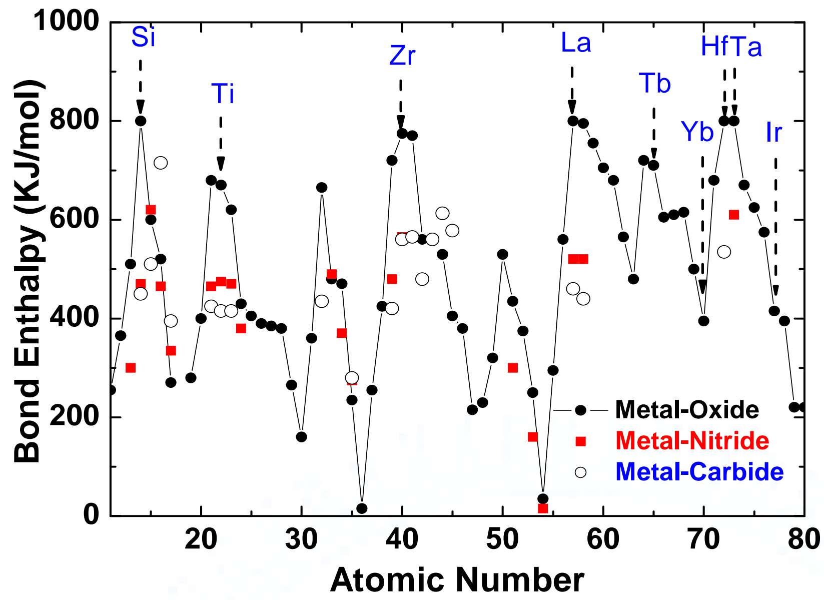


Fig. 1-6 Bond enthalpy for M-O, M-N and M-C in the Periodic Table

Chapter 2

Performance Improvement of TiHfO MIM Capacitors by Using a Dual Plasma Treatment of the Lower Electrode

2.1 Introduction

The technology roadmap for Metal-Insulator-Metal (MIM) capacitors [2-1]-[2-16], which are used for analog, RF and DRAM functions in Integrated Circuits, specifies a continuing increase of the capacitance density ($\varepsilon_0\kappa/t_\kappa$) and lower leakage currents. To achieve this goal, higher κ TiO-based dielectrics - such as TiTaO, TiLaO, TiHfO [2-11]-[2-13] and $SrTiO_3$ (STO) [2-14]-[2-16] – are need for the MIM devices. Unfortunately, there is an interfacial reaction, during device processing, at the lower high-κ dielectric/metal interface [2-14]. This reduces the capacitance density and increases the leakage current, and this reaction increases in importance as the capacitance equivalent thickness (CET) decreases to 1 nm. To inhibit the reaction a nitrogen plasma treatment can be applied to the TaN or TiN bottom electrodes [2-14]-[2-16]. Here we report an improved surface treatment for TaN electrodes. Following a conventional nitrogen plasma treatment, exposing the bottom TaN to an oxygen plasma increased the capacitance density, monotonically, from 22 to 28 fF/μm^2. This combined oxygen and

nitrogen plasma treatment also improved the leakage current by 2 orders of magnitude. Such an improvement occurs because the interfacial reaction is reduced during device processing. This was seen in cross-sectional transmission electron microscopy (TEM). We measured a leakage current of 4.8×10^{-6} A/cm^2 in our 28 fF/μm^2 density TaN/TiHfO/TaN MIM capacitors. This data compares well with other high-κ MIM capacitors [2-1]-[2-16], even when higher work-function Ir [2-11]-[2-15] or Ni [2-16] electrodes are used.

2.2 Experimental procedure

The high-κ TiHfO MIM capacitors were fabricated on standard Si wafers. For VLSI backend integration, a 2-μm-thick SiO_2 isolation layer was deposited on the Si substrates. Then a TaN/Ta (50-nm/200-nm) bi-layer was deposited and used as the bottom capacitor electrode. The nitrogen plasma was applied to the TaN surface [2-13]-[2--15]. This was followed by an O_2 plasma treatment to increase the oxidation resistance, before the high-κ dielectric deposition and post-deposition annealing (PDA). A ~12 nm thick $Ti_xHf_{1-x}O$ (x~0.67) film was deposited by PVD, followed by a 400°C PDA in an oxygen ambient, to reduce the defects and the leakage current [2-3]. Finally, 50 nm layer of TaN was deposited and patterned to form the top electrode. The TiHfO thickness and the interfacial layer between TiHfO and bottom TaN were measured by cross-sectional TEM.

A large capacitor size of 150-μm×150-μm was used to ensure that any dimensional variations were unimportant. The fabricated MIM devices were characterized by *C*-*V* and *J*-*V* measurements.

2.3 Results and discussion

In Figures 2-1 (a) and (b) we show the *C*-*V* and *J*-*V* characteristics of TiHfO capacitors with and without the second oxygen plasma treatment. The capacitance density increased from 22 to 28 fF/μm^2, as the lower TaN electrode was exposed to the oxygen plasma for longer times. Correspondingly, the leakage current at -1 V decreased from 2.5×10^{-4} to 4.8×10^{-6} A/cm^2 with increasing oxygen exposure. Therefore, the increasing exposure time to oxygen plasma improves both capacitance density and leakage current. The comparison of our data with those for other MIM capacitors appears in Table 1. The performance of our TaN/TiHfO/TaN capacitors is comparable with the best reported MIM devices, such as Ir/TiTaO/TaN (23 fF/μm^2 density) [2-11]-[2-12] or Ni/STO/TaN (25 fF/μm^2 density) capacitors [2-16], which used higher work-function Ir (5.3 eV) and Ni (5.1 eV) top electrodes than this TaN (~4.6 eV) case. The high work-function electrode is especially important for leakage current at low voltage due to the Schottky emission mechanism [2-17]-[2-18]. Our result indicates the importance of an additional oxygen plasma treatment on the lower electrode.

We have also measured the variation of the capacitance ($\Delta C/C$) as a function of voltage. In Fig. 2-2 we show such $\Delta C/C$-V data. The voltage dependence of $\Delta C/C$ is expressed as $\beta V+\alpha V^2$ [2-8]-[2-12], where β and α are the linear and quadratic coefficients of $\Delta C/C$-V, respectively. Here α is the important factor for capacitors, since the effects of β can be compensated in the circuit design [2-8]. Increasing the exposure time of the bottom TaN to an oxygen plasma decreased α from 17858 to 3851 ppm/V^2. Since the α improves rapidly with decreasing capacitance density [2-14], further α reduction is possible at lower capacitance density used for analog/RF application.

To understand these performance improvements, we examined the devices using cross-sectional TEM. In Figs. 2-3 (a) and (b) we compare the TEM images for the TiHfO structure without and with the oxygen plasma treatment. A clear interfacial region, ~3 nm wide, can be seen in the conventional nitrogen-only plasma-treated TaN, giving a total thickness of ~15 nm. In contrast, the combined oxygen and nitrogen plasma-treated TaN shows reduced interfacial reactions. A thickness of ~12 nm was measured for the TiHfO dielectric – indicating a κ value of 38, at a capacitance density of 28 fF/μm^2.

In the Fig. 2-4 (a) and (b) the surface roughness of the lower TaN with O_2 plasma is smaller than that without O_2 plasma treatment. This result can explain the small leakage current obtained in the samples with additional O_2 plasma treatment. And the SIMS

analysis in Fig. 2-5 shows that a significant improvement with less Hf diffusion is obtained by using O_2 and N_2 plasma treatment.

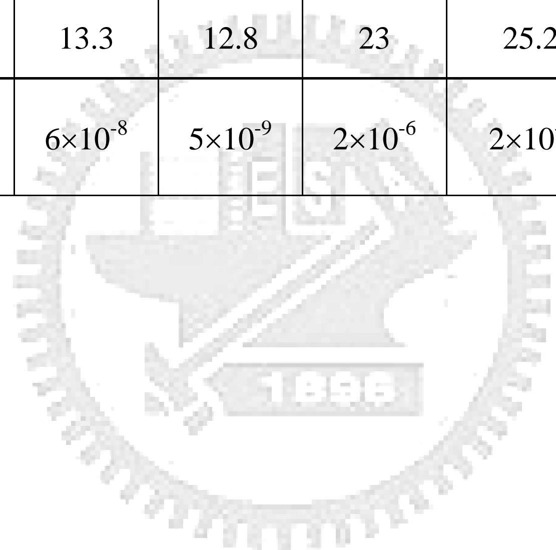
The possible reason for the large improvement, given by the oxygen plasma treatment, may be the larger bond enthalpy of TaO (799 kJ/mol) compared with that of TaN (611 kJ/mol) [2-19]. When applying only a nitrogen plasma treatment, the lower TaN will be oxidized to TaON during unavoidable PDA, due to the thermodynamically favorable larger bond enthalpy – this would lower the capacitance density. The significantly smaller interfacial layer with oxygen plasma treatment may be de to the formation of high quality TaON by highly reactive oxygen plasma, which decreases further oxygen diffusion into underneath TaN to form poor quality thermal TaON at low temperature during PDA.

2.4 Conclusion

We have shown that a nitrogen plasma treatment cannot, alone, suppress the interfacial layer formation that causes degraded capacitance density and leakage current in TaN/TiHfO/TaN MIM capacitors. By using an additional oxygen plasma treatment the interfacial reactions and growth were reduced, leading to a higher capacitance density and lower leakage current.

Table 2-1 Comparison of MIM capacitors having various dielectrics and metal electrodes.

	HfO_2 [2-7]	Tb-HfO_2 [2-9]	Al_2O_3-HfO_2 [2-8]	TiTaO [2-11]-[2-12]	STO [2-16]	**TiHfO This work**
Process Temp. (^oC)	400	400	400	400	400	400
Top Electrode	Ta	Ta	TaN	Ir	Ni	TaN
Work-function (eV)	4.2	4.2	4.6	5.27	5.1	4.6
Cap. Density ($fF/\mu m^2$)	13	13.3	12.8	23	25.2	28
Current Density (A/cm^2) @ 1V	6×10^{-7}	6×10^{-8}	5×10^{-9}	2×10^{-6}	2×10^{-7}	4.8×10^{-6}



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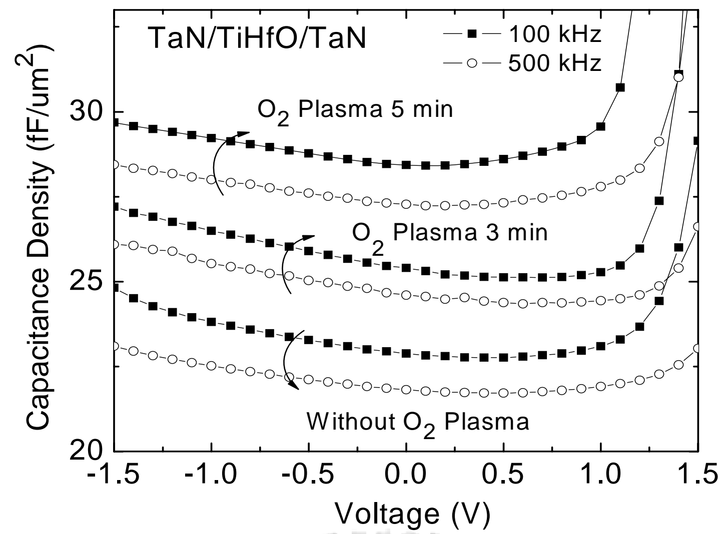
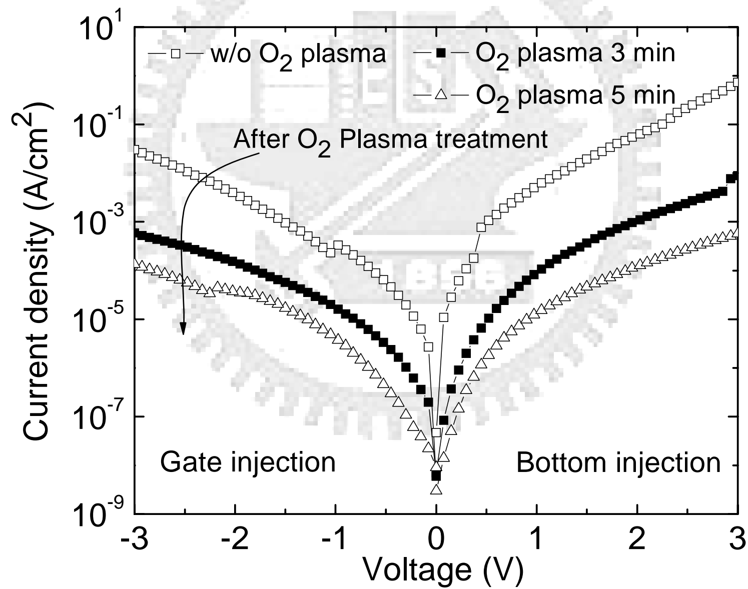


(a)



(b)

Fig. 2-1 (a) *C-V* and (b) *J-V* characteristics for TaN/TiHfO/TaN MIM capacitors measured after the indicated plasma treatments.

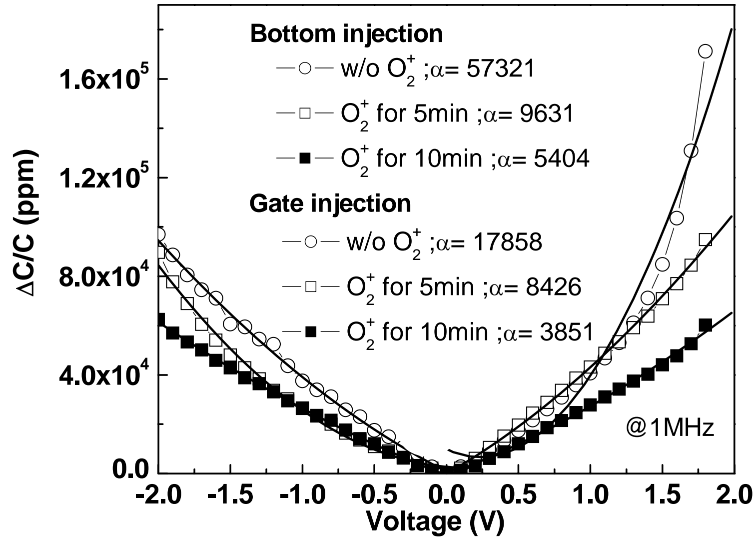
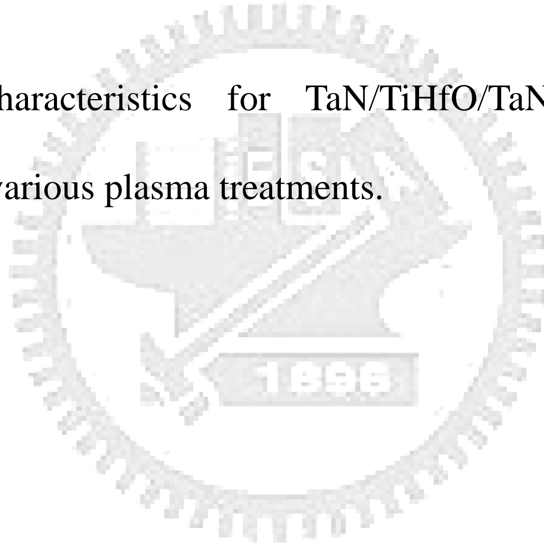
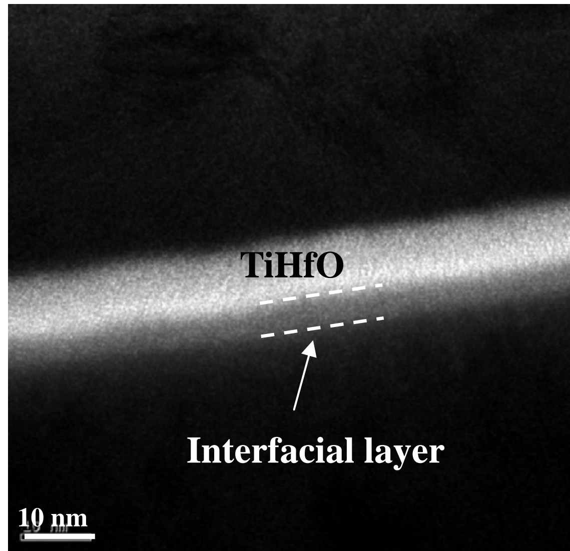
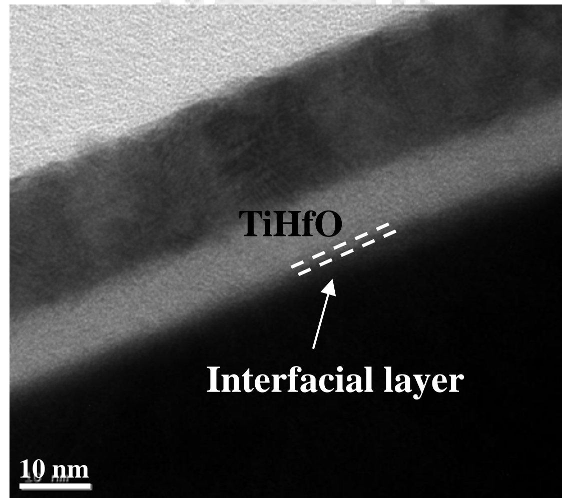


Fig. 2-2 *ΔC/C-V* characteristics for TaN/TiHfO/TaN MIM capacitors following various plasma treatments.



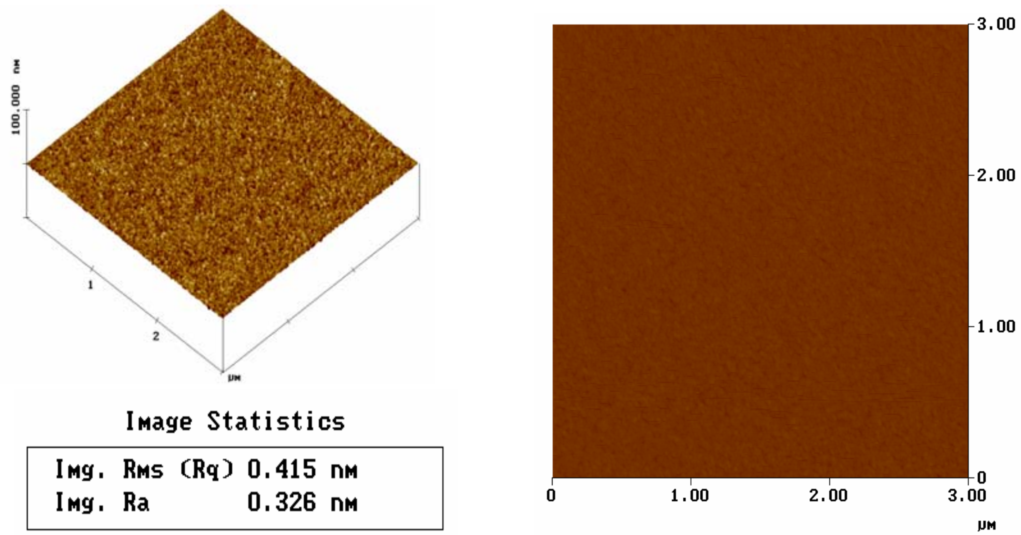


(a)

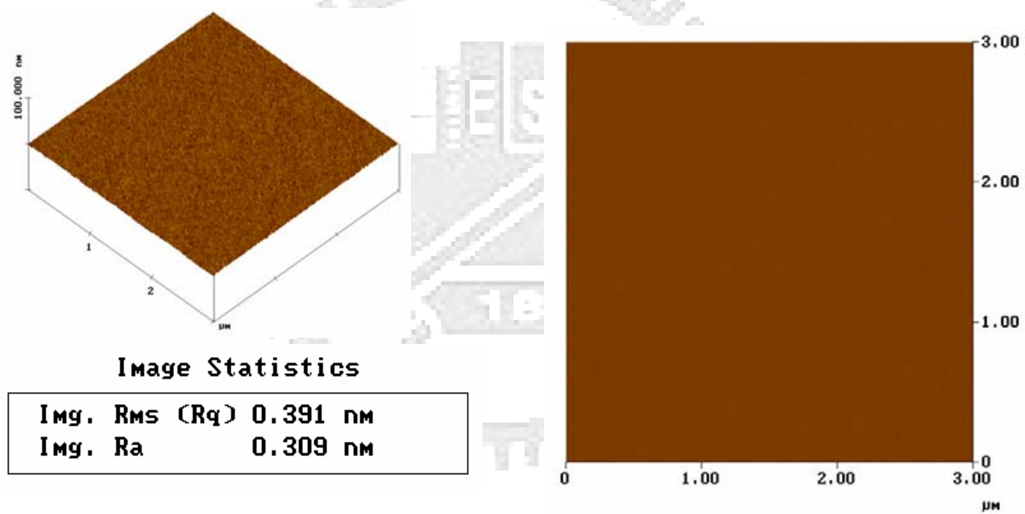


(b)

Fig. 2-3 Cross-sectional TEM images of the TiHfO structure (a) with only a nitrogen plasma treatment and (b) with both a nitrogen and a second oxygen plasma treatment.



(a)



(b)

Fig. 2-4 The surface roughness of bottom electrode (a) with or (b) without O_2 plasma treatment by AFM spectroscopy.

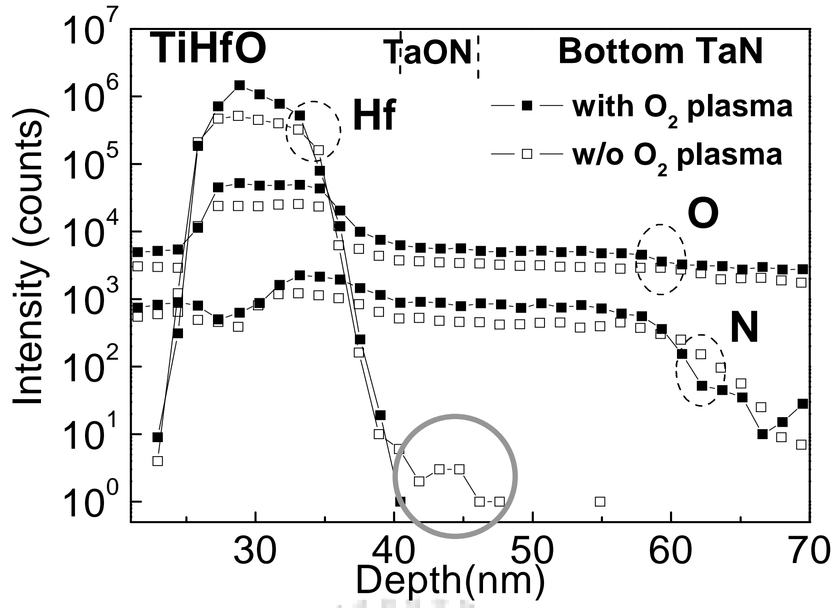
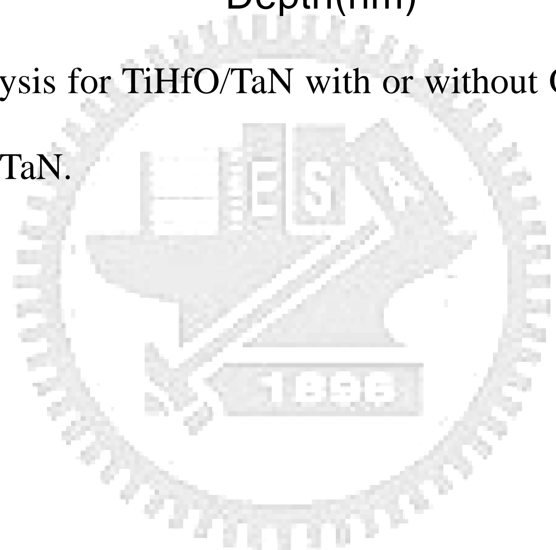


Fig. 2-5 SIMS analysis for TiHfO/TaN with or without O_2 plasma treatment on bottom TaN.



Chapter 3

Low Temperature Crystallized TiO_2 Dielectrics for DRAM Application

3.1 Introduction

There is a strong desire to decrease the processing temperature of Metal-Insulator-Metal (MIM) capacitors [3-1]-[3-16], while maintaining a high capacitance density ($\varepsilon_0\kappa/t_\kappa$) and low leakage current. This requirement is due to the low-temperature processing associated with low-κ isolation dielectrics, such as PAR. For VLSI backend integration, temperatures down to 300°C may be desirable [3-17]. Low-temperature-processed MIM capacitors would be useful in the integration of future-generation Ge-on-Insulator (GOI) [3-18]-[3-19] and IIIV-on-Insulator (IIIVOI) [3-20] technologies, where the device performance can be crucially dependent on the thermal processing budget. Unfortunately, most high-κ dielectrics, as used for high-density MIM capacitors, require a high process temperature to improve their quality and increase the κ value by crystallization.

Here we describe the performance of MIM capacitors processed at only 300°C. A capacitance density of 28 fF/μm^2 was obtained with a leakage current of just 3×10^{-8} A/cm^2. Such capacitor performance compares well with that for devices incorporating

450°C-processed $SrTiO_3$ (STO) [3-14]-[-15], and is better than that for 400°C-processed TiLaO [3-11]-[3-12], TiTaO [3-13] and STO [3-16] capacitors. This was achieved by using a high-κ TiO_2 dielectric which had a high κ value of 65, due to nano-crystal formation. This occurs at processing temperatures as low as 300°C. These MIM capacitors have potential in analog, RF and DRAM applications and are vital for GOI [3-18]-[3-19] and IIIVOI [3-20] technologies.

3.2 Experimental procedure

The high-κ TiO_2 MIM capacitors were fabricated on standard Si wafers having a 2-μm-thick SiO_2 isolation layer on the Si substrates. Then TaN, 50 nm thick, was deposited on a 200 nm Ta layer and used as the lower capacitor electrode. The TaN surface was given an NH_3 plasma treatment first [3-13]-[3-16] and then exposed to an O_2 plasma – this being done to increase the oxidation resistance before the high-κ dielectric deposition and post-deposition anneal (PDA). Then 20 nm thick TiO_2 dielectric was deposited at room temperature by electron-beam evaporation at a pressure of 2×10^{-6} torr, followed by a 300°C PDA for 10 min in an oxygen ambient of 1 atm pressure. Finally, a 20 nm Ir layer was deposited and patterned to form the top electrode. The capacitors were 180-μm×180-μm in size, thus minimizing any complications from variations in dimensions arising from the lithography. The fabricated devices were characterized by

standard *C-V* and *J-V* measurements.

3.3 Results and discussion

In Figures 3-1 (a) and (b), we show the *C-V* and *J-V* characteristics of Ir/TiO_2/TaN capacitors, respectively. A high capacitance density of 28 fF/μm^2 was measured, along with a low leakage current of 3×10^{-8} A/cm^2 at -1 V. These results are compared with other MIM data in Table 1. Our results are an improvement over those for a Ni/STO/TaN device, which had a slightly lower density of 25 fF/μm^2 and were processed at 400°C [3-16]. Since the work-function of the Ni electrode is only slightly lower than Ir, the better leakage in the Ir/TiO_2/TaN device, when compared with Ni/STO/TaN, is due to the larger conduction band offset (ΔE_C) of the TiO_2 with respect to the STO [3-21]-[3-22]. This is because the larger ΔE_C and higher work function electrode will form a higher Schottky barrier height to lower the leakage current by Schottky emission mechanism [3-15]-[3-16]. A larger ΔE_C to the metal electrode is also important for the high-temperature leakage current at 125°C. We found a 125°C leakage current of 6×10^{-7} A/cm^2, measured at -1 V. This is, to the best of our knowledge, better than previous data, and is at a high capacitance density of 28 fF/μm^2 [3-1]-[3-16]. Besides, a dual plasma treatment on the lower electrode to prevent the growth of interfacial layer is another vital improvement for the small leakage current. The Fig. 3-2 showed the XPS depth profile

for TiO_2/TaN with or without O_2 plasma treatment on the bottom TaN. The bottom TaN with O_2 plasma treatment reduced effectively the interface reaction due to the formation of high qualify TaON barrier layer.

A small loss tangent of 0.013 is obtained at such large 28 fF/μm^2 density using advanced four-element model and two-frequency calculation [3-23], which can be decreased with decreasing capacitance density [3-24]. A quadratic voltage coefficient of capacitance (α) of 5010 ppm/V^2 was obtained at 500 kHz, which can also be improved rapidly with a decreased capacitance density [3-14] used for analog/RF application. A temperature coefficient of capacitance (TCC) of 353 ppm/^{o}C was measured even at a high 28 fF/μm^2 density.

To understand the performance improvements we examined the 300°C-processed TiO_2 structure by cross-sectional TEM. As shown in Fig. 3-3, the nano-crystallization of TiO_2 is observable even at 300°C. This nano-crystallization effect yields a high κ value of ~65 for the TiO_2 dielectric – and explains why the leakage current is better than that for previous TiTaO [3-11]-[3-12] and TiLaO [3-13] MIM capacitors, shown in Table 1, which have a κ value of 45. The high κ value, in combination with the ΔE_C and high work-function Ir electrode, helps explain the good 125°C leakage current. This is because the larger ΔE_C lowers the Schottky emission current, and the high κ value decreases the

conducting electric field for both Schottky emission and Frenkel-Pool mechanism [3-15].

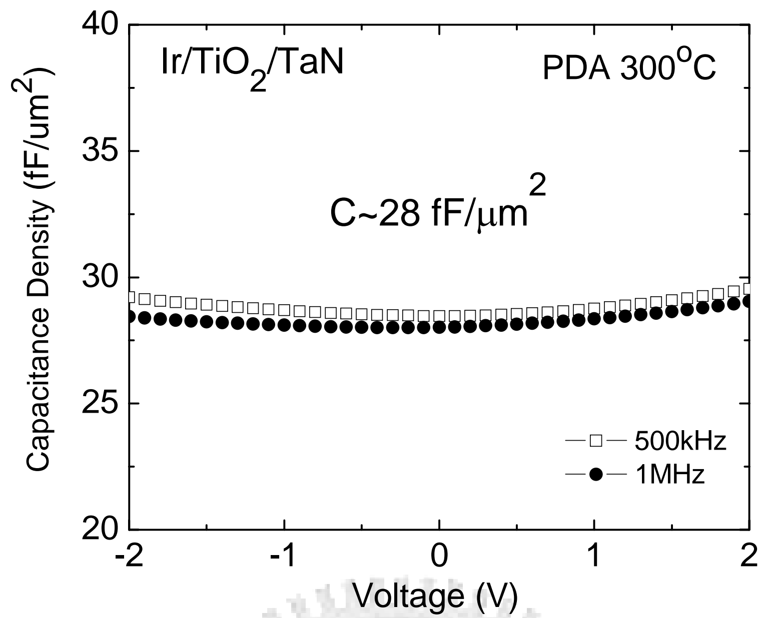
To study the thermal stability we annealed an $Ir/TiO_2/TaN$ capacitor at 350^oC for 20 min under an N_2 ambient. In Figures 3-4 (a) and (b) we display the *C-V* and *J-V* characteristics before and after this thermal treatment. Only a small degradation of the capacitance density and leakage current occurred, indicating the good thermal stability of both the top Ir electrode and the TiO_2 capped metal electrodes. We also note that good thermal stability has been reported for Ir/HfAlON pMOS even at RTA temperatures of up to 900^oC [3-25].

3.4 Conclusion

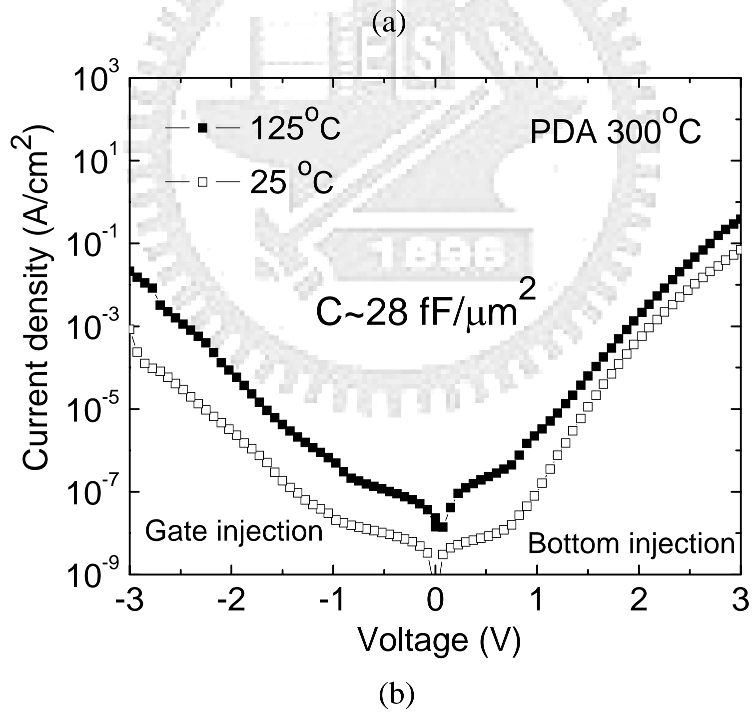
We have demonstrated $Ir/TiO_2/TaN$ MIM capacitors with a capacitance density of 28 $fF/\mu m^2$, along with a leakage current of 3×10^{-8} A/cm^2 at -1 V. Since the device processing was performed at 300^oC this would permit these capacitors to be integrated into a VLSI backend, along with advanced low-κ isolation dielectrics, or with future front-end GOI and IIIVOI technologies.

Table 3-1. Comparison of MIM capacitors which have various dielectrics and metal electrodes.

	HfO_2 [3-7]	Tb-HfO_2 [3-9]	Al_2O_3-HfO_2 [3-8]	TiTaO [3-11]-[3-12]	TiLaO [3-13]	STO [3-16]	STO [3-15]	**TiO_2 This work**
Process Temp. (^oC)	400	400	400	400	400	400	450	300
Top Electrode	Ta	Ta	TaN	Ir	Ir	Ni	TaN	Ir
Work-function (eV)	4.2	4.2	4.6	5.27	5.27	5.1	4.6	5.27
Cap. Density (fF/μm^2)	13	13.3	12.8	23	24	25.2	28	28
Current Density (A/cm^2) @25^oC	6×10^{-7} (1V)	1×10^{-7} (2V)	8×10^{-9} (2V)	2×10^{-6} (1V) 2×10^{-5} (2V)	1×10^{-7} (1V) 2.3×10^{-7} (2V)	2×10^{-7} (1V) 8×10^{-6} (2V)	3×10^{-8} (2V)	3×10^{-8} (1V)
Current Density (A/cm^2) @125^oC	2×10^{-6} (1V)	2×10^{-7} (2V)	6×10^{-9} (1V) 5×10^{-8} (2V)	—	6.6×10^{-7} (1V) 6.7×10^{-6} (2V)	5×10^{-6} (1V)	—	6×10^{-7} (1V)



(a)



(b)

Fig. 3-1 (a) *C*-*V* and (b) *J*-*V* (measured at 25 °C and 125°C) characteristics for $Ir/TiO_2/TaN$ capacitors.

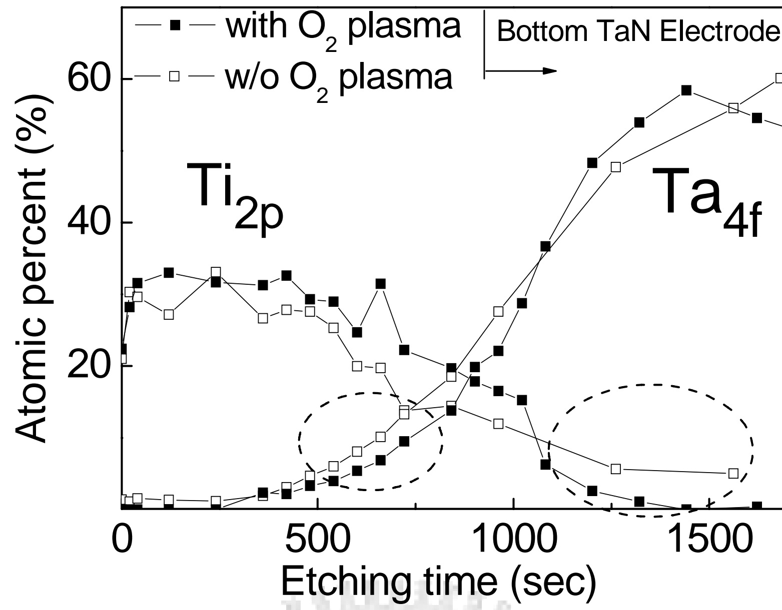


Fig. 3-2 XPS depth profile for TiO_2/TaN with or without O_2 treatment on bottom TaN.

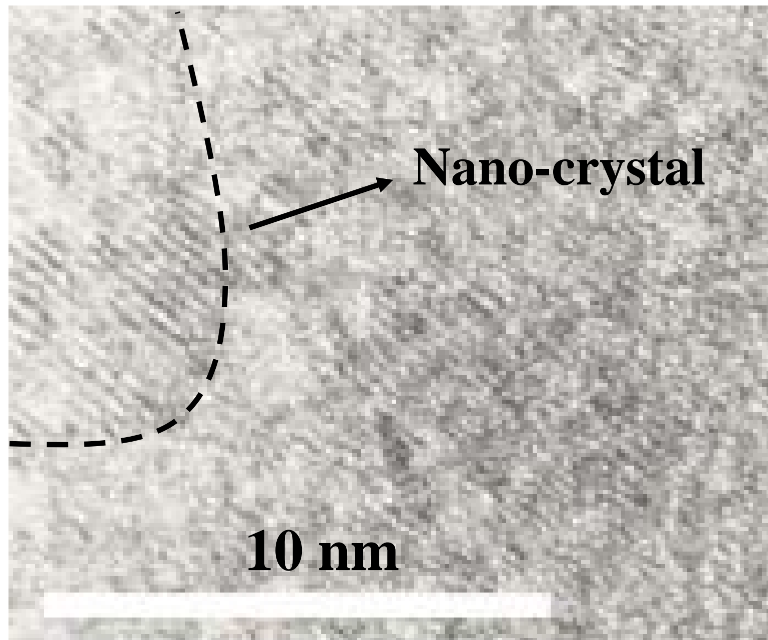
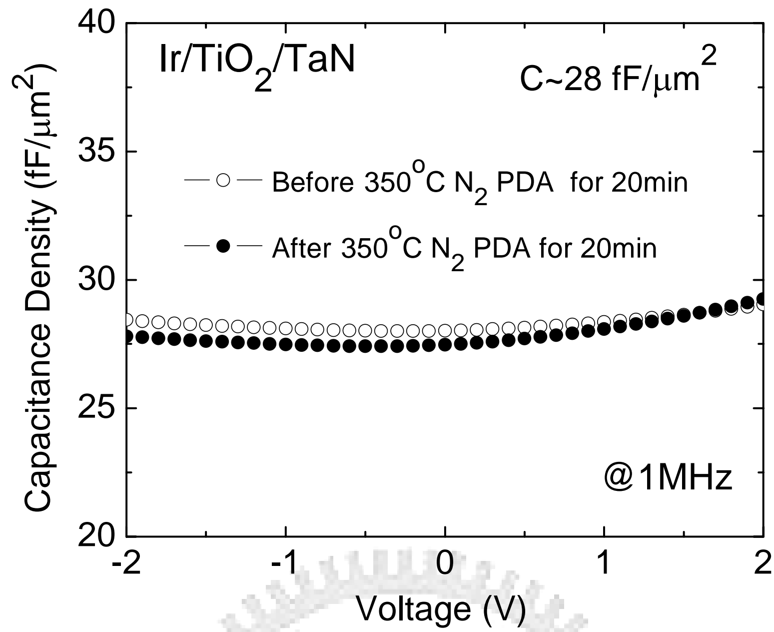
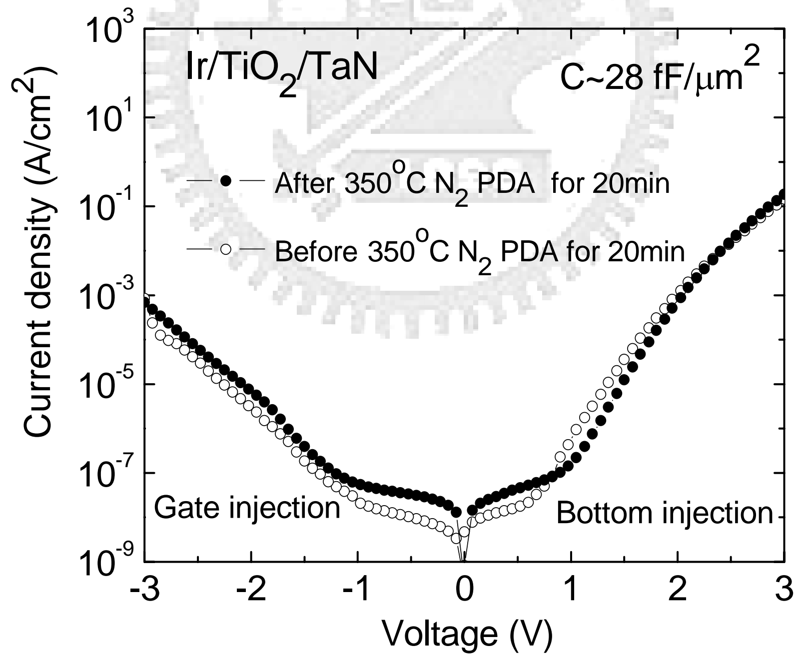


Fig. 3-3 A cross-sectional TEM image of a TiO_2 sample, after 300°C processing.



(a)



(b)

Fig. 3-4 The thermal stability behavior of a 300°C -formed $Ir/TiO_2/TaN$ capacitor after a 350°C N_2 anneal for 20 min.

Chapter 4

Improved High-Temperature Leakage in High Density MIM Capacitors by Using a TiLaO Dielectric and an Ir Electrode

4.1 Introduction

There is a continuing demand to increase the capacitance density ($\varepsilon_0\kappa/t_\kappa$) of the Metal-Insulator-Metal (MIM) capacitors [4-1]-[4-16]. To achieve this, the MIM devices have evolved by using higher κ dielectrics such as SiN [4-3]-[4-4], Al_2O_3 [4-6]-[4-7], Ta_2O_5 [4-5], HfO_2 [4-8]-[4-10], Nb_2O_5 [4-11], TiTaO [4-12]-[4-13] and $SrTiO_3$ (STO) [4-14]-[4-16]. Unfortunately, increasing the κ value usually decreases the conduction band offset (ΔE_C) with respect to the metal electrode. For STO [4-17] ΔE_C can even be slightly negative. This low ΔE_C leads to unwanted poor leakage current of MIM device at elevated temperature [4-16], whereas such high temperature operation is unavoidable due to the increased circuit density with higher power dissipation. Besides, although STO showed higher κ values by forming nano-crystals, this only occurs at a high process temperature >450°C. This exceeds the max temperature (400°C) permitted for backend integration [4-14]-[4-16]. Here we report low thermal leakage TiLaO MIM capacitors

using a high work-function Ir electrode and processed at 400°C. We measured leakage currents of 1×10^{-7} and 6.6×10^{-7} A/cm^2 at respective 1 V at 25 and 125°C that are lower than previous TiTaO and 400°C-processed STO capacitors.

4.2 Experimental procedure

The high-κ TiLaO MIM capacitors were fabricated on standard Si wafers. To permit VLSI backend integration, the process began with depositing a 2-μm-thick SiO_2 isolation layer on the Si substrates. Then 50 nm TaN on a 200 nm Ta layer was deposited by sputtering and used as the lower capacitor electrode. The TaN surface was then given a plasma treatment to increase the oxidation resistance before the high-κ deposition and post-deposition annealing (PDA) [4-5]-[4-6]. A 15 nm thick $Ti_xLa_{1-x}O$ (x~0.67) film was deposited by PVD, followed by a 400°C PDA in an oxygen ambient to reduce the defects and the leakage current [4-3]. (The TiLaO thickness was later measured by cross-sectional TEM.) Finally, 20 nm Ir and/or 50 nm TaN were deposited and patterned to form the top electrode. A large capacitor size of 100-μm×100-μm was chosen to avoid the size difference by lithography. The devices were characterized by *C-V* and *J-V* measurements.

4.3 Results and discussion

Figure 4-1 shows the *C-V*, *J-V* and thermal stability characteristics of TaN/TiLaO/TaN and TaN/Ir/TiLaO/TaN devices and the comparison with other data is

summarized in Table 1. A high capacitance density of 24-24.5 fF/μm^2 was measured for the TiLaO MIM devices, which gives a high-κ value of ~45 for the TiLaO dielectric. A leakage current of 2.2×10^{-6} A/cm^2 at -1 V was measured for the TaN/TiLaO/TaN MIM capacitor, close to that of an Ir/TiTaO/TaN device (Table 1) with a slightly lower capacitance density. Since the work-function of the TaN on TiLaO is ~0.7 V lower than that of Ir on TiTaO, the comparable leakage current indicates that the TiLaO is the better choice for MIM capacitor than TiTaO. This is confirmed by the 5 times lower leakage current of 1×10^{-7} A/cm^2 in the TaN/Ir/TiLaO/TaN device compared with the Ir/TiTaO/TaN capacitor. This improved leakage current, at a comparable capacitance density, is due to the higher ΔE_C between metal and high-κ interface, which lowers the leakage current exponentially. Similar lower leakage current was also reported by adding higher ΔE_C Al_2O_3 into HfO_2 MIM capacitor [4-9]. The very small changes of *J-V* and *C-V* after 400°C N_2 annealing indicates the good thermal stability, while good thermal stability of Ir on HfAlON up to 900°C was reported for metal-gate/high-κ pMOS [4-17].

A larger ΔE_C at the metal/high-κ interface is very important at 125°C, a temperature required for both DRAM and non-volatile memory. This is shown in the comparison with STO: the leakage current (-1 V) of a 400°C-formed Ni/STO/TaN capacitor increased from 2×10^{-7} to 5×10^{-6} A/cm^2, from 25 to 125°C (Table 1), while the TaN/Ir/TiLaO/TaN

capacitor it only increased from 1×10^{-7} to 6.6×10^{-7} A/cm^2. Although the work-function of the Ir electrode (5.27 eV) is slightly higher than Ni (5.1 eV), the improved 125°C leakage current, can be attributed to the large ΔE_C. We note that La_2O_3 has the highest ΔE_C with respect to Si (2.3 eV) compared with HfO_2 (1.5 eV), ZrO_2 (1.4 eV), Ta_2O_5 (0.3 eV), and STO (-0.1 eV) [4-18].

To investigate the current conduction mechanism we plot, in Fig. 4-2, *ln(J)* versus $E^{1/2}$ for the TaN/Ir/TiLaO/TaN MIM capacitors:

$$J \propto \exp\left(\frac{\gamma E^{1/2} - V_b}{kT}\right) \tag{1}$$

$$\gamma = \left(\frac{e^3}{\eta \pi \varepsilon_0 K_\infty}\right)^{1/2} . \tag{2}$$

Here K_∞ is the high-frequency dielectric constant ($= n^2$). The refractive index n is 2.57 or 1.9 for TiO_2 or La_2O_3 [4-19]), and η is 1 or 4 for Schottky emission (*SE*) or Frenkel-Poole (*FP*) conduction, respectively. The data fitting suggests that the current conduction mechanism of the TaN/Ir/TiLaO/TaN device changes from *SE* at low electric fields to *FP* at higher fields. In contrast, the TaN/TiLaO/TaN devices fit an *SE* description at both low and high fields.

The *SE* barrier height (V_b) at 125°C was determined from J/T^2-$E^{1/2}$ plots (Fig. 4-3). Values for V_b were 0.57 and 1.35 eV for TiLaO devices at 125°C with TaN and Ir top

electrodes, respectively. The large V_b difference explains the reduced leakage current and weaker temperature dependence in the TaN/Ir/TiLaO/TaN devices. Thus low leakage current at high temperature can be obtained in MIM capacitors by combining a high-κ dielectric having a high ΔE_C with a high work function metal electrode.

4.4. Conclusion

A high capacitance density and low leakage current at 125°C have been achieved in Ir/TiLaO/TaN MIM capacitors. The device processing temperature of 400°C would enable them to be integrated into VLSI backend technology and be used in multiple functions associated with SoC.

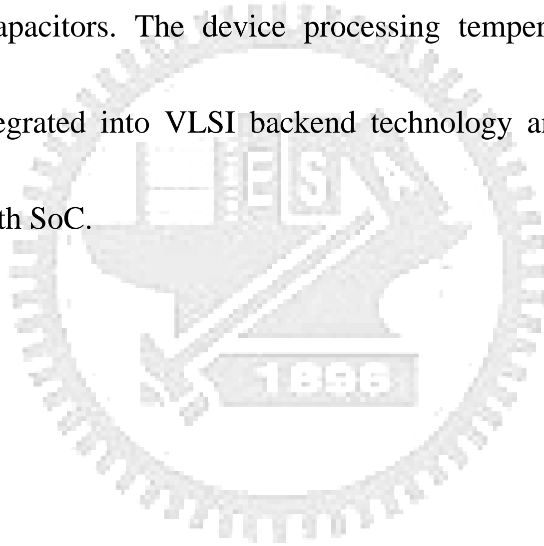
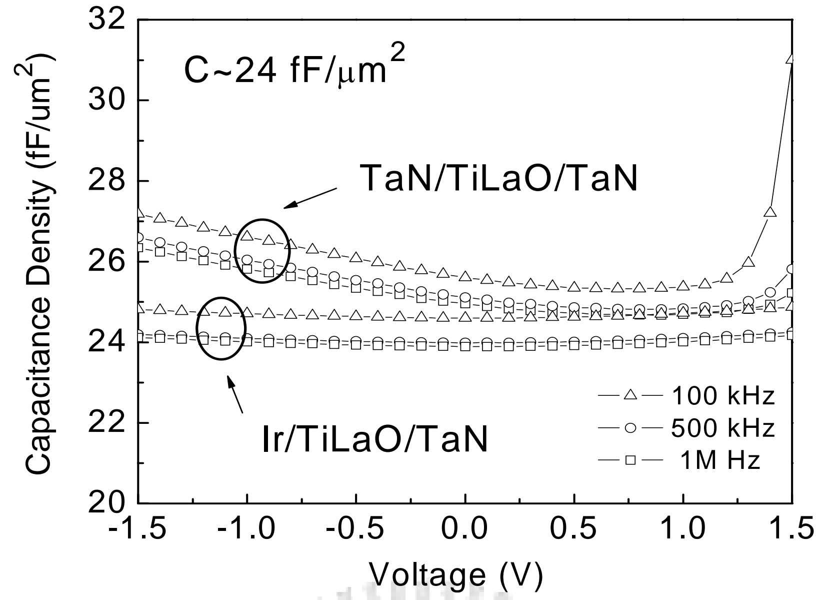
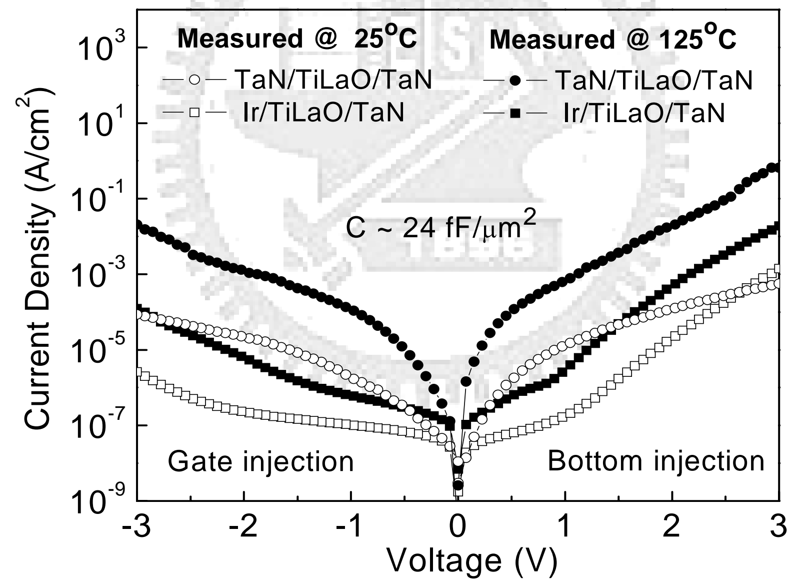


Table 4-1. Comparison of MIM capacitors with various dielectrics and metal electrodes.

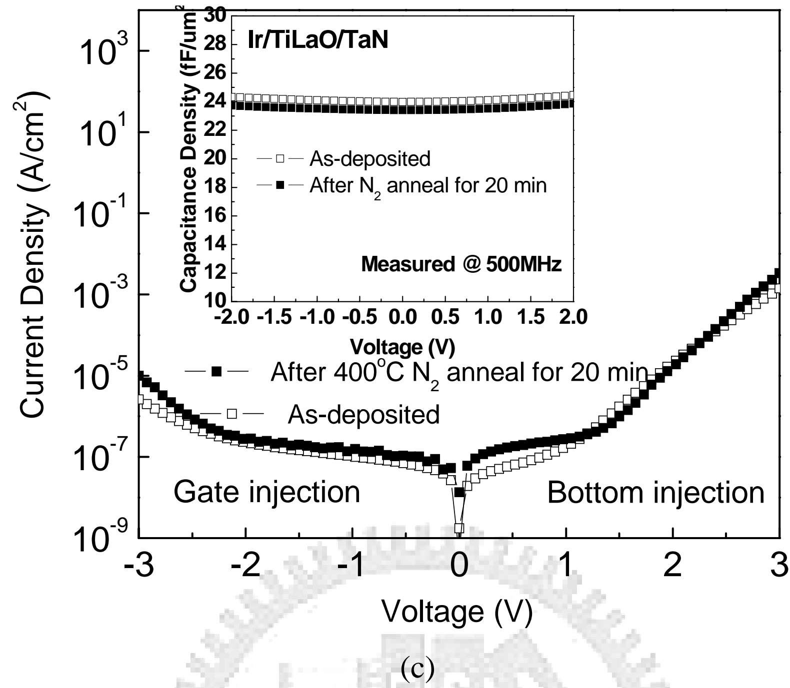
	HfO_2 [4-8]	Tb-HfO_2 [4-10]	Al_2O_3-HfO_2 [4-9]	TiTaO [4-12]-[4-13]	STO [4-16]	STO [4-14]	**TiLaO**	
Process Temp. (^oC)	400	400	400	400	400	450	**400**	
Top Electrode	Ta	Ta	TaN	Ir	Ni	TaN	TaN	Ir
Work-function (eV)	4.2	4.2	4.6	5.27	5.1	4.6	4.6	5.27
C Density (fF/μm^2)	13	13.3	12.8	23	25.2	28	24.5	24
J (A/cm^2) @25^oC	6×10^{-7} (2V)	1×10^{-7} (2V)	8×10^{-9} (2V)	2×10^{-6} (1V) 2×10^{-5} (2V)	2×10^{-7} (1V) 8×10^{-6} (2V)	3×10^{-8} (2V)	2.2×10^{-6} (1V)	1×10^{-7} (1V) 2.3×10^{-7} (2V)
J (A/cm^2) @125^oC	2×10^{-6} (1V)	2×10^{-7} (2V)	6×10^{-9} (1V) 5×10^{-8} (2V)	—	5×10^{-6} (1V)	—	1.3×10^{-4}	6.6×10^{-7} (1V) 6.7×10^{-6} (2V)



(a)



(b)



(c)

Fig. 4-1 (a) *C-V*, (b) *J-V* and (c) thermal stability characteristics of TaN/TiLaO/TaN and TaN/Ir/TiLaO/TaN MIM capacitors measured at various frequencies, at 25 and 125°C. The thermal stability test was performance at 400°C for 20 min at N_2 ambient.

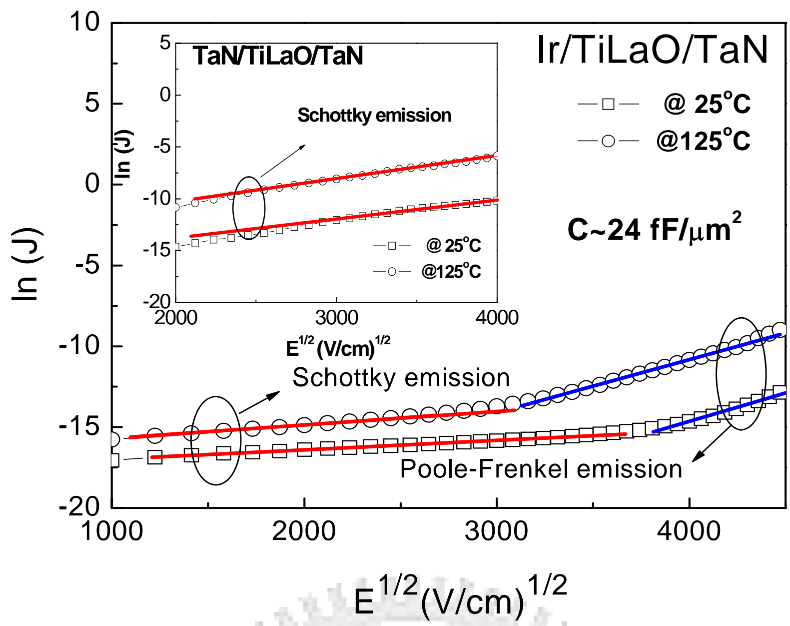


Fig. 4-2 Measured and simulated J-$E^{1/2}$ of an Ir/TiLaO/TaN capacitor. A TaN/TiLaO/TaN device is shown, for comparison, in the insert.

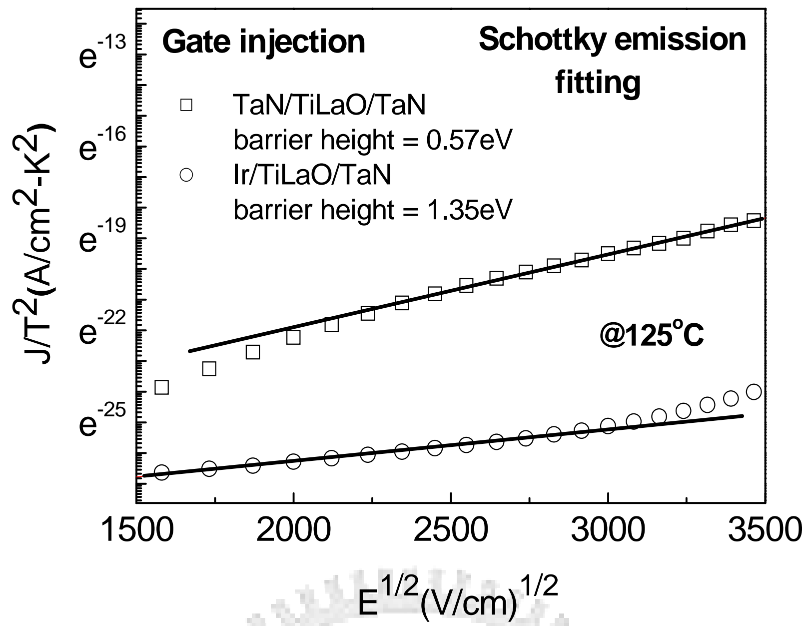


Fig. 4-3 The J/T^2-$E^{1/2}$ plots of TaN/TiLaO/TaN and TaN/Ir/TiLaO/TaN MIM capacitors.

Chapter 5

MIM Capacitors Using a High-κ TiZrO Dielectric for Analog and RF Applications

5.1 Introduction

The continuously increasing capacitance density ($\varepsilon\kappa/t_\kappa$) and preserving low leakage current are the technology trend of the Metal-Insulator-Metal (MIM) capacitors [5-1]-[5-18]. To achieve this goal, the using higher κdielectrics for MIM capacitors are required. However, the increasing κ value usually decreases the conduction band offset (ΔE_C) to the metal electrode, where the ΔE_C even becomes slightly negative (-0.1 eV) in $SrTiO_3$ (STO) [5-18]. Such small ΔE_C increases the unwanted leakage current of MIM capacitors [5-16], and therefore a trade off between ΔE_C and κ value is necessary. Besides, the κ value in STO is strongly dependent on the process temperature due to the formation of nano-crystals at above 450°C [5-16]. Unfortunately, such high temperature is above the maximum allowable temperature of 400°C for VLSI backend integration. In this paper, we report low leakage TiZrO MIM capacitors processed at 400°C. Using a low cost and high work-function (5.1 eV) Ni electrode, low leakage currents of 2.5×10^{-7} and 4×10^{-8} A/cm^2 at -2 V were measured for 18 and 5.5 fF/μm^2 capacitance densities, respectively.

These electrical characteristics are better than previously reported TiTaO [5-12]-[5-13] and TiHfO [5-15] capacitors. Besides, a small quadratic voltage coefficient of capacitance (VCC α) of 105 ppm/V^2 and temperature coefficient of the capacitance (TCC) of 156 ppm/^{o}C were measured in the 5.5 fF/μm^2 TiZrO MIM capacitor. Such excellent device characteristics are due to the higher ΔE_C for ZrO_2 (1.4 eV) than Ta_2O_5 (0.3 eV) and better κ of ZrO_2 than HfO_2 [5-19], [5-20]. These good devices performances of Ni/TiZrO/TaN capacitors can be used for multiple functional System-on-Chip (SoC) application.

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5.2 Experimental procedure

The high-κ TiZrO MIM capacitors were fabricated on Si wafers. For VLSI backend integration, a 2-μm thick SiO_2 isolation layer was first deposited on the Si substrates. After that, the combined bottom electrode of 200 nm Ta and then 50 nm TaN were deposited by sputtering. The TaN surface was exposed to a NH_3^+ plasma treatment to increase the oxidation resistance during the following post-deposition annealing (PDA) [5-5]-[5-6]. Then a 16 nm-, 47 nm- or 56 nm-thick $Ti_xZr_{1-x}O$ (x~0.67) dielectric layer was deposited by physical vapor deposition. A 400°C PDA in oxygen ambient was performed to reduce the defects in TiZrO and leakage current [5-3]. Finally, a 40 nm Ni and/or 50 nm Al was deposited and patterned to form the top electrode. A large capacitor size of

180-μm×180-μm was measured. The devices were characterized by *C-V* and *J-V* measurements.

5.3 Results and discussion

Figures 1(a) and 1(b) show the *C-V* and *J-V* characteristics of Ni/TiZrO/TaN and Al/TiZrO/TaN capacitors. A high capacitance density of 18 fF/μm^2 was measured at 500 kHz. At -2 V, the leakage current of TiZrO MIM capacitors improves by two orders of magnitude using a high work function Ni (5.1 eV) as compared with Al (~4.1 eV) electrode. At this 18 fF/μm^2 capacitance density, low leakage currents of 3.3×10^{-8} A/cm^2 and 2.5×10^{-7} A/cm^2 at -1 V and -2V were measured in Ni/TiZrO/TaN MIM capacitor, respectively. Table 1 summarizes the important device performance of various MIM capacitors. The Ni/TiZrO/TaN device data is better than that of the Ir/TiTaO/TaN MIM capacitors with a lower 14.3 fF/μm^2 capacitance density shown in Table 1, even though higher work function Ir top electrode (~5.27 eV) is used for TiTaO capacitor than Ni electrode (~5.1eV) for TiZrO. This is mainly attributed to the larger conduction band offset of ZrO_2 (1.4 eV) than that of Ta_2O_5 (0.3 eV) [5-19]. The device performance of Ni/TiZrO MIM capacitors is also better than the Ni/TiHfO [5-15], where higher capacitance density is obtained in Ni/TiZrO with comparable leakage current shown in Table 1. This is due to the higher κ for ZrO_2 than HfO_2 with close ΔE_C, which is the

reason why ZrO_2 is used in DRAM to replace HfO_2 [5-20]. For analog IC application, low VCC α is required. Figure 1 (c) showed the *ΔC/C-V* characteristics of TiZrO MIM capacitors, where VCC α can be extracted from the following equation: $C(V) = C_0(\alpha V^2 + \beta V + 1)$; α and β are quadratic and linear VCC, respectively. The VCC α is better using Ni electrode than that of Al. This may arise from the higher work function of Ni than Al, which exponentially decreases the free carriers injection from electrode by Schottky emission and lower the effect of charge relaxation [5-21].

To further lower the VCC, we fabricated TiZrO dielectric capacitors at larger 47 and 56 nm thickness. Figures 2(a), 2(b) and 2(c) show the *C-V*, *J-V* and *ΔC/C-V* characteristics of Ni/TiZrO/TaN capacitors at these TiZrO thicknesses. Low leakage current of 6.7×10^{-8} A/cm^2 and 4×10^{-8} at -2 V were measured at capacitance density of 6.5 and 5.5 fF/μm^2, respectively. Both the VCC α and β decrease with increasing TiZrO thickness or decreasing capacitance density. Small VCC α of 105 ppm/V^2 and VCC β of -757 ppm/V at 500 kHz were obtained at a 56 nm thickness of TiZrO with capacitance density of 5.5 fF/μm^2. From the experimental data presented in above Figs. 1(c) and 2(c), the VCC α improves with increasing metal work-function and dielectric thickness, where both cases give the lower charge injection into the capacitor. This is well explained by the charge injection model reported previously [5-21]. These good device performances

nearly meet the requirements of bypass capacitors used for RF circuits listed in International Technology Roadmap for Semiconductors (ITRS) at year 2012: with capacitance density >5fF/μm^2, VCC $|\alpha|$ <100 ppm/V^2 and VCC $|\beta|$ <1000 ppm/V [5-1].

The temperature coefficient of capacitance (TCC) is an important factor, since modern ICs usually operate at elevated temperatures. Figure 4 shows the measured normalized capacitance as a function of temperature. Small TCC values of 179 and 156 ppm/^{o}C were measured at 100 kHz for the 6.5 and 5.5 fF/μm^2 density TiZrO MIM capacitors, respectively. The decreasing trend of TCC with decreasing capacitance density is similar to the VCC α case, which again may be related to the charge trapping and relaxation in MIM capacitors [5-21].

Such improving trend of VCC α with decreasing capacitance density of MIM capacitors is summarized in Fig. 4. Here the variation of α is plotted as a function of *1/C* to show the dependence of capacitance equivalent thickness (CET=$\varepsilon_0\kappa$/C). The TiZrO shows better chance to meet the ITRS requirement at 2012 than HfO_2 and Ta_2O_5. Besides, for the same required VCC $|\alpha|$ <100 ppm/V^2, the TiZrO can have higher capacitance density than using HfO_2 and Ta_2O_5.

We have further studied the thermal stability of Ni/TiZrO/TaN capacitor. Figures 5(a)

and 5(b) display the *C-V* and *J-V* characteristics of Ni/TiZrO/TaN device before and after thermal annealing at 350°C for 20 min under N_2 ambient. Only a small degradation of the capacitance density and leakage current was found, which indicates the good thermal stability of both the top Ni electrode and the TiZrO dielectric.

5.4. Conclusion

We have investigated the device characteristics of Ni/TiZrO/TaN capacitors. Low leakage current and high capacitance density were obtained and better than previous reported MIM capacitors using TiTaO or TiHfO dielectric. Low leakage current, small VCC α of 105 ppm/V^2 and TCC of 156 ppm/^{o}C have been achieved in Ni/TiZrO/TaN MIM devices at 5.5 fF/μm^2 capacitance density. This high performance device is capable to be integrated into VLSI backend and be used in multiple functions associated with SoC.

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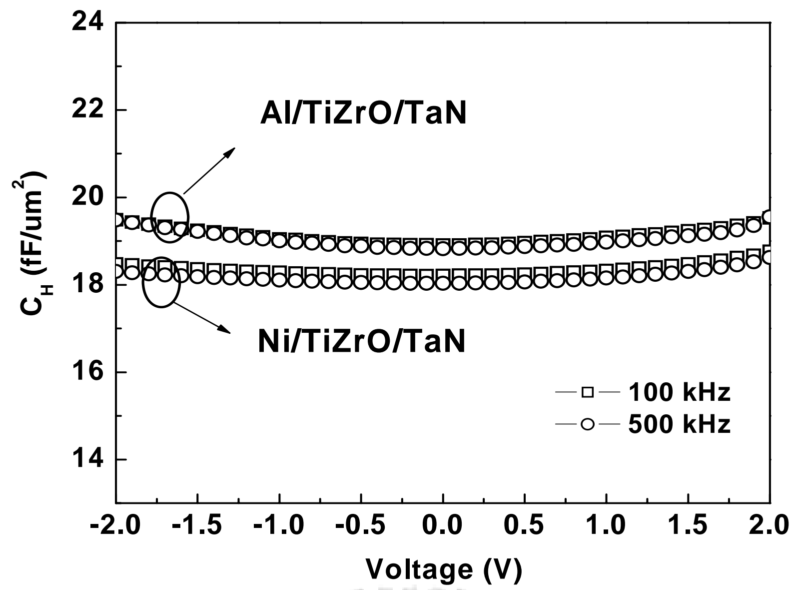
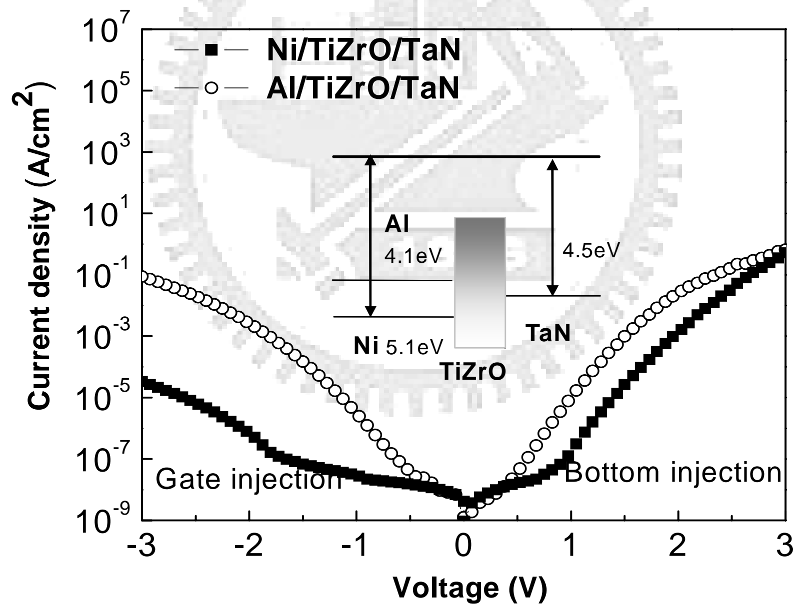
Table 5-1 Comparison of MIM capacitors with various dielectrics and metal electrodes.

	HfO_2 [5-8]	Tb-HfO_2 [5-10]	TiTaO [5-12]-[5-13]	TiHfO [5-15]	ITRS @ 2012 [5-1]	**TiZrO** (This work)		
Top Electrode	Ta	Ta	Ir	Ni	—	Ni		
Work-function (eV)	4.2	4.2	5.27	5.1	—	5.1		
C Density (fF/μm^2)	13	13.3	14.3	14.3	5	18	6.5	5.5
J (A/cm^2) @25°C	6×10^{-7} (2V)	1×10^{-7} (2V)	2×10^{-7} (2V)	8.4×10^{-8} (1V)	—	3.3×10^{-8} (1V) 2.5×10^{-7} (2V)	6.7×10^{-8} (2V)	4×10^{-8} (2V)
α (ppm/V^2)	607	2667	634	3392	α<100	3308	248	105



(a)



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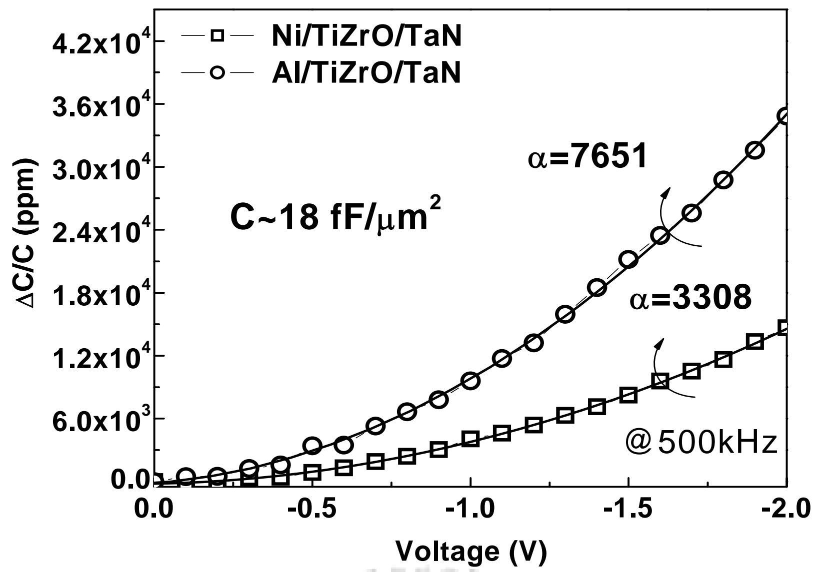
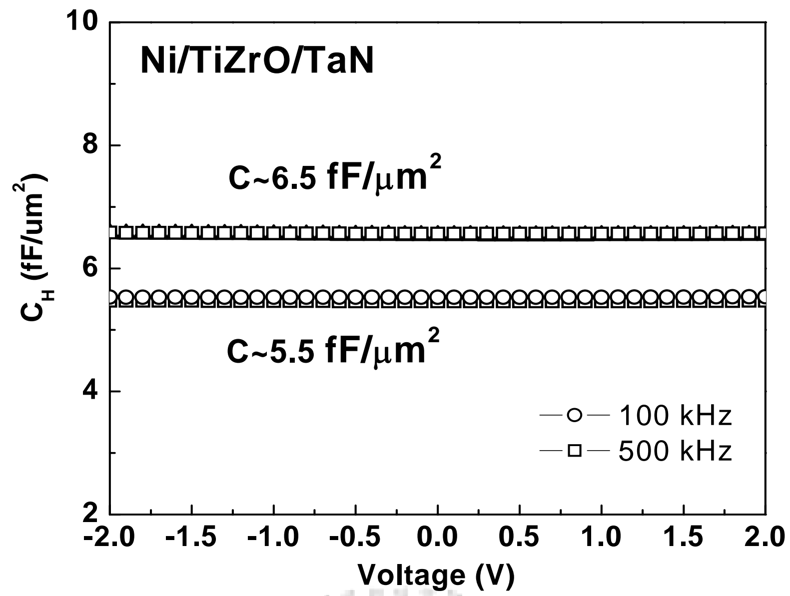


(c)

Fig. 5-1 (a) *C-V*, (b) *J-V* and (c) ΔC/*C-V* characteristics of Al/TiZro/TaN and Ni/TiZrO/TaN MIM capacitors.



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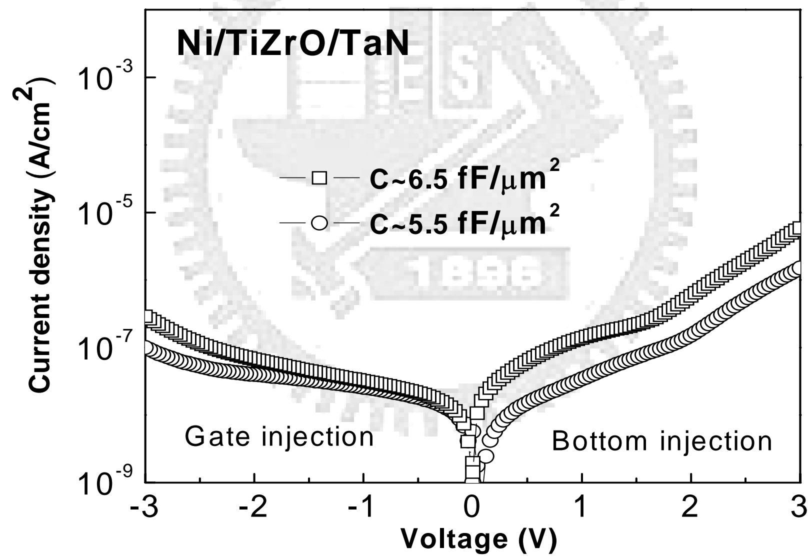

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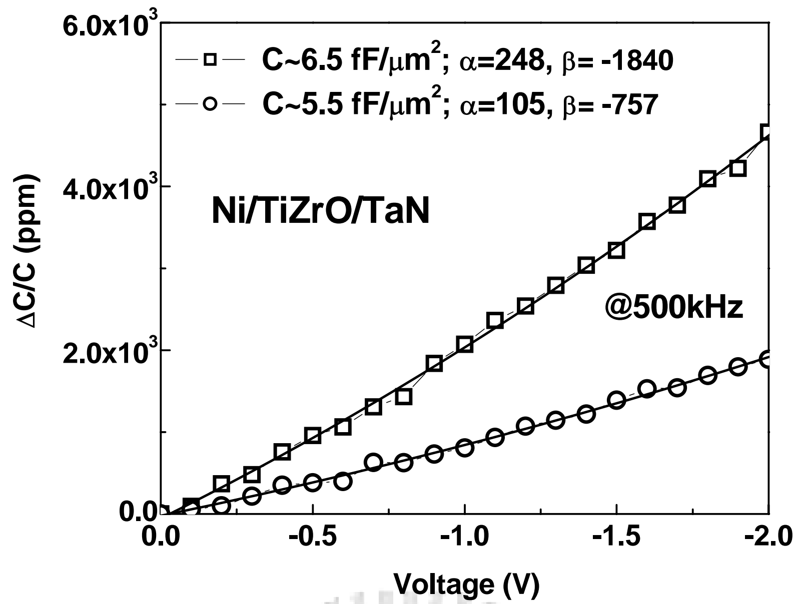


(c)

Fig. 5-2 (a) *C*-*V*, (b) *J*-*V* and (c) ΔC/*C*-*V* characteristics of Ni/TiZrO/TaN MIM capacitors with a 47 or 56 nm TiZrO dielectric thicknesses.

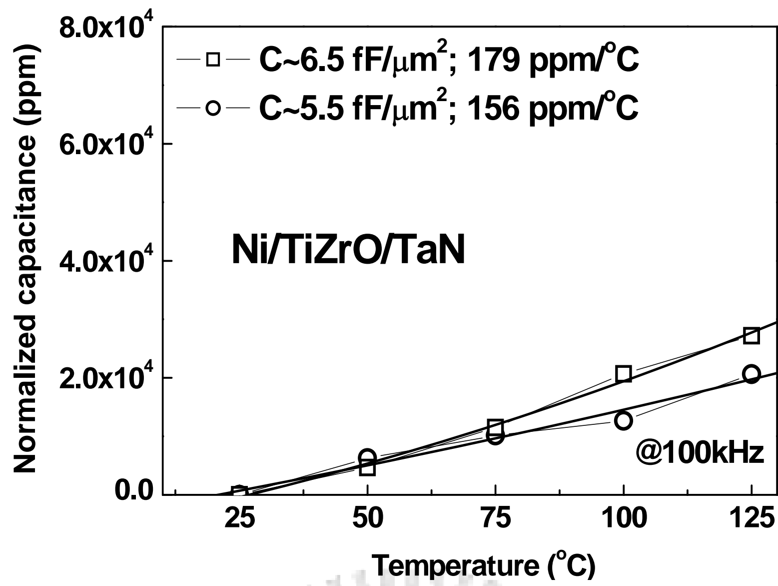


Fig. 5-3 Temperature-dependence of capacitance (TCC) characteristics of Ni/TiZrO/TaN MIM capacitors with 47 nm or 56 nm TiZrO dielectric thicknesses.

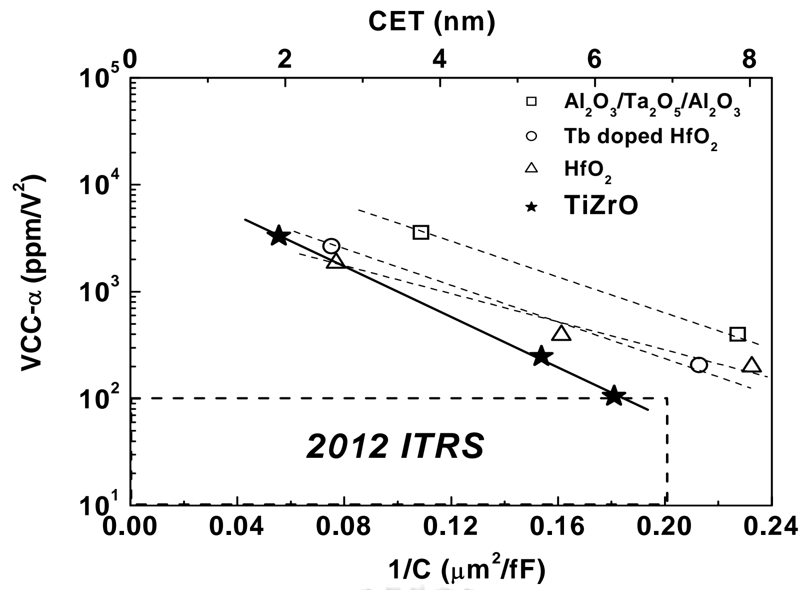
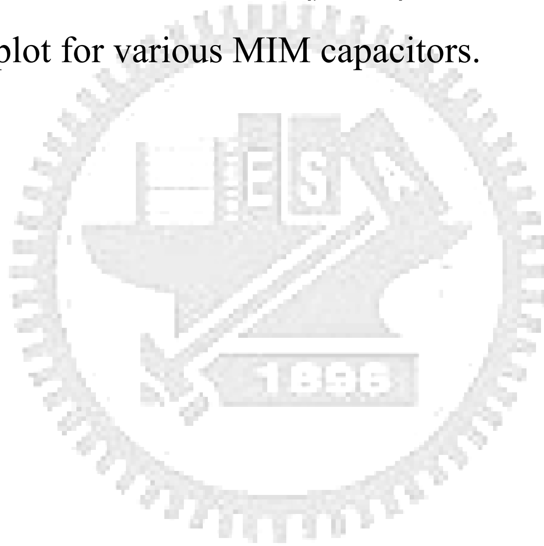
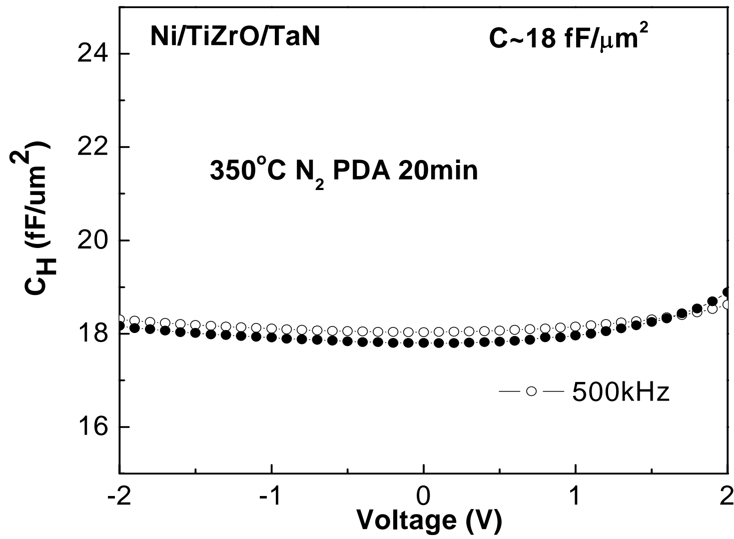


Fig. 5-4 *ΔC/C-1/C* plot for various MIM capacitors.





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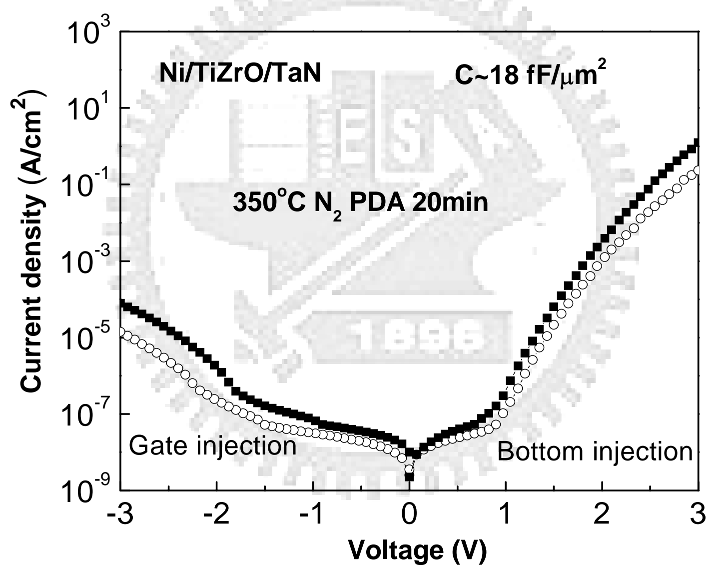


(b)

Fig. 5-5 Thermal stability behavior of (a) *C-V* and (b) *J-V* characteristics for Ni/TiZrO/TaN capacitors after a 350°C N_2 anneal for 20 min.

Chapter 6

Study on Stress Behavior of MIM Capacitors by Constant Voltage Stress

6.1 Introduction

Metal-Insulator-Metal (MIM) capacitors are important devices which are widely-used in Analog, RF and DRAM integrated circuits. The technological evolution of such capacitors [6-1]-[6-17] requires higher capacitance density and lower leakage current, while maintaining good reliability [6-17]-[6-18]. The only method to achieve the high capacitance ($\varepsilon_0\kappa/t_\kappa$) goal, without increasing the leakage current by decreasing the dielectric thickness (t_κ), is to use high dielectric constant dielectric (κ) materials. Thus, MIM capacitors have integrated higher κ dielectrics ranging from Al_2O_3 (κ=10) [6-3], HfO_2-Al_2O_3 (κ~15) [6-9], ZrO_2 (κ~30), TiTaO (κ~45-50) [6-12]-[6-14] to $SrTiO_3$ (κ>100) [6-15]-[6-17]. One drawback when using $SrTiO_3$ is the high thermal budget (>450°C annealing) which is needed to give the high κ value through the formation of nano-crystals [6-15]-[6-16]. This annealing temperature exceeds the normal 400°C maximum backend integration temperature. Other Ti-based ternary oxides, such as TiTaO, do not need such high processing temperatures but still display relatively high κ values.

Here we describe the performance and reliability of TiHfO MIM capacitors. By using a high-work-function Ni electrode (5.1 eV) we have found improvements in the leakage current and the voltage- or temperature-dependence of the capacitance (VCC or TCC), as well as the stress reliability, when compared with using a TaN (4.5 eV) upper electrode. The Ni/TiHfO/TaN devices displayed a capacitance density of 14.3 fF/μm^2 and leakage current of 8.4×10^{-8} A/cm^2 (1 V), and good reliability. The reliability was indicated by the small change in the capacitance ($\Delta C/C$) of ~1% - estimated for a 10-year operation at 1.5 V.

6.2 Experimental procedure

The high-κ TiHfO MIM capacitors were fabricated on standard Si wafers. For VLSI backend integration, a 2-μm-thick SiO_2 isolation layer was first deposited on the Si substrates. Then the TaN/Ta bi-layers were deposited by sputtering deposition and used as the lower capacitor electrode. The TaN surface was treated in a nitrogen plasma to increase the oxidation resistance, before subsequent high-κ deposition and annealing [15]-[17]. A 30 nm $Ti_xHf_{1-x}O$ (x~0.67) film was then deposited by RF sputtering at room temperature. The mixed composition was controlled by individual power supplies for the HfO_2 and TiO_2 targets. A 400°C post-deposition annealing (PDA) in an oxygen ambient was applied to reduce the defects and the leakage current. Finally, a 50 nm thick Ni or

TaN layer was deposited and patterned to form the top capacitor electrode. The fabricated devices, having a 30-μm×30-μm area, were characterized by *C-V* and *J-V* measurements, using an HP4155B semiconductor parameter analyzer and an HP4284A precision LCR meter, respectively.

6.3 Results and discussion

6.3.1. Basic electrical characteristics of TiHfO MIM capacitors

Figure 6-1 (a) and (b) of show the *C-V* and *J-V* characteristics of TiHfO MIM capacitors having different top electrodes. At 0 V, capacitance densities of 14.3~14.5 fF/μm^2 were measured, giving a κ value of 49 for the 30 nm thick TiHfO layer. The improved leakage for the Ni electrode case is not due to the 1.4% difference in capacitance value, but rather to the larger Schottky barrier height with respect to the TiHfO dielectric resulting in lower thermionic emission current from the top electrode. The reduced low leakage current is important for high density MIM capacitors, and avoids the increased costs associated with using a metal such as Ir (5.27 eV) [6-12]-[6-14].

The TCC and quadratic VCC (VCC-α) are important figures of merit for MIM capacitors. The $\Delta C/C$ can be expressed as $VCC\text{-}\beta \times V + VCC\text{-}\alpha \times V^2$, where $VCC\text{-}\beta$ is the linear coefficient of the VCC. Figures 6-2 (a) and (b) show the TCC and VCC-α for

TiHfO capacitors with different top electrodes. The Ni top electrode not only gives a lower leakage current but also improves the TCC and VCC-α. These improvements most probably arise from the higher barrier height between the electrode and the dielectric, which leads to a reduced carrier trapping and capacitance changes. This is confirmed by the lower capacitance at high temperature and the TCC at higher frequency. This is because the trapped charges and newly-formed dipoles cannot respond to rapid AC signals [6-12].

6.3.2. Stress behavior and reliability

The effects of constant voltage stress on VCC-α, leakage current and TCC and of [Ni or TaN]/TiHfO/TaN capacitor were investigated. Figure 6-3 (a) shows the $\Delta C/C$-V characteristics, before and after constant-voltage stress. The VCC-α increases with increasing stress voltage for the TiHfO MIM capacitors, for both TaN and Ni electrode cases. This is related to the trapped charges and the generation of new dipoles. The Ni top electrode still gives a better VCC-α than TaN, which this is due to the smaller charge injection over the metal/TiHfO barrier which produces fewer traps and charged dipoles. The lower leakage current after stress, shown in Fig. 6-3 (b), implies that there is electron trap generation in the high-κ TiHfO dielectric. We suggest that coulomb scattering from

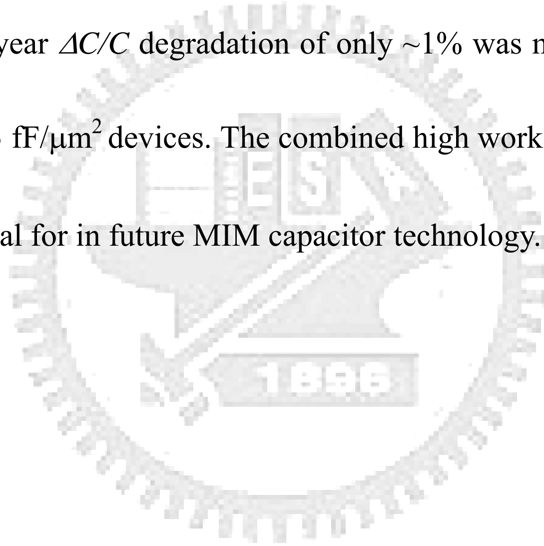
these traps lowers the charge injection from the top electrode. Again, the stress-related changes in the TiHfO devices are better when Ni is the top electrode rather than TaN. This is consistent with the smaller $\Delta C/C$ after stress, as shown in Fig. 6-3 (a). Figure 6-3 (c) displays the capacitance variation as a function of temperature, before and after constant-voltage stress. As with the VCC-α degradation with increasing stress voltage, the TCC increased after constant-voltage stress. Such stress-induced degradation in both VCC-α and TCC is attributed to the electron-trap generation and/or ion displacement, as explained above.

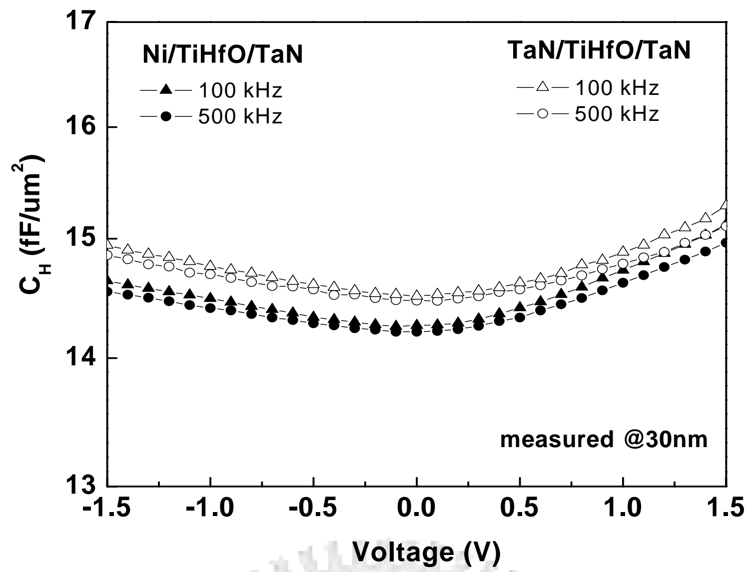
For circuit applications a 10-year reliability estimate is required [6-18]. Figure 6-4 (a) shows $\Delta C/C$ as a function of stress time, after constant-voltage stress in the 1.5 to 3 V range. The Ni-electrode MIM devices give superior performance in terms of a lower $\Delta C/C$ than the TaN case, even at higher stress voltages. Figure 6-4 (b) shows the extrapolated $\Delta C/C$ to a 10 year lifetime, for different stress voltages. The $\Delta C/C$ degradation increases with increasing stress voltage, the Ni electrode case being superior. The $\Delta C/C$ degradation of the TaN/TiHfO/TaN devices shows an unwanted strong dependence on stress voltage. Nevertheless the 10 year $\Delta C/C$ degradation is only ~1% at 1.5 V stress for both TaN and Ni top-electrode TiHfO capacitors. This long-time reliability is useful for the sub-65 nm technology node, where operating voltages can be <

1 V. Thus the choice of a proper high work-function electrode is as important as the high-κ dielectric in the MIM capacitors, as it is in advanced MOSFETs [6-19]-[6-20].

6.4 Conclusion

We have obtained significant improvements in the leakage current, TCC, VCC and long-term *ΔC/C* degradation in TiHfO MIM capacitors by using Ni as the top electrode rather than TaN. A 10 year *ΔC/C* degradation of only ~1% was measured at 1.5 V stress under 25°C for our 14.3 $fF/\mu m^2$ devices. The combined high work-function electrodes and high-κ dielectric are vital for in future MIM capacitor technology.





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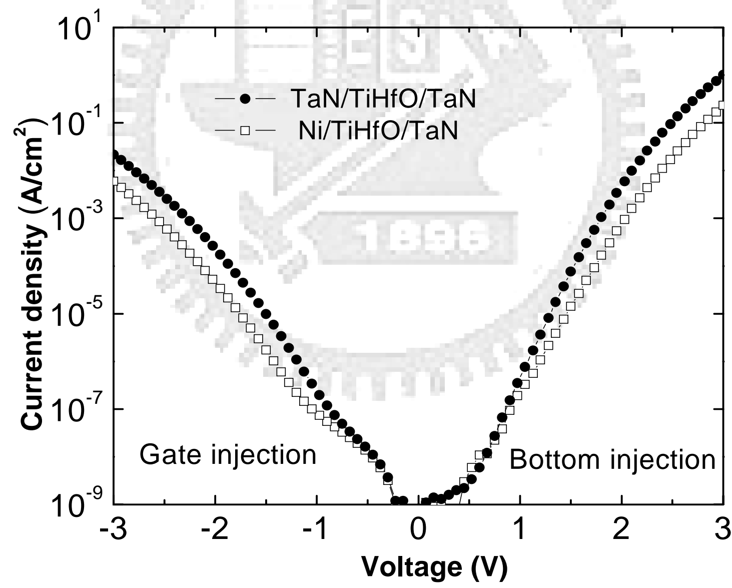
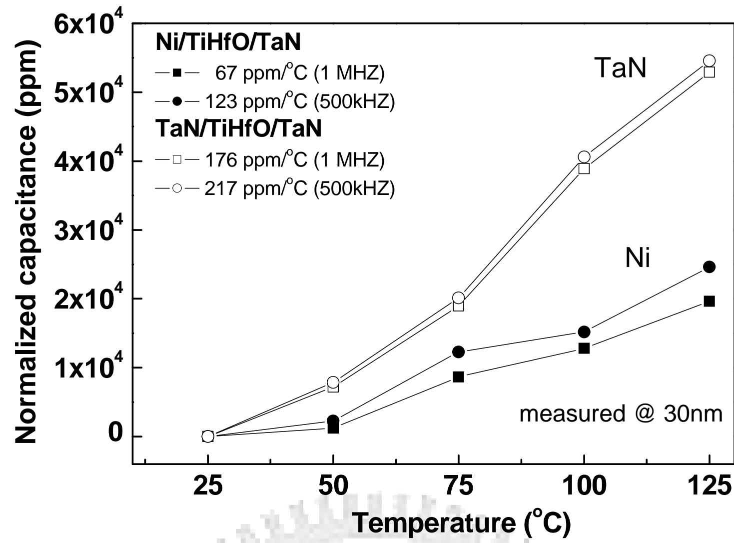


(b)

Fig. 6-1 (a) *C-V* and (b) *J-V* characteristics of the 30 nm TiHfO/TaN MIM capacitors with Ni or TaN top electrode



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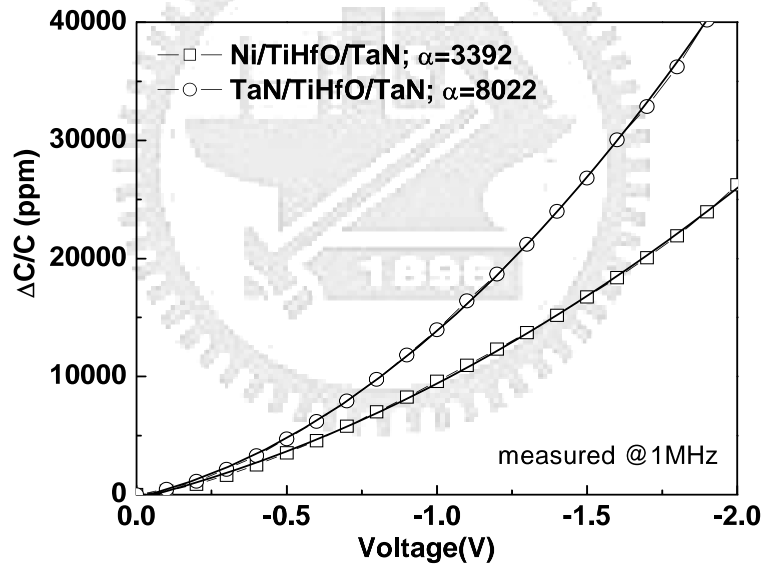
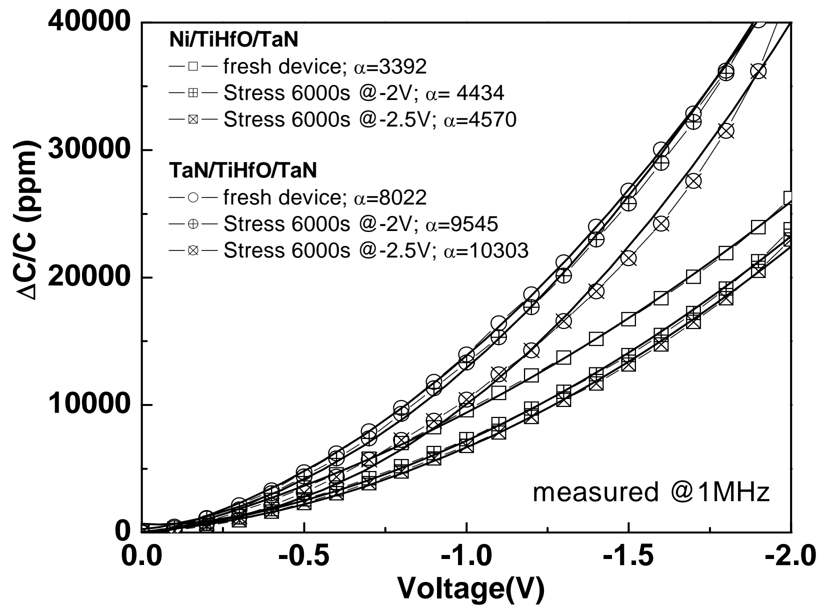


(b)

Fig. 6-2 (a) The temperature-dependent normalized capacitance and (b) *ΔC/C-V* characteristics of TiHfO MIM capacitors with Ni or TaN top electrodes.



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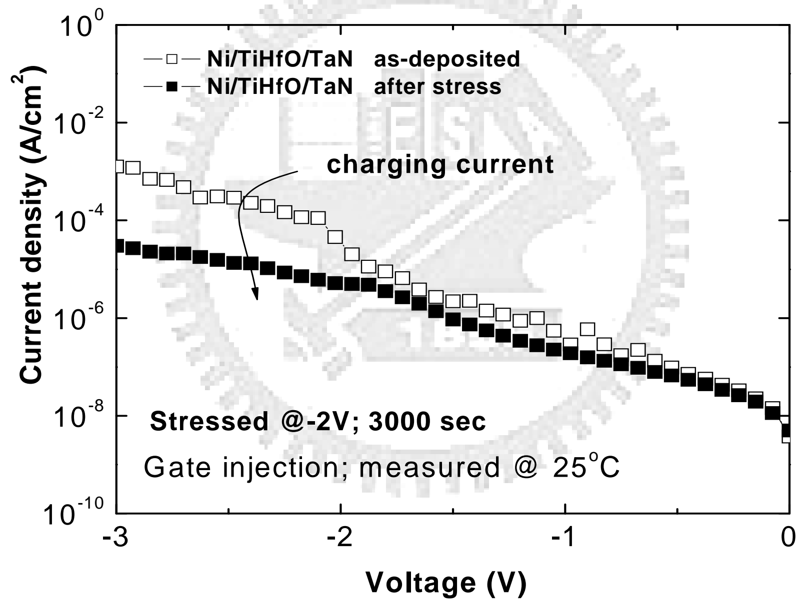

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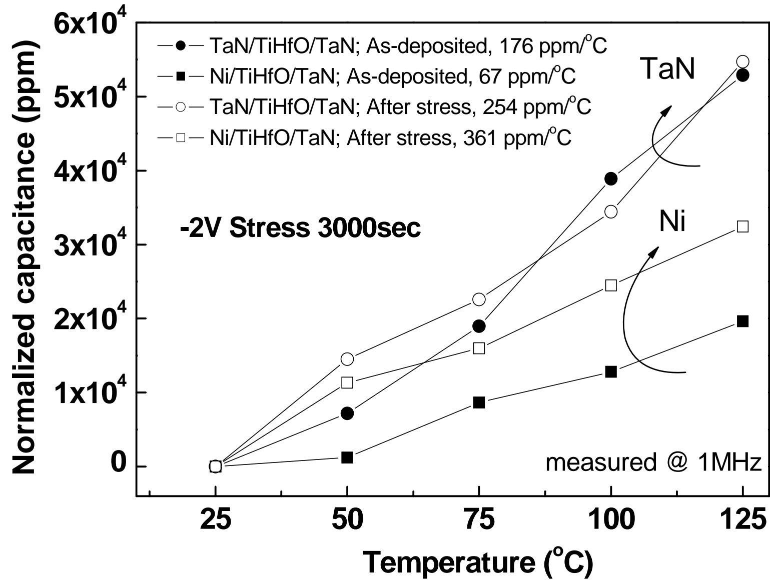
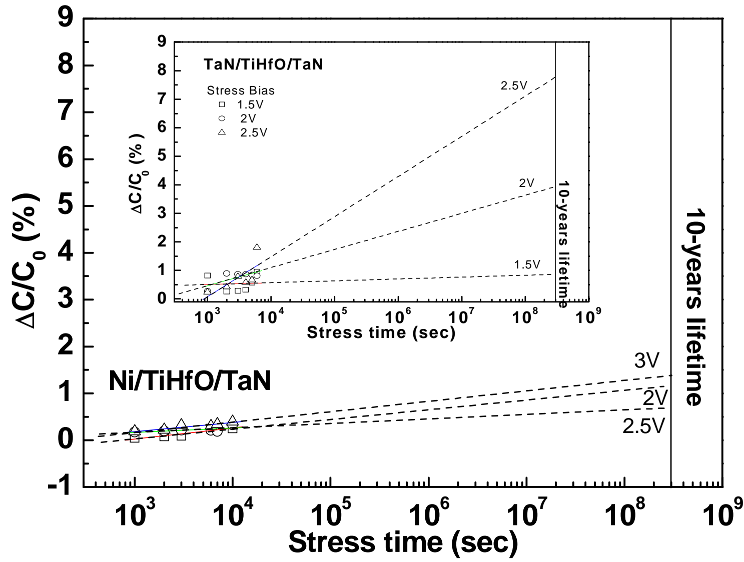


(c)

Fig. 6-3 The effect of constant-voltage stress on (a) VCC-α (b) *J-V* and (c) TCC of [Ni or TaN]/TiHfO/TaN capacitors.



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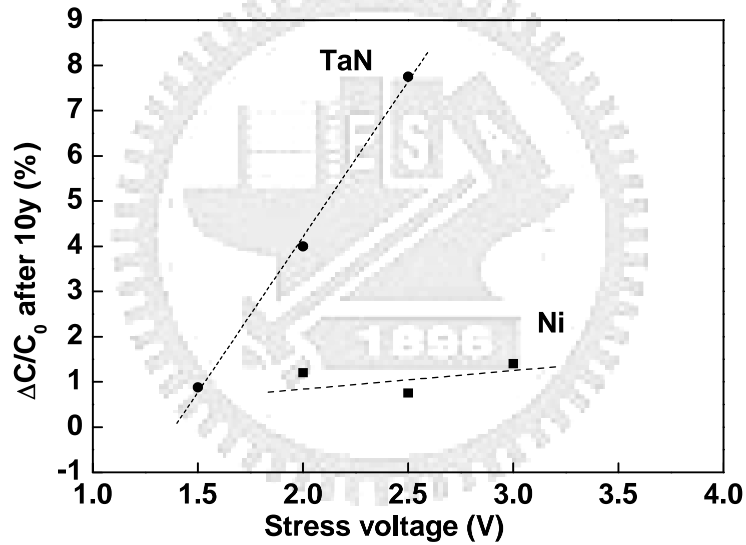


(b)

Fig. 6-4 (a) $\Delta C/C$ as a function of stress time and (b) extrapolated $\Delta C/C$ for a 10 year lifetime as a function of stress voltage for [Ni or TaN]/TiHfO/TaN capacitors.

Chapter 7

Using High Work Function Ni Metal to Improve the Stress Reliability of RF $SrTiO_3$ MIM Capacitors

7.1 Introduction

The passive RF metal insulator metal (MIM) capacitors scales down at a much slower rate and consumes a large portion of the whole die area. Therefore, it is necessary to increase the capacitance density for a smaller device area of RF capacitors used for impedance matching, dc blocking and filtering in RF circuits. $SrTiO_3$ (STO) has a large dielectric constant (κ ~50-200) and is also selected for DRAM candidate material beyond 50nm technology node [7-1], [7-3]-[7-5]. However, this stress degradation is a concern in low-breakdown field and small-bandgap $SrTiO_3$ materials, which also leads to high leakage currents because of the small conduction band discontinuity (ΔE_C ~-0.1eV) with respect to Si [7-7]. We have published the reliability of Analog STO MIM capacitors. [7-6] Here we describe the analog characteristics (VCC) of the STO MIM capacitors under constant voltage stress (CVS) at a GHz frequency for RF application. The use of high-work-function Ni instead of TaN electrodes not only reduces the high temperature leakage current, but also improves the degradations of the capacitance variation ($\Delta C/C$)

by constant voltage stress. The improved stress tolerance was caused by less mobile carrier injection due to higher barrier height reducing the charge detrapped from bulk or interfacial layer in the capacitors.

7.2 Experimental procedure

The process to integrate the MIM capacitors into a VLSI backend process began with depositing a 2-μm-thick SiO_2 isolation layer on the Si substrates. Then the TaN/Ta layers were deposited by sputtering and subsequently treated in a nitrogen plasma, which largely improves oxygen deficiency and capacitance density degradation by forming interfacial TaON during post-deposition anneal (PDA). A 25nm-thick sputtered STO dielectric was then deposited, followed by a 420°C furnace anneal for 30 min under an oxygen ambient. Finally, TaN or Ni was deposited and patterned to form the top capacitor electrode. The fabricated devices, having a 20-μm×20-μm area, were characterized by *C*-*V* and *J*-*V* measurements using an HP4156B semiconductor parameter analyzer and an HP4284A precision LCR meter, respectively. The *S*-parameters to 10 GHz were measured by HP8510C network analyzer and the measured *S*-parameters were followed by a standard deembedding procedure using a dummy open devices. The series parasitic impedances in RF transmission lines are also deembedded using a through dummy device. The RF frequency capacitance value was extracted from measured *S*-parameter using an

equivalent circuit model.

7.3 Results and discussion

Figures 7-1 (a) and (b) showed the band diagram before contact for [Ni or TaN] STO MIM devices respectively. The Ni metal with 5.1eV work function can form larger work function difference than TaN metal of 4.5eV after contact. In Figure 7-2 (a) and (b) we showed the *C-V* and *J-V* characteristics of Ni/STO/TaN and TaN/STO/TaN devices. A high capacitance density of 17 ~ 20 fF/μm^2 was measured at 25°C and capacitance density increase with temperature increasing to 125°C. This is because higher thermal budget increases the probability of thermally activated carriers jump from metal side cross the barrier. The *C-V* characteristics in Figure 7-2 (a) showed that the Ni electrode has less capacitance increase due to high work function suppressed the number of mobile charges from bulk or interfacial layer at 25°C or 125°C. On the other hand, larger barrier height caused by higher work function not only reduced the leakage current but also resisted from performance deterioration by long-term reliability stress. The *J-V* characteristics of Figure 7-2 (b) also showed the stress behavior of stress induced leakage current (SILC) caused by hole generation and the high work function Ni electrode presented a good performance against stressed degradation. The Figure 7-3 (a) shows the measured S-parameter for [Ni or TaN]/STO/TaN capacitors. The capacitance values at RF

frequency were extracted using the equivalent circuit model in Figure 7-3 (b). The MIM capacitor is modeled by Rp and C, where the Rp originates from the hi-κ dielectric loss. In addition, the R_s, L_{s1}, and L_{s2} represent the parasitic impedances in the coplanar transmission line used for RF measurements. Good agreement between measured and simulated data are obtained over entire frequency range from 200 MHz to 10 GHz indicating the equivalent circuit model suitable and reliable for TaN/STO/TaN modeling and capacitance value extraction.

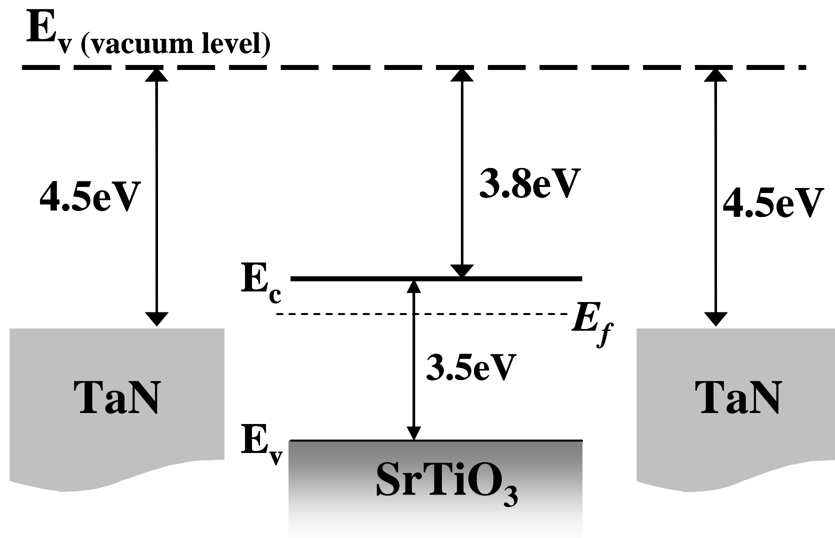
In order to evaluate the long term performance of STO MIM used for RF capacitors, we implement the stress reliability by constant-voltage stress (CVS). The capacitance variation as a function of the frequencies showed in Figure 7-4 (a). The capacitance variation decreases with the frequencies increasing since the charges fail to follow the AC signal in high frequency and increases with the temperature due to the higher carrier injection at higher temperature, which increase largely the number of mobile charges leads to a larger capacitance variation.

For analog/RF functions in a circuit, both a small $\Delta C/C$ and $VCC\text{-}\alpha$ are required. Here $\Delta C/C$ can be expressed as $VCC\text{-}\beta \times V + VCC\text{-}\alpha \times V^2$, where β is the linear coefficient of the VCC. Figure 7-4 (b) and (c) show the effect of constant-voltage stress on the $\Delta C/C\text{-}V$ characteristics of STO MIM capacitors with TaN or Ni electrodes. By

using Ni the required small $\Delta C/C$ and $VCC\text{-}\alpha$ were achieved, regardless of the stress. In general the stress produced a lower $VCC\text{-}\alpha$, which is related to the charge trapping in the STO and the STO/metal interface. The trapped charges decrease the carrier mobility in the dielectric by electrostatic scattering, which in turn produces a smaller $VCC\text{-}\alpha$, according to a free-carrier-injection model [7-2]. Large work function Ni used to obtain higher barrier height may cause less traps to form new dipole and achieve better VCC-α. Besides, the stress behavior for Ni case at 125°C by constant-voltage stress observed from Figure 7-4 (c) not only shows the improvement on stress performance at room temperature but also at 125°C.

7.4 Conclusion

Although the very high κ STO dielectric has a large potential for DRAM technology beyond 45nm node, the low bandgap of STO may be an important issue for long-term reliability. The use of high work function electrode not only suppresses the leakage current at high temperature but also improves the VCC-α under stress-processing as well as high-temperature stress reliability.



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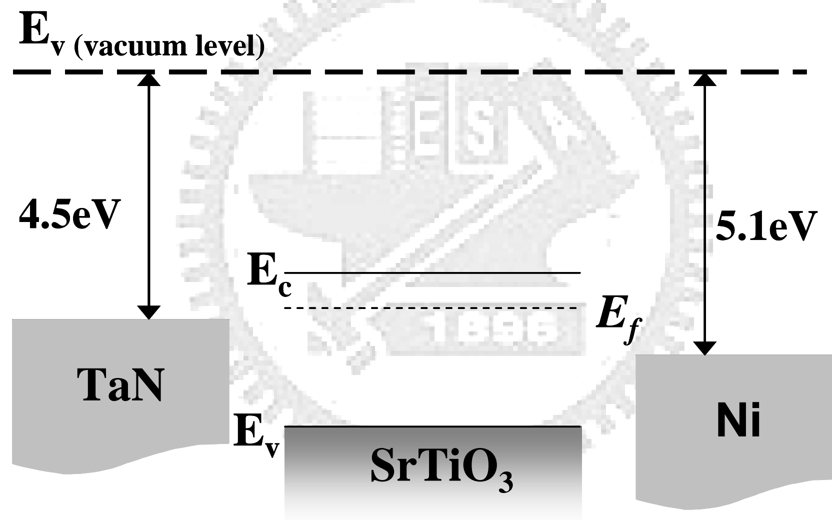
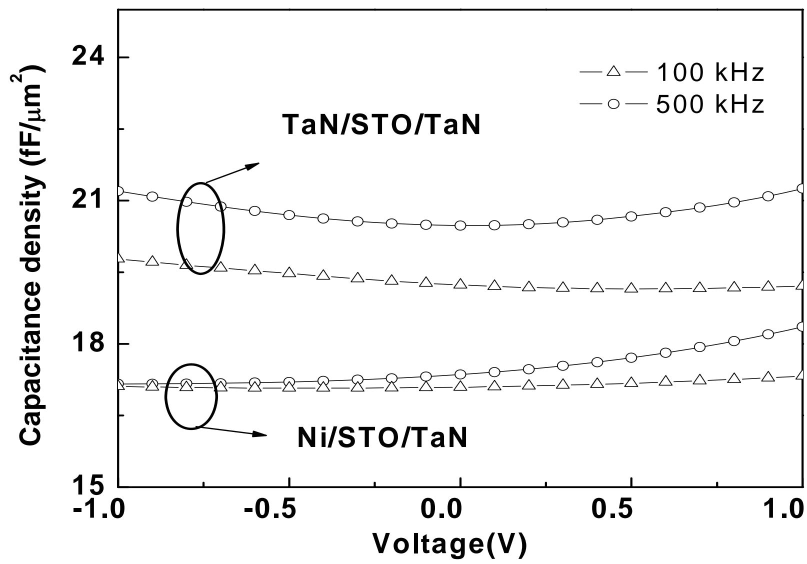


(b)

Fig. 7-1 Band diagrams before contact for (a) TaN or (b) Ni /$SrTiO_3$/TaN MIM capacitors.



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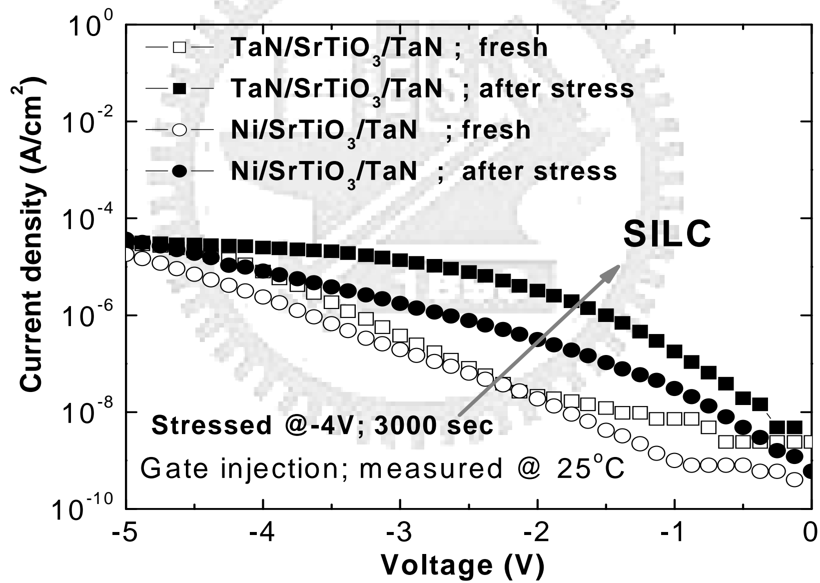


(b)

Fig. 7-2 *C*-*V* characteristics of (a) [Ni or TaN]/STO/TaN at 25ºC or 125ºC and (b) *J*-*V* characteristics of [Ni or TaN]/STO/TaN under CVS test at 25ºC or 125ºC.

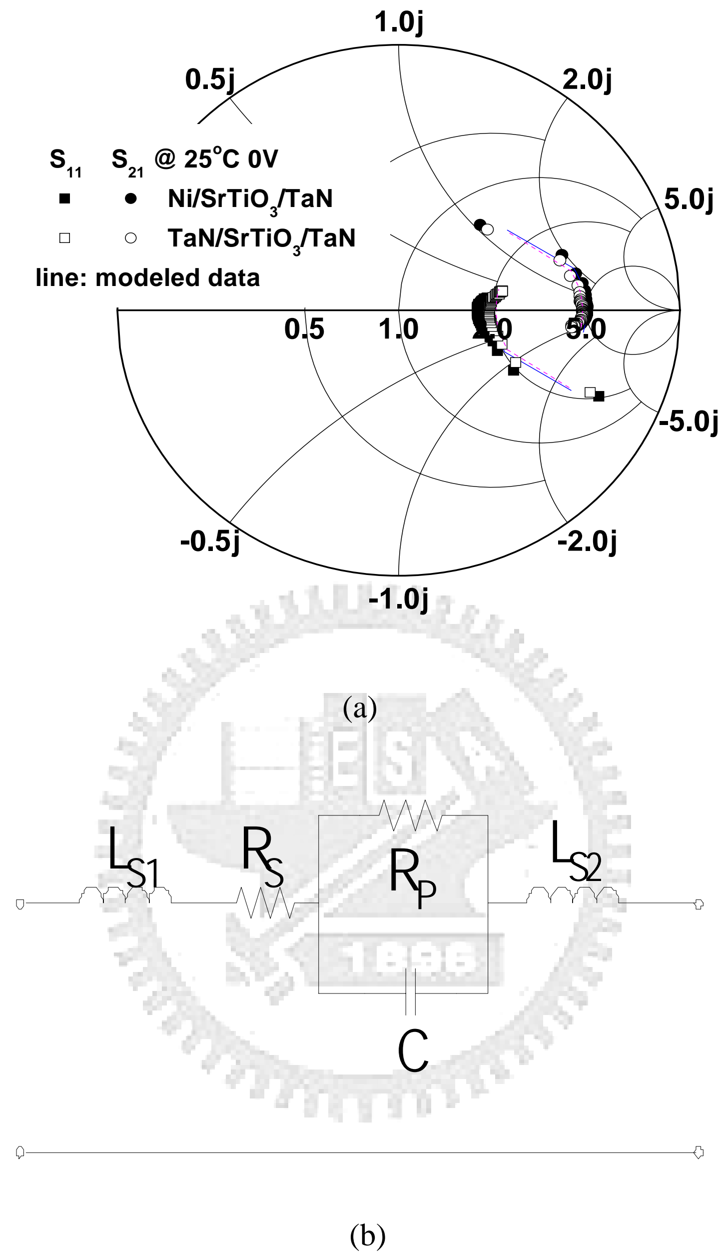
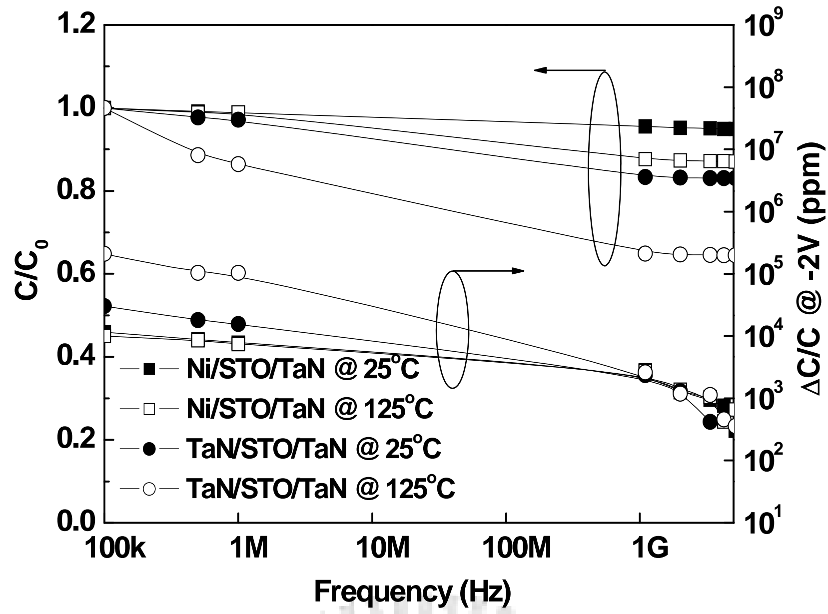


Fig. 7-3 (a) Measured and simulated two-port S-parameters for $SrTiO_3$ MIM capacitors (b) The equivalent circuit for capacitor value extraction from measured S-parameters.



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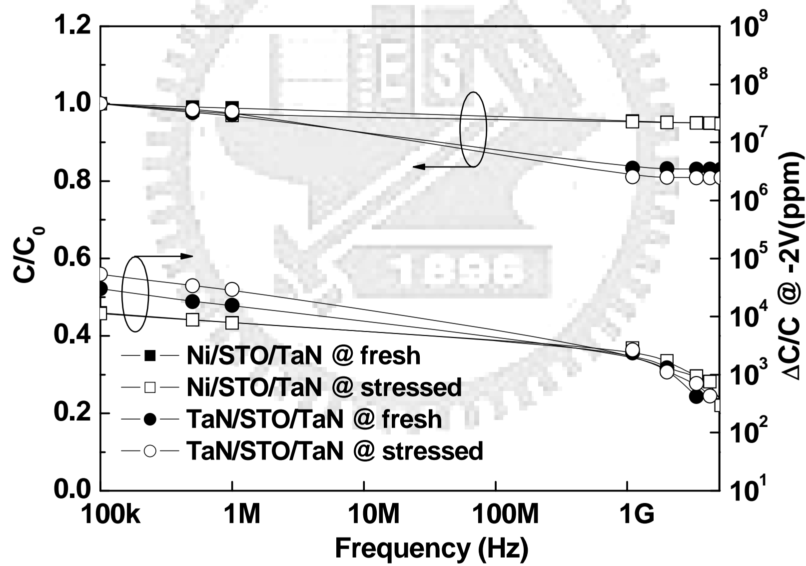

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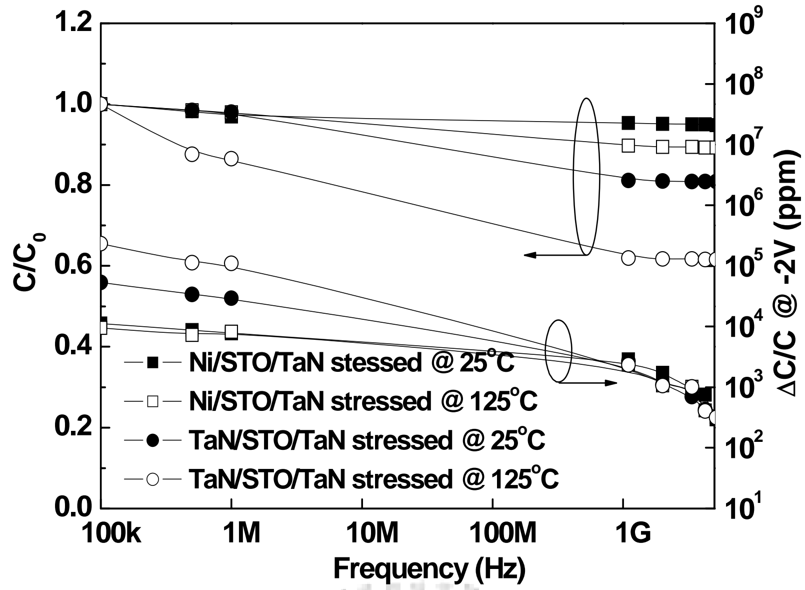

(c)

Fig. 7-4 The *ΔC/C* of [Ni or TaN]/STO/TaN capacitors which measured (a) at 25ºC and 125ºC, (b) before or after CVS and (c) stressed devices measured at 25ºC and 125ºC.

Chapter 8

Conclusion

For DRAM technology, the interfacial layer is responsible for high leakage current, degraded capacitance density and poor VCC-α, which may be caused by higher trap density at the interfacial region. We have developed successfully a novel dual plasma treatment on bottom TaN electrode to improve the electrical properties of MIM capacitors. By using an additional oxygen plasma treatment the interfacial reactions and growth were reduced, leading to a higher capacitance density and lower leakage current.

To integrate the MIM capacitors into a VLSI backend, along with advanced low-κ isolation dielectrics, or with future front-end GOI and IIIVOI technologies, a low temperature crystallized TiO_2 MIM capacitor was fabricated at 300°C and showed a good performance. Besides, with the increase of power dissipation in VLSI circuits, a thermal leakage evaluation of RF capacitors is an important issue. In this thesis, we have proposed an Ir/TiLaO/TaN MIM capacitor which exhibits a very low leakage current at 125°C. The analog characteristics of VCC and TCC are also important index to evaluate a RF capacitor except for leakage current. Low leakage current, small VCC-α of 105 ppm/V^2 and TCC of 156 ppm/^{o}C have been achieved in

Ni/TiZrO/TaN MIM devices at 5.5 fF/μm^2 capacitance density. The TiZrO shows a good performance to meet meets the ITRS requirement at 2012 for Analog/RF application. Moreover, the high work function Ni electrode has been successfully developed and integrated into the process of DRAM stacked capacitors in the industry through our effort.

Besides, a small capacitance variation (ΔC/C) and voltage coefficient of capacitance (VCC-α) affected by mobile charges existing in dielectrics or interfacial layer are especially important for RF application. Therefore, the evaluation on analog characteristics is necessary for the long-term operation. Here, we proposed a method using a constant voltage stress (CVS) on MIM capacitors to observe stress behavior and further evaluate the electrical and analog characteristics of RF MIM capacitors for the long-term reliability.

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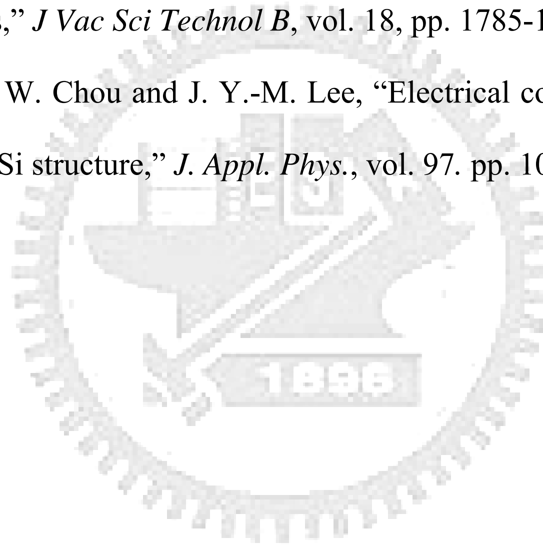

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