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Overlapped patch elimination algorithm for deformable mesh video coding

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Indexing terms: Object detection, Motion estimation, Video coding

Updating mesh nodal points is one of the major tasks in deformable mesh video coding. Owing to object movement and inexact motion estimation, nodal point tracking often results in overlapped patches. A noniterative nodal point processing algorithm is proposed to solve this problem. Simulation results indicate that with this overlapped patch elimination algorithm, the updated mesh can maintain a rather uniform distribution and the moving object can be traced quite well.

Introduction: Video compression technology plays an important role in the transmission of video signals through channels with constrained capacity. Recently, deformable mesh coding has been explored [1-3]. Digital image warping is different from conventional block-based schemes and is used to reduce the interframe correlation between two successive frames. Because of the mesh shape adjustment ability, it produces less noticeable blocking artefacts in compensated pictures. More importantly, the object boundaries can be described in an efficient way to achieve object scalability.

There are two mapping directions for mesh warping, forward mapping and backward mapping. Forward mapping, together with object-based mesh adjustment, can provide an object tracking capability [1-3]. However, it is rather difficult to maintain the mesh structure during the tracking process. Inaccurate motion estimation of nodal points may cause overlapped patches. To solve this problem, Wang and Lee [1] used an energy minimisation criterion. In their criterion, the deformation energy term is used to avoid mesh degeneration. However, their iterative procedure is quite complicated. In this Letter, we propose a noniterative nodal point processing algorithm used in conjunction with the conventional motion estimation algorithm i.e. block matching.

Proposed algorithm: In the development of our algorithm, we have adopted the coding structure in [2]. This structure includes two subsystems: a nodal tracking subsystem and a coding subsystem. In the tracking subsystem, the foreground object is separated from the background by conducting an image segmentation algorithm on the first frame. We then estimate the motion vector associated with each nodal point. A nodal point processing procedure is devised to adjust meshes so that illegal patches (defined below) are eliminated. The procedure involves three steps: (i) relocation of the ambiguous nodal points; (ii) merging the nearby nodal points and (iii) adjustment of the nodal points of illegal patches. The details are described below.

Inaccurate estimation is often the main reason which leads to degenerated patches, and usually occurs in the smooth regions of an image. Therefore, we interpolate the co-ordinates of the nodal points located in the smooth region based on the nearest object boundary nodal points. Assume that (x_c, y_c) is the co-ordinate of the nodal point in the smooth region, and (x_l, y_l) , (x_r, y_r) , (x_t, y_t) , and (x_b, y_b) are the nearest left, right, top, and bottom boundary nodal points updated by the motion estimation algorithm, respectively. Let n_l, n_r, n_t, n_b denote the distances between these four points and (x_c, y_c) , respectively. The new nodal location is then the average bilinear interpolation of these four points. That is

$$\begin{aligned} x_c &= \frac{1}{2} \left(\frac{d_r x_l + d_l x_r}{d_l + d_r} + \frac{d_b x_t + d_t x_b}{d_t + d_b} \right) \\ y_c &= \frac{1}{2} \left(\frac{d_r y_l + d_l y_r}{d_l + d_r} + \frac{d_b y_t + d_t y_b}{d_t + d_b} \right) \end{aligned} \quad (1)$$

This interpolating process not only avoids inaccurate estimation in the smooth region, but also maintains a uniformly distributed mesh.

When an object is tracked for more than several frames, the neighbouring nodal points may either cluster together or depart from each other. Some patches are squeezed while the others are stretched. Patches may even overlap if no specific actions are taken. Therefore, we merge the nearby nodal points to eliminate degenerated or illegal patches. For each nodal point, we check its distance relative to the eight neighbouring nodal points. If any of them is less than a threshold (usually set to 3), the following merging steps are performed to this pair of nodal points.

- (i) If one nodal point is located on the image border, the other nodal point is merged to this nodal point.
- (ii) If one nodal point is located on the edges, the other nodal point is merged to this nodal point to retain the edge information.
- (iii) If this pair of nodal points is located horizontally, we measure the distance between the left nodal point and the nearest nodal point to its left, called the left distance. We also measure the distance between the right nodal point and the nearest nodal point to its right, which is the right distance. If the left distance is greater than the right distance, then the right nodal point is merged to the left one, otherwise, the left nodal point is merged to the right one. A similar check and merge step is applied to the pair located vertically to maintain mesh uniformity.

Even with the above nodal point adjustment steps, we still cannot guarantee that all the degenerated patches are eliminated. Thus, we further check the four vertices of each patch based on the convex quadrilateral constraint [4]. If a quadrilateral patch is convex, all the vector cross products of the adjacent vectors (class 0 in Fig. 1) must be positive. That is

$$\begin{aligned} \mathbf{V}_0 \times \mathbf{V}_1 &> 0 \text{ for the vertex } P_0 \\ \mathbf{V}_1 \times \mathbf{V}_2 &> 0 \text{ for the vertex } P_1 \\ \mathbf{V}_2 \times \mathbf{V}_3 &> 0 \text{ for the vertex } P_2 \\ \mathbf{V}_3 \times \mathbf{V}_0 &> 0 \text{ for the vertex } P_3 \end{aligned} \quad (2)$$

In Fig. 1, all possible shapes of quadrilateral patches are displayed and classified into four classes. The class number is named after the number of rules being violated in eqn. 2. For coding purposes, we further divide these patches into two groups: legal and illegal. Illegal patches contain a negative area (i.e. an overlapped area). If an illegal patch is encountered, we merge a vertex that violates the constraint in eqn. 2 to a nearby vertex to force this patch to become legal in the same class. The location of the merged vertex is selected using the same rules described in the previous paragraph.

Simulation results: The 'Suzie' sequence is used to test the proposed algorithm. Its picture size is 352 pixels by 240 lines and 30 frame/s. The initial regular mesh is composed of 8×8 square patches. The exhaustive search block matching algorithm with half-pixel accuracy is used to estimate the motion vectors.

Table 1: Number of overlapped patches with/without nodal point processing

Frame number	5	10	15	20	25	30
Without processing	4	7	8	12	14	24
After step (i)	0	0	2	4	5	10
After step (ii)	0	0	0	1	1	2
After step (iii)	0	0	0	0	0	0

Table 1 shows the number of overlapped patches (see Fig. 1) in some sampled frames. In general, the number of overlapped patches increases as the frame number increases. After using the merging steps of our method, this number is reduced dramatically. Finally, with convex quadrilateral checking, all the overlapped

patches are eliminated. Fig. 2 shows the mesh structure of the 30th frames using our procedure. After a number of frames, the mesh is still quite uniform and the object is traced very well.

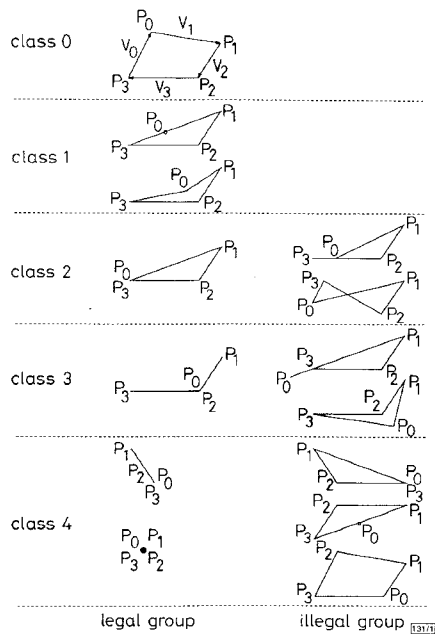


Fig. 1 All possible quadrilateral patches



Fig. 2 Mesh structure in 30th frame of 'Suzie' sequence

Conclusions: In this Letter, we have presented a nodal point processing algorithm in conjunction with the conventional motion estimation techniques for nodal point tracking in deformable mesh coding. Using a simple procedure on the nodal points, all the overlapped patches can be eliminated. Because of the nodal distance consideration in our merging steps, the processed mesh is quite uniform, which reduces the position errors resulting from motion estimation. Owing to its noniterative procedure and simpler arithmetic operations, this method needs a small amount of computational power.

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1.5V power supply CMOS voltage squarer

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Indexing terms: Power supply circuits, CMOS integrated circuits

A CMOS voltage squarer for low voltage applications is proposed. The circuit works with a 1.5V power supply and provides a THD of <3% with input signals up to 260mV_{pp}. A 0.3% lower THD is achieved with input signals up to 120mV_{pp}.

Introduction: Low voltage operation has become a major design goal for most digital and analogue integrated circuits (ICs). This is because a low voltage power supply reduces the power consumption, which in turn means both an increase in the packing density, and an increase in the battery lifetime of portable equipment. Therefore, the design of analogue ICs with a low power supply is becoming mandatory, and great effort is currently devoted to the development of new solutions working with a 1.5V, or even lower voltage power supply [1-4]. Moreover, owing to scaling of CMOS processes to submicrometre dimensions, low voltage nonlinear CMOS circuits are gaining more attention by circuit designers who are involved in the realisation of RF front ends for cellular and cordless communications.

A useful nonlinear block is the voltage squarer [5-7]. Indeed, it can properly be arranged to implement various nonlinear circuits such as multipliers, balanced modulators, phase comparators, etc.

In this Letter a simple CMOS squarer is proposed which has a power supply of 1.5V and accepts input signals of up to 260mV_{pp}.

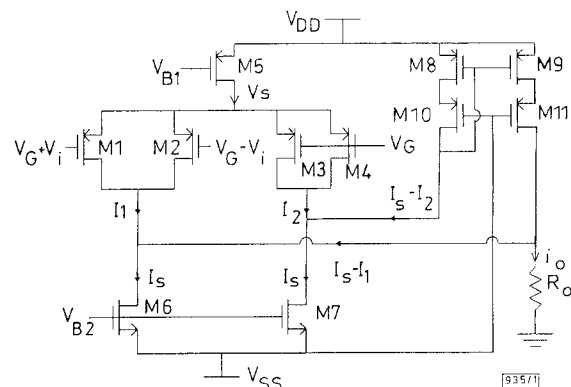


Fig. 1 Schematic diagram of voltage squarer

Circuit description: The proposed squarer is shown in Fig. 1. Transistors M1-M4 perform the basic squarer function, M5-M7 set the bias currents and M8-M11 form a low-voltage cascode current mirror, which provides the differential-to-single ended conversion.

The squarer function is obtained by properly taking advantage of the input-output characteristic of the MOS transistors in the saturation region. Indeed, considering transistors M1-M4 to be in the saturation region and neglecting the channel-length modulation, the mobility degradation, and the body effect, we can state

$$i_{D1} = \frac{\mu_p C_{ox}}{2} \left(\frac{W}{L} \right)_1 (V_s - V_G - v_i + V_{TP})^2 \quad (1)$$

$$i_{D2} = \frac{\mu_p C_{ox}}{2} \left(\frac{W}{L} \right)_2 (V_s - V_G + v_i + V_{TP})^2 \quad (2)$$