The Effect of Film Thickness on the Electrical Properties of LPCVD Polysilicon Films

N. C. C. Lu

IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598

C. Y. Lu

The Institute of Electronics, National Chiao-Tung University, Hsin-Chu, Taiwan, China and Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina 27650

M. K. Lee, C. C. Shih, and C. S. Wang

The Institute of Electronics, National Chiao-Tung University, Hsin-Chu, Taiwan, China

W. Reuter

IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598

T. T. Sheng

AT&T Bell Laboratories, Murray Hill, New Jersey 07974

ABSTRACT

The effect of film thickness on the electrical properties of boron-doped LPCVD polysilicon films with doping concentration ranging from 1×10^{17} to 1×10^{19} cm^{-3} has been characterized from 1.2 μm down to 0.1 μm. The resistivity increases exponentially as the film thickness decreases, rather than remaining constant, and the rate of increase is a strong function of doping concentration. After a quantitative study on the physical mechanisms which can affect the resistivity as film thickness decreases, the carrier trapping effect due to grain-size variation at different film thicknesses is shown to be the dominant factor. A trapping model without assuming the depletion approximation can explain well the experimental data and enhances understanding of the resistivity behavior as the polysilicon film thickness decreases.

Polycrystalline-silicon (polysilicon) material is composed of aggregates of single crystal grains with a grain boundary between adjacent grains. The grain boundary is a transitional region between different orientations of neighboring crystallites. Polysilicon films have been widely used in integrated circuits such as silicon gates, interconnections, passivation or isolation layers, diffusion sources, resistors, monolithic distributed RC filters, diodes, active devices, and redundancy programming elements. Its increasing range of applications ensures the importance of this material in the coming era of VLSI.

Since the demand for better performance and higher packing density of VLSI circuits requires the device size to be scaled not only in the horizontal but also in the vertical direction, the thickness of polysilicon films used in most integrated-circuit applications has been scaled from several micrometers (1, 2) down to tenth of a micrometer (3). In addition, the film deposition generally has changed from atmospheric-pressure chemical vapor deposition (APCVD) (1, 2) to low-pressure chemical vapor deposition (LPCVD) (4) for better film quality and higher throughput. As a result, understanding of the thickness scaling effect on the electrical properties of LPCVD polysilicon films in the submicrometer range is important for device design in VLSI circuits.

Kamins (1) studied the thickness dependence of Hall mobility and resistivity in APCVD polysilicon films, which had thickness ranging from 3 to 24 μm and were doped by diffusion with concentrations ranging from 10^{18} to 10^{19} cm^{-3}. Resistivity of these polysilicon films decreases with increasing film thickness. Kamins showed that this decrease in resistivity is due mainly to the increase of mobility. Because an APCVD polysilicon film with thickness larger than several micrometers is composed of a few layers of grains stacked in the thickness direction, the measured mobility is actually an average mobility over the film thickness. The mobility near the top surface is larger in a thicker film because the grain size becomes larger. Mei *et al.* (5) studied the resistivities of APCVD polysilicon films which had thickness down to 0.25 μm and were doped by phosphorus ion implantation with a concentration of 1.2×10^{19} cm^{-3}. The resistivity also decreases with increasing film thickness. It was reasoned that this resistivity increase is due mainly to dopant segregation to the interface between polysilicon film and its underlying oxide layer. Recently, Colinge *et al.* (6) proposed a theoretical equation [Eq. [5] in (6)] for the mobility in polysilicon films, which considers the effect of film thickness by including the polysilicon/oxide interface scattering mechanism. They used 1.95 μm as the mean free path of electrons in silicon, which implies that if a polysilicon film thickness is reduced to the range of 1.95 μm, the effect due to collisions of electrons to the polysilicon/oxide interface can become a dominant factor to cause the resistivity increase.

The above review shows that the effect of film thickness on the electrical properties of LPCVD polysilicon films at different doping concentrations has not been fully understood and that, in fact, different viewpoints exist on the dominant mechanism for the resistivity changes as the film thickness decreases. In this work, therefore, we first characterized the electrical properties of boron-doped LPCVD polysilicon films which had thickness ranging from 1.2 down to 0.1 μm and doping concentration ranging from 1×10^{17} to 1×10^{19} cm^{-3}. It will be shown that as the film thickness decreases, the resistivity increases exponentially, rather than remaining constant as in conventional resistor materials, and the rate of increase is a strong function of doping concentration. There are several possible physical mechanisms to cause this increase, such as polysilicon/oxide interface scattering, dopant segregation to the grain boundaries, dopant leaching or loss, dopant segregation to the polysilicon/oxide interface, and changes of the number of carriers trapped into grain boundaries because of grain-size variations. A detailed quantitative analysis will show that the dominant mechanism causing the resistivity increase is the carrier trapping effect due to grain-size reduction.

Experimental Results

Sample preparation and measurements.—Undoped polysilicon films 0.1-1.2 μm thick were deposited onto 0.80 μm thick SiO_2 layers thermally grown on silicon wafers. The deposition was done in an LPCVD reactor at 620°C by H_2 ambient pyrolysis of silane with a deposition rate of 80 Å/min. The implanted boron doses were selected to give calculated doping concentrations at three different levels: 1×10^{17}, 2×10^{18}, and 1×10^{19} cm^{-3}. The calculations assumed a uniform dopant profile and no dopant loss. The implantation energies were selected to yield a maximum implantation dose near the center of the polysilicon films. After the devices were patterned by plasma etching, a 0.80 μm-thick CVD oxide layer was deposited at 430°C. Contact windows were opened, and the wafers were divided into two groups. One group had the contact windows implanted heavily with boron to give p^+

contacts; the other group did not have this implantation. All the wafers were then annealed at 900°C for 420 min in N_2 to remove the implantation damage and to ensure uniform dopant distribution. A 1.0 μm-thick aluminum layer was deposited and defined over the contact areas. The contacts were alloyed at 450°C for 20 min in N_2. The devices included different shapes of resistors, van der Pauw structures (8), and cross-bridge structures (8).

The thickness of polysilicon film was measured by an α-step profiler. The grain structure and grain size were studied using transmission electron microscopy (TEM) techniques. Figure 1 shows the typical cross-sectional TEM micrographs. It was found that all the grain structures of undoped and doped samples were conical, and no significant recrystallization was observed, in contrast to the reported grain growth in phosphorus-doped samples in Ref. (9). From thin to thick polysilicon films, the surface roughness becomes worse, and the grain size at the top of the surface, which corresponds approximately to the distance between the hillocks (9), increases. A quantitative measurement of the grain size was performed using top-viewed TEM micrographs shown in Fig. 2. Two methods were used, and the results agreed well. One method was to measure the area of a certain region and to count the number of grains within that area. The average grain size L is calculated from the following equation

$$L = (\text{area/number of grains})^{0.5}/m \quad [1]$$

where m is the micrograph magnification factor. The other method (10) was to draw a line and to count the number of grains across the line. The average grain size is

$$L = (\text{line length/number of grains})/m \quad [2]$$

The measured grain size decreases as the film thickness decreases (Fig. 3).

By using the secondary ion mass spectroscopy (SIMS) technique (11), dopant profiles were proven uniform, and no significant dopant loss was observed. The SIMS analysis was done with a 12 keV O_2^+ beam raster scanned and gated to accept 20% of the central portion. Charging problems were minimized by using the electron flood gun and integration of the secondary ion energy distribution. We used a 50 keV boron implantation with dose of 5×10^{14} cm^{-2} as a standard. The measured doping concentrations were within 20% of the projected values. Figure 4 shows typical SIMS profiles of samples which have projected doping levels of 2×10^{18} cm^{-3} and thickness of either 0.2 or 1.0 μm.

Electrical measurements included the I-V characteristics, resistivity, and Hall voltages. Resistivity was always measured over the linear I-V range with small applied bias. Sheet resistances for some high-value resistors were difficult to obtain from the Hall setup and were calculated, therefore, from measured resistance and device geometry.

Results.—The measured sheet resistance *vs.* film thickness at room temperature is shown in Fig. 5a for a doping concentration of 1×10^{17} cm^{-3}, and in Fig. 5b for 2×10^{18} cm^{-3}. The contacts between aluminum and polysilicon in samples without p^+ contact dopants are ohmic at small applied voltage. Inclusion of the p^+ contact dopants does not significantly affect the sheet resistance. Figure 5a and 5b shows that when the film thickness decreases, the sheet resistance increases exponentially. The thickness dependance of the resistance is considerably larger at a doping concentration of 2×10^{18} cm^{-3} than at 1×10^{17} cm^{-3}. The resistivity, which can be calculated by multiplying the sheet resistance by the film thickness, is also

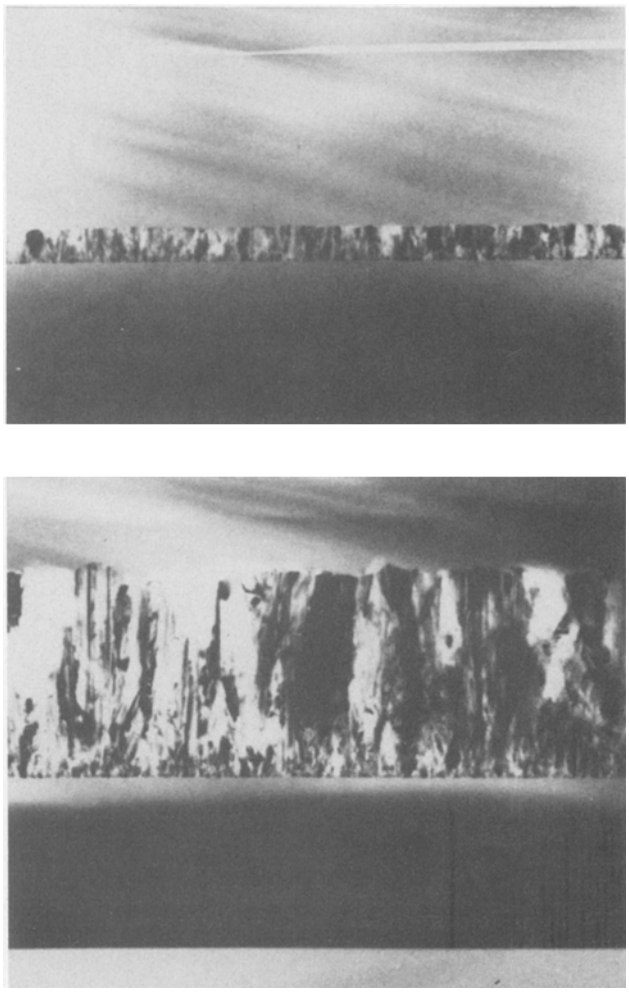


Fig. 1. Cross-sectional TEM micrographs. A, top: t = 1950Å, N = 1×10^{17} cm^{-3}. B, bottom: t = 9800Å, N = 2×10^{18} cm^{-3}. t = film thickness, N = doping concentration.

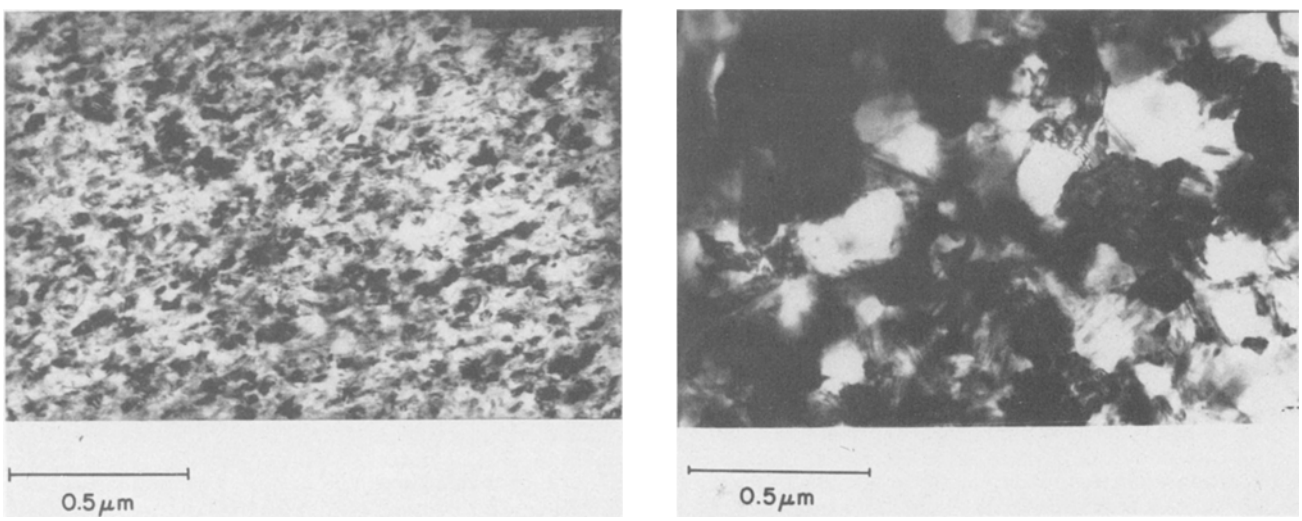


Fig. 2. Top view TEM micrographs of the samples in Fig. 1

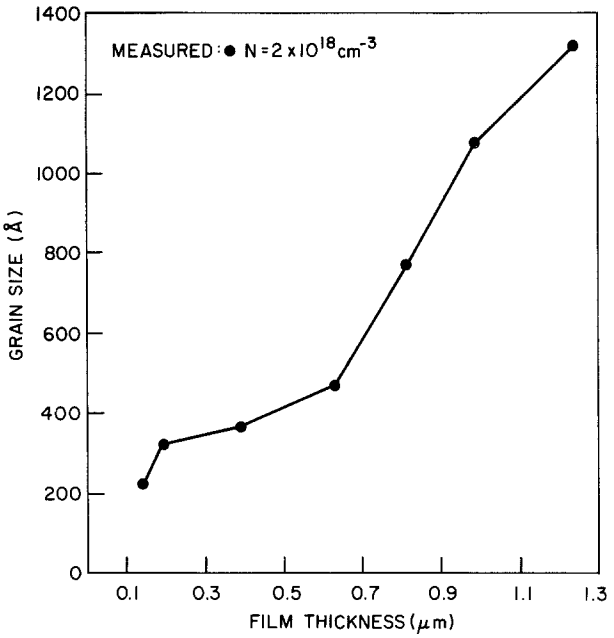


Fig. 3. Measured average grain size vs. film thickness

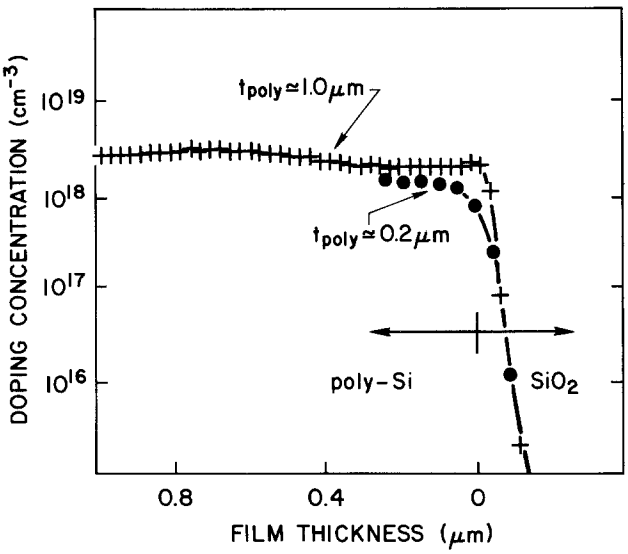
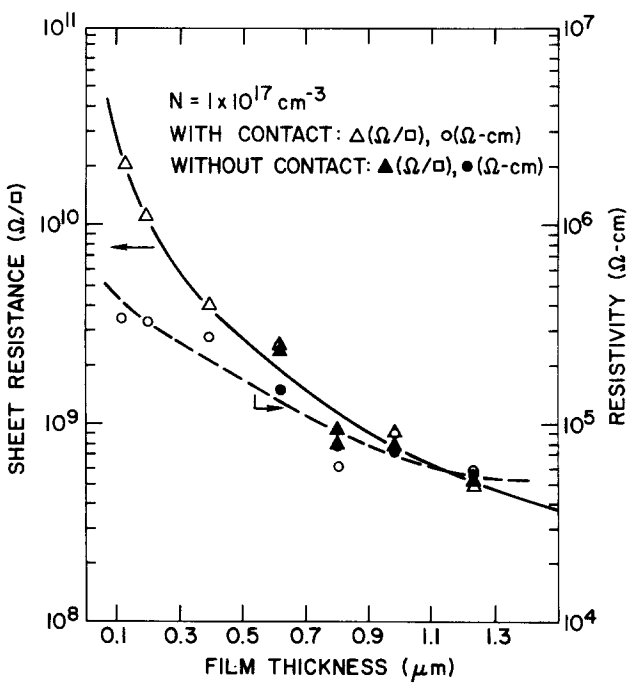


Fig. 4. Measured dopant profiles vs. film thickness

shown in Fig. 5a and 5b as a function of film thickness. A rapid increase of the resistivity with decreasing film thickness occurs, especially at thickness less than 0.8 μm. This behavior is different from ohmic resistors of other materials, the resistivity of which is generally independent of thickness.

Theoretical Interpretation

Two theories have been proposed to model the transport properties of doped-polysilicon films. The first is a dopant-segregation model, where the grain boundary serves as a sink to cause preferential segregation of dopant atoms that become inactive at the boundary (12, 13). This model, however, cannot explain the mobility minimum at a critical doping concentration, the temperature dependence of the resistivity, and the hyperbolic-sine I-V behavior of polysilicon resistors at high electric field. The second theory is a carrier trapping model (1, 2, 7, 14-16), where the trapping states inside the grain boundary, due to defects and incomplete atomic bondings, can trap free carriers from the ionized dopants. This process not only reduces the number of free carriers, but also creates a potential barrier surrounding the grain boundary, which impedes the motion of carriers from one crystallite to another. This model better explains the sharp changes of resistivity with doping concentration, the mobility minimum, the temperature dependence of resistivity, and the hyperbolic-sine I-V behavior at high



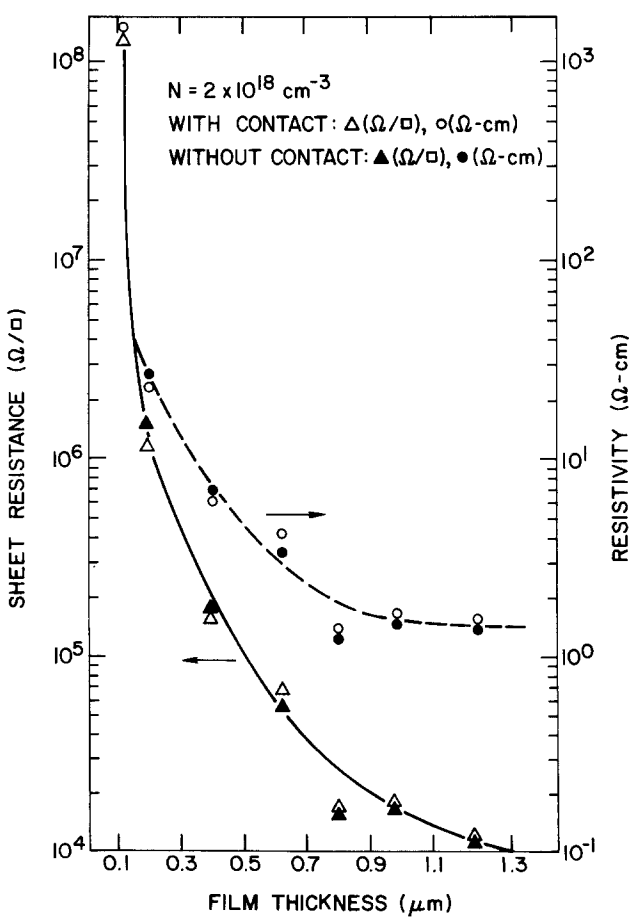


Fig. 5. Measured sheet resistance and resistivity vs. film thickness at room temperature. A, above: $N = 1 \times 10^{17}$ cm^{-3}. B, right: $N = 2 \times 10^{18}$ cm^{-3}.

electric field. Even if the dopants do segregate, the trapping model can still be applied, based on an active dopant concentration that can be obtained by subtracting the inactive dopant concentration from the actual doping concentration (15, 17).

For thin-film polysilicon resistors, several physical mechanisms may cause the observed resistivity increase when film thickness decreases. The effect of these mechanisms will be considered individually below.

Scatterings at horizontal grain boundaries and polysilicon/oxide interface.—TEM results on LPCVD films show that the grain structures in all samples having different film thicknesses are conical. In such conical structures, grain boundaries rarely occur in the direction parallel to the polysilicon/oxide interface, in contrast to the randomly stacked grain structures usually observed in APCVD polysilicon films. If the structure had many stacked layers of such horizontal grain boundaries, the resistances of the samples with p^+ contact dopants could not be the same as those without the contact dopants because the grain boundary is a high resistance region. However, it is found that the resistances of samples with p^+ contact dopants are approximately equal to those without p^+ contact dopants. This demonstrates that, even though horizontal grain boundaries may exist occasionally, they do not seriously disturb the current flow, and the possibility of carriers colliding with the horizontal grain boundaries is low. Since the mean free path of carriers in the intrinsic silicon is approximately 200Å,[1] which is much smaller than the thinnest film thickness in our samples, the carriers should have had several collisions before scattering at the polysilicon/oxide interface. As a result, the scattering effects due to both polysilicon/oxide interface and horizontal grain-boundaries should not be the dominant factor responsible for the resistivity increase (18) in LPCVD polysilicon films with thickness down to 0.1 μm. Another piece of indirect evidence to support the conclusion is that when the oxide layer above polysilicon film is removed, the measured resistance does not change too much from the resistance of samples with the top oxide layer present, and the rate of resistivity increase as the films become thinner is almost the same. In addition, that different rates of the resistivity increase at different doping concentrations is difficult to explain based on scattering effect.

Dopant segregation to grain boundaries.—Although the amount of dopant segregation to grain boundaries can be a function of film thickness, Mandurah *et al.* (19) showed that no significant segregation effect occurs in boron-doped polysilicon films. In our boron-doped samples, the grain-boundary segregation should not be the dominant factor for the resistivity increase.

Dopant leaching or loss.—After inplantation and before annealing, the samples were coated with a thin layer of low temperature deposited oxide to protect their surfaces from furnace ambient and to prevent loss of dopants during the high temperature process. The SIMS results (Fig. 4) proved that the actual doping concentration in the polysilicon film is close to the projected value within 20% variation, and no significant loss was found even in the thinnest samples.

Segregation to polysilicon/oxide interface.—From the SIMS results as shown in Fig. 4, no significant pileup of the dopants was found at the polysilicon/oxide interface in the samples with doping concentration up to 2×10^{18} cm^{-3}. It should be noted that an electron flood gun for charge compensation was employed. While not shown in Fig. 4, the silicon signal remained constant when sputtering through the Si/SiO_2 interface. It has been shown (20) that at normal incidence O_2^+ bombardment, silicon is completely oxidized to SiO_2. At a doping level of 1×10^{19} cm^{-3}, a small pileup of the dopants has been observed; however, its amount is not so significant as to affect the absolute doping level in the film. This effect can become important at higher doping concentration.

[1] The mean free path λ is $v_{th}(m^*\mu/q)$, where v_{th} is thermal velocity of the carriers, $v_{th} = (3kT/m^*)^{0.5}$, and μ is mobility. In intrinsic silicon, $\lambda \cong 237$Å for holes and $\cong 204$Å for electrons at room temperature. In a doped silicon crystallite, λ is even smaller. For example, $\lambda \cong 130$Å at a doping concentration of around 10^{20} cm^{-3}.

Carrier trapping.—Before a quantitative calculation of the carrier trapping effect on the resistivity change due to reduction of film thickness, general features of the carrier trapping model are briefly reviewed here. Several assumptions were made in the previous trapping models (2, 15) to simplify the calculation. The polysilicon film is assumed to be composed of identical crystallites having a grain size L, and the grain boundary is assumed to contain Q_T cm^{-2} of traps located at an energy level of e_T with respect to the intrinsic Fermi level at the grain boundary (Fig. 6). The traps are assumed to be initially neutral and become charged by trapping carriers. When dopants are added into polysilicon films, some of the mobile carriers around the grain boundary are trapped by the trapping states in the grain boundary, resulting in a depletion region. Using these assumptions, an abrupt depletion approximation was used to calculate the energy band in the crystallites. For a given grain size, since the effective trapping states in the grain boundary are finite, there exist two possible conditions, depending on the doping level. If the doping concentration is high, the crystallite can only be partially depleted and a neutral region remains (Fig. 6b). If the doping level is decreased to a critical doping concentration N^*, the crystallite is totally depleted (Fig. 6c). Because the crystallite becomes totally depleted, the number of free carriers remaining in the crystallite drastically decreases, thus causing a sharp resistivity increase. As the doping level further decreases, the crystallites remain in the condition of total depletion, and resistivity increases at a rather gradual rate. This explains why the resistivity *vs.* doping concentration curve of polysilicon films has a sharp change in slope near the critical doping level N^*. Similarly, at a given doping concentration, there exists a critical grain size L^* below which the grains are totally depleted. For a grain size around the value of L^*, as the grain goes from partial to total depletion, the resistivity change due to grain size variation is drastic.

As mentioned above, TEM results showed that when polysilicon film thickness is reduced, the grain size decreases. The effect of such grain-size change on the resistivity of polysilicon films will be examined based on the carrier trapping model below.

The previous trapping models (2, 14, 15) using the depletion approximation can clearly describe the transport

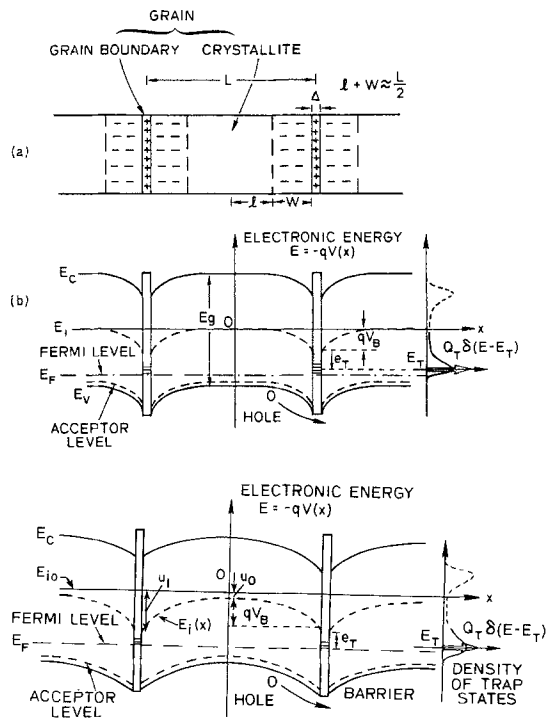


Fig. 6. The polysilicon trapping model. a: One-dimensional grain structure. b: Energy-band diagram of partially depleted grains for p-type dopants. c: Energy-band diagram of totally depleted grains for p-type dopants.

properties of polysilicon films. However, the depletion approximation causes abrupt changes in the resistivity with respect to grain-size variations near the transition between the partial depletion and the total depletion condition (21).[2] These abrupt changes can be smoothed by using a more accurate solution of Poisson's equation without assuming the depletion approximation (21). Recently, an exact solution for polysilicon resistivity was derived, which can avoid such abrupt changes and is valid over a wide range of doping concentrations, temperatures, and grain sizes (22). In this work, because samples are not very heavily doped and data were measured at room temperature, the exact Fermi-Dirac statistics of free-carrier distribution can be approximated by Boltzmann statistics, thus relaxing our exact analysis (22) to similar equations derived by Board and Darwish (21), except that a more precise formulation of the Fermi level should be used. By defining the intrinsic Fermi level in the bulk silicon E_{i_0} as zero energy and assuming the electron (hole) energy positive (negative) for upward and negative (positive) for downward direction (Fig. 6), the Fermi level is

$$E_F = kT \ln \left\{ \frac{1}{4} \exp (E_A/kT) \left[\sqrt{1 + 8(N_A/n_i) \exp (-E_A/kT)} - 1 \right] \right\} \quad [3]$$

where N_A is the doping concentration, n_i is the intrinsic carrier concentration, and impurity level E_A, is (15)

$$E_A = \left(\frac{1}{2} E_g - 0.08 + 4.3 \times 10^{-8} N_A^{1/3} \right) + E_i(0) \quad [4]$$

By solving Poisson's equation and using suitable boundary conditions (21), the relationship of intrinsic Fermi level at grain boundary $E_i(L/2)$ with respect to the intrinsic Fermi level at the center of grain $E_i(0)$ can be calculated from

$$\left(\frac{Q_T^+}{2L_D q N_A} \right)^2 = (u_1 - u_0) + \beta(e^{u_1} - e^{u_0}) + (e^{-u_1} - e^{-u_0}) \quad [5]$$

where $L_D = (2kT\epsilon/q^2N_A)^{0.5}$, $\beta = kT/q$, u_1 and u_0 are defined as $E_i(L/2)/kT$ and $E_i(0)/kT$, respectively, and the ionized trap density in the grain boundary Q_T^+ is related to the number of metallurgical traps Q_T as follows (2, 15)

$$Q_T^+ = \frac{Q_T}{1 + 2 \exp [u_1 + (e_T - E_F)/kT]} \quad [6]$$

where e_T is the trapping-state energy level with respect to the intrinsic Fermi level at the grain boundary. The corresponding grain size L is given by

$$L = L_D \int_{u_0}^{u_1} [(u - u_0) + \beta (e^u - e^{u_0}) + (e^{-u} - e^{-u_0})]^{-1/2} \, du \quad [7]$$

By varying u_0, therefore, the corresponding u_1 and L can be calculated using Eq. [5] and [7].[3] The resistivity is then obtained from (15)

$$\rho = \frac{(2\pi m^* kT)^{1/2}}{Lq^2 p(0)} \exp (qV_B/kT) \quad [8]$$

where $qV_B = kT (u_1 - u_0)$ and $p(0) = N_A \exp (-u_0)$. For simplicity, crystallite bulk resistivity is not included.

To compare theory to the experimental results, it is necessary to determine m^*, permittivity ϵ, n_i, E_g, L, Q_T, and e_T. The values of single-crystal silicon were used for the first five parameters (15) and L was measured from TEM micrographs (Fig. 3). Q_T and e_T were obtained experimentally from the ρ *vs.* $1/kT$ curves of polysilicon resistors by using similar procedures described in Ref. (15). The method is valid because the samples used for parameter extraction have doping concentrations away from N^*, and thus the depletion approximation is valid.

[2] This can be interpreted in terms of film thickness as follows: at a given doping concentration, when film thickness changes such that its grain size is close to L^*, the abrupt depletion approximation becomes invalid.

[3] The contents of Eq. [5], [6], and [7] are different from their corresponding expressions in Ref. (21) by including the necessary corrections.

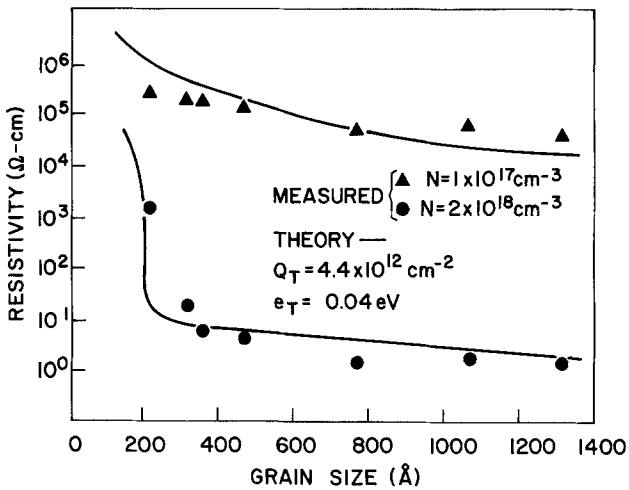


Fig. 7. Measured and theoretical resistivity *vs.* average grain size of different thickness films.

Also, since Q_T could be precisely determined, the value of e_T was adjusted within a reasonable degree to produce the best results of the ρ *vs.* L curves. Figure 7 shows the measured resistivities of different thickness films *vs.* the measured average grain sizes. The theoretical curves agree well with the experimental data and explain the drastic increase of resistivity with decreasing film thickness. Because decrease of film thickness causes reduction of grain size, when the grain size reaches around 210Å at doping concentration of 2×10^{18} cm^{-3}, most of the grains go from partial depletion into total depletion, and the number of free carriers available for conduction drastically decreases, thus causing a sharp increase of resistivity. In contrast, at doping concentration of 2×10^{17} cm^{-3} for the range of film thickness studied in this work, most of the grains have been totally depleted, and therefore, the changes of resistivity are not so drastic as in those samples with doping concentration of 2×10^{18} cm^{-3}. As a result, the carrier trapping effect due to grain-size variation at different film thicknesses is a dominant factor for the resistivity increase in boron-doped LPCVD polysilicon films as the film thickness decreases (≥1000Å).

Conclusions

The effect of film thickness on the electrical properties of boron-doped LPCVD polysilicon films has been studied down to film thickness of 0.1 μm. It has been found that the resistivity increases exponentially as the film thickness decreases, rather than remaining constant, and the increasing rate is a strong function of doping concentration. After a quantitative study of the physical mechanisms which may affect the resistivity as film thickness decreases, the carrier trapping effect due to grain-size variation at different film thicknesses was shown to be the dominant factor. A trapping model without assuming the depletion approximation can explain the experimental observations well and enhances understanding of the resistivity behavior as polysilicon film thickness decreases. It also shows that when the polysilicon films are employed in VLSI circuits, the sensitivity of the resistivity to the film thickness must be considered in the device design (23).

Acknowledgments

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Polycrystalline Silicon Recrystallization by Combined CW Laser and Furnace Heating

J. Shappir* and R. Adar

School of Applied Science and Technology, The Hebrew University of Jerusalem, Jerusalem, Israel

ABSTRACT

A modified CW argon laser-induced lateral recrystallization of polycrystalline silicon is described. Holding the sample in a furnace at elevated temperature of about 1000°C resulted in significantly reduced thermal gradients and stresses. A wider range of power is allowed for proper recrystallization both on oxide and substrate areas simultaneously. Preferred thermal profiles enabled larger lateral epitaxy of ~50 μm per single scan. The higher substrate temperature resulted also in wider melted areas and high scan rates of 80 cm/s enabling much shorter processing time.

In recent years, intensive effort has been made in different techniques to obtain large area silicon on insulator (SOI) as an alternative substrate for integrated circuits. Besides the obvious advantages of reduced junction capacitance, no device coupling, and no contact spiking, it can eventually lead to three-dimensional integration of electronic devices (1, 2). Gat *et al.* observed (3) that the recrystallization of polysilicon layers on an insulating substrate by a CW laser beam results in grains having dimensions up to $2 \times 25\ \mu m^2$.

In order to fabricate larger-area SOI structures without grain boundaries and with complete control of the crystallographic orientation, seeded lateral epitaxy technique has recently been studied (4, 5). In this technique, a region where the polysilicon is in direct contact with the silicon substrate serves as a seed for lateral crystal growth to the area where the polysilicon is over an insulating layer.

With standard isoplanar technology, lateral epitaxy of 20-30 μm was obtained. Modified coplanar structure with no step between the polysilicon on silicon (PS) and polysilicon on oxide (PO) or the utilization of thin underlying insulators (< 1500Å) resulted in further increase of the lateral epitaxy to 70-80 μm (5, 6).

In the standard laser recrystallization configurations, the silicon wafer is attached to a metal chuck that can be heated up to 700°C (6) and the laser beam raises the layer temperature to above its melting point of 1415°C. Such an arrangement suffers from two major drawbacks: (*i*) It is difficult to find optimal recrystallization conditions for both the PS and PO areas due to the difference in the vertical heat conduction in the two regions, and (*ii*) the high lateral thermal gradients are bound to reduce the crystalline quality of the recrystallized layer.

To overcome these two problems, the approach of this work was to raise the substrate temperature to about 1000°C by placing it in a diffusion furnace and use lower laser power to raise locally the polysilicon temperature to its melting point. In this setup, the wafer loses most heat by blackbody radiation rather than by thermal conductance to the metal chuck.

In the following, certain results of this combined laser and furnace recrystallization technique are reported.

Experimental

The experimental setup consisted of the laser, the optics, the scanners, and the furnace, where the wafer was held during the recrystallization process. The laser was a Coherent 18W Ar ion laser, operated in the multiline mode with wavelengths near 0.5 μm. The optical system consisted of two lenses in a beam expanding structure that served both as beam expander and focusing element to obtain an 80 μm diam spot size, at a focal distance of 700 mm. The beam was scanned across the wafer by means of two galvanometer-driven mirrors. The silicon wafer was vacuum held by an adjustable quartz tube which entered the furnace from its back side. The system also included a conventional metal vacuum chuck for comparison purposes. The experimental setup is illustrated schematically in Fig. 1.

The 0.5 μm-thick polycrystalline silicon layer was deposited on a standard isoplanar structure, obtained by local oxidation of the p-type <100> silicon substrate to 0.7 and 1.1 μm oxide thicknesses. As a stabilizing capping layer, use was made of CVD-deposited Si_3N_4 or thermally grown SiO_2 layers of various thicknesses. After the recrystallization step, the capping layers were removed and Secco etch (7) was used to reveal the grain boundaries.

Results

Effects of recrystallization at elevated substrate temperatures.—The main advantage of the recrystalliza-

*Electrochemical Society Active Member.

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