voltages of ±5V and an input signal range of ±2V (Fig. 4). A sinusoidal signal and its sampled output values, and the absolute error and variance, are given in Figs. 5 and 6, respectively. They show an estimated maximum absolute error of 89mV and a standard deviation of 50.5mV, i.e. SNR = 27dB.

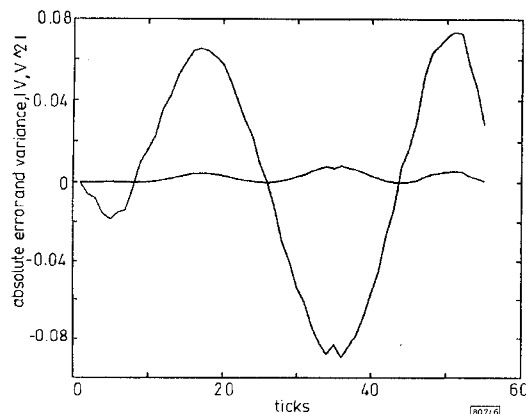

Fig. 6 *Absolute error and variance*

Conclusion: A CMOS snapshot sampling technique suitable for a variety of high speed data acquisition situations, such as the detection of high frequency transients, measurement systems, sonar, radar, or laser systems, etc, has been presented. It uses an optimised inverter chain for sample control and simple track-and-hold-circuits for highest speed and low current consumption. Simulations indicate a data acquisition time of 0.34ns, which represents a reduction of 71.7% compared to that obtainable using CMOS inverters, and a maximum absolute error of 89mV (SNR = 27dB) for a simple 0.8μm digital CMOS process. The maximum input signal frequency is limited to ~0.5–1GHz, according to high switch resistance for a sample capacitance of 300fF.

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Suppression of boron penetration by using inductive-coupling-nitrogen-plasma in stacked amorphous/polysilicon gate structure

Wen Luh Yang, Chiou-Jyi Lin, Tien Sheng Chao, Don-Gey Liu and Tan Fu Lei

Indexing terms: MOS integrated circuits, Plasma

A method is introduced for suppressing the penetration of boron for BF_2^+-implanted pMOS devices with a stacked amorphous/poly-Si (SAP) gate structure. It is shown that after inductive-coupling-nitrogen-plasma (ICNP) treatment, boron diffusion through the thin gate oxide is largely suppressed. As shown from the charge-to-breakdown measurements, the ICNP process will improve the quality of pMOS devices, with Q_{bd} three times higher than for the control samples.

Introduction: It has been proposed that the surface channel structure with a p^+-poly-Si gate implanted by BF_2^+ can be adopted to improve the charge control characteristics of pMOS devices in deep submicrometre CMOS applications [1]. However, it has also been found that the boron atoms tend to penetrate through the gate oxide. Consequently, surface-channel pMOS devices suffer several thermal stability problems, such as shifts in threshold voltage, distorted capacitance-voltage characteristics, and high voltage swing in the subthreshold region. Several techniques to improve this have been proposed which can be categorised into two approaches. First, a nitrogen layer can be introduced, as a diffusion barrier, which is piled up at the layer interfaces between the gate, oxide and substrate. This nitrogen barrier can be established by incorporating N_2O during the oxidation process [2]. Nitridising the oxide layer by several kinds of ambients was also investigated [3 – 5]. The second approach is to modify the gate layer structure with a stacked structure; boron atoms will easily segregate at each layer interface [6]. In this Letter, a novel low temperature process, termed ICNP treatment, is proposed to introduce nitrogen into the gate/oxide and oxide/Si interface with the advantages of a stacked gate structure. In this study, wafers are immersed in the nitrogen plasma created in an inductive-coupling chamber. Since there is no RF power connected to the substrate in the chamber, no DC bias will be exerted on the device surface. The effect of ion bombardment can be eliminated.

Experiments: In this study, MOS capacitors with a p^+-poly-Si gate were fabricated on the (100)-oriented n-type substrates. An 8nm thick thermal oxide layer was first grown in an ambient of dry oxygen at 900°C. After this stage, an amorphous silicon (a-Si) film is deposited on the wafers at a temperature of 550°C. The film thickness is designed to range from 10 to 30nm to investigate the suitable a-Si layer thickness in the SAP structure. These samples were then subjected to ICNP treatment with various process times. In this study, both the RF power and the N_2 flow rate were kept constant at 150W and 50sccm, respectively. The amount of N_2 introduced into the gate layer is expected to be affected only by the process time. A following poly-Si film was deposited at 620°C on the a-Si layer to make the total thickness of the gate layer up to be 300nm. All the wafers were thereafter implanted by BF_2^+ with a dosage of $5 \times 10^{15}cm^{-2}$ and an energy of 50keV. These samples were annealed under an ambient of dry oxygen at 900°C for 10, 20, and 50min that will drive boron into different depths.

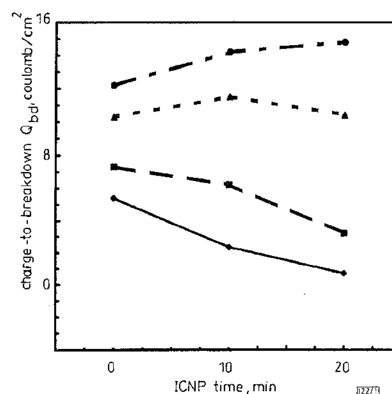

Fig. 1 *Charge-to-breakdown of MOS for various a-Si thicknesses against various ICNP plasma time after annealing at 900°C for 50min*

—◆— without a-Si
—■— a-Si, 10nm
—▲— a-Si, 20nm
—●— a-Si, 30nm

Fig. 1 shows the obtained charge-to-breakdown Q_{bd} values of each MOS capacitor against ICNP process time with the annealing condition at 900°C for 50min. Results of the samples with various a-Si thicknesses are shown together for comparison. Seeing the samples without ICNP treatment, i.e. the results at time = 0 in Fig. 1, it is found that Q_{bd} increases from 5.4C/cm^2 to 12.2C/cm^2 as the thickness of the a-Si layer increases. It seems that the diffusion path of boron becomes longer as the a-Si layer is thickened. This fact indicates that boron will segregate at the interface of poly-Si and a-Si, such that the diffusion of boron is retarded. With a thicker a-Si layer, the degradation in the oxide layer by the

boron is less significant, even though the total gate thickness of each sample is the same. Studying the effect of the ICNP process time on the purely poly-Si gate layer, i.e. 'without a-Si' curve in Fig. 1, the Q_{bd} curve falls away as the process time increases. It is believed that the energetic nitrogen plasma still induces evident damage in the oxide layer, even without a DC bias. In this case, the Q_{bd} value will decrease from 5.4C/cm^2 down to only 0.8C/cm^2 after 20min of ICNP processing. Nevertheless, this negative effect can be diminished in those samples with the stacked gate structure. Seeing the relationship between Q_{bd} and ICNP process time for the samples with an a-Si stacked gate in Fig. 1, the quality of the oxide layer can be improved by using a gate with a thicker a-Si layer. As shown in Fig. 1, the samples with only 10nm thick a-Si will still suffer evident degradation in the oxide layer as the ICNP process continues. Nevertheless, the Q_{bd} value has been improved, compared to the control sample. According to the results obtained in Fig. 1, the effects of a-Si thickness and the ICNP process duration can be explained as below. By increasing the thickness of the a-Si film, the damaging effect is reduced, hence the sample can then endure a longer processing time. In this study, it is expected that the amount of nitrogen introduced into the gate/oxide interface will be higher by using a long-duration ICNP process to suppress boron diffusion. Therefore, the passivation of nitrogen and the damaging effect of the plasma will compete during the ICNP treatment. When the a-Si layer becomes sufficiently thick, degradation by energetic plasma will be overcome and the nitrogen passivation will then dominate. For the samples with a 20nm a-Si layer, the optimum process time is 10min. The best Q_{bd} we obtained here was 15C/cm^2, which is three times higher than that of the control sample with a pure poly-Si gate and without ICNP treatment.

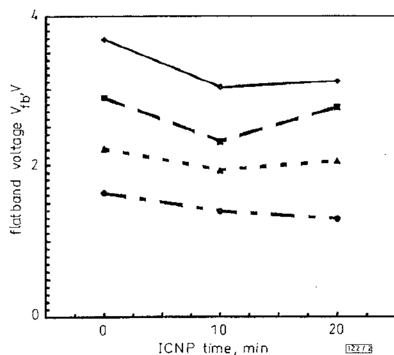

Fig. 2 *Flat band voltage of MOS for various a-Si thicknesses against various ICNP plasma times after annealing at 900°C for 50min*

—◆— without a-Si
—■— a-Si, 10nm
—▲— a-Si, 20nm
—●— a-Si, 30nm

Fig. 2 shows the relationship between the flat-band voltage and the ICNP process time. In general, the ICNP treatment will reduce the flat-band voltage for each sample. This fact means that ICNP can effectively suppress the effect of boron penetration. However, seeing the curve for the pure poly-Si gated samples, this passivation effect will fade out as the ICNP process time increases up to 20min. This degradation may also be attributed to the damaging effect of the plasma, as mentioned above. As seen in Fig. 2, it is consistent with the results found in Fig. 1 that the stacked structure can be used to resist the damaging effect of energetic plasma. For those samples with an a-Si thickness >20nm, the damage caused is insignificant.

Two sets of SIMS profiles, with and without ICNP treatment, are shown in Fig. 3 for comparison. In this case, there are two peaks in the nitrogen concentration, located at the poly-Si/oxide and oxide/Si interfaces. Comparing the profiles of boron in Fig. 3, it is found that the concentration of boron decreases more sharply in the substrate for the sample undergoing the ICNP treatment. The large increased amount of piled nitrogen in the gate/oxide and oxide/Si interface after the ICNP process implies that the reduction of boron penetration is strongly related to the population of nitrogen.

In conclusion, the suppression of boron penetration in the stacked poly-Si/a-Si gate structure by inductive-coupling-nitrogen-plasma is demonstrated. This novel approach provides a very small shift in the flat-band voltage and a large breakdown charge for *p*MOS devices. Better characteristics can be achieved by selecting the SAP structure with a 30nm a-Si layer undergoing the ICNP treatment.

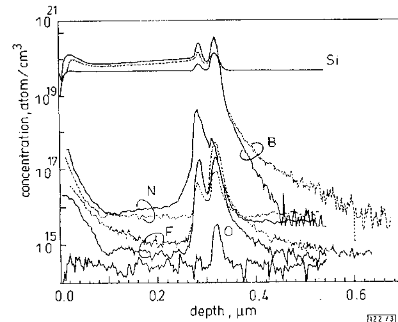

Fig. 3 *Nitrogen and boron profiles of ICNP sample and control sample analysed by SIMS*

——— ICNP
– – – – No ICNP

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Integrated concave grating WDM demultiplexer with 0.144 nm channel spacing

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Indexing terms: Integrated optics, Grating demultiplexers, Wavelength division multiplexing

A 60-channel WDM demultiplexer based on a concave grating with 0.144nm channel spacing in the 1.5µm wavelength region was fabricated. The demultiplexer comprises SiO_2/SiON/SiO_2 waveguides on Si and an individual channel has a full width at half maximum spectral width of 0.09nm.