# 國 立 交 通 大 學

## 平面顯示技術碩士學位學程

## 碩 士 論 文

運算放大器電路之整合式階層模擬應用

An Implementation of Integrated Hierarchical Synthesis in Op-Amp Circuits

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中華民國一百零二年二月

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# 運算放大器電路之整合式階層模擬應用

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## 摘　　要

此篇論文旨將階層式自動合成架構之設計應用於金屬氧化層場效應電晶體運算放大器(CMOS Op-Amp)中。此階層式設計由二階段組合而成 - 由下而上的探索和由上而下的優化處理。前段步驟主要是經由元件契合(device fitting)的過程求得元件及電路的參數對應關係，再經由效能探索(performance exploration)的過程將元件與電路效能做一個描述性的轉換，藉此找出參考電路的效能極限；後段步驟在於從已搜尋到的電路效能集合中選擇出最適者來導出構成元件各項參數的最佳模擬解。然而，由於在先進製程裡的參數變異將會造成 device fitting 的不準確，此由上而下的優化步驟所得之局部區域的最佳結果會經 retargeting 來做修正。基於 Op-Amp 參考電路，此篇加強不同電路模型架構的應用，並另其極有效地找出每個範例電路模型的效能。

An Implementation of Integrated Hierarchical Synthesis in Op-Amp Circuits

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## ABSTRACT

In this thesis, hierarchical design is employed to the automatic synthesis framework applied to the CMOS Op-Amp circuit. This hierarchical framework is consisted of two stages: a bottom-up searching and top-down optimizing. In the bottom-up way, technology device information is transformed into circuit performance domain by device fitting and performance exploration. Then, the appropriate performance among the performance space we have searched is chosen to target the optimal simulation result via our top-down flow. However, the uncertainty of device fitting is damaging on advanced technologies' deviation. This top-down flow will also revise the local optima via retargeting. Based on [1], we further enhance this framework on different circuit model, and methods used to find out maximum efficiency of each circuit model will be more efficient.

# 誌　　謝

98 年的早秋，懷著懵懂的思緒踏進這片學問之海，拎著所內助理雅玲親切的叮嚀，叩起一扇扇知識淵博的實驗之門，尋找心目中理想的研究之路。從沒敢想，也不知修得多少的福氣，能遇見 仁傑前輩殷勤的指點與引薦，得以認識日後無微不至栽培我的老師。國軒前輩與豆子學長的不厭其煩和其通透的思維，時時刻刻點醒我學習的盲點。融洽的氛圍裏，人來人往的長姊弟妹們也一直都是平日生活上不可或缺的學習伴侶。在這人生萬般的起承轉合中，有些事是永遠不會忘記的，尤是我對這裏的想念。

# Contents

# List of Figures

# List of Tables

# Chapter 1

# Introduction

In accordance with different aspects of applications, the development of modern circuit has been gradually moving towards multi-functional integrated design. The complexity and area of the circuit also increased along with the functional improvement. In order to enhance the portability, performance and design timeliness of circuits, the technology of automated computer-aided optimization design has been widely discussed [2, 3, 4, 5]. Such design can be divided into two major approaches. One is to complete the entire calculation process by integrating circuit simulation software, and the other is to establish analysis expressions in place of the simulation software. The latter expression of circuit design is in the form of a polynomial for geometric programming. It could be regarded as a solution to the convex optimization problem. The latter has also improved the implementation efficiency because there is no need to perform overall circuit simulation for the combination of each design variable that is within a specified range. Although the optimization result of the former is relatively accurate, it will require too much runtime if the operating range becomes too large. The hierarchical algorithm is thus created in order to achieve the balance between time and accuracy.

This hierarchical analog synthesis has been proposed by Meng et al. for the design of radio frequency differential amplifier (RFDA) [1]. This thesis is about the application of another Op-Amp circuit. There are three critical differences between this

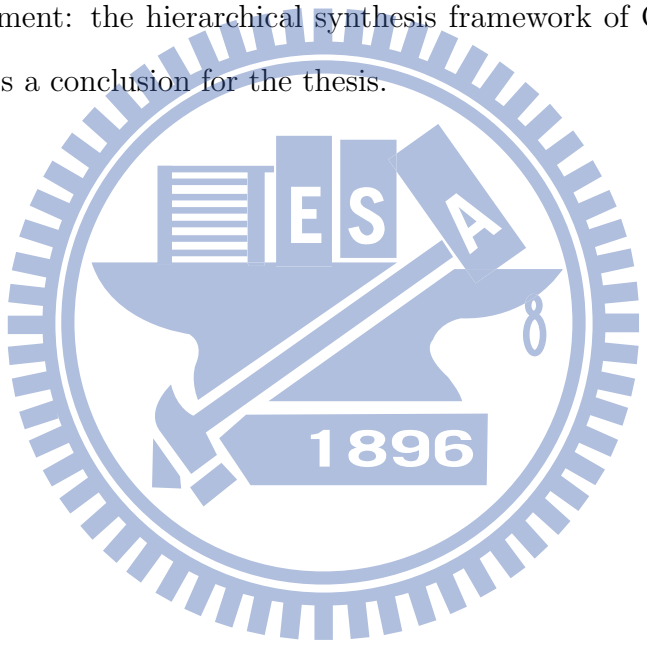
application and RFDA: the first is that the design structure has included a larger variety of considerations with respect to active components; the second is that the framework design has included the description of coexistence of components both in series and in parallel; and the last one is to consider the parameter variation of active components, such as the threshold voltage and the mobility. In the process of circuit optimization, first the mapping table between device and circuit parameters will be obtained by circuit simulation software. The correlation coefficients will be extracted by a device fitting approach, and then they will be combined into the circuit framework with geometric programming achieved in convex form, and then circuit optimization will be achieved in order to obtain the global optimal solution.

The overall processing time will be affected by the number of device-fitting samples. In order to shorten the processing time while keeping the accuracy, proper screening will be applied to samples. For the lightweight feature of circuit design, there should be more samples with small sizes in order to achieve accuracy optimization. However, from the perspective of practicality, there are usually process defects in devices of small sizes. The narrow device width may lead to narrow width effect causing roll-off of threshold voltage, and shorter device length may lead to punch through and malfunction of device. If the manufacturer has provided the mapping table between relevant process impact and the dimension of original piece in model reference, the improper samples should be moderately removed in order to avoid wasting simulation time.

Different processes will need to repeat the design processes. If the required design is applied to a different technology, this means that the circuit must be redesigned. This often entails a lot of time and introduces more of the human factor errors. To reduce the design complexity, the synthesis' main body will be the same for different technologies, and the circuit fitting coefficients and specifications are flexible to modify in order to achieve sizing optimization. This indicates that if the technology

has been changed, there is a need to reset the system coefficients and adjust the performance specifications. Based on this simplified amendment procedure, we can efficiently optimize the circuit components dimension in each technology. In this case, the hierarchical design in practical applications could reach global optimization, and the performance is sensitive to the coefficients of the device.

The rest of this thesis is organized as follows. Chapter 2 draws the manner of the hierarchical synthesis procedure; Sections 2.1 to 2.4 depict the details of each synthesis process under the four steps. Chapters 3 and 4 present a practical example for the experiment: the hierarchical synthesis framework of Op-Amp. Finally, Chapter 5 presents a conclusion for the thesis.



# Chapter 2

# Framework of Synthesis

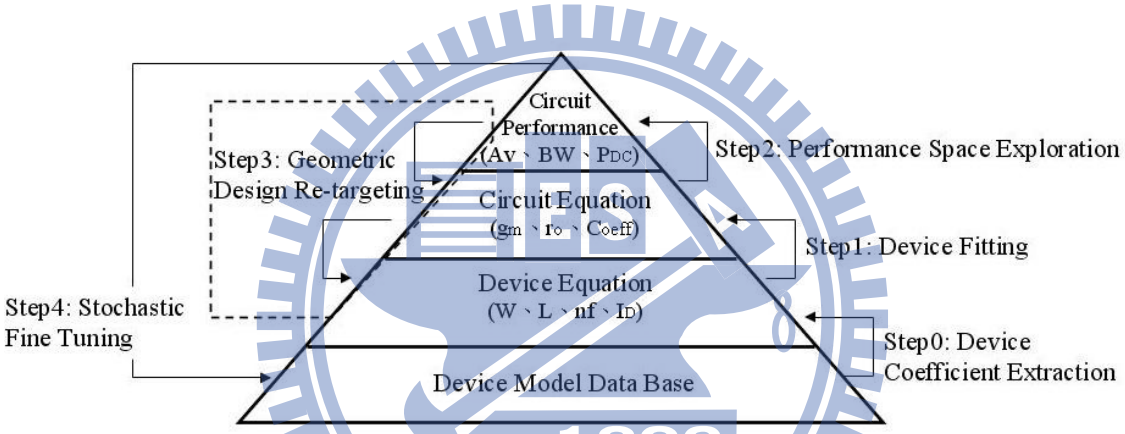



Figure 2.1: The overall structure of Op-Amp synthesis process.

The automatically synthesized framework employed in an analog circuit is demonstrated in this chapter. The prototype of the design flow is shown in Figure 2.1. The synthesis process is divided into two main phases to achieve the optimization, the global search, and the local search. These two phases have their own advantage to guarantee the quality of the optimal solution and the efficiency.

The first phase is the global search. It aimed at the description of actual circuit behavior, the characteristics of each device, and the specification for the expected performance. This process for the prediction of circuit ability could be regarded as an optimization problem, expressed to a convex form of geometric programming [6, 7]. This application for the optimization geometric programming has been widely

used for the analog circuit design [8, 9, 10, 11]. The comparison between the optimization approaches of this convex method and of others [12, 13, 14] shows that the former deals with solving the problem much more reliably and efficiently. It handles large quantity of design variables and constraints. In addition, it executes the optimization process in polynomial time and guarantees the solution to be truly global.

The second phase is the local search, which is a type of reconstruction of circuit using the simulators of an analog circuit. It makes up the offset of the initial guess taken from the previous optimization phase, which is caused by the incomplete formulated design defects. Furthermore, it could adjust the shortcoming of the design, thereby achieving the actual optimum solution. In addition, it works efficiently by starting from the corresponding initial optimum value. On the whole, the optimization work was done through the two phases to achieve a globally optimized solution of the circuit as the initial guess values and then employed the localization fine-tune operation to obtain a reliable synthesis result.

In simple terms, the design sequence of this hierarchical synthesis framework is run under four steps. Step 1 is device fitting, which is an extraction process between the model and the device coefficients of the design equation. Step 2, performance space exploration, and step 3, geometric design retargeting, involve a convex optimization searching of the circuit parameters to satisfy the sets of expectant specification. Step 4, stochastic fine-tuning, is a self-confirm function for the optimum result from the previous steps by localized searching. For instance, in this thesis, steps 1 to 3 accomplish the construction of circuit equations and the global optimization searching of the initial values, while step 4 causes the results to be closer to the actual value by localized searching.

This thesis is focused on step 2, which is divided into two parts: comparing the performance response under different conditions of process technology or foundry

and understanding the difference of the results in foundry and technology.

## 2.1 Device Fitting

The first step aims to create a set of equivalent mathematics equation describing each small-signal device parameter by a simulated electronic-feature database. A foundry provides a model to generate the database, which consists of some sets of mapping between the small-signal parameters and the design variables of a single device. Small-signal parameters include transconductance ($g_m$) and drain conductance ($g_d$), while design variables include effective channel length ($L$), width ($W$), and even the number of fingers ($nf$). The model simulates the characteristics of the device in different types and temperatures under a range of device dimensions. The simulation depends on the partial characteristics acquired from the sample testing of the manufactured products. The range is limited by the largest and the smallest element length and width of the product. The different models provide different types of mapping. Device fitting aims to extract the mapping relationship from the geometry-level design variables to the circuit-level parameters of a required device. The parameters of each device are described as a function as a combination of design variables:

$f_{(X_1,\ldots,X_m)} = \sum_{i=1}^{n}(c_i {X_{1i}}^{a_{1i}} {X_{2i}}^{a_{2i}} \cdots {X_{mi}}^{a_{mi}})$

$f_{(X_1,\ldots,X_m)}$ is the device parameters.

$c_n$ is the constant coefficient of the device parameters.

$a_m$ is the fitting coefficient of design variables.

$X_m$ is the design variables.

The equations above could be transferred into posynomial form by taking logarithm. It could be reformed as follows: $g_{(X_1,\ldots,X_m)} = \sum_{i=1}^{n}(\overline{c}_i + \overline{a}_{1i}\overline{X}_{1i} + \overline{a}_{2i}\overline{X}_{2i} + \ldots + \overline{a}_{mi}\overline{X}_{mi})$

$\overline{c}_i = log(c_i),\ i = 1, \ldots, n$

$\overline{a}_j = log(a_j),\ j = 1, \ldots, m$

$\overline{X}_j = log(X_j),\ j = 1, \ldots, m$

It could be further regarded as a type of geometric program and could form a lean-square error problem to minimize errors such as symbolic analysis or curve fitting [15, 16, 17, 18, 19, 20]. The final form of this fitting process is as follows:

$$\begin{aligned} &Define: \\ &\quad D = \textstyle\sum_{i=1}^{m}\ d_i \\ &\quad C = \textstyle\sum_{i=1}^{n}(\overline{c}_i + \overline{a}_i\overline{X}_{ji}),\ j = 1, \ldots, m \end{aligned} \tag{2.1}$$

$$minimize \quad ||D - C||^2 \tag{2.2}$$

The function of C is the circuit-level design variables

The function of D is the device-level design variables

Another critical concern is device characteristics as the applications of a device are not ideal. The device may suffer from the impact of parasitic effects. For instance, the parasitic capacitors will result in low bandwidth, leakage of alternating current, and more power losses. The phenomenon could be formulated as follows to feed the actual benefits:

$$\begin{aligned} &Define: \\ &\quad D = \textstyle\sum_{i=1}^{m}\ d_i \\ &\quad Peff = \textstyle\sum_{i=1}^{n}(\overline{c}_i + \overline{a}_i\overline{Y}_{ki}),\ k = 1, \ldots, m \end{aligned} \tag{2.3}$$

$$minimize \quad ||D - Peff||^2 \tag{2.4}$$

The function of Peff is the circuit-level parasitic effects of the device.

$c_i$ is the fitting parameters of function D.

## 2.2 Performance Space Exploration

In this step, the overall circuit behavior is expressed, combined with the characteristics of the device, in which the fitting coefficients are obtained from the previous step; this allows the device to achieve the performance specification. This exploration process could be regarded as a solution to the convex optimization problem. This solution is truly global because of the convex search form. This convex form is a special type of geometric programming; hence, it could be handled by interior point methods [21], even if the function is non-linear. This also allows for a more efficient search operation. Considering the form of the geometric program (in convex form), the equation is constructed through a change in variable and transformation of the objective and constraint function, as follows:

$$
\begin{aligned}
&Define: \\
&\quad D = d_i,\ i = 1, \ldots, p \\
&\quad Peff = e_j,\ j = 1, \ldots, q \\
&\quad C = f_j,\ j = 1, \ldots, r \\
&\quad Per = \{g_k,\ k = 1, \ldots, s\}_{l,l=1,\ldots,t} \\
&\quad e_j = h^{C_{om}}(D) \\
&\quad f_j = h_2^{C_{om}}(D) \\
&minimize \quad f_0(D, C, Per) \\
&subject\ to
\end{aligned}
\tag{2.5}
$$

$$
\begin{aligned}
&d_{i_{min}} \leq d_i \leq d_{i_{max}} \\
&f_{j_{min}} \leq f_j \leq f_{j_{max}} \\
&g_{k_{min}} \leq g_k \leq g_{k_{max}}
\end{aligned}
\tag{2.6}
$$

Per is the performance metrics

$e_j$ is the mapping equations from D to Peff

$f_j$ is the mapping equations from D to C

$g_k$ is the design equations from C to Per

The objective and subjectivity must be confined to the posynomial functions.

A set of performance specifications is regarded as the criteria for the determination of the limits of system performance. It is given to serve as constraints, together

with the objective. Circuit performance includes gain, frequency bandwidth, and power consumption.

## 2.3 Geometric Design Re-targeting

The third step is a reverse design project for verifying the integrity of the optimization system constructed from the previous steps. Designers could find a number of feasible specifications, which will be carried into the optimization system as the constrains, by observing the performance space. The circuit performance covers for the new constraints in order to extract the new circuit parameters and device variables. The result must be close to each other if the circuit behavior is expressed completely.

In theory, this step could directly determine the retargeted value of the device parameters from the performance specifications. This process is divided into two sub-steps to accomplish the work: circuit-level geometric design retargeting and device-level geometric design retargeting. It is anticipated that this will reduce the unexpected effective factors during the retargeting process if we verify the value of the device parameters but ignore that of the circuit.

The goal of the first sub-step is to find the optimal value of the circuit parameters from the given feasible specifications under the previously established optimization system. The problem could be formulated as follows:

$$
\begin{aligned}
&Define: \\
&\qquad D = d_i,\ i = 1, \ldots, p \\
&\qquad Peff = e_j,\ j = 1, \ldots, q \\
&\qquad C = f_j,\ j = 1, \ldots, r \\
&\qquad Per = g_k,\ k = 1, \ldots, s \\
&\qquad e_j = h^{C_{om}}(D) \\
&\qquad f_j = h_2^{C_{om}}(D) \\
&minimize \quad f_0(D, C, Per) \\
&subject\ to \\
&\qquad f_{j_{min}} \leq f_j \leq f_{j_{max}} \\
&\qquad g_{k_{min}} \leq g_k \leq g_{k_{max}}
\end{aligned}
\tag{2.7}
\tag{2.8}
$$

One of the given specifications for the performance metrics, $g_{k_{min}}$ and $g_{k_{max}}$, and the specifications, $f_{j_{min}}$ and $f_{j_{max}}$ are the constraints for the subject function, except the specification of the device variables.

The optimal circuit parameters obtained from the previous step are carried into the second sub-step to find the optimal values of the device variables. This process could be formed as follows:

$$
\begin{aligned}
&Define: \\
&\qquad D = d_i,\ i = 1, \ldots, p \\
&\qquad Peff = e_j,\ j = 1, \ldots, q \\
&\qquad C = f_j,\ j = 1, \ldots, r \\
&\qquad e_j = h^{C_{om}}(D) \\
&\qquad f_j = h_2^{C_{om}}(D) \\
&minimize \quad f(D, Peff) \\
&subject\ to \\
&\qquad d_{i_{min}} \leq d_i \leq d_{i_{max}} \\
&\qquad f_j \approx f_j{}^*
\end{aligned}
\tag{2.9}
\tag{2.10}
$$

$d_{i_{min}}$ and $d_{i_{max}}$ are the specification of device variables.

$f_j{}^*$ is the optimal value of circuit parameter, gained from previous step.

The relevant characteristics of the circuit, such as the product of area and the total power consumption, will be described to the object function, related to the device's variables and parasitic effects.

## 2.4 Stochastic Fine Tuning

In the final step, the generally optimal value of the device parameters obtained from the previous synthesis process is placed in the simulator as the initial guess. The model is provided by the manufacturer to carry out the actual circuit simulation. Some of the initial guess values could not reach actual optimization due to some design defects. The designers could go back to step 3 to fine-tune the design conditions according to the simulated differences of performance between the initial and the actual optimal results.

# Chapter 3

# Our Implementation on Op-Amp Synthesis

A representative design of a differential Op Amp is shown in Figure 3.1. In such case, we prefer the single-end double-cascade topologies to achieve high gain and obtain reasonable output swings. There are two types of active component on this circuit: native ($M_3, M_4, M_5, M_6$) and positive ($M_1, M_2, M_7, M_8, M_9, M_{10}$) metal-oxide semiconductor field effect transistors (MOSFET). The coefficients of the device parameter are extracted from the two model types in step 1, device fitting. In order to simulate the characteristics of device connection, the constraints of swing voltage and current flow are increased in the framework. The cascade current sources ($M_7, M_8, M_9$ and $M_{10}$) suppress the channel-length modulation effect, which is independent of the device $V_t$ and temperature. It will provide mirror current $1/2I_D$ on each side of the circuit if $(W/L)_9/(W/L)_{10} = (W/L)_7/(W/L)_8$. Voltages $V_{B_1}, V_{B_2}$ are generated by the current mirror techniques.

Three models of manufacturing technology are involved in the thesis: UMC 90 nm, UMC 65 nm, and TSMC 90 nm mixed-signal CMOS. The variation of these technologies, such as the mobility of electron and hole ($\mu_N, \mu_P$) and the capacity of gate-oxide $C_{ox_N}, C_{ox_P}$ are also factors of the design equations. The design procedure and software packages using this optimization problem are as follows [1]. The hier-

archical synthesis in this optimization case is divided into three main steps: device fitting, performance space exploration, and geometric design retargeting.

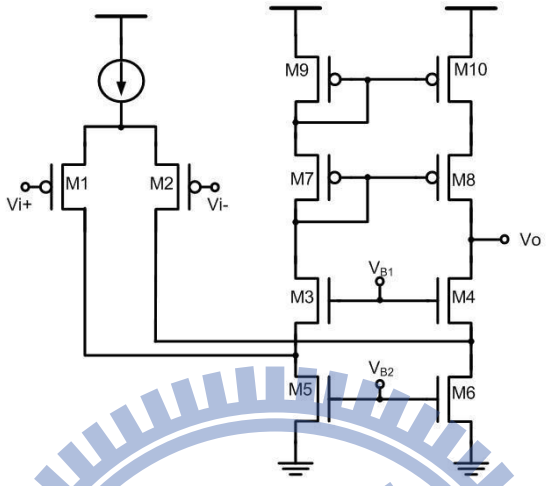



Figure 3.1: An overview of differential operation amplifier construction.

The process starts with device fitting, which involves obtaining the fitting coefficients of the device parameters. The model generates the database for mapping between the device design variables and the parameters within manufacturable ranges. The relationship of the device variables and the parameters could be formulated as a least-square error problem in coefficient fitting system as follows:

$$\begin{aligned} &\textit{minimize} && \| \, g_m - f(W, L, nf, I_D) \, \|^2 \\ &\textit{minimize} && \| \, g_o - f(W, L, nf) \, \|^2 \\ &\textit{subject to} && \\ & && W \geq W_{min} \, , \quad W \leq W_{max} \\ & && L \geq L_{min} \, , \quad L \leq L_{max} \\ & && nf \geq nf_{min} \, , \quad nf \leq nf_{max} \\ & && I_D \geq I_{D_{min}} \, , \quad I_D \leq I_{D_{max}} \end{aligned} \tag{3.1}$$

where $g_m$ is the transconductance of the device-level design parameter and $g_o$ is the reverse of the output resistance of the device-level design parameter.

Based on the coefficients obtained from the approaching of each device-level design

parameter in the previous step, the circuit performance ($A_v$, BW, phase margin (PM), direct current power ($P_{DC}$) and output power ($P_{out}$)) consists of circuit-level design parameters expressed for the function of device-level design parameters. A reasonable range of each circuit performance is shown in a matrix, searching from the matrix to find the optimal solution of the circuit. The performance-space exploration in this case can be formulated as follows:

$$
\begin{aligned}
&Define: \\
&\quad A_v = \frac{g_{m_1} \cdot g_{m_4} \cdot g_{m_8}}{g_{m_8} \cdot g_{o_4} \cdot g_{o_6} + g_{m_4} \cdot g_{o_8} \cdot g_{o_{10}}} \\
&\quad P_{out} = (V_{o_{max}} - V_{o_{min}})^2 \cdot g_o \\
&\quad P_{DC} = 3 \cdot V_{DD} \cdot I_{DP_{M_8}} \\
&\quad \omega_{3_{dB}} = \frac{g_o}{C_o}, g_o = \frac{g_{m_2} \cdot g_{m_5}}{g_{m_2} \cdot g_{o_4} \cdot g_{o_5} + g_{m_5} \cdot g_{o_2} \cdot g_{o_3}} \\
&\quad PM = \frac{pi}{2} - \sum_{i=1}^{2} \arctan(\frac{\omega_{UGB}}{\omega_i}) \\
&minimize \quad \sum(W_i \cdot nf_i \cdot L_i \cdot I_{D_i}) \\
&subject\ to \\
&\quad A_{v_i} \geq A_{v_{spec_i}}, \quad \omega_{3_{dB_i}} \geq \omega_{3_{dB_{spec_i}}} \\
&\quad P_{out_i} \geq P_{out_{spec_i}}, \quad P_{DC_i} \leq P_{DC_{spec_i}} \\
&\quad V_{ov_i} \geq V_{ov_{i_{min}}}, \quad V_{ov_i} \leq V_{ov_{i_{max}}} \\
&\quad A_v \geq A_{v_{min}}, \quad A_v \leq A_{v_{max}} \\
&\quad \omega_{3_{dB}} \geq \omega_{3_{dB_{min}}}, \quad \omega_{3_{dB}} \leq \omega_{3_{dB_{max}}} \\
&\quad P_{out} \geq P_{out_{min}}, \quad P_{out} \leq P_{out_{max}} \\
&\quad P_{DC} \geq P_{DC_{min}}, \quad P_{DC} \leq P_{DC_{max}} \\
&\quad PM \geq PM_{min} \\
&\quad W \geq W_{min}, \quad W \leq W_{max} \\
&\quad L \geq L_{min}, \quad L \leq L_{max} \\
&\quad nf \geq nf_{min}, \quad nf \leq nf_{max} \\
&\quad I_D \geq I_{D_{min}}, \quad I_D \leq I_{D_{max}}
\end{aligned}
\tag{3.2}
$$

$P_{DC}$ is the DC power consumption

$P_{out}$ is the output power

$A_v$ is the voltage gain

$PM$ is defined in terms of the phase of the transfer function at the unity-gain bandwidth

$\omega_{3_{dB}}$ is the cut-off frequency

$\omega_{UGB}$ is the unit-gain bandwidth frequency, can be expressed as $\frac{g_{m_1}}{C_o}$

$\omega_i$ is the non-dominant pole frequency. The second and third pole ($\omega_1$ and $\omega_2$) can be expressed as follows:

$\omega_1 = \frac{g_{m7}}{C_a}, C_a = C_{db_{M_7}} + C_{gs_{M_7}} + \frac{g_{m7}}{g_{o7}} \cdot (C_{gs_{M_8}} + C_{gd_{M_8}})$

$\omega_2 = \frac{g_{m6}}{C_b}, C_b = C_{db_{M_2}} + C_{dg_{M_2}} + C_{db_{M_6}} + C_{dg_{M_6}} + C_{sg_{M_4}} + \frac{g_{m6}}{g_{o6}} \cdot (C_{sb_{M_4}})$

$g_o$ is the output reverse impedance

$C_o$ is the output capacitance

$C_a$ is the capacitance at the gate of $M_7$

$C_b$ is the capacitance at the drain of $M_6$

$W_i$ is the width of the transistor

$nf_i$ is the number of fingers of the transistor

$L_i$ is the length of the transistor

$I_{D_i}$ is the drain current of the transistor

A set of each performance specifications - $[A_{v_{min}}, A_{v_{max}}]_j$, $[\omega_{3_{dB_{min}}}, \omega_{3_{dBmax}}]_j$, $[PM_{min}, PM_{max}]_j$, $[P_{out_{min}}, P_{out_{max}}]_j$, $[P_{DC_{min}}, P_{DC_{max}}]_j$, j = 1, . . . , n - on the performance metrics is considered the constraints for the optimization problem, given the objective function. The objective function in (3.2) is to minimize the overall circuit area and power consumption.

In order to ensure that each transistor is working in the saturation region, the overdrive voltage $V_{ov}$ is defined in a limited range. The lowest boundary of $V_{ov}$ is $V_{ov} \geq 0$, and the highest on each transistor is shown as follows:

$$
\begin{aligned}
V_{ov_{M_1}} &\leq V_{ref} + V_{t_{ref}} - V_{t_{M_1}} - V_{i+} \\
V_{ov_{M_2}} &\leq V_{ref} + V_{t_{ref}} - V_{t_{M_2}} - V_{i-} \\
V_{ov_{M_3}} &\leq V_{B_1} + V_{t_{M_5}} - V_{B_2} - V_{t_{M_3}} \\
V_{ov_{M_4}} &\leq V_{B_1} + V_{t_{M_6}} - V_{B_2} - V_{t_{M_4}} \\
V_{ov_{M_3}} + V_{ov_{M_5}} &\leq V_{B_1} - V_{t_{M_3}} \\
V_{ov_{M_4}} + V_{ov_{M_6}} &\leq V_{B_1} - V_{t_{M_4}} \\
V_{ov_{M_7}} + V_{ov_{M_9}} &\leq V_{DD} + V_{t_{M_3}} - V_{B_1} - V_{t_{M_7}} - V_{t_{M_9}} \\
V_{ov_{M_8}} + V_{ov_{M_{10}}} &\leq V_{DD} + V_{t_{M_4}} - V_{B_1} - V_{t_{M_8}} - V_{t_{M_{10}}} \\
V_{ov_{M_7}} &= V_{ov_{M_8}} \\
V_{ov_{M_9}} &= V_{ov_{M_{10}}}
\end{aligned}
\tag{3.3}
$$

$V_{ov_{M\star}}$ is the function of W, L, nf, $I_D$, mobility $\mu$ and oxide capacitor $C_{ox}$

Each $V_{ov}$ is the function of $W, L, nf$ and $I_D$, which could be expressed as follows:

$$
V_{ov_{M_n}}^2 = \frac{2 \cdot I_{D_{M_n}} \cdot L_{M_n}}{\mu M_n \cdot C_{ox_{M_n}} \cdot W_{M_n} \cdot nf_{M_n}}, n = 1, \cdots 10 \tag{3.4}
$$

The limit of the output swing is $V_{DD} - V_{GS_9} - V_{GS_7} + V_{t_{M8}}$. Inserting additional cascade devices in each branch will cause more gain but will further limit the output swing, which will make it more difficult to design each device working in the saturation region.

Geometric-design retargeting ensures that the optimization in the previous steps is effective. It is divided into two sub-steps. The goal of the first sub-step, which is called circuit-level geometric design retargeting, is to find the optimal values of the device $(g_m, g_o)$ from a given specification of performance metrics under the optimization problem used in the previous step. The problem formulation can be formed as follows:

$$
\begin{aligned}
&Define: \\
&\quad A_v = \frac{g_{m_1} \cdot g_{m_4} \cdot g_{m_8}}{g_{m_8} \cdot g_{o_4} \cdot g_{o_6} + g_{m_4} \cdot g_{o_8} \cdot g_{o_{10}}} \\
&\quad P_{out} = (Vo_{max} - Vo_{min})^2 \cdot g_o \\
&\quad P_{DC} = 3 \cdot V_{DD} \cdot IDP_{M_8} \\
&\quad \omega_{3_{dB}} = \frac{g_o}{C_o}, g_o = \frac{g_{m_2} \cdot g_{m_5}}{g_{m_2} \cdot g_{o_4} \cdot g_{o_5} + g_{m_5} \cdot g_{o_2} \cdot g_{o_3}} \\
&\quad PM = \frac{pi}{2} - \sum_{i=1}^{2} \arctan(\frac{\omega_{UGB}}{\omega_i}) \\
&minimize \quad \sum(W_i \cdot nf_i \cdot L_i \cdot I_{D_i}) \\
&subjectto \\
&\quad g_m \leq g_{m_{max}}\ , \qquad g_m \geq g_{m_{min}} \\
&\quad g_o \leq g_{o_{max}}\ , \qquad g_o \geq g_{o_{min}} \\
&\quad A_v \geq A_{v_{spec}}\ , \qquad \omega_{3_{dB}} \geq \omega_{3_{dB_{spec}}} \\
&\quad P_{out} \geq P_{out_{spec}}\ , \qquad P_{DC} \leq P_{DC_{spec}} \\
&\quad PM \geq PM_{min}
\end{aligned}
\tag{3.5}
$$

The second sub-step, which is called device-level geometric design retargeting, aims to find the optimal value of W, L, nf, and $I_D$ of each single transistor obtained in the circuit-level geometric design retargeting. The problem formulation can be generally written as follows:

$$
\begin{aligned}
&minimize \quad \sum(W_i \cdot nf_i \cdot L_i \cdot I_{D_i}) \\
&subjectto \\
&\quad g_{m_i} \approx g^*_{m_i}\ , \qquad g_{o_i} \approx g^*_{o_i} \\
&\quad W \geq W_{min}\ , \qquad W \leq W_{max} \\
&\quad L \geq L_{min}\ , \qquad L \leq L_{max} \\
&\quad nf \geq nf_{min}\ , \qquad nf \leq nf_{max} \\
&\quad I_D \geq I_{D_{min}}\ , \qquad I_D \leq I_{D_{max}}
\end{aligned}
\tag{3.6}
$$

$g^*_m$ is the optimal trans-conductance acquired from previous sub step.

$g^*_o$ is the optimal output resistance acquired from previous sub step.

# Chapter 4

# Experimental Results

The cases of Op-Amp synthesis using UMC 90 nm, TSMC 90 nm, and UMC 65 nm technology are shown in Figures 4.1, Figure. 4.2 and Figure. 4.3. The hardware used is Intel Xeon-E5160 processor, 3.0 GHz core speed with 32 GB RAM. Two trends were observed: the Op-Amp with higher gain or bandwidth improves the fan-out and induces more of the power consumption, and that the fan-out in U 65 advanced process is better than the others.

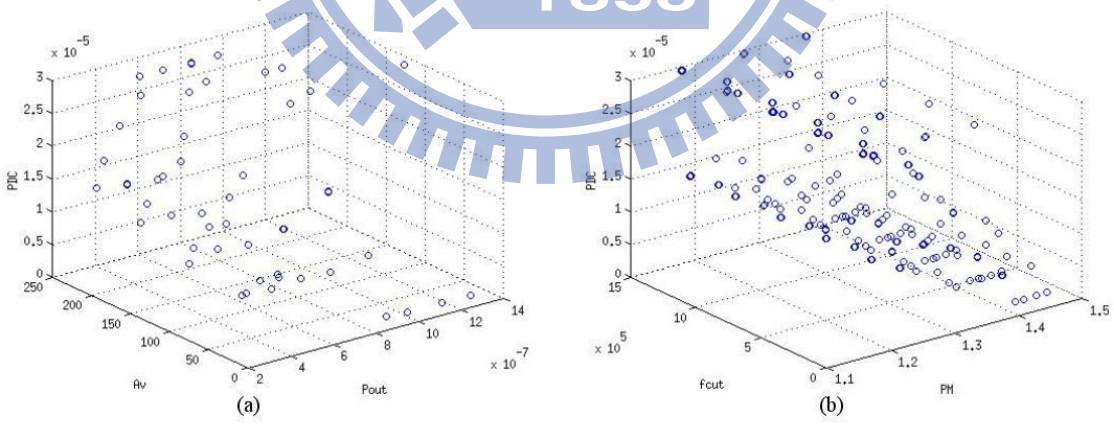



Figure 4.1: The performance space under UMC90nm technology.

The relationship between power consumption and gain response of the circuit on each technology is as shown in Figure 4.1 (a), 4.2 (c) and 4.3 (e), while the relationship between power consumption and frequency response is as shown in Figure

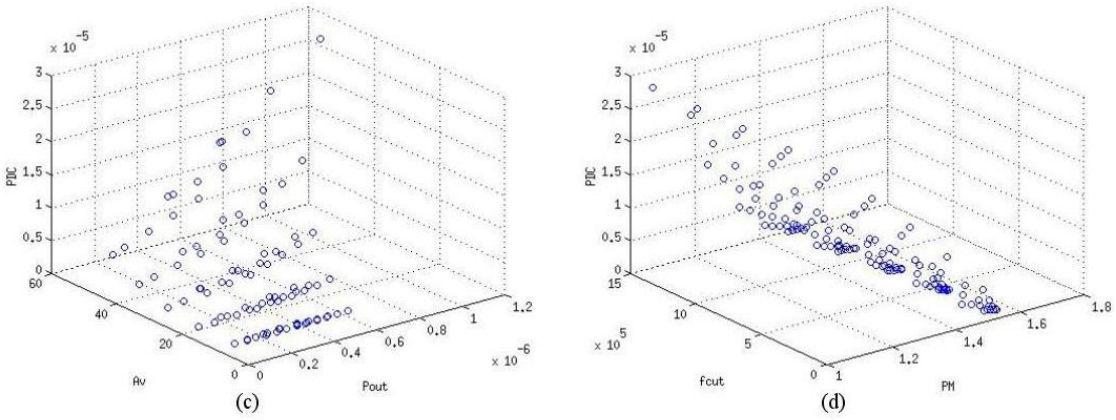



Figure 4.2: The performance space under TSMC90nm technology.

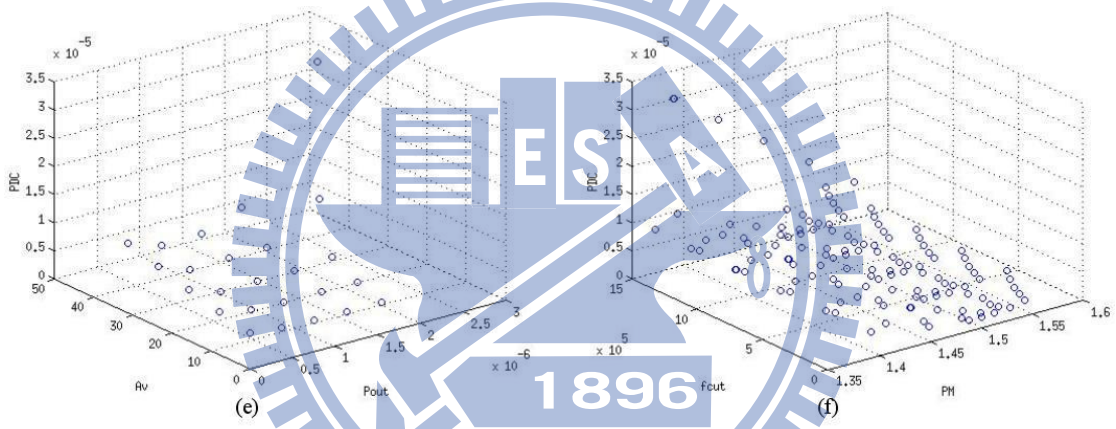



Figure 4.3: The performance space under UMC65nm technology.

4.1(b), 4.2 (d) and 4.3 (f). For the example of Figure 4.1, there are a total of 3125 points obtained from performance exploration in (a) and (b), while each point indicates a result of optimization. Due to the relationship of trade-off between gain and bandwidth, the set of regional points with relatively higher gain must be obtained from (a), and the set of regional points with relatively higher cut-off frequency must be obtained from (b) under same conditions of power consumption, output power and phase margin in order to figure out the most appropriate points in accordance with the judgement rules of low power consumption, high output power and high phase margin.

The mapping by different technologies for circuit performance exploration is shown

in Table 4.1. The coefficients extraction of device fitting parameters is shown in Tables 4.2-4.4, which simulation result is shown in Table 4.5. In Table 4.1, it shows that from the previous bottom-up design procedures, an optimization space of circuit performance can be calculated efficiently, but which is not correspondent with one calculated via the simulation method actually. Using the simulation method to find out optimal solutions will consume a lot of time. Therefore, Table 4.6 shows that as estimating a simulation optimal solution in this space of circuit performance via the top-down fine-tuning method, the time can be shortened. And the solution can also be as exact as the solution found out via the simulation method.

Table 4.1: SUMMARY OF STEP 2, MAPPING BETWEEN CIRCUIT PARAMETERS AND PERFORMANCE METRICS.

| Technology | UMC $90_{nm}$ CMOS | TSMC $90_{nm}$ CMOS | UMC $65_{nm}$ CMOS |
|---|---|---|---|
| $P_{DC}(mW)$ | $\leq 100$ | $\leq 100$ | $\leq 100$ |
| $P_{OUT}(uW)$ | $\leq 0.65$ | $\leq 0.095$ | $\leq 0.91$ |
| $A_V(dB)$ | $20 \sim 46.77$ | $20 \sim 34.15$ | $20 \sim 32.26$ |
| $BW(MHz)$ | $0.08 \sim 1.47$ | $0.08 \sim 1.47$ | $0.08 \sim 1.47$ |
| $PM(rad)$ | $0.5236 \sim 1.0472$ | $0.5236 \sim 1.0472$ | $0.5236 \sim 1.0472$ |

Table 4.2: DEVICE FITTING PARAMETERS ($g_m$)

| | UMC $90_{nm}$ | | TSMC $90_{nm}$ | | UMC $65_{nm}$ | |
|---|---|---|---|---|---|---|
| | NMOS | PMOS | NMOS | PMOS | NMOS | PMOS |
| $coeff.$ | 66.5443 | 21.13 | 62.9751 | 30.8794 | 4.8847 | 4.0834 |
| $W$ | 0.3922 | 0.4707 | 0.6369 | 0.6904 | 0.528 | 0.5255 |
| $L$ | 1.3E-8 | -6.93E-9 | 3.72E-9 | 4.16E-8 | 1.49E-8 | 4.42E-9 |
| $nf$ | -3.19E-8 | -3.19E-8 | 2.77E-10 | -1.35E-8 | -1.68E-8 | -9.05E-9 |
| $I_D$ | 0.5836 | 0.4985 | 0.3681 | 0.3156 | 0.2892 | 0.307 |

The comparison of the circuit performance in step 3, performance exploration, and step 4, stochastic fine-tuning, is shown in Table 4.6. The simulation result from the initial guesses is close to the value of fine-tuning. The performance of fine-tuning

Table 4.3: DEVICE FITTING PARAMETERS (*Resist.*)

| | UMC $90_{nm}$ | | TSMC $90_{nm}$ | | UMC $65_{nm}$ | |
|---|---|---|---|---|---|---|
| | NMOS | PMOS | NMOS | PMOS | NMOS | PMOS |
| $coeff.$ | 1.16E+7 | 1.05E+7 | 2.12E+10 | 1.06E+9 | 5.03E+7 | 4.36E+10 |
| $W$ | -0.91 | -0.991 | -0.9722 | -1.0277 | -0.547 | -0.6509 |
| $L$ | 1.1584 | 1.1852 | 1.7042 | 1.5191 | 0.9559 | 1.4046 |
| $nf$ | -0.0633 | 0.0144 | -0.9901 | -1.013 | -0.2674 | -0.2153 |

is better than that of the initial guesses. The experiments confirmed that each set of synthesis of performance space exploration could be accomplished within a few minutes, in the case of hundreds of variables and constraints.

The processing time of performance exploration and device fitting are shown as table 4.7. The samples of performance exploration for each technology are 3125 sets. For the model difference, such as the margin of device corner, the samples of device fitting are about thousands to ten thousand for each technology. On the other hand, more samples will enhance more accuracy of device fitting and require more runtime.

Table 4.4: DEVICE FITTING PARAMETERS ($Cap.$)

| | UMC $90_{nm}$ | | TSMC $90_{nm}$ | | UMC $65_{nm}$ | |
|---|---|---|---|---|---|---|
| | NMOS | PMOS | NMOS | PMOS | NMOS | PMOS |
| $C_{dg}$ | | | | | | |
| $coeff.$ | 0.028 | 0.029 | 0.2793 | 3.3299 | 0.0572 | 0.0057 |
| $W$ | 1.6656 | 1.6368 | 1.7193 | 1.8859 | 1.702 | 1.6185 |
| $L$ | 0.8449 | 0.8827 | 0.973 | 0.9865 | 0.856 | 0.783 |
| $nf$ | 0.0989 | 0.0839 | 1 | 1 | 0.0666 | 0.0886 |
| $C_{db}$ | | | | | | |
| $coeff.$ | 2.34E-6 | 2.0E-4 | 4.96E-16 | 7.09E-21 | 5.70E-10 | 1.21E-9 |
| $W$ | 0.6823 | 1.1019 | -0.518 | -1.2254 | 0.7149 | 0.6502 |
| $L$ | 1.1896 | 1.1089 | 1.0415 | 0.9895 | 0.5506 | 0.7253 |
| $nf$ | -0.0775 | -0.1971 | 1 | 1 | 0.2068 | 0.2127 |
| $C_{gs}$ | | | | | | |
| $coeff.$ | 0.2132 | 0.0867 | 8.2999 | 89.6328 | 2.5552 | 0.1064 |
| $W$ | 1.2859 | 1.2568 | 1.4586 | 1.6209 | 1.444 | 1.3075 |
| $L$ | 0.8978 | 0.8761 | 0.9956 | 0.9913 | 0.8871 | 0.815 |
| $nf$ | 0.0701 | 0.0983 | 1 | 1 | 0.0487 | 0.0765 |

Table 4.5: SIMULATOR RESULT.

| Technology | UMC $90_{nm}$ CMOS | TSMC $90_{nm}$ CMOS | UMC $65_{nm}$ CMOS |
|---|---|---|---|
| $A_V(dB)$ | 41.16 | 38.14 | 45.02 |
| $GBW(MHz)$ | 190 | 52.66 | 140.42 |
| $Phase$ | -119.8 | -95.3 | -106.4 |
| $PhaseMargin$ | 60.2 | 84.7 | 73.65 |

Table 4.6: PERFORMANCE COMPARISON TO STEP 3, PERFORMANCE EXPLORATION AND STEP 4, STOCHASTIC FINE-TUNING.

| | UMC $90_{nm}$ CMOS | | TSMC $90_{nm}$ CMOS | | UMC $65_{nm}$ CMOS | |
|---|---|---|---|---|---|---|
| | Exploration | Fine-Tuning | Exploration | Fine-Tuning | Exploration | Fine-Tuning |
| $P_{DC}(mW)$ | $\leq 100$ | 238 | $\leq 100$ | 218 | $\leq 100$ | 324 |
| $P_{OUT}(uW)$ | $\leq 0.65$ | 10.06 | $\leq 0.095$ | 0.45 | $\leq 0.91$ | 11.77 |
| $A_V(dB)$ | $20 \sim 46.77$ | 42.63 | $20 \sim 34.15$ | 46.01 | $20 \sim 32.26$ | 40.25 |
| $BW(MHz)$ | $0.08 \sim 1.47$ | 620 | $0.08 \sim 1.47$ | 591 | $0.08 \sim 1.47$ | 951 |

Table 4.7: PROCESSING TIME OF PERFORMANCE EXPLORATION AND DEVICE FITTING.

| | Unit | UMC $90_{nm}$ | TSMC $90_{nm}$ | UMC $65_{nm}$ |
|---|---|---|---|---|
| Performance Exploration | Hrs. | 3.65 | 3.66 | 3.75 |
| Device Fitting | Hrs. | 1.38 | 1.67 | 1.43 |

# Chapter 5

# Conclusion

In this thesis, the hierarchical synthesis methodology was applied in the Op Amp circuit design to achieve sizing optimization. Base on the simplified amendment procedure of framework for each different technology application, the good preliminary solution could be obtained from excellent execution efficiency.

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