Chapter 1

Introduction

1-1 Evolution of Lithography Technology

Optical lithography has become the driving force behind the miniaturization on integrated circuits (ICs), since the first metal-oxide-semiconductor-field-effect-transistor (MOSFET) was invented at Bell Laboratory in the early 1960s. In the past few decades, optical lithography has always managed with Moore's Law; however, it faces some challenges recently [1-2].

The minimum feature size of advanced ICs have been reduced by over 100X, from several microns in the early 1980s to around 20 nm today, with plan for sub-20 nm production at most major manufacturers. In order to keep path with the demand for printing smaller features, it is necessary to gradually reduce the wavelength of the light source. The reason can be described by the following equation:

$$Resolution = \frac{k_1 \lambda}{NA} \quad , \tag{1-1}$$

where k_1 is a constant, λ is the wavelength of the exposure light, and NA is the numerical aperture of the image system. The constant k_1 depends on the process being used. Commonly the value of k_1 ranges from 0.5 to 0.8, and the NA of lithography tools are about 0.5 to 0.6 today. Thus, the resolution can be expressed as about equal to the wavelength of the light to be used. Therefore, when the feature size shrinks, it must achieve better resolution on lithography system. In other words, the exposure light source needs shorter wavelength.

In the beginning, it used visible g-line (436 nm) and ultraviolet i-line (365 nm) as light sources which are produced by mercury arc lamp. After that, when ICs feature size

continually shrank beyond half a micron, the deep ultraviolet KrF (248 nm) and excimer laser ArF (193 nm) were introduced. Recently the advanced lithography technique is a combination of 193 nm immersion and double patterning even multi-patterning at 22 nm technology node. However the main lithography technique in the next generation has not been determined yet.

The following list three possible candidates which could be the next generation lithography techniques. They are nanoimprint, e-beam direct write (EBDW), and extremely ultraviolet lithography (EUVL).

Nanoimprint uses a molding and stamping process to replicate patterns on the wafer, as depicted in Fig.1-1. This method has now been included in the ITRS lithography roadmap 2011 [3]. The most competitive advantage of nanoimprint is that it is a relatively low cost method than EBDW and EUVL. Nevertheless, there are two primary difficulties in applying it to IC industry. The first is the fabrication of the mold. It is hard to fabricate 1X mold to accord critical dimension. The second problem is the defects on the mold. When the mold is used for many times, the remaining defects on the mold may influence the exposure.

EBDW is a kind of maskless lithography (ML2), as depicted in Fig.1-2 [4]. This method uses energetic electron beam to react with photoresist directly, and then create patterns on the wafer. It has high resolution as compared to optical lithography due to smaller wavelength of 10~50 keV electrons. Because of its very short wavelength and reasonable energy density characteristics, EBDW has the ability to expose pattern having nanometer feature sizes. EBDW eliminates some problems like mask cost and contamination. Nevertheless the major problem of EBDW is its much lower throughput rate. The average wafer throughput should be 200~300 wafers/hour, but the throughput of EBDW is far away from this requirement. If EBDW want to become a contender of

nanoimprint and EUVL, the target is to develop a moderate throughput and low cost EBDW tools or use multiple electron beams system.

Comparing to the above two methods, EUVL is also a promising technique, as depicted in Fig. 1-3 [1]. In many respects, EUVL may be viewed as a natural extension of optical lithography because it uses shorter wavelength light to carry out projection imagining. According to ITRS lithography roadmap 2011 [5], EUVL will be applied to IC's fabrication process at about 2014. Before that, it has already announced that IBM, AMD, and Toshiba had used the EUVL system produced by ASML to fabricate 22 nm devices successfully [6].

In summary, lithography defined critical dimensions will shrink with device scaling which enables higher speeds and larger density of transistors. Many important issues will meet challenges and should be considered such as light sources, resist processes, mask making, contamination controlling, resolution, accuracy, reliability, yield enhancements, and cost. The fundamental limitation of optical lithography is the trade-off between speed and resolution. For example, nanoimprint is a kind of contact printing, facing challenges like mask cost, mask damage and defect density. The throughput is an important issue for EBDW and the cost of investment is the major issue for EUVL.

1-2 Development of EUVL

Although EUVL is expected to be the main choice for the ICs product below the 20 nm node; still, it exists some challenges to be resolved [7-8]. The basic introduction and some predicaments of EUVL are illustrated in the following paragraphs.

The construction of EUVL was first proposed in 1988 by Hawryluke and Seppala at Lawrence Livermore National Laboratories [9], and the possibility of the method and

multilayer optics were inspected at NIT LSI Laboratories in the following years [10]. Then it became a popular researchable topic and was explored and developed constantly until now.

The basic optical lithography sub-systems used in EUVL are also used today in optical projection lithography. However, the main difference between EUVL and UVL is the interaction between light and materials. EUV radiation is strongly absorbed in nearly all materials, even gases; that is, the EUVL system must be operated in a vacuum environment, and the image systems must be entirely reflective type.

EUV is also called soft X-ray. The range of wavelength is from 4 to 40 nm. Nowadays, it is commonly using 13.5 nm as the exposure light because it has the best reflectivity. In fact, the EUV reflectivity of individual material at near-normal incidence is very low. In order to achieve reasonable reflectivity at near-normal incidence, surface has to be coated with multilayer thin films (ML's), as known as the Bragg reflector. According to previous studies, the Molybdenum/Silicon (Mo/Si) double layers was selected by industry as the main EUV multilayer structure because it has the best reflectivity (about 70%) when the wavelength of exposure light is 13.4 nm [7]. The MLs reflector must consist of a high-electron-density material as absorber (Mo) and a low-electron-density as spacer (Si), and it can be deposited by magnetron sputter, as shown in Fig.1-4 [11]. Furthermore, how to reduce the defects in the MLs is also an important issue because it may cause perturbation when the light is in progress.

Numerous methods have been investigated to be the source of EUV radiation. There are three common methods to produce EUV radiation. They are laser-produced plasma (LPP), discharge-produced plasma (DPP), and synchrotron. The basic requirements for the EUV manufacturing tool are how to reliably provide sufficient power to yield wafer throughput and lower its cost. The synchrotron radiation is stable; however, the high-priced facilities and large space limit its to be a practical production

tool. DPP and LPP are the two main candidates for EUVL. The Dutch company, ASML has successfully devised DPP demo tool, and many companies used this machine to fabricate 45 nm test chip [6]. Besides, reducing the prime cost of EUVL source is ongoing continually.

Mask and photoresist (PR) development are quite important issues in the whole EUVL program. The EUVL mask is also reflective, not transmissive because of the radiation absorption. The mask often consists of a pattern absorber placed on top of a ML's reflector deposited on a sturdy and solid substrate such as Si substrate. In order to eliminate defect influence, a defect-free mask should be developed. The commonly ML's deposited by magnetron sputter have been found too high defect density for mask blanks. For example, in the 22 nm node, the defect dimension should be controlled at 18 nm on the mask. It is not an easy work to achieve. Moreover, the defect inspection and mask repair should be considered, too. PR selecting is also a challenging issue. Today's state-of-the-art PR is chemical amplified resist (CAR), which is widely used for 248 nm, and 193 nm optical lithography. The CAR has high sensitivity and resolution; nevertheless, the pattern collapse and line edge roughness (LER) do not meet the requirements of EUVL. So far, Poly Methyl Methacrylate (PMMA) is a better choice to replace CAR for EUVL [7].

Above all, although EUVL has so many problems to be resolved; still, it is a hopeful technology and most likely to be the next generation lithography technique. Perhaps someday EUVL will be used by industry. Subsequently, the radiation damage effect under IC's fabricating process is inevitable and should be considered carefully.

1-3 Radiation Damage Effect

The radiation damages have been gradually emphasized by people since 1962 due

to repair Telstar I communication satellite [12]. In the beginning, this subject mainly focused on the radiation sources from outer space such as cosmic rays and α particles. With the technology development, electronic devices have more and more opportunities to be exposed under various radiation environments. For example, high-energy physics, nuclear weapons, high-flying airplane, and synchrotron, even in IC manufacturing process such as ion implantation and plasma treatment are common radiation environments. EUV is also a radiation source. Its energy is even higher than those radiations generated by conventional IC processes. Therefore, as EUVL is used in IC's manufacturing process, the radiation damage due to EUV exposure should be evaluated carefully.

The mechanisms of radiation induced damages are depicted in Fig.1-5 [13]. Fig. 1-5 shows the band diagram for a p-substrate MOS capacitor with positive applied gate bias. As long as the energies of radiation are higher than the material's bandgap, the energy may generate electron hole pairs (e-h pairs) which are known as photoelectric effect. Immediately, after the e-h pairs are created, most of electrons will be rapidly drifted toward the gate electrode within picoseconds and holes will be drifted toward the Si/SiO_2 interface because of the electric field. A part of electrons may recombine with holes before they leave the oxide. Those holes which escape initial recombination will transport toward the Si/SiO_2 interface by hopping through localized states in the oxide. When the holes gradually approach the interface, some fraction will be trapped, forming positive oxide trapped charges. The hydrogen ions (atoms) can also be drifted (diffuse) to the interface at where they may react to form interface traps.

After irradiation, the increment of oxide trapped charges and interface trapped charges may change the electric characteristics of devices. These degradations such as threshold voltage (V_{th}) shift, off-state leakage current increasing, subthreshold swing degradation, and GIDL increasing may affect devices seriously [14]. Even worse, all of

these characteristics will change with time, so the designers have to make some trade-off on performance and work margin to ensure circuits will not malfunction.

To summarize, after irradiation, the dielectric is the most sensitive part in the device. The radiation damages on SiO_2 gate dielectric have been investigated by many previous works [14]. However, the effects on alternative dielectrics such as high-dielectric constant (high-k) dielectrics need to be investigated further. On the other hand, not only gate dielectric but also other parts of device may be affected by high energy radiation such as shallow trench isolation (STI), LOCOS isolation and SOI structure; hence, we should also consider it together [15].

1-4 High-k Dielectric and Metal Gate

1-4-1 From SiO_2 to High-k Material

Device scaling and performance promoting are trends with technology development. In order to improve the speed of devices, driving current should be raised. From the simple model for MOSFET, the driving current could be written as

$$I_D = \frac{W}{L}\mu C_{ox}(V_G - V_T - \frac{V_D}{2})V_D \quad , \tag{1-2}$$

where W is the channel length, L is the channel width, μ is the channel carrier mobility, C_{ox} is the capacitance density of gate underlying channel in the inverted state, V_G is the gate bias, and V_D is the drain bias. Then C_{ox} could be written as

$$C_{ox} = \frac{\kappa\varepsilon_0 A}{t_{ox}} \quad , \tag{1-3}$$

where κ is the relative dielectric constant, ε_0 is the permittivity of free space, A is the area of the capacitor, and t_{ox} is the thickness of oxide. According to eqs. 1-2 and 1-3, shrinking t_{ox} will increase C_{ox} and promote driving current; nevertheless, t_{ox} could not

be shrunk forever. The reason can be shown in Fig. 1-6 [16]. With the shrinkage of t_{ox}, the drain current increase and accompany rising gate leakage current. The increment of gate current is due to direct tunneling of carriers and may cause extra power consumption. For this reason, it should find another way to promote gate capacitance.

Increasing the permittivity of dielectric is another method to increase C_{ox}. Therefore, high-k materials were introduced. Although high-k materials can theoretically increase the C_{ox}, but there still exist some problems in the integration considerations because of its material properties.

First of all, selecting a gate dielectric with a higher permittivity than SiO_2 is clearly essential. Besides, the tunneling barrier should also be considered because the too low band offset may lead to unacceptable high leakage current. Second, the thermodynamic stability of dielectric film is also an important issue. When the high-k thin film is deposited, it will react with the silicon substrate to form an unwanted interfacial layer, and this interfacial layer may cause interfacial defects and mobility degradation. Hence the interface quality and engineering should be considered cautiously. In the meantime, such as film morphology, gate compatibility, process compatibility, and reliability are several key issues that the alternative gate dielectrics should be noticed.

In brief, in order to achieve small leakage current, quantum mechanics indicates the gate oxide must be sufficiently thick; subsequently high-k materials were introduced. However, choosing applicable high-k dielectric is not an easy work. Many previous studies suggested that Hf-based dielectric is a good candidate to replace SiO_2 because it has many advantages as mentioned above [17-18]. In fact, Hf-based dielectrics have already been used in the advanced MOSFET devices, and the devices in this thesis also use HfO_2 as gate dielectric.

1-4-2 Choice of Metal Gate

In order to avoid poly-Si-gate depletion effect, metal gate becomes a promising candidate once again for device under 45 nm technology nodes. Metal gate has some advantages, such as low resistivity, high transconductance, and improving mobility when high-k gate dielectric is used [19-21]. Similarly, metal selection is not an easy work, too. First, the metal must have appropriate work function value to get the desire V_{th} for both nMOS and pMOS devices. Second, the thermal stability during manufacturing process is also a problem. Commonly 1000℃/10 sec annealing is set as an important parameter to estimate thermal stability, and only few metals are able to satisfy this criteria. There are many promising metal gates have been proposed including element metals, metal nitrides, metal silicon nitrides, and binary metal alloys. In this thesis, TiN is chosen as the gate electrode in order to agree with HfO_2.

1-5 Reliability issues of High-k Dielectric

Currently, high-k materials, particularly Hf-based dielectric have been investigated as the main candidates for conventional SiO_2. However, how to make the lifetime of these materials equal to or better than SiO_2 is an important question. As compared with the conventional thermal SiO_2, high-k dielectric has a lot of intrinsic defects which can lead to undesired transport and the trapping-induced instabilities [22]. The following sub-sections describe two common reliability issues.

1-5-1 Threshold Voltage Instability

Threshold voltage instability, also called hysteresis phenomena is one of the leading challenges for high-k dielectrics. The hysteresis is a V_{th} shift due to a trapping of charge in the pre-existing traps without creation of additional traps. The origins of these intrinsic defects are attributed to interstitial oxygen atom and positively charged

oxygen vacancies [23-24]. The hysteresis mechanism can be easily depicted in Fig.1-7 [25]. Electron trapping and detrapping in the ‘’border traps” is the primary reason for the hysteresis. The term ‘’border trap” was first introduced by D. M. Fleetwood in 1994 [26-27]. It is a kind of near interfacial oxide trap that are able to exchange charge through tunneling with the silicon substrate with time when the measurement is in progress.

At applied different biases, the amount of electrons tunneling into the dielectric is different, and cause different V_{th} shifts. Besides, according to the previous literature, not only applied bias but also time, stack thickness, and temperature can also influence hysteresis [22]. For these reasons, how to maintain V_{th} stability becomes a challenge for the future integration of high-k dielectrics.

1-5-2 Positive Bias Temperature Instability

Bias temperature instability (BTI) on SiO_2 was known since the late 1960s. There were many studies and models to debate this degradation effect. Unfortunately, the high-k dielectric such as HfO_2 has more serious instability than SiO_2 for both nMOSFET and pMOSFET after a bias temperature stress [22, 28-31]. The reasons of this effect are not well understood yet, but it is now commonly admitted that under a constant voltage stress and a raised temperature, a build-up of charges created at interface or in the oxide layer lead to the degradation of MOSFET performances.

The comprehensive positive bias temperature instability (PBTI) mechanisms of HfO_2 nMOSFET are shown in Fig. 1-8. During the PBT stress, the defect density increases and electrons may tunnel into the dielectric through direct tunneling and be trapped in the dielectric. The V_{th} shift in PBTI is predominately attributed to the shallow trapped charge in the dielectric, and the possible explanation of temperature behavior can be illustrated by the U-traps model reported by Kang et al. [32].

All in all, the reliability issues of high-k materials are related to the interfacial layer as well as the high-k dielectrics layer. It can be improved by some methods and extensively research is ongoing. The destination of this thesis is to investigate the changes of reliability after EUV irradiation.

1-6 Motivation and Thesis Organization

The main purpose of this thesis is to investigate the influence of the device after EUV irradiation. In the P. H. Li and T. T. Su's theses [33-34], two conclusions have been made. First, the EUV radiation can cause more seriously impact on high-k dielectric than SiO_2. Second, the chemical oxide offers the better radiation hardness among the various interfacial engineering. We utilize the previous results and investigate the radiation damage effect further.

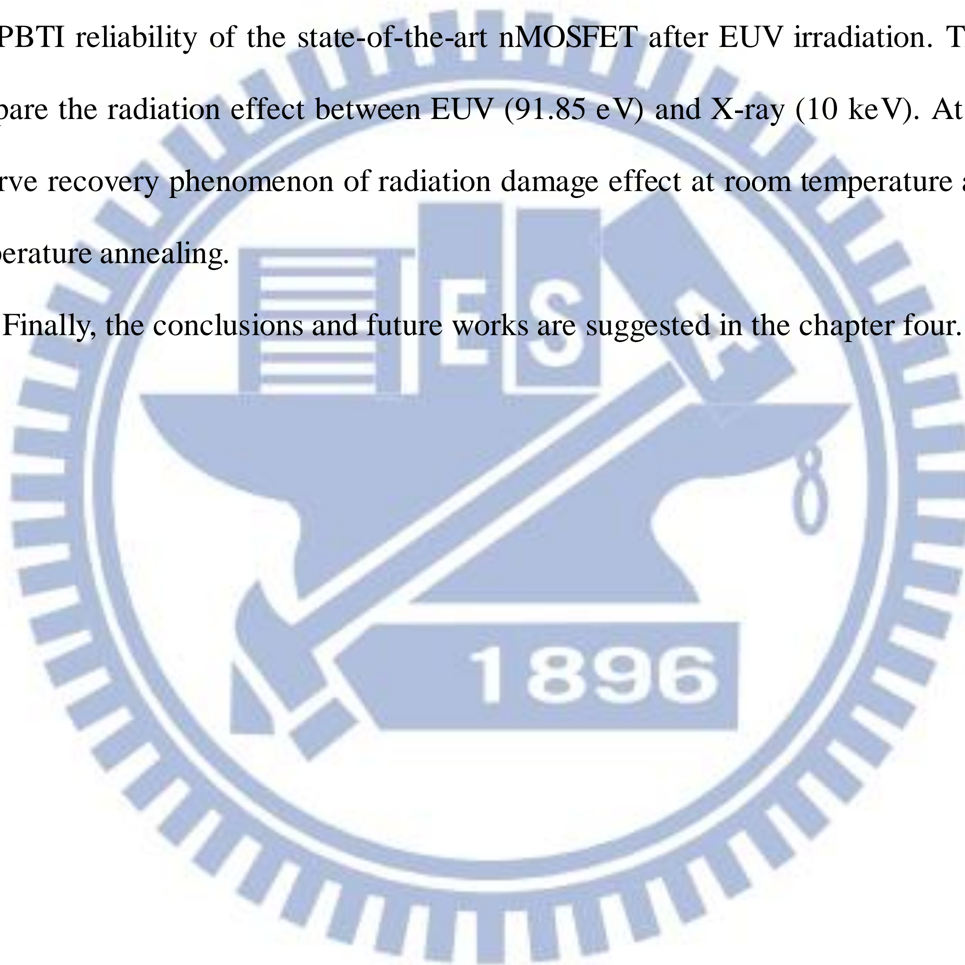
The motivation of the thesis involves four parts. At first, the gate dielectric's thickness continually decreases in order to get the higher C_{ox}. For this reason, we hope to investigate the EUV radiation effect among different dielectric's thickness, especially the ultrathin gate oxide. Second, we examine the performance and reliability of the state-of-the-art nMOSFET after EUV irradiation. Third, the recovery of the radiation damage effect has not been investigated entirely, and we hope to understand whether high temperature annealing can recover the radiation damage effect or not. At last, we investigate the radiation damage effect between the different radiation sources because of there are more and more opportunities to expose devices under various radiation conditions nowadays.

The first chapter is the introduction including the evolution of lithography, the development of EUVL, the essential of high-k dielectric and metal gate, and the reliability issues of high-k material.

The second chapter illustrates the fabricating process of the devices, the extraction methods of the parameters, and the experimental environment in the National Synchrotron Radiation Research Center (NSRRC).

The third chapter is the results and discussions. First, we compare the radiation damage effect among three different high-k dielectric thicknesses, 5 nm, 10 nm, and 15 nm, by using MIS capacitor structure. Second, we examine the electric characteristics and PBTI reliability of the state-of-the-art nMOSFET after EUV irradiation. Third, we compare the radiation effect between EUV (91.85 eV) and X-ray (10 keV). At last, we observe recovery phenomenon of radiation damage effect at room temperature and high temperature annealing.

Finally, the conclusions and future works are suggested in the chapter four.



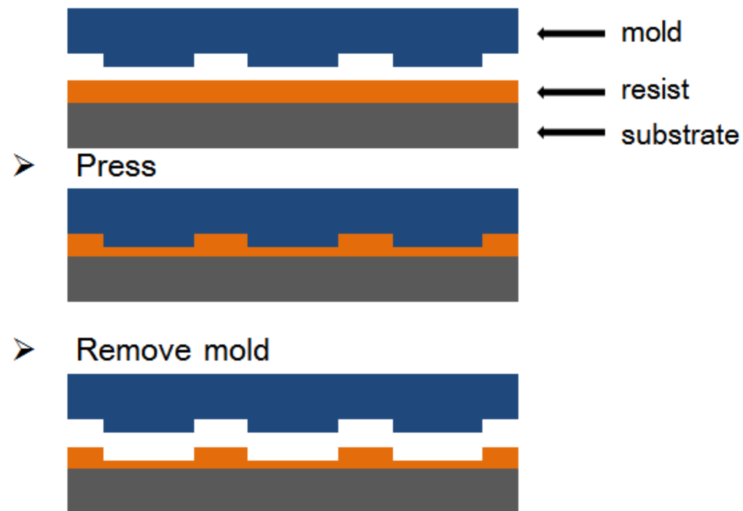


Fig. 1-1 Schematic structure of nanoimprint.

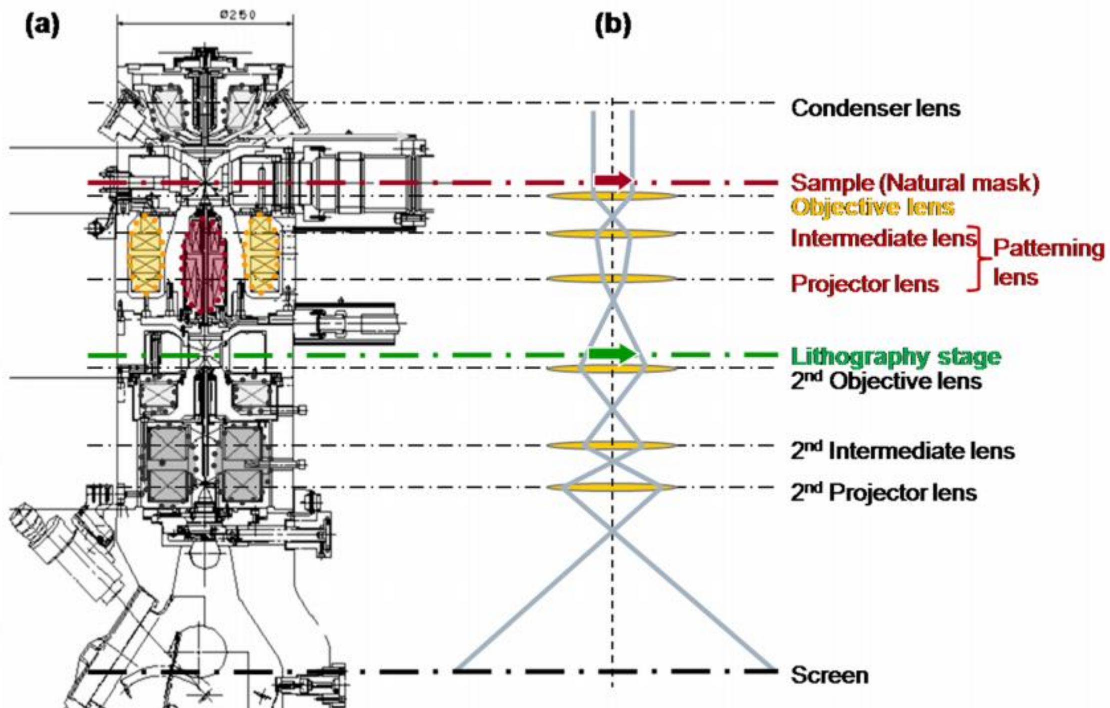


Fig. 1-2 Schematic structure of EBDW, (a) design diagram, (b) ray diagram [4].

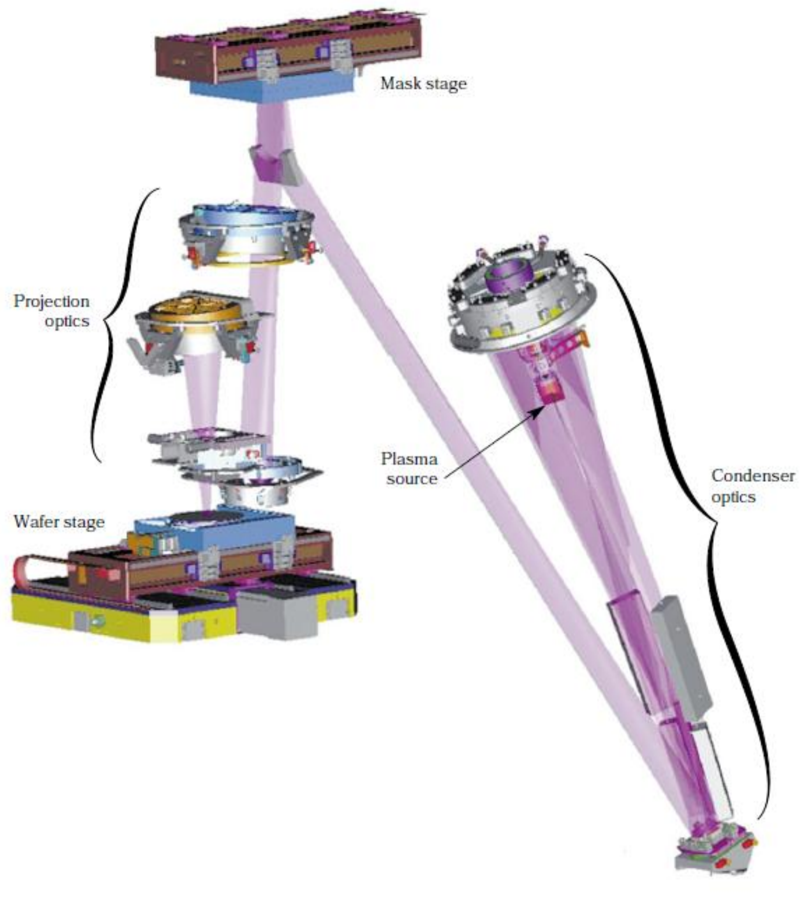


Fig. 1-3 Schematic structure of EUVL system [1].

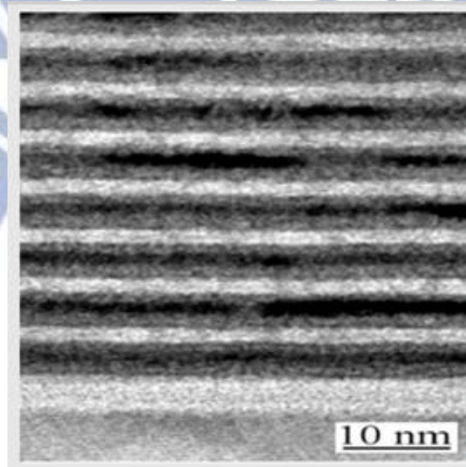


Fig. 1-4 TEM cross section of a Mo/Si multilayer. Such materials are employed to produce Bragg mirrors that reflect EUV light [11].

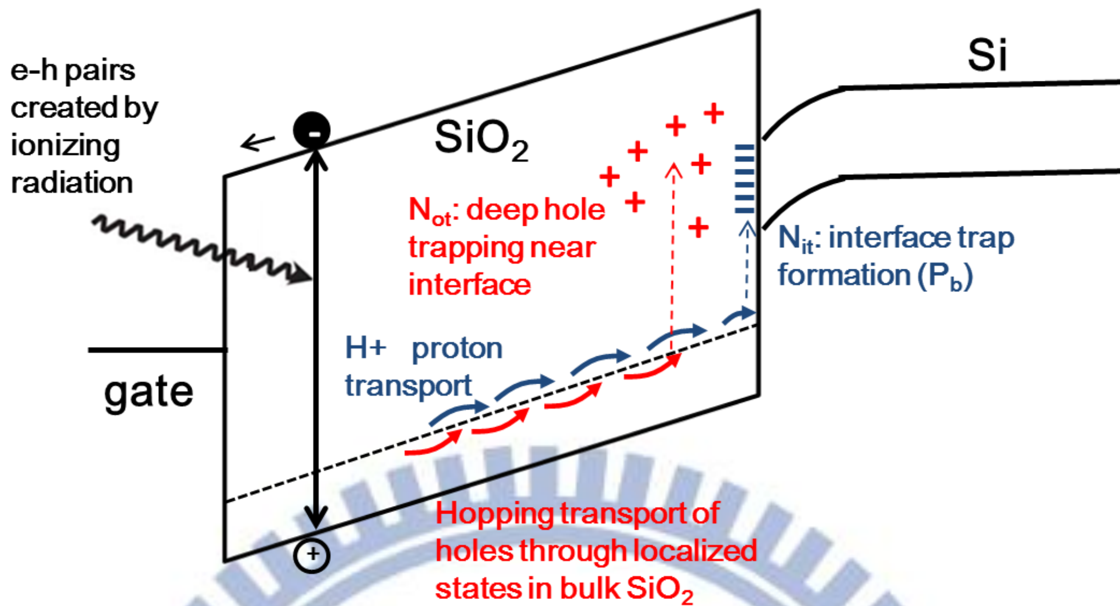


Fig. 1-5 Schematic of ionizing-radiation-induced effects in MOS structures, with the case of positive gate bias is shown [13].

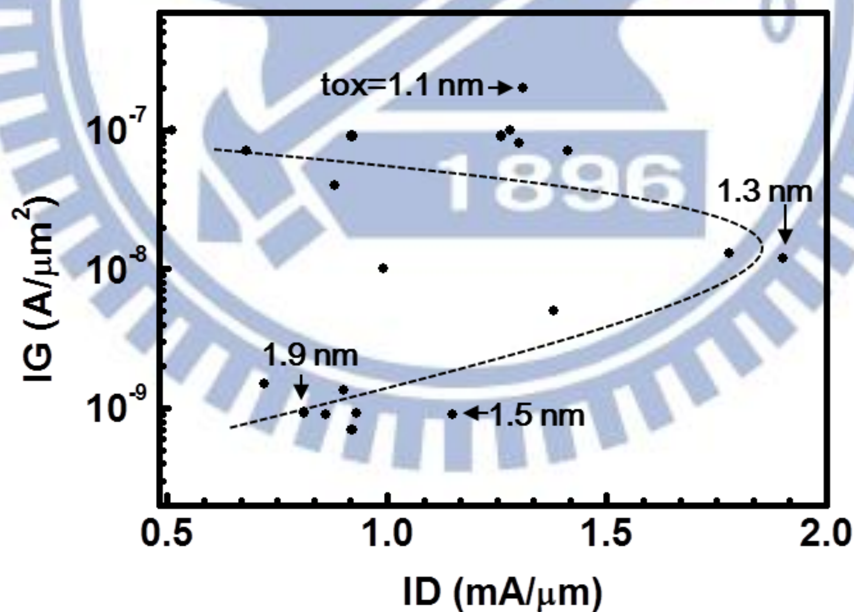


Fig. 1-6 Driving current vs. gate leakage current for a L_g=70 nm nMOSFET. The driving current measurements were all obtained at V_D=V_G=1.5 V. The leakage was measured at V_G=1.5 V and V_D=0 V. The dotted lines are a guide to the eye. The oxide thicknesses associated with 4 of the results are indicated. The maximum driving current in each case corresponds to an oxide thickness of about 1.3 nm. The driving current capability deteriorates for thicker or thinner oxides [16].

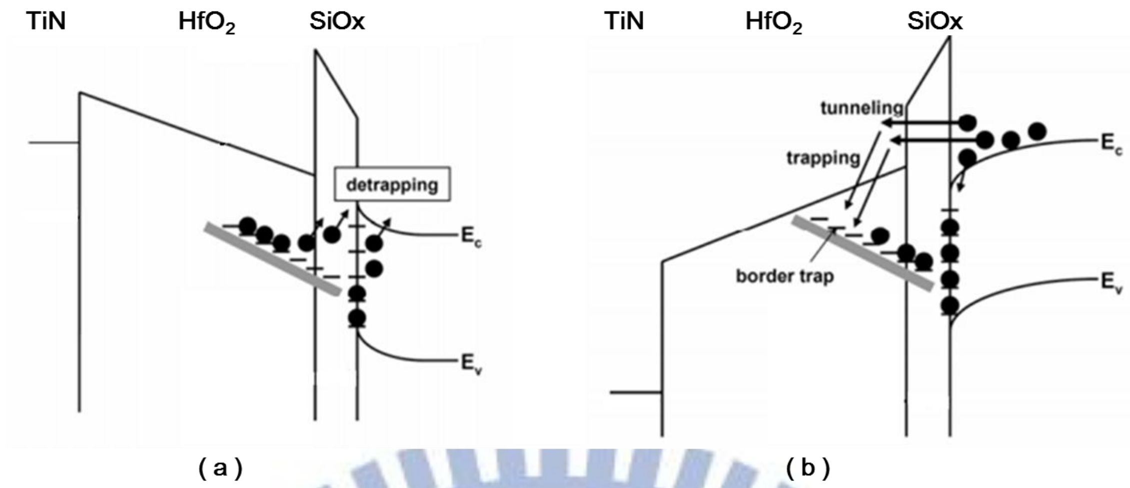


Fig. 1-7 Schematic of hysteresis phenomenon in MIS capacitor, (a) detrapping process with negative gate bias, (b) trapping process with positive gate bias [25].

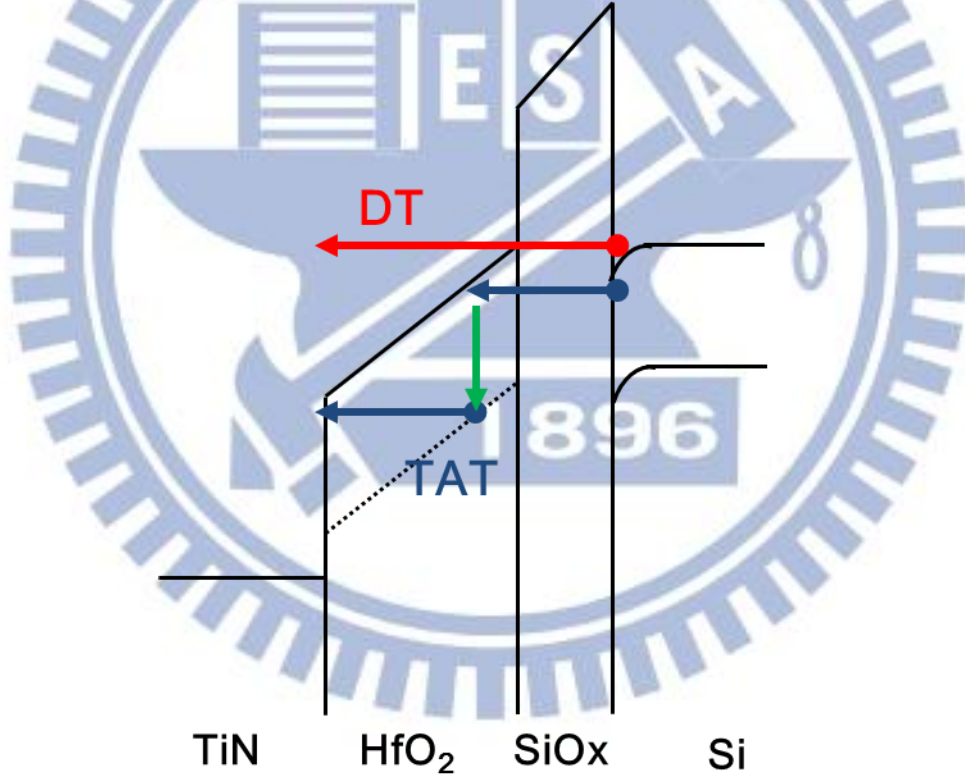


Fig. 1-8 Schematics illustrating charge trapping and tunneling under PBT stress.

Chapter 2
Experimental Procedure

2.1 Device Fabrication

Metal-insulator-semiconductor (MIS) capacitors and state-of-the-art nMOSFETs are prepared to investigate EUV radiation damage effect in this thesis. In most cases, we utilize MIS capacitor because it is a relatively simple structure hence we can easily distinguish the change in the dielectric after EUV irradiation. We use HfO_2 as gate dielectric because it is a popular alternative dielectric to replace SiO_2 and it has been applied in many advanced devices by industry. TiN is selected as the gate electrode to match up HfO_2 because it is a midgap metal and bring appropriate V_{th} for both nMOS and pMOS. A thin chemical oxide is used as the interfacial layer because it results in better radiation hardness which has been verified by previous work. We modulate the thickness of TiN to 40 nm in order to ensure that the EUV radiation can penetrate into gate dielectric.

In the following sub-sections, the devices fabrication processes are described in detail.

2-1-1 Fabrication Process of MIS Capacitor

Fig.2-1 shows the structures of the MIS capacitor with various dielectric thicknesses. The device was fabricated on 4-inch p-type Si wafer with resistivity of 1~10 Ω-cm and all of the processes were performed at the Nano Facility Center (NFC) at NCTU and the National Nano Device Laboratories (NDL). The detailed process steps are listed below.

1. In order to achieve better ohmic contact characteristic on the back electrode, the backside of the wafer was first implanted by BF_2^+ at 40 keV to a dose of 5×10^{15} cm^{-2} at NDL.
2. The wafer was cleaned by the standard RCA clean process, and then a 150-nm-thick SiO_2 was thermally grown as field oxide by a horizontal furnace system at NFC. The process temperature was 1000 ℃.
3. After defining the active region by lithography, the second RCA clean process was used to clean the wafer before the gate dielectric deposition. The key point is that we deleted the last DHF dip step of the RCA clean process in order to remain the chemical oxide as interfacial layer.
4. The HfO_2 was deposited as gate dielectric by atomic layer deposition (ALD) system at NFC. The thicknesses of HfO_2 were 5 nm, 10 nm, and 15 nm. The process temperature was 250 ℃, the pressure was about 200 mtorr in 200 sccm Ar chamber and the precursors were TEMAH and H_2O.
5. In order to protect the dielectric, we in-situ continually deposited a 5-nm-thick TiN after HfO_2 deposition by the same ALD system at NFC, and then a 35-nm-thick TiN was deposited by a sputtering system at NDL.
6. After the metal deposition, devices were processed by a rapid thermal annealing in N_2 gas at NDL. The process condition was 500℃/30s.
7. The gate electrode was patterning by a high-density plasma reactive-ion-etching (HDP-RIE) system at NFC. The etching recipe used the mixed gas of Cl_2 and BCl_3, and the mass flow is 35 sccm, respectively. The etching power is 450 W.
8. After the gate patterning, devices were capped with a 100-nm-thick nitride by a plasma enhanced chemical vapor deposition (PECVD) system at NDL in order to avoid the influence of moisture [35]. The etching chemistry was DHF with HF : H_2O = 1 : 20.

9. The backside of the wafer was wiped by BOE to remove native oxide, then immediately was evaporated a 300-nm-thick Al as back electrode by a thermal evaporation system at NFC.
10. All samples were annealed in forming gas at 300 ℃ for 30 minutes.

2-1-2 nMOSFET Structure

We also prepared the state-of-the-art nMOSFETs to actually investigate the EUV radiation damage effect. The nMOSFET used in this study is a planar structure fabricating by the gate last process. The isolation technique is shallow trench isolation (STI) and the Ni-silicide was formed on source/drain to reduce the parasitic resistance. The materials of gate electrode and gate dielectric are TiN and Hf-based dielectric, respectively. The gate dielectrics consist of a 2-nm-thick HfO_2 and a 0.2-nm-thick interfacial oxide.

2.2 Experimental Environment in NSRRC

As mentioned in chapter one, the synchrotron radiation is one of a method to produce EUV. The basic concept of synchrotron radiation is whenever electrons move close to the speed of the light are deflected by the accelerated bending magnets, they may radiate a thin beam of radiation tangentially from their path. This thin beam is called the synchrotron radiation. The electrons in the NSRRC are first accelerated in the linear accelerator (LINAC) and booster ring. They are then sent through the transport line and into the storage ring where they circulate in vacuum pipes for several hours emitting synchrotron radiation. The emitted light is channeled through beam lines to the experimental station where experiments are conducted. The illustration is shown in Fig. 2-2 which is provided by NSRRC. Unlike conventional X-ray tube, the synchrotron

radiation has many excellent properties such as high intensity, continuous spectrum, excellent collimation, low emittance, and polarization light. For these reasons, the synchrotron radiation is a good radiation source to provide stable EUV light.

There are twenty-four beamlines in the NSRRC. In this study, we make major use of beamline number 08A1 to proceed EUV experiments and we also use beamline 07A as high energy X-ray source. In the following sub-sections, the experimental steps are described in detail.

2-2-1 End-station Setup at Beamline Number 08A1

The beamline number 08A1 is also called flying-dragon beam line, which uses spherical optical elements and a movable exit slit to maximize the photon throughput and energy resolving power. It consists of one horizontal focusing beam (HFM), one vertical focusing beam (VFM), one spherical grating monochromator with three gratings, and one toroidal refocusing mirror (RFM). This beamline is designed for a spectral range of 15 to 200 eV, and it covers the energy of EUV light (91.85 eV).

At the end of the beamline is an end-station where it is the main experimental region. Our end-station consists of a main chamber, a differential chamber, three valves, and two turbo pumps. The outlook and photo of the whole system are shown in Fig. 2-3. The main chamber is the place where we put the sample in and the differential chamber alleviate the pressure of the main chamber.

The shape of the beamline is a smiling shape (Fig. 2-4) and the size is 0.016 cm^2. The structure of the sample rod is shown in Fig. 2-5. The sample rod is an adjustable rod which can move up and down. It consists of a photodiode and a steel board with a window. We use photodiode to measure photoelectrical current and then convert it to the dose of EUV. Among the experiment, we stick the sample on the steel board behind the window; it can avoid the radiation contamination. The following is the operating

procedures.

1. Check all the valves (V1, V2, and V3) and turbo pump 1 and 2 are close (The user should wait at least 20 minutes after turn off the turbo pump to let the turbo pump slow down).
2. Vent the main chamber from the back turbo pump 1 with N_2 gas purge.
3. Open the sample rod and take it out.
4. Stick the sample on the sample rod.
5. Load the sample rod into the main chamber and lock it off.
6. Open V2, the scroll will pump down the pressure of main chamber to 5×10^{-2} torr then open V3 and wait for 1 minute.
7. Start turbo 1 and turbo 2.
8. Open V1.

As the pressure of the main chamber is pumped down to 1×10^{-7} ~ 5×10^{-8} torr, then we can start to expose EUV radiation. The EUV light is invisible hence first we have to use white light to adjust the light position. The main irradiation processes are as follows:

1. Set the synchrotron light to white light.
2. Open the beamline valve and make the white light pass through differential chamber and incident in the main chamber.
3. Using telescope to observe white spot and set the telescope cross line on the light spot site.
4. Open beamline valve to block the white light and set light to EUV.
5. Move the sample to the telescope cross line in order to ensure that EUV can incident on the sample.
6. Open beamline valve then EUV incidents on the sample and count down the exposure time.

7. Turn off the beamline valve to block EUV.
8. Return to step 5 if there are other samples on the sample rod.

After the irradiation process is over, user can follow the changing steps to repeat the experiment or finish the experiment.

2-2-2 Experimental Setup at Beamline Number 07A

The beamline 07A is designed for general purpose experiments including wide angel X-ray diffraction (WAXD), grazing-incidence X-ray diffraction (GIXD), X-ray absorption fine structure (XAFS), and so on. The spectral range of this beamline is 5 to 23 keV. The monochromator is used to adjust the energy of radiation, and the energy is estimated from Bragg formula. The energy might not be a specific value since the Bragg angle cannot be accurately controlled. This beamline consists of three experiment stations including XAFS station, scattering experiment station, and micro-probe experiment station. In this study, the energy we used to investigate the radiation damage effect is 10 keV.

The end-station of beamline 07A is a guarding room (Fig. 2-6). Vacuum environment is not necessary for this beamline; in other words, the whole experiments are performed in the atmosphere environment. The following is the operation procedures.

1. At first, we have to measure the beam position by a photographic paper. When the X-ray incidents into the paper; it will emerge a mark on the paper, and then we use this mark to align the sample.
2. Stick the sample on the experiment station (Fig. 2-7) and let it aligning with the mark upon the photographic paper, and then leave the guarding room.
3. Set the parameters of X-ray and start the irradiation.

After the irradiation process, user can repeat the steps mentioned above or finish

the experiment.

2-3 Electrical Characterization

In this section, the measurement setup and parameter extraction methods in this study are introduced. This section is partitioned into three sub-sections: dose calculation, oxide and interface trap extraction, and PBTI measurement.

2-3-1 Dose Calculation

The unit of dose used in this study is energy per area. The dose is estimated through the flux of the beamline. In fact, there are already two slits to control the flux, one is located near the end-station, and the other is located near the front of the beamline, as shown in Fig. 2-8. However, this is just a rough setting and the variation of flux always exists even if at the same beamline. In order to solve this uncertainty, we have to use photodiode to extract the accurate dose during experiments. We can adjust these two slits to control the photoelectrical current, and then convert it to the dose we want in the experiment.

The photodiode used in this study is AXUV100G which is developed by the International Radiation Detectors incorporation (IRD inc.). It is installed on the sample rod and is connected to a current meter. The sensible range of this photodiode is 7 to 100 eV of photon energy. One of the advantages of this photodiode is that it provides a high quantum efficiency. Fig. 2-9, which is provided by IRD inc., shows the photon energy versus the quantum efficiency of this photodiode. The quantum efficiency is 24 when the light source is at 13.5 nm wavelength (EUV). The flux related to the current can be described as:

$$Flux = \frac{current}{24 \times 1.6 \times 10^{-19}} \quad (2\text{-}1)$$

The flux can be calculated from the photoelectric current. Generally, the flux of beamline 08A1 is about 1×10^{12} photons/sec. The area of the beamline is 0.016 cm^{-2}. Hence, the dose rate can be expressed as:

$$\frac{(1\times10^{12})\times91.85\times1.6\times10^{-19}}{0.016}=0.918\frac{mJ}{cm^{2}\bullet\text{sec.}} \tag{2-2}$$

According to this equation, we only need to adjust the exposure time and then get the dose we want. By the same method, the flux of beamline 07A is also $1\text{x}10^{12}$ photons/sec, the dose rate of the beamline 07A is 100 $mJ/cm^2 \cdot$ sec..

In fact, the dose calculated by eq. 2-2 is on the sample surface. The real dose on the dielectric layer is related to the layer over the dielectric. We should consider it carefully. The following eq. is the probability of radiation passing through the material:

$$p(x)=e^{-\frac{x}{\lambda}}, \tag{2-3}$$

where p(x) is the probability of radiation passing through the dielectric, x is the depth, and λ is the attenuation length. According to eq. 2-3, the probability is in connection with two factors: the attenuation length and the thickness of material. The attenuation length is related to the radiation source. High energy radiation has longer attenuation length and deeper penetration depth. Also, the thicker material has lower passing through probability because the thicker layer absorbs more photons.

2-3-2 Oxide Trap and Interface Trap Estimation

High energy radiation will cause damages on the device through generating e-h pairs and breaking chemical bondings in the dielectric. We utilize the capacitance-voltage (C-V) measurement to calculate the degree of the radiation damages. After irradiation, C-V curve may distort or shift in parallel. The distortion of the C-V curve means the increasing of interface traps and the parallel shift of the C-V curve indicates that there are trapped charges in the dielectric. The important thing we

focus on is the change of oxide trap (ΔN_{ot}) and interface state density (ΔN_{it}) before and after irradiation. In other words, we do not have to calculate the total oxide traps and interface traps. We can use the midgap voltage difference before and after irradiation (ΔV_{mg})) and the flatband voltage difference before and after irradiation (ΔV_{fb})) to estimate the ΔN_{ot} and ΔN_{it}. The equations are listed in the following.

$$\Delta V_{mg} \equiv V_{mg1} - V_{mg2} \tag{2-4}$$

$$\Delta V_{fb} \equiv V_{fb1} - V_{fb2} \tag{2-5}$$

Where V_{mg1} and V_{mg2} stand for the midgap voltage before and after irradiation, respectively; V_{fb1} and V_{fb2} are the flatband voltage before and after irradiation, respectively. Then the ΔN_{ot} and ΔN_{it} can be easily estimated by the following equations.

$$\Delta N_{ot} = -\frac{C_{ox} V_{mg}}{qA} \tag{2-6}$$

$$\Delta N_{it} = -\frac{C_{ox}(V_{fb} - V_{mg})}{qA} \tag{2-7}$$

The basic concept of this method can be explained by the band diagram, as shown in Fig.2-10. Figs.2-10 (a) and (b) are the band diagrams which the gate voltage is at flatband and midgap, respectively. It is known that the interface states in the upper half of the Si bandgap are predominately acceptor-like; in contrast, those in the lower half of the bandgap are predominately donor-like [14]. Therefore, at a gate voltage when the Fermi-level intersects the middle of the bandgap at the Si surface; the charge state of the interface traps is neutral because all the donor-like traps are filled and all the acceptor-like traps are empty. Accordingly, the presence of the N_{it} causes no effect on V_{mg}, and the V_{mg} is only determined by the N_{ot}. On the other hand, the V_{fb} is affected by both N_{it} and N_{ot}. For this reasons, we can figure out the eq. 2-6 and eq. 2-7.

2-3-3 PBTI Measurement

In this study, we also use the state-of-the-art nMOSFET to investigate the effects of radiation damages. The positively-biased temperature instability (PBTI) measurement condition is shown in Fig. 2-11. The source, drain, and body are grounded together and the gate is applied a positive bias. The gate bias applied is 1.5 V corresponding to an about 10 MV/cm electric field at room temperature and 150°C. The stress time is 10^4 seconds and it is partitioned into several stress time intervals. After each stress time interval, we immediately measure the V_{th} in order to avoid the trapping/detrapping effects in the dielectric with time. In fact, the positive bias temperature stress is an accumulative process hence we should not use the identical device before and after irradiation. We select the devices which electrical characteristics are similar to do experiment as possible as we can.

The method we used to extract the V_{th} is the maximum transconductance (G_m) method. We plot the G_m versus V_g curve and then extrapolate a gate voltage which is defined as $V_{Gm,max}$ corresponding to the maximum G_m. The equation of V_{th} is defined as：

$$V_{th} = V_{Gm,\max} - \frac{V_{DS}}{2} \tag{2-8}$$

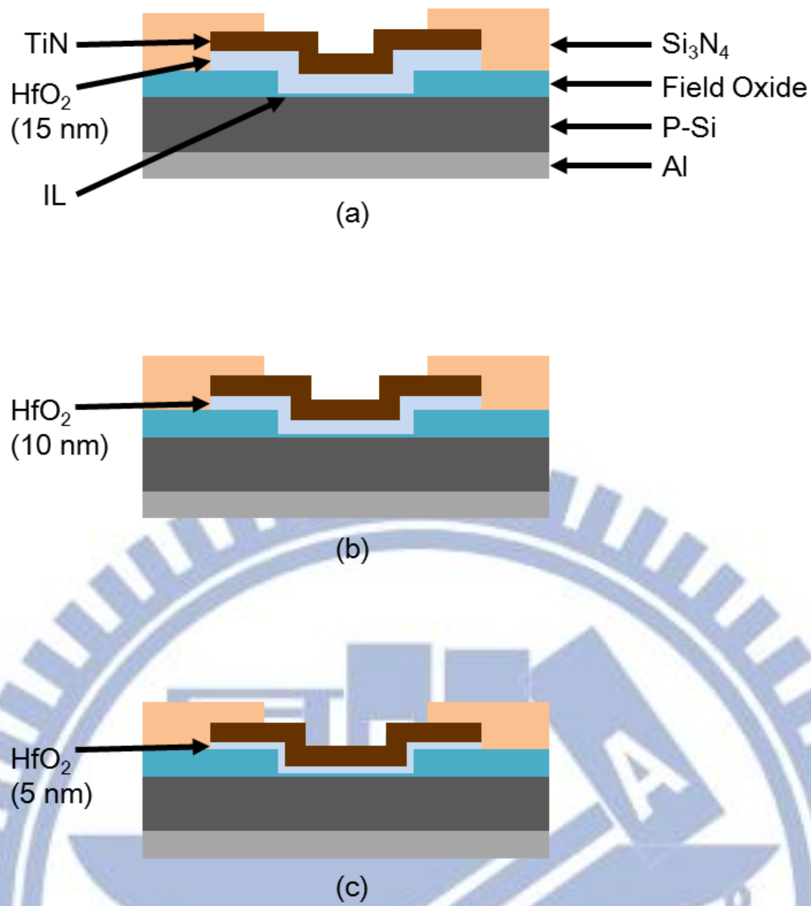


Fig. 2-1 Schematic cross-sectional structures of the MIS capacitors with different HfO_2 thicknesses.

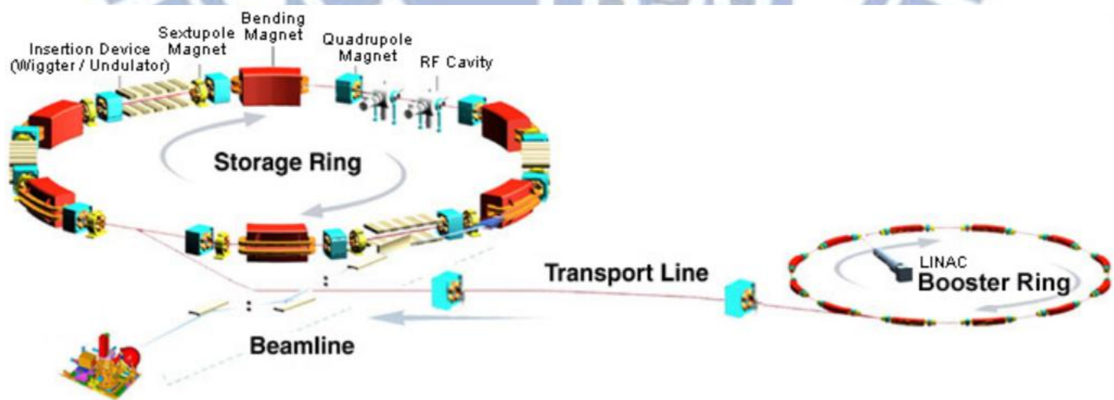


Fig. 2-2 Illustration of synchrotron working in the NSRRC. The Fig. is provided by the website of NSRRC.

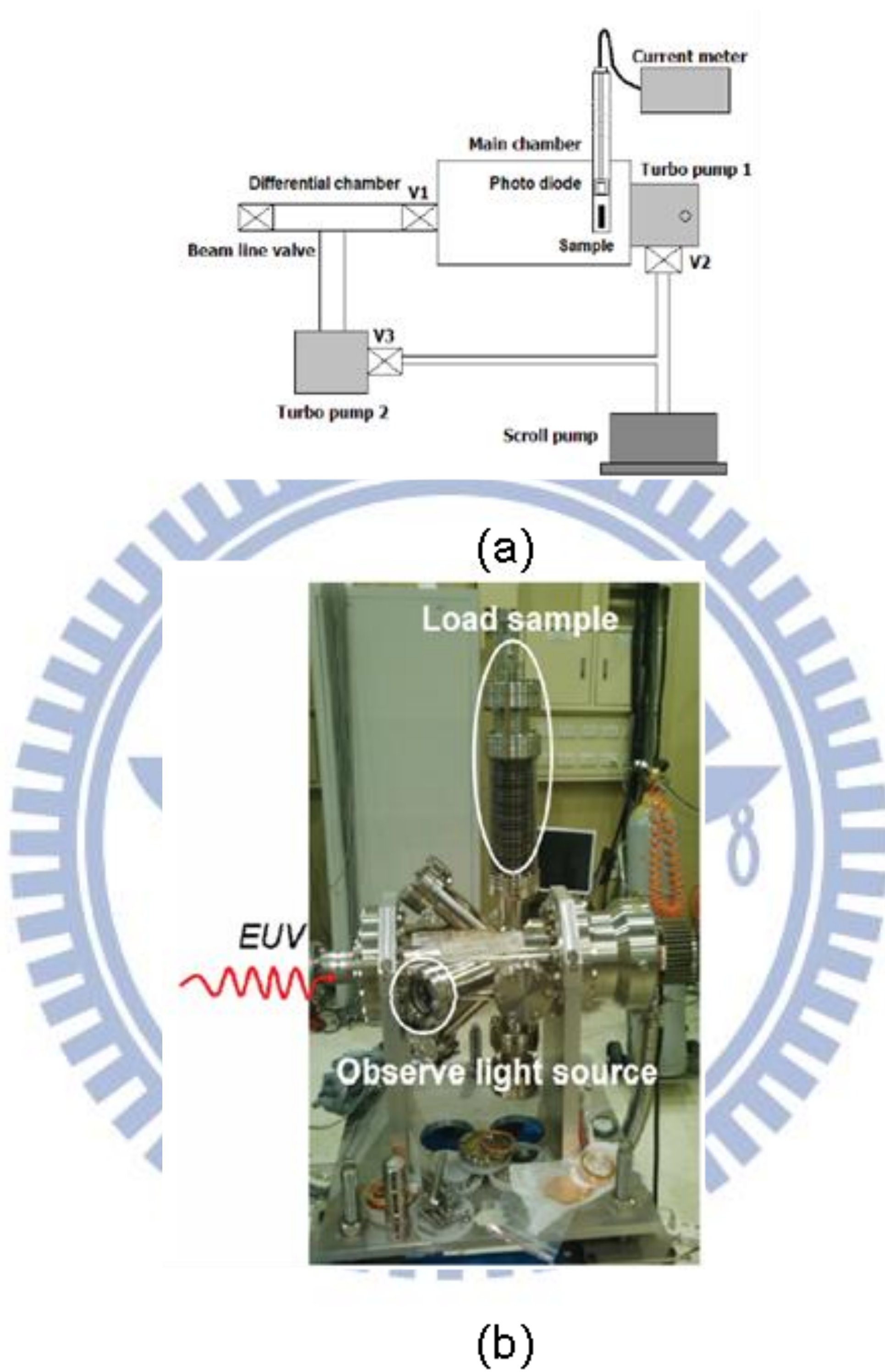


Fig. 2-3 (a) System module of the end-station, (b) Photo of the end-station.

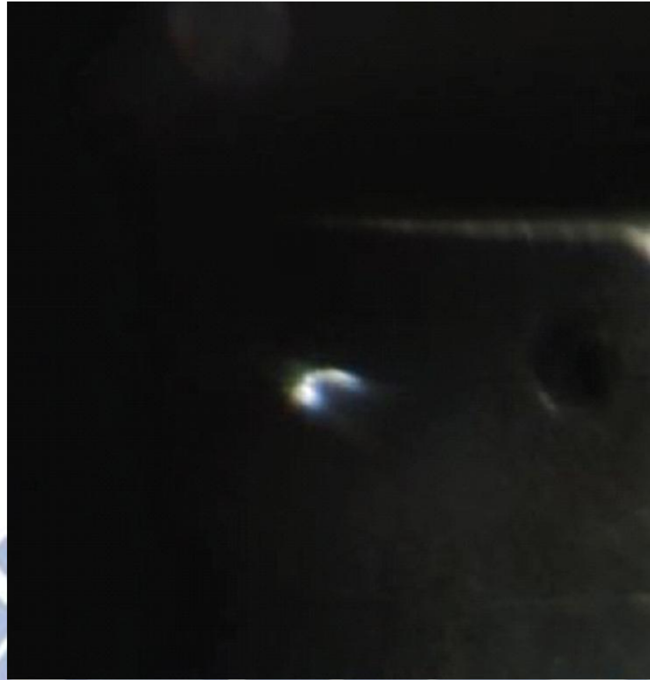


Fig. 2-4 Smiling shape of beamline 08A1 and its size is 0.016 cm^{-2}.

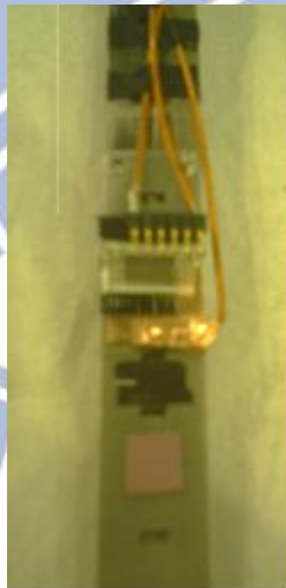


Fig. 2-5 Photo of the sample rod.

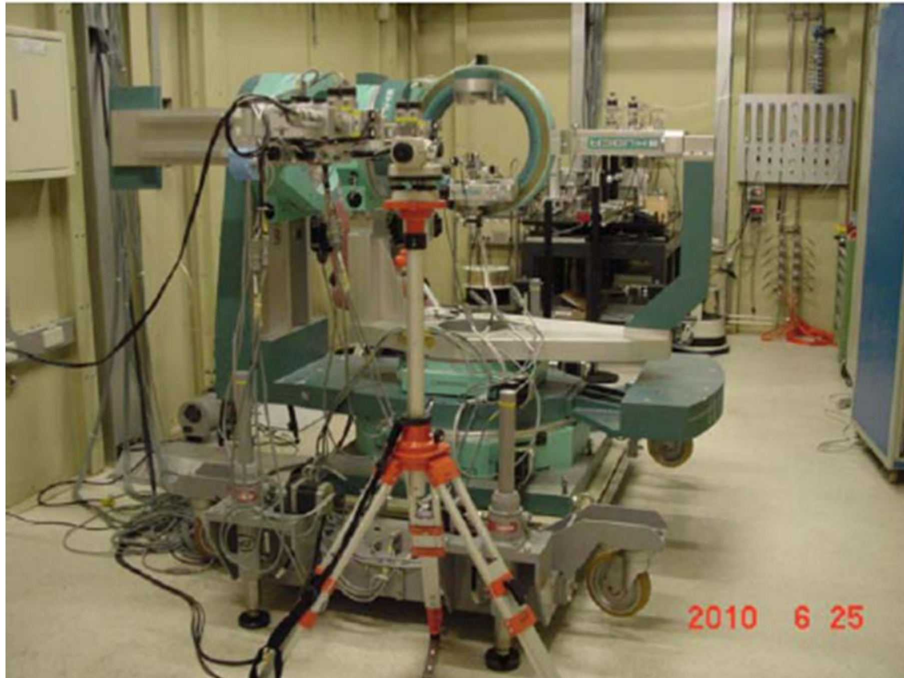


Fig. 2-6 Guarding room of beamline 07A.

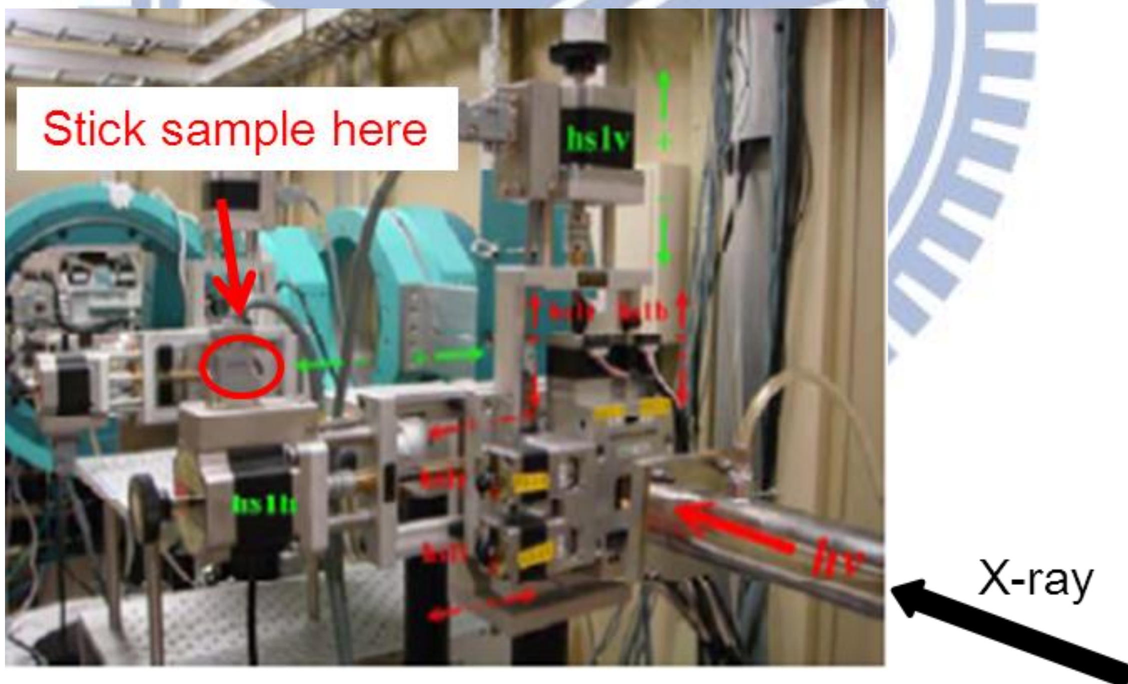


Fig. 2-7 Photo of the end-station in beamline number 07A.

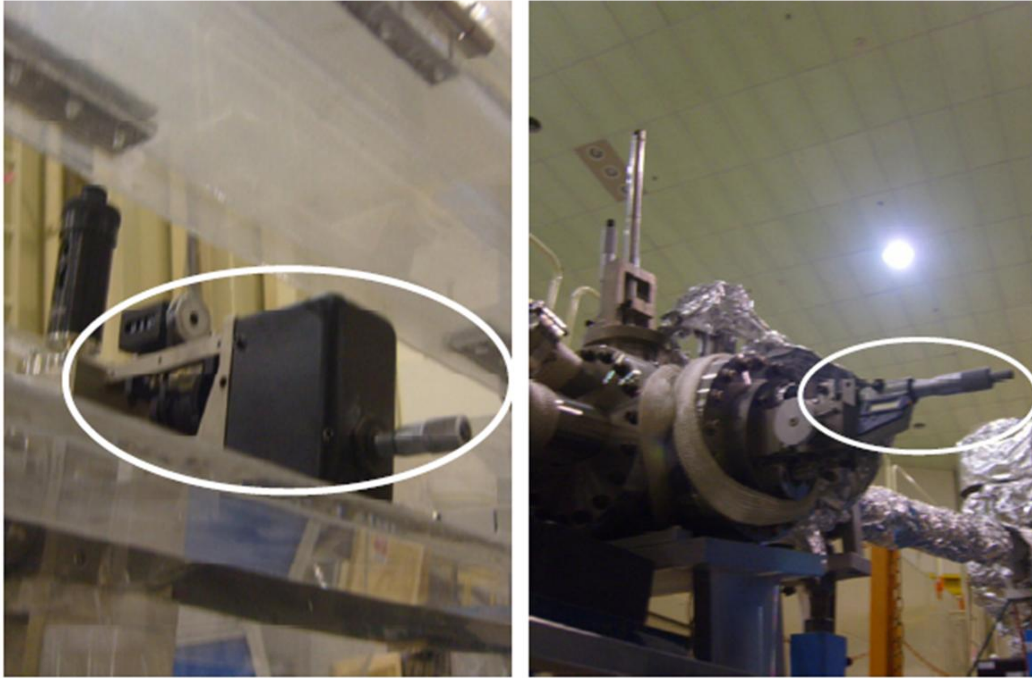


Fig. 2-8 Photographs of two slits at beamline 08A1. One is near the end-station, and the other is in front of the beamline.

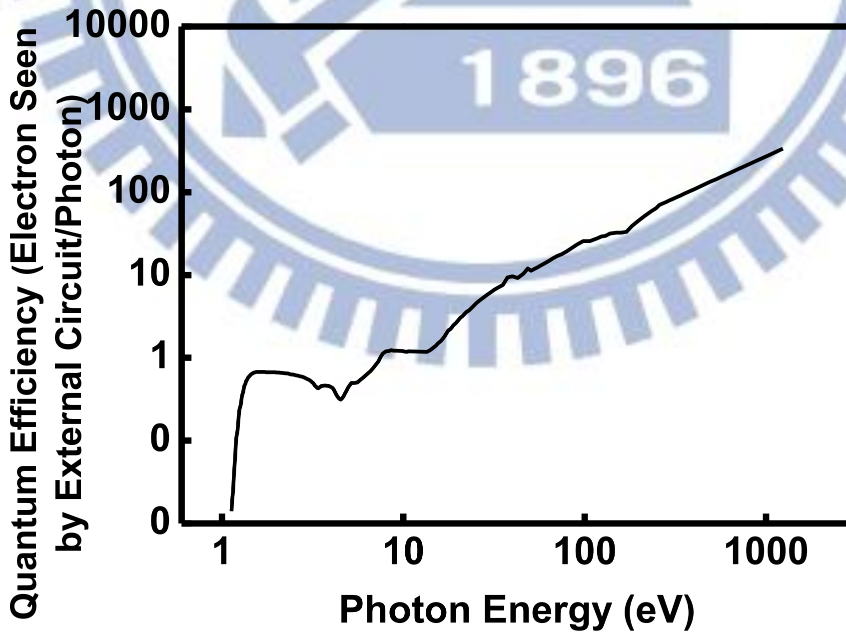


Fig. 2-9 Quantum efficiency versus photon energy plot. The data is provided by IRD inc..

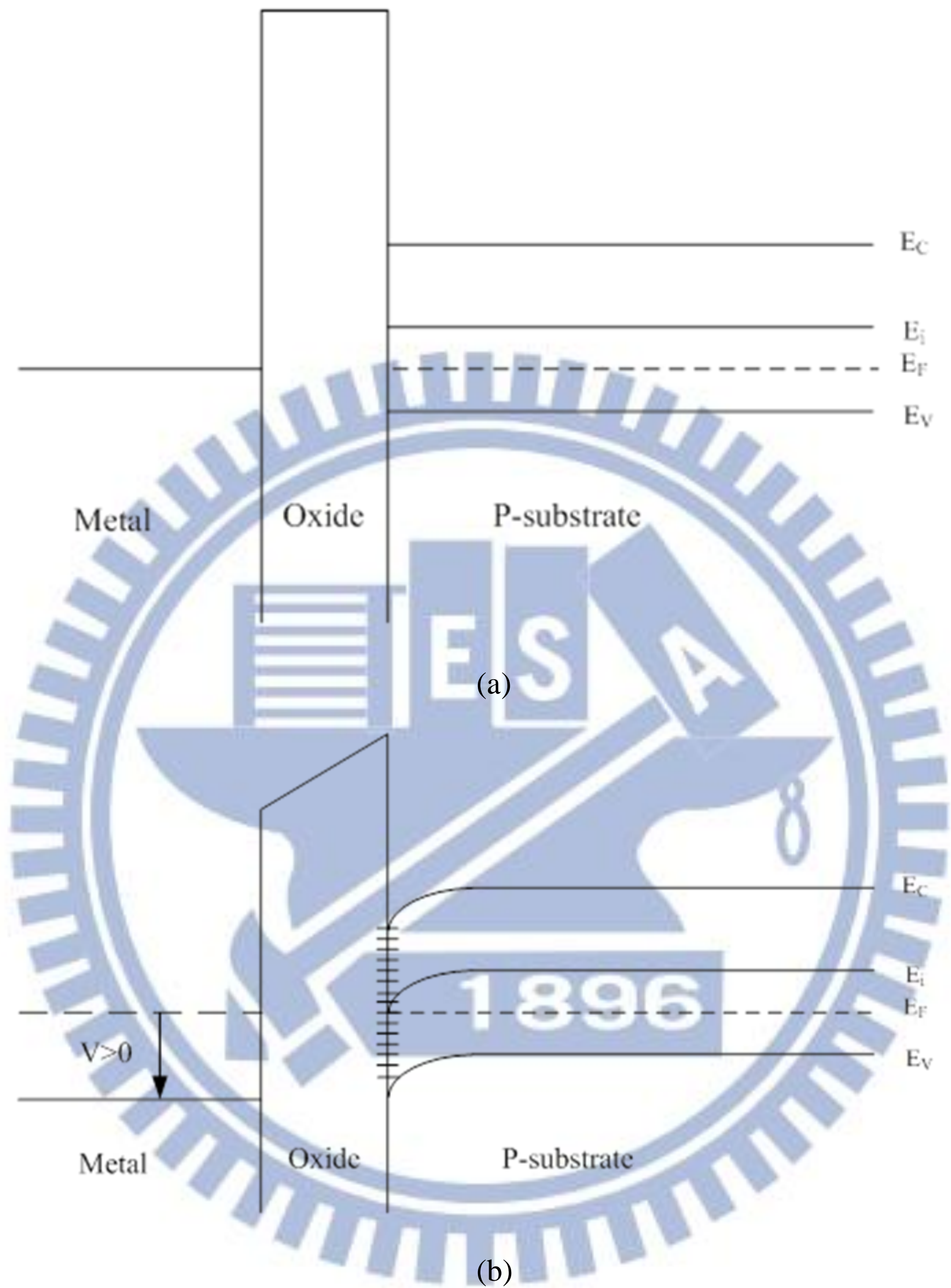


Fig. 10 (a) Band diagram at flatband voltage, (b) Band diagram at midgap voltage [33].

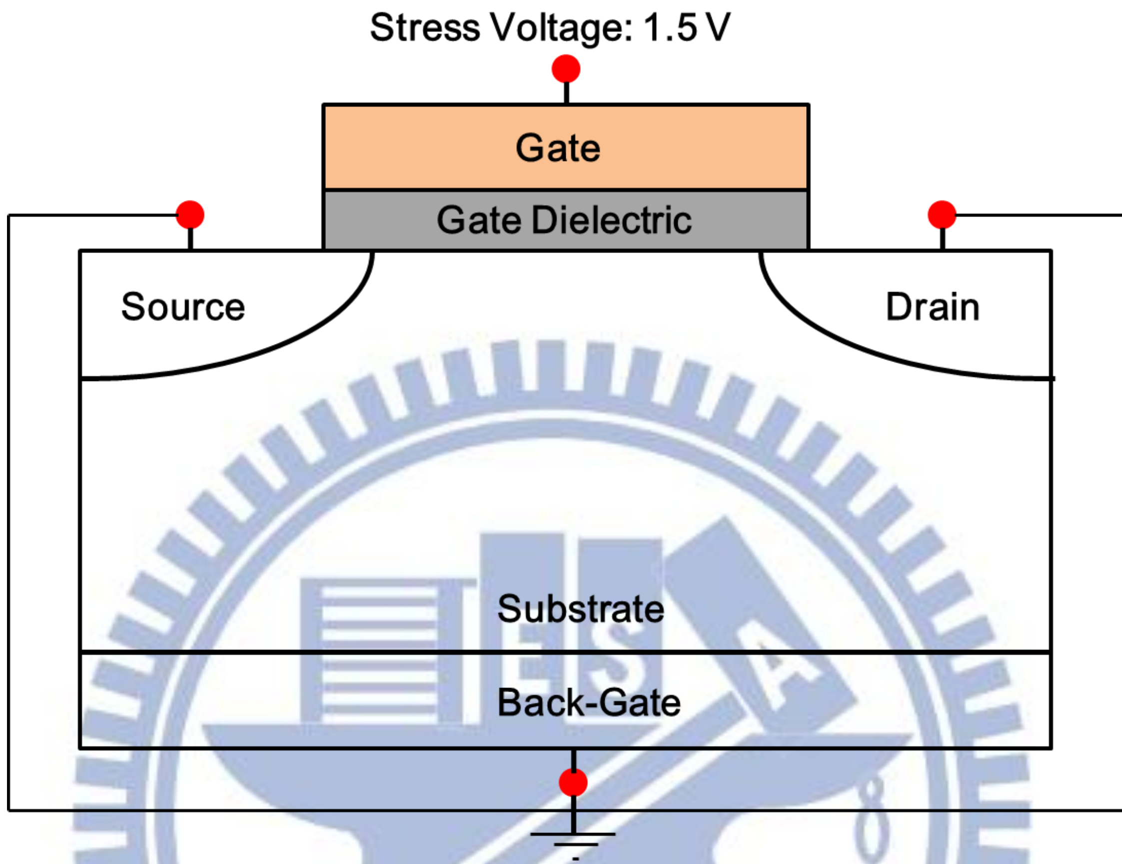


Fig. 2-11 PBTI stress condition for nMOSFET .

Chapter 3

Experimental Results and Discussion

3-1 Introduction

In this chapter, the characteristics of the MIS capacitor and the state-of-the-art nMOSFET after EUV and 10 keV X-ray irradiation are investigated. At the beginning, the MIS capacitors with three different dielectric thicknesses are analyzed and discussed. The radiation hardness on each sample by various doses, the magnitude of flatband voltage shift ($\triangle V_{fb}$), midgap voltage shift ($\triangle V_{mg}$), recovery properties with time and high temperature annealing are evaluated. Second, we utilize the state-of-the-art nMOSFET to investigate radiation hardness in order to be close to the actually operative condition. We distinguish the difference of radiation damage effect between MIS capacitor and nMOSFET. Third, we compare the radiation hardness between EUV and 10 keV X-ray irradiation. We observe that the degree of radiation damages is quite different between these two radiation sources. At last, we investigate the reliability of the state-of-the-art nMOSFET through positive bias temperature instability (PBTI) measurement. The accelerated testing conditions are listed: the stress voltage is 1.5 volt and the temperatures are set at room temperature (25 ℃) and 150 ℃. Similarly, we measure the PBTI of devices before and after EUV and 10 keV X-ray irradiation and discuss the influence of ionizing radiation.

3-2 Ionizing Radiation Irradiation on MIS capacitor

3-2-1 Basic Electrical Characteristics

In this thesis, we prepared two sets of MIS capacitors to evaluate the radiation damage effects. The variables of these two sets are dielectric's thickness and the RTA temperature after gate dielectric deposition. The devices of the first set have three different dielectric thicknesses concluding a 15-nm-thick, a 10-nm-thick, and a 5-nm-thick HfO_2 layer as gate dielectric and the sample IDs are defined as T15, T10, and T5, respectively. The second set uses the same fabrication process as the first set, only RTA temperatures after gate dielectric deposition are different. The RTA temperatures are 400℃ and 900℃, and the sample ID are defined as RTA400 and RTA900, respectively. The main fabrication parameters and the sample IDs are listed in Table 3-1.

The initial C-V curves of the MIS capacitors are shown in Fig. 3-1. The sweep direction of C-V curves is from negative bias to positive bias (forward sweep) and then from positive bias to negative bias again (reverse sweep). The forward-swept flatband voltage (V_{fb}) of the T15, T10, T5, RTA400 and RTA900 samples are -1.36V, -1.04V, -0.54V, -0.46V and -0.36V, respectively. From Fig. 3-1, the counterclockwise hysteresis phenomenon is observed in each sample, especially distinct on the T15 sample. The magnitudes of hysteresis on the T15, T10, T5, RTA400, and RTA900 samples are 0.33V, 0.25V, 38mV, 11mV, and 10mV, respectively. It is apparent that the T15 sample suffers from the worst hysteresis; it indicates that there are a large number of intrinsic border traps in the HfO_2 layer. As has been mentioned in chapter one, border traps are able to exchange charges through tunneling with silicon substrate easily. In fact, even if the amount of the border traps are the same, thicker dielectric would results in larger flatband voltage shift. On the other hand, the tunneling time is also proportional to the oxide thickness; hence, charge tunneling into thicker oxide needs much more time. For these two reasons, we can realize that the device with thicker dielectric may suffers from worse hysteresis. Besides, the tunneling probability is strongly related to the

electric field across the gate dielectric; hence, we modulate the electric field by changing applying voltage during measurement. That is, we apply a lager voltage on the thicker gate dielectric, as can be seen in the initial C-V curves.

Fig. 3-2 shows the cross-sectional TEM micrographs of each sample. We can see an obvious interfacial layer between HfO_2 layer and silicon substrate. The physical thicknesses of the HfO_2 layer and the interfacial layer for the T15 sample are 13.8 nm and 0.5 nm, respectively, and they are 8.6 nm and 0.5 nm for the T10 sample, and 4.7 nm and 0.8 nm for the T5 sample. Similarly, the physical thicknesses of the HfO_2 layer and the interfacial layer for the RTA400 sample are 4 nm and 0.9 nm, respectively, and they are 3.8 nm and 1.5 nm for the RTA900 sample. We notice that the interfacial layer of the RTA900 sample is about two times thicker than those of the other samples because it experienced a 900℃ RTA annealing after gate dielectric deposition. According to the physical thickness and the gate capacitance (C_{ox}), we can calculate the dielectric constant of the ALD HfO_2 is about 16. The effective oxide thicknesses (EOT) of T15, T10, T5, RTA400, and RTA900 samples are about 3.24 nm, 2.27 nm, and 1.66 nm, 1.41 nm, and 1.82 nm, respectively. The reason why the RTA900 sample has thicker EOT is related to its thicker interfacial layer.

3-2-2 EUV Radiation Damage Effect on Different Dielectric Thickness

In this sub-section, we mainly discuss the effect of EUV irradiation induced damages on the MIS capacitors with different dielectric thicknesses. Before experiment, we should select the devices which have similar electrical characteristics in order to avoid misjudgments. The pattern on the wafer has been designed to ensure that the beamsize is bigger than a device group; thus, all of the devices in one die can be exposed under ionizing radiation. A device group is composed of ten devices. Before

and after EUV irradiation, we measure these ten devices and find the devices with the best and the worst radiation hardness as our data in the following paragraphs.

Some reports suggest that the exposure dose of EUV photoresist is about 10 to 20 mJ/cm^2 [36]. Previous study using relatively high dose have identified the damage modes clearly. Therefore, we select lower dose in order to agree with real exposure condition. In this thesis, we mainly use 275 mJ/cm^2 and 50 mJ/cm^2 as doses. As has been mentioned in chapter two, the dose rate of the beamline 08A1 is 0.981 mJ/cm^2 · s hence the exposure time of 275 mJ/cm^2 dose and 50 mJ/cm^2 dose are 280 s and 51 s, respectively. The experimental operation procedures have been described in detail in chapter two.

Fig. 3-3 and Fig. 3-4 show the C-V curves of the T15, T10, and T5 samples after EUV irradiation with 275 mJ/cm^2 and 50 mJ/cm^2 doses, respectively. Each figure consists of two sets of C-V curves from the same device group with the best and the worst radiation hardness after EUV irradiation. First, we observe that part of C-V curves shift and distort after EUV irradiation. The fundamental model of the radiation damage effect has been introduced in chapter one and we describe the model here in detail again. As we know, the oxide layer is the most sensitive part in the device. When EUV radiation passes through the HfO_2 layer, the high energy deposited creates electron-hole pairs (e-h pair). When the measurement is in progress, electrons are swept out of the HfO_2 layer within picoseconds, and part of electrons will recombine with holes before leaving the HfO_2 layer. Those holes which escape the recombination will transport through the localized state in the HfO_2 layer toward the dielectric/Si interface by hopping. As holes moving toward interface, it may cause a distortion of the local potential of HfO_2 lattice. This local distortion could increase the trap depth at the localized site and confine the holes to its immediate vicinity then becoming a positive oxide-trapped charge [13]. These positive oxide-trapped charges may cause C-V curve

shifting toward negative voltage axis in parallel. In addition to oxide traps, ionizing radiation also leads to interface states. It is due to holes or hydrogen ions which hop through the HfO_2 layer and be trapped near the dielectric/Si interface then becoming interface-trapped charges. The interface-trapped charges may cause C-V curves distortion. Both oxide trap and interface trap degradations can be seen in our devices, especially obvious on the T15 sample. Furthermore, interface traps always exist within silicon bandgap near the interface, so the charges of interface traps can be easily changed by applying bias. In our samples, we notice that the distortion of C-V curve occurs at the upper half, it means that the EUV generated interface states are predominately donor-like traps and locate at the lower half of the silicon bandgap. To summarize, e-h pairs generation, transportation, and trapping are the three basic radiation-induced processes leading to the radiation damages. We will discuss the influence of dielectric thickness through these three respects later.

In this paragraph, we discuss the radiation damage effect between different dielectric thicknesses by numerical analyze, and the explanation will be discussed in the next paragraph. Table 3-2 lists the change of the oxide traps ($\triangle N_{ot}$), the interface traps ($\triangle N_{it}$), the border traps ($\triangle N_{bt}$), and the hysteresis after EUV irradiation at a total dose of 275 mJ/cm^2 and 50 mJ/cm^2. According to this table, the T5 sample with the thinnest dielectric thickness seems to offer the best radiation hardness both in 275 mJ/cm^2 and 50 mJ/cm^2 doses. The smallest value of $\triangle N_{ot}$, $\triangle N_{it}$, and $\triangle N_{bt}$ of the T5 samples with 275 mJ/cm^2 dose are 2.95×10^{10}, 1.76×10^{10}, and 1.29×10^{10} cm^{-2}, respectively. The smallest value of $\triangle N_{ot}$, $\triangle N_{it}$, and $\triangle N_{bt}$ for the T5 samples with 50 mJ/cm^2 dose are 7.21×10^{10}, 7.20×10^{9}, and 6.66×10^{9} cm^{-2}, respectively. It is deserved to be mentioned that all of these values are equal to or smaller than the order of 10^{10}, it is a very small value. Besides, we also notice similar phenomenon in the C-V curves, the C-V curves change the least after EUV irradiation both in 275 mJ/cm^2 and 50 mJ/cm^2 doses for the

T5 sample. On the contrary, the T15 sample almost suffers the worst radiation damages both at the total dose of 275 mJ/cm^2 and 50 mJ/cm^2. According to Table 3-2, Fig. 3-2 and Fig. 3-3, the C-V curves shift and distort after EUV irradiation corresponding to the generation of more $\triangle N_{ot}$ and $\triangle N_{it}$ both at a total dose of 275 mJ/cm^2 and 50 mJ/cm^2. Irregularly, there are some conditions that the T10 sample has the worst hysteresis and $\triangle N_{bt}$. Back to examine the C-V curves, we can see the C-V curves shift toward positive in the reverse sweep direction (sweep from depletion to accumulation) after EUV irradiation, especially on the T10 sample at a total dose of 50 mJ/cm^2. It indicates that there are many electrons from silicon substrate tunneling into the HfO_2 layer, and recombine with the trapped holes; it can be explained by the band diagram shown in Fig. 1-7. However, in the observation of forward sweep direction (sweep from accumulation to depletion), the C-V curves of the T15 sample still shift most after EUV irradiation both at a total dose of 275 mJ/cm^2 and 50 mJ/cm^2. On the other hand, we also observe that the radiation damages on the samples at the dose of 275 mJ/cm^2 are more severe than that of the samples at the dose of 50 mJ/cm^2 as shown in Fig. 3-5. Fig. 3-5 summarizes the $\triangle V_{fb}$ and the $\triangle V_{mg}$ after EUV irradiation with different dielectric thicknesses and different doses. Because there are more photons radiating into dielectric layer and generating more e-h pairs, then leading to more severe radiation damages at higher dose. The relation between total dose and radiation damage will be discussed again in the following paragraph.

Experimental results indicate that the thinner oxide offers better radiation hardness. We try to explain the phenomenon through the charge generation, transportation, and trapping. First of all, we discuss the generation of e-h pairs in the HfO_2 layer. The factor affecting the amount of e-h pairs are the bandgap and attenuation length of the material. The bandgap of HfO_2 is about 6 eV, and the attenuation length is a constant when the energy of ionizing radiation is fixed. Nevertheless, the probability of radiation passing

through the dielectric is different since the thickness of dielectric is different. Based on Eq. 2-3, the probability is lower when the λ is fixed and x is larger; that is, more photons are absorbed by material. The attenuation length in HfO_2 under EUV irradiation is 9.97×10^{-2} μm. According to Eq. 2-3, the probabilities of HfO_2 absorption under EUV irradiation for T15,T10, and T5 samples are 37.61 %, 26.98 %, and 14.55 %, respectively. As a result, although the amounts of incident photons are the same, the thicker dielectric absorbs more photons and generates more e-h pairs than the thinner one. Second, we discuss the characteristics of charge transportation in the HfO_2 layer. Fig. 3-6 depicts the charge distribution after irradiation. One of the important factors affecting hole transportation is the electric field across the dielectric. In this study, in order to let the electric field across the dielectric is equal on each sample, we modulate the applying voltage according to the C_{ox} when the measurement is in progress. The maximum applying voltages on T15, T10, and T5 samples are -4.0 V, -3.2 V, and -2.0 V, respectively. In addition, the electric field across the gate dielectric is weak after irradiation. Electrons near the interface of dielectric/gate and dielectric/substrate will leave the dielectric quickly due to its high mobility. Holes near the interface will cause a weak build-in electric field which direction is toward the bulk of dielectric. In the thicker dielectric, this weak build-in electric field is distinct and may increase holes accumulation in the bulk of the dielectric. On the contrary, in the thinner dielectric, the build-in electric field may not occur because charges can easily leave the dielectric through direct tunneling; that is, the charges cleared region covers the whole dielectric. Third, we discuss the trapping mechanisms of holes generated by EUV. It is known that high-k material has more intrinsic defects than conventional SiO_2, and these defects can lead to undesired transport and the trapping-induced instabilities [22]. In fact, the microscopic of these defects are referred as to oxygen vacancy, oxygen interstitial, or lattice mismatch [23-24]. These defects can act as a trapping center. Subsequently, we

focus on the dielectric thickness dependence between hole transport and trapping. At first, we know that there are large amounts of intrinsic defects in the thicker HfO_2 layer than the thinner one; besides, the thicker dielectric also absorbs more photons and offers a long transportation distance. Accordingly, the holes generated by EUV radiation have relatively high probability to be trapped in the thicker dielectric.

Figs. 3-7 shows the total dose effect on the T15, T10, and T5 samples, respectively. The T15 sample has the most apparent dose effect as the dose increasing. On the contrary, the dose effect on the T10 and T5 samples are nearly invisible. It is an interesting phenomenon that the radiation damage effects do not change significantly in the thinner dielectric with the dose increasing. In fact, several studies have reported the linear dependence between threshold voltage shift and dielectric thickness, and employ physical models to explain it [37-40]. Nevertheless, for very thin oxide (< 20 nm), especially ultrathin oxide (< 5 nm), the threshold voltage shift is substantially smaller than that would be extrapolated from the linear dependence of the thicker oxides. It is widely believed that the holes which are captured by hole traps within a very short distance (2-5 nm) of the silicon can be recombined with tunneling electrons from the conduction band of silicon substrate. These process is also called tunnel anneal, and it will be discussed in the subsection 3-2-4 later. For this reason, we do not fit the linear dependence between voltage shift and dielectric thickness, but we still show it in the Fig. 3-5. In Fig. 3-5, we can see easily that both delta flatband and midgap voltages are very small on the T5 sample, it implies that the smaller voltage shift is influenced by tunneling process.

Moreover, we also investigate the radiation damages on the RTA400 and RTA 900 samples. Fig. 3-8 shows the C-V curves of RTA400 and RTA900 samples after EUV irradiation to a dose of 275 mJ/cm^2 and 50 mJ/cm^2. Table 3-3 lists the electrical characteristics. As same as the T5 sample, the radiation damage effect on both RTA 400

and RTA900 samples are very slight, and the C-V curves do not change visibly. The value of $\triangle N_{ot}$, $\triangle N_{it}$, and $\triangle N_{bt}$ are all equal to or smaller than the order of 10^{10}. Accordingly, although the RTA temperature of the post dielectric deposition annealing is different, the dominant factor affecting radiation damage is still the thickness of dielectric.

In summary, we investigate the radiation damages on samples with different dielectric thicknesses at a high dose (275 mJ/cm^2) and a low dose (50 mJ/cm^2). It is observed that the thinner dielectric offers better radiation hardness; furthermore, it has slight dose effect. The experimental results on the RTA400 and RTA900 samples demonstrate the thickness of dielectric is an important factor affecting radiation damage effect again. Most important of all, shrinking dielectric thickness is a trend for current ICs technology. These experimental results maybe present hopeful news if EUVL will be used by industry in the future.

3-2-3 Radiation Damage Effect on Different Radiation Source

In addition to EUV irradiation, we also investigate the radiation damage effect of high energy X-ray which energy is 10 keV. We select T15 sample for experiment because its radiation damage effect can be distinguished easily. We want to know whether the radiation damages depend on radiation source or not. Fig. 3-9 shows the C-V curves of the T15 sample after EUV and 10 keV X-ray irradiation at a total dose of 300 mJ/cm^2. From the figure, it is observed that the radiation influence of 10 keV X-ray is weaker than EUV according to the shift and distortion of the C-V curves. Table 3-4 lists the change of the electrical characteristics due to these two radiation sources after irradiation to a total dose of 300 mJ/cm^2. The value of $\triangle N_{ot}$ and $\triangle N_{it}$ of the EUV sample are 3.25×10^{12} and 1.24×10^{12} cm^{-2}, respectively, and the hysteresis and $\triangle N_{bt}$ are 0.338V and 2.38×10^{11} cm^{-2}, respectively. The value of $\triangle N_{ot}$ and $\triangle N_{it}$ of the X-ray

sample are 2.80×10^{12} and 1.06×10^{10} cm^{-2}, respectively, and the hysteresis and $\triangle N_{bt}$ are 0.343V and 2.81×10^{11} cm^{-2}, respectively. We can see that both $\triangle N_{ot}$, and $\triangle N_{it}$ of the EUV sample are larger than those of the X-ray sample, and the hysteresis and $\triangle N_{bt}$ are nearly the same. The 10 keV X-ray generates relatively fewer interface traps, and it also can be observed on the C-V curves, the distortion of EUV sample is more severe than that of the X-ray sample.

The main difference between these two radiation sources is their photon energy. EUV is also a kind of soft X-ray; however, its energy is 110 times smaller than the 10 keV X-ray. It is well-known that high energy radiation has strong penetrating property. We try to explain the experimental results from this viewpoint. First, we calculate the percentage of assimilable photons in the HfO_2 layer. We assume that all the radiations are normally incident. The attenuation length in HfO_2 for EUV and 10 keV X-ray are 3.18×10^{-2} μm and 5.17 μm, respectively. The thickness of HfO_2 layer is 15 nm. According to Eq. 2-3, we can calculate the probability of radiation passing through the HfO_2 layer for EUV and 10 keV X-ray are 62.38 % and 99.71 %, respectively. In other words, the percentages of photons which are absorbed by HfO_2 layer for EUV and 10 keV X-ray are 37.62 % and 0.29 %. For these data, although the energy of EUV is 110 times smaller than the 10 keV X-ray; however, the percentage of photons which are absorbed by HfO_2 layer for EUV is 130 times larger than that for the 10 keV X-ray; hence, the radiation damages due to EUV irradiation is more severe than that due to 10 keV X-ray irradiation. Besides, the dielectric thickness and the method of measurement are all the same in both conditions; thus, the influence of charge transportation and trapping are nearly equivalent. In brief, the absorptivity of HfO_2 layer is also an important factor affecting the radiation damages.

3-2-4 Recovery Property on MIS Capacitor

In the previous sub-sections, we knew that the characteristics of MIS capacitors may be changed more or less by ionizing radiation. Therefore, how to reduce or repair these damages caused by ionizing radiation is an important issue. In fact, the radiation damage effects are time dependent, and can be probably repaired by some methods. In this sub-section, we discuss the recovery properties of the MIS capacitors after EUV and 10 keV X-ray irradiation.

After irradiation, it has been identified that the radiation damage effects including the increment of oxide traps, interface traps, and border traps. Subsequently, we store these samples at room temperature, and measure their characteristics as time progressed. Fig. 3-10 shows the C-V curves of the T15, T10, and T5 samples after EUV irradiation for 50 days, and after high temperature annealing. The samples were annealed by a backend vacuum annealing furnace at NDL at 500 ℃ for 30 minutes, the pressure was under 1×10^{-6} torr. The reason for using vacuum annealing is in order to avoid the reaction between metal and atmosphere forming unwanted oxide layer. After 50 days, a little recovery on the T15 samples both at the dose of 275 mJ/cm^2 and 50 mJ/cm^2 is observed, but it is not evident. Besides, we do not see evidently recovery on the T10 and T5 samples, especially on the T5 samples. Previous studies have reported that the radiation damage effects may recover with time at room temperature which is called "self-annealing" among different gate dielectrics [33]. The self-annealing is connected to electron tunneling process from silicon substrate, and will be discussed in the next paragraph. However, the self-annealing effect is not evident in this study. Another method which has been used to repair radiation damage is to raise annealing temperature. Previous study reported that the radiation damages can be partially repaired by 400 ℃ vacuum annealing and 400 ℃ forming gas annealing; nevertheless, the damages has not been repaired completely [34]. In this study, we raise the annealing temperature to 500 ℃ and the results are effectual. After a 500 ℃

vacuum annealing, all of the C-V curves nearly recover to the initial state before irradiation, especially distinct on the T15 samples. Fig. 3-11 shows the change of flatband voltage and midgap voltage during recovery process. We can still see slight self-annealing effect, and all of the samples almost fully recover after 500 ℃ annealing. The T15 sample recovers 96.3% and 98.2% of flatband voltage and midgap voltage after 500℃ annealing; the T10 sample recovers 95.1% and 99.9%, and the T5 sample recoveres 94.0% and 91.3%, respectively. The T5 sample recovers fewer because its original radiation damage effect is weaker. Besides, we also observe the recovery property of T15 sample after 10 keV X-ray irradiation. The C-V curves and the change of flatband voltage and midgap voltage are shown in Fig. 3-12 and Fig. 3-13. Similarly, the self-annealing effect and recovery after 500 ℃ annealing are also observed. The percentage of flatband voltage and midgap voltage recovery are 99.9% and 99.9%, respectively. It is almost recovery completely.

In fact, there are already some physical models to try to explain the annealing effect of the radiation-induced trapped holes [41]. Basically, these models can be attributed to two primary mechanisms: electrons tunneling from silicon substrate into dielectric recombine with the oxide-trapped holes and the thermal emission electrons from oxide valence band into the trapped holes. These two mechanisms can be approximated by the tunnel front model and the thermal emission front model as illustrated in Fig. 3-14. It is assumed that all the tunneling process or thermal emission process occurs with a constant distance at any given time. The tunneling front can be written as a function which is proportional to ln(t), where t is the annealing time, i.e. the time after irradiation. Similarly, the thermal emission front can be written as a function which is proportional to $\ln(T^2t)$, where T is the annealing temperature and t is the annealing time. Through these models, the amounts of the trapped holes can be quantitatively predicted and the threshold voltage shift by the ionizing radiation can be

calculated. According to the mathematical equations, we can see that thermal emission model is the dominant factor of these two mechanisms because it is proportional to $\ln(T^2t)$. That is to say, raising annealing temperature can effectively improve the recovery property after irradiation.

In summary, a 500 ℃ vacuum annealing for 30 minutes can effectively repair radiation-induced trapped holes. The recovery property is especially obvious in the thicker dielectric. In the thinner oxide, owing to the radiation-induced trapped holes can be easily exchange charges with silicon substrate through tunneling process causing relatively fewer radiation damages; however, it still can be repaired by high temperature annealing. Specially, high temperature annealing can accelerate recovery property; its efficiency is faster than that at room temperature.

3-3 Ionizing Radiation Irradiation on nMOSFET

3-3-1 Basic Electrical Characteristics

The state-of-the-art nMOSFET is utilized to study the radiation damage effect in this section. Fig. 3-15 shows the cross-sectional TEM micrographs of the MOSFET. The gate dielectric consists of a 2-nm-thick HfO_2 and a 0.4-nm-thick interfacial layer. A 1.5-nm-thick TiN layer is used to adjust the work function of the metal gate. The total thickness of the gate electrode is 38 nm. There is a 40-nm-thick PSG above the metal gate as inter layer dielectric (ILD). The isolation technique is shallow trench isolation (STI). According to Eq. 2-3, we can calculate the probability of radiation passing through the layers above dielectric is about 29%.

The gate width and gate length of all MOSFETs measured has various dimensions. We usually use the device with 10 μm gate width and 0.15 μm gate length in this thesis.

The initial threshold voltage (V_{th}) and subthreshold swing (S.S.) are about 0.59 V and 79 mV/dec. The on/off current ratio is about 10^8.

3-3-2 EUV Radiation Damage Effect on nMOSFET

Fig. 3-16 shows the I_d-V_g curves of nMOSFET after EUV irradiation to a dose of 1000 mJ/cm^2 and 2000 mJ/cm^2. Table 3-5 lists the electrical characteristics. Owing to the small geometry of device; it is hard to align the beam spot on device precisely during exposing radiation; hence, we measure all of devices in one die and select the device with the most significant degradation as experimental data. First, we can see that the V_{th} and S.S. do not change a lot on the I_d-V_g curves, but the off-state leakage current obviously increases by a magnitude of two to three orders. In fact, according to Table 3-5, we still observe that the decrease of V_{th} and the S.S. degradation although they are not easily visible on the I_d-V_g curve. The magnitude of V_{th} shift is about 1 to 8 mV, and the average S.S. degradation is about 4%. The damage mechanisms are the same as that of MIS capacitors which have been illustrated in the sub-section 3-2-2. The V_{th} shift is owing to the positive oxide-trapped charges generated by EUV, and the S.S. degradation implies the increment of interface traps. This result can be verified with the result of MIS capacitors each other. The slight radiation damage effect is referred to as the ultrathin gate dielectric.

After EUV irradiation, the off-state leakage current increases apparently, and we discuss the mechanisms in this paragraph. At the beginning, we have to confirm the leakage path. We check the gate current first. The magnitude of gate current is about 10^{-12} to 10^{-13} A. Hence, the probability of gate leakage current can be excluded. In fact, radiation-induced charge build-up in the field oxide is the main reason of this phenomenon. Generally, the thickness of field oxide in advanced device is about several hundred nanometers, it is too thick to avoid radiation damage effect. As has been

mentioned in the subsection 3-2-2, the radiation damage effect comes from two primary reasons: oxide-trapped charge and interface-trapped charge. We discuss oxide-trapped charge first. As we know, radiation-induced charge in the dielectric is predominately positive. When there are sufficient positive oxide-trapped charges in the field oxide on p-type substrate, it can invert the silicon surface, forming an inversion layer under field oxide. This inversion layer can form a leakage path between adjacent n-type regions. Fig. 3-17 depicts two possible leakage paths in the STI [42]. One occurs at the edge of nMOSFET between the source and drain. Another occurs between the source and drain of nMOSFET and the n-well of the adjacent pMOSFET. Next, we discuss the influence of interface traps. After EUV irradiation, the interface state density increases and a depletion region forms under the field oxide. As we apply a reverse bias, the interface states in the depletion region can act as a generation center and contribute to the leakage current, as shown in Fig. 3-18. The increment of the off-state leakage current is composed of these two mechanisms. Then, we want to know which mechanism is the dominant factor after EUV irradiation. We measure the I_d-V_d curves of the n^+-p junction at reverse bias, as shown in Fig. 3-19. The magnitude of the drain current is still small. It implies that there is no inversion layer on silicon surface. Consequently, we predict although both oxide traps and interface traps increases after EUV irradiation; however, the oxide traps are insufficient to invert the silicon surface, and the increment of leakage current is primary attributed to the interface states.

In summary, both V_{th} shift and S.S. degradation are observed on the state-of-the-art nMOSFET after EUV irradiation, but it is not evident on the I_d-V_g curves because of the thickness of gate dielectric is only 2 nm. Most significantly, the off-state leakage current raises two to three orders after EUV irradiation. It is primarily due to interface-trapped charge in the field oxide of STI.

3-3-3 Radiation Damage Effect on Different Radiation Source

Similar to the sub-section 3-2-3, we discuss the radiation damage effect on the state-of-the-art nMOSFET after 10 keV X-ray irradiation in this sub-section. Fig. 3-20 shows the I_d-V_g curves of nMOSFET after 10 keV X-ray irradiation to a dose of 1000 mJ/cm^2 and 2500 mJ/cm^2. Table 3-6 lists the electrical characteristics. The V_{th} shift and S.S. degradation also occur, and they are not easily visible on the I_d-V_g curve, too. The magnitude of the V_{th} shift is about 1 to 6 mV, and the average S.S. degradation is about 3%. The off-state leakage raises one order on at a total dose of 2500 mJ/cm^2, and only rises two to three times at a dose of 1000 mJ/cm^2. Fig.3-21 compares the off-state leakage currents after EUV and 10 keV X-ray irradiation. We can see the variation between different radiation sources and the dose effect clearly.

We calculate the probability of X-ray passing through the field oxide according to Eq. 2-3. The attenuation length in SiO_2 of EUV and 10 keV X-ray are 9.97×10^{-2} μm and 252.14 μm, respectively. We assume all of the radiation is normally incident. The percentage of photons absorbed by the field oxide is 77.78% for the EUV and 0.06% for the 10 keV X-ray. It means that almost all of the X-ray penetrates the field oxide. Although the energy of X-ray is 110 times larger than EUV; however, the percentage of absorption for EUV is 1296 times larger than X-ray. As a result, the radiation damage effect for the EUV is more severe than the 10 keV X-ray. This result is the same as that on the MIS capacitors, and can be verified each other.

3-3-4 Recovery Property on nMOSFET

The radiation damage effect on the state-of-the-art nMOSFET has been identified. We observe the recovery property in this sub-section. Similarly, we store the samples at room temperature for a long time, the damages still have not been repaired entirely, so we anneal the samples by a backend vacuum annealing furnace at 400 ℃ for 30

minutes. Fig. 3-22 shows the I_d-V_g curves, and Fig. 3-23 shows the recovery properties of V_{th}, S.S., and off-state leakage current after EUV irradiation, after storing the samples at room temperature for 20 days and 50 days, and after 400℃/30 minutes vacuum annealing. First, we check the recovery property of V_{th} shift and S.S. degradation. After storing the samples at room temperature dozen of days, the recovery of V_{th} and S.S. is not evident. However, after 400℃/30 minutes vacuum annealing, the V_{th} and S.S. recover obviously both at the dose of 1000 mJ/cm^2 and 2000 mJ/cm^2. Besides, we notice that the reversional levels of V_{th} and S.S. are limited not only after storing dozen of days but also after 400 ℃ annealing. On the one hand, the degree of radiation damage effects is very weak in the ultrathin gate dielectric; on the other hand, the trapped charges in the ultrathin gate dielectric can easily exchange charges with silicon substrate. Next and most importantly, we focus on the recovery property of the off-state leakage current because of the increment of off-state leakage current can cause additional static power consumption. Hence we should consider it cautiously. After storing the samples at room temperature for 20 days and 50 days, the self-annealing effect on the off-state leakage current is obvious because the field oxide is thick enough; however, the samples have not been repaired entirely. After a 400℃/30 minutes vacuum annealing, we can see that the leakage current recover to the level before irradiation or even better. This result implies that high temperature annealing can effectively repair the radiation damages. The recovery mechanisms have been described in the sub-section 3-2-4. With the same method, we also observe the recovery property of nMOSFET after 10 keV X-ray irradiation. Fig. 3-24 shows the I_d-V_g curves, and Fig. 3-25 shows the recovery properties. The results are absolutely the same with the EUV experiment.

To summarize, the V_{th} shift, S.S. degradation, and off-state leakage current may recover with time at room temperature, but the rate is relatively slow and it does not seem to repair the damage entirely. Nevertheless, after a 400 ℃ vacuum annealing, all

of the electrical characteristics can be repaired effectively. Using high temperature annealing is a quick method and a short cut to eliminate the damage which is caused by ionizing radiation.

3-3-5 Reliability Issue after Ionizing Radiation Irradiation

In this sub-section, we investigate the reliability of the state-of-the-art nMOSFET by PBTI measurement after EUV and 10 keV X-ray irradiation. Generally, PBTI degradation is more severe than NBTI on currently advanced device using high-k dielectric as gate dielectric; hence we have a priority to investigate the PBTI degradation after irradiation. The stress voltage is 1.5 V corresponding to about 10 MV/cm of electric field across the gate dielectric. The temperatures during stress condition are room temperature and 150 ℃. Fig. 3-26 shows the I_d-V_g curves after 10^4 s PBT stress at room temperature and 150 ℃. We observe that the V_{th} shifts toward positive in parallel, and the S.S. does not change a lot after PBT stress. It implies that the main mechanism of PBTI is due to oxide trapped charge [22, 28-31]. Besides, the V_{th} degradation at 150 ℃ is more apparent than at room temperature. The average V_{th} shift after 10^4 s PBT stress is about 30 mV at room temperature, and about 90 mV at 150 ℃. It means that high temperature stress may cause violent electro-chemical effect in the gate dielectric, and generate more defects. All of the above observations are consistent with those reported in literature.

Fig. 3-27 and Fig. 3-28 show the distribution of V_{th} degradation without irradiation, after EUV irradiation to a dose of 1000 mJ/cm^2, and after 10 keV X-ray irradiation to a dose of 1000 mJ/cm^2 at room temperature and 150℃, respectively. Fig. 3-29 compares the average V_{th} degradation without irradiation and after irradiation to a dose of 1000 mJ/cm^2 by different radiation sources. It is observed that the distributions of the V_{th} degradation after EUV and 10 keV X-ray irradiation are nearly equal to that of the

samples without irradiation both at room temperature and 150℃. In fact, this state-of-the-art nMOSFET offers an excellent radiation hardness, the gate dielectric is damaged slightly by EUV and 10 keV X-ray irradiation. The V_{th} shift is only several mV after irradiation; nonetheless, the V_{th} shift is much larger for the sample under PBT stress than exposing under ionizing radiation. For example, after a 100 s PBT stress at room temperature, the average V_{th} shift is 15 mV which is about two or three times larger than the V_{th} shift after ionizing radiation exposure. In other words, on the part of device's damage, the influence of PBT stress is much evident than ionizing radiation.

In summary, we investigate the reliability of the state-of-the-art nMOSFET by PBTI measurement with different radiation sources at different temperatures. We observe that no matter what radiation source is used, the distribution of V_{th} degradation is nearly the same both at room temperature and 150 ℃. This result implies that the ionizing radiation do not affect directly on the reliability of the state-of-the-art nMOSFET.

Table 3-1 Fabricating condition and electrical properties of MIS capacitor are summarized.

Sample ID	**T15**	**T10**	**T5**	**RTA400**	**RTA900**
Dielectric Thickness	HfO_2 15 nm	HfO_2 10 nm	HfO_2 5 nm	HfO_2 5 nm	HfO_2 5 nm
Forming Method	ALD	ALD	ALD	ALD	ALD
Interfacial Layer	chemical oxide	chemical oxide	chemical oxide	chemical oxide	chemical oxide
RTA Temperature	500 ℃	500 ℃	500 ℃	400 ℃	900 ℃
EOT(nm)	3.24	2.27	1.66	1.41	1.82
Flatband Voltage(V)	-1.36	-1.04	-0.54	-0.46	-0.36
Hysteresis	0.33 V **(Worst)**	0.25 V	38 mV **(best)**	11 mV	10 mV

Table 3-2 Comparison of △N_{ot}, △N_{it}, △N_{bt}, and hysteresis of T15, T10 and T5 samples after EUV irradiation. (a) with 275 mJ/cm^2 dose, (b) with 50 mJ/cm^2 dose.

EUV 275 mJ/cm^2	**T15**	**T10**	**T5**
ΔN_{ot} (10^{10} cm^{-2})	312~325 **(worst)**	146~153	2.95~23.5 **(best)**
ΔN_{it} (10^{10} cm^{-2})	41.1~43.3 **(worst)**	4.83~5.25	1.76~53.3 **(best)**
Hysteresis (V)	0.351~0.355 **(worst)**	0.288~0.325	0.035~0.046 **(best)**
ΔN_{bt} (10^{10} cm^{-2})	23.3~24.0	37.8~67.6 **(worst)**	1.29~4.15 **(best)**

(a)

EUV 50 mJ/cm^2	**T15**	**T10**	**T5**
ΔN_{ot} (10^{10} cm^{-2})	221~272 **(worst)**	70.1~84.7	7.27~12.4 **(best)**
ΔN_{it} (10^{10} cm^{-2})	25.3~30.3 **(worst)**	7.49~30.3	0.72~7.31 **(best)**
Hysteresis (V)	0.325~0.358	0.393~0.419 **(worst)**	0.032~0.043 **(best)**
ΔN_{bt} (10^{10} cm^{-2})	17.0~28.7	138~165 **(worst)**	0.67~3.04 **(best)**

(b)

Table 3-3 Comparison of $\triangle N_{ot}$, $\triangle N_{it}$, $\triangle N_{bt}$, and hysteresis of RTA400 and RTA900 samples after EUV irradiation. (a) with 275 mJ/cm^2 dose, (b) with 50 mJ/cm^2 dose.

EUV 275 mJ/cm^2	**RTA400**	**RTA900**
ΔN_{ot} (10^{10} cm^{-2})	0.63	2.43
ΔN_{it} (10^{10} cm^{-2})	7.01	7.47
Hysteresis (mV)	10	10
ΔN_{bt} (10^{10} cm^{-2})	0.12	0.26

(a)

EUV 50 mJ/cm^2	**RTA400**	**RTA900**
ΔN_{ot} (10^{10} cm^{-2})	1.71	0.55
ΔN_{it} (10^{10} cm^{-2})	0.67	2.07
Hysteresis (mV)	10	10
ΔN_{bt} (10^{10} cm^{-2})	0.52	0.13

(b)

Table 3-4 Comparisons of $\triangle N_{ot}$, $\triangle N_{it}$, $\triangle N_{bt}$, and hysteresis of T15 samples after EUV and 10 keV X-ray irradiation with 300 mJ/cm^2 dose.

T15 300 mJ/cm^2	**EUV (91.85 eV)**	**X-ray (10 keV)**
ΔN_{ot} (10^{10} cm^{-2})	325	280
ΔN_{it} (10^{10} cm^{-2})	124	1.06
Hysteresis (V)	0.338	0.343
ΔN_{bt} (10^{10} cm^{-2})	23.8	28.1

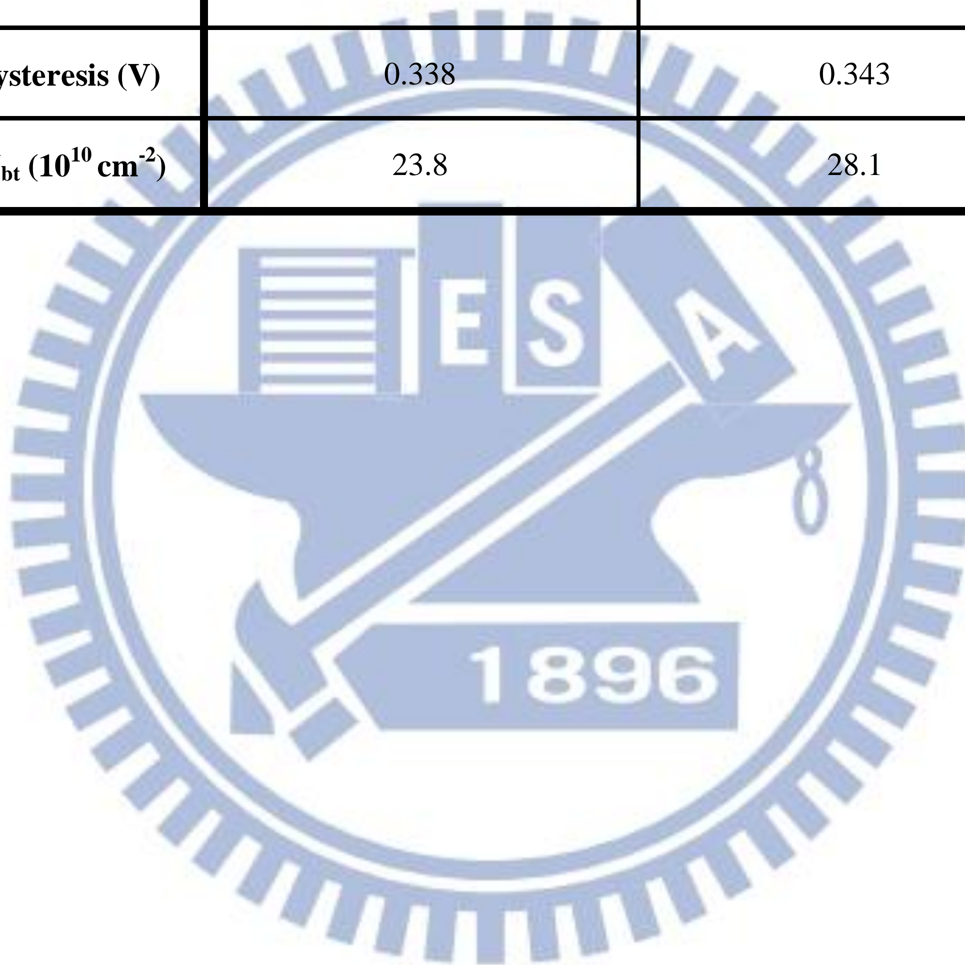


Table 3-5 Comparison of threshold voltage shift and sub-threshold swing degradation of nMOSFET after EUV irradiation. (a) with 1000 mJ/cm^2 dose, (b) with 2000 mJ/cm^2 dose.

EUV 1000 mJ/cm^2	**Vth(V)**		**Swing(mV/dec.)**	
	Before	**After**	**Before**	**After**
W=10/L=0.15	0.588	0.582	79.32	81.96
W=10/L=0.4	0.619	0.618	73.39	78.25

(a)

EUV 2000 mJ/cm^2	**Vth(V)**		**Swing(mV/dec.)**	
	Before	**After**	**Before**	**After**
W=10/L=0.35	0.622	0.618	73.60	76.05
W=10/L=0.12	0.588	0.580	78.72	80.88

(b)

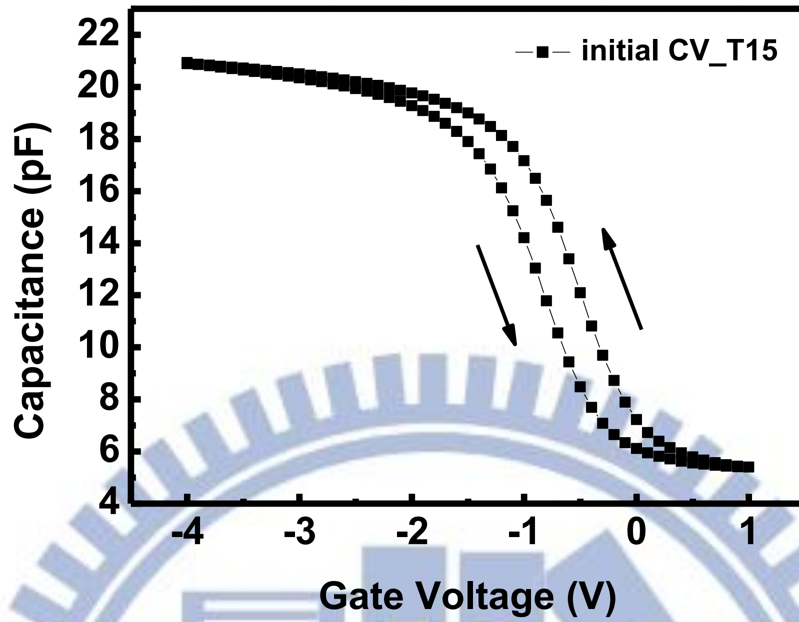
Table 3-6 Comparison of threshold voltage shift and sub-threshold swing degradation of nMOSFET after 10 keV X-ray irradiation. (a) with 1000 mJ/cm^2 dose, (b) with 2500 mJ/cm^2 dose.

X-ray 1000 mJ/cm^2	Vth(V)		Swing(mV/dec.)	
	Before	**After**	**Before**	**After**
W=10/L=0.3	0.610	0.609	73.38	76.55
W=10/L=0.35	0.615	0.613	74.29	75.69

(a)

X-ray 2500 mJ/cm^2	Vth(V)		Swing(mV/dec.)	
	Before	**After**	**Before**	**After**
W=10/L=0.5	0.624	0.618	74.85	76.94
W=10/L=0.2	0.588	0.584	78.16	80.47

(b)



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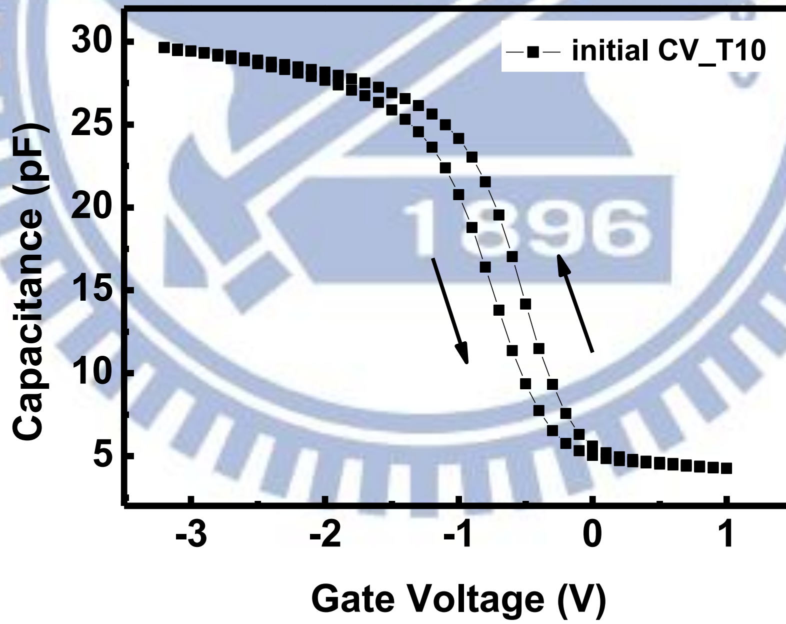

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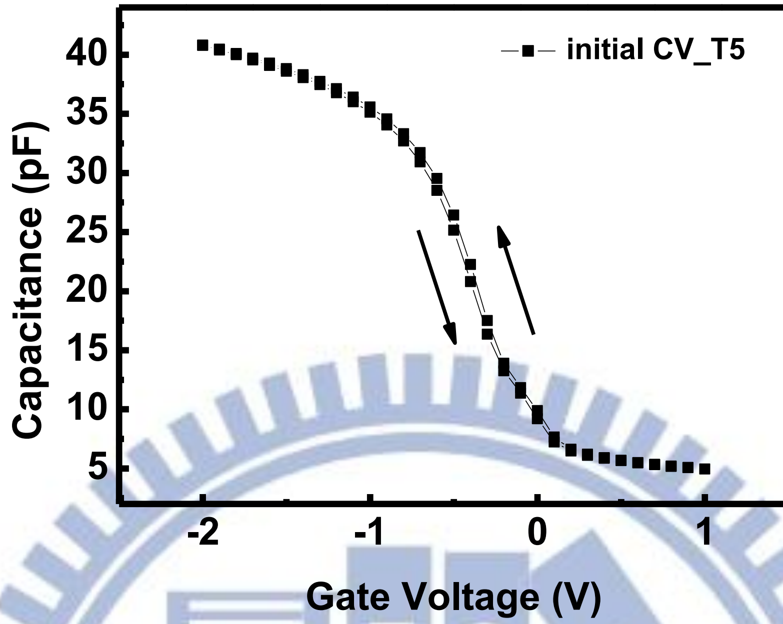

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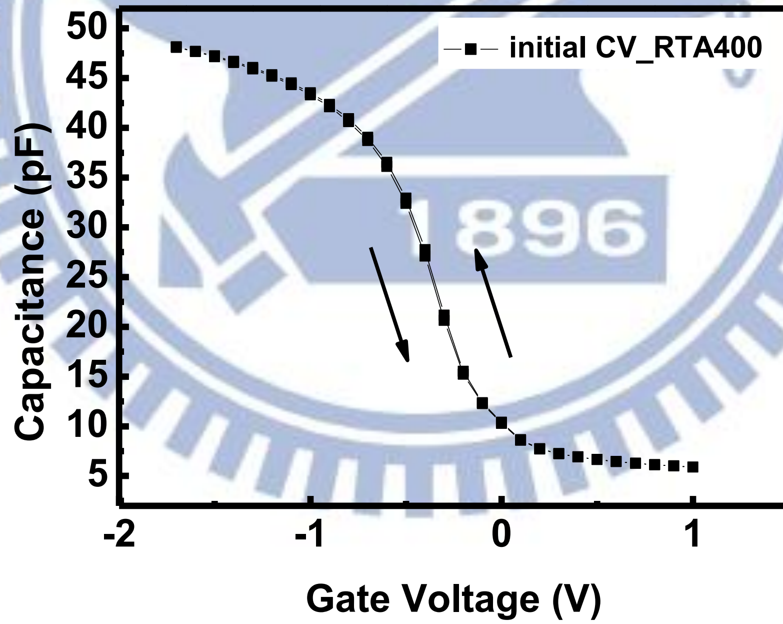

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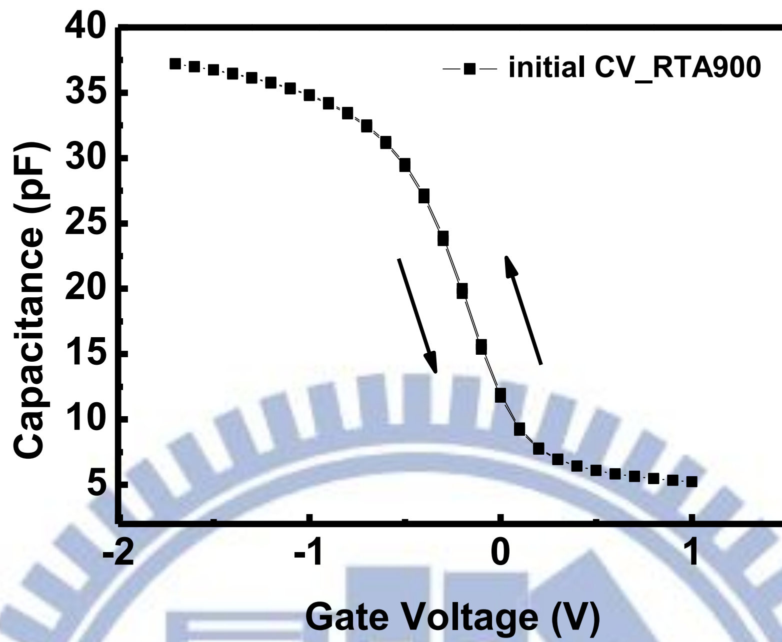
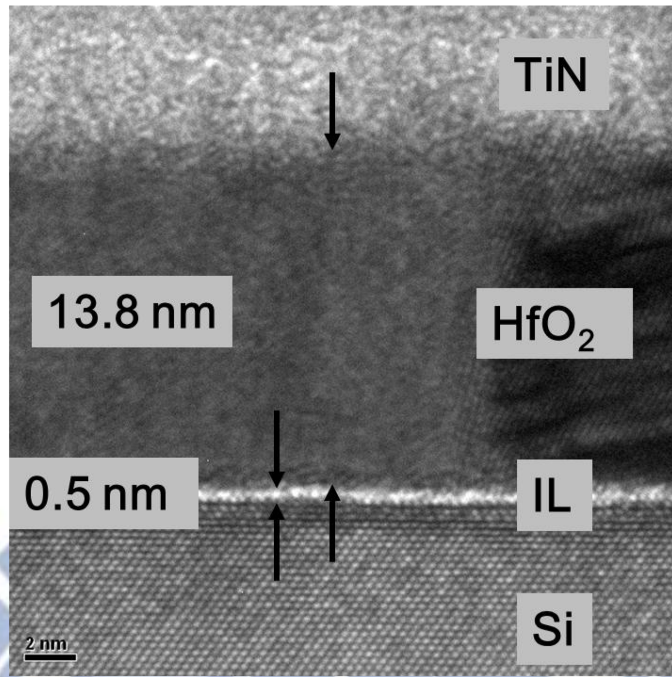
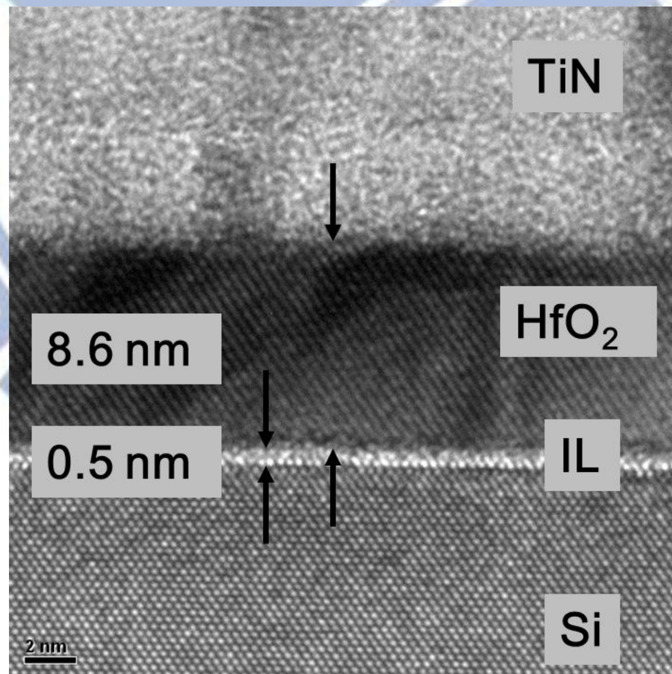


(e)

Fig. 3-1 High-frequency C-V curves of MIS capacitor without irradiation. (a) T15 sample, (b) T10 sample, (c) T5 sample, (d) RTA400 sample, (e) RTA900 sample.



(a)



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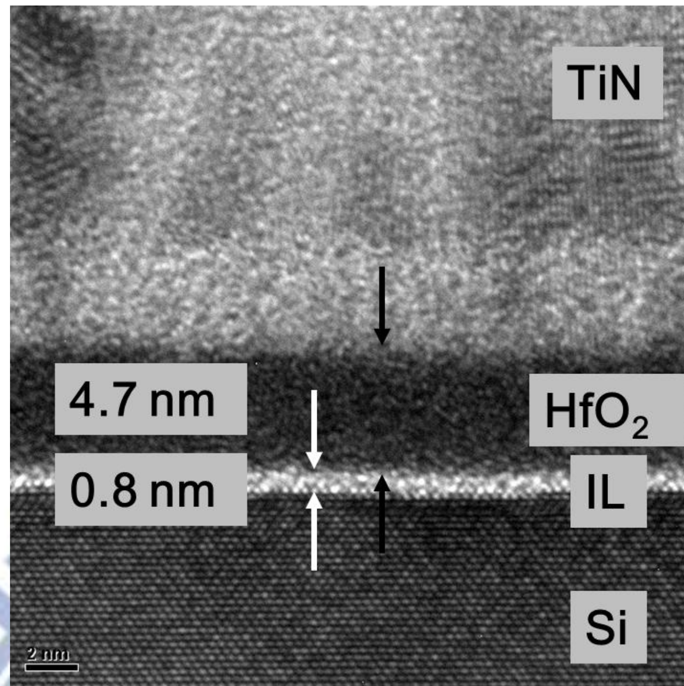

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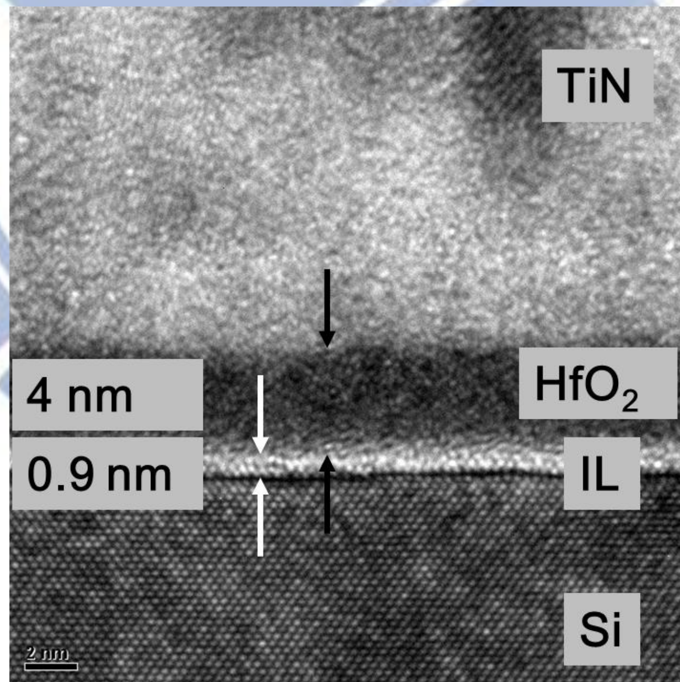

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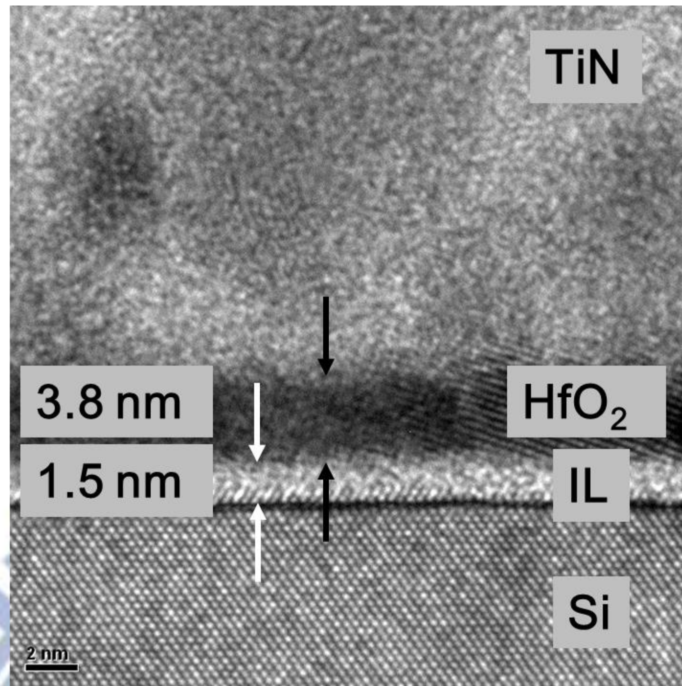
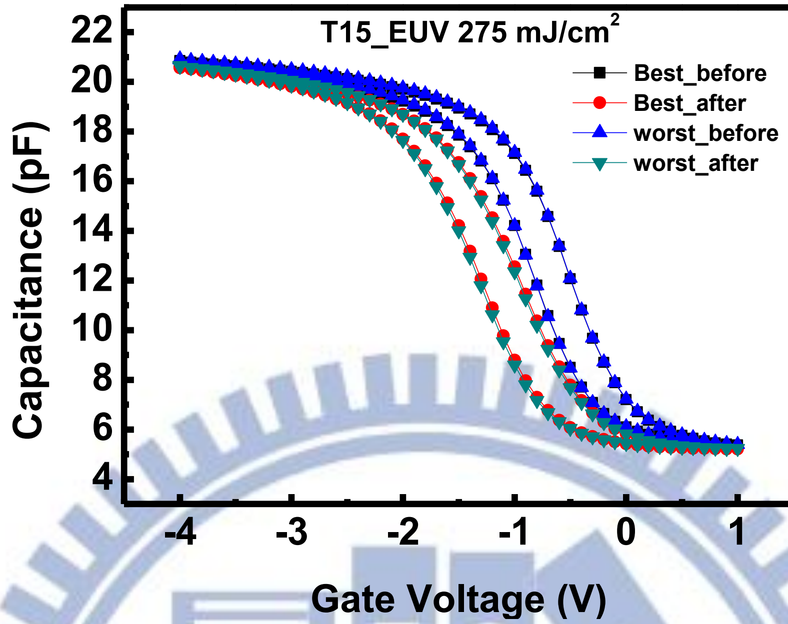
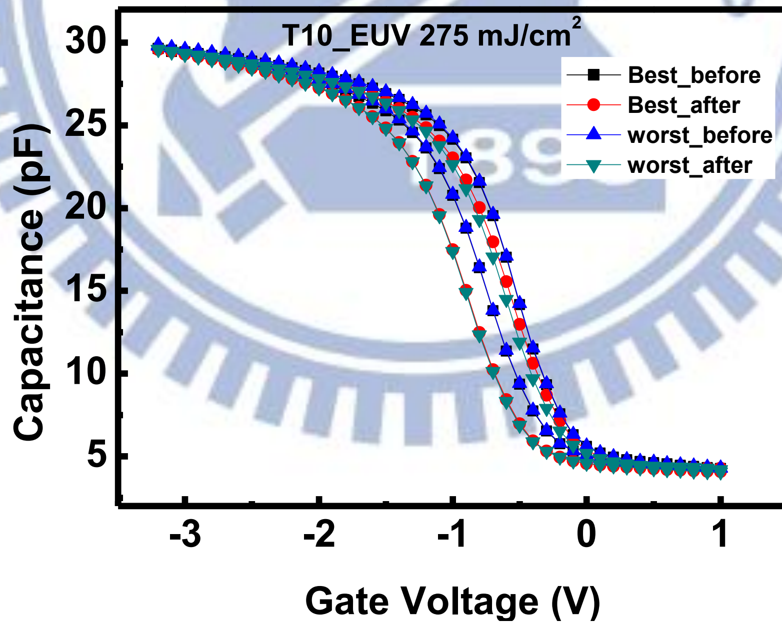


(e)

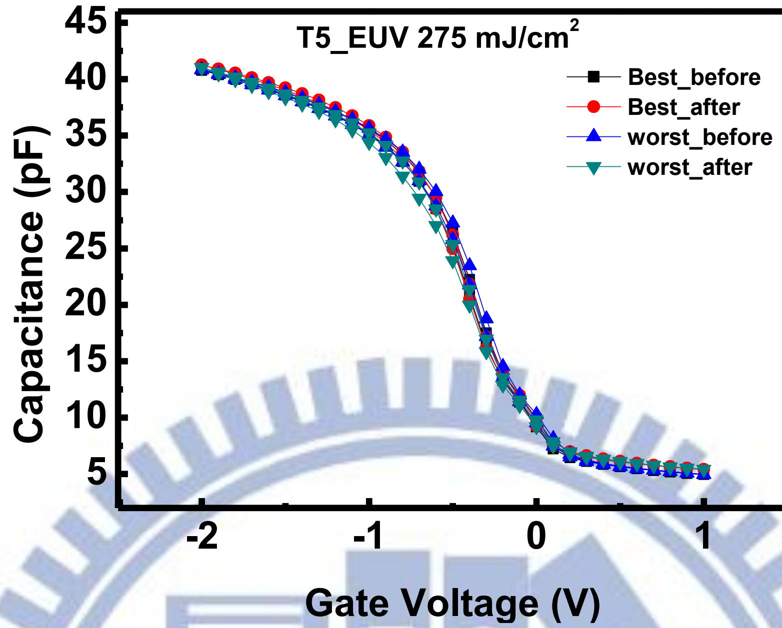
Fig. 3-2 Cross-sectional TEM micrographs of MIS capacitor. (a) T15 sample, (b) T10 sample, (c) T5 sample, (d) RTA400 sample, (e) RTA900 sample.



(a)

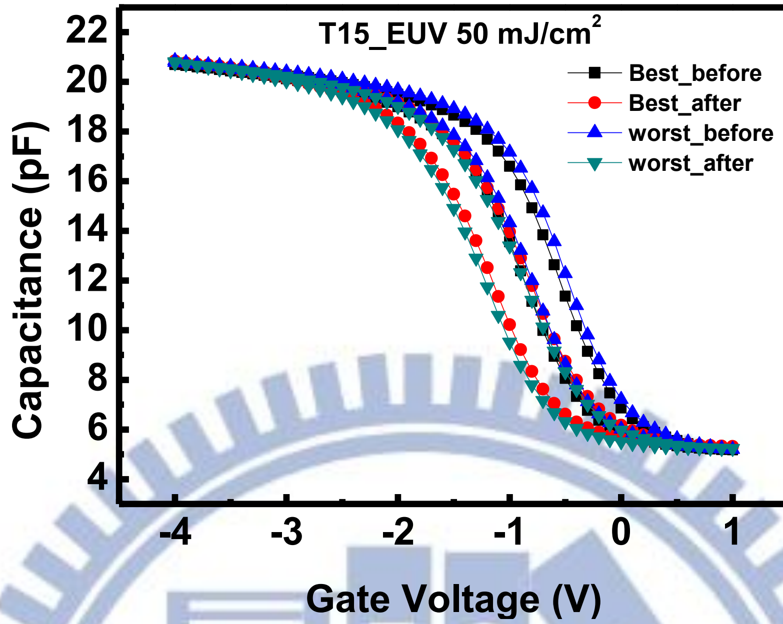


(b)

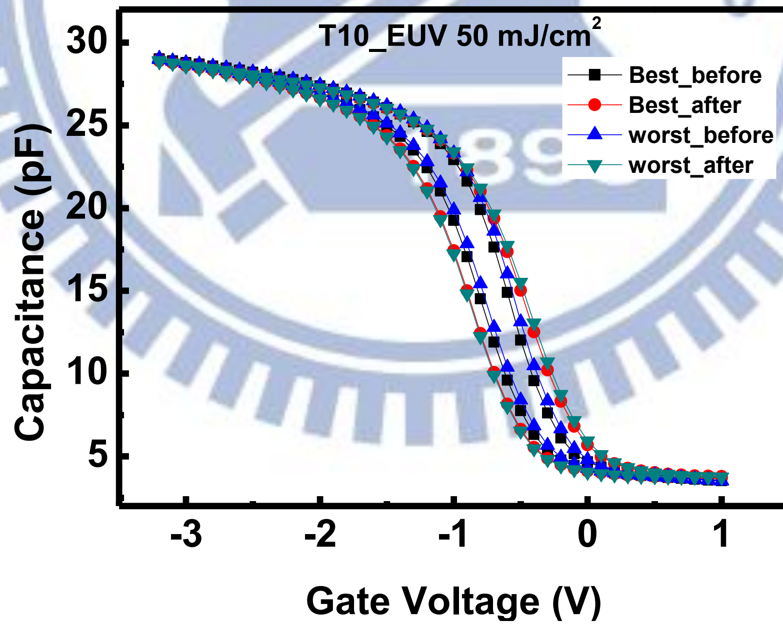


(c)

Fig. 3-3 High-frequency C-V curves of MIS capacitor after EUV irradiation with 275 mJ/cm^2 dose. (a) T15 sample, (b) T10 sample, (c) T5 sample.



(a)



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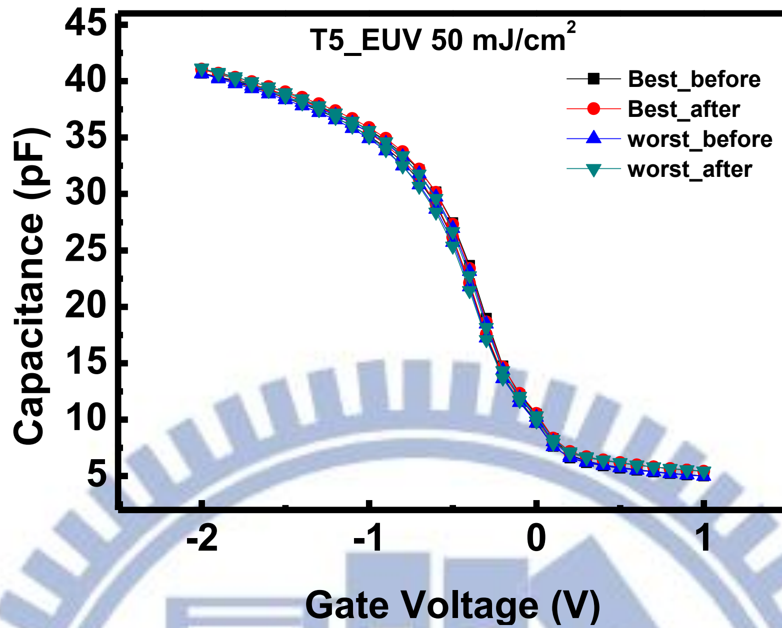
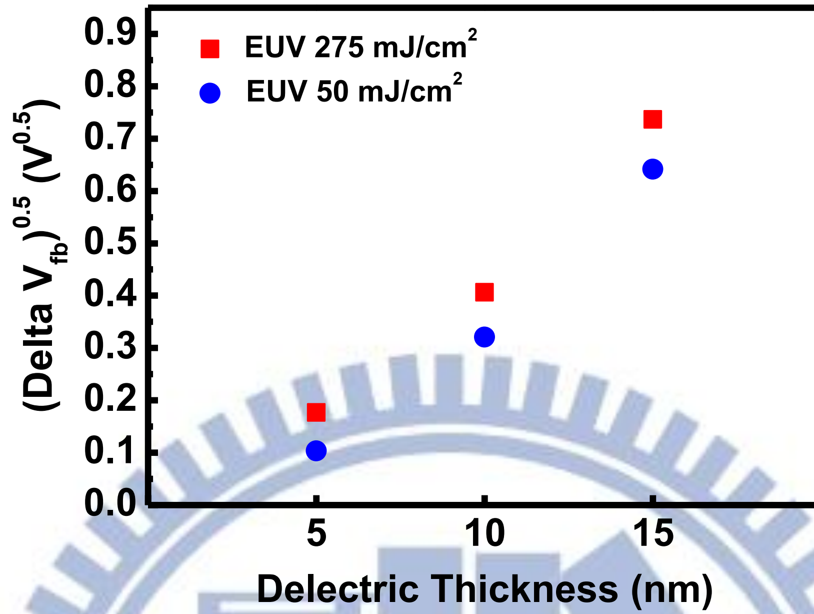
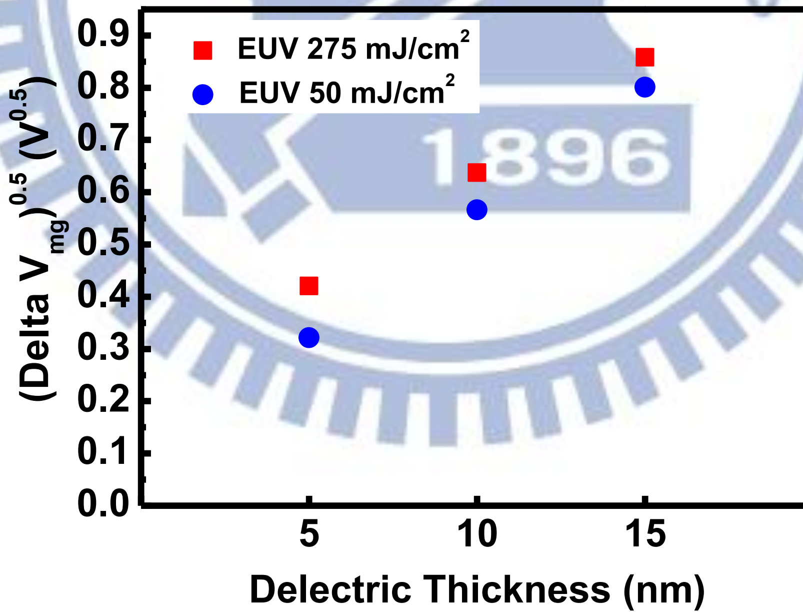


(c)

Fig. 3-4 High-frequency C-V curves of MIS capacitor after EUV irradiation with 50 mJ/cm^2 dose. (a) T15 sample, (b) T10 sample, (c) T5 sample.



(a)



(b)

Fig. 3-5 Change of flatband and midgap voltage after EUV irradiation between different dielectric thicknesses and different doses. (a) flatband voltage shift after EUV irradiation , (b) midgap voltage shift after EUV irradiation.

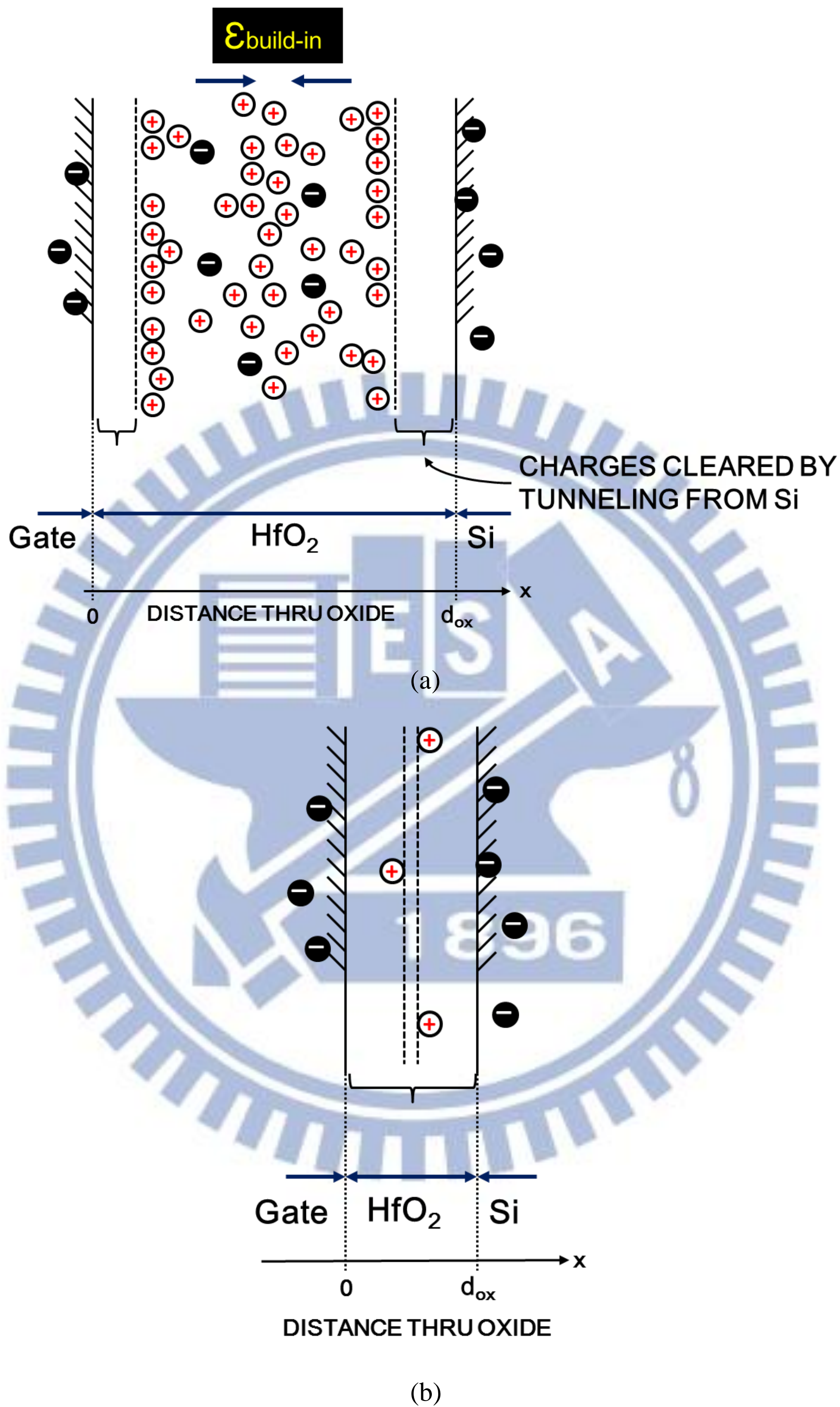


Fig. 3-6 Hole trapping and removal processes in a MIS capacitors after irradiation. (a) thicker dielectric (b) thinner dielectric.

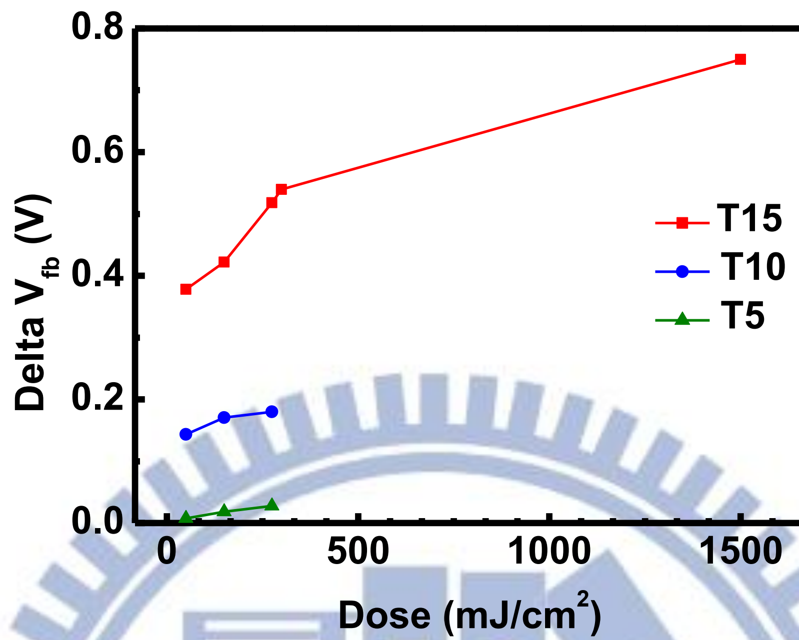
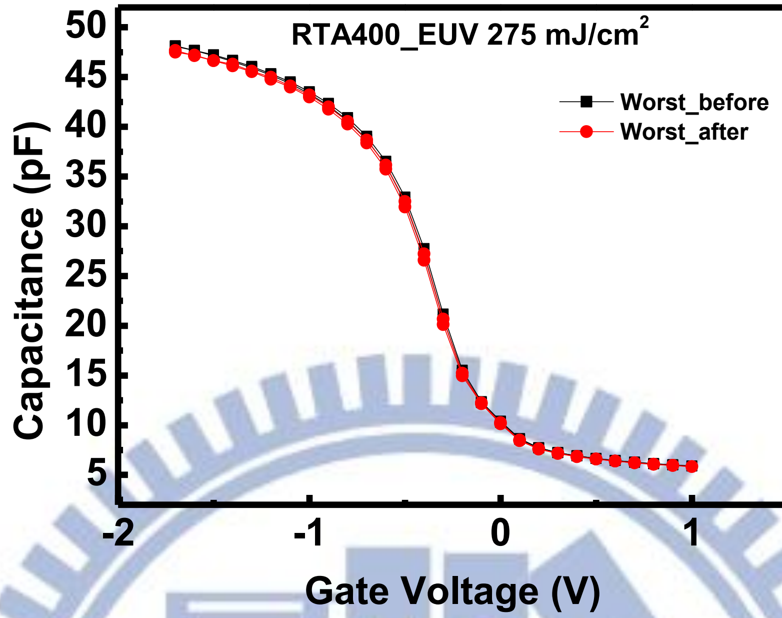
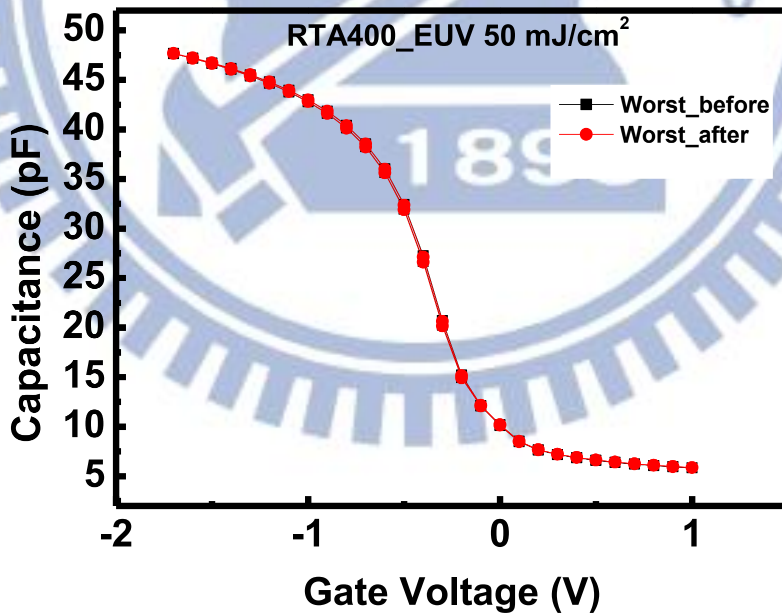


Fig. 3-7 Dose effect of T15, T10, and T5 MIS capacitors after EUV irradiation to various doses.



(a)



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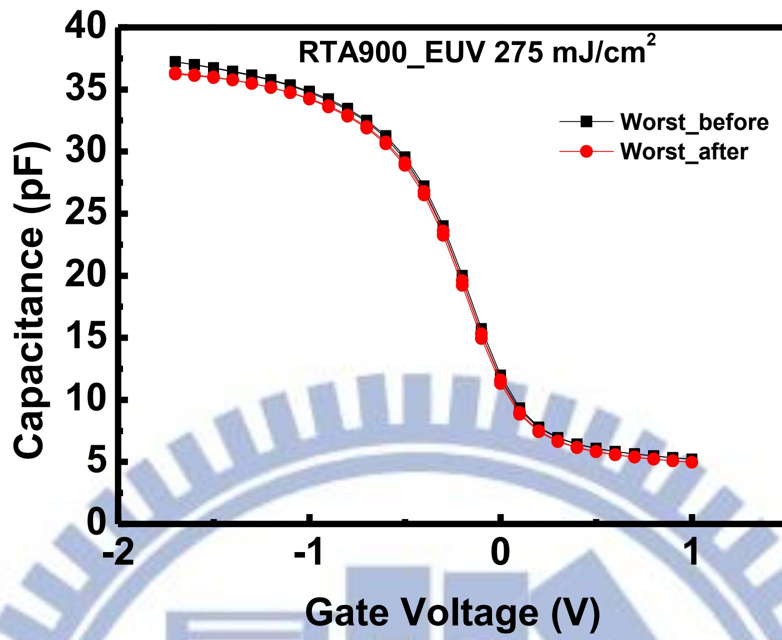

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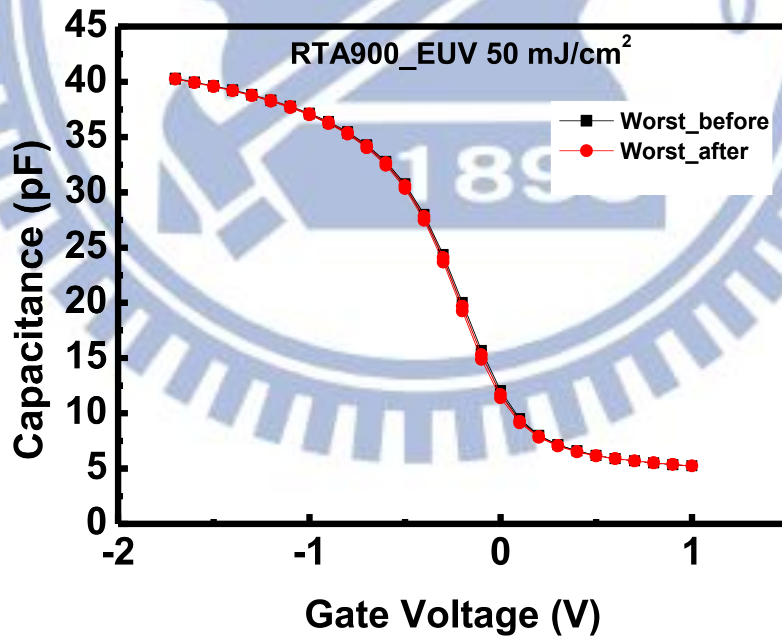


(d)

Fig. 3-8 High-frequency C-V curves of MIS capacitor after EUV irradiation. (a) RTA400 sample with 275 mJ/cm^2 dose, (b) RTA400 sample with 50 mJ/cm^2 dose, (c) RTA900 sample with 275 mJ/cm^2 dose, (d) RTA900 sample with 50 mJ/cm^2 dose.

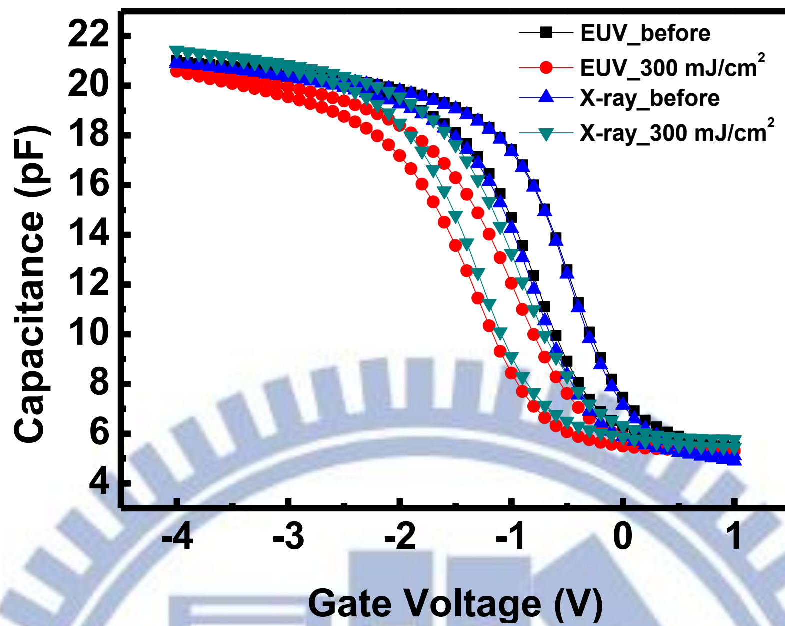
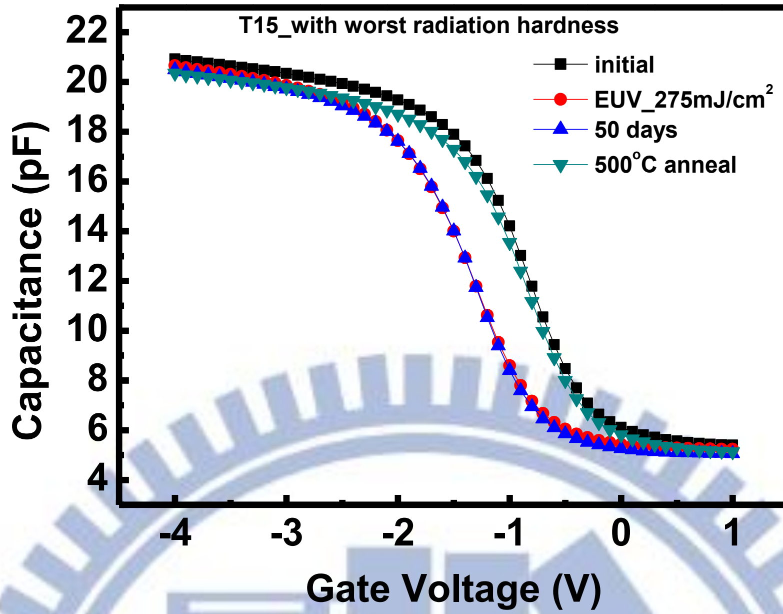
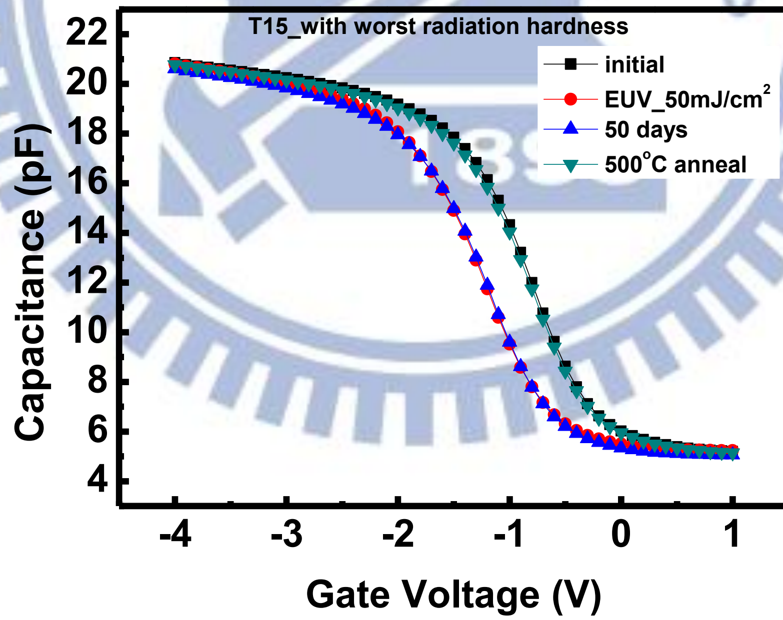


Fig. 3-9 High-frequency C-V curves of T15 sample after EUV and 10 keV X-ray irradiation with 300 mJ/cm^2 dose.



(a)



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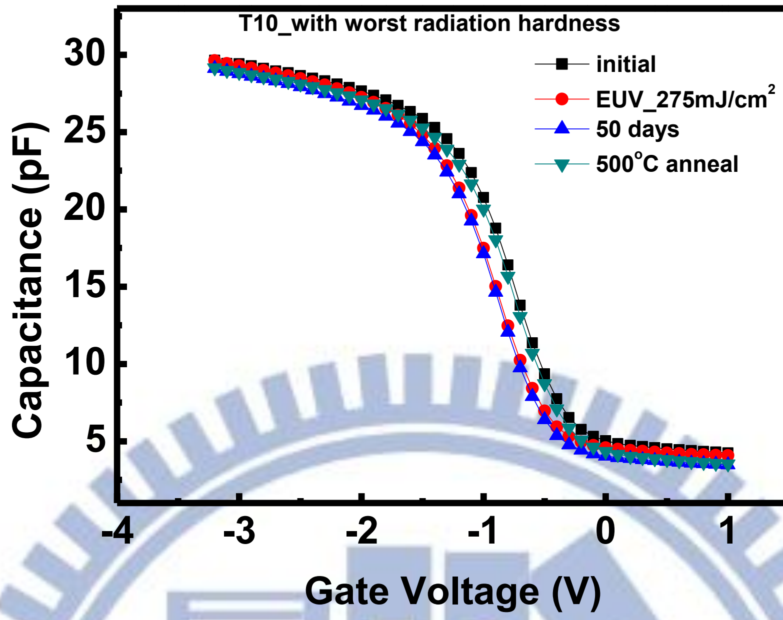

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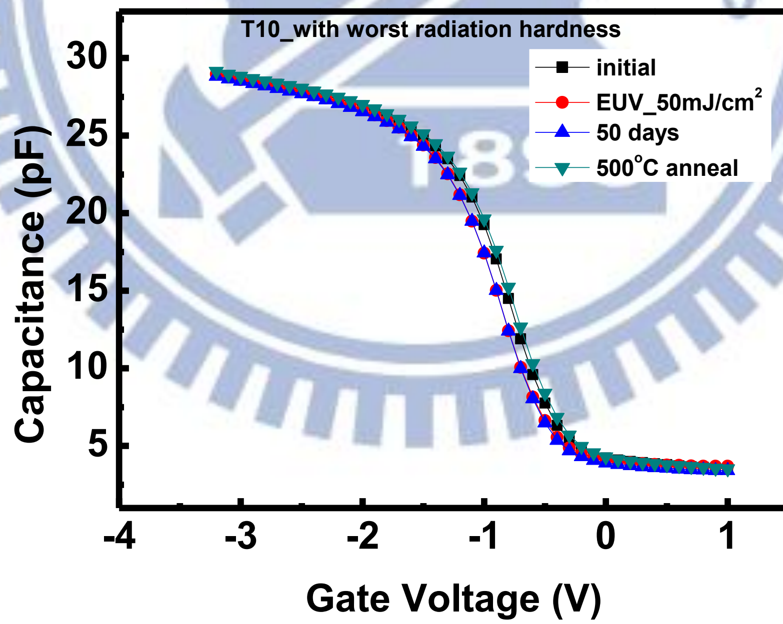

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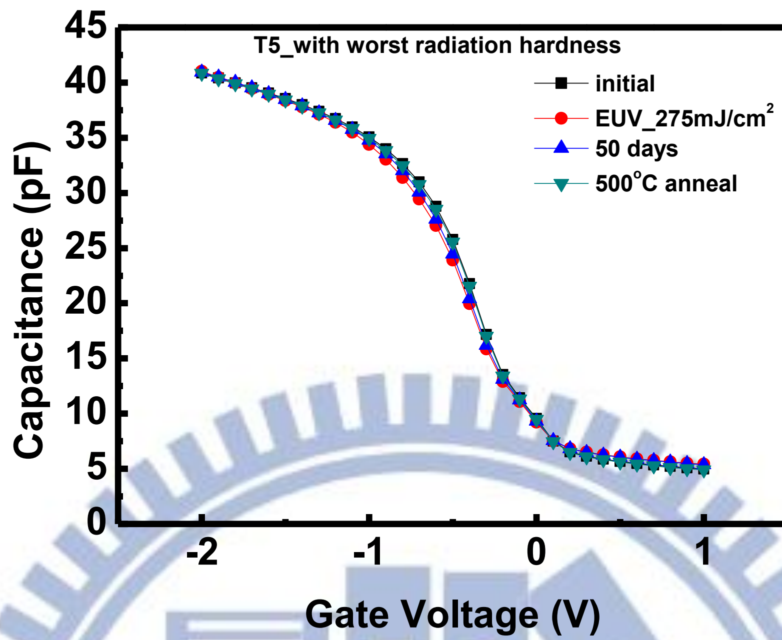
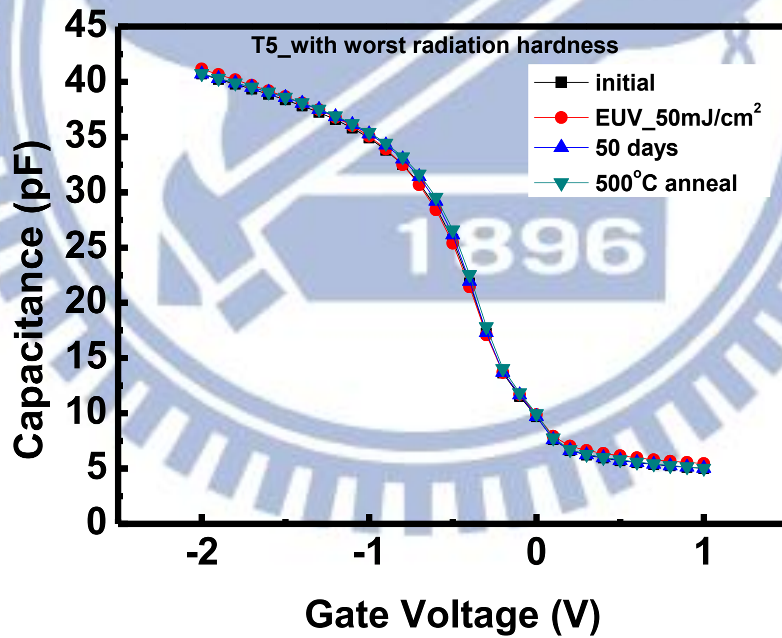
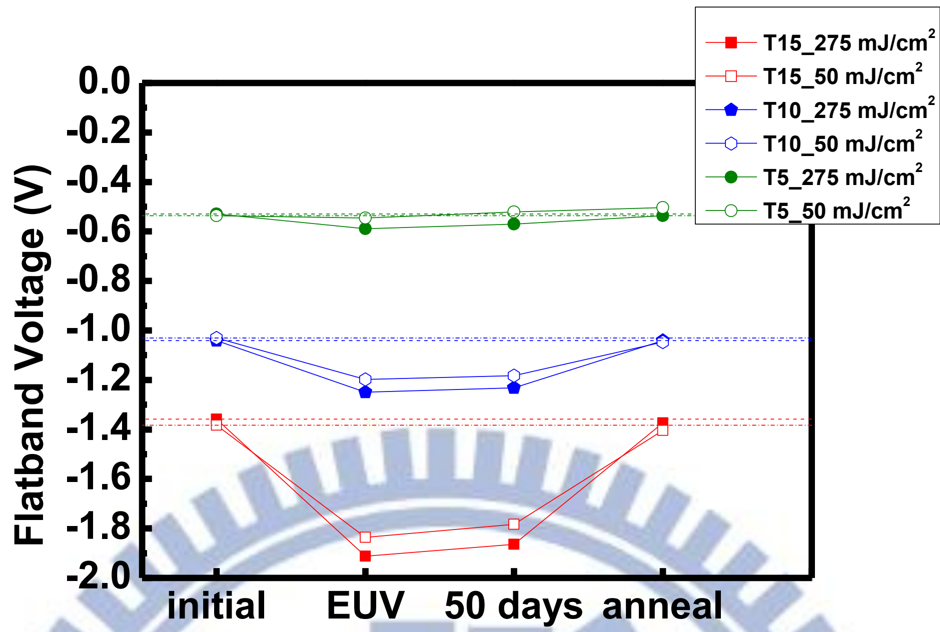


(e)

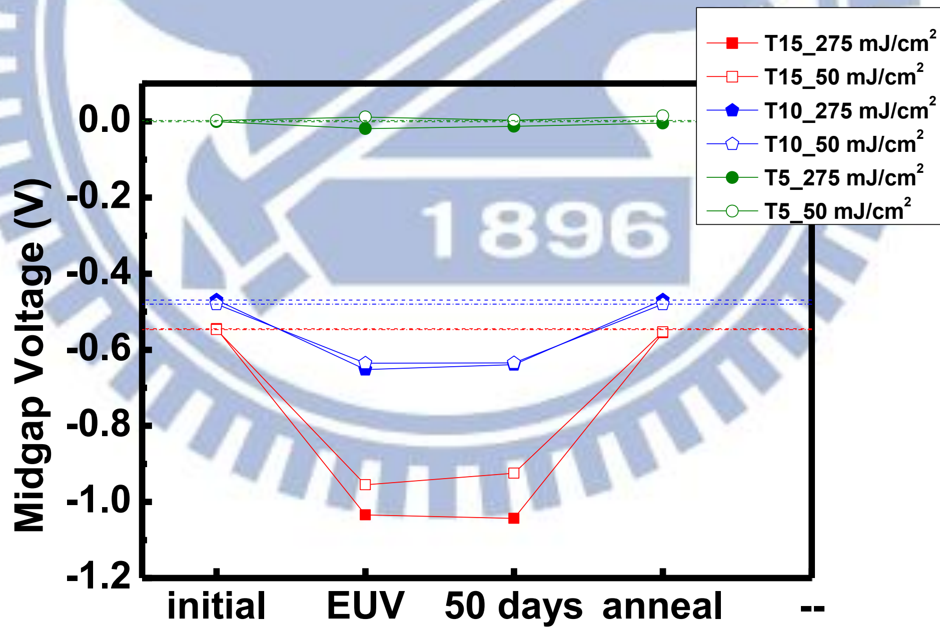


(f)

Fig. 3-10 Recovery behaviors of MIS capacitors after EUV irradiation. (a) T15 sample with 275 mJ/cm^2 dose, (b) T15 sample with 50 mJ/cm^2 dose, (c) T10 sample with 275 mJ/cm^2 dose, (d) T10 sample with 50 mJ/cm^2 dose, (e) T5 sample with 275 mJ/cm^2 dose, (f) T5 sample with 50 mJ/cm^2 dose.



(a)



(b)

Fig. 3-11 Change of electrical characteristics during recovery process after EUV irradiation. (a) flatband voltage, (b) midgap voltage.

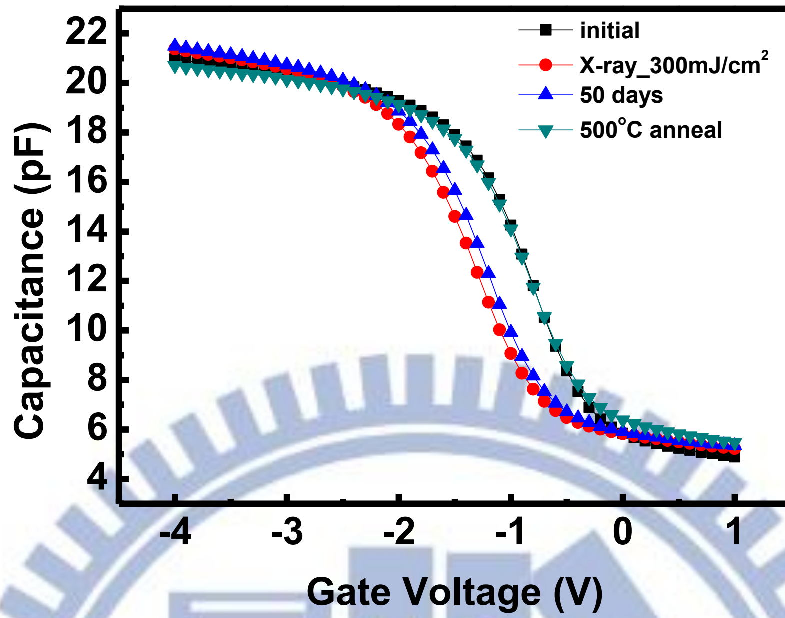
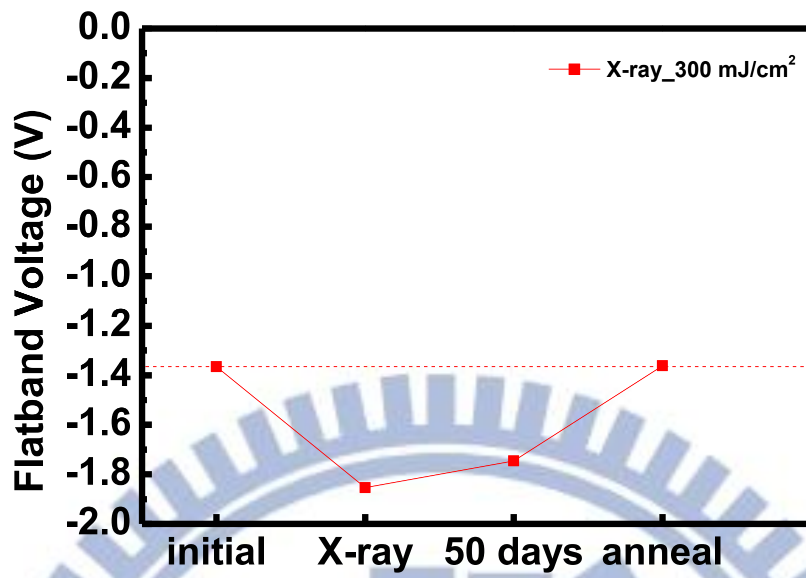
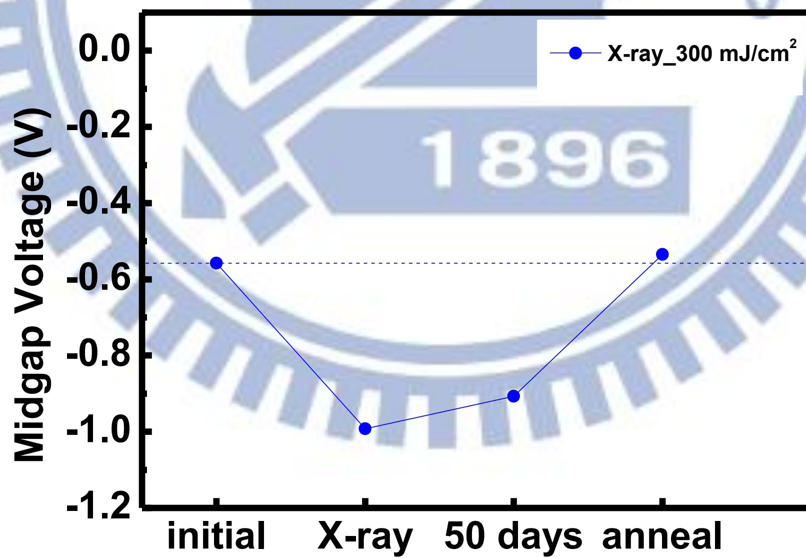


Fig. 3-12 Recovery behaviors of T15 sample after 10 keV X-ray irradiation with 300 mJ/cm^2 dose.



(a)



(b)

Fig. 3-13 Change of electrical characteristics during recovery process after 10 keV X-ray irradiation. (a) flatband voltage, (b) midgap voltage.

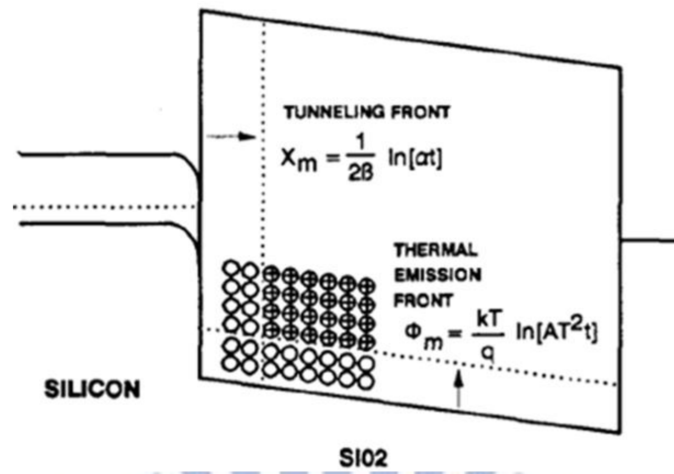


Fig. 3-14 Band diagram illustrating the combination of tunneling front model and thermal emission front model [41].

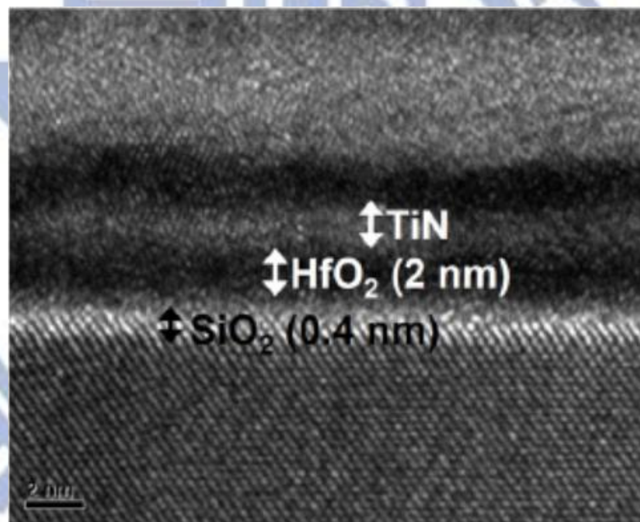
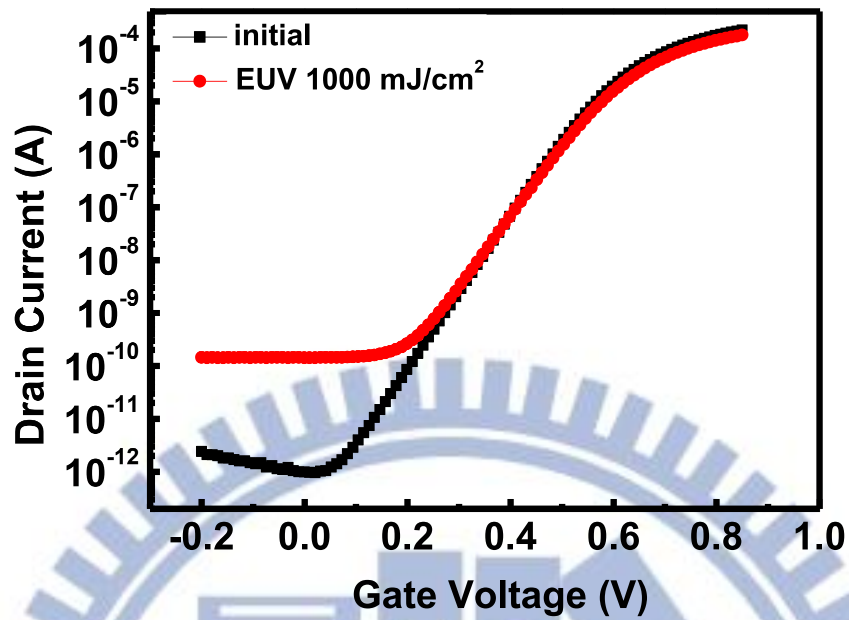
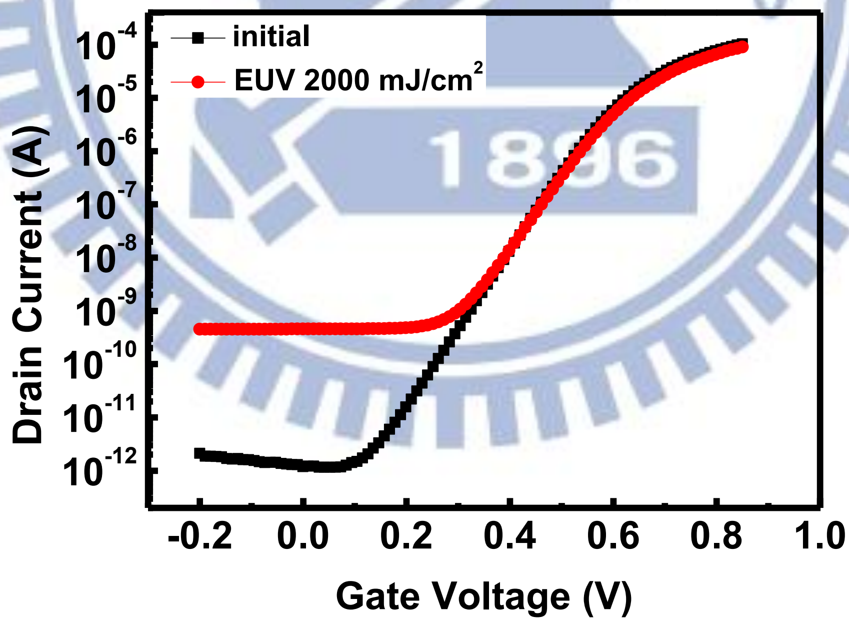


Fig. 3-15 Cross-sectional TEM micrograph of the state-of-the-art nMOSFET.



(a)



(b)

Fig. 3-16 I_d-V_g curves of nMOSFET after EUV irradiation with (a) 1000 mJ/cm^2 dose, (b) 2000 mJ/cm^2 dose.

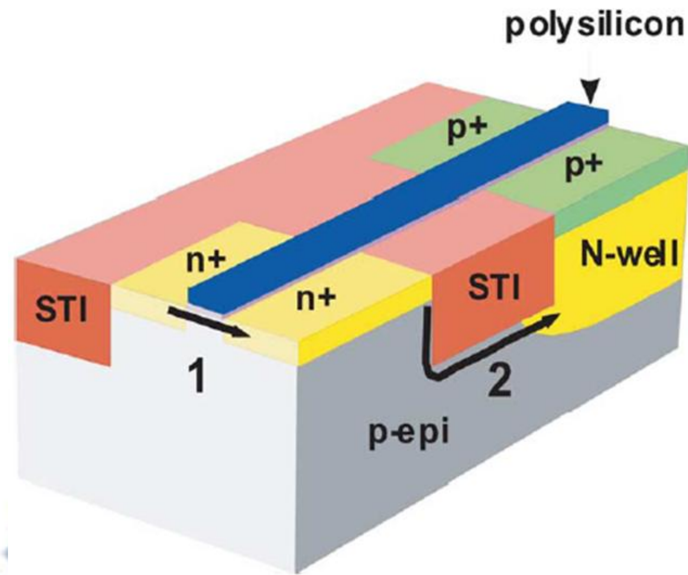


Fig. 3-17 Two possible leakage paths in a shallow trench isolation technology [42].

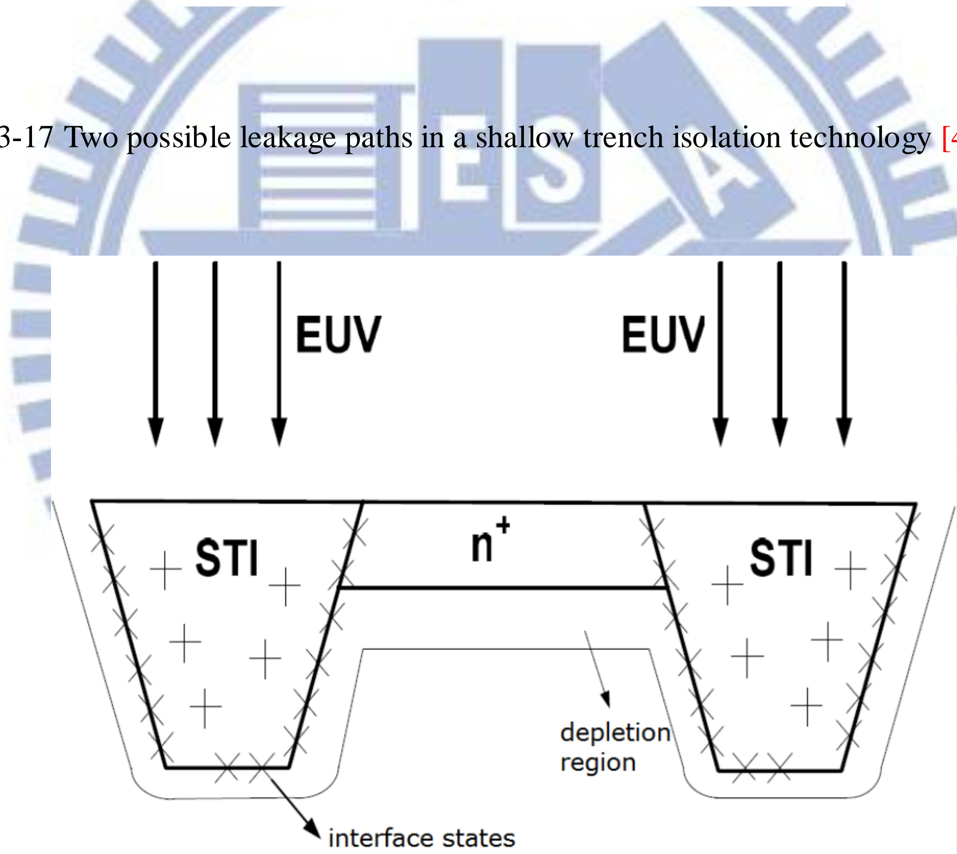


Fig. 3-18 Mechanism of the increment of the off-state leakage current after EUV irradiation [34].

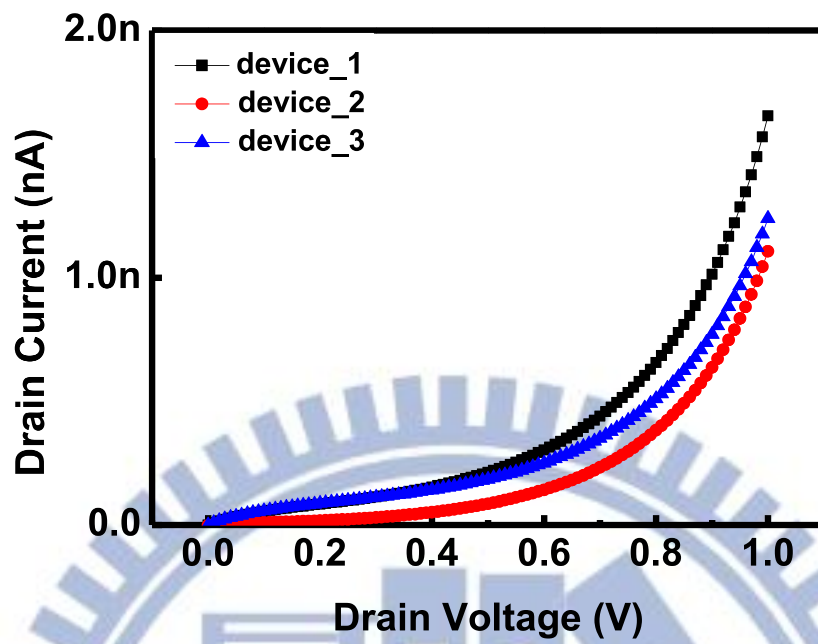
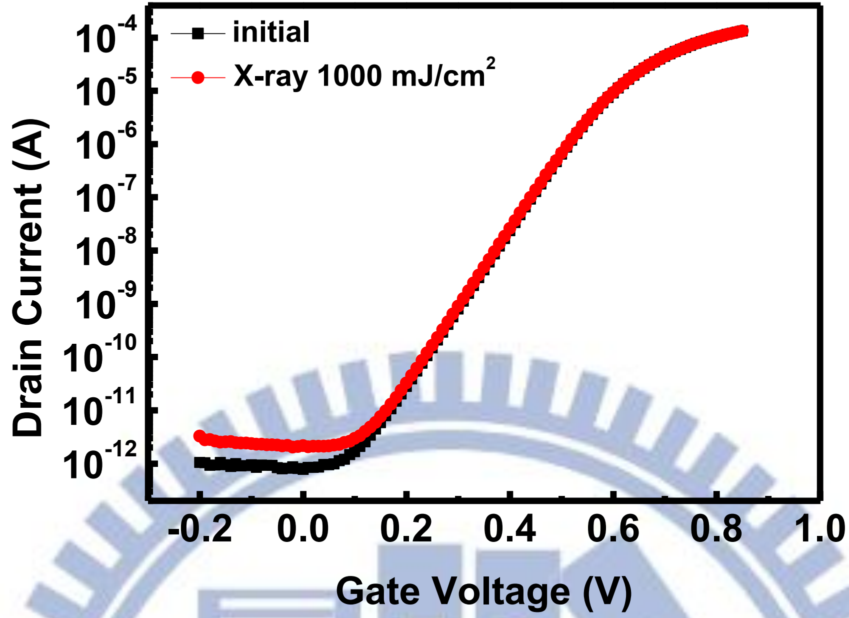
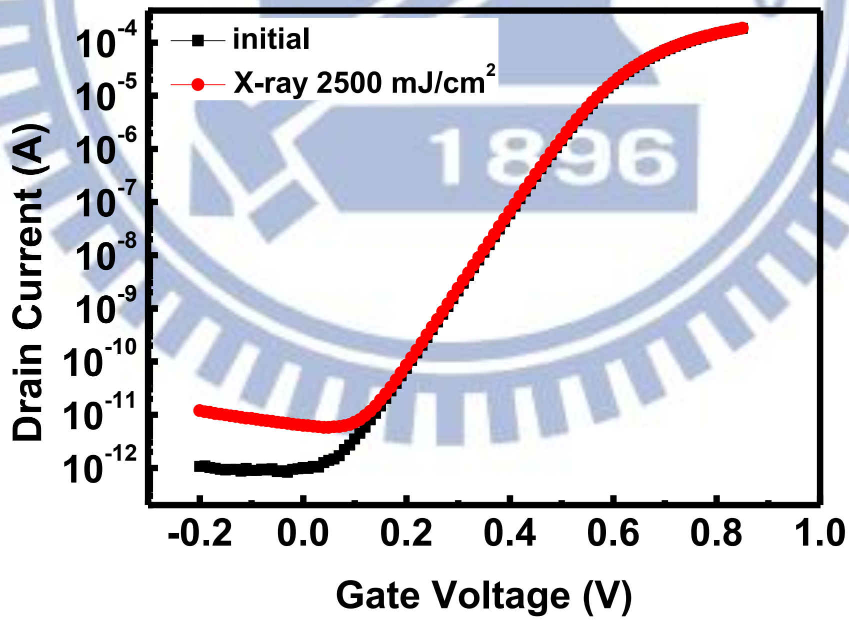


Fig. 3-19 n^+-p junction current of nMOSFET at reverse bias after EUV irradiation.



(a)



(b)

Fig. 3-20 I_d-V_g curves of nMOSFET after 10 keV X-ray irradiation with (a) 1000 mJ/cm^2 dose, (b) 2500 mJ/cm^2 dose.

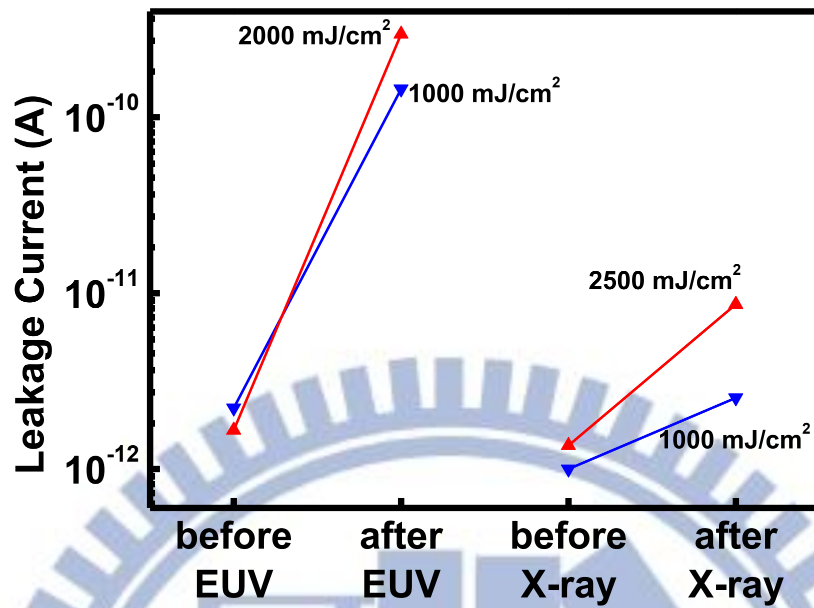
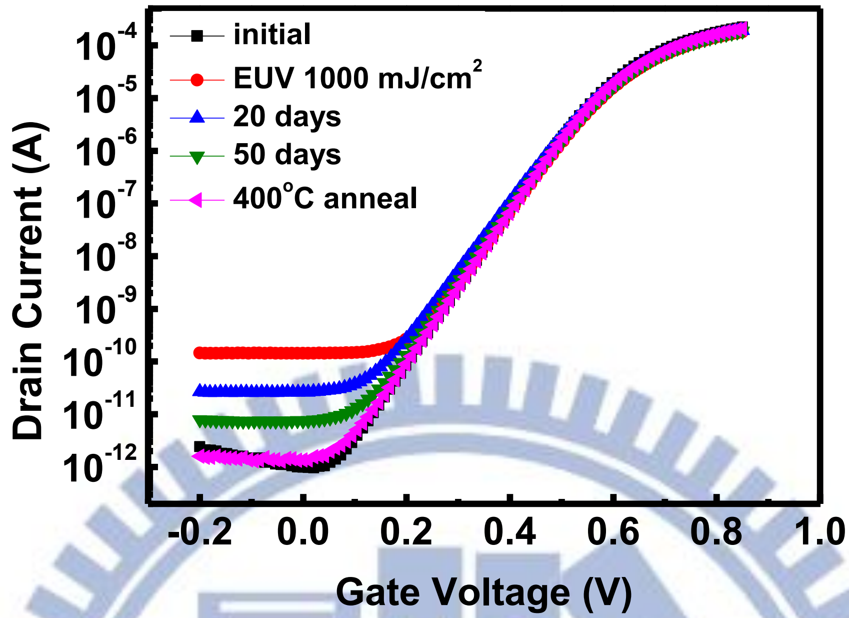
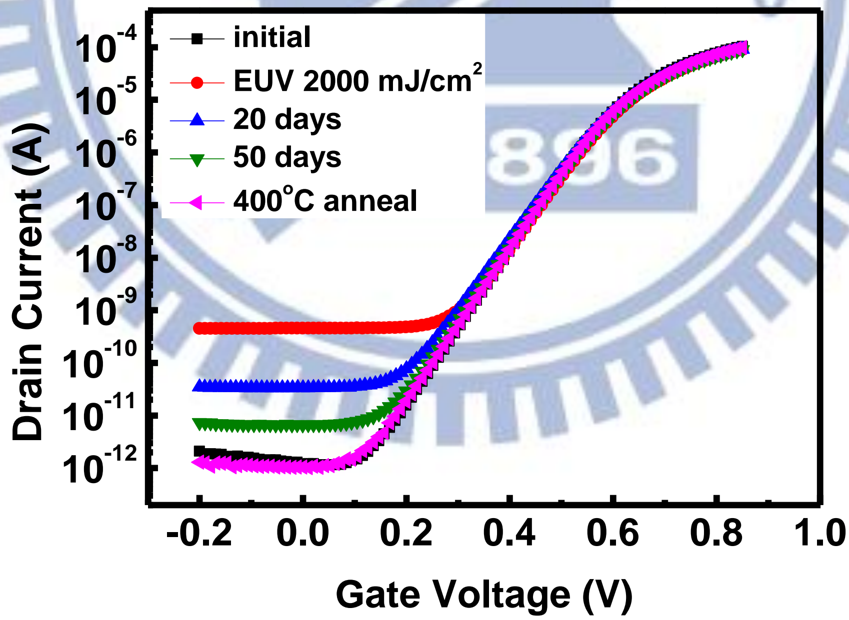


Fig. 3-21 Comparison of off-state leakage current level after EUV and 10 keV X-ray irradiation with different doses.

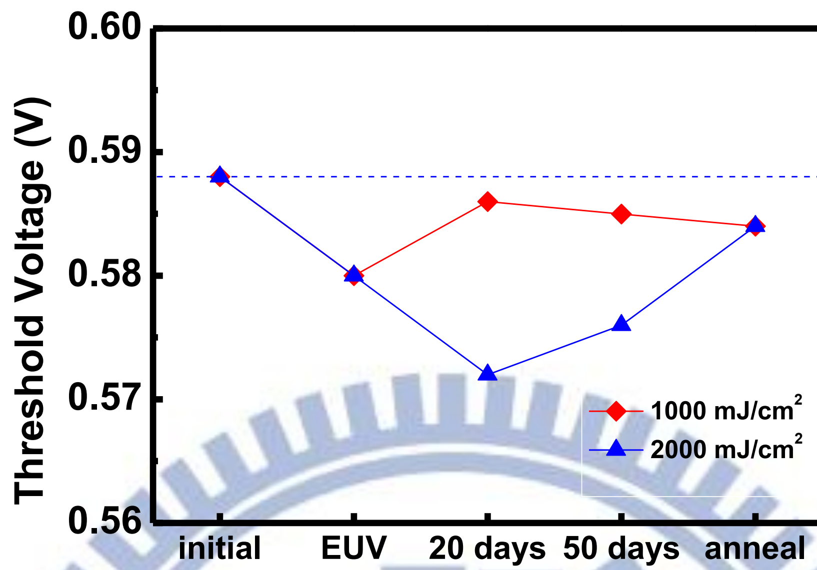


(a)

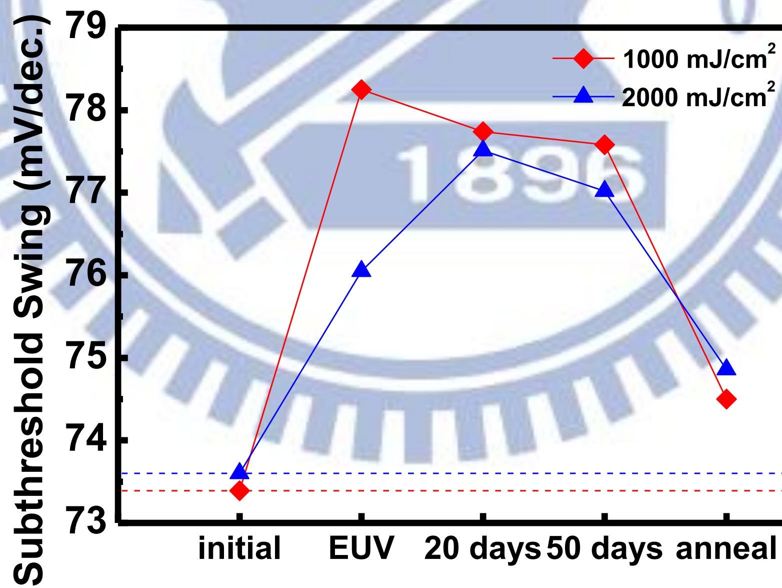


(b)

Fig. 3-22 Recovery behaviors of nMOSFET after EUV irradiation with (a) 1000 mJ/cm^2 dose, (b) 2000 mJ/cm^2 dose.



(a)



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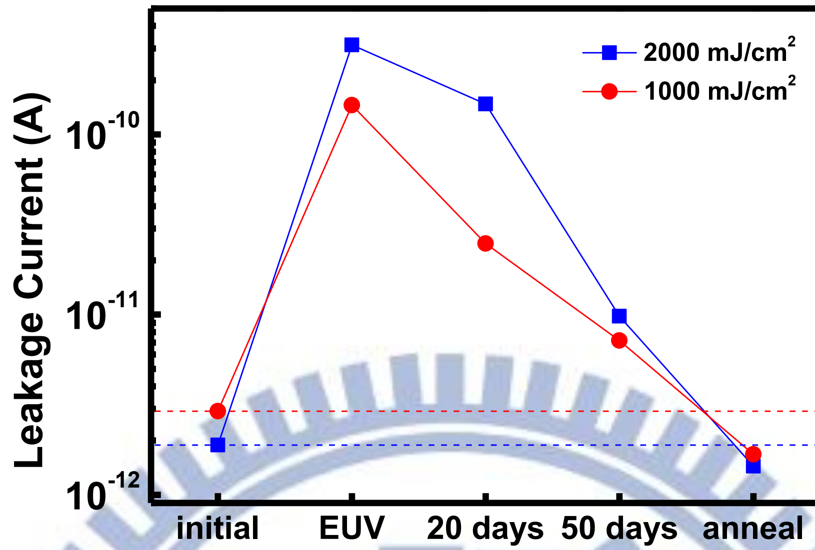
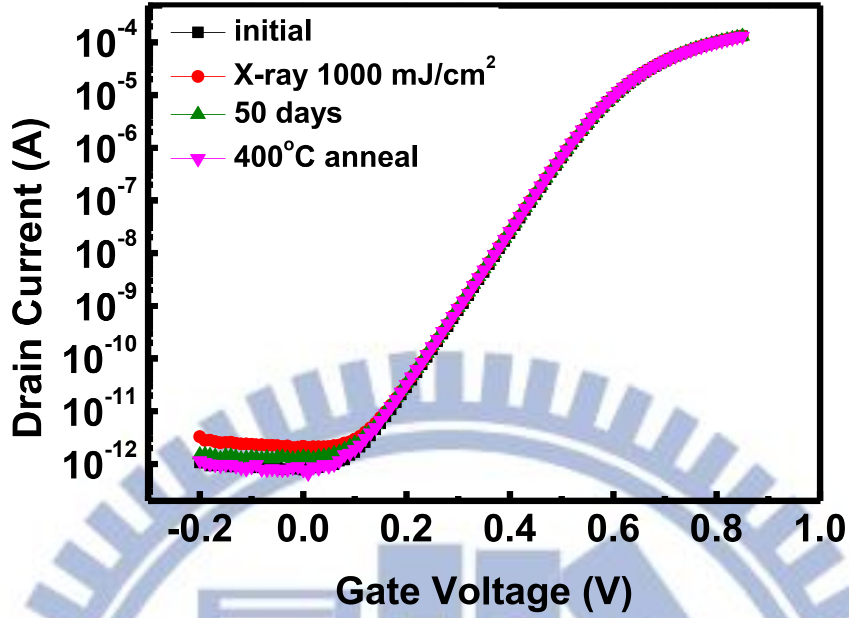
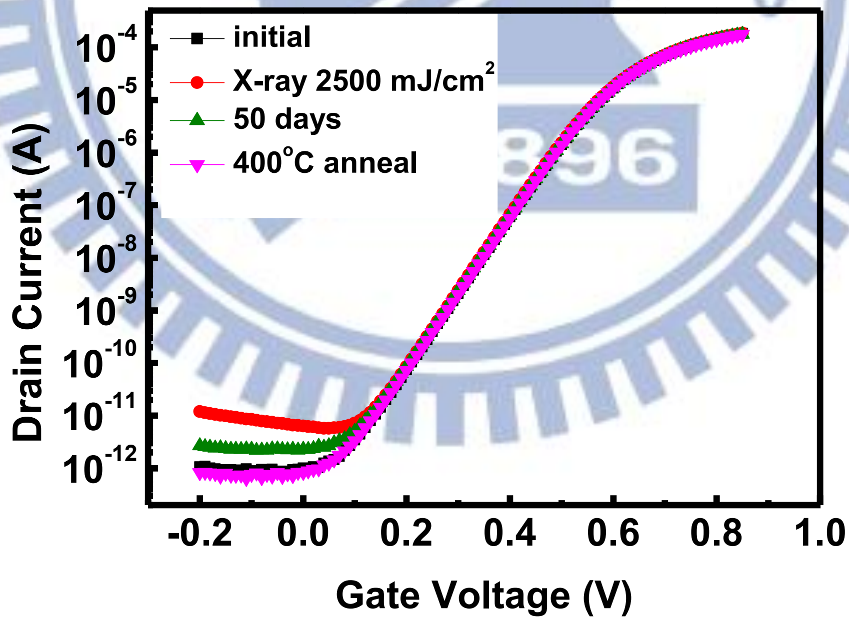


(c)

Fig. 3-23 Recovery property of electrical characteristics during recovery process after EUV irradiation. (a) threshold voltage, (b) sub-threshold swing, (c) off-state leakage current level.

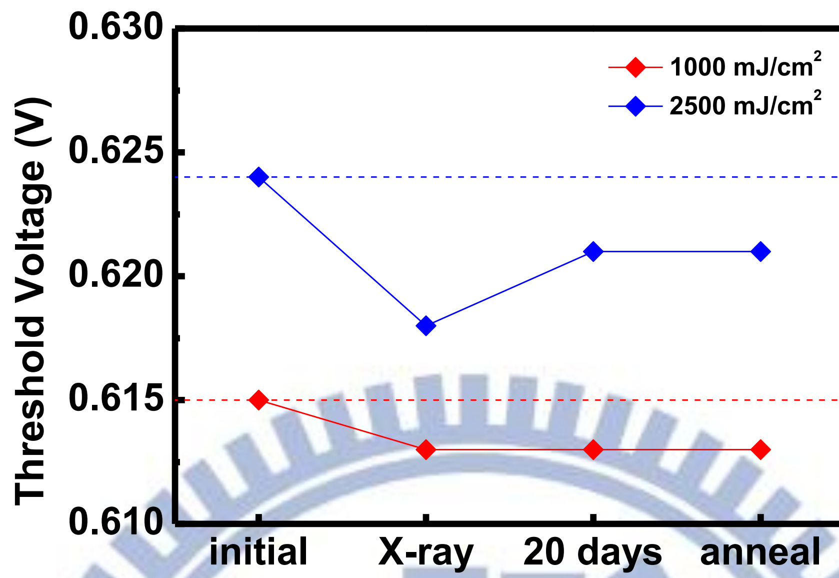


(a)

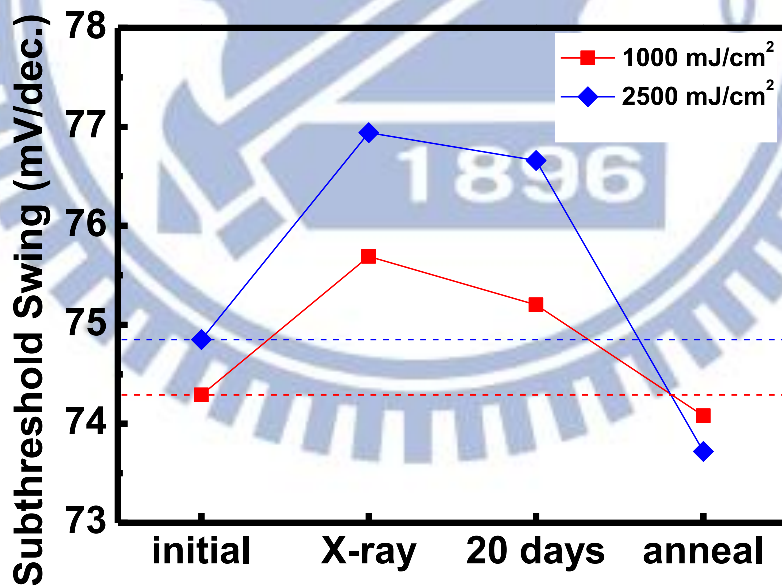


(b)

Fig. 3-24 Recovery behaviors of nMOSFET after 10 keV X-ray irradiation with (a) 1000 mJ/cm^2 dose, (b) 2500 mJ/cm^2 dose.



(a)



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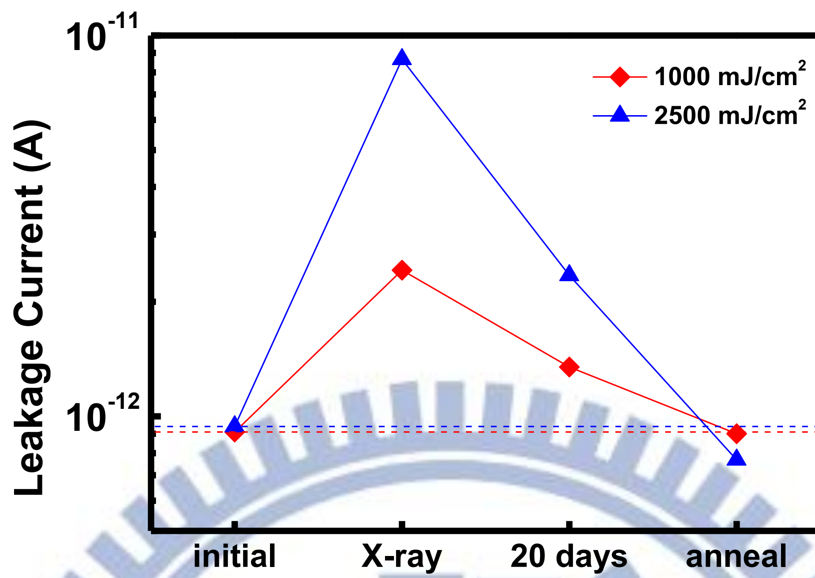
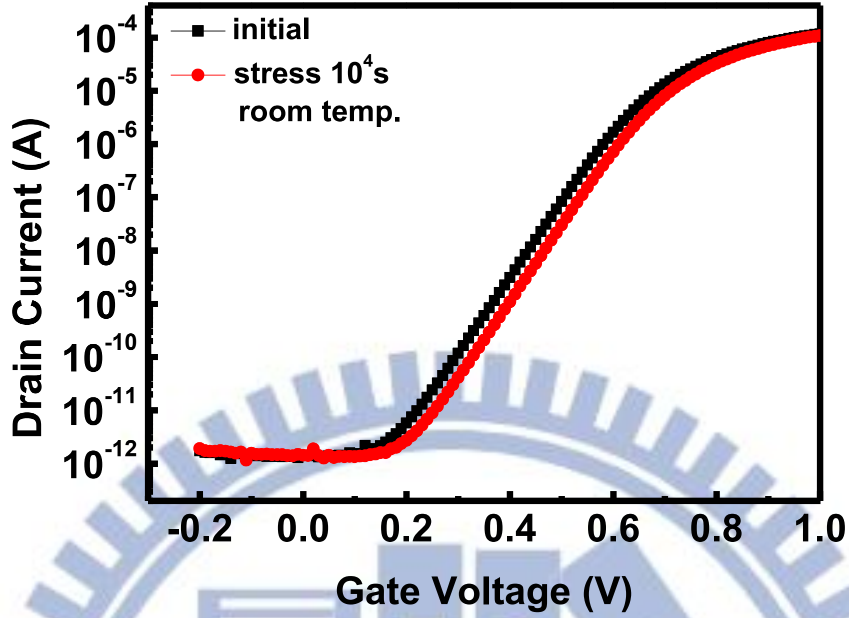
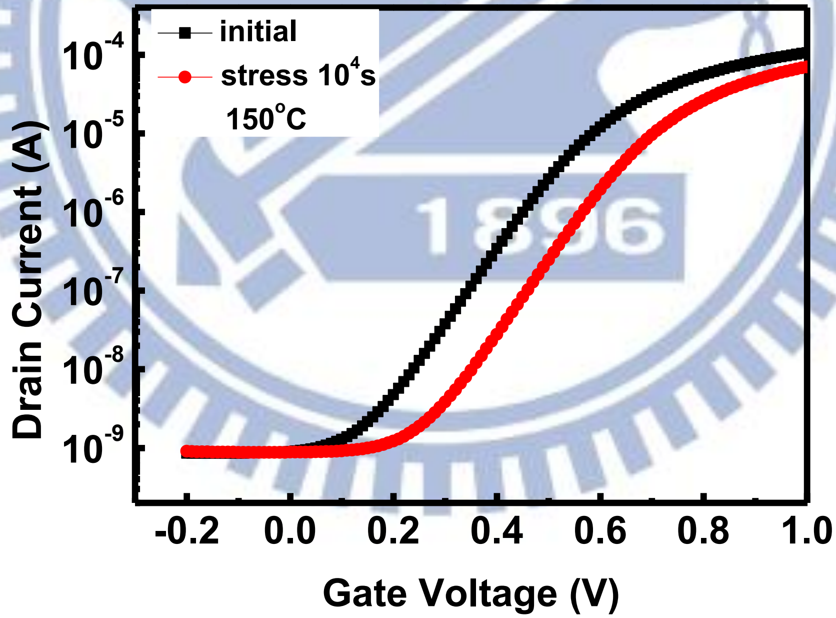


(c)

Fig. 3-25 Recovery property of electrical characteristics during recovery process after 10 keV X-ray irradiation. (a) threshold voltage, (b) sub-threshold swing, (c) off-state leakage current level.

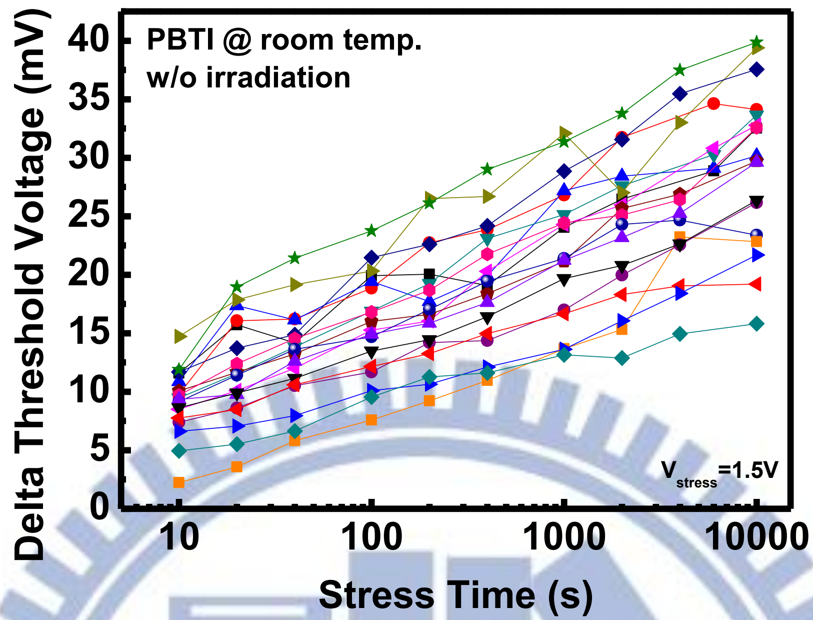


(a)

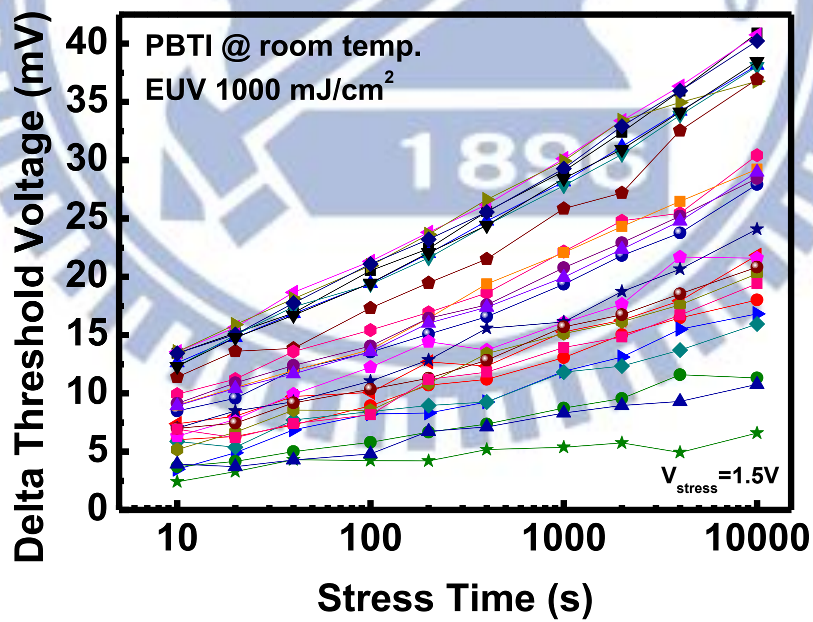


(b)

Fig. 3-26 I_d-V_g curves of nMOSFET without irradiation after 10^4 s PBT stress at (a) room temperature, (b) 150 ℃.



(a)



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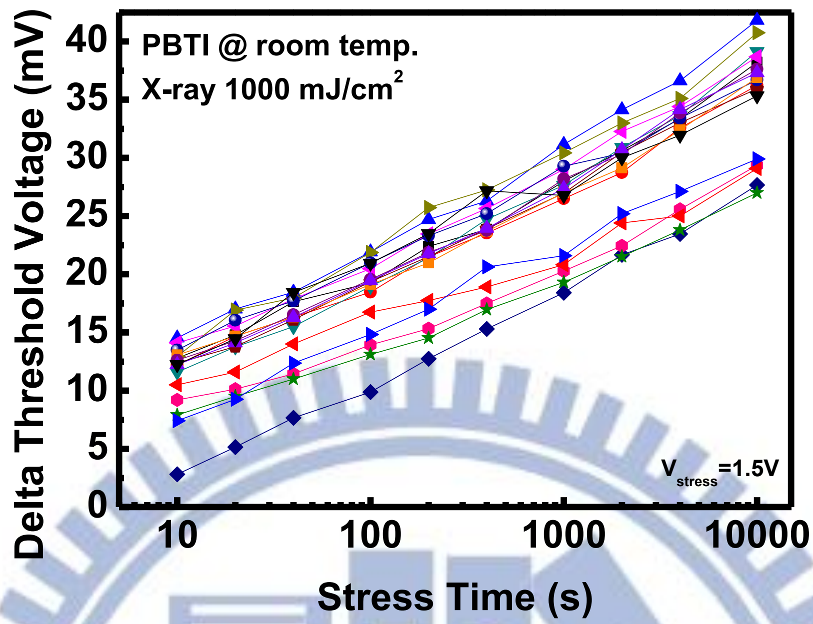
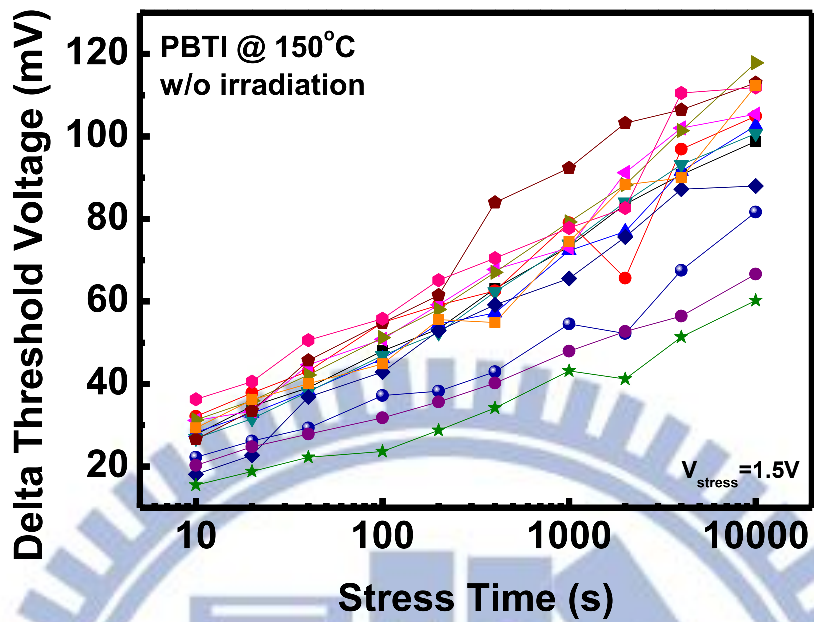
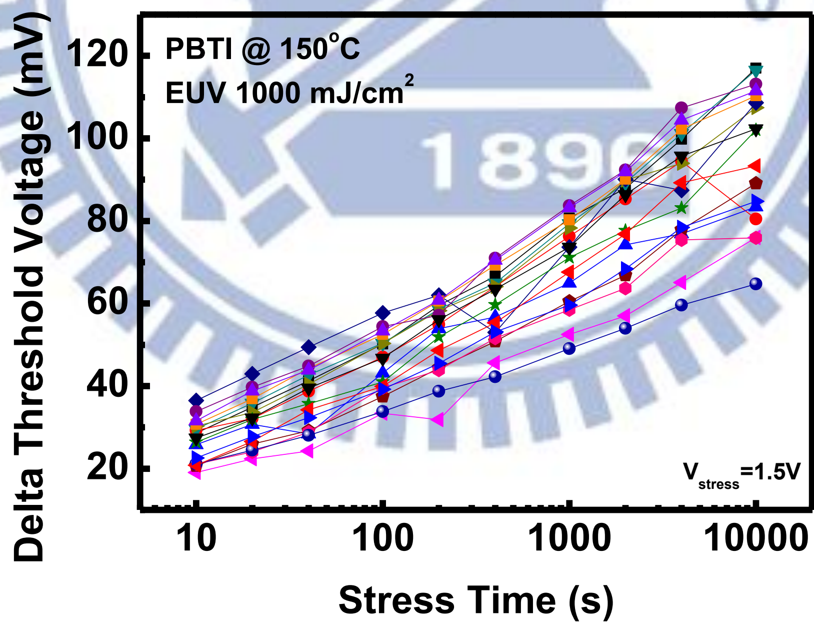


(c)

Fig. 3-27 Distribution of threshold voltage shift versus stress time at room temperature (a) without irradiation, (b) after EUV irradiation, (c) after 10 keV X-ray irradiation.



(a)



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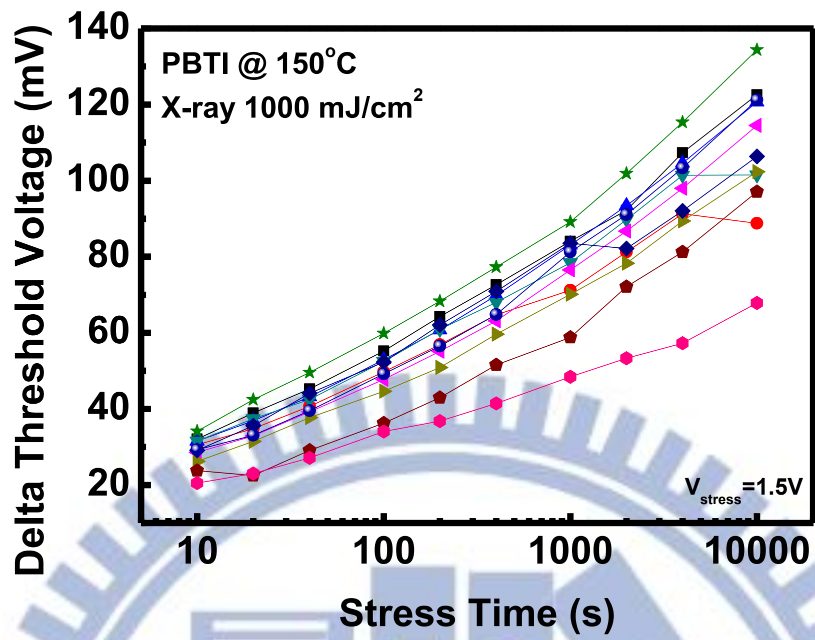

(C)

Fig. 3-28 Distribution of threshold voltage shift versus stress time at 150 ℃ (a) without irradiation, (b) after EUV irradiation, (c) after 10 keV X-ray irradiation.

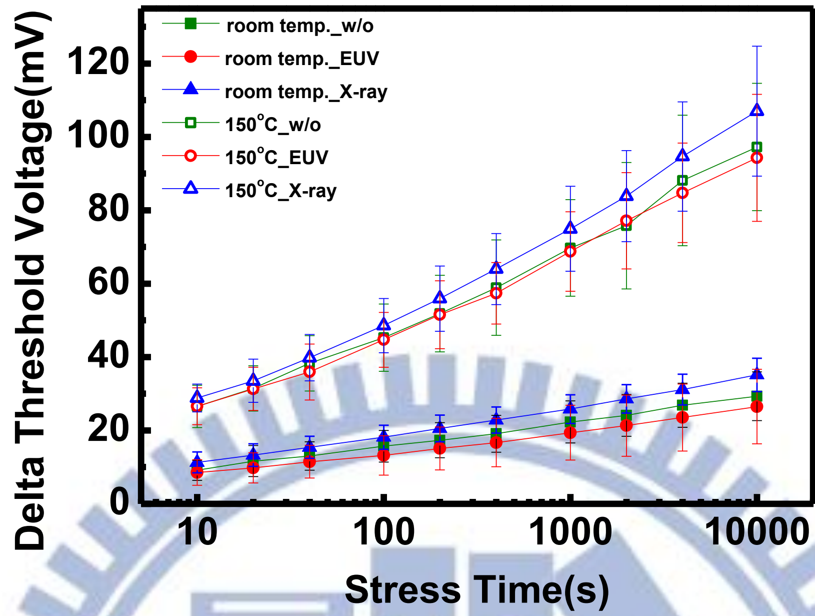

Fig. 3-29 Comparison of PBTI degradation of nMOSFET between different temperatures and different radiation sources.

Chapter 4
Conclusions and Future works

4-1 Conclusions

In this thesis, we have demonstrated that exposing device under ionizing radiation may degrade the electrical performances both on the high-k metal gate MIS capacitor and the state-of-the-art nMOSFET. On the part of high-k metal gate MIS capacitor, ionizing radiation may cause C-V curves shift and distortion. These phenomena are due to positive oxide-trapped charges and interface-trapped charges. Besides, the hysteresis also gets worse after irradiation. It is owing to the increment of border traps. Utilizing these electrical characteristics to evaluate the radiation damage effect, we focus on the radiation hardness on the device with different gate dielectric thicknesses. We discover that the device with the thinnest dielectric thickness offers the best radiation hardness. The reason can be concluded to three emphases. First, the thinner gate dielectric has fewer intrinsic defects. Second, the thinner gate dielectric absorbs fewer photons from ionizing radiation. Third, the e-h pairs generated by ionizing radiation can easily exchange charge with silicon substrate through tunneling process in the thinner gate dielectric. On another set of MIS capacitors, we try to investigate the radiation hardness between the devices with different post dielectric deposition RTA temperatures. However, we still discover that the dielectric thickness is the predominant factor affecting the radiation damage effect. We cannot distinguish the influence of RTA temperatures on radiation hardness clearly because the thickness of dielectric is very thin.

On the part of state-of-the-art nMOSFET, ionizing radiation may cause V_{th} shift

and S.S. degradation. They are also due to positive oxide-trapped charges and interface-trapped charges. The observations consist with those discovered on the MIS capacitor. Fortunately, the degree of V_{th} shift and S.S. degradation are not so critical because its ultrathin gate dielectric thickness. On the contrary and most significantly, the off-state leakage current raises two orders or even higher after EUV irradiation. By measuring the n^+-p junction characteristics, it is believed that the interface states induced by ionizing radiation at the field oxide/Si interface act as the generation and recombination centers and produce the leakage current. These experimental results illustrate an actuality. The key component affecting radiation hardness on the advanced device is no longer the gate dielectric; the field isolation oxide is too thick to prevent radiation damage effect. On the other hand, we have investigated the reliability of nMOSFET by the PBTI measurement before and after irradiation. We discover that the influence of the radiation is much smaller than the PBT stress; ionizing radiation do not affect directly on the reliability of the state-of-the-art nMOSFET.

We have also investigated the radiation damage effect by not only EUV but also 10 keV X-ray. It is believed that the absorptivity of material is an important factor affecting radiation damage effect. Even though the energy of EUV (91.85 eV) is lower than that of the 10 keV X-ray; however, most of EUV will be absorbed by the dielectric, and most of 10 keV X-ray will penetrate the dielectric under exposing. Hence, we discover the radiation damage effect for EUV is more apparent than 10 keV X-ray both on high-k metal gate MIS capacitor and state-of-the-art nMOSFET.

In the meantime, we monitor the electrical characteristics continuously at room temperature after irradiation. The self-annealing behavior is observed, especially on the device with thicker dielectric and field isolation oxide. The V_{fb} and V_{mg} may recover with time on MIS capacitors, and V_{th}, S.S. and off-state leakage current may also recover with time on nMOSFET. Nevertheless, these electrical characteristics can be

partially recovered to a better level after a long time storage at room temperature; hence, we anneal the devices by high temperature vacuum annealing. After 400~500 ℃ vacuum annealing, the damages seem to be fixed completely both on the MIS capacitor and nMOSFET. It illustrates that raising temperature can help recovery property after irradiation.

All in all, the main destination of this thesis is to evaluate the influence on MIS devices with high-k gate dielectric after ionizing radiation exposing. Fortunately, shrinking the thickness of gate dielectric is a trend for current ICs technology. It is believed that the advanced device offers good radiation hardness in the future according to the experimental results of this thesis. More importantly, the radiation hardness of isolation structure should be considered cautiously. Furthermore, high temperature annealing can effectively repair the damage caused by ionizing radiation. At last, not only EUV but also 10 keV X-ray is utilized to evaluate radiation hardness of device in this study. The absorptivity of material plays an important role to influence the radiation damage effect.

4-2 Future works

In this study, several progresses have been achieved and summarized in the previous section. However, some topics are worthy for further investigation. They are listed below.

1. Only p-substrate MIS capacitors and nMOSFET were irradiated by ionizing radiation in this study. The response of n-substrate MIS capacitors and pMOSFET should also be investigated.
2. About interfacial engineering, previous study has shown that chemical oxide offers the best radiation hardness. We can try to improve the interface quality unceasingly

by some method such as nitrogen-incorporation or plasma treatment.

3. The radiation damage effect between EUV and 10 keV X-ray have been investigated in this study. It is worthy for further investigation to find the relation between the energy of radiation source and the radiation hardness.
4. On the respect of dielectric reliability, we can investigate the PBTI and NBTI characteristics of high-k metal gate MIS capacitor before and after irradiation. It can help us realizing the mechanism further.
5. The current transport mechanisms and dielectric breakdown characteristics before and after irradiation have not been investigated in this study.
6. On the respect of recovery properties, previous study has shown that the radiation damage cannot be repaired entirely at 400 ℃ annealing on the MIS capacitors; however, we obtained a good recovery performance after 500 ℃ vacuum annealing. The recovery properties between 400 ℃ and 500 ℃ should be investigated further to reduce the thermal budget. On the other hand, the radiation damages can be completely repaired by a 400 ℃ vacuum annealing on the nMOSFET in this study, we can try to lower the annealing temperature and observe recovery properties again.
7. The reliability of the state-of-the-art nMOSFET has been evaluated by PBTI measurement. The influence of PBT stress is much larger than ionizing radiation. The stress voltage we used is 1.5 V, it is higher than practical driving voltage. We should use lower stress voltage to match with the realistic operational condition in the future.

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