voltage-controlled semiconductors has been demonstrated. A six cell monolithic PDA, when subjected to a normally incident flux of 50 mW/cm^2 at 865-nm peak wavelength, produces an open-circuit voltage of 5.3 V and a short-circuit current of 33 μA. These values are more than sufficient for numerous voltage-controlled switching applications. The ability to grow an area of approximately seven square centimeters of uniform material reproducibly, combined with the interconnecting of the PDA elements in a single metallization evaporation, provides a viable approach for using III-V arrays for such applications. The technological approach described here could easily be applied to other III-V systems, such as InP/InGaAs(P), where the wider bandgap binary could be used as the "window" layer and the ternary and quaternary absorbing layers could be adjusted to a specific composition to match the emitter's wavelength and assure efficient absorption of its spectral range.

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A New Dynamic Random Access Memory Cell Using a Bipolar MOS Composite Structure

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***Abstract*—A new dynamic random access memory (RAM) cell which incoperates an n-p-n bipolar junction transistor with an n-channel MOSFET in a composite structure, is proposed and investigated. In this novel cell called the BIMOS cell, the collector-base junction serves as a buried storage capacitor whereas the n-MOSFET as a transfer gate. The fabrication technology is simple and compatible with that of single-polysilicon CMOS IC's and a minimum cell size of 14.875F^2 with a minimum feature size F is realizable. The write, read, and standby operations of the cell are analyzed and simulated. An experimental cell is fabricated and characterized. Dynamic test is successfully performed. The investigation on the cell performance is also made. It has shown that large storage capacitance to bit-line capacitance ratio as well as fairly good packing density, soft-error immunity and leakage characteristics are expected. Furthermore, as compared to the conventional 1-transistor cell the new cell can be scaled down with less processing troubles and better performance improvements. Simple process and good scaled-down properties offer great potential for the proposed new cell to be used in the design of larger dynamic MOS RAM's.**

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LIST OF SYMBOLS

C_B	Base-charging capacitance of base-emitter junction.
C_{BC}	Reverse-biased junction capacitance of base-collector junction.
C_{BE}	Reverse-biased junction capacitance of base-emitter junction.
C_{BEJ}	Depletion capacitance of base-emitter junction.
C_{BL}	Bit-line capacitance.
C_{gs}	Gate-source overlap capacitance.
C_p	Parasitic capacitance.
g_m	Transconductance of a bipolar junction transistor.
I_{C0}	Reverse saturation current of a diode.
I_{CE0}	Collector-emitter current with opened base.
I_L	Leakage current of the cell.
n	Number of cells per bit line.
$Q_{i1(0)}$	Charge storage in the storage capacitor of the cell storing binary 1 (0).
t_s	Storage time of the cell.
$V_{BET(f)}$	Transient (final) base-emitter voltage.

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$V_{C1(0)}$	Coupling voltage at the storage node of the cell storing binary 1(0).
V_{DD}	Power supply voltage.
V_l	Signal size of the cell.
V_{REF}	Standby bit-line voltage.
$V_{S1(0)}$	Storage node voltage in the cell storing binary 1(0).
V_{th}	Threshold voltage of a MOSFET.
ΔV	$= V_{S1} - V_{S0}$.
ΔV_{BET}	Change of transient base-emitter voltage during Δt.
Δt	Time period of the write binary 0 operation.
β	Current gain of a bipolar junction transistor.
τ_F	Forward base transit time of a bipolar junction transistor.

I. Introduction

In the past decade, dynamic random access memories (RAM's) have evolved continuously toward larger bit capacity, higher performance, and lower cost per bit. To achieve these goals, many factors such as the signal size, leakage rate, packing density, complexity of clocks, and fabrication complexity should be carefully considered [1]. Since these factors strongly depend upon the performance of dynamic RAM cell itself, considerable efforts have been concentrated on the cell design and improvement.

So far the one-transistor-one-capacitor (1T) cell structure [2] has been the most popular one used in current MOS dynamic RAM's [3]. Such a cell stores a charge packet on an MOS capacitor with a MOS transistor as a transfer gate for charging and discharging. However the 1T cell suffers from low packing density and high leakage rate [4] which will become more severe as the bit capacity reaches 64K or higher. Therefore, many new concepts [1] have been explored to construct new cells with higher performance. One of these concepts is the buried junction storage which has been used in the VMOS dynamic RAM cell [5], the punchthrough isolated (PTI) cell [6], and the BO-MOS dynamic RAM cell [7]. All these new cells need epitaxy process and/or V-groove etching process which are more critical and complex than that in conventional MOS IC's.

This paper demonstrates a new cell design which incorporates an n-p-n bipolar junction transistor (BJT) with an n-channel MOSFET in a composite structure. In this new cell which is called the BIMOS cell according to its structure, the collector-base junction capacitor of the merged BJT serves as a buried storage element whereas the MOSFET as a transfer gate. The fabrication process of the new cell is compatible with that of the CMOS IC's. Moreover, it shows a good compromise between cell performance and process complexity. In Section II of this paper, read, write, and standby operations of the new cell are analyzed. The cell performance including chip area, signal size, leakage considerations, and process compatibility, is investigated in Section III. In Sections IV and V, experimental results of the test cell, simulated transient waveforms, and the performance of the scaled-down cell are described. Discussion and conclusion are made in the last section.

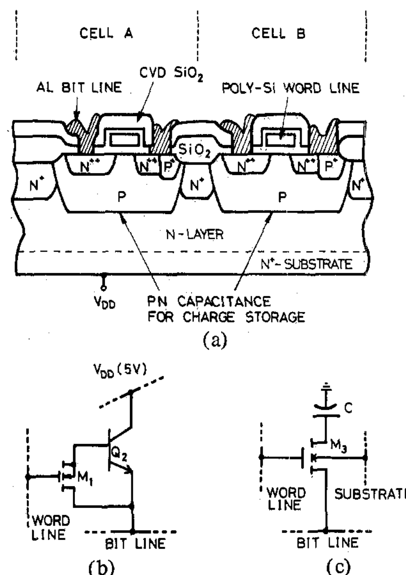


Fig. 1. (a) Cross-sectional views of two new dynamic RAM cells; equivalent circuit of (b) a new dynamic RAM cell; (c) a conventional 1 T cell.

II. Cell Operations

The basic integrated structure of the proposed new dynamic RAM cell is shown in Fig. 1(a). This cell mainly contains an n-MOSFET siting on a p-well. The polysilicon gate is extended to form the word line while the aluminum line, which contacts one of the two n^{++} regions in the n-MOSFET, is extended to form the bit line. The other n^{++} region is connected to the p^+ region of the p-well through an aluminum contact. Besides the n-MOSFET M_1, there is a merged BJT Q_2 with the n-substrate as collector, p-well as base, and n^{++} bit line diffusion region as emitter. Thus the equivalent circuit of the new cell may be drawn as in Fig. 1(b). As compared with the 1T cell circuit shown in Fig. 1(c), the M_1 transistor in the new cell serves as a transfer gate to charge or discharge the storage capacitor, similar to the M_3 transistor in the 1T cell. However, the storage capacitor here is base-collector p-n junction capacitor which lies beneath the M_1 transistor, instead of an MOS capacitor upon the semiconductor surface as in the case of 1T cell.

To write 1, the word line potential of the selected cell is rised from 0 to 5 V and its bit line potential is also rised to 5 V. At this time, the transistor M_1 is turned on and the p-well, i.e., the base region of the transistor Q_2, is charged. Then the bit line is left floating by a clock such as chip-enable clock. During this time, the word line potential is dropped to 0 V. At last the whole write 1 operation is finished by promoting the bit line potential to standby level V_{REF} which is equal to V_{DD} (5 V). If the charging action is complete, just after the write operation, the voltage at the base terminal called the storage node is

$$V_{S1} = V_{DD} - V_{th}. \qquad (1)$$

To write 0, the operation is similar to that of write 1 except that the bit line potential is lowered to 0 V. During the operation, the storage node potential first is discharged to 0 V and

finally is rised to some positive level by the capacitance coupling effect. Therefore, just after the write operation, the voltage level V_{S0} may be expressed by

$$V_{S0} = V_{C0} \tag{2}$$

where V_{C0} is the coupling voltage on the junction capacitance C_{BC} through C_{BE}. Since C_{BC} and C_{BE} are all voltage dependent, V_{C0} should be determined by the transient calculations.

To determine the final voltage at the storage node, the cell after the write 1(0) operation is considered to be always deselected before the next refresh cycle reaches. If this deselected cell is subjected to the standby operation, the bit line potential is kept at 5 V (V_{REF}) and two junctions of the bipolar transistor are reverse-biased. Thus the storage node is isolated from the bit line except that small reverse saturation current and leakage current flow through both reverse-biased junctions. Although these currents tend to increase the potential of storage node, such increase is so small that the potential of storage node will be nearly undisturbed. In the read and the write binary 1 operations, bit line potential is either 5 or near 5 V. Thus the deselected cell is not severely disturbed as in the standby case.

In the write or read binary 0 operation, the bit line potential is lowered to 0 V. At this moment, the storage node of the deselected cell storing binary 0 is also lowered to a small positive residue voltage which is generated during the standby period by the charging of small currents in reverse biased junctions. As the bit line remains at 0 V, the increasing rate of this residue voltage will be lower than that in the standby case because charging currents to the storage node from the two junctions are opposed rather than superposed. After the bit line potential is rised back to 5 V, the storage node potential is also rised to that of binary 0 and the original stored data is restored without destruction.

For the deselected cell storing binary 1, the voltage on the storage node is high. As the bit line potential is decreased to 0 V in the write or read binary 0 operation, the storage node voltage is decreased according to the capacitance coupling effect between base-collector junction capacitance and emitter-base junction capacitance. Finally, the emitter-base junction is forward-biased while the base-collector junction is kept reverse-biased. At this moment, the transient base-emitter voltage V_{BET} which is determined by the base-collector and base-emitter junction capacitances during the transient process, tends to be decreased by the base-emitter discharging current. This current is formed by the net flow of: 1) holes injected from base to emitter; 2) electrons injected from emitter and not collected by the collector and 3) holes injected from collector to base. The first two components are just the base current under V_{BET} whereas the last component is approximately the reverse saturation current I_{C0} of the base-collector junction. Thus the change of V_{BET} during the time period Δt can be written as

$$\Delta V_{BET} = (I_{C0} - I_C/\beta)\Delta t/(C_{BEJ} + C_B)$$
$$\simeq V_T \, \Delta t (I_{C0}/\tau_F I_C - 1/\beta\tau_F) \tag{3}$$

where the forward base-emitter junction capacitance is the sum of base-charging capacitance $C_B = \tau_F g_m$ which is the dominant component, and the forward depletion capacitance C_{BEJ}.

Assume that the deselected cell storing binary 1 is continuously subjected to the write or read binary 0 operation, the worst-case storage node voltage can be expressed as

$$V_{S1,\min} = V_{BEf} + V_{C1} \tag{4}$$

where V_{BEf} is the final base-emitter voltage when the bit line voltage is 0 V, and V_{C1} is the coupling voltage. Note that V_{C1} is greater than V_{C0} since the initial condition for V_{C1} has a larger forward-biased emitter-base junction capacitance C_{BE}.

From the above considerations, it is seen that if ΔV_{BET} is negligibly small, both V_{BEF} and $V_{S1,\min}$ will be nearly the same as those in the first time the bit line voltage is 0 V, and the stored voltage will be not severely distributed. However, if ΔV_{BET} is large, V_{BEf} will be equal to the steady-state open-base base-emitter voltage, and the binary 1 will be held with a lower $V_{S1,\min}$.

In the case of very large C_{BC}/C_{BE} ratio, both V_{C1} and V_{C0} are small. Thus $V_{S0} \simeq 0$, $V_{S1,\min} \simeq V_{BEf}$, and the stored informations will still be not destroyed. It should be emphasized that only when the storage node voltage of the deselected cell storing binary 0 has enough long time to be charged to V_{BEf}, the stored information could be destroyed.

In the proposed cell structure, both the emitter and base impurity concentration difference and the base width, i.e., the difference of p-well depth and source/drain depth, is rather large. This leads to a large $\beta\tau_F$. Furthermore, the time period Δt in the write or rewrite binary 0 operation can be small as will be seen in Section IV. Thus ΔV_{BET} can be strictly reduced. With very small ΔV_{BET}, each time the stored binary 1 level in the deselected cell storing binary 1 is recovered from one write or read binary 0 operation, the loss of its storage node voltage is quite small.

When the cell is scaled down, the base area is reduced and a smaller C_{BC} is resulted. The base-emitter C_{BE} is, however, also reduced to obtain the same or larger C_{BC}/C_{BE} ratio. Moreover, in the scaled-down cell, both the depth and the impurity concentration of the source/drain and the p-well can be designed to obtain the same large $\beta\tau_F$ and the smaller Δt. Thus very small ΔV_{BET} can also be obtained. Under this case, the stored binary 1 in the deselected cell is still not distroyed.

From (2) and (4), the stored charge quantity on the storage capacitor of the cell is written as

$$Q_{i1} = C_{BC}(V_{DD} - V_{S1,\min}) = C_{BC}(V_{DD} - V_{BEf} - V_{C1}) \tag{5}$$

$$Q_{i0} = C_{BC}(V_{DD} - V_{S0}) \tag{6}$$

where Q_{i1} (Q_{i0}) is the charge quantity when the cell stores 1(0). Therefore the signal swing on the bit line with capacitance C_{BL} is

$$V_l = \frac{C_{BC}}{C_{BC} + C_{BL}}(V_{BEf} + V_{C1} - V_{C0}). \tag{7}$$

The bit line capacitance per cell generally contains three components: 1) C_{BE} in series with C_{BC}; 2) gate-source overlap capacitance C_{gs} which is much smaller than that in 1), and 3) parasitic capacitance C_P which is also much smaller than that in 1). For a bit line with n cells connected in it, C_{BL} may be written as

$$C_{BL} = (n-1)\frac{C_{BC}C_{BE}}{C_{BC}+C_{BE}} + nC_{gs} + nC_P \simeq (n-1)\frac{C_{BC}C_{BE}}{C_{BC}+C_{BE}}. \quad (8)$$

Substituting (8) in (7), we have

$$V_l = \frac{1}{1+(n-1)\dfrac{C_{BE}}{C_{BC}+C_{BE}} + n\dfrac{(C_{gs}+C_P)}{C_{BC}}}(V_{DD}-V_{\text{th}}) \simeq \frac{1}{1+(n-1)\dfrac{1}{1+\dfrac{C_{BC}}{C_{BE}}}}(V_{BEf}+V_{C1}-V_{C0}). \quad (9)$$

From (9), it is seen that the signal size is strongly dependent upon the capacitance ratio C_{BE}/C_{BC}. As the bit capacity increases, n increases and C_{BE}/C_{BC} should be decreased in order to obtain a detectable V_l. The decrease of junction capacitance ratio C_{BE}/C_{BC} can be achieved by increasing C_{BC} and/or decreasing C_{BE} which are all feasible through various process technologies.

III. Performance

A. Chip Area

Since every cell has its own p-well as shown in Fig. 1, the spacing between two p-wells is the most important parameter in determining the cell area. Fortunately, the spacing can be strictly minimized due to the following reasons:

a) Only n-regions are connected to the power supply or the bit line while all p-regions are left floating. There is no way for the hold current to flow. Thus latchup cannot occur among the cells.

b) The n^+ region between two p-wells, which is formed before p-well implantation has a higher impurity concentration than the p-well region. Thus the lateral diffusion of p-well and the space charge width in n^+ region are effectively reduced.

c) The vertical scale down of p-well [8] also reduces the spacing between p-wells.

Although an extra contact is needed, the area of this contact plus other spacings is expected to be smaller than that of capacitor in conventional 1T cell. Thus the total chip area of the new cell will be smaller. Based on the single-poly process technology with minimum feature F and the same design rule in the BO-MOS cell [7], the minimum cell area is $14.875F^2$ as indicated in the layout shown in Fig. 2. For $F = 3$ μm, the area is 134 μm^2 which is smaller than that of 1T cell and VMOS cell, comparable with that of Hi-C cell [1] and PTI cell, but larger than that of a BO-MOS cell.

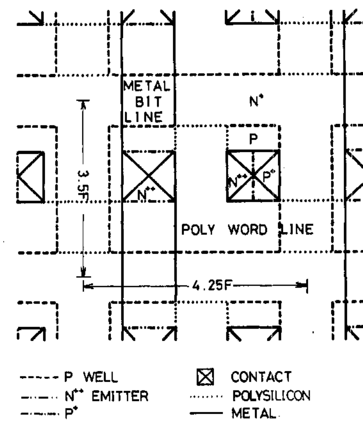


Fig. 2. A minimum layout of the BIMOS cell.

B. Storage Capacitance

In general the p-n junction reverse-bias capacitance per unit area is lower than the MOS capacitance per unit area. This disadvantage can be compensated partially by the fact that the entire cell area is available for the p-well which forms the cell storage capacitor with the n-substrate, and the fact that the depth of p-well is large to provide considerable sidewall capacitance. Moreover the n^+ diffusion on the n-substrate between p-wells is effective to increase the sidewall capacitance.

According to the cell layout in Fig. 2, the bottom area of p-well is 7 times that of n^{++} region whereas the typical depth of p-well is nearly 4 times that of n^{++} region. Furthermore, the difference between doping concentrations of two p-n junction capacitance C_{BC} and C_{BE} is offset by the n^+ diffusion on the substrate. Therefore the ratio C_{BC}/C_{BE} can be made large to obtain a larger signal size.

C. Leakage Considerations

The leakage current of a reverse-biased p-n junction generally increases with the junction area and decreases with the impurity concentration. Therefore the storage capacitance C_{BC} has a larger current than the bit line capacitance C_{BE} when the cell is in its standby mode. However, these two currents are expected to be low even at high bias because the p-well doping is quite low to effectively reduce tunneling [9] in both reverse-biased junctions despite of the high doping concentration of both n^+ and n^{++} regions.

The n^+ region between p-wells is effective to decrease the numbers of hole-electron pairs generated in the depletion region by α-particles or cosmic rays [10] and to repel the migrating holes from the bulk [7]. Therefore the soft-error immunity is not worse than the conventional 1 T cell.

D. Process Compatibilities

As may be seen from the integrated structure of the new cell shown in Fig. 1(a), the fabrication process is similar to that of Si-gate p-well CMOS except an extra n^+ implantation. Thus the cell can be easily fabricated by using the conventional technologies without paying a lot of efforts to develope other complicate or difficult processes. Moreover, the peripheral circuits can be built with CMOS, the way leading to a simpler

TABLE I
TYPICAL FABRICATION PROCESSES OF THE NEW CELL

1. Thermal oxidation
2. CVD Si_3N_4 and CVD SiO_2
3. P-well definition (Mask #1)
4. N^+ region implantation (AS)
5. Field oxidation (LOCOS)
6. Si_3N_4 remove
7. P-well implantation
8. Drive-in and oxidation
9. Active region definition (Mask #2)
10. Gate oxidation
11. CVD polysilicon
12. Gate definition (Mask #3)
13. P^+ region definition (Mask #4)
14. P^+ implantation
15. N^{++} region definition (Mask #5)
16. N^{++} implantation
17. CVD SiO_2
18. Ohmic contact opening (Mask #6)
19. Metallization (Mask #7)
20. Passivation (Mask #8)

TABLE II
SIMULATED SURFACE CONCENTRATION AND JUNCTION DEPTH OF THE DEVICE

Regions	Surface Concentration (cm^{-3})	Junction Depth (μm)
N^{++} Emitter	8×10^{19}	0.508
N^+ Diffusion	5×10^{17}	1.540
P-Well	5×10^{16}	2.690
N-Layer	5×10^{15}	—

circuit design [11] and a better balance of power and speed [12].

To be compatible with the n-well CMOS technology, the proposed cell can also be made on p-substrate with an n-well as its storage node and an p^+ region as its emitter.

IV. SIMULATED RESULTS

The proposed fabrication processes of the new cell with a p-type well are listed in Table I where only main steps are concerned. Except the n^+ region implantation which may also be viewed as a kind of field implantation, the processes are just the same as those of a typical p-well Si-gate CMOS. Based on the actual process parameters, the simulated surface concentrations and junction depths of the cell, which are generated from the SUPREM program [13], are shown in Table II.

To calculate the reversed junction capacitance, all the implanted profiles are assumed to be of Gaussian distribution which is a good approximation to the simulated profiles in

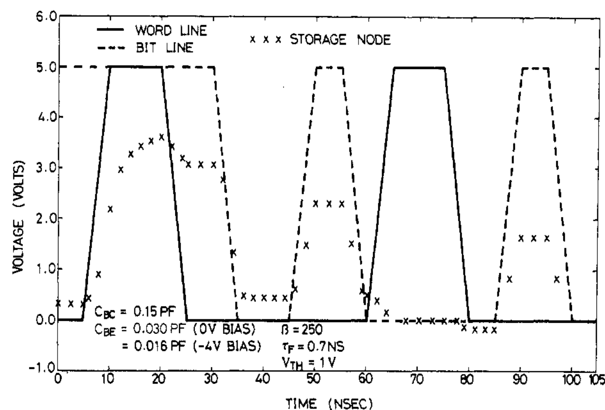


Fig. 3. Simulated timing diagram of the write operation.

TABLE III
PROPOSED DEVICE DIMENSION IN THE SCALED-DOWN CELL

Minimum Feature Size F (μm)	5	4	3	2	1	0.5
P-well Depth (μm)	2.69	2.69	2.69	2	1	0.5
Source-Drain Depth (μm)	0.508	0.508	0.508	0.4	0.2	0.1
N^+ Depth (μm)	1.54	1.54	1.54	1.14	1	0.5
Surface Concentrations	All Unchanged					

TABLE IV
CALCULATED JUNCTION CAPACITANCES AND THEIR RATIOS AT DIFFERENT MINIMUM FEATURE SIZE

Minimum Feature Size (μm)		5	4	3	2	1	0.5
Total Capacitance Ratio (C_{BC}/C_{BE})	with n^+	4.0	4.4	5.2	5.9	8.5	14.8
	without n^+	2.3	2.5	2.7	3.7	4.3	6.7
Sidewall Capacitance Ratio	with n^+	29.3	29.7	30.0	30.5	33.0	37.2
	without n^+	16.5	16.8	17.3	18.0	18.8	25
C_{BC} (with n^+) (fF)		70	60	51	14	7.0	5.5
C_{BE} (fF)		17.5	14.0	9.8	2.4	0.82	0.37

Fig. 3. The capacitance of the bottom plate in B-E and B-C junctions is calculated by the method proposed by Lin [14]. The sidewall capacitance of the p-well touching the n-region is calculated by the conventional method [15] whereas the sidewall capacitance of the p-well touching the n^+ region and the sidewall capacitance of B-E junction, both being of double Gaussian distribution, are calculated by the numerical method [16]. Based on these methods, a simulation program for the reversed junction capacitance has been constructed to simulate the cell capacitances.

According to the cell layout shown in Fig. 2 and the simulated profiles, a scale-down on the dimension of the cell is proposed, as shown in Table III, to investigate the performance of the scaled-down cell. Both the p-well and the source-drain junction depths are not subjected to scale down until the minimum feature size is below 3 μm. The surface impurity concentrations of all the implantation regions remain the same as those in Table I for all values of F.

The total capacitance ratio C_{BC} to C_{BE} and their sidewall capacitance ratio for the cells storing binary 1 are listed in Table IV. For the cell with the n^+ diffusion outside the p-well

the ratio increases from 3.8 at $F = 5$ μm to 5.2 at $F = 3$ μm and finally to 14.8 at $F = 0.5$ μm. This implies that when the cell area is scaled down in order to be used in a larger RAM, the ratio of storage capacitance to bit line capacitance is favorably increased without involving critical processes such as thin capacitor oxide growth as the conventional 1T cell should do. This increase is due to the following reasons:

a) Due to the logarithmic dependence of the sidewall capacitance per unit area on the depletion width [15], the difference of the sidewall capacitance density between B-C and B-E junctions is smaller than that of the bottom plate capacitance density. Therefore the total sidewall capacitance in the B-C junction which has a larger sidewall area, is larger than in the B-E junction and their ratio is large as may be seen from Table IV. When the horizontal dimension is scaled down by a factor K and the vertical dimension remains unchanged, the sidewall area and its capacitance become more and more significant. Therefore, although the sidewall capacitance ratio is not changed, the total capacitance ratio is still increased from $F = 5$ μm to $F = 3$ μm as listed in Table IV. The increase of sidewall capacitance ratio when F is smaller then 3 μm is due to the increase in the percentage of p-well sidewall area touching the n^+ region. This increase also contributes part of the increase of the ratio C_{BC}/C_{BE}.

b) The p-well depth is scaled down under the fixed surface impurity concentration. This leads to a lower p-well concentration at the B-E junction and a larger gradient at the B-C junction. Therefore when scaled down, C_{BE} is decreased more fast than C_{BC} is, as listed in Table IV. This leads to the result that the ratio C_{BC}/C_{BE} is remarkably increased from $F = 2$ μm to $F = 0.5$ μm as listed in Table IV.

For the purpose of comparison, the ratios and capacitances for the cell without the n^+ diffusion are also listed in Table IV. The increase of C_{BC} by the n^+ diffusion can be easily seen. For the cell storing binary 0, the characteristics are similar to those of the cell storing binary 1 cited earlier.

To show the dynamic characteristics of the cell, the voltages of V_{BET}, V_{BEf}, V_{C1}, and V_{C0} are simulated by using the SPICE program [17] and are listed in Table V for different C_{BC}/C_{BE}. In this table, the value of V_{BET} is determined at the first time the bit line is lowered to 0 V just after the write 1 operation, that of $V_{S1,\min}$ (V_{S0}) is determined from the worst case that the bit line voltage has been kept at 0 V (5 V) 2 ms long. Based on these data, the number of cells n which can be connected together on one bit line and can offer 100-mV signal size in the worst case, is estimated by (9) and is also listed in Table V. It may be seen that at larger value of C_{BC}/C_{BE}, the signal swing $V_{S1,\min} - V_{S0}$ is smaller than the value of $V_{DD} - V_{th}$. Therefore the value of n is smaller than the 1T cell for the same bit line capacitance to storage capacitance ratio. However, the C_{BC}/C_{BE} ratio is large when the cell is scaled down. This leads to a large enough n value to be used in a large DRAM.

Typical write transient waveforms in the case of large ($\simeq 10$) C_{BC}/C_{BE} ratio which is the practical condition for DRAM cells, are shown in Fig. 3. It is evident that $V_{S1,\min} \simeq V_{BEf}$ and $V_{S0} \simeq 0$ as predicted in Section II.

TABLE V
CALCULATED VOLTAGE LEVELS AND NUMBER OF CELLS PER BIT LINE FOR 100-mV SIGNAL SIZE IN THE CELLS WITH DIFFERENT C_{BC}/C_{BE}

Device Parameters	$\beta=250$ $\tau_F=0.7$ns $V_{Th}=1.0$V $C_{BE}=0.016$pf (-4V bias)			
C_{BC} (PF)	1	0.5	0.15	0.08
V_{BET} (V)	0.4547	0.4426	0.4287	0.1850
$V_{S1,\min}$ (V)	0.73	1.09	2.21	3.03
V_{S0} (V)	0.39	0.73	1.75	2.37
number of cells	150	80.6	36	28

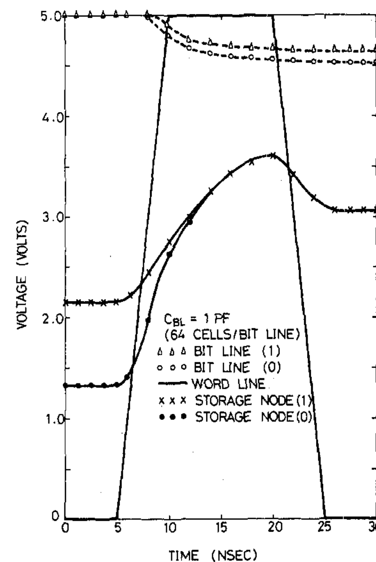


Fig. 4. Simulated timing diagram of the read operation.

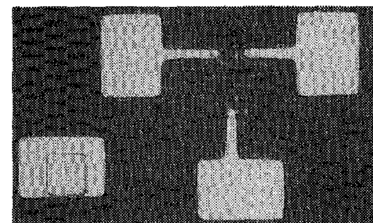


Fig. 5. Surface photograph of a fabricated cell.

The corresponding read transient is shown in Fig. 4 where the bit line capacitance C_{BL} is 1 PF which is equivalent to that of bit line with 64 cells on it. The signal swing of 112 mV can be obtained within 10 ns.

V. EXPERIMENTAL RESULTS

To observe some properties of the proposed new dynamic RAM cell, a test chip for the new cell is designed by using 10-μm design rule. The fabrication processes are the same as listed in Table I except that the n^+ diffusion region outside the p-well is simply defined by an extra mask rather than by the LOCOS method. The surface photograph of the fabricated cell is shown in Fig. 5. The measured capacitance at various

TABLE VI
JUNCTION CAPACITANCE AND LEAKAGE CURRENT DENSITY OF THE EXPERIMENTAL CELL

Junction Voltage (V)		0	1	2	3	4	5
C_{BC} (with n^+)	Experimental (PF)	0.79	0.55	0.44	0.37	0.33	0.31
	Theoretical (PF)	0.80	0.56	0.45	0.39	0.35	0.33
C_{BC} (without n^+)	Experimental (PF)	0.67	0.44	0.34	0.29	0.28	0.26
	Theoretical (PF)	0.67	0.48	0.38	0.32	0.29	0.28
C_{BE}	Experimental (PF)	1.48	0.66	0.54	0.47	0.39	0.35
	Theoretical (PF)	1.52	0.67	0.53	0.44	0.36	0.33
Leakage current density in C_{BC} (nA/cm^2)	Area 100μm×60μm	3.0	8.0	18	38	45	48
	50μm×30μm	0.95	3.5	7.0	9.0	12	14

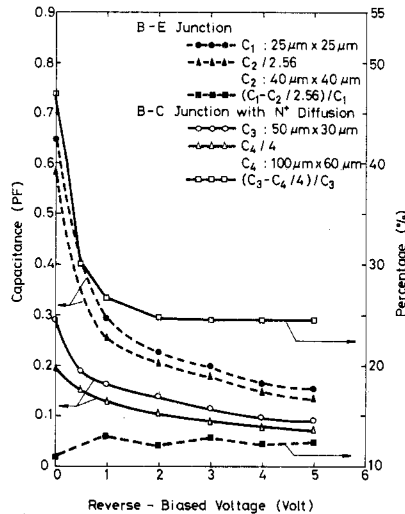


Fig. 6. Characteristics of capacitance increment in the scaled-down B-C and B-E junctions.

reverse-biased voltages for the base-collector junction with and without n^+ diffusion and the base-emitter junction are listed in Table VI. As may be seen from Table VI, the capacitance is increased by the n^+ diffusion. However, since the fabricated cell is not optimized in its dimension, the capacitance C_{BE} appears larger than C_{BC}. Theoretical calculations are also compared to the experimental results and a satisfactory agreement between them is obtained.

To investigate the scale-down properties of the cell capacitances, the capacitances of two B-C junctions with an area ratio 4 and two B-E junctions with an area ratio 2.56 are measured and the results are shown in Fig. 6. Due to the contribution of the sidewall capacitance as mentioned in Section IV, the capacitance of the scaled-down B-C junction is larger than one-fourth of the capacitance of the larger B-C junction by 24 percent. It is larger than that of B-E junction, 12 percent. Therefore the scale-down is effective to increase the ratio C_{BC}/C_{BE}.

Typical leakage current density of two B-C junctions at various reverse voltages is listed in Table VI where the increase of current with respect to the increase of voltage is rather small. Therefore the tunneling current component [9] in these junctions is negligible.

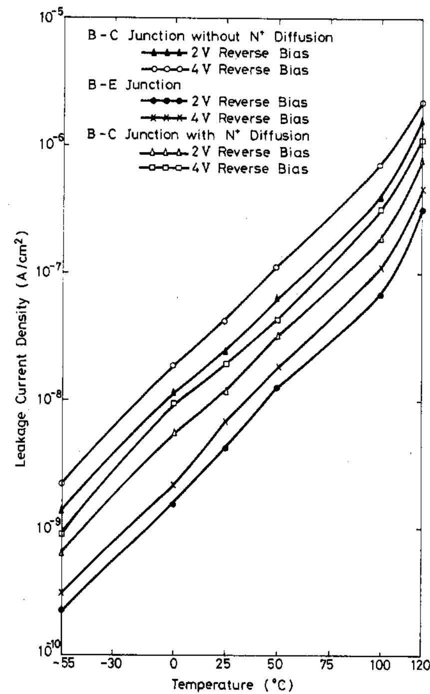


Fig. 7. Leakage current as a function of ambient temperature in various p-n junctions.

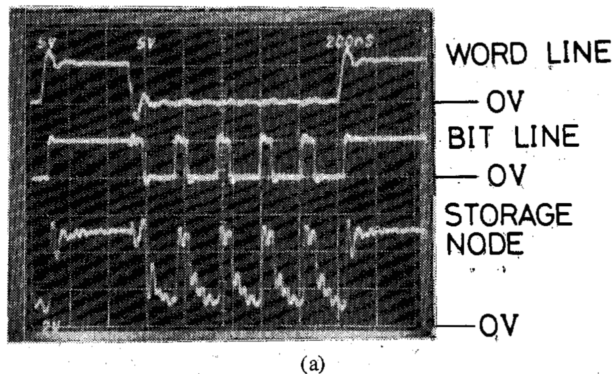
Since the leakage current in the sidewall junction which has higher impurity concentration is smaller than that in the bottom junction and the contribution of sidewall become more significant than that of bottom wall when scaled down. Thus the total leakage current density of the whole junction is smaller in the smaller junction than in the larger one as listed in Table VI. Similar result is also obtained in the case of B-E junction.

When the reverse-biased junction voltage exceeds 1 V, the variation of capacitance with temperature in both junctions are observed to be negligibly small. However the leakage current is increased with the increase of ambient temperature as shown in Fig. 7 where the B-E junction, the B-C junction with n^+ diffusion, and the B-C junction without n^+ diffusion are measured. It may be seen that the n^+ diffusion in the sidewall is also effective in reducing leakage current. From Fig. 7, the total leakage current I_L of the cell storing binary 0 is about 1.25 pA at 25°C. For the averaged storage capacitance C_{BC} = 0.44 pF and voltage swing between 0 and 1 $\Delta V = 1$ V, the storage time t_s of the fabricated cell may be estimated by [7]

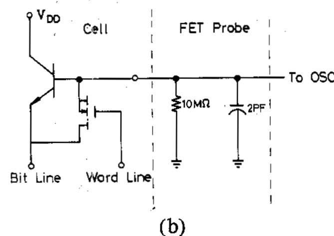
$$t_s = C_s \, \Delta V / I_L = 350 \text{ ms}.$$

When the cell is operated at 120°C, the storage time reduces to 6 ms due to a larger I_L = 73 pA.

Dynamic test of the fabricated cell is also performed. The waveforms in the write 1 and standby operations are shown in Fig. 8(a) with test circuit shown in Fig. 8(b). The cell is first selected to write 1 and then is deselected. During the deselected or standby period, the bit line voltage is subjected to several times of droping to 0 V. However, the storage node voltage can follow the bit line voltage changes and recover itself without destroying the stored binary 1. Note that short

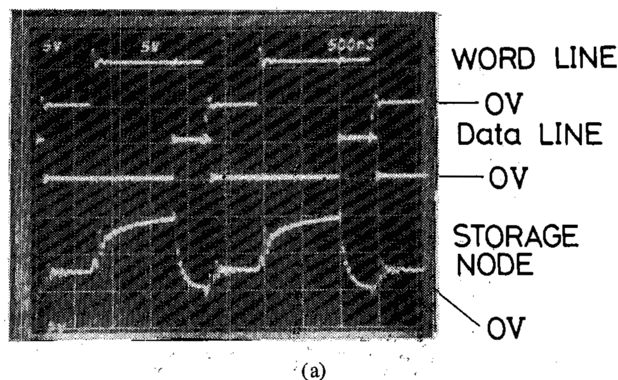


(a)

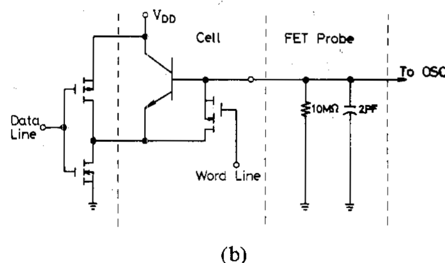


(b)

Fig. 8. (a) Dynamic waveforms of the write 1 and standby operations; (b) its test circuit.



(a)



(b)

Fig. 9. (a) Dynamic waveforms of the write 0 and standby operations; (b) its test circuit.

clocks are used to prevent the cell from discharging through the input resistance of the probe. Thus the storage node voltage can be directly observed.

The waveforms in the write 0 and standby operations are shown in Fig. 9(a) with the test circuit shown in Fig. 9(b). The cell is first selected to write 1 and then write 0, finally is deselected and standby at binary 0. The voltage difference of the storage node between 0 and 1 is clearly seen. Due to the effect of the external circuit the charging of write 1 is slow down in this test.

VI. Discussion and Conclusion

We have proposed a new dynamic RAM cell which consists of an n-channel MOSFET as a transfer gate and a base-collector junction of a merged BJT as a storage capacitor. The write and read operations of the new cell have been analyzed, described, and simulated. It has been shown that the signal size depends upon the capacitance ratio of the base-collector junction and the base-emitter junction. In the standby operation, the cell leakage current is small enough to obtain a good data retention capability. The stored data in the deselected cell is not destroyed by the bit line potential variations.

Due to the facts that latchup cannot occur and lateral diffusion width is reduced by the n^+ diffusion, the spacing between p-wells can be strictly minimized. Thus a minimum area $14.875F^2$ with a minimum feature size F is realizable. Furthermore, the n^+ region between p-wells is effective to reduce carrier generation and collection, therefore the soft-error immunity of the cell is not worse than the conventional 1T cell.

Unlike other cells using the buried junction storage, no epitaxy or V-groove cutting is required. The fabrication technology of the cell is fully compatible with that of p-well or n-well Si-gate CMOS. Using the p-well silicon-gate CMOS processes and relaxed design rule, the experimental cell is fabricated and tested. The fabricated cell has a leakage current of 1.25 pA at 25°C and an averaged storage capacitance of 0.44 pF, which lead to a storage time of 350 ms. Dynamic test of the fabricated cell is also successfully performed to verify the cell operation descriptions. However, because optimal dimension is not performed in the fabricated cell, the capacitance ratio is small. Further improvements on the cell will be done and a whole test RAM IC will be fabricated in the near future.

When the cell is scaled down, the capacitance ratio is simulated to be increased from 3.8 at $F = 5$ μm to 5.2 at $F = 3$ μm and finally to 14.8 at $F = 0.5$ μm. This is due to the contributions of both the sidewall junction and the p-well doping profile. The number of cell per bit line for 100-mV signal size is also increased as the cell is scaled down. Furthermore the leakage current density is reduced when scaled down.

In summary, the proposed new cell has simple fabrication process and good performance of large storage capacitance to bit-line capacitance ratio, as well as fairly good packing density, soft-error immunity and leakage characteristics. Moreover, as compared with the conventional 1T cell, the scaling down of the cell can be performed with less processing troubles and better performance can be obtained. Thus it is felt that the new cell has great potential for further developments.

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Silicon-Rich SiO_2 and Thermal SiO_2 Dual Dielectric for Yield Improvement and High Capacitance

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***Abstract*—The use of silicon-rich SiO_2 and thermal SiO_2 dual dielectric in memory capacitors and FET's is investigated. It is shown that the silicon-rich layer was conductive and introduced only a small decrease in the series capacitance of the dual dielectric. Consequently, the capacitance of the dual dielectric is close to that of the thermal oxide only. The response time of the silicon-rich layer is measured by using FET response time and is shown to be in the nanosecond range. With this fast response time, it is possible to use the dual dielectric in memory and logic circuits. Another advantage of the dual dielectric is the very high yield due to the field screening of the silicon-rich layer to any nonuniformities in the thermal oxide or at the SiO_2-contact interface. This dual dielectric has the promise of high yield and high capacitance for future VLSI circuits.**

I. INTRODUCTION

IN VLSI circuits, a high-dielectric-constant gate-material is very desirable. It can increase storage capacitance in 1-device dynamic memory cells [1] thus increasing signal levels and reducing the impact of alpha particles [2], increasing transconductance of FET's, and reducing short-channel effects [3]. Insulators like silicon nitride [4] and tantalum pentoxide [5] have been proposed and used to give higher dielectric constant compared to that of thermal oxide. However, the use of such insulators is still experimental, and their compatibility with standard polysilicon gate processing and long-term reliability are questionable.

Recently, it was demonstrated that silicon-rich silicon dioxide (deposited by CVD with approximately 13-percent excess silicon) [6] could be used on top of thermal silicon dioxide for enhanced electron injection into the oxide [7]-[9]. Furthermore, silicon-rich oxide has a high dielectric constant (approximately 7.5 in the above composition) and such a composite structure has been demonstrated to have well controlled high field conduction properties [9]. In the low field region (less than 5 MV/cm) where there was no significant injection of electrons, such a dual dielectric gave higher capacitance compared to pure oxide of the same thickness and had very few low field breakdowns, giving high yields [9]. It will be shown in this paper that under suitable conditions, the response time of stored charge in the silicon-rich layer can be in the nanosecond range, fast enough to be used in most circuits. From a

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