國立交通大學

電子工程學系 電子研究所碩士班

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# 降低金屬與N型鍺接觸電阻之研究

# A Study on the Contact Resistance Reduction in Metal/n-type Germanium Contacts

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## 摘要

隨著製程技術的發展，使用矽做為主要半導體材料的金氧半場效電晶體不斷地成功微縮，但是如果繼續發展下去很快的會碰到了物理極限的限制而導致無法繼續提升性能。許多方式被提出來解決這個問題，鍺由於其較高的載子遷移率以及與矽製程較大的相容性，被視為是下個世代中有機會取代矽做為通道的半導體材料。但是N型鍺與金屬接面會有較大的蕭基位能障而導致較大的接觸阻抗，所以如果我們要使用鍺做為金氧半場效電晶體的材料，降低N型鍺與金屬接觸阻抗是必要的。本論文探討兩種不同的方式來降低N型鍺與金屬的接觸阻抗，分別是以調變蕭基位能障的介電層插入元件與增加接面載子濃度的修正蕭基位障元件。

介電層插入製程已有文獻發表，前人研究使用三氧化二鋁以及二氧化鈦做為介電層，由於二氧化鈦與鍺有較低的導帶差，因而在降低蕭基位能障之外還能達到較小的穿隧阻抗，以致於有較大的導通電流，但是實際改善機制尚無定論。本論文首先觀察到蕭基位能障鎖定效應在不同厚度的二氧化鈦介電層插入元件上並沒有太大差異，所以推斷介電層插入元件是以改變鎖定位置為主的方式調變蕭基位能障。再利用金氧半電容結構計算出介電層內部的固定電荷量並不足以造成如此大的調變幅度，所以推論其調變方式是主要以接面因不同極性而產生的感應偶極電荷為主。除此之外，我們發現介電層插入元件在攝氏300度經30分鐘的退火條件下，特性就會變差且蕭基位能障會回升，退火溫度愈高，蕭基位能障愈高。根據微結構分析，我們推論介電層因退火而產生的結晶化是導致特性變差的主要原因，由於介電常數因結晶化而增加，介電層電容值增加所以電壓改變量較小，

導致蕭基位能障增加。較厚的二氧化鈦介電層會有較低的電容值，可能也是其蕭基位能障較低的原因。

修正蕭基位障元件因為離子植入在金屬鍺化物而不是直接植入鍺基板，鍺基板中產生的缺陷較少，所以之後退火時雜質就不會因為與缺陷的反應而提升雜質擴散速率，進而在金屬與半導體的接面產生較淺且載子濃度較高的摻雜層。研究發現提升活化溫度能得到更高的載子活化濃度，但是鎳化鍺的熱穩定性不佳，限制了活化溫度在攝氏500度。為了增進鎳化鍺的熱穩定性，本論文提出在鎳與鍺中間插入一層矽再讓其反應的技術，研究發現加入矽之後，鎳化鍺的熱穩定性從500度提升到了550度，且具有較低的片電阻值。藉由使用摻雜矽的鎳化鍺來製做修正蕭基位障元件，將活化溫度提升到550度，得到了更高的活化濃度。與傳統直接植入鍺基板再退火的元件相比，修正蕭基位障元件具有較佳的活化濃度與較淺的高濃度區域，因此修正蕭基位障接面具有當做短通道鍺基板金氧半場效電晶體的源極與汲極的潛力。

本論文提出插入介電層以降低蕭基位能障高度的物理機制，並解釋了厚度與退火溫度的效應，並提出新的修正蕭基位障技術，以降低接觸電阻，並得到高濃度的淺接面，對於提升N型鍺的金氧半場效電晶體，極具應用潛力。

# A Study on the Contact Resistance Reduction in Metal/n-type Ge Contacts

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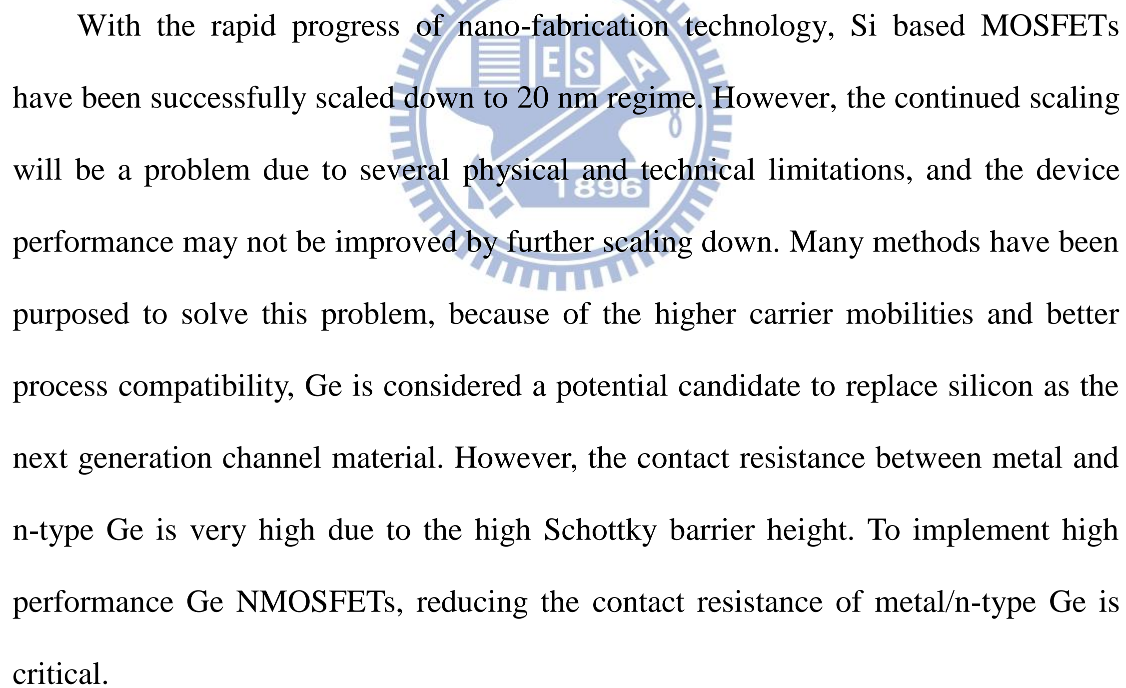
## Abstract



With the rapid progress of nano-fabrication technology, Si based MOSFETs have been successfully scaled down to 20 nm regime. However, the continued scaling will be a problem due to several physical and technical limitations, and the device performance may not be improved by further scaling down. Many methods have been purposed to solve this problem, because of the higher carrier mobilities and better process compatibility, Ge is considered a potential candidate to replace silicon as the next generation channel material. However, the contact resistance between metal and n-type Ge is very high due to the high Schottky barrier height. To implement high performance Ge NMOSFETs, reducing the contact resistance of metal/n-type Ge is critical.

In this thesis, two different methods to reduce the contact resistance of metal/n-type Ge are investigated. One is inserted dielectric-inserted junction and the other is modified Schottky barrier junction. The former is to modulate the Schottky barrier height and the latter is to enhance the doping concentration at the metal/Ge interface.

The dielectric insertion method has been reported in literature. Both $Al_2O_3$ and $TiO_2$ have been used as the inserted dielectric layer. Because of the lower conduction band offset of $TiO_2$ to Ge, it can not only reduce the Schottky barrier height but also achieve low tunneling resistance and high conduction current. However, the mechanism has not been well understood. In this thesis, we first observed that the Fermi level pinning effect is a very weak function of the $TiO_2$ thickness so we infer that the Schottky barrier height reduction by the dielectric insertion is due to the change of the pinning position. The amount of fixed charges in the thin dielectric layer is extracted from a MIS structure and it is found that the small amount of fixed charges is not sufficient to produce such a pronounced voltage drop to modulate the Schottky barrier height. It is thus recommended that the mechanism of the dielectric insertion method mainly comes from interface dipoles. Besides, it is observed that after annealing at 300 ℃ for 30 minutes, the Schottky barrier height will increase. The increase of the Schottky barrier height increase with the increasing of the annealing temperature. According to the microstructural analysis, it is postulated that the crystallization of the dielectric layer after annealing is the main reason for the increase of Schottky barrier height. Due to the dielectric constant increase after crystallization, the capacitance of the dielectric capacitor increases and causes smaller voltage drop so that the Schottky barrier height increases. The thicker $TiO_2$ dielectric layer has smaller capacitance, which might be the reason for the lower Schottky barrier height.

In the modified Schottky barrier method, dopants are implanted into metal-germanide instead of Ge so that the number of defects formed in substrate could be negligible, which would mitigate the dopants diffusion caused by the interaction between defects and dopants. A thin and high doping concentration layer can be formed at the metal/semiconductor interface. Increasing the activation

temperature will achieve higher doping concentration. But the allowed annealing temperature is limited by the poor thermal stability of NiGe films. To improve the thermal stability of NiGe films, a Si layer is inserted between Ni and Ge before annealing. The result shows that the thermal stability of NiGe film is improved by this Si-insertion layer from 500 ℃ to 550 ℃. Using the Si-insertion technique, the activation temperature of MSB junctions can be raised to 550 ℃ so that the doping concentration is enhanced. Compared to the conventional junction with direct implantation into Ge, the junction depth is much shallower and the carrier concentration is much higher for the MSB junction which suggests that the MSB process is attractive for the short channel Ge MOSFETs.

In summary, this thesis proposed the mechanism of the Schottky barrier height modulation by dielectric insertion. The thickness effect and annealing effect are also explained. A new method, modified Schottky barrier method, is propsed to reduce the contact resistance between metal and n-type Ge by forming a thin and high concentration layer at the metal/Ge interface. This method is very promising for short channel Ge NMOSFET.

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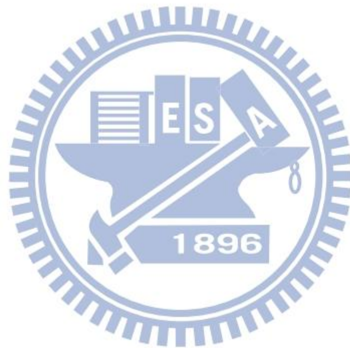

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# Chapter 1
# Introduction

## 1-1 Why Studying Germanium

In 1947, John Bardeen and Walter Brattain fabricated the first transistor using Ge as the semiconducting material at Bell Laboratories, by which they got 1956 Nobel Prize in Physics, along with William Shockley. From then on, Ge had been the predominant material for solid-state devices through 1950s and early 1960s. But during 1960s, once the crystal growth technology of Si became mature, Ge was quickly replaced by Si due to two major reasons: (1) Ge has smaller band gap (~0.67eV at room temperature) than Si resulting in larger leakage current and, most importantly, (2) Ge dioxide is water-soluble, which would produce many problems with device fabrication. Then with metal oxide semiconductor field effect transistors (MOSFETs) became the most important device, the excellent qualities of thermally grown Si dioxide as gate dielectric for Si resulted in more researches on Si instead of Ge.

In recent years, because of the device scaling limits, many methods have been proposed to improve devices performance. One of the most significant methods is that replacing Si dioxide gate dielectric with high-dielectric-constant (high-k) materials like $HfO_2$ [1]. With the implement of the high-k dielectric, the lack of high-quality native oxide with Ge becomes much less significant and because Ge has better electron (3900 vs 1400 $cm^2/Vs$) and hole (1900 vs 500 $cm^2/Vs$) bulk mobility than Si, it becomes one of the potential candidates to replace Si as next generation channel material.

However, Ge still encounters many challenges on MOSFET fabrication. First, Ge devices have high off-state leakage current because of the narrow band gap, which will introduce large tunneling current due to gate induce drain leakage (GIDL) effect as well as generation/recombination current. Second, the low solid-state solubility of dopants in Ge causes incomplete activation [2]. In addition, dopants diffusion with defects during annealing is more severe in Ge than in silicon, which would make it difficult to implement shallow and low resistivity source/drain junctions [3]. Although Ge $p^+$/n junctions with high activation level of boron have been demonstrated [4,5], high performance $n^+$/p junctions have not achieved because of the solid-state solubility and dopant diffusion limits. Third, the contact resistance at the metal/$n^+$ Ge contact is large due to the high Schottky barrier height at the metal/n-Ge interface, which comes from Fermi level pinning effect [6,7] and results in high parasitic resistance so that degrading the on current of Ge NMOSFET. To improve the performance of Ge NMOSFET, contact resistance is one of the major problem has to be solved.

## 1-2 Contact Resistance and Fermi Level Pinning in Germanium

To reduce contact resistance of metal/Ge contacts, doping concentration and Schottky barrier height are the most critical factors have to be improved. Unfortunately, n-type doping concentration in Ge is very difficult to be increased because dopant diffusion is fast and the solid-state solubility is low in Ge. On the other hand, Schottky barrier height is also hard to be decreased due to Fermi level pinning. To deal with the Fermi level pinning problem, first we have to understand how Schottky barrier formed and its relationship with contact resistance.

## 1-2-1. Schottky Barrier Formation

When a metal is contacted with a semiconductor, a potential barrier will form at the interface due to the difference in the work functions between these two materials. The energy band diagrams in Fig.1[8] illustrate the process of the barrier formation. Fig.1-1(a) shows the electron energy band diagram of a metal of work function $\varphi_m$ and an n-type semiconductor of work function $\chi + \varphi_n$, where $\chi$ is the semiconductor electron affinity and $\varphi_n$ is the difference between Fermi energy and conduction band edge of semiconductor. According to the Einstein relation, the Fermi levels of the two materials must come into coincidence when electrostatic equilibrium is established, the electrons which have higher energy will transport to another material till the Fermi level of the two sides are equal, as shown in Fig.1-1(b). As the electrons move out of the semiconductor into the metal, the free electron concentration in the semiconductor region near the interface decreases, which causes the band bending of the semiconductor and forms a potential barrier at the interface, as shown in Figs.1-1(c) and 1-1(d). This potential barrier is called Schottky barrier, which plays an important role on the current transport of the metal-semiconductor contact.

In electrostatic equilibrium, the Fermi levels must be aligned at the interface, the Fermi level in the metal would move by an amount of equal to $\varphi_m - (\chi + \varphi_n)$ the difference between the two thermionic work functions amounting to, where $\chi$ is the electron affinity and $\varphi_m$ is the metal work function. The final barrier height will be given by $\varphi_{bn} = \varphi_m - \chi$ .

## 1-2-2. Contact Resistance

In general, contact resistance is described as $\rho_c = R_c \times A_c \propto \exp\left[\frac{2\sqrt{\varepsilon m^*}}{\hbar}\left(\frac{\phi_{bn}}{\sqrt{N_D}}\right)\right]$,

where $\rho_c$ is the specific contact resistance, *Ac* is the contact area, $\varepsilon$ is the dielectric constant, $m^*$ is the electron mobility of the semiconductor, $N_D$ is the doping concentration, and $\varphi_{bn}$ is the Schottky barrier height. If we want to reduce contact resistance, there are two strategies we can do: (1) increasing the doping concentration or (2) decreasing the Schottky barrier height. For several years in semiconductor industry, the effect of raising doping concentration at the CMOS source/drain region is significant, but doping concentration is too hard to be increased in Ge because of the solid-state solubility limit. So how to decrease the Schottky barrier height is an important issue for improving the metal/Ge contact resistance.

## 1-2-3. Fermi-Level Pinning

Fermi-level pinning effect means that when metal contacts with Ge, the Schottky barrier height almost does not change with the metal work function, just like Fermi level is pinned at a local energy level in semiconductor band gap. In other words, the relationship of $\varphi_{bn} = \varphi_m - \chi$ has to be modified to $\varphi_{bn} = S\ (\varphi_m - \varphi_{CNL}) + (\varphi_{CNL} - \chi)$, where S is the pinning factor defined as $d\varphi_{bn}/d\varphi_m$ and $\varphi_{CNL}$ is the semiconductor charge neutrality level. The pinning factor ranges from 0 to 1. If S approaches to 1, it means that the pinning effect is not apparent. On the contrary, if S approaches to 0, the pinning effect is significant and the semiconductor Fermi level would be pinned at $\varphi_{CNL}$, which makes Schottky barrier height to be nearly a constant value with any metal.

Fermi-level pinning arises from surface states. If there are a lot of surface



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states at a local position in band gap as shown in Fig.1-2 [9], when Fermi-level moves to there, a large number of carriers would flow into another material which has a lower Fermi energy to make the Fermi level be aligned with each other. As a consequence, semiconductor Fermi level is almost not changed till the junction being electrostatic equilibrium.

Surface states come from two factors, surface dangling bonds and metal-induced gap states (MIGS). The MIGS is caused by metal electron wave function penetrating into the semiconductor band gap [10]. In general, Fermi level would be pinned at the semiconductor charge neutrality level (CNL). The position of the CNL is determined by the weights of the conduction band (acceptor-like states) and valence band derived states (donor-like states). For Ge, it is shown experimentally [6] that the CNL lies about 0.1 eV above the valence band edge. The CNL and Fermi level will affect the interface charges. If the Fermi level lies below the CNL, donor-like states would be empty and is positively charged. On the other hand, if the Fermi level is above the CNL, acceptor states would be filled with electron and is negatively charged. Energy considerations thus make it favorable for the Fermi level to be aligned with the CNL. The result of the Fermi level pinning is the Shottky barrier height on n-type Ge is higher than 0.5 eV no matter what kind of metal is used. Such a high Schottky barrier height results in a high contact resistance at source and drain, and thus a poor driving capability of the NMOSFET.

## 1-3 Methods for Fermi Level Depinning

Because of Fermi-level pinning, the Schottky barrier height of metal/Ge contact is difficult to be reduced using metals with different work functions. But recent experiments have demonstrated that Fermi level can be depinned by the

following two methods. The first method is surface passivation, which reduces the number of dangling bonds at the Ge surface so that surface states would be decreased and then the Fermi level pinning effect is relaxed. Surface passivation could be achieved through several techniques, such as $(NH_4)_2S$ solution immersion [11], implantation of sulfur into Ge [12], and $CF_4$ plasma treatment [13]. The second method is inserting a thin dielectric layer between metal and Ge as a tunneling barrier. Several dielectrics have been employed. They are $Si_3N_4$ [14,15], $Ge_3N_4$ [16], MgO [17,18], $Al_2O_3$ [19,20], and $TiO_2$ [21,22]. The role of the thin dielectric layer is theoretically considered as either to passivate the semiconductor surface states and/or reduce the metal-induced gap states by suppressing the penetration of wave function of the metal into the band gap of Ge. However, inserting an insulator may introduce a large tunneling resistance and limit the conduction current.

The tunneling resistance is dominated by tunneling width and the conduction band offset (CBO) between the inserted dielectric and Ge. It was pointed out that $TiO_2$ may be a good material since it has a nearly zero CBO to Ge so that the tunneling resistance is small [21]. The band diagrams of $Al_2O_3$/Ge and $TiO_2$/Ge are shown in Fig.1-3. By inserting $TiO_2$ as the depinning layer on Ge, the effective Schottky barrier height can be reduced to about 0.1 eV with Al/$TiO_2$/Ge structure [22].

The actual physical mechanism for the Fermi level depinning by inserting an dielectric layer has not been clear so far. Some researches indicated that there would be a dipole formed at the interface which causes additional potential drop to reduce the effective Schottky barrier height [15,23,24]. The other research considered that there would exist many fixed charges in the dielectric which also causes extra band bending so the Schottky barrier height is decreased [25].

## 1-4 Germanium Metal Contact

### 1-4-1. Metal Germanide

With CMOS devices scaling down, the parasitic resistance at the source/drain region contributes to larger and larger proportion of the total resistance. In order to solve this issue, self-aligned metal silicide (salicide) process had been proposed since 1980s. Around many kinds of metals, nickel silicide has the advantages of low sheet resistance, low forming temperature, no line-width dependence, and less silicon consumption during the silicide formation, so nickel silicide has been extensively used in current CMOS fabrication.

Although nickel germanide has higher resistivity than nickel silicide which would induce larger parasitic resistance at device source/drain region, nickel germanide is a better choice over the other metal germanides. It has been reported that high processing temperatures are required to form low resistivity titanium germanide (>800 ℃) and cobalt germanide (>500 ℃) [26], while nickel germanide can be formed at temperature as low as 270 ℃ [27,28]. Such a low processing temperature can be used with high-k gate stack without degradation, which makes nickel germanide more suitable for Ge device fabrication.

However, it has been found that nickel germanide is thermally unstable after annealing at temperatures above 500 ℃ with prominent grain growth and then broken into many small islands [26]. As a result, the film becomes discontinuous and the resistivity increases apparently. To improve the thermal stability of nickel germanide, alloying method has been proposed and widely studied, in which additive metals are introduced by alloyed target [29-31], or by inserting an ultrathin interlayer between nickel and germanium before germanidation [32-34]. With these metals incorporated in the nickel germanide films, the agglomeration effect can be

postponed.

### 1-4-2. Dopant Activation

In advanced CMOS processes, source/drain doping is formed by ion implantation because it can control doping concentration precisely and decouple the doping concentration and the doping profile. However, ion implantation produces many crystal defects in substrate due to energy transfer which would enhance dopant diffusion. Due to high diffusion coefficients and low solid-state solubility of n-type dopants in Ge, it is hard to achieve high percentage dopant activation [35,36]. Besides, n-type dopant diffusion is further enhanced by defects introduced by ion implantation [3], and high dosage implantation will aggravate this problem.

There were many methods trying to fabricate high doping concentration and shallow junction in Ge: (1) Laser annealing, with a nanosecond annealing and the small melting area, the dopant would not diffuse far from surface in such a short period and the doping concentration was very high because of the high temperature annealing [37,38]; (2) Co-sputter of P and Sb [39]; (3) Gas phase doping, with nearly no defect in substrate during annealing, the dopant diffusion effect could be suppressed and the device leakage current could be improved [40].

## 1-5 Motivation

This thesis will focus on how to improve the metal/Ge contact resistance through dielectric insertion and modified Schottky barrier (MSB) methods. The former method is trying to mitigate the Fermi level pinning effect and make Schottky barrier height decrease but it is not compatible with the self-aligned process, while the latter method is trying to enhance the dopant concentration at the metal/Ge

interface and it can be integrated with the self-aligned process.

As mentioned in the section 1-3, the Schottky barrier height can be reduced significantly by inserting an dielectric layer between metal and Ge. And it has been demonstrated that $TiO_2$ has the best efficiency. However, the physical mechanism and the process stability are not clear. In this these, $TiO_2$ and $Al_2O_3$ were used to reduce the Schottky barrier height on Ge. The thickness effect and the post deposition annealing effect on the contact are investigated. Besides, metals with different work functions are used to clarify how the $TiO_2$ layer affects the Fermi level pinning effect.

Recently, modified Schottky barrier (MSB) junctions have been proposed to improve the contact resistance. The MSB junction is a Schottky junction with a very thin and high doping concentration layer at the metal/semiconductor interface which can make the Schottky barrier thinner so that the tunneling resistance decreases. It can be accomplished by either dopant segregation (DS) [41-43] or implantation-to-silicide (ITS) [44- 47] process. The former process performs ion implantation before metal deposition on the semiconductor. During the silicidation process, the dopants are activated and segregated at the silicide-semiconductor interface by the snow-plow effect. On the contrary, in the ITS process, the dopants are implanted into silicide and then annealed at a low temperature to make them diffuse out from silicide to silicon and segregate at the interface. A thin and high doping profile at the edge of the silicide can be obtained. We try to use this process on Ge. Dopants are implanted into germanide instead of Ge so that the number of defects formed in substrate during ion implantation is reduced, which might mitigate dopant diffusion effect during dopant activation, and a thin and high concentration doping profile at germanide/Ge interface is expected. Finally, NiSi has lower sheet resistance and better thermal stability than NiGe. If a thin Si layer is inserted between Ni and Ge,

NiSi will be the main phase instead of the NiGe. The sheet resistance and thermal stability is expected to be improved. This thesis will examine this technique.

## 1-6 Thesis Organization

The organization of this thesis is described below. Chapter 1 introduces the characteristics of Ge and problems with n-type Ge metal contact. Methods to reduce contact resistance for Ge are also discussed. Chapter 2 describes the fabrication process of the samples, including the recipes of the etch process and device structures. Material and electrical analysis methods are also introduced.

Chapter 3 is studying on dielectric insertion junctions, first shows the current improvement by $Al_2O_3$ and $TiO_2$ inserted dielectric layers and different $TiO_2$ thicknesses, and how the dielectric insertion method affects the Schottky barrier height depinning, finally studying on the annealing effect of the dielectric insertion junctions. Chapter 4 is studying on modified Schottky barrier junctions, first shows current of the MSB junctions with different activation temperature and time, then describes the thermal stability problem of NiGe films and the improvement by incorporating Si into NiGe films, finally makes a comparison of doping profiles and junction currents between MSB and direct implantation to Ge samples.

Chapter 5 summarizes the experiment results and makes some conclusions on the Ge contact improvement by the two methods. Future works are also suggested.

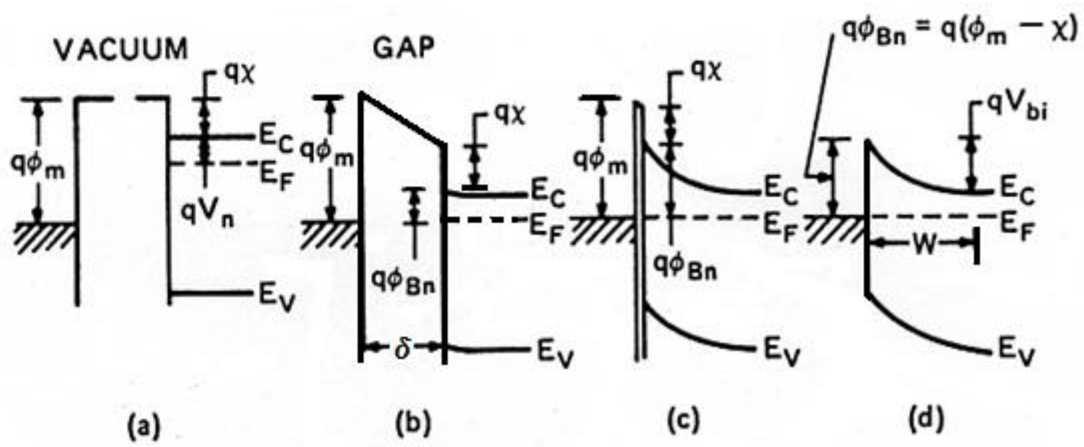
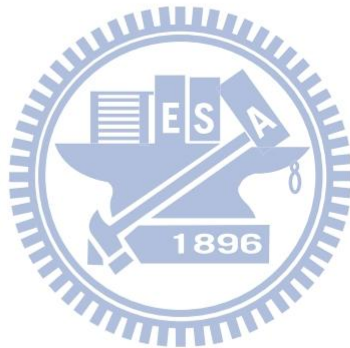



Fig. 1-1 Formation of the Schottky barrier as metal approaches semiconductor surface[8].



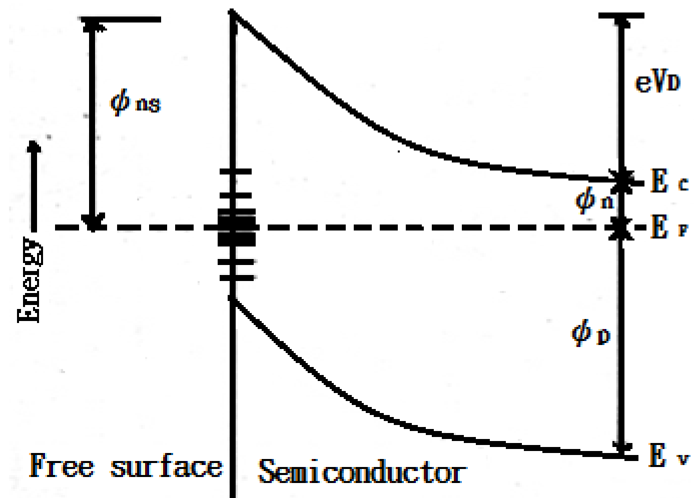



Fig.1-2 Schematic illustration of Fermi level pinning of a semiconductor surface with non-uniformly distributed surface states[9].

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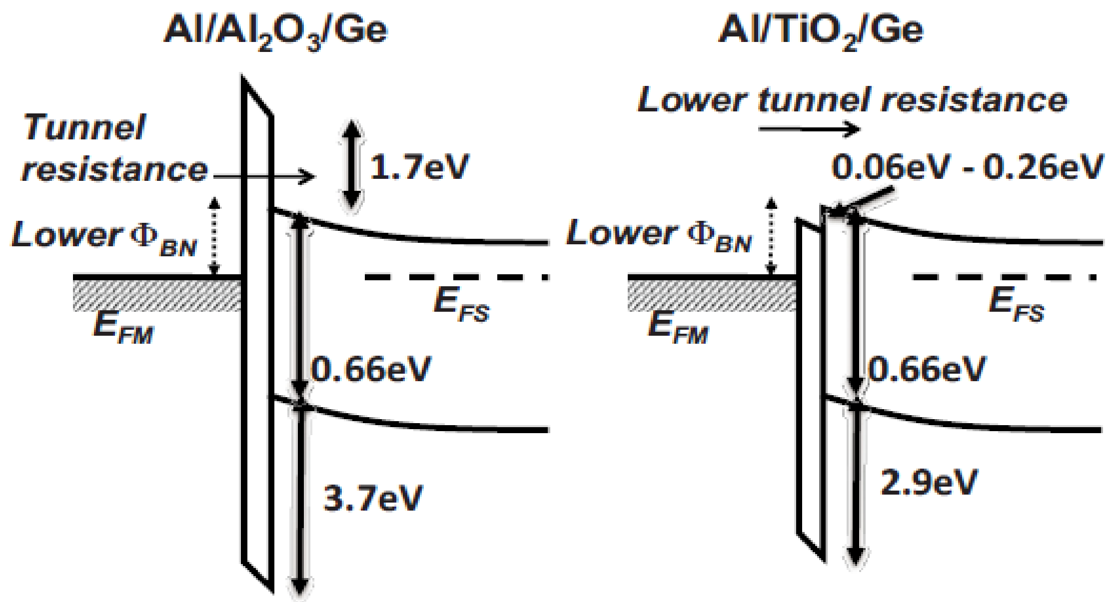
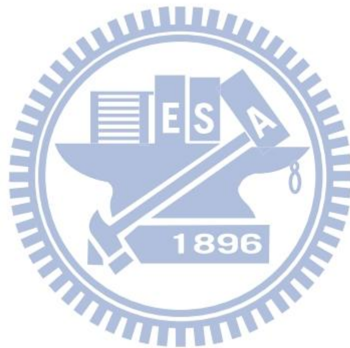



Fig. 1-3 Band diagrams of $Al_2O_3$/Ge and $TiO_2$/Ge structure [20].



# Chapter 2
# Experiments

## 2-1 Device Fabrication

### 2-1-1. Dielectric Insertion Layer Junctions

N-type Sb doped Ge wafer with resistivity about 0.01 ohm-cm was used. Samples were dipped in diluted HF solution ($H_2O$:HF = 20:1) and DI-water for one minute circularly by three times to clean the surfaces. Then samples were loaded to an atomic layer deposition (ALD) chamber to deposit thin dielectric layers immediately. There are two kinds of insertion layer in this study, one is $Al_2O_3$ and another is $TiO_2$. The $Al_2O_3$ layer was deposited using Trimethylaluminium (TMA) and $H_2O$ as precursors. The $TiO_2$ layer was deposited using Tetrakis(dimethylamino) titanium (TDMAT) and $H_2O$ as precursors. The deposition cycle was composed of one $H_2O$ pulse and one TMA/TDMAT precursor pulse at temperature 250 ℃. For the $Al_2O_3$ sample, the thickness is 1 nm grown by 11 cycles. For the $TiO_2$ sample, the thicknesses are 1 nm and 7 nm grown by 22 and 154 cycles, respectively. Some of these samples were then deposited by a 5-nm-thick TiN layer in the same ALD chamber using TDMAT as precursor and $N_2$ plasma.

After ALD deposition, samples with TiN layer were annealed in vacuum furnace at 300 ℃, 400 ℃, and 600 ℃ for 30 minutes. Then a 300-nm-thick Al was deposited on these samples by a thermal coater and the contact metal was patterned by a typical lithography process and high density plasma - reactive ion etching (HDP-RIE) with $Cl_2$ and $BCl_3$ as the reaction gas. Finally, after removing the native oxide on the sample backside by buffered oxide etchant (BOE), backside contact was completed with a 300-nm-thick Al deposition by a thermal coater. The schematic diagram of the

process flow is shown in Fig. 2-1.

The $TiO_2$-inserted samples without TiN contact metal were deposited with different metals including Pt, Ni, and Co and the contact metal was patterned by lift-off process. Pt and Ni were deposited by a sputter system. The deposition rate and thicknesses were 0.6 nm/min and 20 nm at Ar gas flow rate at 24 sccm, respectively, for Pt, and 3 nm/min and 100 nm at Ar gas flow rate at 100 sccm, respectively, for Ni. Co was deposited by an e-gun system with a deposition rate of 1.2 nm/min and a thickness of 80 nm. The other processes were identical to those of the samples using TiN as contact metal. The main process recipes of all samples are summarized in Table 2-1.

$Al_2O_3$ capacitors are made to extract the fixed charge density in the $Al_2O_3$ before and after annealing. N-type silicon wafer with resistivity of 15~25 Ω-cm was used. After RCA clean, a 5-nm-thick dry oxide was grown by a horizontal furnace, then samples were deposited a 1-nm-thick $Al_2O_3$ by an ALD system, the deposition condition was identical to that of the $Al_2O_3$ insertion layer described in previous sub-section. After deposition, samples were annealed in vacuum furnace at 300 ℃, 400 ℃, and 600 ℃ for 30 minutes. Then a 300-nm-thick Al was deposited by a thermal coater and patterned by typical lithography and lift-off process. Finally, after removing the native oxide on the sample backside by buffered oxide etchant (BOE), a 300-nm-thick Al was deposited by a thermal coater as backside contact.

### 2-1-2. Modified Schottky Barrier (MSB) Junctions

The Ge substrate and initial clean process are identical to those of the dielectric insertion samples. After cleaning, a 400-nm-thick Tetraethyl orthosilicate (TEOS) $SiO_2$ were deposited by a plasma enhanced chemical vapor deposition (PECVD)

system at 350 ℃. The contact area was patterned by typical lithography process and BOE etching. The residual photo-resist was removed by sonicating in acetone.

Both blanket and patterned samples were dipped in diluted HF solution ($H_2O$:HF = 100:1) to remove native oxide. A 20-nm-thick Si film was deposited on some samples by a sputter system, the process pressure is 7.6 mTorr and the Si deposition rate is 1.2 nm/min with Ar gas flow rate at 24 sccm. After Si deposition, samples were annealed in a vacuum furnace at 400 ℃ for 30 minutes to densify the Si film. Using typical lithography process, the Si outside contact hole was etched by poly-Si etchant ($HNO_3$:$H_2O$: $NH_4F$ = 64:33:3) and residual photo-resist was removed by sonicating in acetone. Then after dipping in diluted HF solution ($H_2O$:HF = 100:1), samples with/without Si film were all sputtered a Ni/TiN film to a thickness of 10 nm/10 nm. The Ni deposition rate is 3 nm/min with Ar gas flow rate at 100 sccm. The TiN deposition rate is 4.2 nm/min with Ar gas flow rate at 100 sccm and $N_2$ gas flow rate at 4 sccm.

After the Ni/TiN deposition, samples were annealed in $N_2$ ambient by a rapid thermal annealing (RTA) system at 400 ℃, 500 ℃, 550 ℃, 600 ℃ for 30 seconds to form nickel germaniude. The TiN and the unreacted Ni was selectively etched by hot HCl solution.

The 500 ℃ annealed samples were implanted by $As^+$ at 10 keV to a dose of $5x10^{15}$ $cm^{-2}$. Direct implantation into Ge samples with implantation energy 10 keV to a dose of $2x10^{15}$ $cm^{-2}$ were also fabricated. Before dopant activation, a 10-nm-thick TEOS oxide was deposited to avoid dopant out-diffusion. The MSB annealing was performed in a vacuum furnace with different thermal budgets. The annealing conditions are summarized in Table 2-2. After dopant activation, the capped oxide was etched by diluted HF solution ($H_2O$:HF = 100:1) and the device fabrication was finished by a 300-nm-thick Al deposition on sample backside by a thermal coater. The

schematic diagram of this process is in Fig. 2-2.

## 2-2 Material Analysis and Electrical Measurement

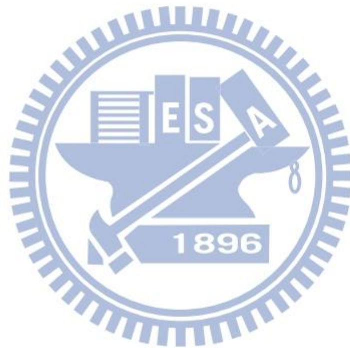
Several materal analysis techniques including X-ray Diffraction (XRD), Transmission Electron Microscopy (TEM), Scanning Electron Microscopy (SEM), and Spreading Resistance Profiling (SRP) were used in the study. Sheet resistance was measured by a four point probe system on blanket samples. Device forward/reverse bias current-voltage characteristics were measured by the semiconductor analyzer of model Agilent 4156C.

XRD analysis is used to observe the crystallization condition of the $TiO_2$ layer after annealing at different temperatures; it can tell us how annealing process affects the crystalline structure of the $TiO_2$ layer. TEM analysis is used to inspect the microstructure of the $TiO_2$/Ge structure to reveal if there has an interfacial layer formation after annealing.

SEM can help us to inspect the surface morphology of the nickel germanide. In general, nickel germanide surface would be rough due to agglomeration effect after high temperature annealing. With SEM image, we can see how agglomeration effect affects the nickel germanide resistance. SRP is used to analyze the dopant distribution of the MSB junction after thermal activation.

Schottky barrier height was extracted by the thermionic emission model, which is given by $J = \left( A^{*}T^{2}e^{-\frac{q\phi_{Bn}}{kT}} \right)\left( e^{\frac{qV}{kT}} - 1 \right)$, where *Ac* is the Richardson constant and T is the absolute temperature. If V is negative and -V>>3kT/q, then the function can be simplified to $\ln(J/A^{*}T^{2}) = -q\varphi_{Bn}/kT$. Plot ln(J/A*T) as a function of q/kT, the slope is $-\varphi_{Bn}$. Consider the dielectric insertion samples, because of the tunneling effect; the

function has to be multiplied by an additional tunneling term, which is proportional to tunneling width and tunneling barrier height [19]. But in general, these two factors do not change with temperature, so we can still extract the Schottky barrier height by the same procedure as if there is no insertion layer.

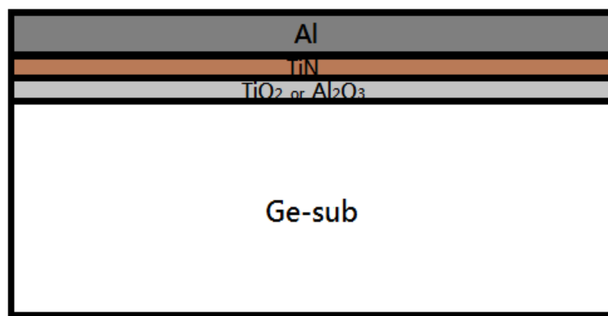


| | Thickness | Annealing recipe | Contact metal |
|---|---|---|---|
| $Al_2O_3$ | 1nm | 300 °C for 30min<br>400 °C for 30min<br>600 °C for30min | TiN |
| $TiO_2$ | 1nm<br>7nm | 300 °C for 30min<br>400 °C for 30min<br>600 °C for30min | TiN<br>Co<br>Ni<br>Pt |

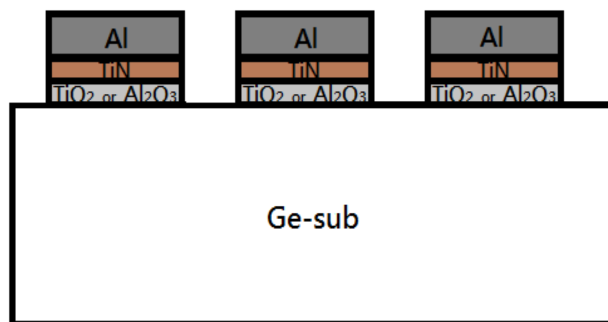
Table 2-1 The main process recipes of depinning layer junction samples.

| | Activation temperature | Activation time (minutes) |
|---|---|---|
| NiGe | 400 °C, 450 °C, 500 °C<br>for 30 minutes | 10, 30, 50, 70 at 500 °C |
| NiGe with Si | 550 °C for 30 minutes | 10, 30, 50, 70 at 550 °C |

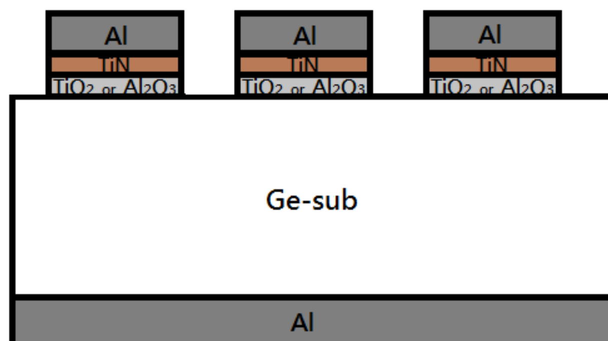
Table 2-2 The annealing conditions of MSB junction samples.




1. **HF Dip.**
2. **Use ALD to grow $TiO_2$ or $Al_2O_3$ layer and TiN layer.**
3. **300nm Al deposited by a thermal coater.**

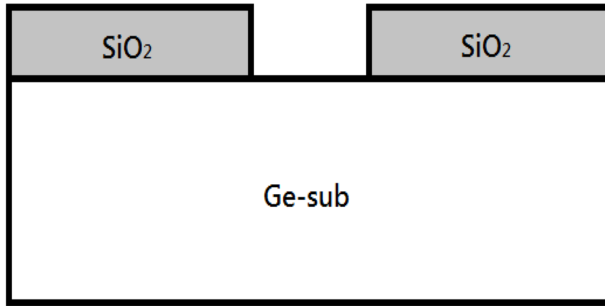



4. **Contact holes are defined by Lithography process.**
5. **HDP-RIE dry etching.**
6. **Remove residual PR.**

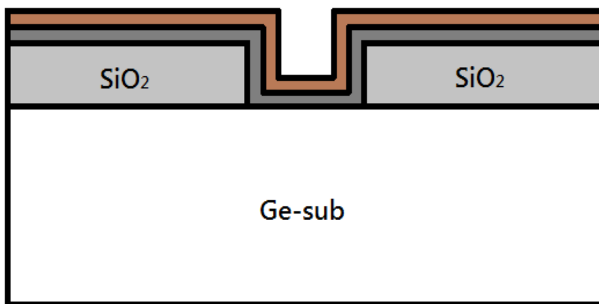



7. **Al backside contact deposited by a thermal coater.**

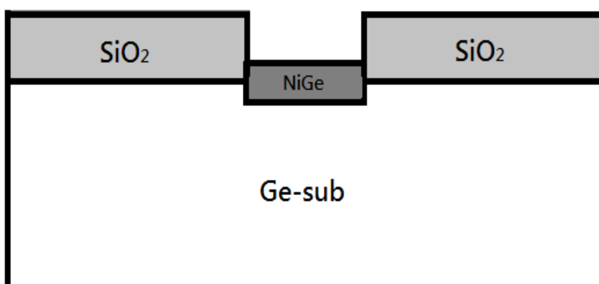
Fig. 2-1 The process flow of depinning layer junction fabrication.



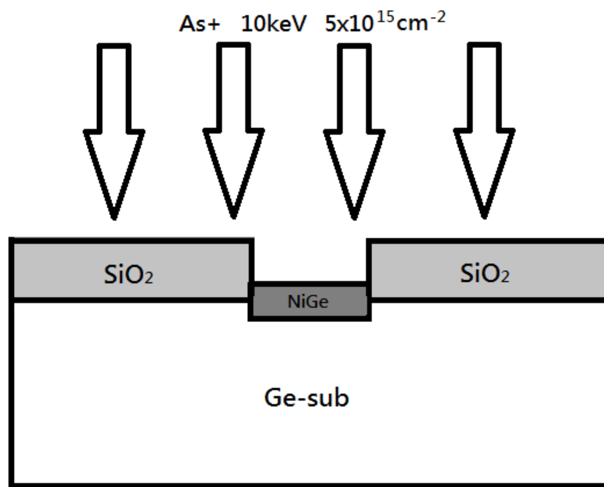

6. **HF Dip.**
7. **Use PECVD to grow TEOS oxide 400nm.**
8. **Active region define by Lithography process.**
9. **Oxide etched by BOE and remove residual PR.**



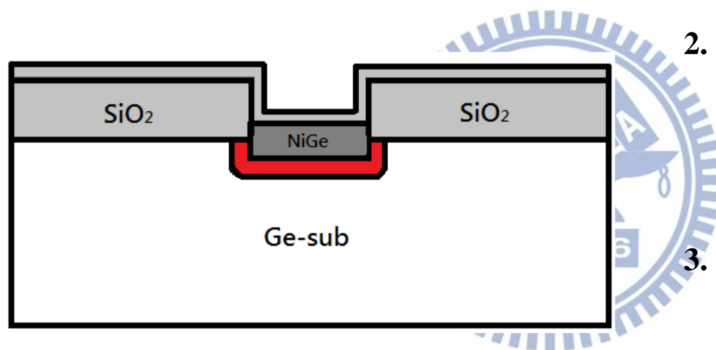

10. **Ni 10nm and TiN 10nm are deposited by a sputter system.**



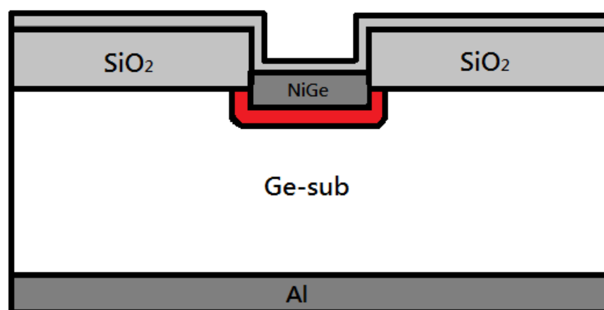

11. **Germanidation by a RTA system.**
12. **Residual metals are etched by hot HCl solution.**




1. **Implanted by As$^+$ 10keV with dose 5x15 cm$^{-2}$**




2. **TEOS oxide 10nm deposited by a PECVD system.**
3. **Doping activation by a vacuum furnace.**




4. **Oxide etched by diluted HF solution.**
5. **Al backside contact deposited by a thermal coater.**

Fig. 2-2 The process flow of MSB junction fabrication.

# Chapter 3
# Dielectric Insertion Junctions

## 3-1 Introduction of Dielectric Insertion Method

N-type Ge suffers from large contact resistance due to Fermi level pinning at the charge neutrality level which is about 0.09 eV above the Ge valence band. It has been reported that inserting a thin dielectric layer between metal and semiconductor could alleviate the Fermi level pinning effect [14]. Although this dielectric layer could reduce the Schottky barrier height, it also introduces large tunneling resistance due to the conduction band offset between the dielectric layer and Ge. If we want to obtain low contact resistance, the thickness of the dielectric layer has to be very thin to attain low tunneling resistance. Besides, the actual physical mechanism of this method has not been clear so far. There are three major explanations: (1) These dielectric layers can block the electron wave function from metal to semiconductor and therefore decrease the number of surface defects [14]. (2) There would be a dipole formed at metal/semiconductor interface which cause extra voltage drop to reduce the Schottky barrier height [15,23,24]. (3) There would be some fixed charges in the dielectric layer which could also cause extra voltage drop in the dielectric layer [25]. In this chapter, sequential experiments are designed to clarify which mechanism dominates the Schottky barrier height modulation.

## 3-2 Currents of the two Dielectric Insertion Junctions – $Al_2O_3$ & $TiO_2$

Fig.3-1 shows the current-voltage (I-V) characteristics of the Al/Ge diode. According to the function $\varphi_{bn} = \varphi_m - \chi$ , the $\chi$ of Ge is about 4.05 eV and the $\varphi_m$ of

Al is about 4.1 eV so the ideal Shottky barrier height is about 0.05 eV, but the Shottky barrier height is about 0.53 eV extracted from the I-V curve, which confirms severe Fermi level pinning effect on Ge.

Fig.3-2 and Fig.3-3 show the I-V characteristics and the Schottky barrier heights, respectively, of the junctions with 1-nm-thick $Al_2O_3$, 1-nm-thick $TiO_2$, and 7nm-thick $TiO_2$ dielectric layers. The contact metal is a 5-nm-thick TiN layer deposited by ALD process. The forward/reverse current ratio of these three samples decreases apparently in comparison with that of the simple Al/Ge diode. These results indicate that the Schottky barriers heights are very low. It can be also found that although the 1-nm-thick $Al_2O_3$ sample has near Schottky barrier height with 1-nm-thick $TiO_2$ sample, its current density is still much smaller than 1-nm-thick $TiO_2$ sample because the large conduction band offset of $Al_2O_3$ to Ge limits the current conduction [22]. On the contrary, $TiO_2$ has nearly zero conduction band offset to Ge so it can not only decrease the Schottky barrier height but also make the tunneling resistance small.

In general, thicker dielectric layer will introduce higher tunneling resistance under the same tunneling barrier height. However, it is observed that the Schottky barrier height of the 7-nm-thick $TiO_2$ sample is smaller than that of the 1-nm-thick $TiO_2$ sample. This phenomenon has been reported previously, but was not discussed [22]. To clarify this effect, we first consider that thicker dielectric layer would suppress the MIGS effect more effectively because the metal electron wave function is exponentially decayed in the dielectric layer. Thus, the number of surface states caused by the MIGS will decrease with the increase of the dielectric layer thickness. If the MIGS effect is mitigated, the Fermi level pinning effect is mitigated, too. To verify this postulation, different metals are used as contact metal with 1-nm-thick and 7-nm-thick $TiO_2$ layers to observe the Fermi level pinning effect of these junctions.

## 3-3 Fermi Level Pinning Effect of $TiO_2$ Dielectric Insertion Junctions

Fig.3-4 and Fig.3-5 show the I-V characteristics of junctions with different contact metals. Four kinds of metals are used in this experiment; they are Pt, Ni, Co, and TiN which have work functions about 5.65 eV, 5.1 eV, 5 eV, and 4.5 eV, respectively. Metal with further lower work function is not used in this experiment because the Schottky barrier height of the 7-nm-thick $TiO_2$ sample would be very small (about 0.04 eV for TiN which work function is 4.5 eV) so that we can't extract Schottky barrier height accurately due to most supply voltage is consumed on the parasitic resistance instead of the Schottky barrier. With higher work function metal, the current densities are lower, which indicates that Schottky barrier height increases with the work function.

Fig.3-6 shows the extracted Schottky barrier height of the 1-nm-thick and 7-nm-thick $TiO_2$ samples with different contact metals. The Schottky barrier height of the pure metal/Ge junctions is also shown in the figure 6. The slopes of the linear regression lines give the pinning factors S. The pinning factor is about 0.05 for the pure Ge junction which indicates the severe Fermi level pinning effect on Ge. For the junctions with $TiO_2$ insertion layer, the pinning factors are about 0.14 and 0.12 for the junctions with 1-nm-thick and 7-nm-thick $TiO_2$, respectively. These values are larger than that of the pure Ge junction which means that the Fermi level pinning effect is mitigated with the $TiO_2$ insertion layer. However, the pinning factors are still much smaller than 1. In the case of complete depinning, the pinning factor should approach to 1; the small values of the pinning factors indicate that the Fermi level pinning effect is not mitigated completely by the $TiO_2$ insertion layer.

The improvement of pinning factor compared to pure Ge may come from alleviating of MIGS effect. However, it is worthy to notice that the pinning factors of both $TiO_2$ thicknesses are about the same, which indicates that the depinning effect of the 7-nm-thick $TiO_2$ is not better than that of the 1-nm-thick $TiO_2$. It is thus inferred that the lower Schottky barrier height of the 7-nm-thick $TiO_2$ sample than the 1-nm-thick sample is not due to the thicker dielectric layer suppresses the MIGS effect more effectively, but because that the pinning position is changed more for thicker $TiO_2$ layer. The changed pinning position may result from two factors, fixed oxide charges or dipoles formed at $TiO_2$/Ge interface, both can introduce an additional potential drop in the current conduction path and results in the reduction of the Schottky barrier height. The band diagrams of both cases are shown in Fig. 3-7.

To understand how fixed oxide charges affect the Schottky barrier height, we can examine the annealing effect on the junctions with insertion layer because the fixed oxide charges will be reduced after annealing.

## 3-4 Annealing Effect of Dielectric Insertion Junctions

Fig.3-8 shows the I-V characteristics of the TiN/$Al_2O_3$/Ge junctions before and after annealing in vacuum at 300 ℃, 400 ℃ and 600 ℃ for 30 minutes. It is observed that with the increased annealing temperature, the currents of the junctions decreased at all annealing temperatures. Chui and coworkers have also found this phenomenon, and they proposed that the $Al_2O_3$ layer has some fixed charges that cause potential drop and change the electric field in the oxide. They observed that the capacitance-voltage curves of the MIS capacitors with different $Al_2O_3$ dielectric thicknesses would be overlapped after annealing, so they considered the oxide charges in the $Al_2O_3$ were eliminated which caused the junction current decreased [25]. Only

one annealing condition was performed in their work. In this thesis, the junction current further decreases after 600 ℃ annealing. If the current reduction is due to the annealing of fixed charges, it must be supposed that the fixed charges are not completely eliminated at 300 ℃ for 30 minutes.

To verify the influence of fixed charges on the Schottky barrier height modulation, $Al_2O_3$ capacitor was fabricated to calculate the number of fixed charges in the 1-nm-thick $Al_2O_3$ film. Because the 1-nm-thick $Al_2O_3$ is too thin so that the tunneling current would be too high and the capacitance-voltage characteristic cannot be measured, a 5-nm-thick $SiO_2$ was thermally grown to block the leakage current. Fig.3-9 shows the C-V characteristics of the Al/$Al_2O_3$(1nm)/$SiO_2$(5nm)/Si and the Al/$SiO_2$(5nm)/Si capacitors. The difference of the mid-gap voltage between the two samples is about 0.05 V. According to the function $Qox = Cox \times \Delta V$, where Qox is oxide charge density, Cox is accumulation capacitance, and $\Delta V$ is mid-gap voltage difference, the Qox is about $2.27 \times 10^{11}$ $cm^{-2}$ in the 1-nm-thick $Al_2O_3$ layer. The capacitance of a 1-nm-thick $Al_2O_3$ capacitor is about $7.8 \times 10^{-6}$ $F/cm^2$, to produce a 0.1 V voltage drop, the oxide charges have to be $4.87 \times 10^{12}$ $cm^{-2}$. We can infer that the number of fixed charges in such a thin dielectric layer is not sufficient for producing a large voltage drop to make the Schottky barrier height shifts more than 0.3 eV. Thus, it is recommended that the Schottky barrier height modulation of the $Al_2O_3$ inserted junction is mainly caused by interface dipoles.

Fig.3-10 and Fig.3-11 show the I-V characteristics of the 1-nm-thick and 7-nm-thick $TiO_2$ inserted junctions, respectively, before and after annealing in vacuum at 300 ℃, 400 ℃, and 600 ℃ for 30 minutes. The corresponded Schottky barrier heights are shown in Fig.3-12. Similar to the $Al_2O_3$-inserted junctions, the conduction current decreases after annealing. It is noticed that the Schottky barrier heights of the annealed 7-nm-thick $TiO_2$ junction is still lower than that of the annealed 1-nm-thick

$TiO_2$ junction. If the Schottky barrier height modulation mechanism of the $TiO_2$ inserted junction mainly results from the fixed charges in $TiO_2$ and these charges are annealed-out completely, the Schottky barrier height of the 7-nm-thick $TiO_2$ junction should equal to that of the 1-nm-thick $TiO_2$ junction. However, this prediction conflicts with the experimental results. Therefore, it is recommended that the Schottky barrier height modulation of the $TiO_2$-inserted junction is mainly caused by interface dipoles, too. According to Fig.3-12, the trend of the increase of Schottky barrier height with annealing temperature of the two junctions are similar, probably there is a same mechanism for the increase of Schottky barrier height after annealing of these two junctions.

To observe if there is a new interfacial layer formed after annealing, the cross-sectional structure of the 600 ℃ annealed TiN/$TiO_2$/Ge junction was inspected by the high-resolution TEM and the micrograph is shown in Fig.3-13. It is clearly that there is no interfacial layer formed at the $TiO_2$/Ge interface and the TiN/$TiO_2$ interface. The thin layer between Al and TiN is probable AlOx layer according to EDS analysis which was formed during Al deposition by a thermal coater. It would not affect the Schottky barrier height. The thicknesses of the deposited $TiO_2$ and TiN layers are 7 nm and 5 nm, respectively. Their thicknesses after annealing are almost the same with the as deposited thicknesses which means that no chemical reaction between the three layers. This result suggests that the Schottky barrier height increment is not due to new layer formation after 600 ℃ annealing.

Fig.3-14 (a)-(c) show the XRD spectra of the 7-nm-thick $TiO_2$-inserted junction after annealing at 300 ℃, 400 ℃, and 600 ℃ for 30 minutes, respectively. The $TiO_2$ and TiN layers remain in amorphous state after 400$^o$C annealing. The (110) crystalline phase of $TiO_2$ is detected on the 600 ℃ annealed sample, which means that with the increasing annealing temperature, the $TiO_2$ layer is gradual crystallized. If a

dielectric layer is crystallized, the dielectric constant will be higher than that in amorphous state, so the capacitance of $C_{OX} = \varepsilon / T_{OX}$ would be higher and the voltage drop of $\Delta V = Q_{OC} / C_{OX}$ would be smaller. The $Q_{OC}$ here includes fixed charges and interface dipole charges. It is thus postulated that the crystallization of the inserting layer is one possible explanation of Schottky barrier height shift after annealing. Thicker dielectric results in smaller capacitance Cox, and the voltage drop of $\Delta V = Q_{OC} / C_{OX}$ would be larger so that the Schottky barrier heights are modulated more. The more effective Schottky barrier height modulation by 7-nm-thick $TiO_2$ than that by 1-nm-thick $TiO_2$ might be explained by this postulation.

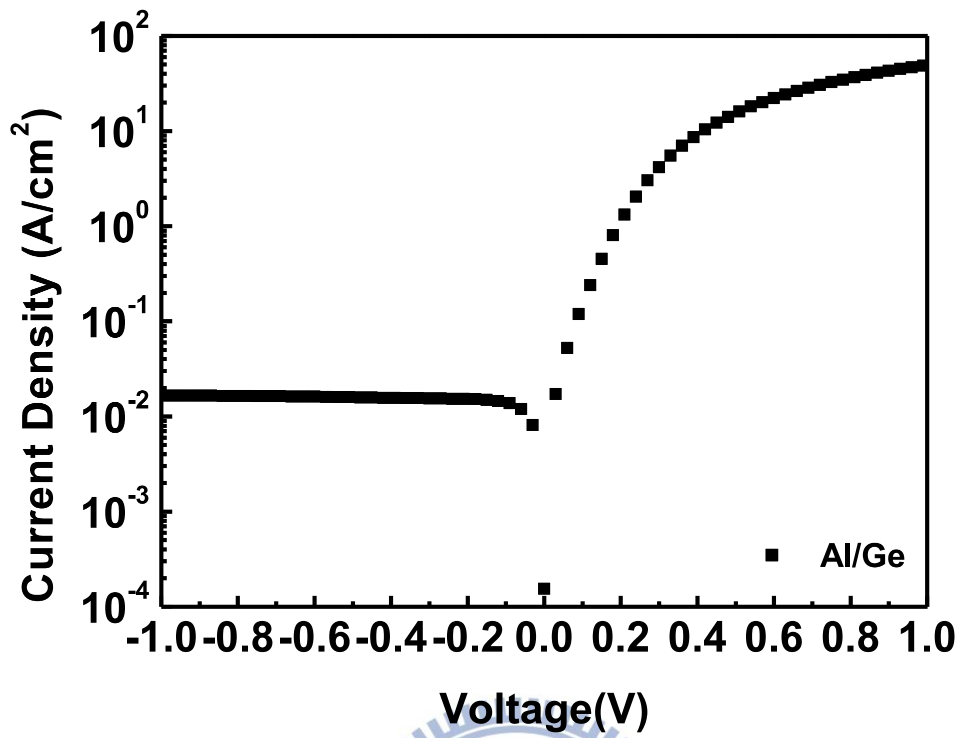
## 3-5 Summary of Dielectric Insertion Junctions

The effect and mechanism of Schottky barrier height modulation of the metal/n-type Ge Schottky junction by inserting dielectric layer are examined. Both $Al_2O_3$ and $TiO_2$ insertion layer result very low Schottky barrier height than the sample without insertion layer. The conduction current of the $Al_2O_3$–inserted junction is smaller than that of the $TiO_2$–inserted junction because of the larger conduction band offset of $Al_2O_3$ to Ge.

Different metals are used to determine the Fermi-level pinning factor. The pinning factor of the $TiO_2$-inserted junction is larger than that of the simple metal/Ge junction but is still much smaller than 1. This result indicates that the Fermi level pinning effect is only slightly mitigated by the insertion layer. The pinning factor does not increases with the increase of the insertion layer thickness, which indicates that the modulation of Schottky barrier height is not due to the suppression of the MIGS effect by the inserted dielectric layer. The amount of the fixed charges in the inserted dielectric is extracted by a MIS capacitor. The value is too low to produce the

apparent Schottky barrier height modulation. It is recommended that the mechanism of the Schottky barrier modulation by inserting dielectric layer mainly comes from the interface dipoles.

The Schottky barrier height of the dielectric inserted junction is not thermally stable. The Schottky barrier height increases with the increase of annealing temperature. Since no interfacial layer formation can be observed at the $TiN/TiO_2$ and the $TiO_2/Ge$ interfaces, it may due to the crystallization of the dielectric layer so that the dielectric constant is increased.



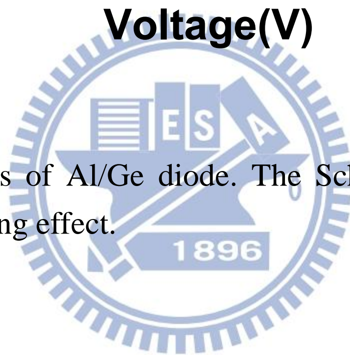




Fig. 3-1 I-V characteristics of Al/Ge diode. The Schottky barrier is large due to Fermi level pinning effect.

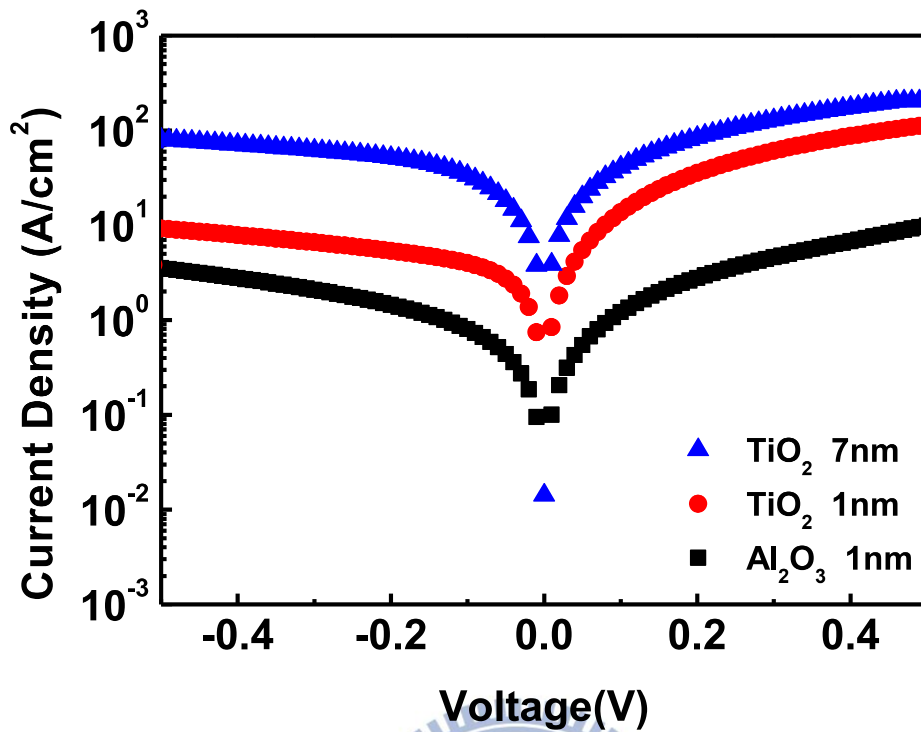



Fig. 3-2 I-V characteristics of the junctions with 1-nm-thick $Al_2O_3$, 1-nm-thick $TiO_2$, and 7-nm-thick $TiO_2$ dielectric layers. The junction currents of 1-nm-thick $Al_2O_3$ are smaller than 1-nm-thick $TiO_2$ because of the larger conduction band offset to Ge. It is noticed that the current of 7nm-$TiO_2$-inserted junction is larger than the 1nm-$TiO_2$-inserted junction.

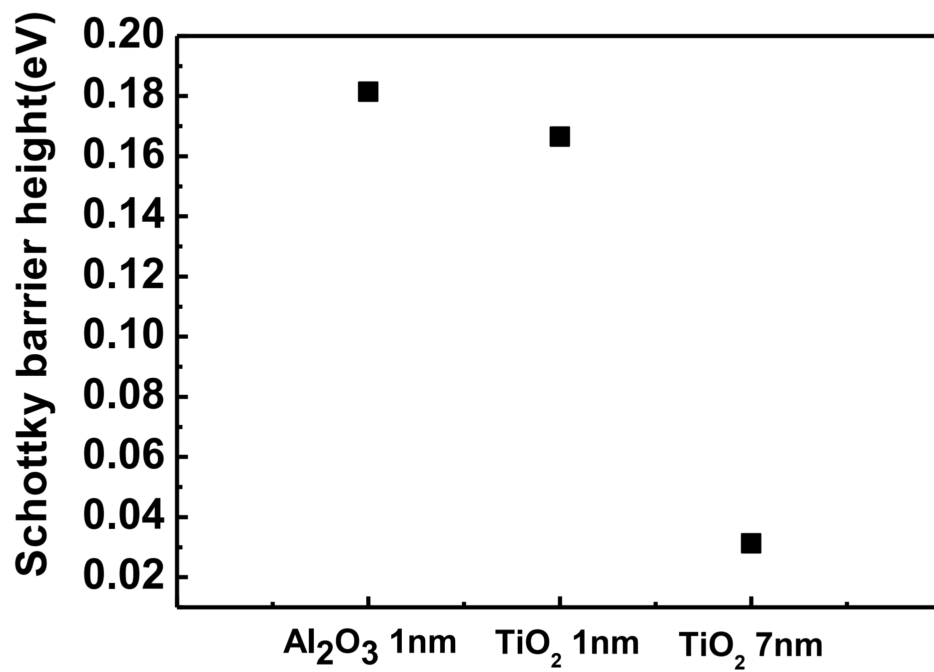



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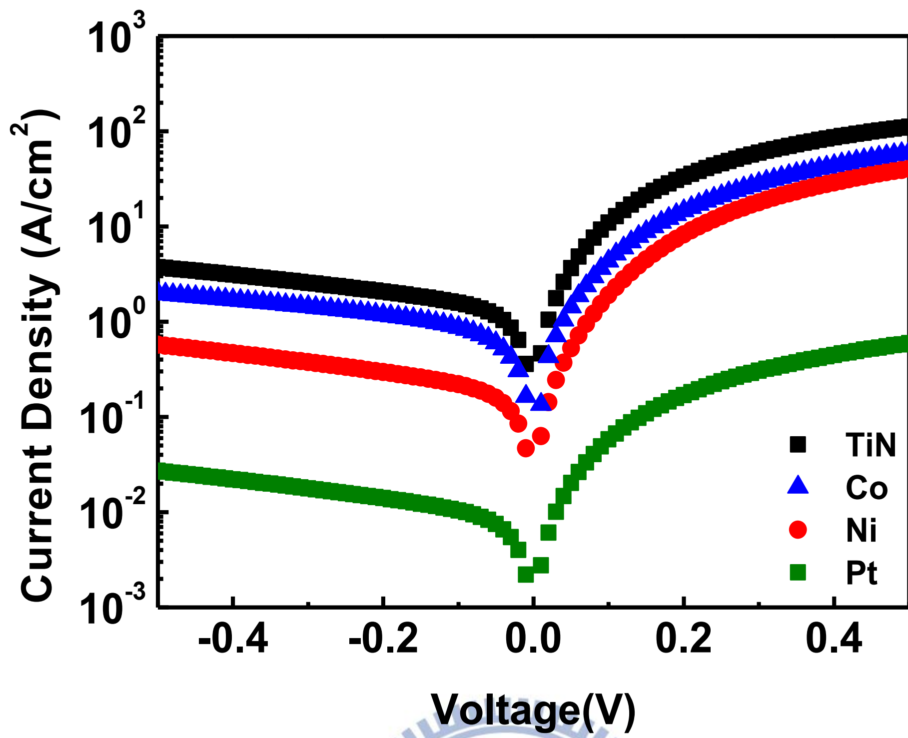
Fig. 3-3 Schottky barrier height of the junctions with 1-nm-thick $Al_2O_3$, 1-nm-thick $TiO_2$, and 7-nm-thick $TiO_2$ dielectric layers. 7nm $TiO_2$-inserted junction has lowest Schottky barrier height.



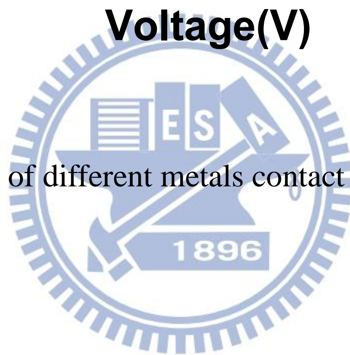
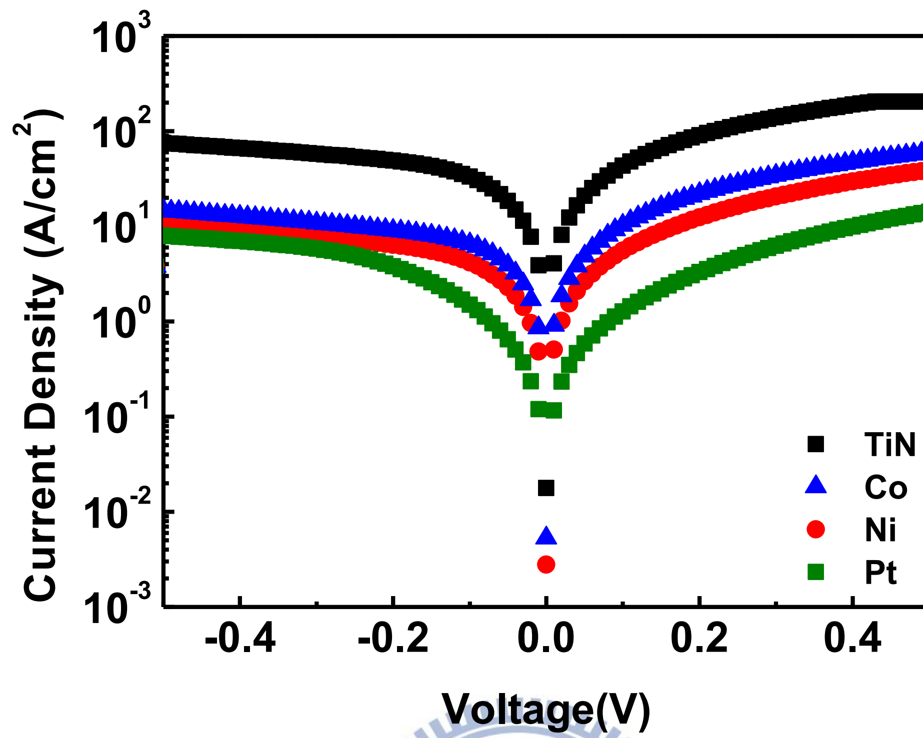



Fig. 3-4 I-V characteristics of different metals contact on 1nm-$TiO_2$-inserted junction.



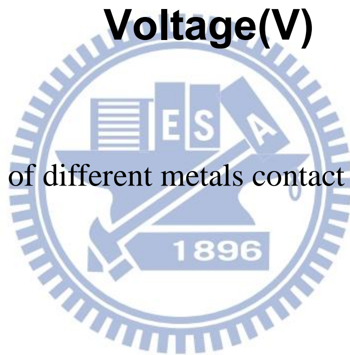




Fig. 3-5 I-V characteristics of different metals contact on 7nm-$TiO_2$-inserted junction.

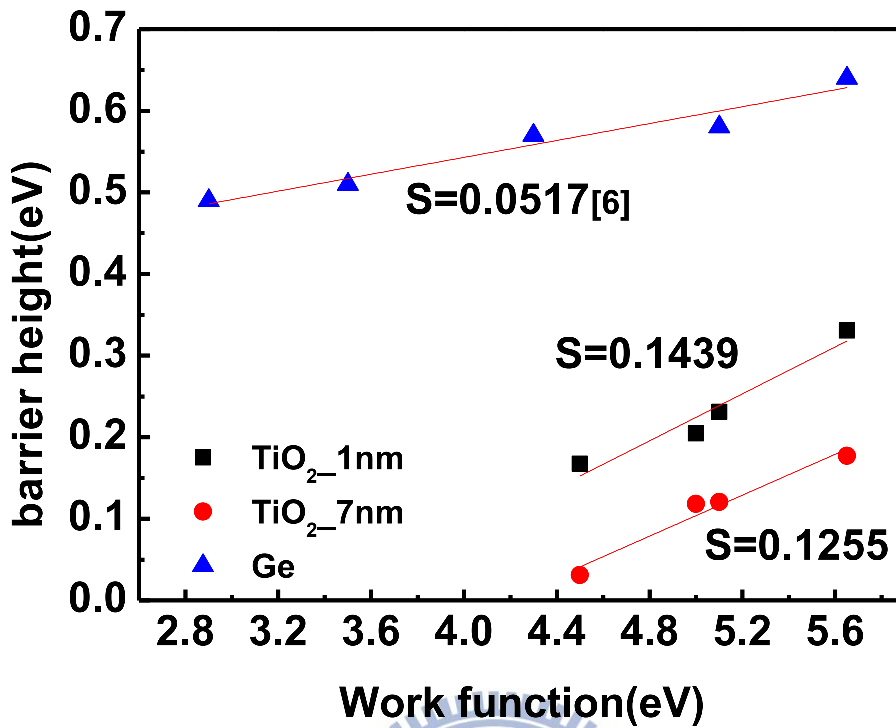



Fig.3-6 Schottky barrier heights versus Work functions of 1 and 7nm $TiO_2$-inserted junctions, pure metal/Ge junctions is also shown. The slopes of the linear regression lines give the pinning factors S. The pinning factors of the two samples are larger than the pure Ge junction but are still much smaller than 1 which indicatess the Fermi level pinning effect is just slightly mitigated. The pinning factor of 7nm $TiO_2$-inserted junction is not larger than the 1nm $TiO_2$-inserted junction indicates the lower Schottky barrier height is due to the pinning position shifted more for 7nm $TiO_2$-inserted junction.

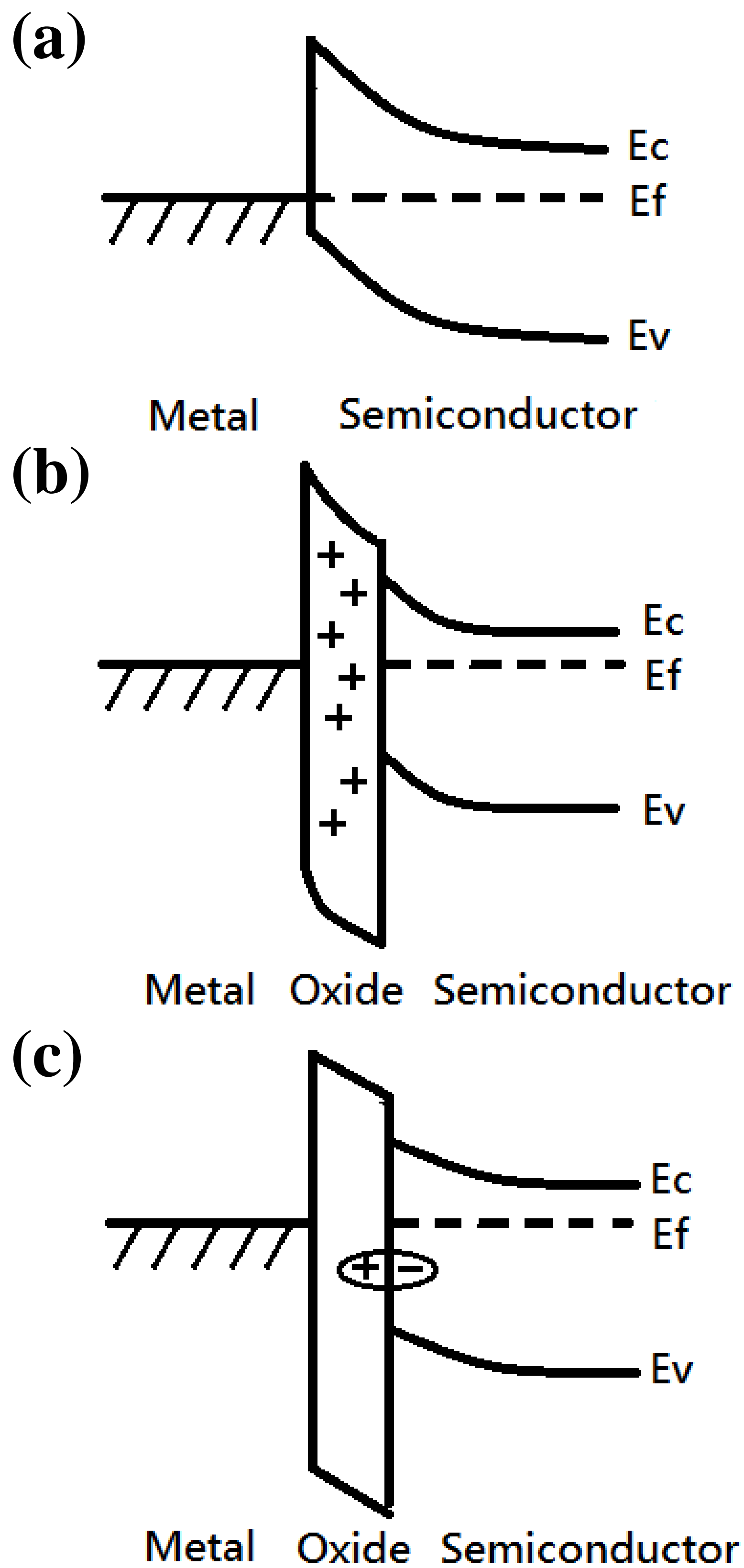



Fig. 3-7 Band diagrams of dielectric insertion junctions with (b) fixed oxide charges (c) dipoles at interface.

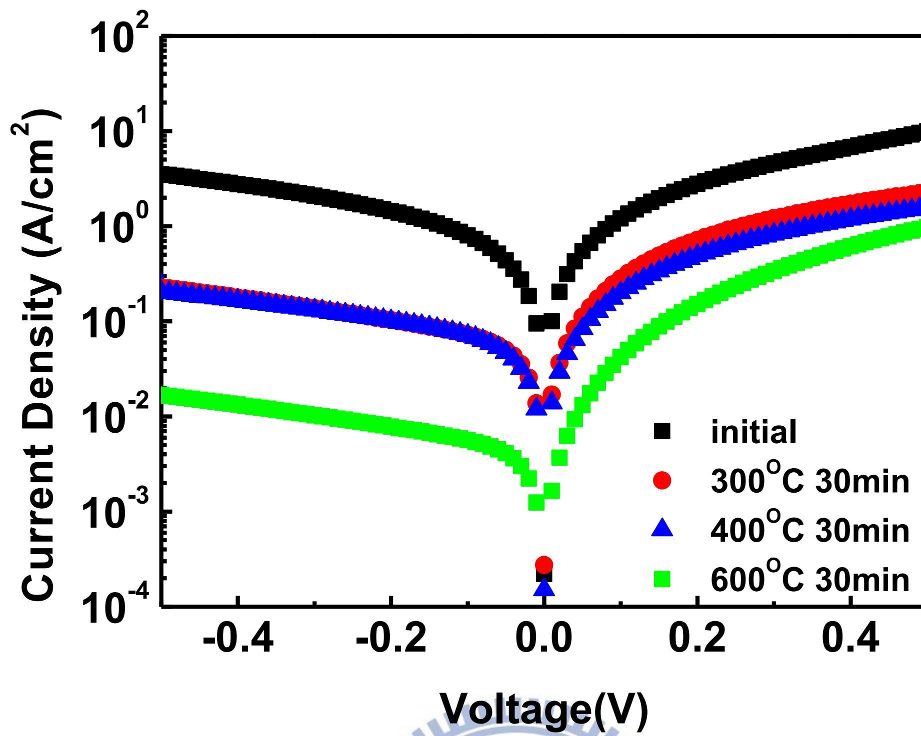



Fig. 3-8 I-V characteristics of the TiN/$Al_2O_3$/Ge junctions before and after annealing at 300 ℃, 400 ℃ and 600 ℃ for 30 minutes. Currents are all decreased with increased annealing temperature.

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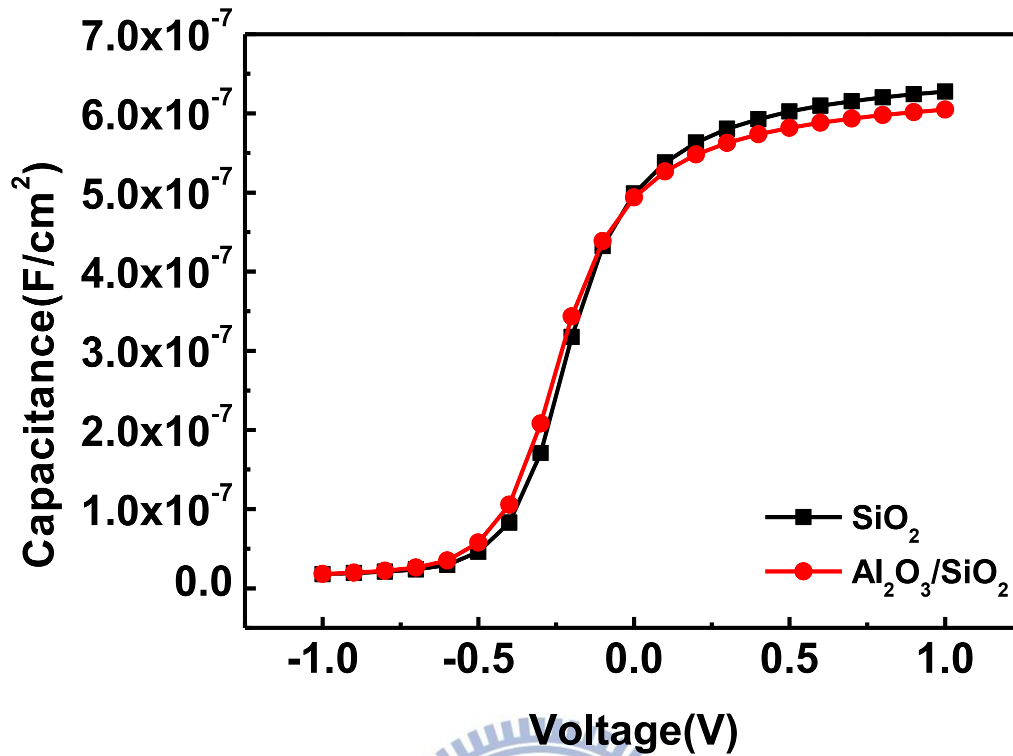



Fig. 3-9 C-V characteristics of the $Al/Al_2O_3$(1nm)/$SiO_2$(5nm)/Si and the $Al/SiO_2$(5nm)/Si capacitors. The amount of fixed oxide charges in the 1nm $Al_2O_3$ is a little.

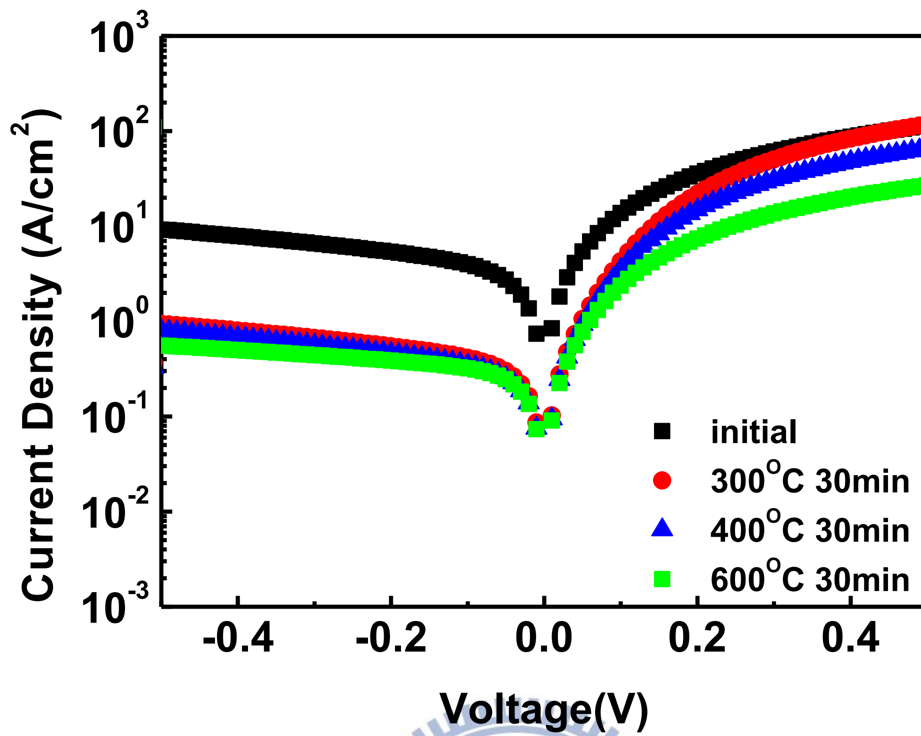



Fig. 3-10 I-V characteristics of the 1-nm-thick $TiO_2$ inserted junctions before and after annealing at 300 ℃, 400 ℃ and 600 ℃ for 30 minutes. Currents are all decreased with increased annealing temperature.

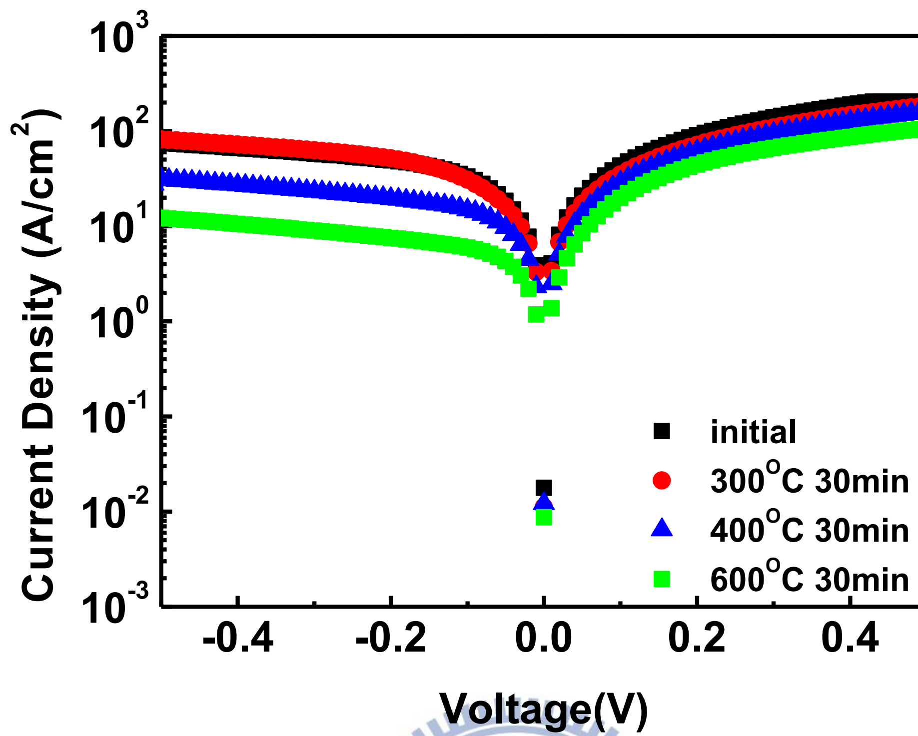



Fig. 3-11 I-V characteristics of the 7-nm-thick $TiO_2$ inserted junctions before and after annealing at 300 ℃, 400 ℃ and 600 ℃ for 30 minutes. As same as 1-nm-thick $TiO_2$ inserted junction, currents are all decreased with increased annealing temperature.

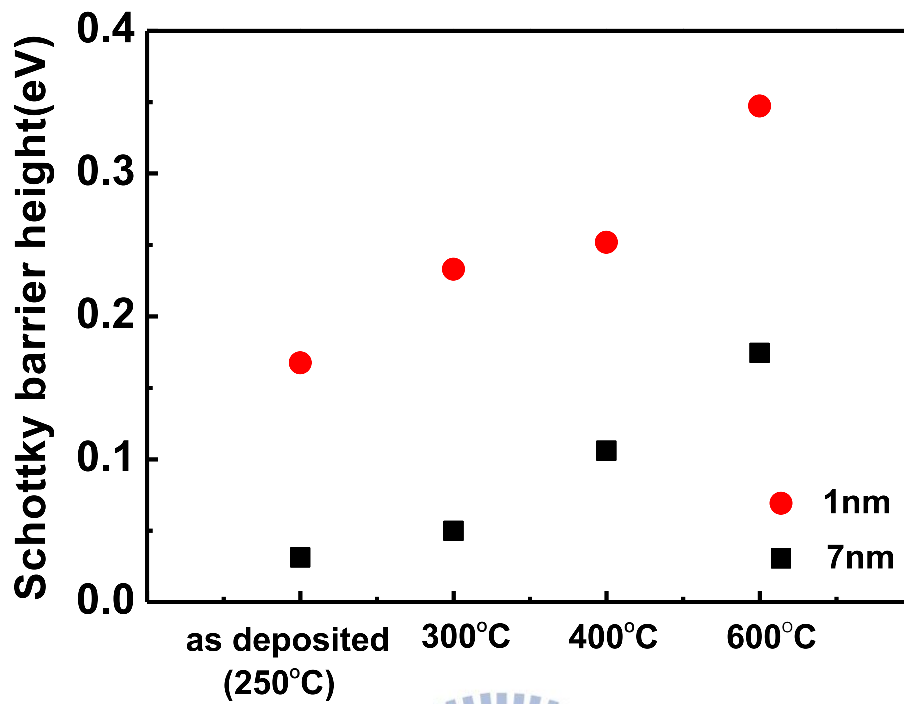
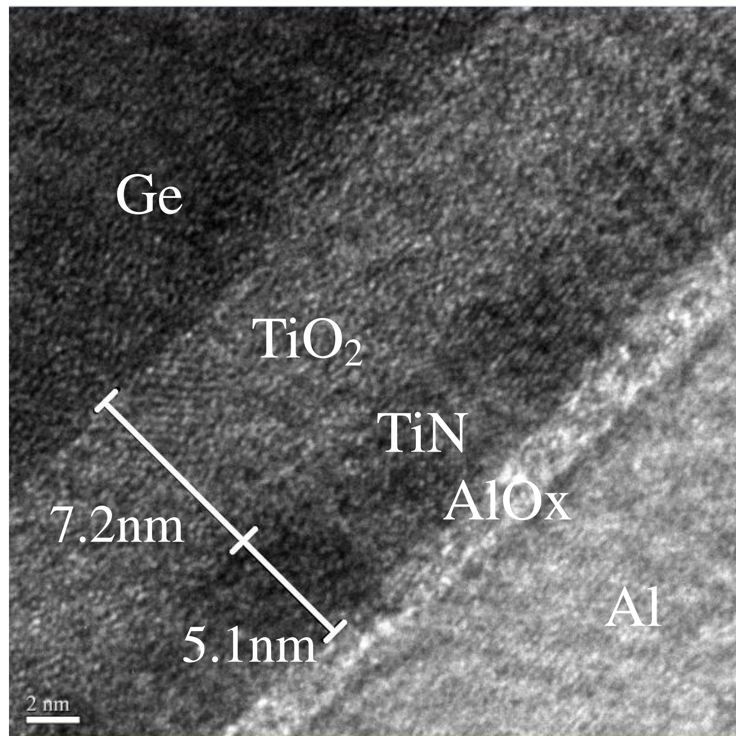



Fig. 3-12 Schottky barrier height of 1nm and 7nm-$TiO_2$-inserted junctions after annealing at 300 °C, 400 °C and 600 °C for 30 minutes. The Schottky barrier heights are all increased with increasing temperature for both samples.



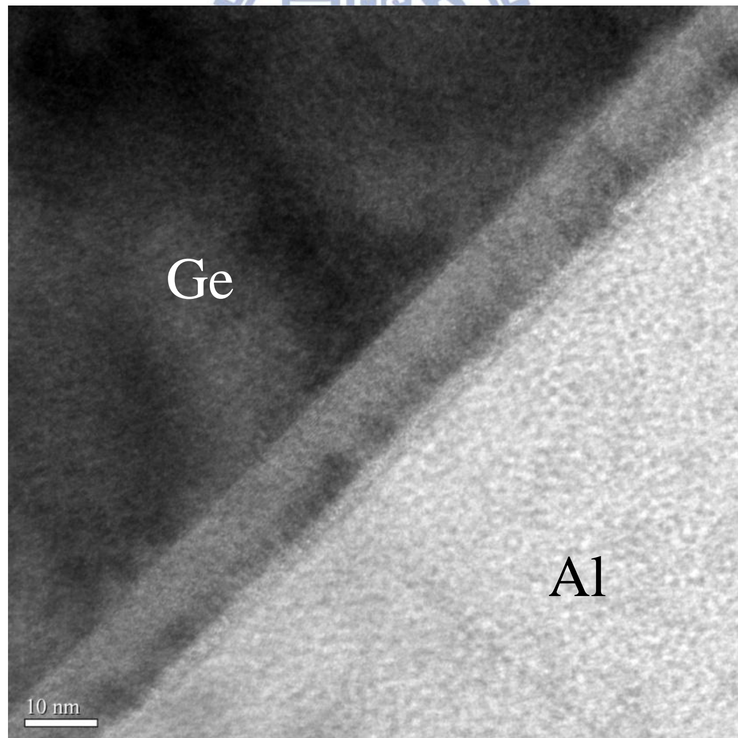




Fig. 3-13 TEM micrographs of $TiN/TiO_2/Ge$ junctions after 600 ℃ for 30 minutes annealing. No interlayer formed at the interface.

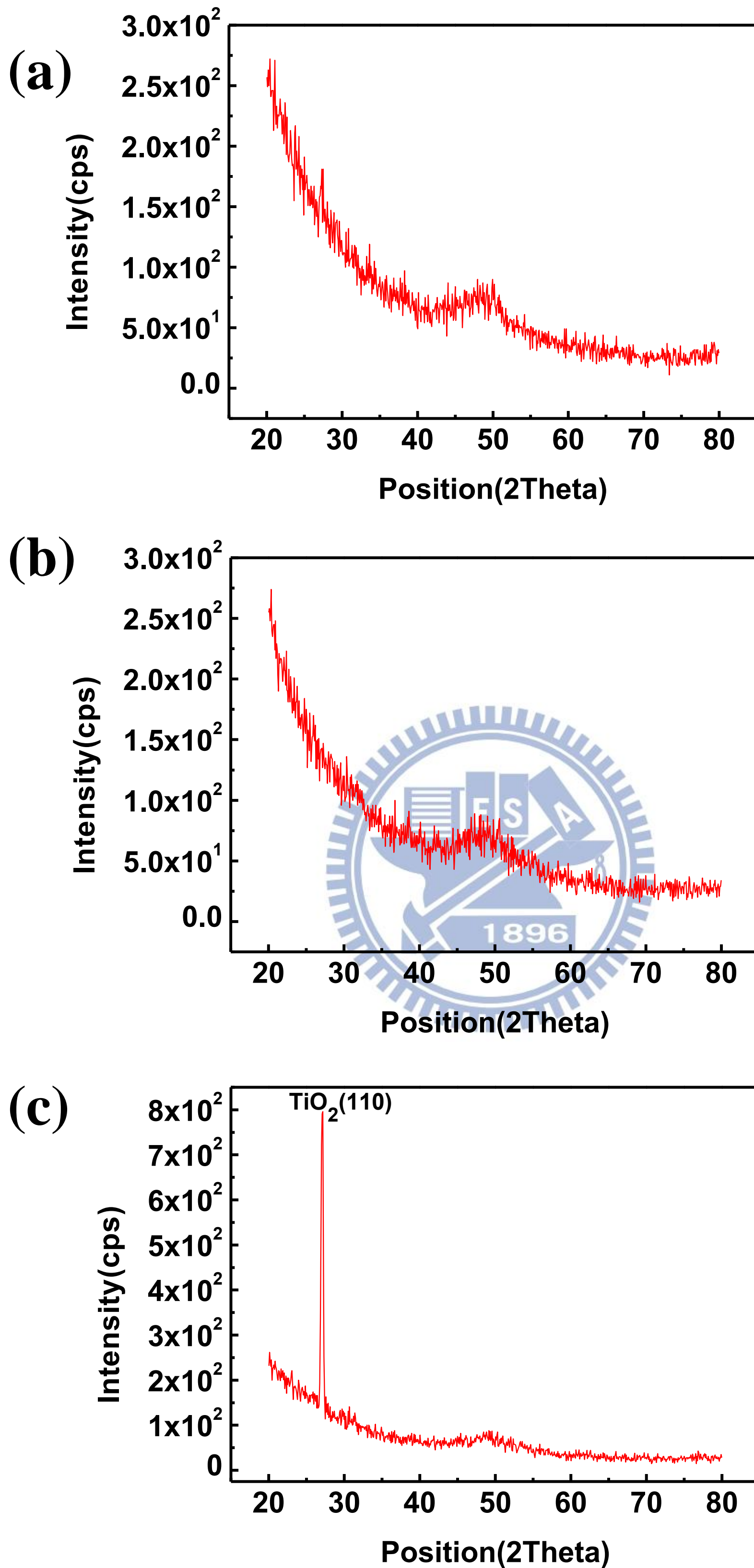



Fig. 3-14 XRD results of $TiO_2$ layer after (a) 300 ℃ (b) 400 ℃ (c) 600 ℃ annealing. The (110) crystalline phase of $TiO_2$ is detected for 600 ℃ annealed sample.

# Chapter 4
# Germaium MSB Junctions

## 4-1 Introduction of Germanium MSB Junctions

Recently, modified Schottky barrier (MSB) junctions have been proposed to reduce the contact resistance by increasing doping concentration at the metal/semiconductor interface. In the MSB junctions, the dopants are implanted into metal-semiconductor compound followed by a low temperature annealing to make them diffuse out from the compound to semiconductor and then segregate at the interface. In Ge, doping concentration is difficult to be raised because the dopants diffusion is fast which caused by large number of defects formed during ion implantation. With MSB method, dopants are implanted into metal-germanide instead of Ge so that the number of defects formed in substrate during ion implantation can be reduced, which might mitigate dopant diffusion effect during dopant activation to form a thin and high doping profile at germanide/Ge interface.

## 4-2 Activation of NiGe MSB Junctions

Fig.4-1 shows the I-V characteristics of NiGe MSB junctions annealed at 400 ℃, 450 ℃ and 500 ℃ for 30 minutes, junction current without MSB process is also shown in the picture. It is observed that the currents are all enhanced by increasing annealing temperature, which indicates that more effective doping activation at higher annealing temperature. The difference of forward and reverse current of sample without implantation is about two orders at 0.5 V, whereas it is nearly symmetrical of the forward and reverse current of the 500 ℃ activated MSB samples. This result

means that the effective Schottky barrier height is very low due to the high doping concentration at the germanide/Ge interface.

Why we use effective Schottky barrier height here instead of original Schottky barrier height is because that if the doping concentration at the germanide/Ge interface is very high, the thickness of the Schottky barrier will be very thin so that carriers tunnel the barrier easily. The large tunneling current is called the field emission current. In this case, the Schottky barrier height extracted from the thermionic emission model will be lower than the exact Schottky barrier height. Therefore, it is called the effectively barrier height.

Fig.4-2 shows the I-V characteristics of the NiGe MSB junctions annealed at 500 ℃ for10, 30, 50, and 70 minutes. It can be found that the currents increases as the annealing time increases from 10 minutes to 50 minutes but the increments are smaller than that by increasing annealing temperature. When the annealing time increases to 70 minutes, the current is almost the same as the current of the 50 minutes annealed junction, which means the doping concentration is not enhanced furthermore for such a long annealing time.

According to the experimental results of different annealing recipes, if we want to further enhance the performance of MSB junctions, we have to increase the annealing temperature for higher dopant activation, but the poor thermal stability of NiGe limits the annealing temperature above 500 ℃. Besides, although the number of defects in Ge can be reduced by MSB process, the resistance of germanide will be increased which results from ion implantation damage in germanide. The thermal stability and increased resistance problems of NiGe MSB junction will be discussed in the next section.

## 4-3 Thermal Stability of NiGe after MSB Formation

Fig.4-3 shows the sheet resistance values of the NiGe films formed at different temperatures form 400 ℃ to 600 ℃, it is observed that the sheet resistance value increases to about 40 Ω/□ at 550 ℃ and largely increases at 600 ℃. Figs.4-4 (a)-(d) shows the surface morphology of the NiGe films with different annealing temperatures inspected by SEM, according to these pictures, when the annealing temperature is higher than 500 ℃, the NiGe film breaks into many small islands and becomes discontinuous which results in increasing of the sheet resistance of the NiGe film. The severe agglomeration phenomenon limits the activation temperature of NiGe MSB junctions.

Fig 4-5 shows the sheet resistance of NiGe films before and after MSB formation. Because of the damages caused by ion implantation, the sheet resistance value increases to 34 Ω/□, which is about two times than the sample without ion implantation (about 15 Ω/□). After annealing at 450 ℃ or 500 ℃ for 30 minutes, the sheet resistance value decreases to about 25 Ω/□ because of the recrystallization of the NiGe film, but this value is still larger than that before ion implantation. The sheet resistance values of samples annealed at 400 ℃ for 30 minutes and at 500 ℃ for 10 minutes are still high. These result indicates that the thermal budget is not sufficient for the recrystallization of the NiGe films. It is noticed that the sheet resistance value increases when the annealing time is longer than 30 minutes at 500 ℃ for both samples with/without implantation, which might due to the poor thermal stability of the NiGe films. This poor thermal stability will limit the performance of the NiGe MSB junctions. To solve this problem, the thermal stability of the NiGe films has to be improved.

## 4-4 Thermal Stability Improvement by Inserting a Si Film

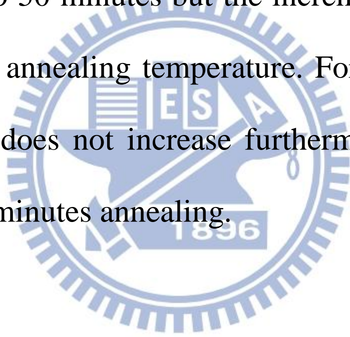
It has been reported that incorporating some materials into NiGe films will improve thermal stability, such like Pt[29], Pd[31,34], Ti[32]. In this thesis, Si is used because of the better thermal stability and lower sheet resistance of NiSi film. Besides, in nowadays CMOS fabrication, SiGe is used for the source/drain regions of PMOSFET and Ni is used as reaction metal for salicide process. It has been reported that the thermal stability and the sheet resistance of the chemical compound of Ni and SiGe are better than those of NiGe[48,49]. So we can infer that by incorporating Si into NiGe films, the thermal stability and sheet resistance could be improved.

Fig.4-6 shows the sheet resistance values of the NiGe films with and without silicon incorporated. Compared to samples without silicon incorporation, the sheet resistance values of samples with Si incorporation are lower at all temperatures, and it still has the value about 18 Ω/□ after 550 ℃ annealing. A sharp increase atfter 600 ℃ annealing is observed. The surface morphology of the NiGe with silicon films with different annealing temperatures inspected by SEM are shown in Fig.4-7 (a)-(d). It can be observed that the surface agglomeration phenomenon is alleviated for the 550 ℃ annealed sample, and the agglomerated islands are smaller than those of the sample without silicon incorporation after 600 ℃ annealing. From the results above, we can infer that the insertion of a Si layer between Ni and Ge will delay the reaction between Ni and Ge so that the agglomeration phenomenon can be extended to 550 ℃. It should be noted that the thermal stability of the Si-insertion sample is still poorer than that of the pure NiSi sample. It is postulated that Ge atoms diffuse into the Si layer quickly so that Ni encounters Ge before the consumption of the inserted Si layer.

Fig.4-8 shows the sheet resistance values of the NiGe with Si-insertion after 550 ℃ MSB annealing. It is observed that the sheet resistance values are all lower

than those of samples without Si-insertion with 500 ℃ annealing. This result confirms that the thermal stability is improved by incorporating silicon into NiGe films. By incorporating Si into NiGe films, we can extend the MSB junction activation temperature to 550 ℃.

Fig.4-9 shows the I-V characteristics of the MSB junctions annealed at different temperatures for 30 minutes. For the 550 ℃ annealed sample, the current is higher than that of the 500 ℃ annealed sample which indicates more effective dopant activation at 550 ℃ annealing. Fig.4-10 shows the I-V characteristics of the NiGe MSB junctions with Si-insertion and annealed at 550 ℃ for different annealing times. Similar to the 500 ℃ annealed samples, the currents increases as the annealing time increases from 10 minutes to 50 minutes but the increments are smaller compared to the increment by increasing annealing temperature. For the sample with 70 minutes annealing time, the current does not increase furthermore which means the doping activation saturates after 50 minutes annealing.



## 4-5 Dopant Diffusion and Activation of MSB Junctions

Fig.4-11 compares the SRP profiles of MSB junctions and conventional ion implanted junction. With the same annealing temperature at 550 ℃, the MSB junctions have much higher doping concentrations and much shallower junction depths than the conventional junction (~0.8 μm). The implantation induced damages are mainly in germanide instead of in Ge for the MSB process. Without the defects like vacancies or interstitials caused by implantation in Ge, the dopant diffusion effect which comes from the interaction of dopants and defects would be alleviated and the doping activation could be more effective.

Fig.4-12 shows the I-V characteristics of the MSB junctions and the

conventional junction. Even with 600 ℃ activation, the current density of the conventional junction is lower than that of the 550 ℃ activated MSB junction because the carrier concentrations of the MSB junctions are higher than that of the conventional junction even though the activation temperature is lower. With higher doping activation temperature for the conventional junction, the carrier concentration would saturate due to the solid state solubility limit. Furthermore, the deep junction depth is not suitable for nowadays CMOS fabrication demands.

## 4-6 Summaries of MSB Junctions

To sum up, modified schottky barrier junction has been made for $n^+$-p Ge junctions. Because dopants are implanted into germanide instead of Ge, the defects in Ge are negligible and the dopants diffusion effect caused by the interaction between defects and dopants could be mitigated.

The poor thermal stability of NiGe limits the activation temperature of MSB junctions, to solve this problem, Si is incorporated into the NiGe films and the thermal stability is improved to 550 ℃. With higher activation temperature, the carrier concentration and the conduction current of the MSB junctions are further enhanced.

Compared to the conventional junction with direct implantation into Ge, the junction depth is much shallower and the carrier concentration is much higher for the MSB junction. It should be noted that the Ge substrate contributes significant parasitic resistance as the contact resistance of the NiGe/$n^+$ Ge contact is low, the contact resistance of the MSB junction is expected to be much lower than that of the conventional junction.

High carrier concentration and shallow junction depth suggest the MSB process is attractive for the short channel Ge MOSFETs.

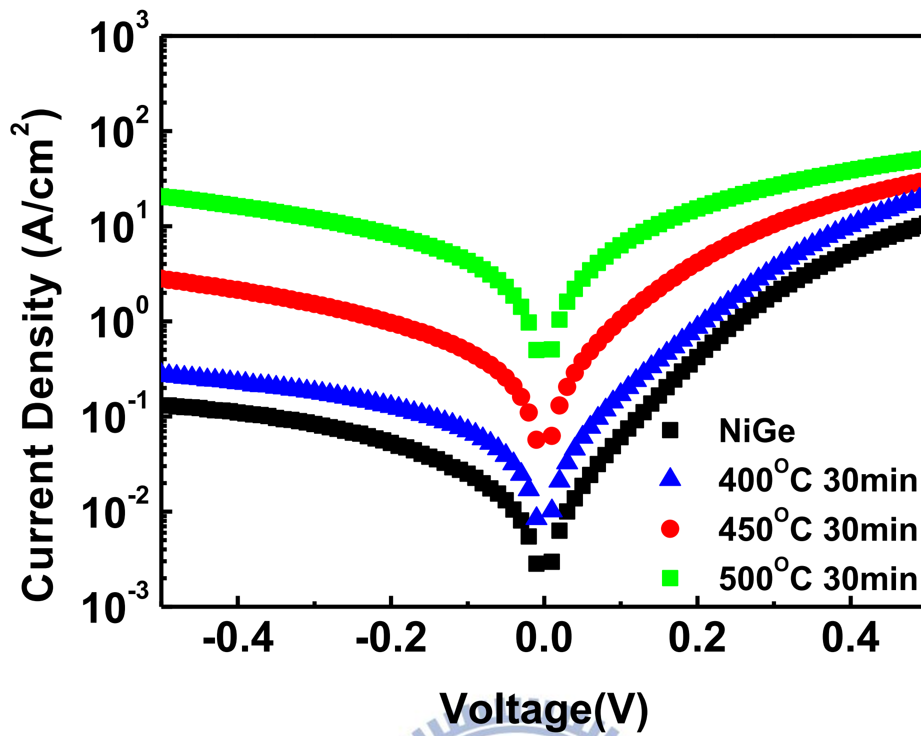



Fig. 4-1 I-V characteristics of NiGe MSB junctions activated at 400 ℃, 450 ℃ and 500 ℃ for 30 minutes, current of NiGe without implantation junction is also shown. Currents are all enhanced with increasing annealing temperature, which indicates that more effective doping activation with higher annealing temperature.

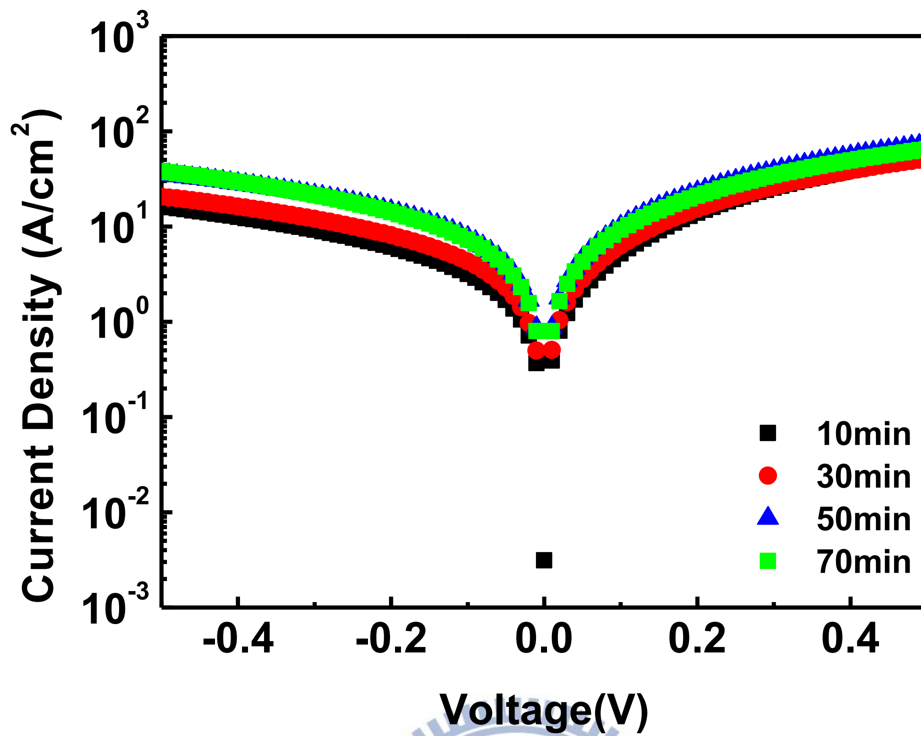



Fig. 4-2 I-V characteristics of NiGe MSB junctions activated at 500 ℃ for 10, 30, 50, and 70 minutes. Currents are increased for annealing time from 10 minutes to 50 minutes except for 70 minutes which means the doping concentration is saturated.

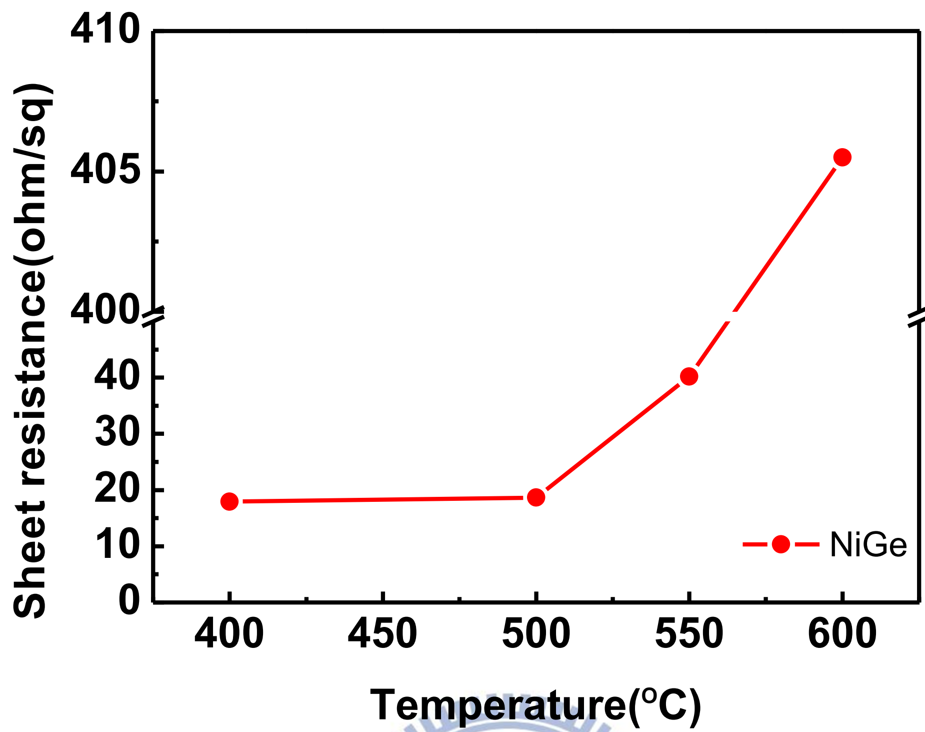



Fig. 4-3 Sheet resistance values of NiGe filmes formed at 400 ℃, 500 ℃, 550 ℃, and 600 ℃ for 30 seconds. The sheet resistance value is sharply increased after 500 ℃ annealing.

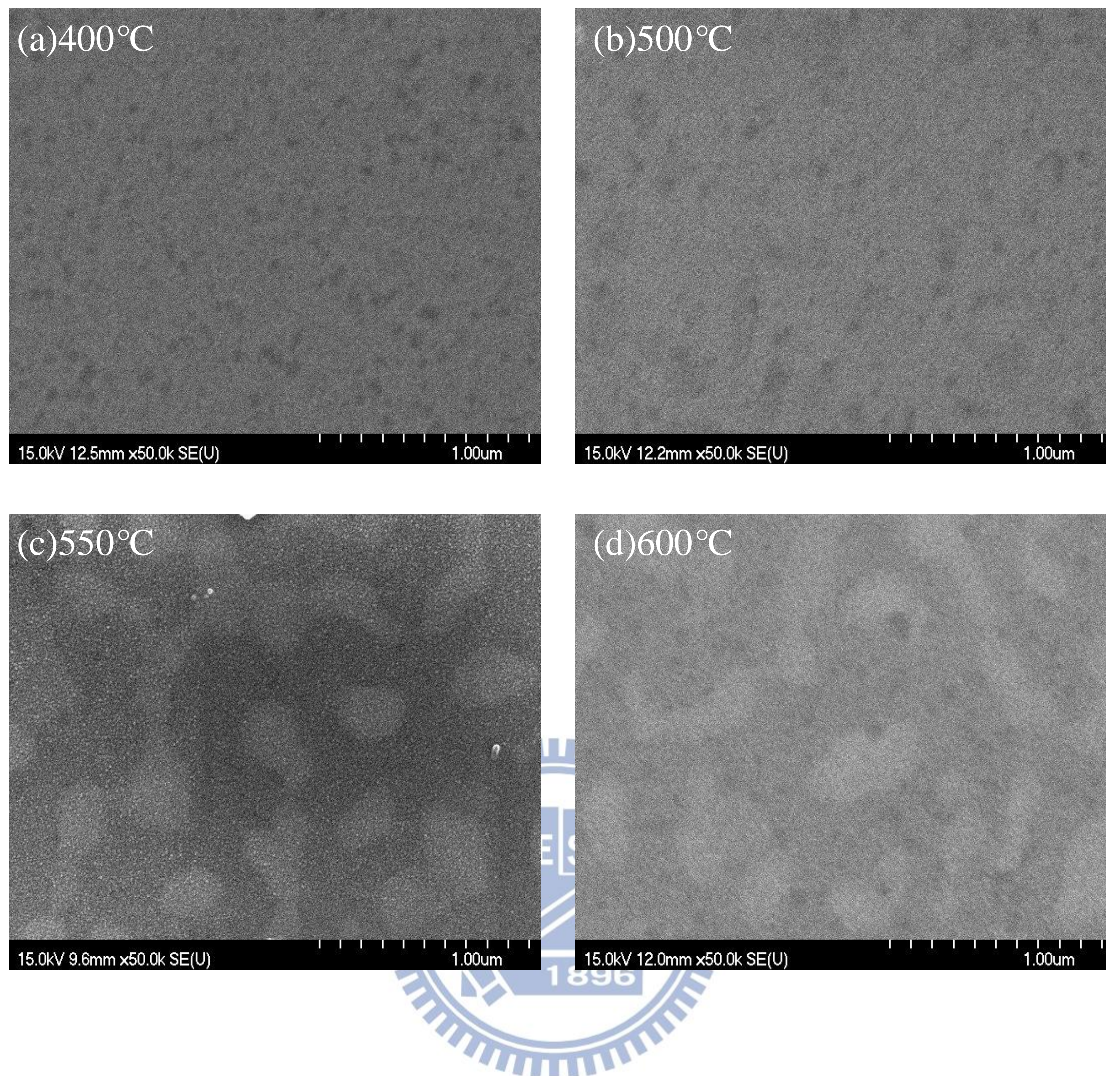



Fig. 4-4 SEM images of NiGe filmes formed at (a) 400 ℃, (b) 500 ℃, (c) 550 ℃, and (d) 600 ℃ for 10 seconds. Severe agglomeration phenomenon is observed after 550 ℃ annealing.

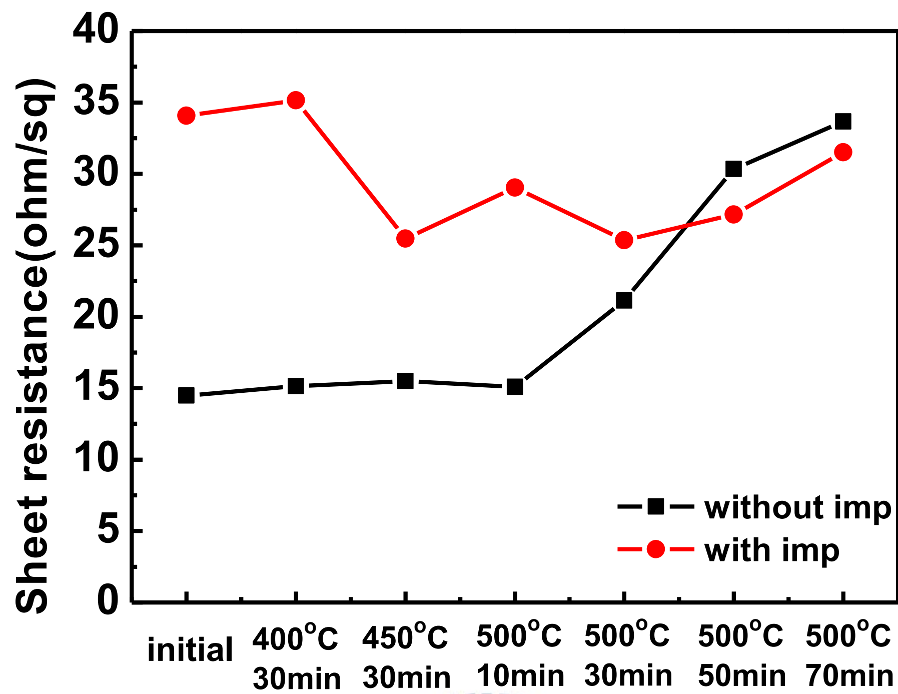



Fig. 4-5 Sheet resistance values of NiGe films with or without implantation after different post annealing temperature and time. After activation, the sheet resistance value is first decreased due to the recrystallization of the NiGe films, but it would increase when the annealing time is above 30 minutes.

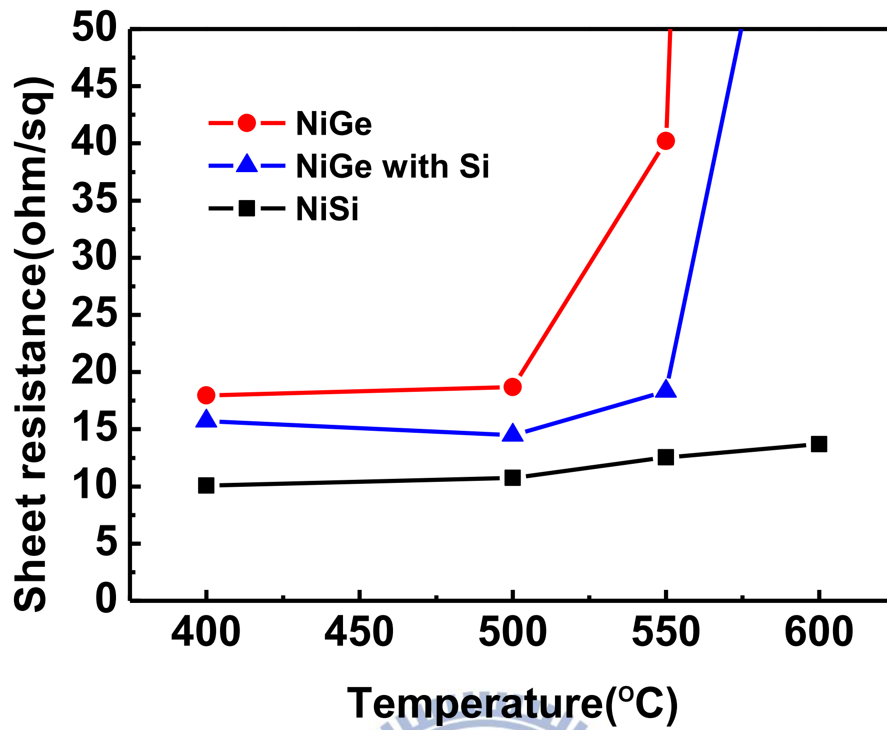



Fig. 4-6 Sheet resistance values of NiGe, NiSi, and NiGe with Si insertion films at different formation temperature for 30 seconds. By incorporating Si into the NiGe films, the thermal stability and sheet resistance are improved.

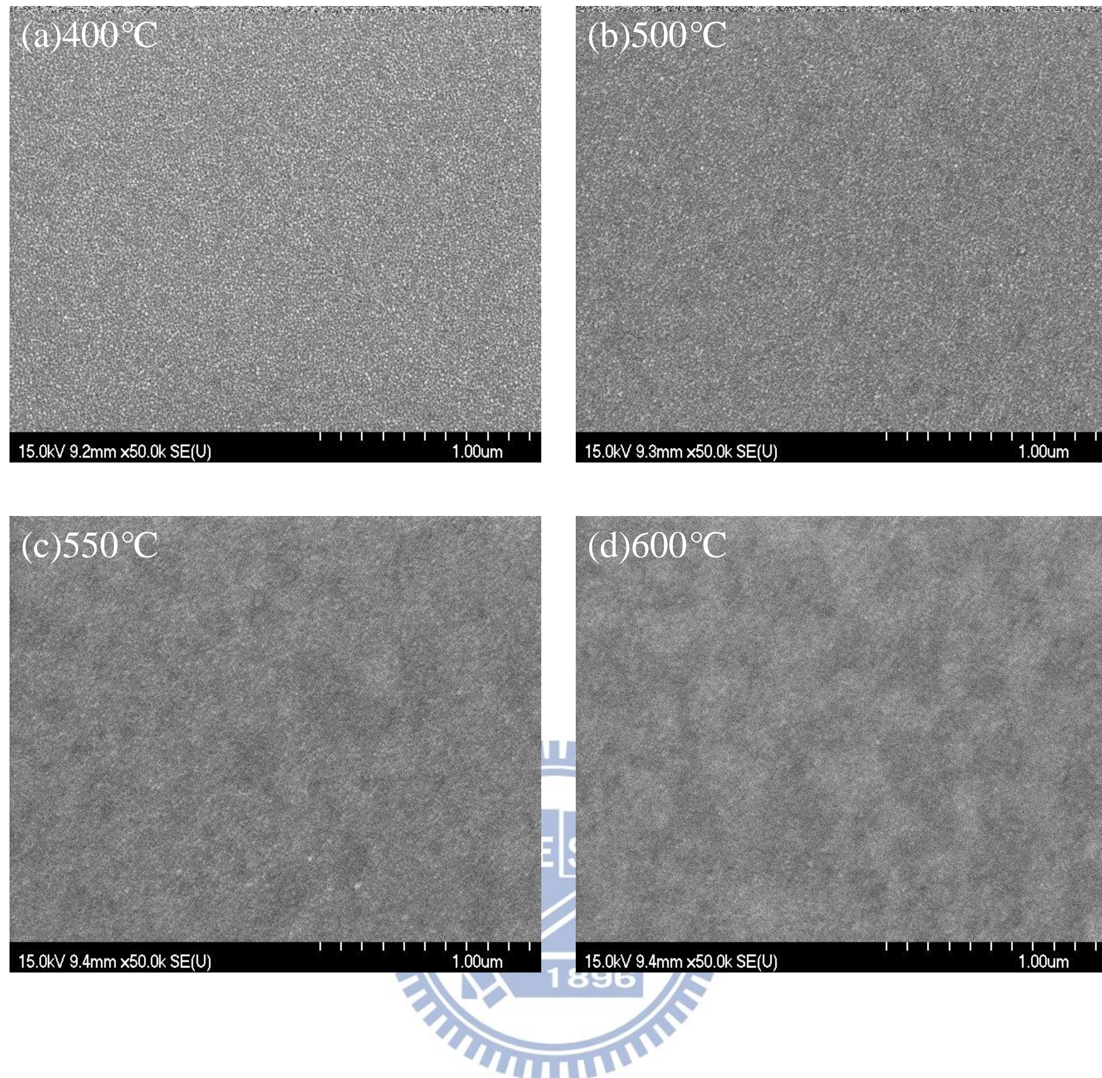



Fig. 4-7 SEM images of NiGe with Si-insertion filmes formed at (a) 400 ℃, (b) 500 ℃, (c) 550 ℃, and (d) 600 ℃ for 10 seconds. The agglomeration phenomenon is alleviated.

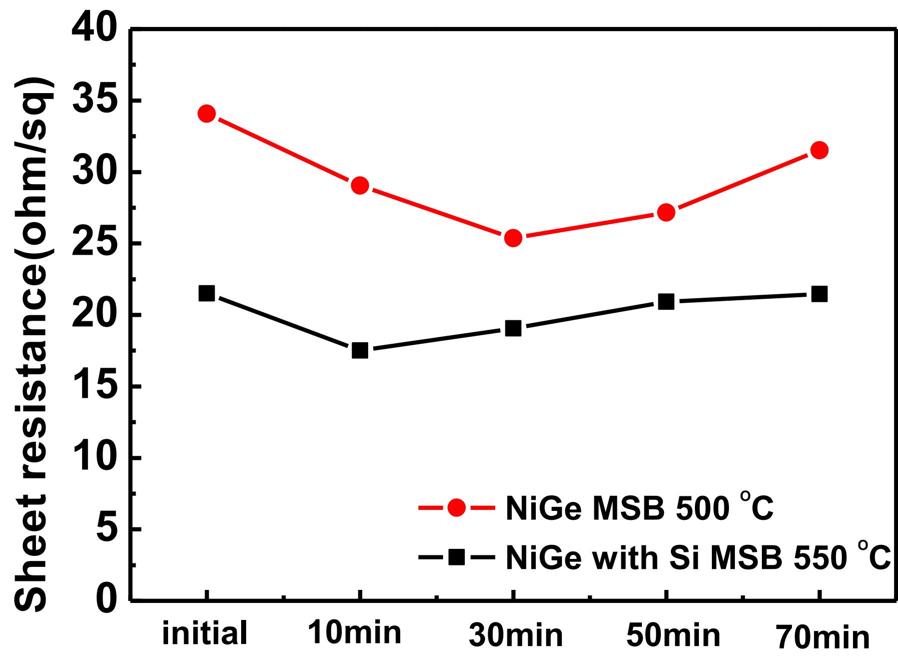



Fig. 4-8 Sheet resistance values of NiGe and NiGe with Si films after MSB formation with activation temperature at 500 ℃ and 550 ℃ for different times. The sheet resistance values of NiGe with Si-insertion films are all smaller than NiGe films even for the annealing temperature is higher.

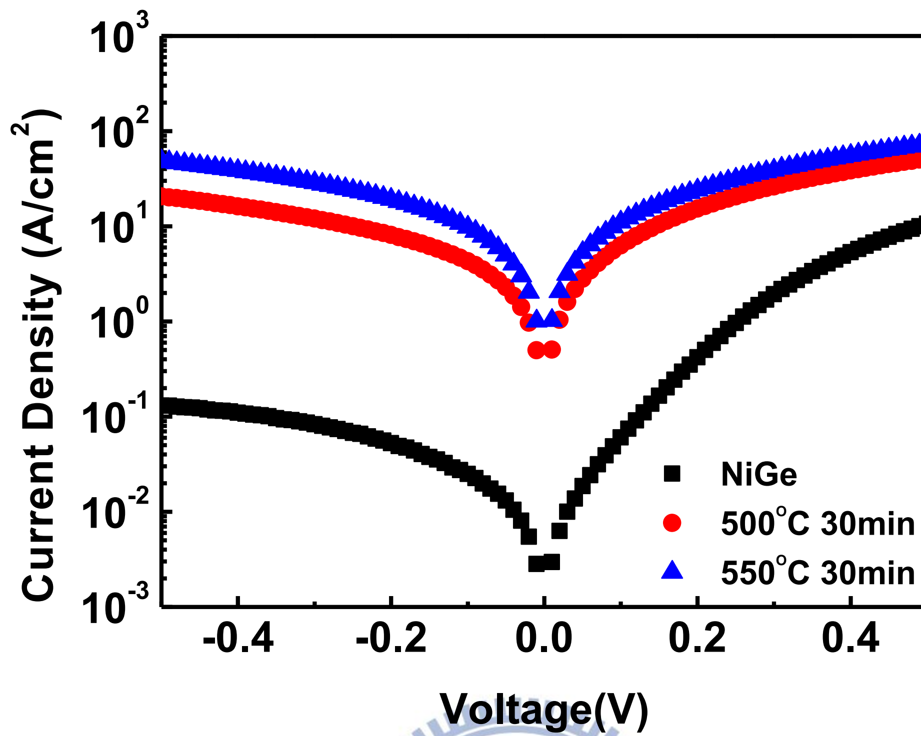



Fig. 4-9 I-V characteristics of the MSB junctions after different activation temperature 500 ℃ and 550 ℃ for 30 minutes. With the activation temperature is raised to 550 ℃, the junction current is further enhanced.

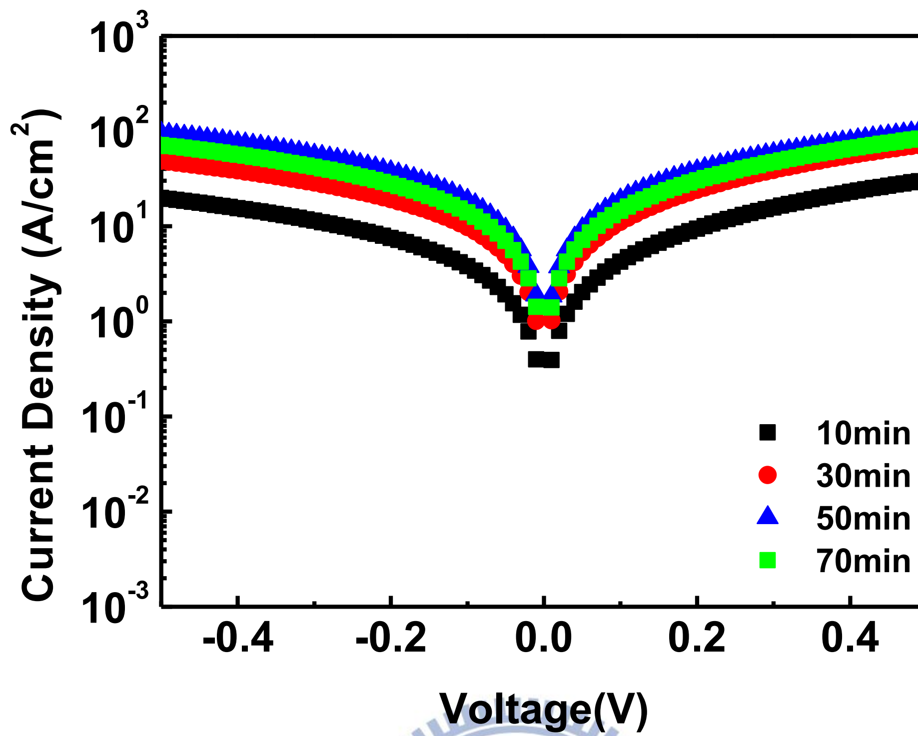



Fig. 4-10 I-V characteristics of NiGe with Si-insertion MSB junctions activated at 550 ℃ for different times. Currents are increased for annealing time from 10 minutes to 50 minutes except for 70 minutes which means the doping concentration is saturated.

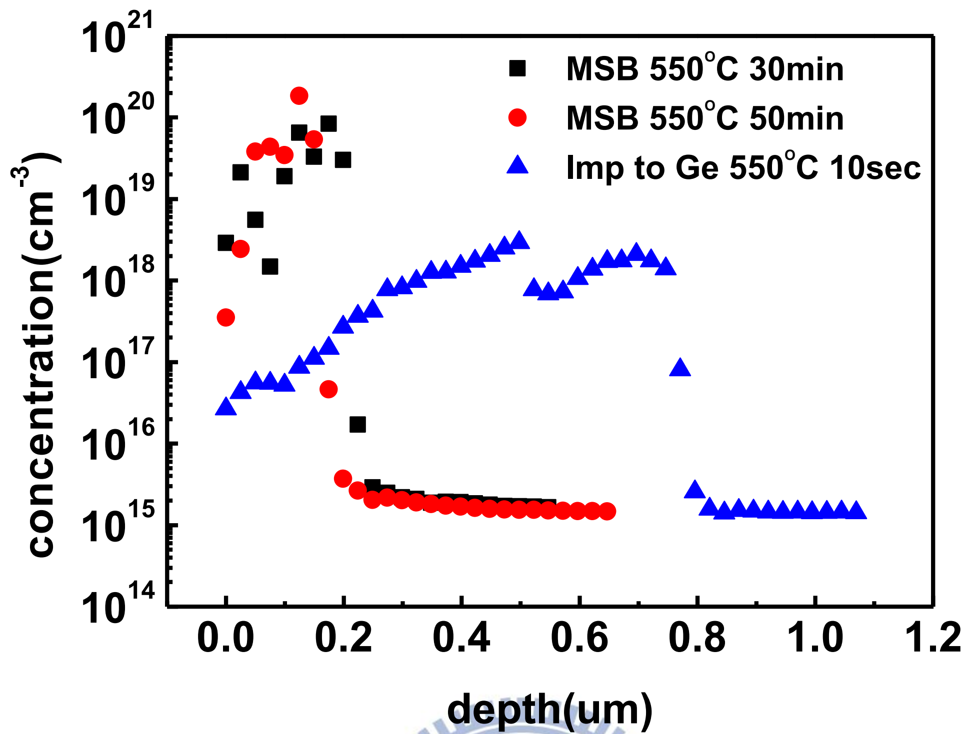



Fig. 4-11 SRP profiles for MSB junctions activated at 550 ℃ for 30 and 50 minutes, direct implantation to Ge sample activated at 550 ℃ for 10 seconds is also shown. The junction depths are much shallower and the doping concentrations junctions are much higher compared to conventional direct implantation junctions.

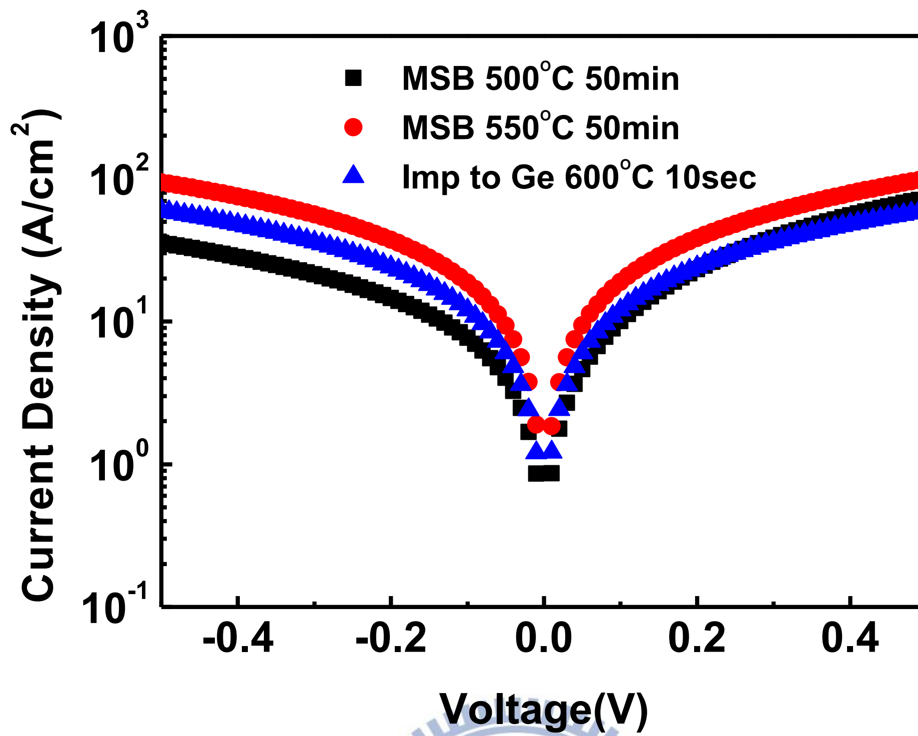



Fig. 4-12 I-V characteristics of the MSB junctions and the conventional direct implantation to Ge junction. The currents are comparable even for the lower annealing temperature of MSB junctions.

# Chapter 5
# Summary and Future Works

## 5-1 Summary

The effect and mechanism of Schottky barrier height modulation of the metal/n-type Ge Schottky junction by inserting dielectric layer are examined. Both $Al_2O_3$ and $TiO_2$ insertion layer result very low Schottky barrier height. Although the Schottky barrier height of the $Al_2O_3$–inserted junction is only slightly higher than that of the $TiO_2$–inserted junction, the conduction current is apparent lower because of the larger conduction band offset of $Al_2O_3$ to Ge. Due to the small conduction band offset of $TiO_2$ to Ge, it can not only decrease the Schottky barrier height but also achieve low tunneling resistance. The 7-nm-thick $TiO_2$–inserted junction has lower Schottky barrier height than the 1-nm-thick junction. However, the Schottky barrier height reduction is not thermally stable. After annealing, the barrier height increases with the increase of annealing temperature from 300 ℃ to 600 ℃. The mechanisms of these phenomena including MIGS effect, fixed charges, and interface dipole, are investigated.

First we examine the mechanism of MIGS. Different metals are used to determine the Fermi-level pinning factor. The pinning factors are about 0.14 and 0.12 for the 1-nm-thick and 7-nm-thick $TiO_2$-inserted junctions, respectively, which are larger than that of the simple metal/Ge junction (about 0.05) but are still much smaller than 1. This result indicates that the Fermi level pinning effect is only slightly mitigated by the insertion layer. Since the pinning factor does not increases with the increase of the insertion layer thickness, the modulation of Schottky barrier height is

not due to the suppression of the MIGS effect but because that the pinning position is changed more for thicker $TiO_2$ layer. Then we examine if the fixed charges in the insertion layer would produce additional potential drop to modulation the Schottky barrier height. The amount of the fixed charges in the inserted dielectric is extracted by a MIS capacitor. The value is too low for such a thin dielectric layer to produce the apparent Schottky barrier height modulation. It is thus recommended that the mechanism of the Schottky barrier modulation by inserting dielectric layer mainly comes from the interface dipoles.

The thermal stability of the Schottky barrier height is examined by microstructural analysis. No interfacial layer formation can be observed form the high resolution TEM inspection at the TiN/$TiO_2$ and the $TiO_2$/Ge interfaces. According to XRD spectra, the $TiO_2$ layer is gradual crystallized with increasing annealing temperature. It is known that crystallization of dielectric layer would increase the dielectric constant. Higher dielectric constant and thinner dielectric thickness result in higher capacitance $C_{ox}$, and the voltage drop of $\Delta V = Q_{OC} / C_{OX}$ would be smaller so that the Schottky barrier height is modulated less significantly.

Modified Schottky barrier method is proposed to reduce the metal/n-type Ge contact resistance. Because dopants are implanted into germanide instead of Ge, the defects in Ge are negligible and the dopants diffusion caused by the interaction between defects and dopants could be mitigated. The MSB junction currents are all enhanced by increasing annealing temperature and annealing time, but it saturates after annealing at 500 ℃ for 50 minutes. To further improve the MSB junctions current, the annealing temperature must be increased, but the poor thermal stability of NiGe after 500 ℃ annealing limits the activation temperature of the MSB junctions. To solve this problem, Si is incorporated into the NiGe films and the thermal stability is improved to 550 ℃. From the SEM inspection, the agglomeration phenomenon is

more alleviated for the Si-incorporated film than the pure NiGe film, and the sheet resistance values of NiGe with Si-incorporation keeps low after MSB 550 ℃ annealing process. With higher activation temperature, the carrier concentration and the conduction current of the MSB junctions are further enhanced.

Compared to the conventional junction with direct implantation into Ge, the junction depth is much shallower and the carrier concentration is much higher for the MSB junction. Even with 600 ℃ activation, the current density of the conventional junction is lower than that of the 550 ℃ activated MSB junction. These result indicates that the carrier concentrations of the MSB junctions are higher than that of the conventional junction even though the activation temperature is lower. High carrier concentration and shallower junction depth suggest the MSB process is attractive for the short channel Ge MOSFETs.

Fig. 5-1 compares the I-V characteristic of 550 ℃ annealed MSB junction and 7-nm-thick $TiO_2$ inserted junction before/after annealing. Although the current of 7-nm-thick $TiO_2$ inserted junction is larger than MSB junction, the current would decrease after annealing and be lower than the MSB junction.

To sum up, dielectric insertion junction can achieve very low Schottky barrier height but the poor stability limits its application, and it can’t be integrated with self-align process. MSB junction has higher germanide resistance but the junction is much shallower and dopant concentration is much higher than conventional direct implantation junction, and it can be integrated with self-align process. So the MSB process is more appropriate for CMOS fabrication.

## 5-2 Future Works

The thickness effect of $TiO_2$–inserted junction could be further studied by

using more different thicknesses, and the reason why $TiO_2$ dielectric layer could induce larger surface dipole than $Al_2O_3$ should also be studied. Besides, the thermal stability of the dielectric insertion junctions could be examined by using smaller thermal budget to observe what annealing recipe could be endured, which is important for using this process to fabricate junctions of MOSFET. To verify the mechanism of Schottky barrier height modulation by dielectric insertion is changing the pinning position; p-type Ge substrate could be used to observe if the Schottky barrier height is high.

The mechanism of thermal stability improvement by inserting a Si layer to NiGe films should be studied, if the Si thickness and the annealing recipes could be optimized, the thermal stability might be further enhanced. How to further improve the thermal stability of germanide by other methods could also be studied.

To extract the contact resistance and observe the $n^+/p$ junction characteristic for MSB process, p-type Ge substrate should be used.

To fabricate short channel Ge MOSFET by using MSB S/D junctions, the activation recipes and the implantation dosage should be optimized, and the thermal stability of the high-k dielectric and metal gate should also be considered. To verify the improvement of MSB process, short channel Ge NMOSFET with MSB S/D junctions should be fabricated.

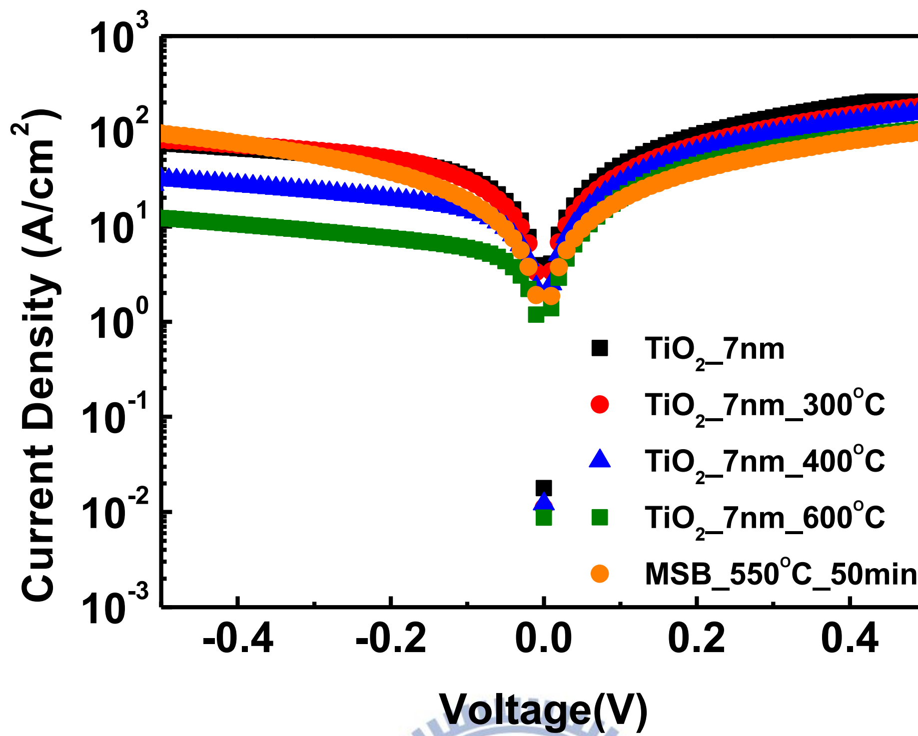



Fig. 5-1 I-V characteristics of the 550 ℃ annealed MSB junction and the 7-nm-thick $TiO_2$ inserted junction before/after annealing. Although the current of 7-nm-thick $TiO_2$ inserted junction is larger than MSB junction, the current would decrease after annealing and be lower than the MSB junction.

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碩士論文題目：

降低金屬與 N 型鍺接觸電阻之研究

A Study on the Contact Resistance Reduction in Metal/n-type Germanium Contacts