國 立 交 通 大 學

電子工程學系　　電子研究所碩士班

碩 士 論 文

三閘極金氧半場效電晶體利用基極偏壓調變臨界電壓之分析與模型建立

Investigation and Modeling of Threshold-Voltage Modulation through Substrate Bias for Tri-gate MOSFETs

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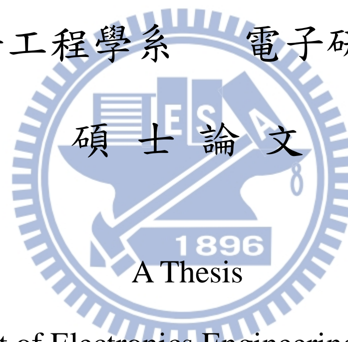

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摘 要

本論文探討三閘極金氧半場效電晶體藉由基極偏壓調變臨界電壓的可行性。我們利用三維原子等級模擬探討隨機參雜濃度變動(Random Dopant Fluctuation)對於 BULK 三閘極元件中 Punch-Through-Stopper (PTS)區域的影響。我們的研究發現藉由高濃度摻雜的 PTS 區域雖能有效的幫助基極偏壓調變元件的臨界電壓，但同時也造成額外 Bulk 三閘極電晶體的元件變異。因此，在比較 BULK 以及 SOI 三閘極元件的變異度時，上述效應的影響應該要納入考量。

由於 bulk 三閘極元件中 PTS 區域會引起額外的元件變異，因此利用基極電壓來調變 SOI 三閘極元件結構的臨界電壓似乎是個較佳的選項。為了有利於 SOI 三閘極元件多重臨界電壓的設計，我們準確地推導了具有高度深埋氧化層(BOX)厚度微縮性的次臨界解析模型。利用此模型，我們可以有效率且廣泛地探討 SOI 三閘極元件參數對於多重臨界電壓調變的影響。基於相同次臨界斜率(Subthreshold Slope)的比較基準之下，我們的研究指出低高寬比及薄深埋氧化層(BOX)的三閘極 SOI 元件結構設計可較有效率地利用基極偏壓來調變臨界電壓。

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Abstract

This thesis investigates the feasibility of threshold voltage (V_{th}) modulation through substrate bias for tri-gate MOSFETs. Through 3-D atomistic simulation, the random dopant fluctuations in the Punch-Through-Stopper (PTS) region of Bulk tri-gate devices are examined. Our study indicates that to achieve an efficient threshold-voltage modulation through substrate bias, the high-doping PTS region may introduce excess variation in Bulk tri-gate devices. This effect has to be considered when one-to-one comparisons between Bulk tri-gate and SOI tri-gate regarding device variability are made.

Because of the PTS-induced variability in Bulk tri-gate, SOI tri-gate with substrate bias seems to be a better device structure to achieve multiple V_{th}. In order to facilitate multi-V_{th} device design in tri-gate SOI MOSFETs, we have derived an analytical subthreshold model with an accurate BOX-thickness scalability. Using this model, we can efficiently investigate multi-V_{th} device design in tri-gate SOI MOSFETs with wide range of design space. Under constant subthreshold swing criterion, our study indicates that tri-gate SOI device with low aspect ratio (AR) and thin BOX is a promising structure to enable efficient V_{th} modulation by substrate bias.

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隨著這本碩士論文的完成，我短暫而充實的兩年碩士班生活也將畫下句點。

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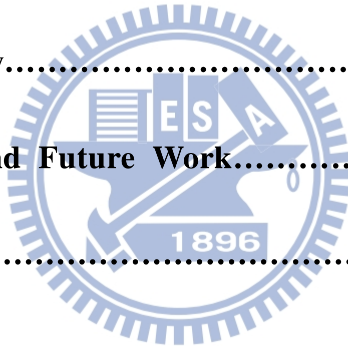

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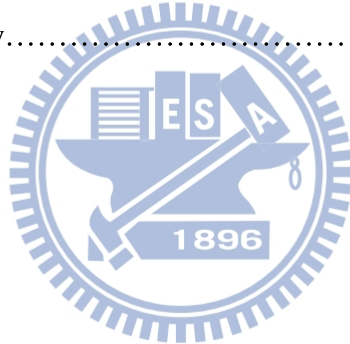

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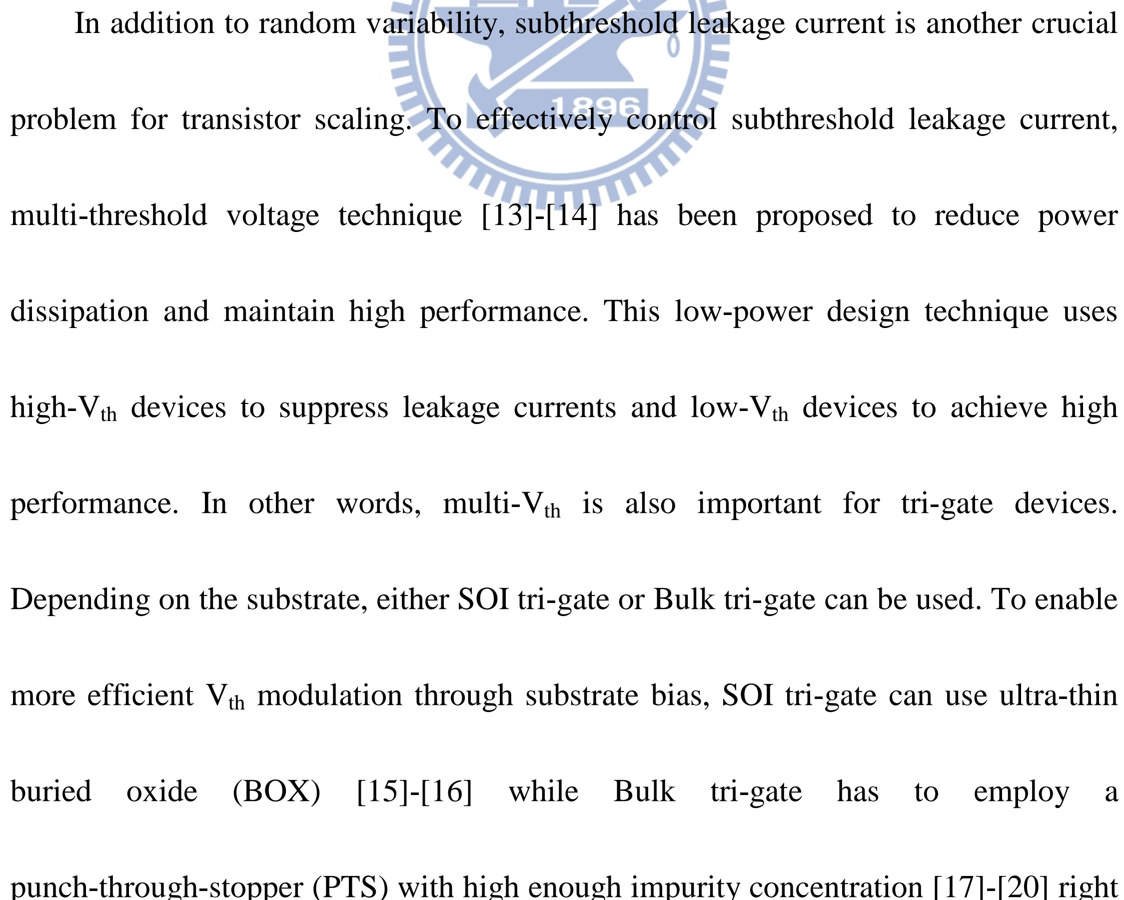
Chapter 1
Introduction

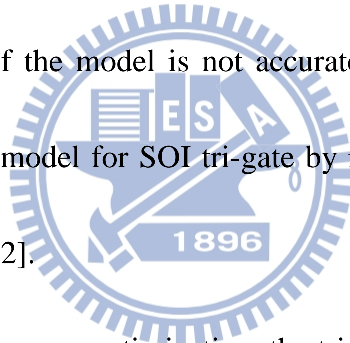
Because multiple gates can provide superior electrostatic control, tri-gate MOSFETs [1]-[4] have better immunity to short-channel effects (SCE), and can be used to extend the Moore's Law in transistor scaling. In addition, random variation such as random dopant fluctuation [5]-[9], line edge roughness [10]-[11] has become a curial problem for nanoscale CMOS. Undoped or lightly-doped tri-gate MOSFETs can mitigate the channel random-dopant-fluctuation (RDF) problem for planer bulk MOSFETs [12].



In addition to random variability, subthreshold leakage current is another crucial problem for transistor scaling. To effectively control subthreshold leakage current, multi-threshold voltage technique [13]-[14] has been proposed to reduce power dissipation and maintain high performance. This low-power design technique uses high-V_{th} devices to suppress leakage currents and low-V_{th} devices to achieve high performance. In other words, multi-V_{th} is also important for tri-gate devices. Depending on the substrate, either SOI tri-gate or Bulk tri-gate can be used. To enable more efficient V_{th} modulation through substrate bias, SOI tri-gate can use ultra-thin buried oxide (BOX) [15]-[16] while Bulk tri-gate has to employ a punch-through-stopper (PTS) with high enough impurity concentration [17]-[20] right

beneath the lightly-doped channel. In this work, we use 3-D atomistic simulation to investigate the body-effect induced variability in Bulk tri-gate MOSFETs [21].

Due to the PTS-induced variability in Bulk tri-gate, SOI tri-gate with thin BOX seems to be a better device structure to enable threshold-voltage modulation. In order to physically assess the electrostatic integrity and facilitate device design for SOI tri-gate, we have derived a subthreshold model for SOI tri-gate considering the fringing field induced by the drain and source electrodes through the BOX. Although reference [22] has provided a subthreshold model for multi-gate SOI MOSFETs, the BOX-thickness scalability of the model is not accurate. In this work, we provide a more accurate subthreshold model for SOI tri-gate by improving the BOX-thickness scalability of the model in [22].



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To enable power/performance optimization, the tri-gate SOI MOSFETs with thin BOX [15]-[16] has been recognized a promising device structure to achieve multiple threshold voltage (V_{th}). Whether different tri-gate device designs will impact the efficiency in V_{th} modulation is an important question. In this work, we investigate the multi-V_{th} device design of tri-gate SOI MOSFETs by using the derived analytical model. Based on the contour of equal subthreshold swing (SS), the impacts of device design on the threshold voltage modulation through substrate bias and channel doping are investigated.

This thesis is organized as follows. In chapter 2, we investigate the PTS-induced variability in Bulk tri-gate MOSFETs. In chapter 3, an analytical subthreshold model for SOI tri-gate devices with thin BOX is derived and verified with TCAD numerical simulation. In chapter 4, the impact of device design on multi-V_{th} modulation for SOI tri-gate is investigated by using the model derived in chapter 3. The conclusions are drawn in chapter 5.

Chapter 2
Body Effect Induced Variability in Bulk Tri-gate MOSFETs

2.1 Introduction

Undoped/lightly-doped tri-gate MOSFET has been recognized as an important device structure to mitigate the channel random-dopant-fluctuation (RDF) problem for planer bulk MOSFET. Depending on the substrate, either SOI tri-gate or Bulk tri-gate can be used. Comparing with the SOI tri-gate, bulk tri-gate possesses lower wafer cost and higher process compatibility. References [17]-[18] have reported a successful 20 nm-FinFET fabrication on bulk silicon wafer. Both [17] and [18] employed the deep well implant to isolate the body from the substrate. This extra implantation process intended to suppress the leakage current beneath the channel region and was called as punch-through-stopper (PTS) layer. Several simulation works [18]-[20] have been made to investigate the device design optimization considering the PTS doping profile. However, these works have not considered the device variation introduced by the PTS. In addition, whether there is any difference regarding random variability between Bulk tri-gate and SOI tri-gate has rarely been known and merits investigation.

Although tri-gate MOSFETs have an improved immunity to short-channel effects (SCE), body effect in such device structure is usually weaker than planer MOSFETs [15]. To enable more efficient threshold-voltage (V_{th}) modulation and power/performance optimization through substrate bias, SOI tri-gate can use ultra-thin BOX [15]-[16] while Bulk tri-gate may employ the PTS with high enough doping concentration [20] right beneath the lightly-doped channel (Fig. 2.1). In this chapter, using 3-D atomistic simulation [23], we investigate the body-effect induced variability in Bulk tri-gate MOSFETs [21].

2.2 Device Design and Simulation Methodology

Bulk tri-gate and SOI tri-gate structures investigated in this chapter are based on the device design used in [24]-[25]. Schematics of Bulk tri-gate and SOI tri-gate structures are shown in Fig. 2.1 and Fig. 2.2, respectively. Channel length (L_g=25nm), channel doping (N_{ch}=1x10^{17}cm^{-3}), gate oxide thickness (t_{ox}=1.3nm) and fin thickness (H_{fin}=W_{fin}=10nm) are designed identically for Bulk tri-gate and SOI tri-gate to ensure similar front gate controllability. As indicated in the Fig. 2.5, in order to achieve comparable body effect with SOI tri-gate, the PTS of Bulk tri-gate is designed with 1x10^{19} cm^{-3} in doping, 30 nm in depth (T_{PTS}), 10 nm in width, and 25 nm in length, while the BOX of SOI tri-gate is designed with 10 nm in depth (T_{box}), 20 nm in width and 65 nm in length (2*L_{SD}+L_g). As indicated in the Fig. 2.1(b), the PTS doping

profile does not extend to the substrate below source/drain because the abrupt p-n junction between source/drain and PTS will induce significant band-to-band tunneling current. Other pertinent device parameters are listed in Table 2.1.

Discrete impurity atoms are randomly distributed in the PTS of Bulk tri-gate and the substrate of SOI tri-gate, respectively, in our 3-D atomistic simulation [23]. It is noted that the total number of impurity atoms in the PTS/substrate region follows the Poisson Random Distribution (Fig. 2.3) and the impurity atoms space distribution is shown in the Fig. 2.4. The detailed simulation procedure follows the methodology described in [38]. Since the continuous channel and source/drain doping profiles are identical for both the Bulk tri-gate and SOI tri-gate devices, the random variability assessed in this study stems from the PTS/substrate region. The value of gate work function used in our simulation is 4.5eV for both SOI tri-gate and bulk tri-gate.

2.3 Results and Discussion

2.3.1 Threshold Voltage Variability

Fig. 2.6 shows the dispersion of subthreshold characteristics for Bulk tri-gate and SOI tri-gate devices with 150 random samples. It is noted that the dispersion among the SOI tri-gate samples is negligible because the substrate doping variation is shielded by the thin BOX. Fig. 2.7 compares the spread of the threshold voltage for

Bulk tri-gate and SOI tri-gate devices. The nominal V_{th} of bulk tri-gate is larger than the SOI tri-gate because bulk tri-gate can deplete excess PTS ion charges in addition to the lightly doped channel. It can be seen that the V_{th} variation of Bulk tri-gate is significantly larger than that of SOI tri-gate. This is because the doping profile of PTS dramatically affects the total depletion charge (Q_{dep}) enclosed by front gates and PTS. For example, near the interface of PTS and channel, one Bulk tri-gate sample with small number of discrete dopant atoms has larger Q_{dep} than that of the other Bulk tri-gate sample with large number of discrete dopant atoms. For the SOI tri-gate, on the contrary, the heavily doped substrate beneath the BOX has negligible impact on V_{th} variation even an ultrathin (10 nm) BOX is used [39].

Fig. 2.8 shows the threshold voltage and its standard deviation (σV_{th}) at different substrate biases (V_{bs}). The similarity of substrate sensitivity in two devices shows that the comparable body-effect has been design through tuning SOI thickness and PTS doping. It is also noted that the σV_{th} dependence on V_{bs} is only about 1mV/V due to the heavily doped PTS. Fig. 2.9 (a) and (b) compare the spread of body-effect coefficient γ for Bulk tri-gate and SOI tri-gate devices under high and low drain bias, respectively. Bulk tri-gate shows slightly larger γ than that of SOI tri-gate because of the high enough PTS doping. The body-effect coefficient can be determined by [15] and [26]:

$$\Upsilon_{SOI} = \left[\frac{1}{1+\left(C_{si}+2C_L\right)/C_{box}} \right] \times \frac{C_{si}+2C_L}{3C_{ox}} \tag{2.1}$$

$$\Upsilon_{BULK} = \frac{C'_{si}+2C'_L}{3C_{ox}} \tag{2.2}$$

However, to model the depletion layer formed in the substrate (W_{dep_sub}), the buried oxide capacitance (C_{box}) in (2.1) should be replaced by

$$C_{box} = \frac{\varepsilon_{ox}/t_{box} \times \varepsilon_{si}/W_{dep_sub}}{\varepsilon_{ox}/t_{box} + \varepsilon_{si}/W_{dep_sub}} \tag{2.3}$$

In addition, the channel depletion capacitance (C'_{si}) in (2.2) should consider the depletion region in PTS (W_{dep_ch}) as

$$C'_{si} = \frac{\varepsilon_{si}}{H_{fin}+W_{dep_ch}} \tag{2.4}$$

Other capacitances are defined as

$$C_{si} = \varepsilon_{si}/H_{fin} \tag{2.5}$$

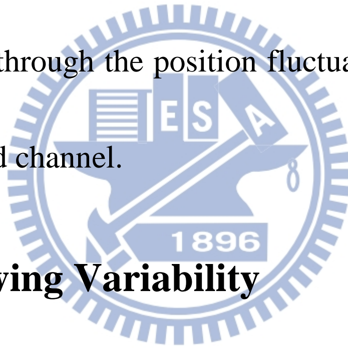
$$C_{ox} = \varepsilon_{ox}/t_{ox} \tag{2.6}$$

$$C_L = (C_{si}/\pi) \times \ln(W_{fin}/r) \tag{2.7}$$

$$C'_L = (C'_{si}/\pi) \times \ln(W_{fin}/r) \tag{2.8}$$

It can be seen from (2.2) that the RDF in PTS will result in significant variation in the numerator of Υ_{BULK} because Q_{dep_ch} as well as W_{dep_ch} shows strong dependence on the PTS profile. For SOI tri-gate, on the contrary, the impact of the variation in W_{dep_sub} is suppressed by the smaller and dominant buried oxide capacitance ($C_{buried} = \varepsilon_{ox}/t_{box}$).

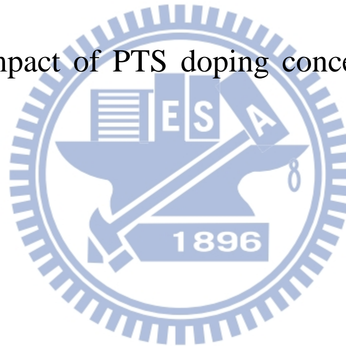
Fig. 2.10 (a) and (b) show the impact of the PTS doping level on the γ of Bulk tri-gate devices under high and low drain bias, respectively. It is noted that the nominal γ shows a discrepancy between continuous and atomistic simulations. It has been reported in [27] that PTS profile locating slightly away from the channel can enhance γ effectively because the carrier conduction path moves downward and the capacitance between the current path and substrate increases. This mechanism is also observed in our simulation result as indicated in the Fig. 2.11. Note that the horizontal axis d_{PTS} is defined as the position of the PTS. It is plausible that this mechanism manifests itself through the position fluctuation of discrete dopant atoms near the interface of PTS and channel.



2.3.2 Subthreshold Swing Variability

Fig. 2.12 shows the substrate-bias dependence of subthreshold swing (SS) and its standard derivation (σSS) for Bulk tri-gate and SOI tri-gate devices. The similarity in subthreshold swing and its back-gate bias dependence in the two devices show that the device electrostatic integrity is similar by employing proper PTS doping/BOX thickness design. It is noted that the subthreshold swing variation is negligible because the channel is well controlled by the gate. Despite of the minor variation in SS, its correlation with V_{th} variation is also important for the circuit design considering mismatch [40]. Fig. 2.13 shows the correlation of threshold voltage and

subthreshold swing for Bulk tri-gate devices with a varying PTS doping. It can be seen from the inset that the correlation coefficient decreases with decreasing channel length. That means the subthreshold current mismatch characteristics may be different between the long and short channel devices. When the fin width and fin height are much smaller than the channel length, threshold voltage and subthreshold swing increase with the PTS doping concentration due to the enhancement of body effect. However, for the short channel devices, serious drain to source electric field coupling makes threshold voltage decrease and subthreshold swing increase. In other words, SCEs counterbalance the impact of PTS doping concentration on threshold voltage and subthreshold swing.



2.4 Summary

In this chapter, we investigate and report the body-effect induced variability in Bulk tri-gate MOSFETs. Through 3-D atomistic simulation, the random dopant fluctuations in the Punch-Through-Stopper (PTS) region of Bulk tri-gate devices are examined. Our study indicates that to achieve an efficient threshold-voltage modulation through substrate bias, the high-doping PTS region may introduce excess variation in Bulk tri-gate devices. This effect has to be considered when one-to-one comparisons between Bulk tri-gate and SOI tri-gate regarding device variability are made.

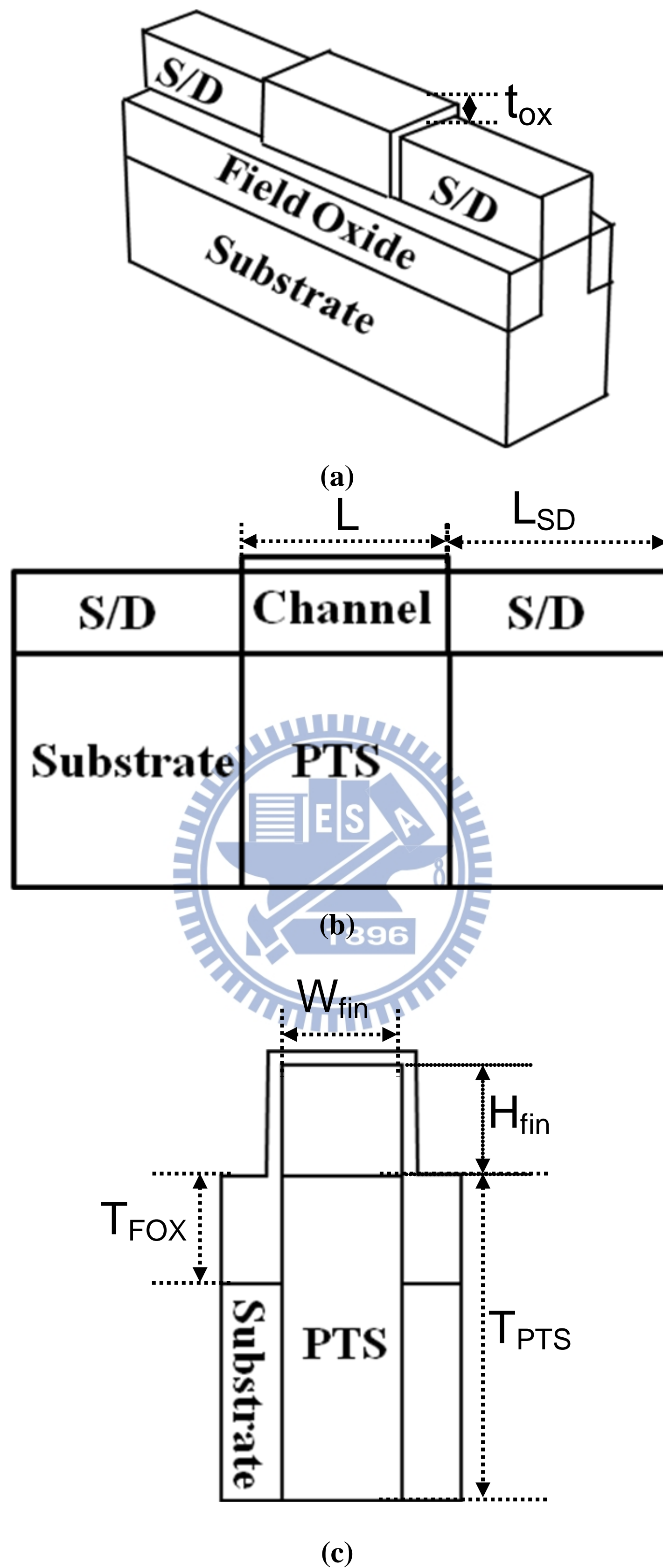


Fig. 2.1 Schematics of (a) 3-D Bulk tri-gate structure and the corresponding cross-sectional view along (b) the channel and (c) the fin-width direction. It is noted that the PTS doping profile does not extend to the substrate below source/drain.

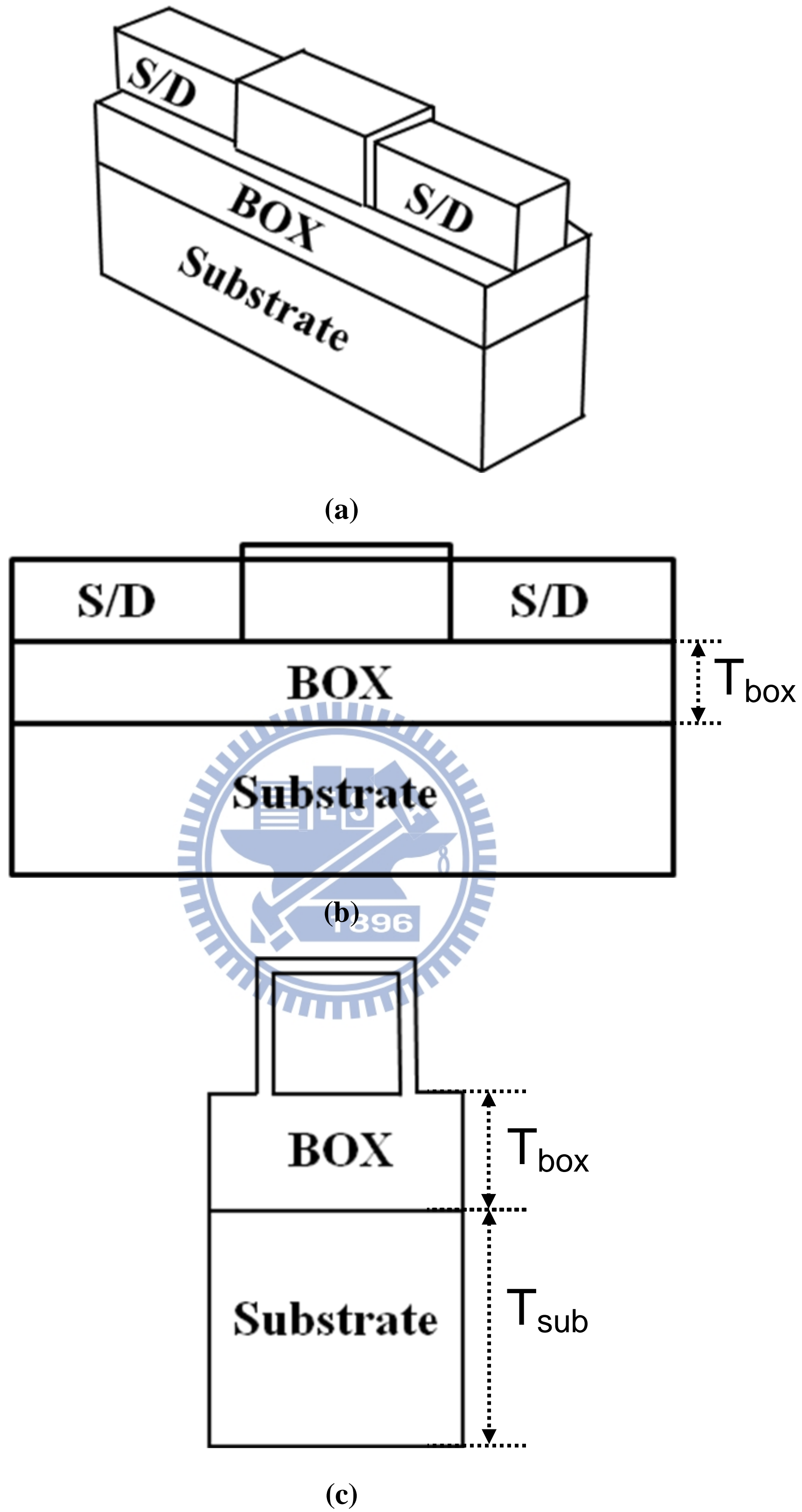


Fig. 2.2 Schematics of (a) 3-D SOI tri-gate structure and the corresponding cross-sectional view along (b) the channel and (c) the fin-width direction.

Table 2.1 Device parameters of the simulated Bulk and SOI devices.

	Bulk tri-gate	**SOI tri-gate**
L	25nm	25nm
L_{SD}	20nm	20nm
W_{fin}	10nm	10nm
H_{fin}	10nm	10nm
t_{ox}	1.3nm	1.3nm
	T_{PTS}=30nm	T_{box}=10nm
	T_{FOX}=10nm	T_{sub}=20nm
Channel Doping	$1x10^{17}cm^{-3}$	$1x10^{17}cm^{-3}$
Substrate doping	$1x10^{17}cm^{-3}$	$1x10^{19}cm^{-3}$
Source/Drain doping	$2x10^{20}cm^{-3}$	$2x10^{20}cm^{-3}$
Variation source	PTS doping $N_{PTS}=1x10^{19}cm^{-3}$	Substrate doping $N_{sub}=1x10^{19}cm^{-3}$

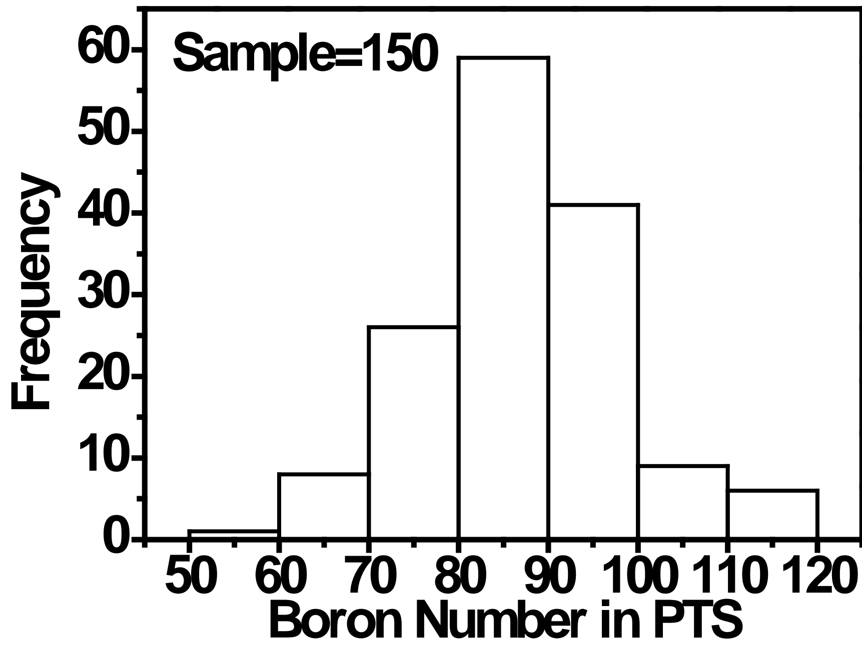


Fig. 2.3 Total number of impurity atoms follows a Poisson distribution in the PTS region.

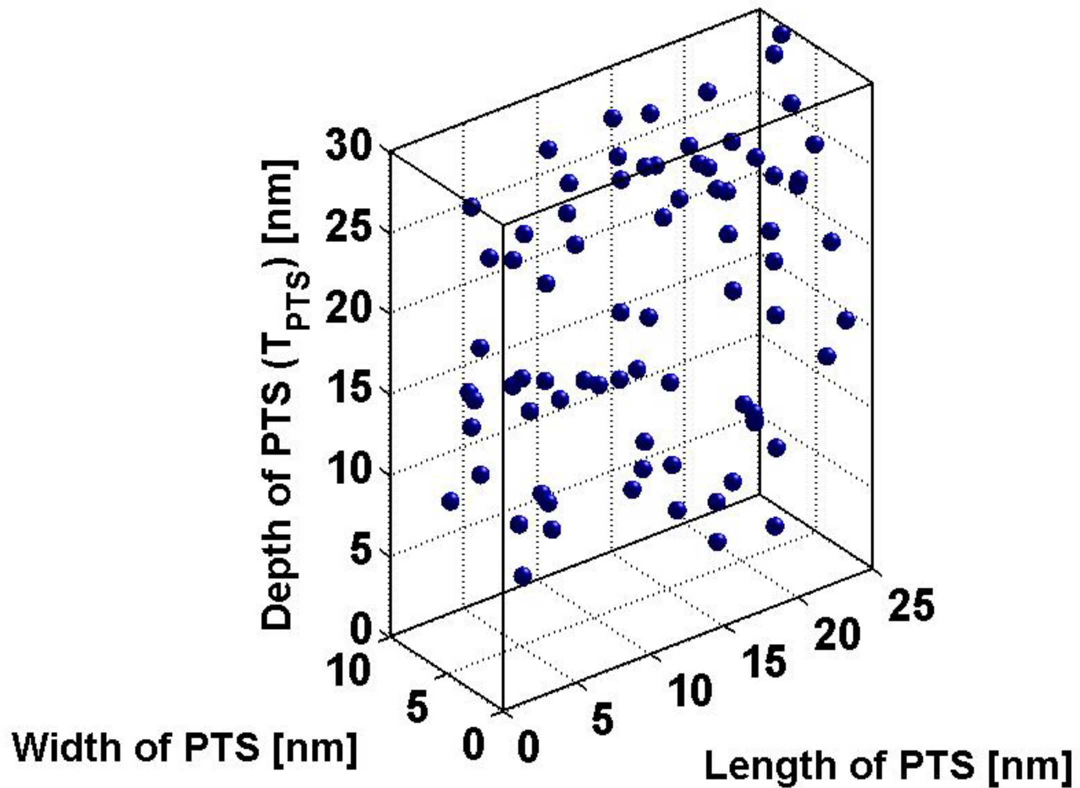


Fig. 2.4 Impurity atoms space distribution in the PTS region.

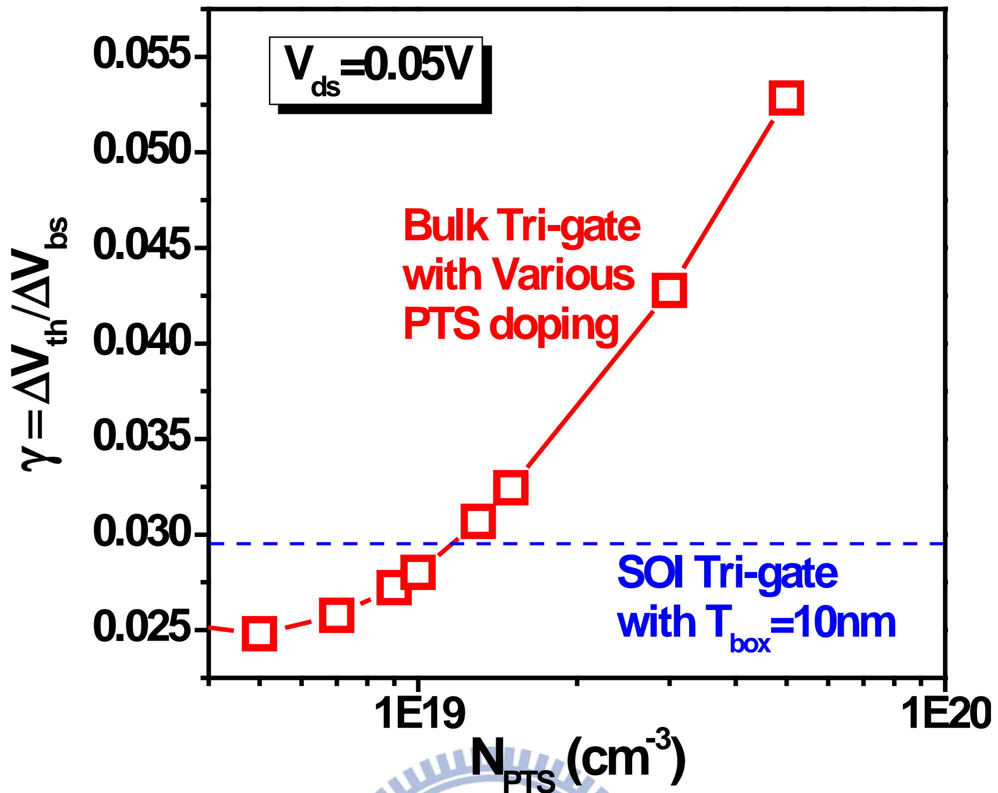
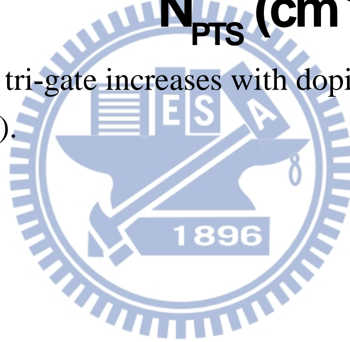


Fig. 2.5 Body factor of Bulk tri-gate increases with doping concentration of the punch-through-stopper (PTS).



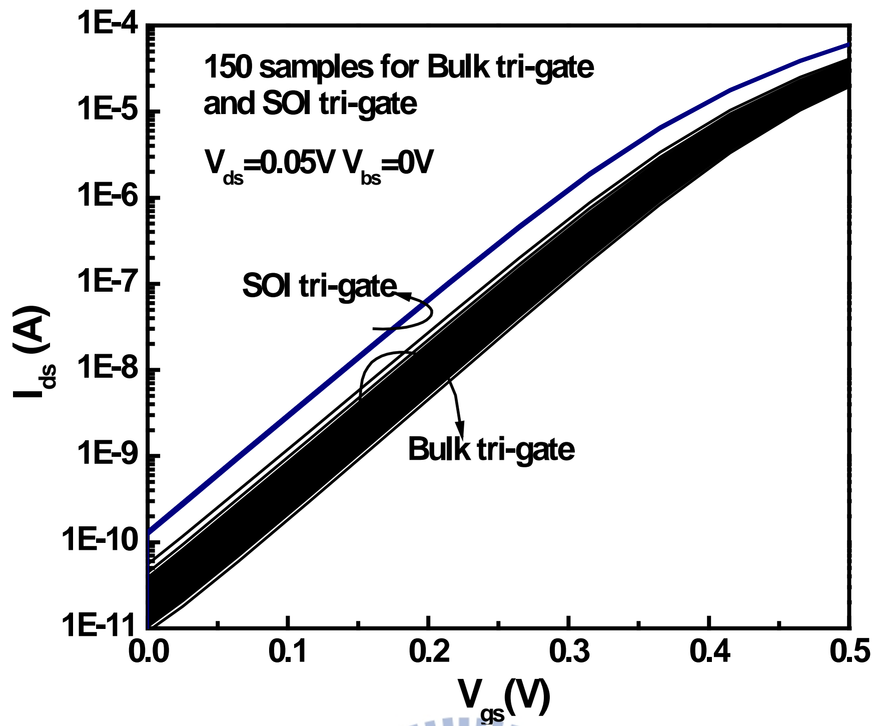


Fig. 2.6 Subthreshold characteristics of 150 samples of Bulk tri-gate and SOI tri-gate devices.

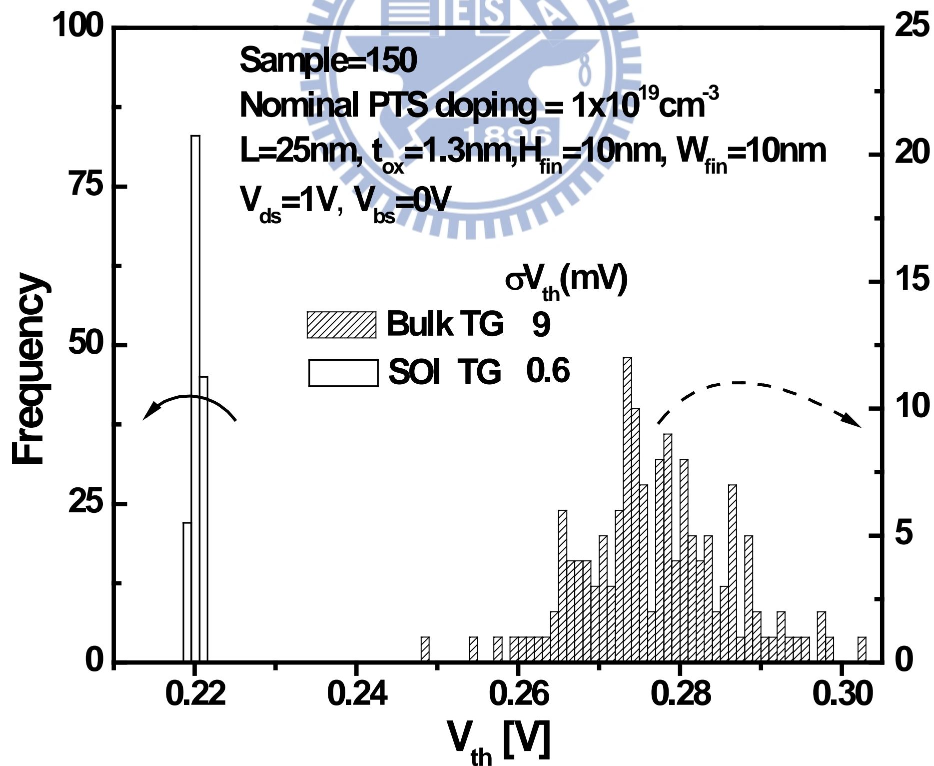


Fig. 2.7 Comparison of the V_{th} spread for Bulk tri-gate and SOI tri-gate devices. V_{th} is determined by the constant current $I_0=(W_{total}/L)*100nA$ with $W_{total}=2*H_{fin}+W_{fin}$.

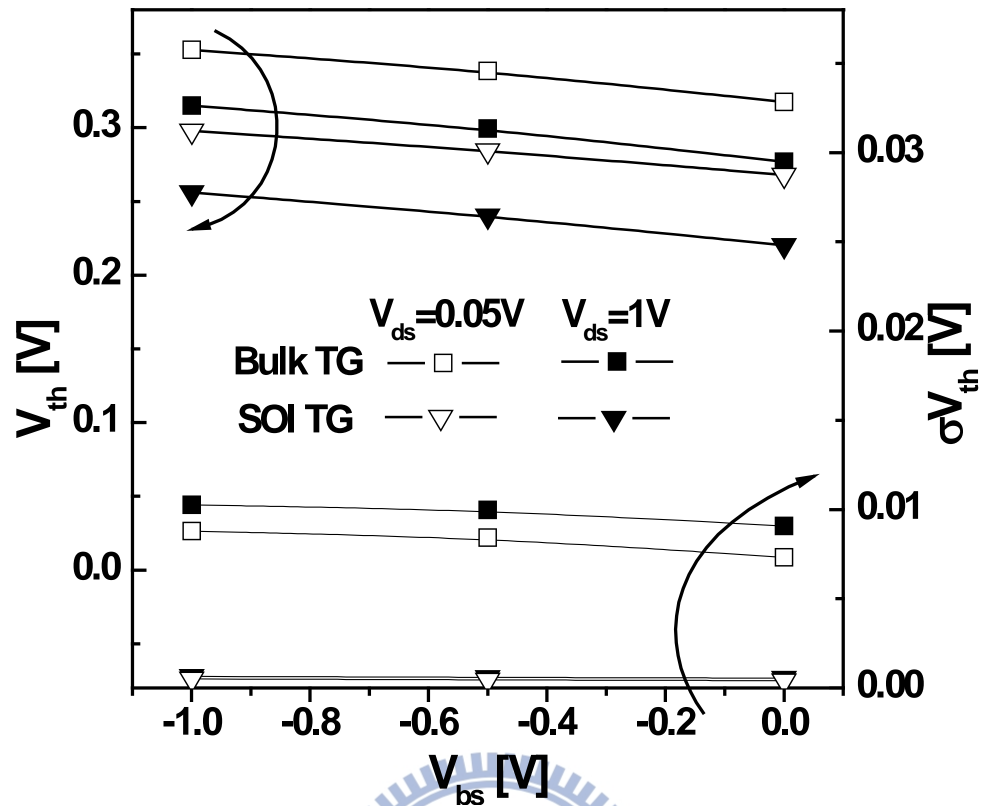
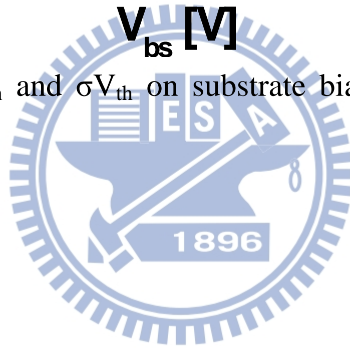


Fig. 2.8 Dependence of V_{th} and σV_{th} on substrate bias for Bulk tri-gate and SOI tri-gate devices.



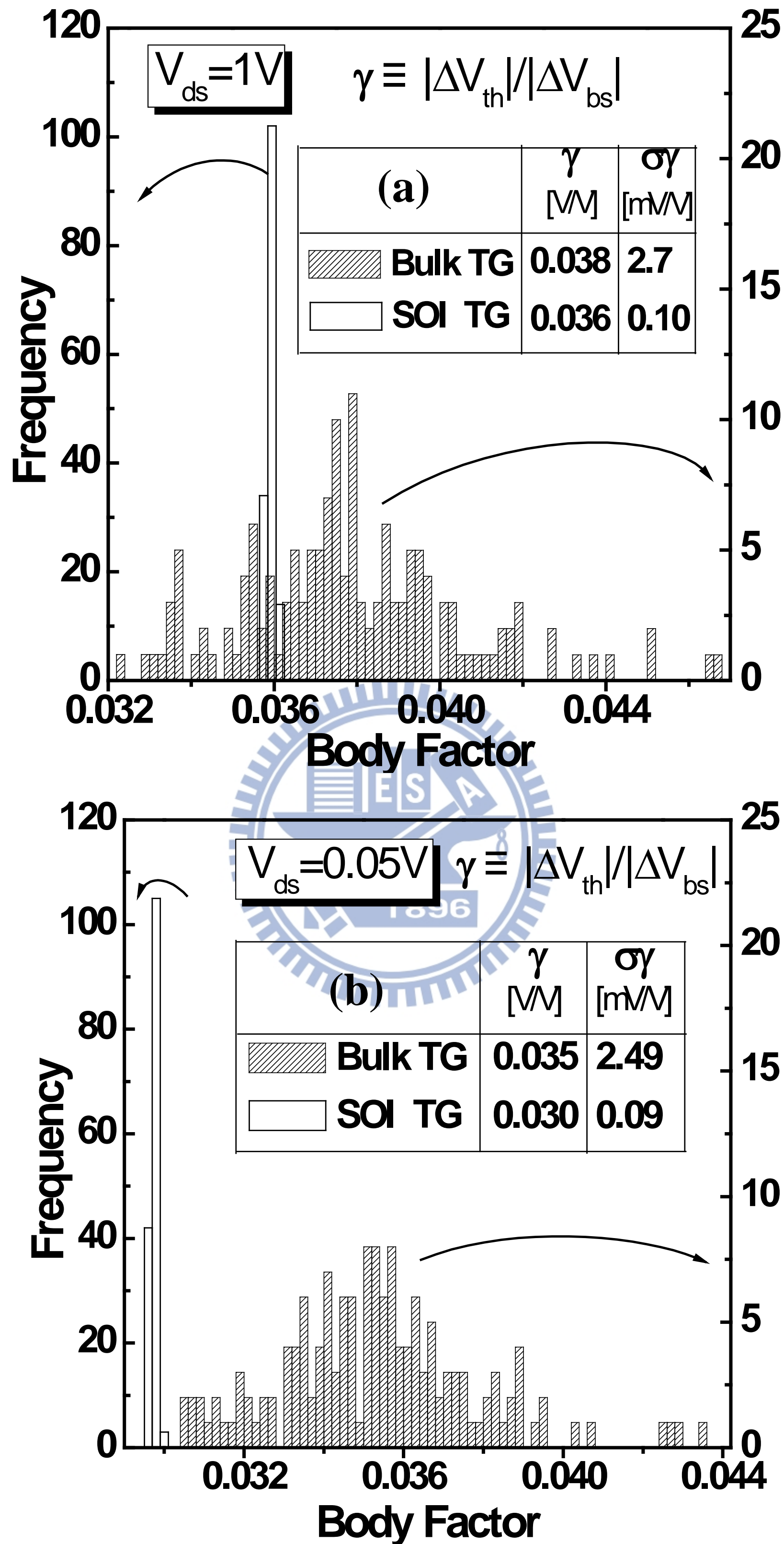


Fig. 2.9 Comparison of the γ dispersion for Bulk tri-gate and SOI tri-gate deices under (a) high drain and (b) low drain bias. $\gamma \equiv |\Delta V_{th}|/|\Delta V_{bs}|$.

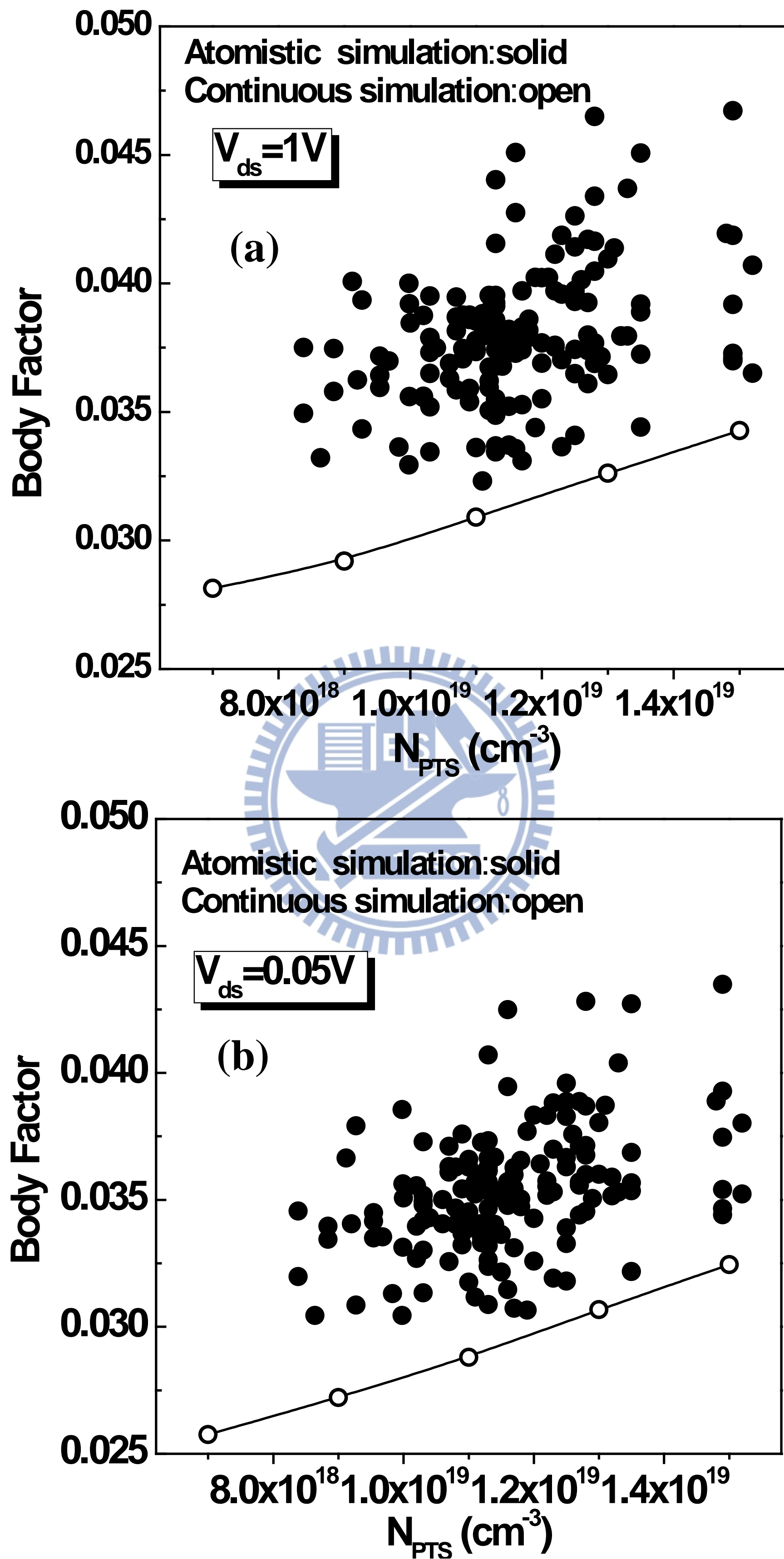


Fig. 2.10 Impact of the PTS doping level on γ under (a) high drain and (b) low drain bias.

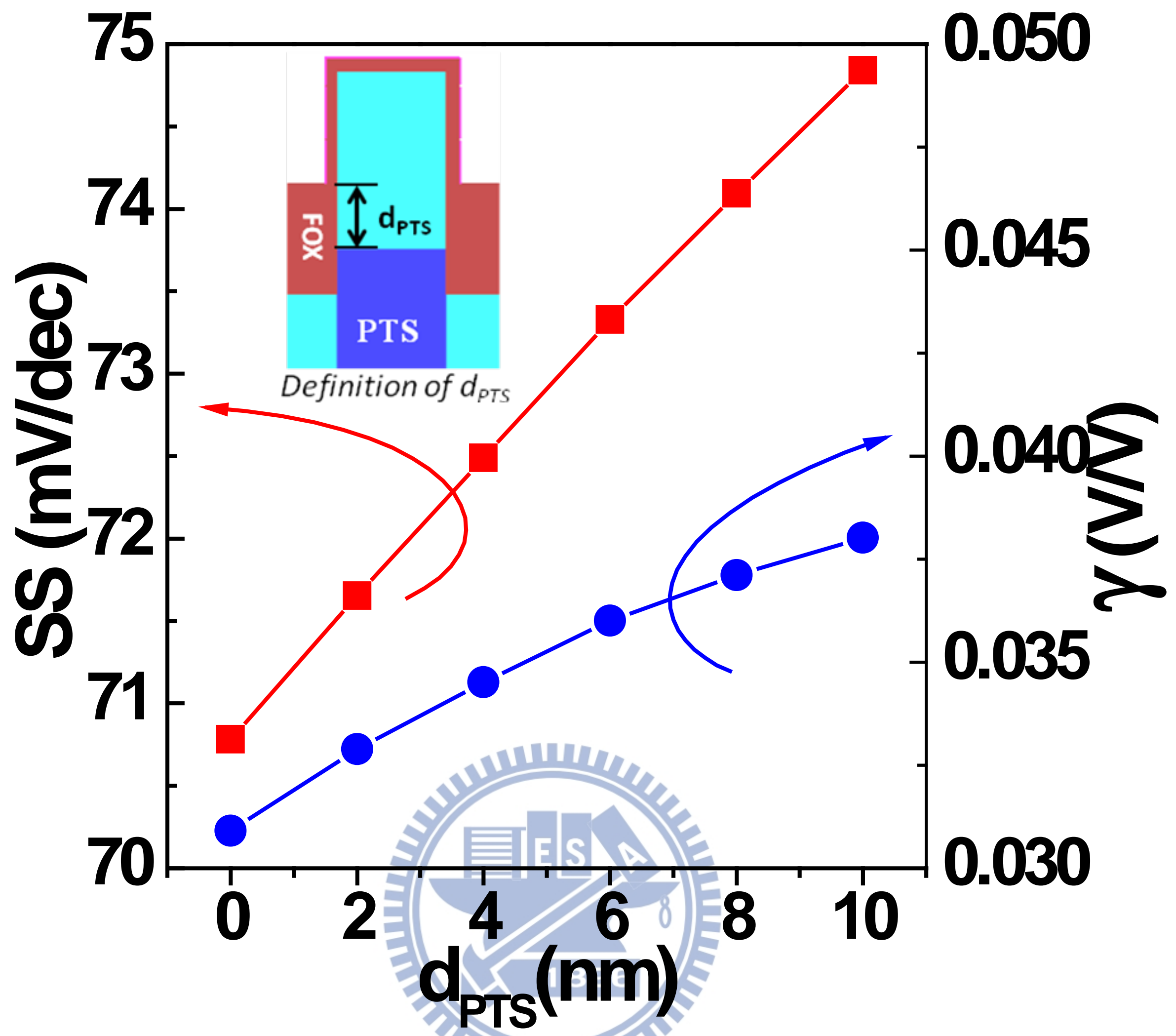


Fig. 2.11 The impact of the PTS depth on subthreshold swing (SS) and body factor (γ).

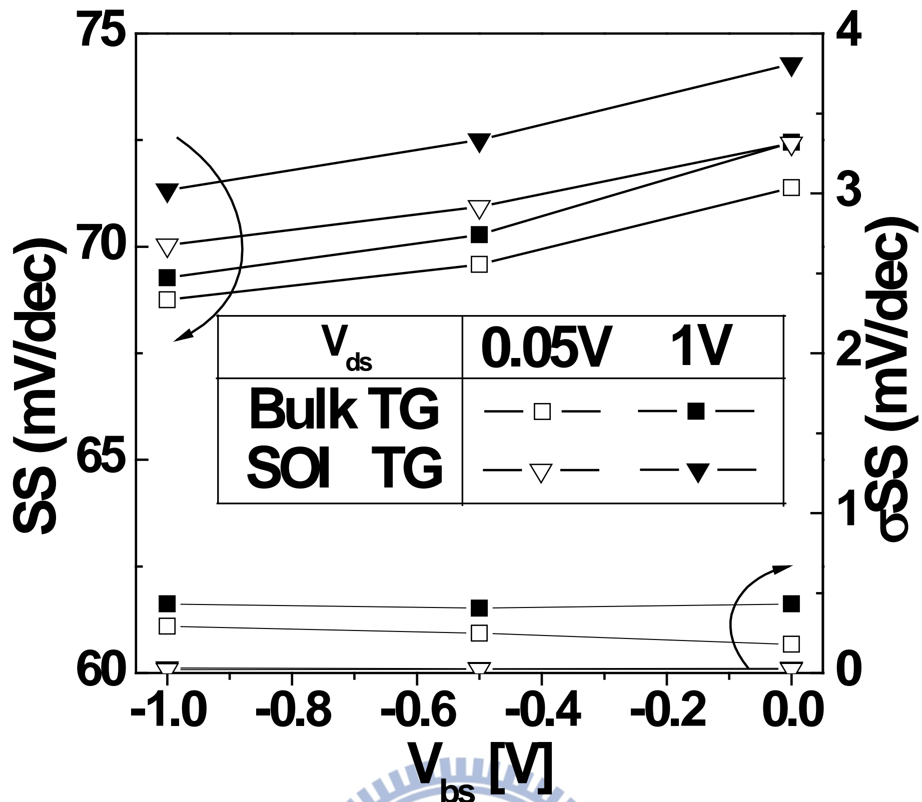


Fig. 2.12 Dependence of SS and σSS on substrate bias for Bulk tri-gate and SOI tri-gate devices.

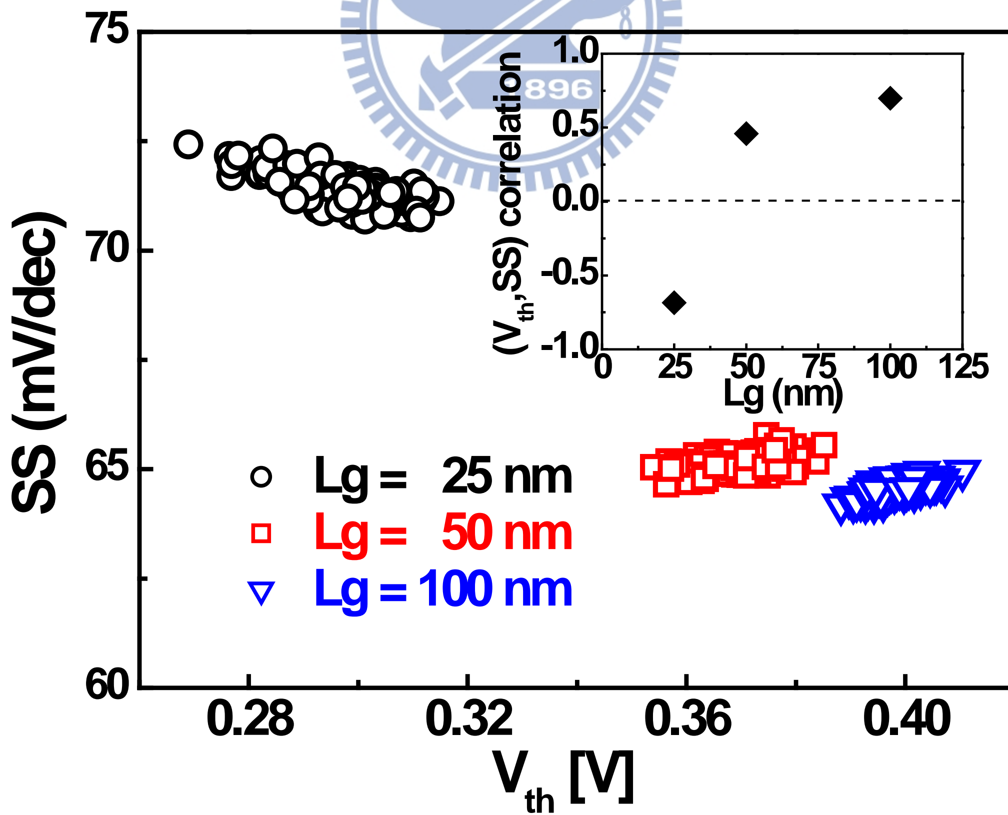


Fig. 2.13 Correlation plot between V_{th} and SS for Bulk tri-gate devices. The inset shows the correlation coefficient for Bulk tri-gate devices with various channel lengths.

Chapter 3
Analytical Subthreshold Model For Tri-Gate SOI MOSFETs With Thin Buried Oxide

3.1 Introduction

Due to superior electrostatic control, tri-gate MOSFETs provide improved immunity to short-channel effects (SCE) and become a promising candidate to extend the CMOS scaling. In order to physically assess the electrostatic integrity and facilitate device design for tri-gate SOI MOSFETs, an analytical subthreshold model is important. Although [22] has provided a subthreshold model for multi-gate SOI MOSFETs, the BOX-thickness scalability of this model is not accurate. In this work, we provide an analytical subthreshold model for tri-gate SOI MOSFETs by improving the BOX-thickness scalability of the model in [22].

Due to the homogeneous dielectric approximation in the BOX region, the original model in [22] is only suitable for the SOI tri-gate with BOX thickness from 10 to 30nm. When the BOX is thinner than 10nm, the discontinuity of the vertical electric field at BOX/channel interface becomes significant. We have considered this effect in our new model by making our potential solutions satisfy the boundary

condition (3.5). On the other hand, as the BOX thickness is larger than 30nm, the fringing field induced by the drain and source through the BOX leads to an increase in the channel potential. Since our potential solutions satisfy the boundary conditions (3.4b)-(3.4e) and (3.6) in the BOX region, the channel potential shift induced by the fringing field is well predicted by our model.

3.2 Subthreshold Model for Tri-gate SOI MOSFETs with Thin BOX

3.2.1 Poisson's Equation and Boundary Conditions

The schematic device structure of tri-gate SOI MOSFETs is shown in Fig. 2.1. The potential distribution in the subthreshold regime can be calculated by solving the 3D Poisson equation (3.1) within the silicon channel

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$$\frac{\partial^2 \varphi_{ch}(x,y,z)}{\partial x^2} + \frac{\partial^2 \varphi_{ch}(x,y,z)}{\partial y^2} + \frac{\partial^2 \varphi_{ch}(x,y,z)}{\partial z^2} = -\frac{qN_{ch}}{\varepsilon_{ch}} \tag{3.1}$$

Where ε_{ch} and N_{ch} are the dielectric constant and doping concentration of the silicon fin, respectively.

In addition, the electrostatic potential in the buried oxide region can be described by 3D Laplace's equation (3.2).

$$\frac{\partial^2 \varphi_{box}(x,y,z)}{\partial x^2} + \frac{\partial^2 \varphi_{box}(x,y,z)}{\partial y^2} + \frac{\partial^2 \varphi_{box}(x,y,z)}{\partial z^2} = 0 \tag{3.2}$$

The required boundary conditions for $\varphi_{ch}(x,y,z)$ and $\varphi_{box}(x,y,z)$ can be

described as

$$\varphi_{ch}(x,y,0)=V_{gb}-V_{fb}-t_{ib}\frac{\varepsilon_{ch}}{\varepsilon_{ox}}\frac{\partial\varphi_{ch}(x,y,z)}{\partial z}\bigg|_{z=0} \tag{3.3a}$$

$$\varphi_{ch}(x,y,W_{fin})=V_{gf}-V_{fb}-t_{if}\frac{\varepsilon_{ch}}{\varepsilon_{ox}}\frac{\partial\varphi_{ch}(x,y,z)}{\partial z}\bigg|_{z=W_{fin}} \tag{3.3b}$$

$$\varphi_{ch}(H_{fin},y,z)=V_{gt}-V_{fb}-t_{it}\frac{\varepsilon_{ch}}{\varepsilon_{ox}}\frac{\partial\varphi_{ch}(x,y,z)}{\partial x}\bigg|_{x=H_{fin}} \tag{3.3c}$$

$$\varphi_{ch}(x,0,z)=-\varphi_{ms}+V_{s} \tag{3.3d}$$

$$\varphi_{ch}(x,L,z)=-\varphi_{ms}+V_{d} \tag{3.3e}$$

$$\varphi_{box}(-t_{ox.u},y,z)=V_{gu}-V_{fb} \tag{3.4a}$$

$$\varphi_{box}(x,0,z)=V_{gu}-V_{fb}+\frac{(-\varphi_{ms}+V_{s})-(V_{gu}-V_{fb})}{t_{ox.u}}(x+t_{ox.u}) \tag{3.4b}$$

$$\varphi_{box}(x,L,z)=V_{gu}-V_{fb}+\frac{(-\varphi_{ms}+V_{d})-(V_{gu}-V_{fb})}{t_{ox.u}}(x+t_{ox.u}) \tag{3.4c}$$

$$\varphi_{box}(x,y,-t_{ib})=V_{gu}-V_{fb}+\frac{(V_{gb}-V_{fb})-(V_{gu}-V_{fb})}{t_{ox.u}}(x+t_{ox.u}) \tag{3.4d}$$

$$\varphi_{box}(x,y,W_{fin}+t_{if})=V_{gu}-V_{fb}+\frac{(V_{gf}-V_{fb})-(V_{gu}-V_{fb})}{t_{ox.u}}(x+t_{ox.u}) \tag{3.4e}$$

$$\varepsilon_{ch}\cdot\frac{\partial\varphi_{ch}(x,y,z)}{\partial x}\bigg|_{x=0}=\varepsilon_{ox}\cdot\frac{\partial\varphi_{box}(x,y,z)}{\partial x}\bigg|_{x=0} \tag{3.5}$$

$$\frac{\partial\varphi_{ch}(x,y,z)}{\partial y}\bigg|_{x=0}=\frac{\partial\varphi_{box}(x,y,z)}{\partial y}\bigg|_{x=0} \tag{3.6}$$

Here ε_{ch} and ε_{ox} are the permittivity of channel material and oxide, respectively. W_{fin}, H_{fin} and L are defined as fin width, fin height, and channel length, respectively. t_{ib}, t_{if}, t_{it} and $t_{ox.u}$ are thickness of back gate dielectric, front gate

dielectric, top gate dielectric , and buried oxide, respectively. V_{gb}, V_{gf}, V_{gt}, V_{gu}, V_s, and V_d are the voltage biases of back gate, front gate, top gate, buried gate, source, and drain terminal, respectively. V_{fb} is the flat-band voltage for these gate terminals. φ_{ms} is the built-in potential of the source/drain to the channel.

3.2.2 Power Series Solution to Boundary Value Problems

To solve the potential solution in (3.1) using the above boundary conditions, we divide the 3D boundary value problems into three sub-problems, including 1-D Poisson equation, 2-D, and 3-D Laplace equation [22]. Using the superposition principle, the 3D Poisson equation can be solved sequentially by 1-D Poisson equation, 2-D and 3-D Laplace's equation. So the complete channel potential solution is $\varphi_{ch}(x,y,z) = \varphi_{ch,1}(x) + \varphi_{ch,2}(x,y) + \varphi_{ch,3}(x,y,z)$, where $\varphi_{ch,1}(x)$, $\varphi_{ch,2}(x,y)$ and $\varphi_{ch,3}(x,y,z)$ are the solutions of 1-D, 2-D, and 3-D sub-problems in the channel, respectively. The 1-D solution can be expressed as

$$\varphi_{ch,1}(x) = -\frac{qN_{ch}}{2\varepsilon_{ch}}x^2 + Ax + B \tag{3.7}$$

$$A = \frac{(V_{gt}-V_{fb}) - (V_{gu}-V_{fb}) + \frac{qN_{ch}}{2\varepsilon_{ch}}\left(H_{fin}^2 + 2H_{fin}\cdot t_{it}\frac{\varepsilon_{ch}}{\varepsilon_{ox}}\right)}{H_{fin} + t_{it}\frac{\varepsilon_{ch}}{\varepsilon_{ox}} + t_{ox.u}\frac{\varepsilon_{ch}}{\varepsilon_{ox}}} \tag{3.8}$$

$$B = \frac{\varepsilon_{ch}}{\varepsilon_{ox}}A\cdot t_{ox.u} + (V_{gu}-V_{fb}) \tag{3.9}$$

In solving the 2-D and 3-D sub-problems, the boundary conditions [(3.3a)-(3.3c)] of gate oxide/channel interface are simplified by converting the gate oxide dielectric

thickness to $(\varepsilon_{ch}/\varepsilon_{ox})$ times and replacing the gate oxide region with an equivalent channel-material region. The electric field discontinuity across the gate oxide and channel interface can thus be eliminated. In other words, the channel region and the gate oxide region are treated as homogeneous cuboids with an effective width W_{eff} and an effective H_{eff} defined by (3.10) and (3.11), respectively.

$$W_{eff} = W_{fin} + \frac{\varepsilon_{ch}}{\varepsilon_{ox}}(t_{if} + t_{ib}) \tag{3.10}$$

$$H_{eff} = H_{fin} + t_{it}\frac{\varepsilon_{ch}}{\varepsilon_{ox}} \tag{3.11}$$

The 2-D solution $\varphi_{ch,2}(x, y)$ can be calculated using the method of separation of variables

$$\varphi_{ch,2}(x, y) = \sum_{n=1}^{\infty}\left\{\left[B_n \sinh\left(\frac{n\pi}{H_{eff}}y\right) + E_n \sinh\left(\frac{n\pi}{H_{eff}}(L - y)\right)\right]\cdot \sin\left(\frac{n\pi x}{H_{eff}}\right)\right\} \tag{3.12a}$$

where

$$B_n = \frac{1}{\sinh\left(\frac{n\pi L}{H_{eff}}\right)}\left[\frac{qN_{ch}\cdot(H_{eff})^2}{\varepsilon_{ch}\pi}\left(\frac{2\cdot[(-1)^n - 1]}{(n\pi)^3} - \frac{(-1)^n}{n}\right) + \frac{2AH_{eff}(-1)^n}{n} + 2(-\varphi_{ms} + V_d - B)\frac{1-(-1)^n}{n}\right]$$

(3.12b)

$$E_n = \frac{1}{\sinh\left(\frac{n\pi L}{H_{eff}}\right)}\left[\frac{qN_{ch}\cdot(H_{eff})^2}{\varepsilon_{ch}\pi}\left(\frac{2\cdot[(-1)^n - 1]}{(n\pi)^3} - \frac{(-1)^n}{n}\right) + \frac{2AH_{eff}(-1)^n}{n} + 2(-\varphi_{ms} + V_s - B)\frac{1-(-1)^n}{n}\right]$$

(3.12c)

For the channel/buried oxide interface, both the potential distribution in the channel $\varphi_{ch,3}(x, y, z)$ and that in the buried oxide $\varphi_{box,3}(x, y, z)$ have to be

considered to satisfy the boundary conditions (3.5) and (3.6). Similarly, the 3-D solution $\varphi_{ch,3}(x,y,z)$ can be obtained and expressed as

$$\varphi_{ch,3}(x,y,z)=\sum_{n=1}^{\infty}\sum_{m=1}^{\infty}\left[B_{n,m}\sinh\left(\sqrt{\left(\frac{n\pi}{H_{eff}}\right)^2+\left(\frac{m\pi}{L}\right)^2}\cdot z\right)\right]\cdot\sinh\left(\frac{n\pi}{H_{eff}}x\right)\cdot\sin\left(\frac{m\pi}{L}y\right)$$
$$+\sum_{n=1}^{\infty}\sum_{m=1}^{\infty}\left[E_{n,m}\sinh\left(\sqrt{\left(\frac{n\pi}{H_{eff}}\right)^2+\left(\frac{m\pi}{L}\right)^2}\cdot(W_{eff}-z)\right)\right]\cdot\sinh\left(\frac{n\pi}{H_{eff}}x\right)\cdot\sin\left(\frac{m\pi}{L}y\right)$$
$$+\sum_{i=1}^{\infty}\sum_{m=1}^{\infty}H_{i,m}\sinh\left(\sqrt{\left(\frac{i\pi}{W_{eff}}\right)^2+\left(\frac{m\pi}{L}\right)^2}(H_{eff}-x)\right)\cdot\sin\left(\frac{i\pi}{W_{eff}}z\right)\cdot\sin\left(\frac{m\pi}{L}y\right)$$

(3.13a)

The coefficients $B_{n,m}$, $E_{n,m}$ and $H_{i,m}$ in (3.13a) can be expressed as

$$B_{n,m}=\frac{1}{\sinh\left(\sqrt{\left(\frac{n\pi}{H_{eff}}\right)^2+\left(\frac{m\pi}{L}\right)^2}\cdot W_{eff}\right)}\times$$
$$\left\{\begin{array}{l}\frac{2}{m\pi}\left(1-(-1)^m\right)\times\left[\begin{array}{l}2(V_{gf}-V_{fb}-B)\frac{1-(-1)^n}{n\pi}+\frac{2AH_{eff}\left(-1\right)^n}{n\pi}+\\ \frac{qN_{ch}\cdot\left(H_{eff}\right)^2}{\varepsilon\pi_{ch}}\left(\frac{2\cdot\left[(-1)^n-1\right]}{(n\pi)^3}-\frac{(-1)^n}{n}\right)\end{array}\right]\\ -B_n\frac{2}{L}\cdot\frac{\frac{-1}{m\pi/L}(-1)^m\sinh\left(\frac{n\pi L}{H_{eff}}\right)}{1+\left(\frac{n}{H_{eff}}\times\frac{L}{m}\right)^2}-E_n\frac{2}{L}\cdot\frac{\frac{1}{m\pi/L}\sinh\left(\frac{n\pi L}{H_{eff}}\right)}{1+\left(\frac{n}{H_{eff}}\times\frac{L}{m}\right)^2}\end{array}\right\}\quad(3.13b)$$

$$E_{n,m} = \frac{1}{\sinh\left(\sqrt{\left(\frac{n\pi}{H_{eff}}\right)^2 + \left(\frac{m\pi}{L}\right)^2} \cdot W_{eff}\right)} \times$$

$$\left\{ \begin{array}{l} \frac{2}{m\pi}\left(1-(-1)^m\right) \times \left[\begin{array}{l} 2(V_{gb} - V_{fb} - B)\frac{1-(-1)^n}{n\pi} + \frac{2\mathrm{AH_{eff}}\left(-1\right)^{\mathrm{n}}}{n\pi} + \\ \frac{\mathrm{qN_{ch}} \cdot \left(H_{eff}\right)^2}{\varepsilon_{\mathrm{ch}}\pi} \left(\frac{2 \cdot \left[(-1)^n - 1\right]}{\left(\mathrm{n}\pi\right)^3} - \frac{(-1)^n}{n} \right) \end{array} \right] \\ -\mathrm{B_n}\frac{2}{L} \cdot \frac{\frac{-1}{m\pi/L}(-1)^m \sinh\left(\frac{n\pi L}{H_{eff}}\right)}{1+\left(\frac{n}{H_{eff}} \times \frac{L}{m}\right)^2} - E_n\frac{2}{L} \cdot \frac{\frac{1}{m\pi/L}\sinh\left(\frac{n\pi L}{H_{eff}}\right)}{1+\left(\frac{n}{H_{eff}} \times \frac{L}{m}\right)^2} \end{array} \right\} \quad (3.13c)$$

$$H_{i,m} = \frac{\sinh\left(\lambda_{i,m} \cdot t_{ox,u}\right)}{\sinh\left(\lambda_{i,m} \cdot H_{eff}\right)} \times \frac{RHS_{n,m}}{LHS_{i,m}} \quad (3.13d)$$

where

$$\lambda_{i,m} = \sqrt{\left(\frac{i\pi}{W_{eff}}\right)^2 + \left(\frac{m\pi}{L}\right)^2} \quad (3.13e),$$

$$LHS_{i,m} = \lambda_{i,m}\cosh(\lambda_{i,m} t_{ox,u}) + \frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_{\mathrm{ox}}} \frac{\sinh\left(\lambda_{i,m} \cdot t_{ox,u}\right)}{\sinh\left(\lambda_{i,m} \cdot H_{eff}\right)} \lambda_{i,m}\cosh(\lambda_{i,m} H_{eff}) \quad (3.13f),$$

$$RHS_{n,m}=\frac{\varepsilon_{ch}}{\varepsilon_{ox}}\sum_{n=1}^{\infty}\left[B_n\frac{2}{L}\cdot\frac{\frac{-1}{m\pi/L}(-1)^m\sinh\left(\frac{n\pi L}{H_{eff}}\right)}{1+\left(\frac{n}{H_{eff}}\times\frac{L}{m}\right)^2}+E_n\frac{2}{L}\cdot\frac{\frac{1}{m\pi/L}\sinh\left(\frac{n\pi L}{H_{eff}}\right)}{1+\left(\frac{n}{H_{eff}}\times\frac{L}{m}\right)^2}\right]\times\left(\frac{n\pi}{H_{eff}}\right)\times\frac{2\left(1-(-1)^i\right)}{i\pi}$$

$$+\frac{\varepsilon_{ch}}{\varepsilon_{ox}}\sum_{n=1}^{\infty}\left[B_{n,m}\cdot\frac{2}{W_{eff}}\cdot\frac{\frac{-1}{i\pi/W_{eff}}(-1)^i\sinh\left(\gamma_{n,m}\cdot W_{eff}\right)}{1+\left(\frac{\gamma_{n,m}}{i\pi/W_{eff}}\right)^2}+E_{n,m}\cdot\frac{2}{W_{eff}}\cdot\frac{\frac{1}{i\pi/W_{eff}}\sinh\left(\gamma_{n,m}\cdot W_{eff}\right)}{1+\left(\frac{\gamma_{n,m}}{i\pi/W_{eff}}\right)^2}\right]\times\left(\frac{n\pi}{H_{eff}}\right)$$

$$-\sum_{n=1}^{\infty}\left[K_n\frac{2}{L}\cdot\frac{\frac{-1}{m\pi/L}(-1)^m\sinh\left(\frac{n\pi L}{t_{ox,u}}\right)}{1+\left(\frac{n}{t_{ox}}\times\frac{L}{m}\right)^2}+P_n\frac{2}{L}\cdot\frac{\frac{1}{m\pi/L}\sinh\left(\frac{n\pi L}{t_{ox,u}}\right)}{1+\left(\frac{n}{t_{ox,u}}\times\frac{L}{m}\right)^2}\right]\times\left(\frac{n\pi\cdot(-1)^n}{t_{ox,u}}\right)\times\frac{2\left(1-(-1)^i\right)}{i\pi}$$

$$-\sum_{n=1}^{\infty}\left[K_{n,m}\cdot\frac{2}{W_{eff}}\cdot\frac{\frac{-1}{i\pi/W_{eff}}(-1)^i\sinh\left(\Gamma_{n,m}\cdot W_{eff}\right)}{1+\left(\frac{\Gamma_{n,m}}{i\pi/W_{eff}}\right)^2}+P_{n,m}\cdot\frac{2}{W_{eff}}\cdot\frac{\frac{1}{i\pi/W_{eff}}\sinh\left(\Gamma_{n,m}\cdot W_{eff}\right)}{1+\left(\frac{\Gamma_{n,m}}{i\pi/W_{eff}}\right)^2}\right]\times\left(\frac{n\pi\cdot(-1)^n}{t_{ox,u}}\right),$$

(3.13g)

$$\Gamma_{n,m}=\sqrt{\left(\frac{n\pi}{t_{ox,u}}\right)^2+\left(\frac{m\pi}{L}\right)^2}\quad(3.13\text{h}),$$

and

$$\gamma_{n,m}=\sqrt{\left(\frac{n\pi}{H_{eff}}\right)^2+\left(\frac{m\pi}{L}\right)^2}\quad(3.13\text{i}).$$

The coefficients K_n, P_n, $K_{n,m}$ and $P_{n,m}$ in (3.13g) stem from the 2-D and 3-D potential solution in the buried oxide region, and they can be expressed as

$$K_n=\frac{2}{\sinh\left(\frac{n\pi L}{t_{ox,u}}\right)}\left(-\varphi_{ms}+V_s-B\right)\frac{(-1)^{n+1}}{n\pi}\quad(3.13\text{j})$$

$$P_n=\frac{2}{\sinh\left(\frac{n\pi L}{t_{ox,u}}\right)}\left(-\varphi_{ms}+V_d-B\right)\frac{(-1)^{n+1}}{n\pi}\quad(3.13\text{k})$$

$$K_{n,m} = \frac{1}{\sinh\left(\sqrt{\left(\frac{n\pi}{t_{ox,u}}\right)^2 + \left(\frac{m\pi}{L}\right)^2} \cdot W_{eff}\right)} \left\{ \begin{array}{l} \frac{2}{m\pi}\left(1-(-1)^m\right) \times \left[(V_{gf} - V_{fb} - B)\frac{(-1)^{n+1}}{n\pi} \right] \\ -K_n \frac{2}{L} \cdot \frac{\frac{-1}{m\pi/L}(-1)^m \sinh\left(\frac{n\pi L}{t_{ox,u}}\right)}{1+\left(\frac{n}{t_{ox,u}} \times \frac{L}{m}\right)^2} - P_n \frac{2}{L} \cdot \frac{\frac{1}{m\pi/L}\sinh\left(\frac{n\pi L}{t_{ox,u}}\right)}{1+\left(\frac{n}{t_{ox,u}} \times \frac{L}{m}\right)^2} \end{array} \right\}$$

(3.13m)

$$P_{n,m} = \frac{1}{\sinh\left(\sqrt{\left(\frac{n\pi}{t_{ox,u}}\right)^2 + \left(\frac{m\pi}{L}\right)^2} \cdot W_{eff}\right)} \left\{ \begin{array}{l} \frac{2}{m\pi}\left(1-(-1)^m\right) \times \left[(V_{gb} - V_{fb} - B)\frac{(-1)^{n+1}}{n\pi} \right] \\ -K_n \frac{2}{L} \cdot \frac{\frac{-1}{m\pi/L}(-1)^m \sinh\left(\frac{n\pi L}{t_{ox,u}}\right)}{1+\left(\frac{n}{t_{ox,u}} \times \frac{L}{m}\right)^2} - P_n \frac{2}{L} \cdot \frac{\frac{1}{m\pi/L}\sinh\left(\frac{n\pi L}{t_{ox,u}}\right)}{1+\left(\frac{n}{t_{ox,u}} \times \frac{L}{m}\right)^2} \end{array} \right\}$$

(3.13n)

Finally, analytical expressions for the potential in the channel and BOX region are shown as equation (3.14) and (3.15), respectively.

$$\varphi_{ch}(x,y,z) = \varphi_{ch,1}(x) + \varphi_{ch,2}(x,y) + \varphi_{ch,3}(x,y,z)$$

$$= \left[-\frac{qN_{ch}}{2\varepsilon_{ch}} x^2 + Ax + B \right] + \sum_{n=1}^{\infty} \left\{ \left[B_n \sinh\left(\frac{n\pi}{H_{eff}} y\right) + E_n \sinh\left(\frac{n\pi}{H_{eff}}(L-y)\right) \right] \cdot \sin\left(\frac{n\pi}{H_{eff}} x\right) \right\}$$

$$+ \sum_{n=1}^{\infty}\sum_{m=1}^{\infty} \left[B_{n,m} \sinh\left(\gamma_{n,m} \cdot z\right) + E_{n,m} \sinh\left(\gamma_{n,m} \cdot (W_{eff} - z)\right) \right] \times$$

$$\sinh\left(\frac{n\pi}{H_{eff}} x\right) \cdot \sin\left(\frac{m\pi}{L} y\right) + \sum_{i=1}^{\infty}\sum_{m=1}^{\infty} H_{i,m} \sinh\left(\lambda_{i,m}(H_{eff} - x)\right) \cdot \sin\left(\frac{i\pi}{W_{eff}} z\right) \cdot \sin\left(\frac{m\pi}{L} y\right)$$

(3.14)

$$\varphi_{box}(x,y,z) = \varphi_{box,1}(x) + \varphi_{box,2}(x,y) + \varphi_{box,3}(x,y,z)$$

$$
=\left[\frac{\varepsilon_{ch}}{\varepsilon t_{ox}}A(x+t_{ox,u})+(V_{gu}-V_{fb})\right]+\sum_{n=1}^{\infty}\left\{\left[K_n \sinh\left(\frac{n\pi n\pi}{t_{ox,u}}y\right)+P_n \sinh\left(\frac{}{ox,u}(L-y)\right)\right]\cdot\sin\left(\frac{n\pi(x+t_{ox,u})}{ox,u}\right)\right\}
$$

$$
+\sum_{n=1}^{\infty}\sum_{m=1}^{\infty}\left[K_{n,m}\sinh\left(\Gamma_{n,m}\cdot z\right)+P_{n,m}\sinh\left(\Gamma_{n,m}\cdot(W_{eff}-z)\right)\right]\times
$$

$$
\sinh\left(\frac{n\pi(x+t_{ox,u})}{t_{ox,u}}\right)\cdot\sin\left(\frac{m\pi}{L}y\right)+\sum_{i=1}^{\infty}\sum_{m=1}^{\infty}H_{i,m}\frac{\sinh(\lambda_{i,m}\cdot H_{eff})}{\sinh(\lambda_{i,m}\cdot t_{ox,u})}\sinh\left(\lambda_{i,m}\cdot(x+t_{ox,u})\right)\cdot\sin\left(\frac{i\pi}{W_{eff}}z\right)\cdot\sin\left(\frac{m\pi}{L}y\right)
$$

(3.15)

Based on the potential solution, the subthreshold current can be calculated by [22]

$$
I_{DS}=q\mu\frac{n_i^2}{N_{ch}}\frac{kT}{q}\left[1-e^{-(qV_{DS}/kT)}\right]\cdot\frac{1}{L}\cdot\int_0^{H_{fin}}\int_0^{W_{fin}}e^{q\phi_{ch}(x,y_{\min},z)/kT}dzdx \qquad (3.16)
$$

where $\phi_{ch}(x,y_{\min},z)$ is the minimum potential along the channel direction.

3.3 Model Verification

We verify our potential solution with the TCAD *Silvaco ATLAS* [28]. The schematic device structure is indicated in Fig. 3.1. In order to demonstrate the improvement of our model, we also compare our model with the model in [22] (dashed lines) which adopted a simpler boundary condition at the channel/BOX interface. Fig. 3.2 (a), (b), and (c) show the potential distribution in an *undoped* tri-gate SOI MOSFET. The discrepancy between the dashed lines and TCAD is significant because the homogeneous dielectric approximation in the BOX region does not consider the fringing field induced by the drain and source through the BOX. This longitudinal coupling causes an increase in channel potential near the substrate.

In other words, the channel potential shift induced by drain bias is similar to a positive substrate bias. It results in threshold voltage lowering and subthreshold swing degradation. As indicated in Fig. 3.3, as channel length scaled down below 20nm, the model without considering drain to source coupling fails to match the TCAD result even for a low drain bias condition.

Fig. 3.4 shows the potential distribution along the fin height direction for tri-gate devices with various BOX thicknesses. It is noted that our model shows good agreement with the TCAD simulation while the model in [22] (dashed line) fails to predict the potential profiles for the thin-BOX cases. Fig. 3.5 (a) shows the potential distribution along the fin height direction for long channel devices with various fin thicknesses. It is noted that the discrepancy of the model in [22] with TCAD increases with decreasing fin thickness. The potential barrier rise at the BOX/channel interface leads to a negligible impact on subthreshold current for devices with larger fin width. However, the same potential barrier perturbation introduces significant errors in the small dimension device. As indicated in Fig. 3.5 (b), it is difficult for the dashed lines to agree with TCAD results even for the devices with good electrostatic integrity.

Fig. 3.6 (a) and (b) show the potential distribution along the fin height direction and the subthreshold current characteristics, respectively. It can be seen that the model in [22] fails to capture the impact of substrate bias on subthreshold characteristics,

while our new model shows satisfactory accuracy. The error of the model in [22] increases with the thickness of the BOX. Fig. 3.7 (a) and (b) show the potential and subthreshold characteristics for SOI tri-gate with a 30-nm thick BOX. Apparently, the potential distribution along the fin height direction for the model in [22] cannot faithfully respond to the substrate bias, and the subthreshold current shows wrong substrate-bias sensitivity.

3.4 Summary

We have derived a subthreshold model for tri-gate SOI MOSFETs considering the fringing field induced by the drain and the source through the BOX. Our model is better than the model in [22] because the potential solution in the BOX region is exactly solved. Based on the BOX potential, the boundary conditions of the channel region are improved. With this improvement, our model has successfully predicted the SCEs and the substrate sensitivity for tri-gate SOI devices with various BOX thicknesses. This model enhancement is especially important for the multi-V_{th} scheme. Based on our new model, the device design of multiple-threshold voltage in tri-gate SOI devices will be investigated in the next chapter.

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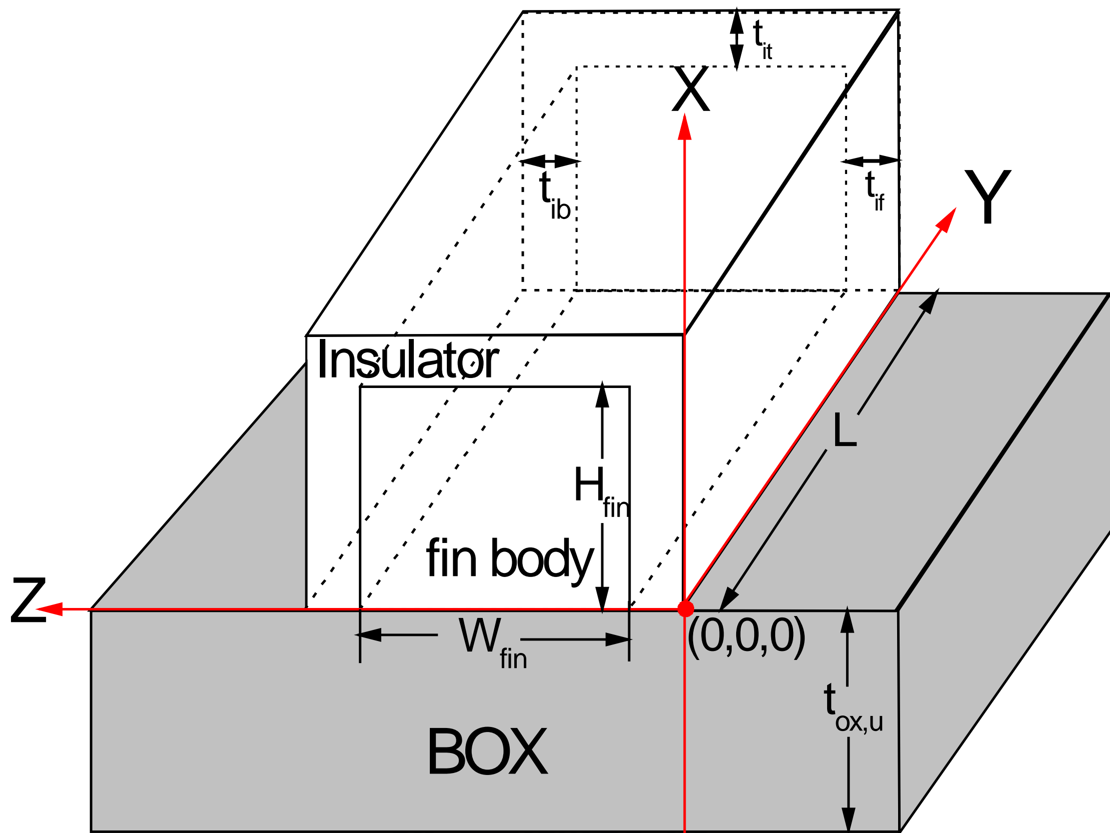

Fig. 3.1 Schematic tri-gate device structure and the coordinate definition of our potential model.

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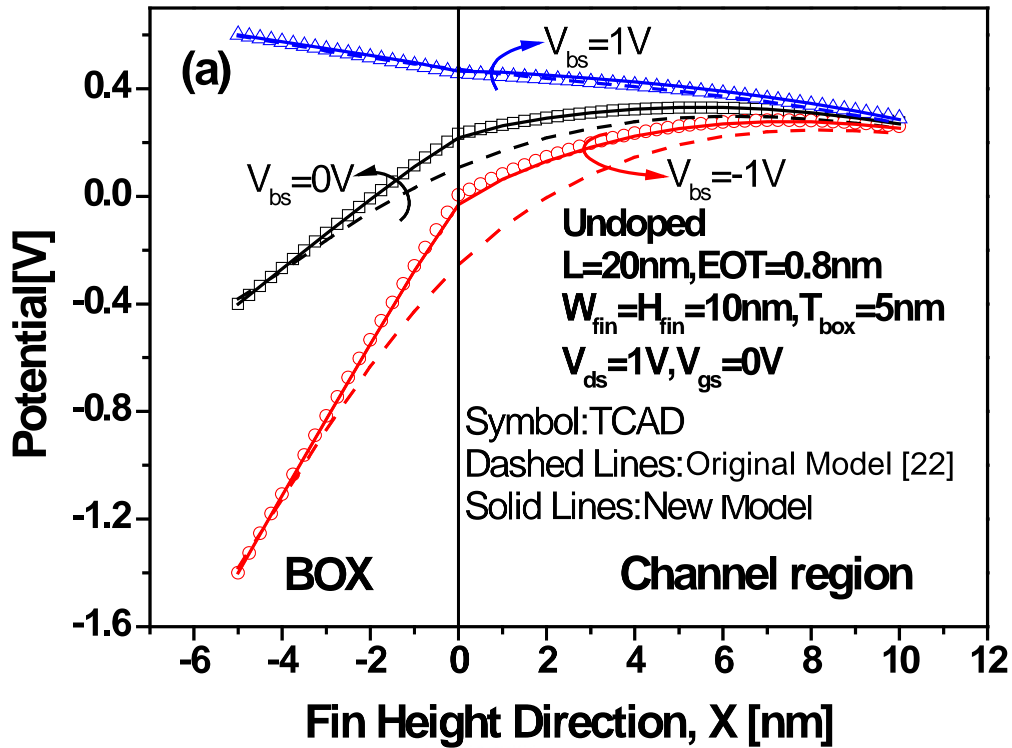


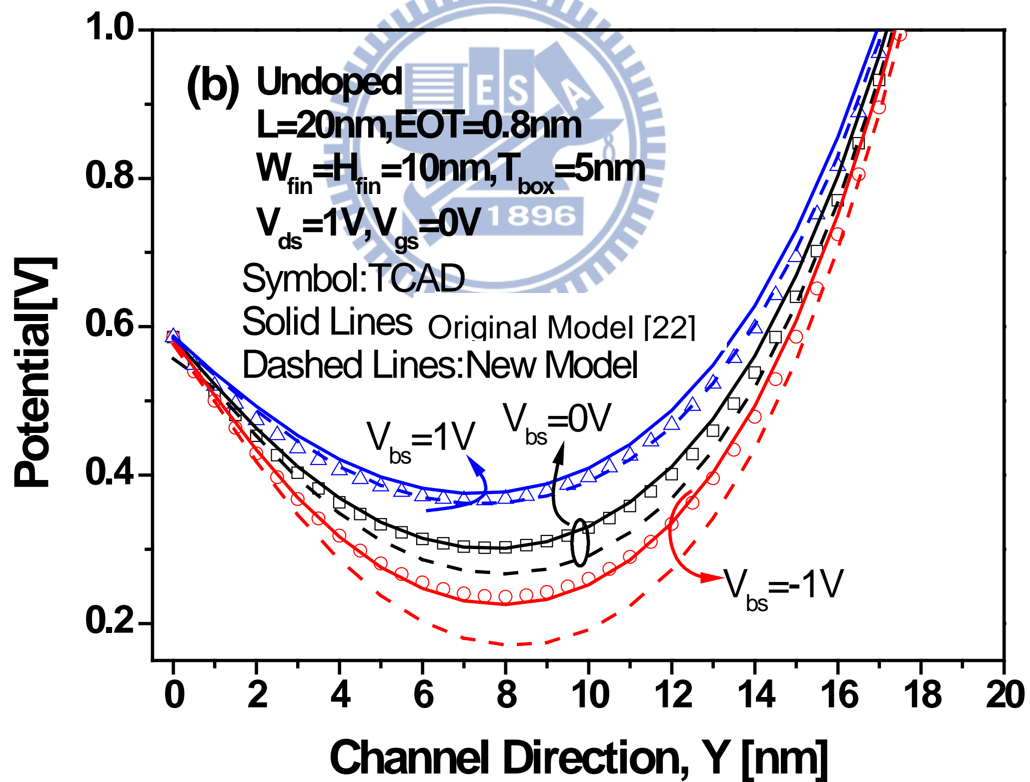


Fig. 3.2 Potential distribution of the *undoped* tri-gate device at (a)Y=L/2,Z=W_{fin}/2 ,(b)X=H_{fin}/2,Z=W_{fin}/2.

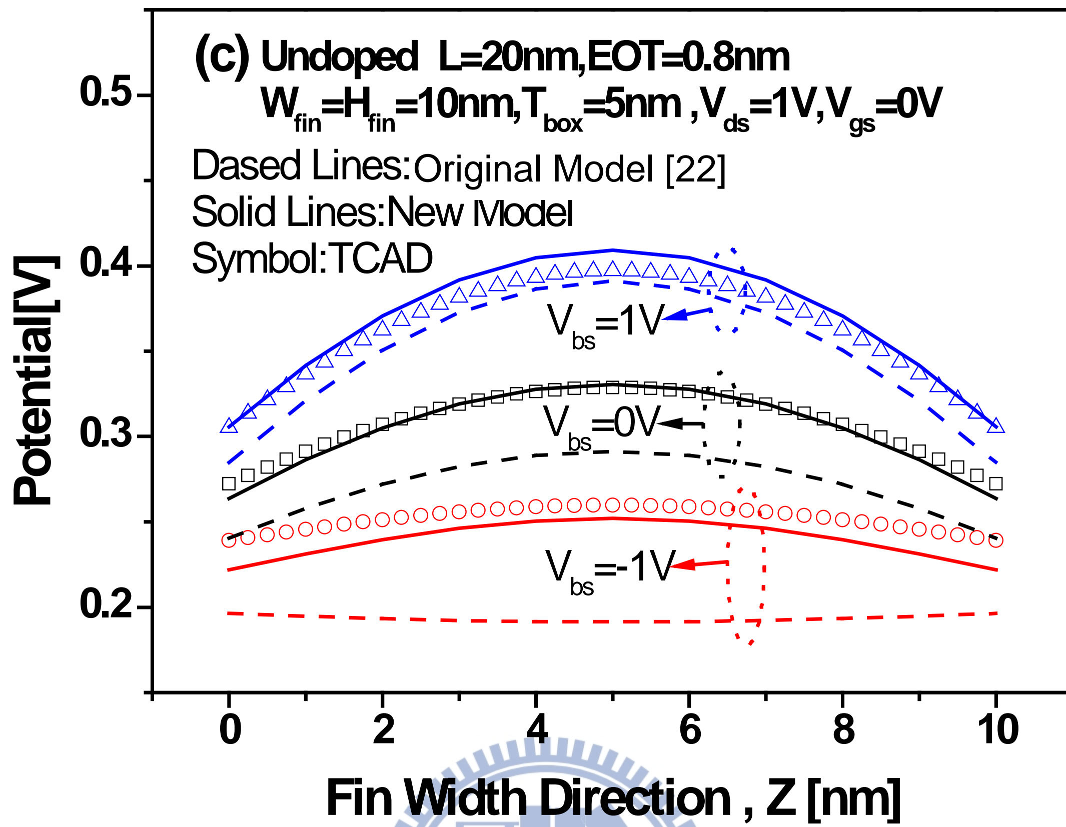


Fig. 3.2 (c) Potential distribution of the *undoped* tri-gate device at Y=L/2,X=H_{fin}/2.

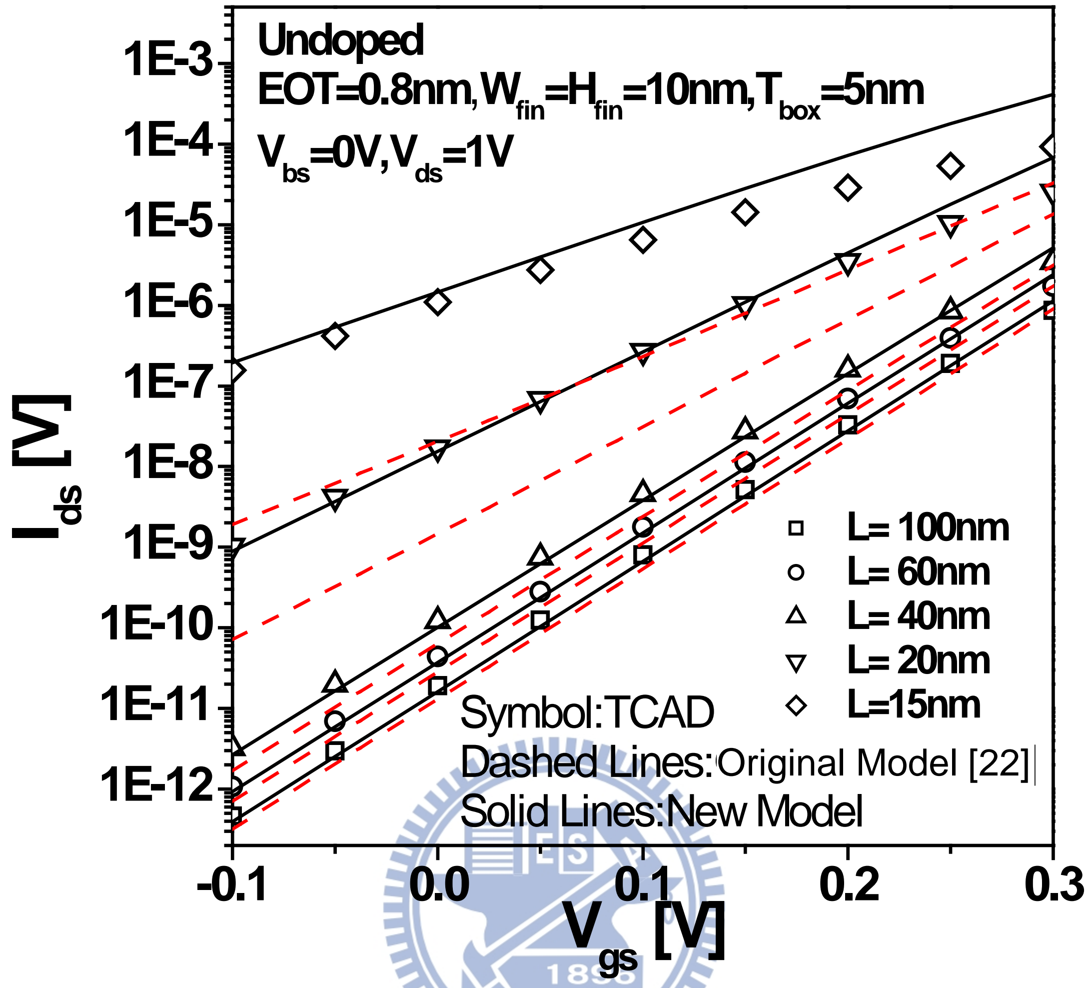


Fig. 3.3 Subthreshold characteristics of undoped tri-gate devices with various channel lengths.

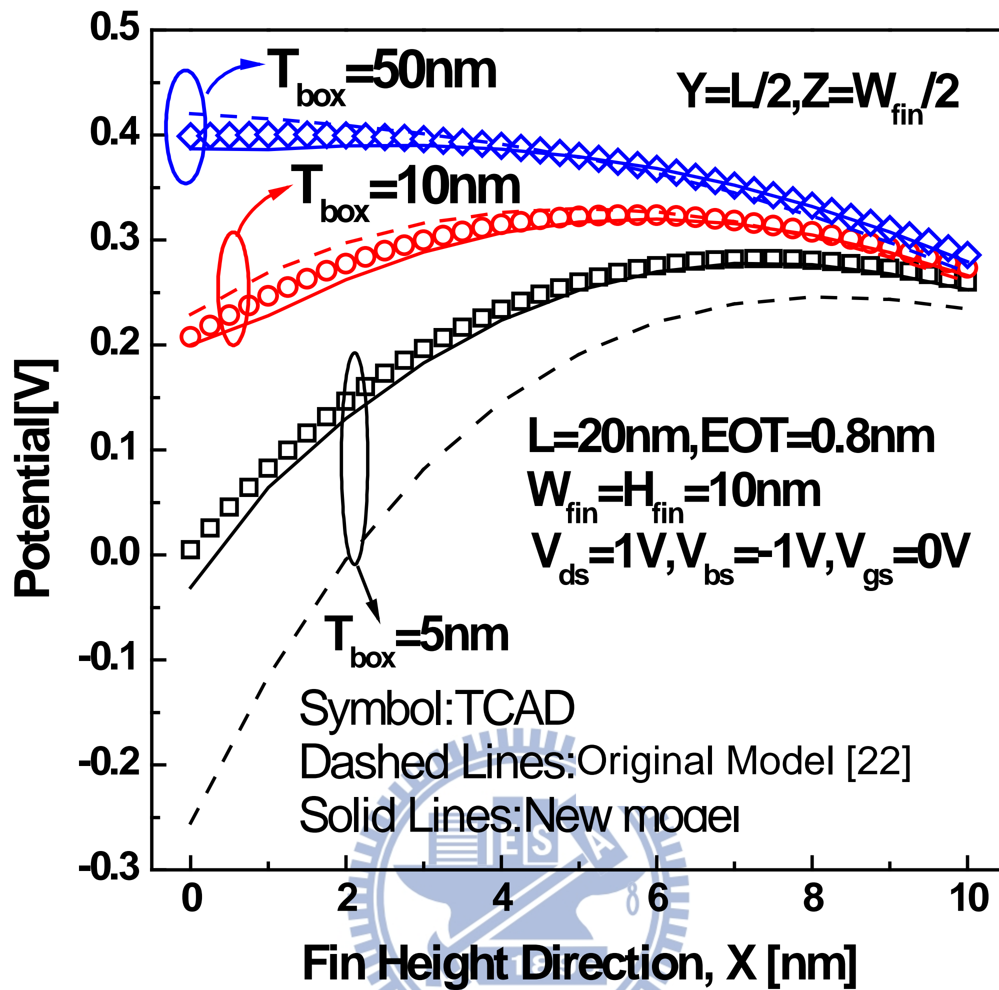


Fig. 3.4 Potential distribution along the fin height direction for tri-gate devices with various BOX thicknesses.

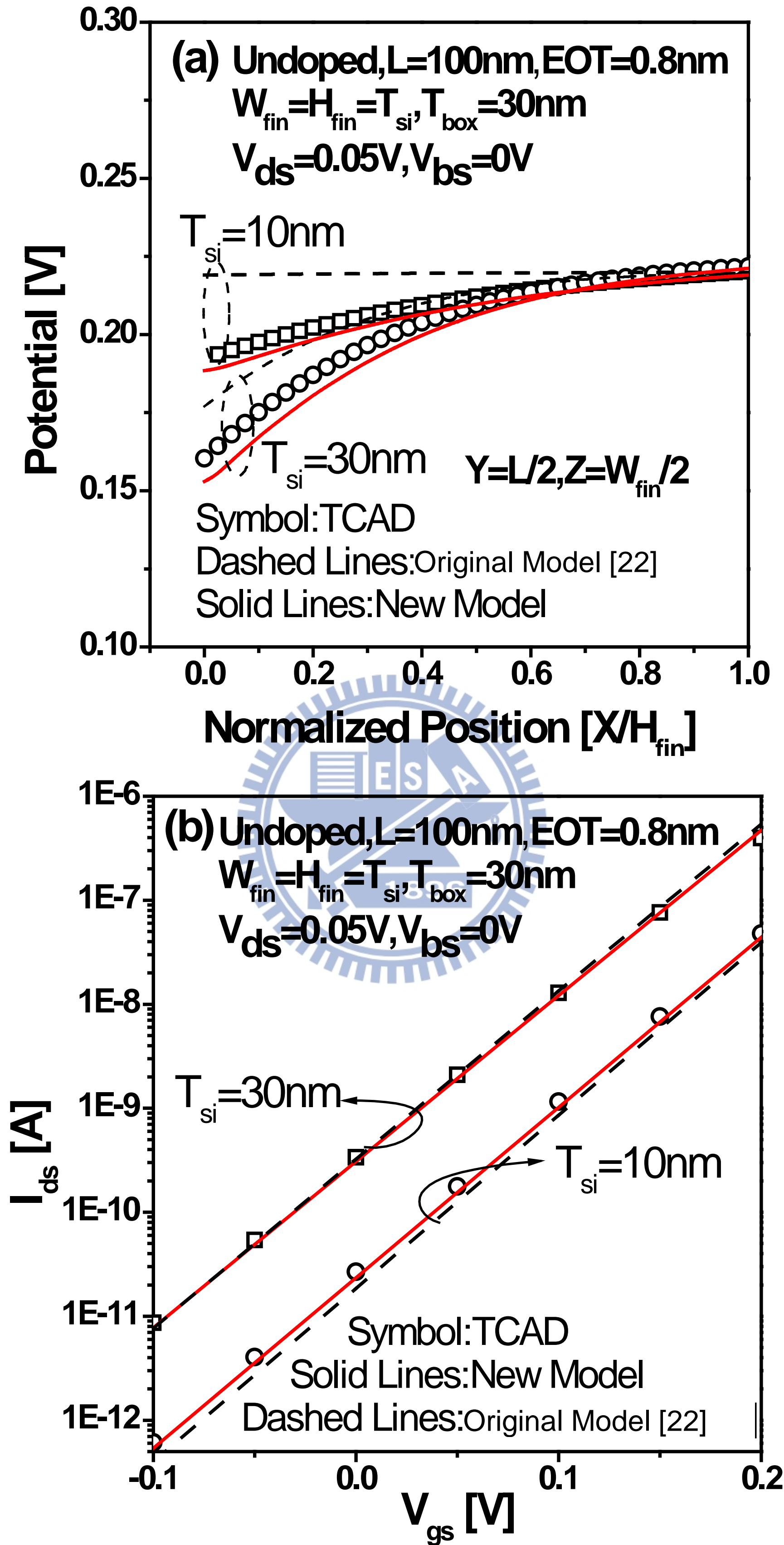


Fig. 3.5 (a)Potential distribution along the fin height direction for tri-gate devices with various fin thicknesses and (b)Subthreshold I_{ds}-V_{gs} characteristics for tri-gate devices with various fin thicknesses.

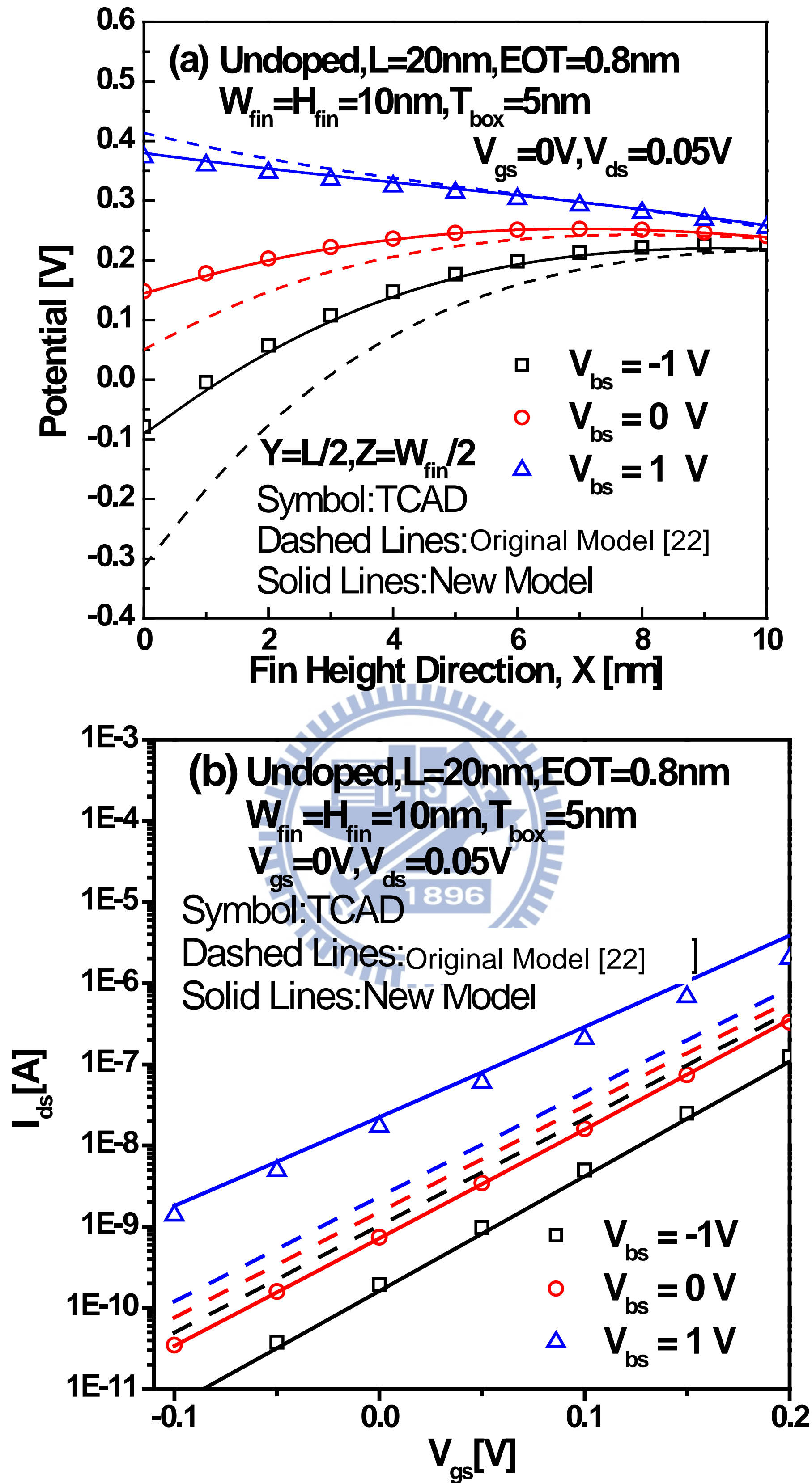


Fig. 3.6 (a) Potential distribution along the fin height direction for tri-gate devices with 5nm T_{box} under various substrate bias conditions, and (b) Subthreshold I_{ds}-V_{gs} characteristics for tri-gate devices under various substrate bias conditions.

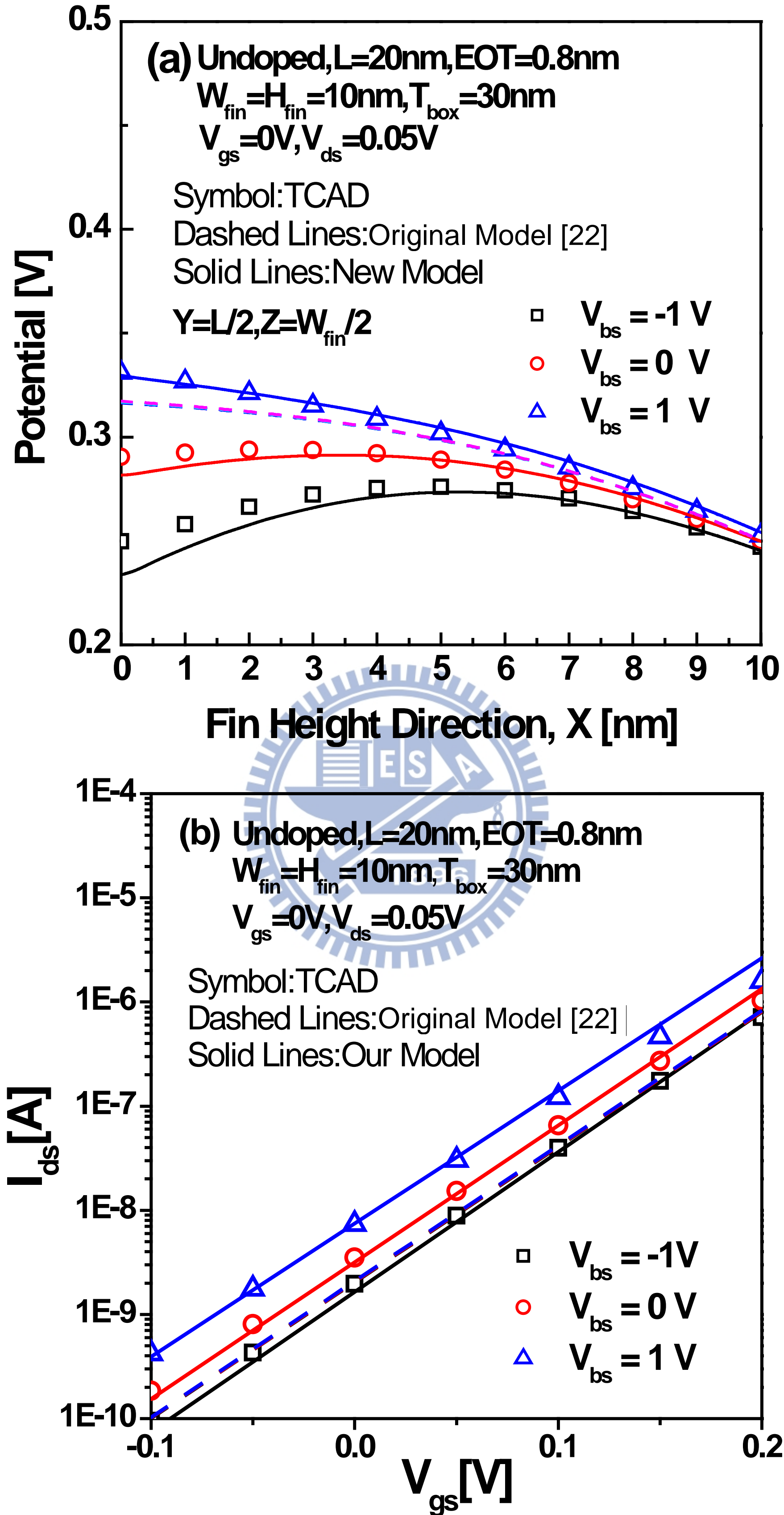


Fig. 3.7 (a)Potential distribution along the fin height direction for tri-gate devices with 30nm T_{box} under various substrate bias conditions ,and (b) Subthreshold I_{ds}-V_{gs} characteristics for tri-gate devices under various substrate bias conditions.

Chapter 4
Theoretical Investigation of Multi-Threshold Device Design for Tri-Gate SOI MOSFETs with Thin BOX

4.1 Introduction

To enable power/performance optimization in the tri-gate SOI MOSFETs, thin BOX structure has been proposed [24] to achieve multiple threshold voltage (V_{th}). Whether different tri-gate device designs will impact the efficiency in V_{th} modulation is an important question. In this chapter, we investigate the multi-V_{th} device design of tri-gate SOI MOSFETs by using the derived analytical model in chapter 3. Based on the contour of equal subthreshold swing (SS), the impacts of device design on the threshold voltage modulation through substrate bias and channel doping are investigated in section 4.2 and section 4.3, respectively.

In this work, the V_{th} is determined by the constant current method: $I_0=(W_{total}/L)*100nA$ with $W_{total}=2*H_{fin}+W_{fin}$. The body factor γ is used to assess the substrate sensitivity or body effect in the tri-gate devices. It is defined as the ratio of the V_{th} shift to the change in substrate bias. The fin aspect ratio (AR) is defined as the ratio of fin height (H_{fin}) to fin width (W_{fin}).

4.2 Multi-V_{th} by Substrate Bias

After the potential profiles are calculated by our analytical model in chapter 3, the subthreshlold swing (SS) can be derived and the equi-SS contour map on the W_{fin}-H_{fin} plane can be efficiently constructed. To make a fair comparison among different fin geometries, the constant SS criterion is used. Fig. 4.1 (a) and (b) show an equi-SS contour map for undoped and doped ($3x10^{18}cm^{-3}$) devices under low/high drain bias. It is noted that the doped device shows a wider SS design space than that of the undoped one. Due to the suppressed SCE in the doped device, the relaxed SS design space can be expected for the doped device.

Devices A, B, C and D in Fig. 4.1 have equi-SS and identical fin aspect ratio (AR) of 0.5. Fig. 4.2 shows the body factor dependence on AR under various channel doping. It can be seen that the undoped device has larger body factor than that of the doped device. Since the channel doping degrades the body factor for a given SS, the doped device needs a smaller AR to achieve the required body factor (γ).

Fig. 4.3 shows the electron distribution for device A, B, C and D. Under the low drain bias condition, in device A, the subthreshold carrier forms in the middle of the undoped channel. On the contrary, the surface inversion occurs in the doped device B. However, when the high drain bias is applied, the subthreshold carrier distributes closer to the substrate in either the undoped device C or the doped device D.

Fig. 4.4 shows the equi-SS contour map for tri-gate devices with L=20nm and L=40nm under the high drain bias condition. Fig. 4.5 shows the body factor versus AR for tri-gate devices with L=20nm (left figure) and L=40nm (right figure). In the left side of Fig. 4.5, the dashed line indicates the body factor of the tri-gate devices with a 5nm thick BOX. Since the substrate sensitivity degrades with the downscaling of channel length, the shorter channel device needs a smaller AR to maintain a given body factor. As indicated by the dashed line in Fig. 4.5, the shorter device (L=20nm) with 5nm thick BOX has comparable body factor with the longer channel device (L=40nm). Fig. 4.6 shows the contour map of SS=80mV/dec and its corresponding body factor versus aspect ratio for EOT=0.8nm and 1.5nm. The body factor decreases as EOT scales down because smaller EOT enhances the capacitive coupling between the gate and the channel.

4.3 Multi-V_{th} by Channel Doping

Recently, several works [29]-[30] have reported that the threshold voltage can be modulated by the fin doping of the tri-gate devices. In [29] and [30], the tri-gate devices were fabricated on thick SOI substrate (more than 40nm) without the capability of substrate-bias modulated V_{th}. On the other hand, reference [24] has proposed the multiple V_{th} control by thin BOX (20nm) in 10nm-diameter tri-gate devices. Although these two multiple V_{th} approaches seem to be applicable for the

tri-gate devices, whether there is any trade-offs between these two approaches has still not been clear and merits investigation.

Since channel doping modulates both SS and V_{th}, we use the constant SS criterion to ensure the same SCE control among devices with different channel doping. Fig. 4.7 shows the contour map of SS=70mV/dec for devices with T_{box}=10nm and various channel doping. It can be seen that the heavily doped device has more relaxed design space. Fig. 4.8 shows the V_{th} dependence on AR with various fin doping under the SS=70mV/dec criterion. As indicated in the Fig. 4.9, the tri-gate device with lower AR has smaller V_{th} shift as the channel doping varies from $1x10^{15}cm^{-3}$ to $5x10^{18}cm^{-3}$. In other words, the efficiency of V_{th} modulation by doping increases with AR. This is because as the tri-gate device has low AR and thin BOX, the channel potential is strongly controlled by the capacitive coupling between the substrate and the channel.

Fig. 4.10 shows the SS contour map of the tri-gate devices with 30nm T_{box} and various fin doping. The corresponding V_{th} dependence on AR is indicated in Fig. 4.11. It can be seen that the impact of AR on the V_{th} modulation efficiency by doping becomes weaker. Fig. 4.12 shows that the V_{th} dependence on channel doping for both the low AR and high AR devices is larger than that of the thin-BOX cases (Fig. 4.9). This is because the thicker BOX weakens the capacitive coupling between the substrate and the channel, and enhances the impact of doping on channel potential.

4.4 Summary

Using the analytical model derived in chapter 3, we investigate multi-V_{th} device design in tri-gate SOI MOSFETs by exploring wide range of device design space. To enable the power/performance optimization, multiple V_{th} level can be achieved by substrate bias or channel doping. Based on constant SS criterion, we find that the tri-gate device with low AR and thin BOX is a promising structure to enable the V_{th} modulation by substrate bias. In addition, channel doping can modulate V_{th} for the tri-gate device with high AR.

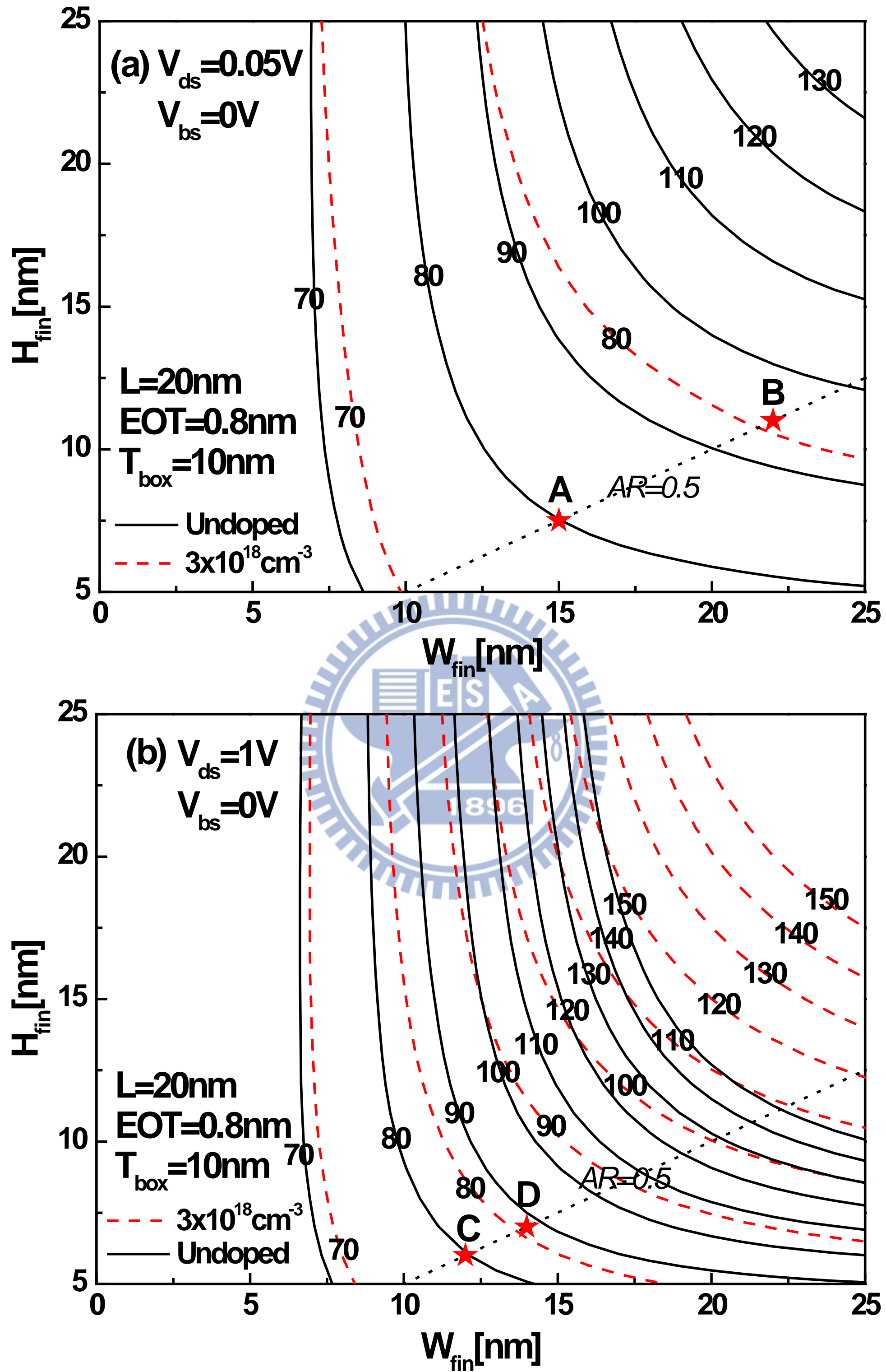


Fig. 4.1 Calculated contour of SS on a W_{fin}-H_{fin} plane under (a)low drain bias and (b)high drain bias. The dashed lines indicate the SS contour map of the doped devices while the solid lines indicate that of the undoped devices.

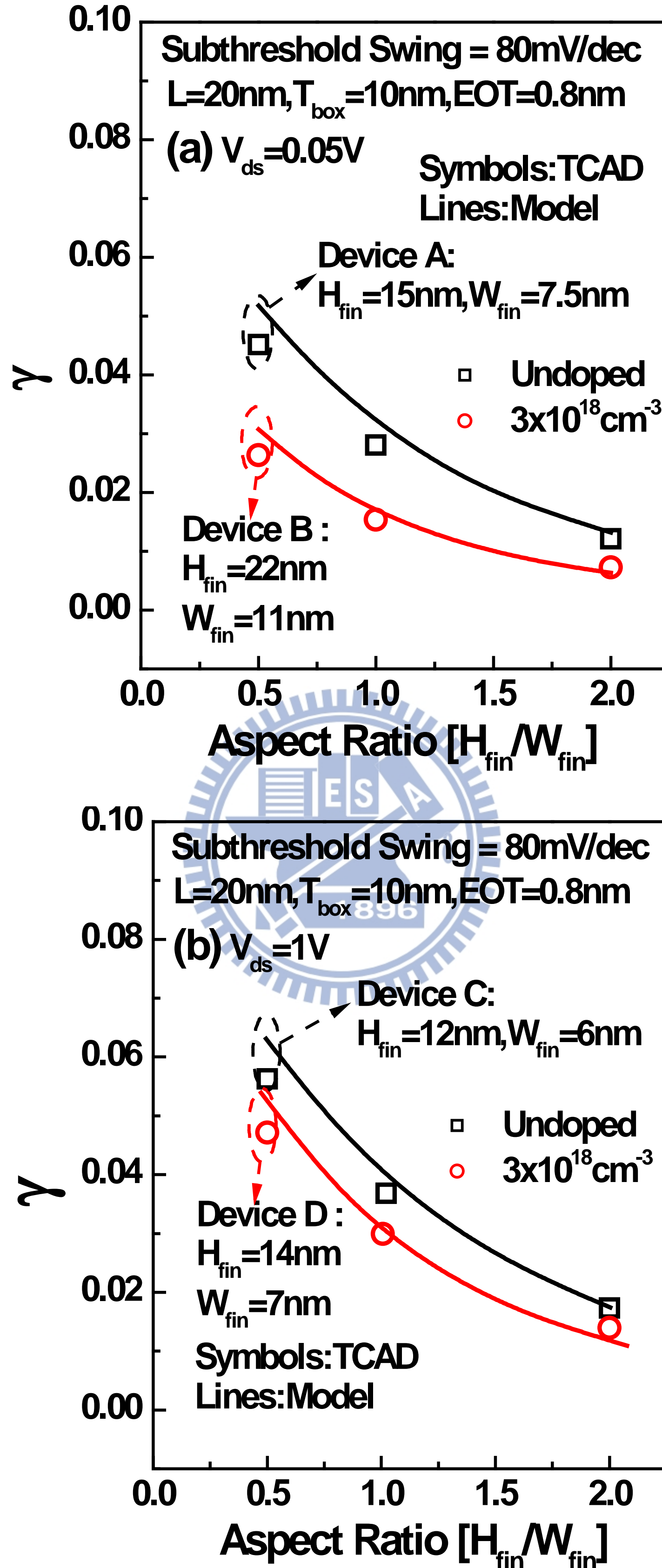


Fig. 4.2 Body factor (γ) dependence on fin aspect ratio (AR) under the (a) low drain bias and (b) high drain bias. It is noted that γ is derived by threshold voltage at V_{bs}=0V and V_{bs}=-1V.

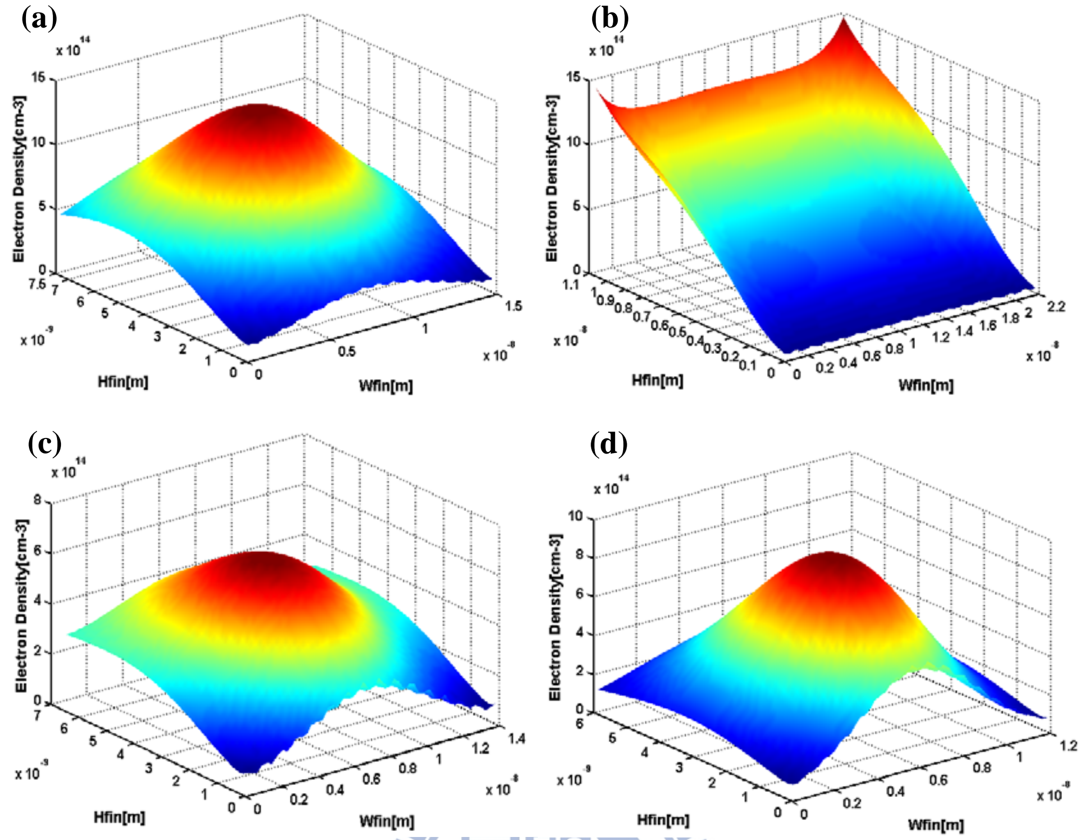


Fig. 4.3 Calculated subthreshold carrier distribution on the cross section at the middle of the channel for (a) device A , (b)device B, (c) device C and (d)device D. The origin of the axis "H_{fin}" starts from BOX/channel interface. In addition, the origin of axis "W_{fin}" starts from gate oxide/channel interface. It is noted that the carrier profiles are all extracted at V_{gs}=V_{th}-0.1V and V_{bs}=0V.

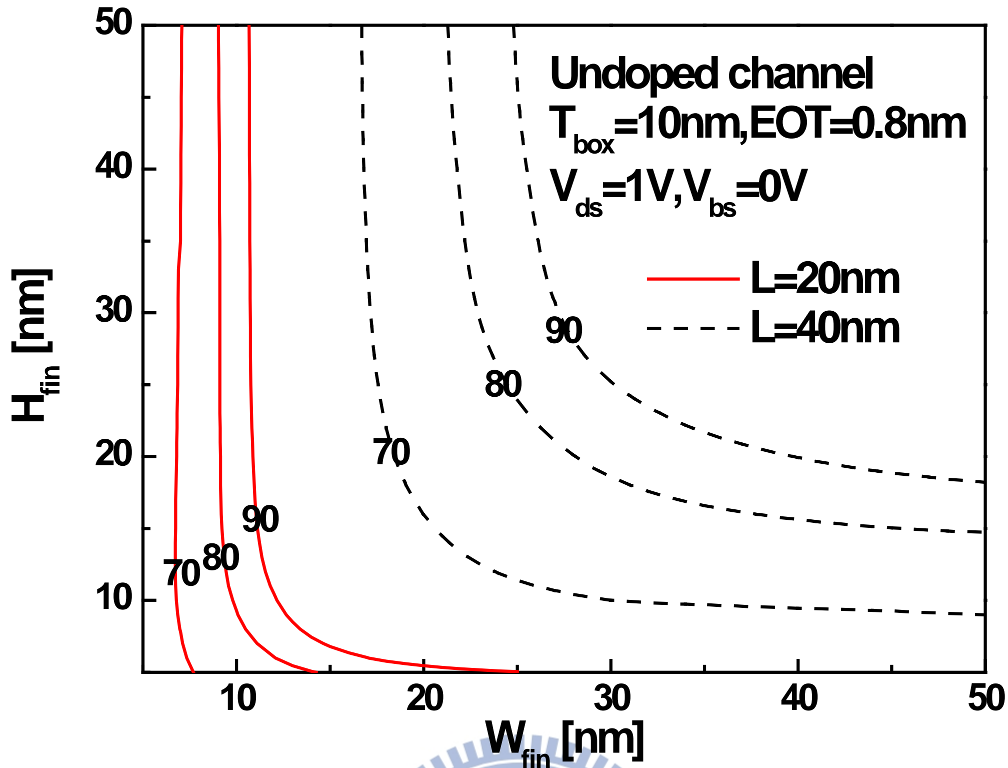


Fig. 4.4 Calculated contour of SS on a W_{fin}-H_{fin} plane for the tri-gate devices with various channel lengths.

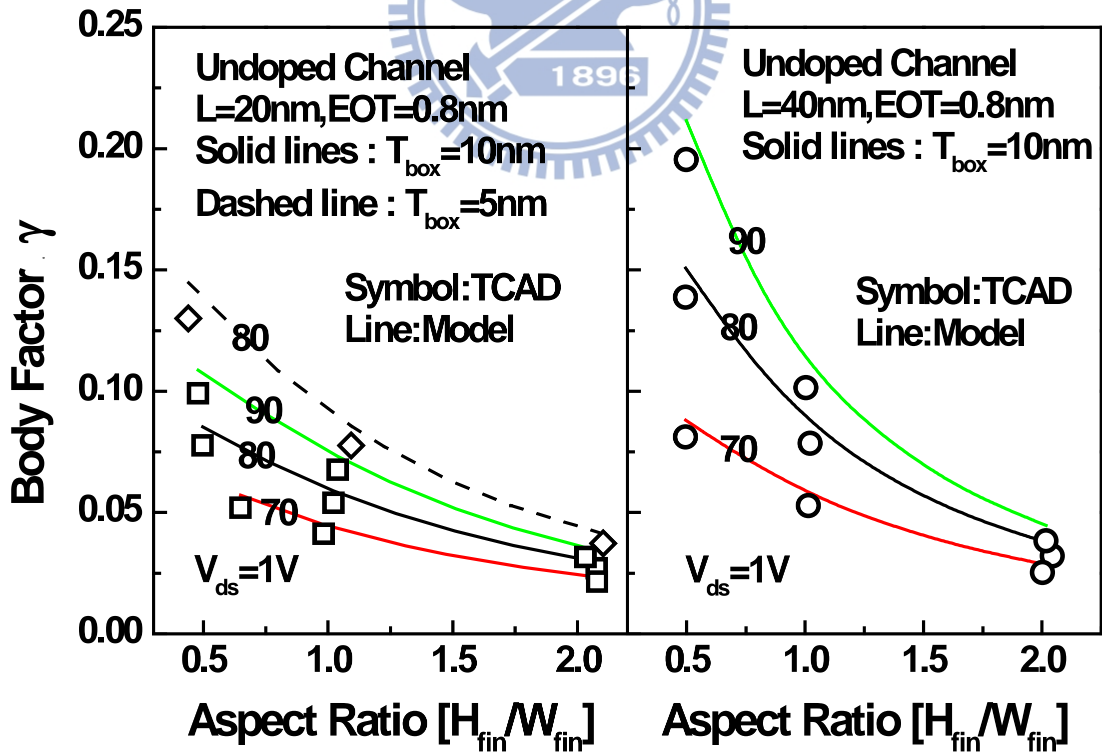


Fig. 4.5 Body factor dependence on fin aspect ratio for the tri-gate devices with L=20nm in the left figure and L=40nm in the right figure. It is noted that body factor is derived by threshold voltage at V_{bs}=1V and V_{bs}=-1V.

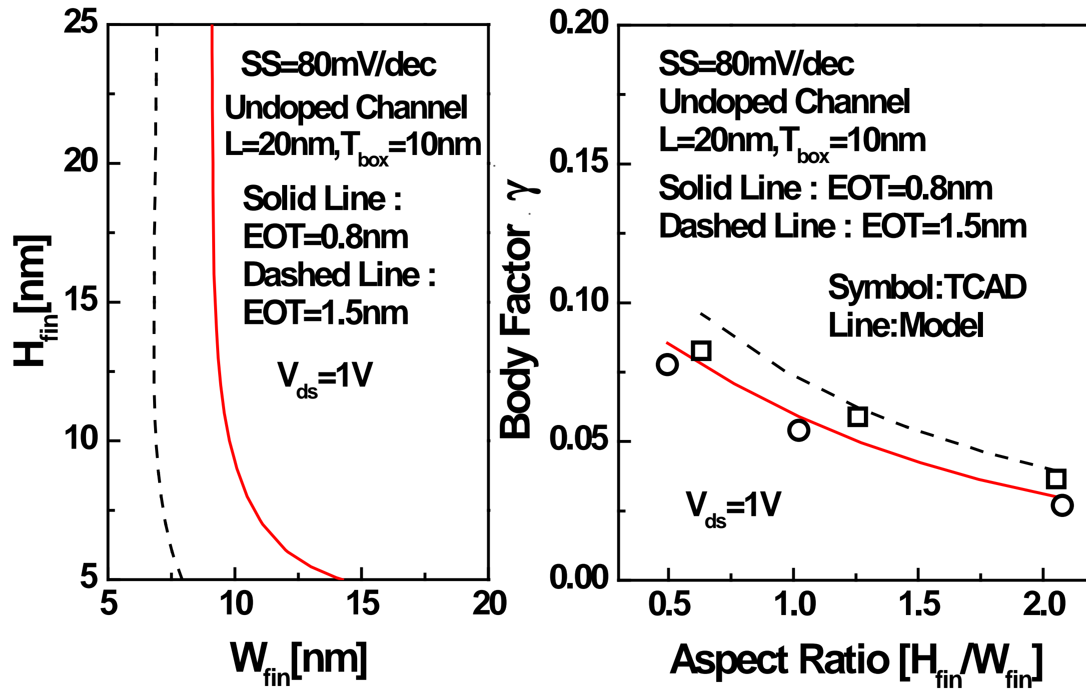
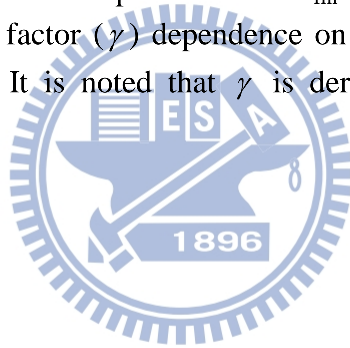


Fig. 4.6 (Left) Calculated contour map of SS on a W_{fin}-H_{fin} plane for the devices with various EOT. (Right) Body factor (γ) dependence on fin aspect ratio (AR) for the devices with various EOT. It is noted that γ is derived by threshold voltage at V_{bs}=1V and V_{bs}=-1V.



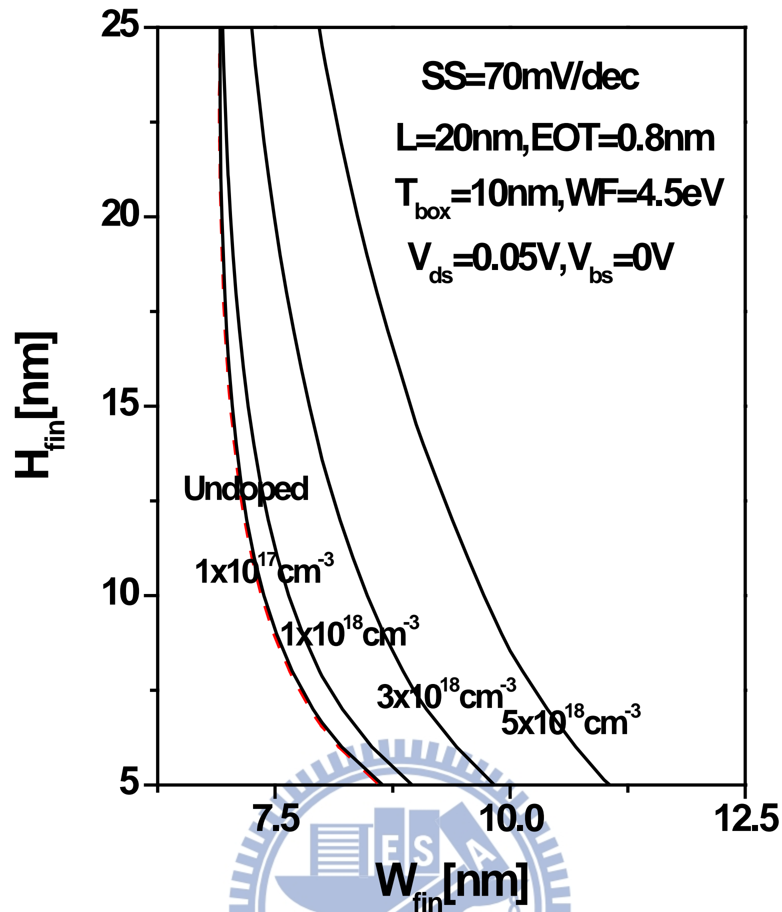


Fig. 4.7 Contour map of SS =70mV/dec for devices with various channel doping. The equi-SS contour for the undoped devices is indicated by the dashed curve. The buried oxide thickness (T_{box}) is 10nm.

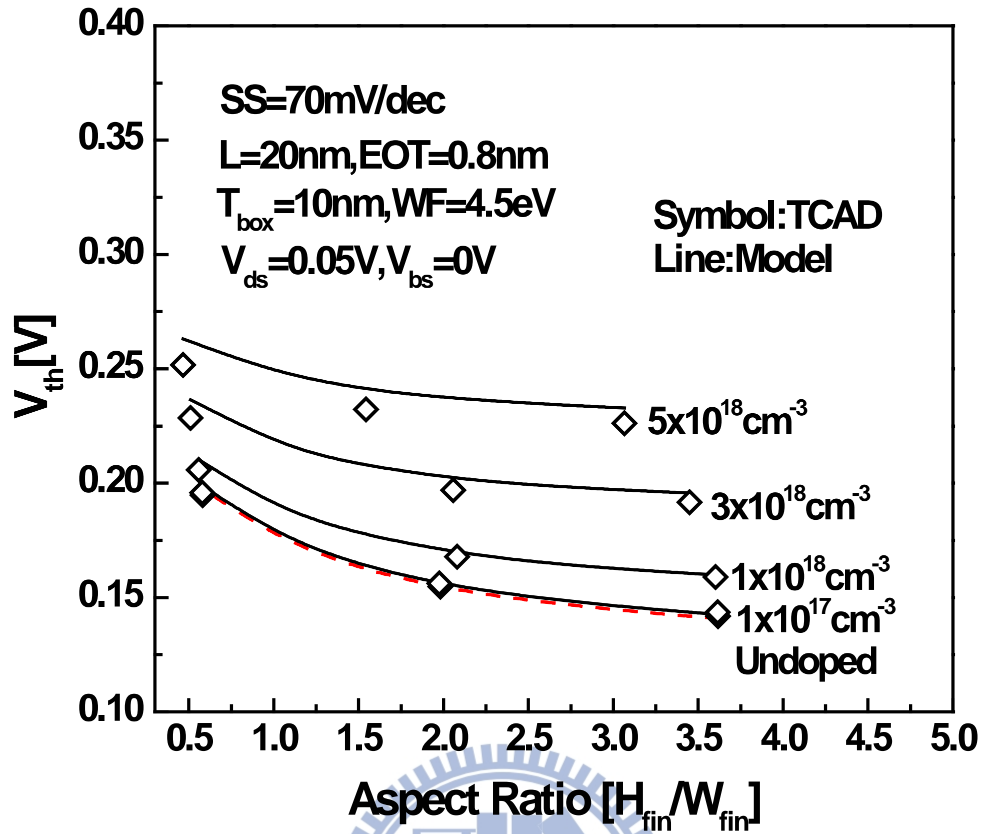


Fig. 4.8 Threshold voltage (V_{th}) versus aspect ratio (AR) for tri-gate devices with various channel doping. The buried oxide thickness (T_{box}) is 10 nm. The undoped case is indicated by the dashed line.

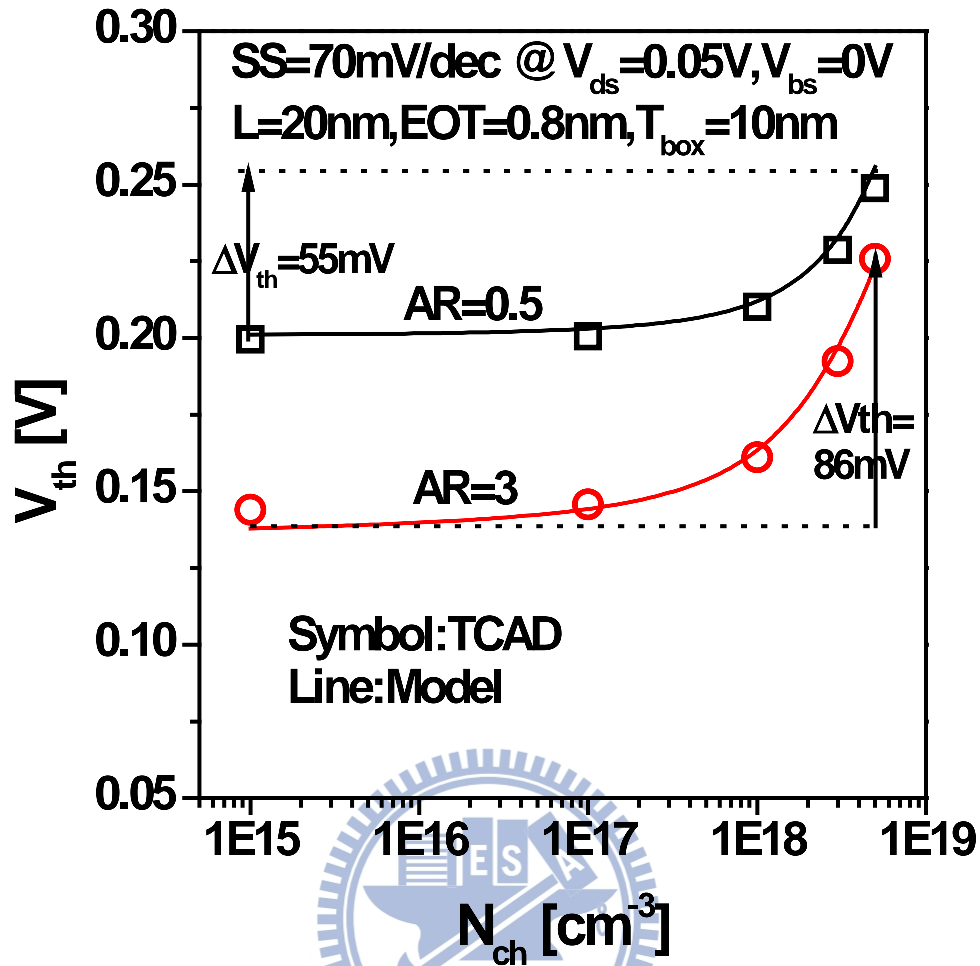


Fig. 4.9 Threshold voltage (V_{th}) versus channel doping (N_{ch}) for devices with AR=0.5 and AR=3. The buried oxide thickness (T_{box}) is **10**nm. The threshold voltage modulation (ΔV_{th}) by channel doping (from $1x10^{15}cm^{-3}$ to $5x10^{18}cm^{-3}$) is around 0.055V and 0.086V in tri-gate devices with AR of 0.5 and 3, respectively

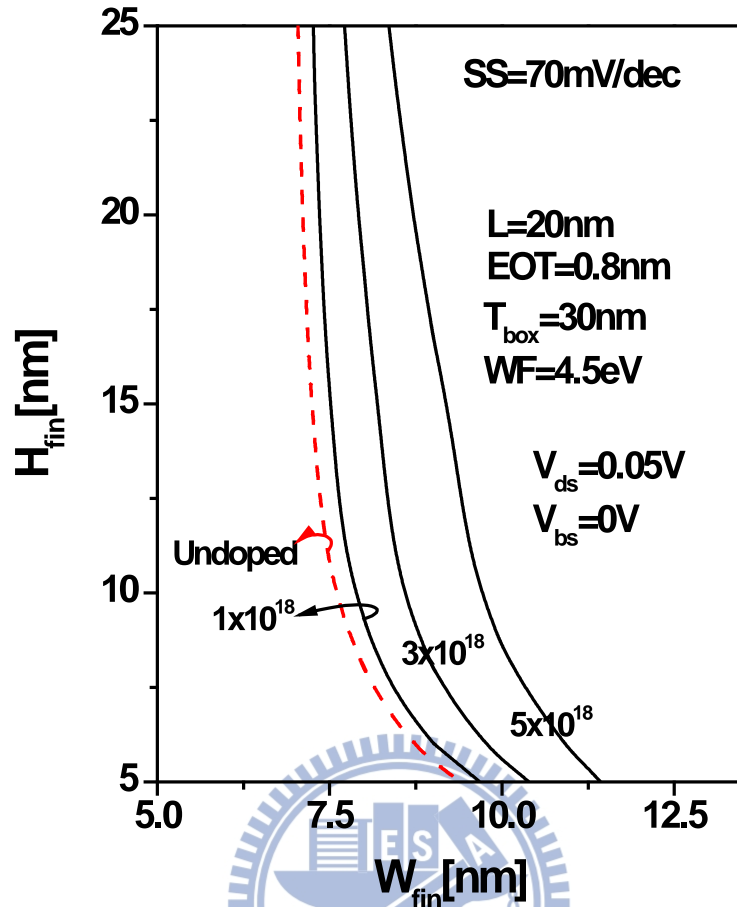


Fig. 4.10 Contour map of SS=70mV/dec for devices with various channel doping. The equi-SS contour for the undoped devices is indicated by the dashed curve. The buried oxide thickness (T_{box}) is **30**nm.

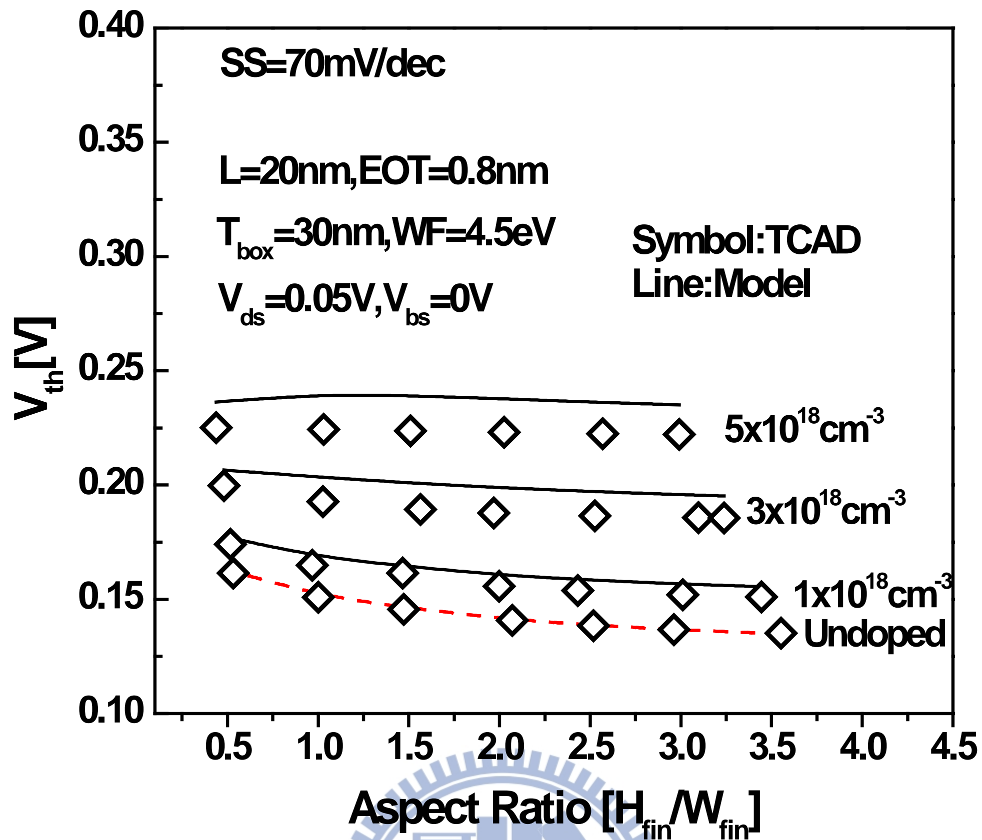


Fig. 4.11 Threshold voltage (V_{th}) versus aspect ratio (AR) for devices with various channel doping. The buried oxide thickness (T_{box}) is **30**nm. The undoped case is indicated by the dashed line.

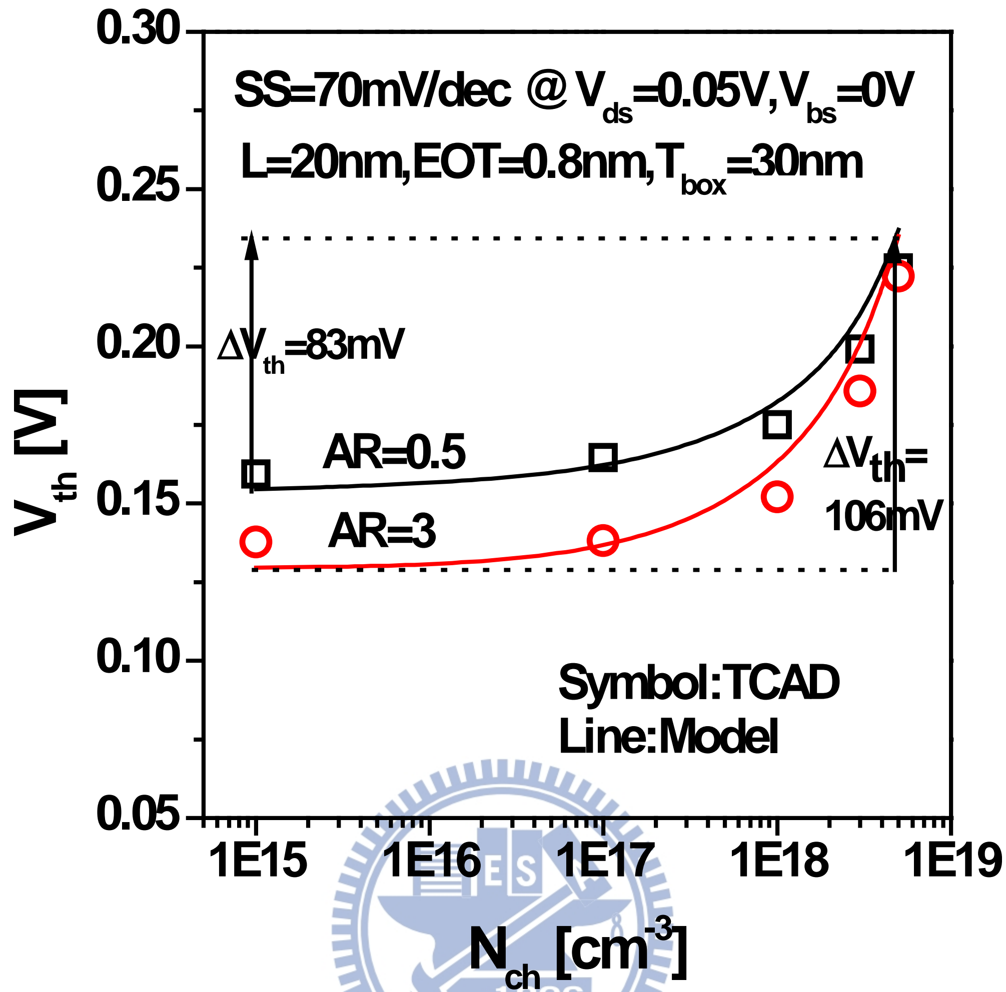


Fig. 4.12 Threshold voltage (V_{th}) versus channel doping (N_{ch}) for tri-gate devices with AR=0.5 and AR=3. The buried oxide thickness (T_{box}) is **30**nm. The threshold voltage modulation (ΔV_{th}) by channel doping (from $1x10^{15}cm^{-3}$ to $5x10^{18}cm^{-3}$) is around 0.083V and 0.106V in tri-gate devices with AR of 0.5 and 3, respectively.

Chapter 5
Conclusions and Future Work

In this thesis, we have investigated the body-effect induced variability in Bulk tri-gate MOSFETs [21]. Through 3-D atomistic simulation, the random dopant fluctuations (RDF) in the Punch-Through-Stopper (PTS) region of Bulk tri-gate devices are examined. Our study indicates that to achieve an efficient threshold-voltage modulation through substrate bias, the high-doping PTS region may introduce excess variation in Bulk tri-gate devices. It should be noted that the study in chapter 2 only considers the RDF in substrate and PTS regions for SOI tri-gate and Bulk tri-gate, respectively. However, in addition to RDF, other variation sources such as fin line edge roughness (fin LER) [10]-[11] and work function variation (WFV) [31]-[37] may also affect the threshold voltage variation for tri-gate devices. In addition, ultra-thin BOX may also introduce excess variation for SOI tri-gate devices. Therefore, a more comprehensive investigation considering all these effects can be conducted in the future.

Because of the PTS-induced variability in bulk tri-gate, SOI tri-gate with substrate bias seems to be a better device structure to achieve multiple V_{th}. In order to facilitate multi-V_{th} device design, we have derived a subthreshold model for tri-gate SOI MOSFETs considering the fringing field induced by the drain and source

electrodes through the buried oxide (BOX). Our model is more accurate than [22] because the potential solution in the BOX region is exactly solved. In addition, the boundary conditions of the channel region are improved. With this improvement, our model can accurately predict the short channel effect (SCEs) and the substrate sensitivity for tri-gate SOI device with various BOX thicknesses.

Using the enhanced subthreshold model, we have investigated multi-V_{th} device design in tri-gate SOI MOSFETs with wide range device design space. To enable the power/performance optimization, multi-V_{th} can be achieved by substrate bias or channel doping. Under constant subthreshold swing criterion, our study indicates that the tri-gate SOI device with low fin aspect ratio and thin BOX is a promising structure to enable the V_{th} modulation by substrate bias.

In addition, we have found that channel doping can also be used to modulate V_{th} effectively for tri-gate SOI devices with high aspect ratio (AR). However, the scaled fin width of high-AR devices may result in a significant V_{th} variation due to fin line edge roughness (fin LER). In addition, high channel doping concentration may cause significant random dopant fluctuations. These random variations should also be considered in multi-V_{th} device design.

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