國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

原子層沉積三氧化二鋁介電層於砷化銦鎵金氧半電容之電性與化性的研究

Study on Electrical and Chemical Characteristics of Indium Gallium Arsenide Metal-Oxide-Semiconductor Capacitors with Atomic-Layer-Deposited Al_2O_3 Gate Dielectric

研 究 生：鄒秉翰

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電 子 工 程 學 系　電 子 研 究 所 碩 士 班

碩 士 論 文

A Thesis

Submitted to Department of Electronics Engineering and Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

In Partial Fulfillment of the Requirements

For the Degree of

Master of Science

In Electronics Engineering

April 2013

Hsinchu, Taiwan, Republic of China

中 華 民 國 一 〇 二 年 四 月

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摘要

在此篇論文初，我們主要研究晶向(100)的砷化銦鎵通道層與三氧化二鋁(原子層沉積，ALD)之間的界面。粗劣的界面和氧化層品質會導致高頻率分散、費米能階釘札及高閘極漏電流。為了要改善界面與閘極氧化層間的品質，不同的熱處理作用在電容上，例如：後金屬化退火（PMA）、氮氫混合氣體退火（FGA）、後沉積退火（PDA）。首先，我們先探討電容經過 PMA 的處理與 FGA 處理後的差異。與 PMA 相比，在聚積區的頻率分散可被 FGA 有效地降低。另外，我們利用電導法來萃取界面缺陷電荷密度（D_{it}）；在能隙深處(midgap)的缺陷電荷經過 FGA 後可被輕微地降低，例如：D_{it} (E_t= 0.428 eV)在 FGA 後降低約 22.28%。其後，電容在 FGA 下與不同 PDA 的效應也已探討。從量測的數據分析指出電容在 PDA 溫度 500 度 120 秒及 FGA 下展現最差的電性。此外，越高的 PDA 溫度，越高的 D_{it} 存在於能隙深處。電性之所以劣化的原因，從 XPS 分析來看為較低的三氧化二砷與五氧化二砷比值（As_2O_3/As_2O_5）及砷化物的析出。接著，在我們

的實驗中，晶向（100）砷化銦鎵的電性較優於晶向（111）A 砷化銦鎵的電性，如較低的頻率分散和較低的 D_{it}。這個結果可能是因為相較於三氧化二鋁和晶向(111)A 砷化銦鎵間的界面，有較高的 As_2O_3/As_2O_5 於三氧化二鋁和晶向(100)砷化銦鎵間的界面。

最後，根據TEM影像和EDX分析，自我對準鎳-砷化銦鎵合金之源極／汲極之*n*型通道金氧半場效電晶體的失敗原因歸因於鎳-砷化銦鎵合金的未形成。其中，最有可能阻礙鎳-砷化銦鎵合金形成的原因為原生氧化層存在於鎳與砷化銦鎵通道層間。

Study on Electrical and Chemical Characteristics of Indium Gallium Arsenide Metal-Oxide-Semiconductor Capacitors with Atomic-Layer-Deposited Al_2O_3 Gate Dielectric

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ABSTRACT

In the beginning of the thesis, we have mainly studied the interface between (100)-oriented $In_{0.53}Ga_{0.47}As$ channel layer and Al_2O_3 (atomic layer deposition, ALD). Poor interface and oxide qualities may cause high frequency dispersion, Fermi level pinning, and high gate leakage current. In order to improve interface and gate oxide qualities, different thermal treatments are applied to the capacitors, such as post-metallization annealing (PMA), forming gas annealing (FGA), and post deposition annealing (PDA). Firstly, we study the difference between the capacitors treated with PMA and those treated with FAG. Compared to PMA, frequency dispersion in accumulation can be efficiently reduced by FGA. In addition, we utilize the conductance method to extract the interface state density (D_{it}). The midgap traps can be slightly reduced: for instance, D_{it} (E_t= 0.428 eV) decreases about 22.28% after

FGA. Subsequently, the effects of MOSCAPs under different PDA temperature with FGA have also been discussed. It is noted that MOSCAPs under PDA 500 ^{o}C for 120 s with FGA show the worst electrical characteristics. Furthermore, higher PDA temperature is, the higher D_{it} exists close to midgap. The reason for the degradation of electrical characteristics may be lower ratio of As_2O_3 to As_2O_5 and the precipitation of arsenide, which is shown in our XPS analysis. Next, in our experiment, the electrical characteristics of $In_{0.53}Ga_{0.47}As$ (100) is better than $In_{0.53}Ga_{0.47}As$ (111)A, such as lower frequency dispersion and lower D_{it}. This consequence is possibly due to higher amounts of As_2O_3/As_2O_5 at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) interface, compared to $Al_2O_3/In_{0.53}Ga_{0.47}As$ (111)A interface.

Eventually, the failure of self-aligned Ni-InGaAs S/D $In_{0.53}Ga_{0.47}As$ *n*-MOSFETs is attributed to the non-formation of Ni-InGaAs according to the TEM image and EDX analysis. The possible reason that inhibits the formation of Ni-InGaAs may the existence of native oxides between Ni and $In_{0.53}Ga_{0.47}As$ channel layer.

誌謝

自由自在的學生生涯終於要畫下最後的休止符了。兩年多的碩士生活，經歷了不只是在課業上所遇到的困難，還有生活上許多大大小小的喜怒哀樂等。首先，感謝我的指導老師－簡昭欣教授，提供挑戰的自由學習環境與實驗資源，讓我們更可以知道一個成功的元件製程，是需要經過多少次的測試、嘗試、實驗和到最後的量測分析。無數次的失敗與打擊、外在無預期的因素，真的是層層關卡、層層磨練，不經意佩服前人在這領域上的貢獻，及克服瓶頸的心理素質。另外，老師時常告訴我們做出來成品的特性，不一定是要最好的，但要有創新性，有其獨特與眾不同的地方。同樣的道理，我想在各行各業或人生道路上都有其應用價值與幫助。最後再次感謝老師如此耐心地等待我完成碩士學業，也非常珍惜這段研究生的點點滴滴與經驗，永生難忘！

信淵學長，非常感謝您在最後的拔刀相助！這段時間裡的學習真的非常充實，也讓我見識到您的廣博知識及驚人的 paper 海，問題每問必答；也謝謝學長能配合我做實驗的時間，期待未來還可以一起歡樂籃球。政庭學長，您的製程手藝與敏銳判斷真是讓我望洋興嘆！每次在製程遇到問題和經驗，都可以好好請教您一番，也感謝您的指教提醒與製程機台的給力幫忙。哲偉學長，實驗室的歡樂籃板王斑蛙，常常帶來意想不到的促咪，感謝您在製程與分析上的教導。您在實驗上的認真拚勁和熱誠，我想這輩子再怎麼努力，也是望塵莫及。這精神我會好好運用在其他領域上，也期待聽到您早日被交易（畢業）出去阿！家豪學長，感謝您在一些問題的指點迷津和經驗分享，常常能感受到您的邏輯思考和處理問題的功力，也恭喜您完成博士學業。偉大的 Acer 學長，非常欽佩您能學業生活兼顧，也是我碩士生涯希望可以做到的。在無塵室聊天總是能得到一些不錯的想法和樂趣，也感謝您的前期機台訓練和幫忙與打氣，讓我們做實驗的時候感受不到孤單！整個新竹只有一個宏基！東昇學長，謝謝您的工作經驗分享與建議，讓我更珍惜

學生的好，也讓我對未來有更多的想法，非常欽佩您能在工作狀態下又能堅持學業，也祝福您能在今年能同時拿到兩張證書！感謝昶智和韋志學長的指教和幫助，尤其是製程 SOP 精神，難人可貴！在此也祝福碩博班學長們都能順利畢業和工作事業順利，快快樂樂。

哲鎮、就舉哥，跟你們住在一起的三個月多，一起吃飯，一起互嗆，尤其是即將離別的惡靈之夜，不亦樂乎！小林，從大學到研究所的夥伴，咱們的活計算機，同為三重埔人的驕傲！從你們身上學習不少特質，也認識到更多的朋友，一同努力的甘苦實驗人生，一同歡笑，難以忘懷！也祝你們在未來的道路上一切順利，成功的話，請多多提拔小弟我！也感謝邦聖和主元的機台供應，讓你們做了不少白工，真不好意思！小弟才疏學淺，實驗沒幫你們太多，請見諒！小龜和純敏也希望你們實驗有所突破和進展，一切順利！碩一學弟們就不一一唱名了，希望你們都能找到自己想走的路，熬過來就是你們的。

旅途上，陪伴我度過無數的喜怒哀樂、酸甜苦辣的朋友們：從小一起在三重埔長大的六人幫、高中的 bro 們和皇家滑輪社的姐妹們、中山物理兄弟們、NPNT 的姐姐和辣媽們、師大心測的帥哥美女們、對岸的天大、東北、北大朋友們、曾經一同出遊的朋友們・・・・・等。總之，沒有你們，就沒有今天的小弟我，謝謝你們一路的支持與不斷的出現，也希望你們能幸福美滿。

最後特別感謝我的家人們，不論是在經濟上和精神上的支持，讓我到這年紀還能享受無憂無慮的學生生活，謝謝你們讓我完成交大夢，也讓我有機會再去更多地方，目睹山川水秀和友誼結交。或許未來不一定會繼續走同樣的路，但我想某些道理應該也適用在其它條道路吧！自己的人生自己負責，趁年輕多去嘗試、多出去看看與經歷、多吃苦、多拓展人脈，我想慢、難、苦之路或許可以體驗和收獲更多吧！ 9911514 下線，準備國軍 on-line！

鄒秉翰

於新竹交通大學

2013 年 3 月 15 日

Contents

Figure Captions

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Chapter 1

Introduction

1.1 General Background

As the scaling of Si-based metal-oxide-semiconductor field effect transistors (MOSFETs) is approaching the physical limit, development of high mobility channel material has been recognized as a potential solution to sustain performance improvements in the upcoming sub-10nm gate length era [1]. Particularly, III-V compound semiconductors are one of the most promising candidates for realizing high performance n-channel metal-insulator-semiconductor field effect transistors (MISFETs) [2,3] due to their high electron mobilities. In 1965, Becke and White reported the first GaAs MOSFET work, using SiO_2 as the gate dielectrics with a large amount of interface states [4]. It was obviously realized that SiO_2 might not the right gate dielectrics for III-V compound semiconductors. Therefore, a variety of dielectrics and techniques have been investigated in the following decades. In 1987, researchers at Bell Labs discovered that sulfur passivation on the surface of III-V semiconductors before dielectrics deposition can improve electrical characteristics [5,6]. The first inversion channel GaAs MOSFETs with MBE-grown Ga_2O_3 (Gd_2O_3) as a gate dielectric were announced in 1996 from Bell Labs [7-9]. After that a series of device work were led by Hong and Ren, including InGaAs enhancement-mode (*E*-mode) MOSFETs [10] and GaAs complementary MOSFETs [11]. At the end of 2001, Ye and Wilk started to work on atomic-layer-deposition (ALD) high-κ Al_2O_3 and HfO_2 on

III-V materials [12]. Detailed interface studies were carried out to demonstrate the unpinning of the Fermi level in III-V semiconductors using ALD high-κ dielectrics [13-15]. In particular, In-rich InGaAs is identified as the potential III-V material for future technology node with higher effective mobility and manageable band gap for low drain voltage.

In the future generations, CMOS fabricated by integrating III-V *n*MOSFETs and Ge *p*MOSFETs, respectively, because of their high electron and hole mobilities, shown in **Table 1.1**, on the same Si platform, shown in **Fig. 1.1**, can be one of the ultimate CMOS structure [16].

1.2 Motivation

One of the major problems enabling widespread use of III-V compound semiconductors to fabricate MOSFETs is lack of a high quality, natural insulator for III-V substrates like that available for the SiO_2/Si material system [17]. In order to realize MOSFETs with III-V channels, suitable gate dielectrics must form a stable interface within the thermal budget of the transistor fabrication process, possess a high dielectric constant and sufficient band offsets with semiconductor conduction band to allow for scaling and low gate leakage, and have a low interface states density (D_{it}). Especially, engineering the interface between the III-V channel material and gate oxide is extremely challenging.

The other challenge to achieve high performance III-V MOSFETs is the reduction of source and drain (S/D) series resistance ($R_{S/D}$), which includes metal-semiconductor contact resistance [18]. Therefore, we have to find the appropriate techniques and conditions to engineer S/D region.

For MOSFET surface channels beyond the 16 nm node, the candidate III-V material $In_xGa_{1-x}As$ alloys which have a band gap of ($0.36 \leqq E_g \leqq 1.42$ eV) and $E_g \geqq$ 14kT are potentially suitable for many applications with power supply operating voltages $\leqq$ 0.5 V envisioned for short gate lengths ($L_g \leqq$ 20 nm) [19]. In particular, alloys with an In content greater than 50% are commonly used as a channel material due to their high electron mobility relative to Si. Here, we use $In_{0.53}Ga_{0.47}As$ as a channel layer which is epitaxial growth on InP substrates to do our studies.

1.3 Organization of the Thesis

In **Chapter 1**, we gave a brief overview on the history and main obstacles in realizing III-V MOSFET. Current status of CMOS research was also described.

In **Chapter 2**, in order to study the interface between $In_{0.53}Ga_{0.47}As$ and Al_2O_3, conductance method was applied to admittance measurement from metal oxide semiconductor capacitors (MOSCAPs). The influence of post-metallization N_2 annealing (PMA), post-metallization forming gas annealing (FGA), and post deposition annealing (PDA) were demonstrated. In addition, the difference in electrical characteristics between the orientation of (100) and (111)A was also studied.

In **Chapter 3** and **Chapter 4**, we tried to fabricate $In_{0.53}Ga_{0.47}As$ channel *n*MOSFETs with self-aligned Ni-InGaAs source and drain. Although the devices could not work, we found the possible reasons for the failure of our *n*-MOSFETs. Eventually, we made the conclusion as mentioned above and gave some suggestions for future works.

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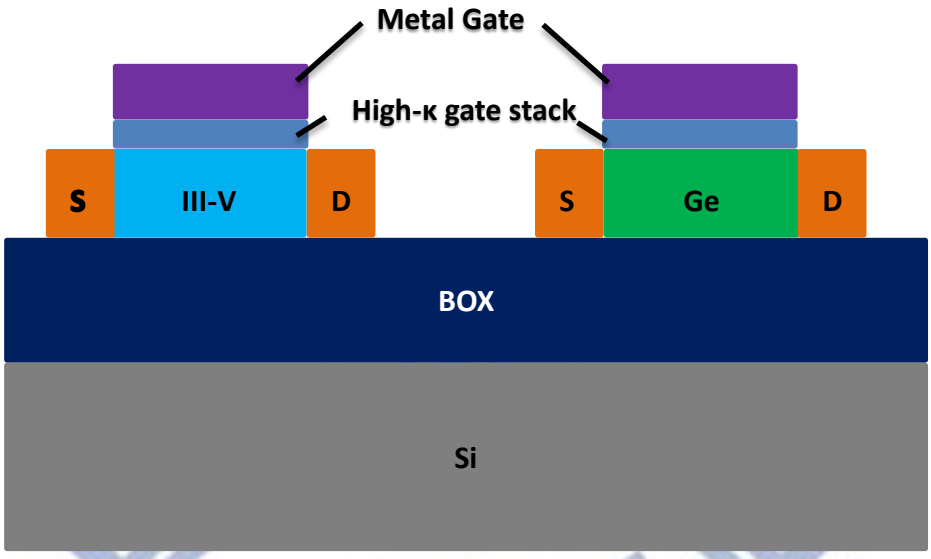

Fig. 1.1 Ultimate CMOS transistors with III-V *n*MOSFETs and Ge *p*MOSFETs on Si substrates with BOX layer

	Si	Ge	GaAs	$In_{0.53}Ga_{0.47}As$	InAs
Lattice constant (Å)	5.431	5.646	5.653	5.869	6.058
Band gap (eV)	1.12	0.66	1.42	0.74	0.36
Permittivity	11.8	16	12	13.9	14.8
Intrinsic carrier conc. (cm^{-3})	9.6×10^{9}	2.4×10^{13}	2.2×10^{6}	7.7×10^{11}	1×10^{15}
Effective conduction band density of states (cm^{-3})	2.8×10^{19}	1.04×10^{19}	4×10^{17}	2.2×10^{17}	8.7×10^{16}
Effective valence band density of states (cm^{-3})	1.04×10^{19}	6×10^{18}	9.7×10^{18}	7.8×10^{18}	6.6×10^{18}
Electron mob. (cm^2/Vs)	1600	3900	9200	12000	40000
Electron effective mass ($/m_0$)	m_t: 0.19 m_l: 0.916	m_t: 0.082 m_l: 1.467	0.067	0.043	0.023
Hole mob. (cm^2/Vs)	430	1900	400	300	500
Hole effective mass ($/m_0$)	m_{HH}: 0.49 m_{LH}: 0.16	m_{HH}: 0.28 m_{LH}: 0.044	m_{HH}: 0.45 m_{LH}: 0.082	m_{HH}: 0.45 m_{LH}: 0.052	m_{HH}: 0.57 m_{LH}: 0.35

Table 1.1 Material properties of bulk Si, Ge, GaAs, $In_{0.53}Ga_{0.47}As$, and InAs at 300K

Chapter 2

Interface Studies of ALD-Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOSCAPs with Different Annealing Conditions and Orientations

2.1 Introduction

Recently, surface-channel $In_{0.53}Ga_{0.47}As$ *n*MOSFETs have drawn much attention as dimensional scaling of Si technology is progressively approaching the limits [1-4]. A longstanding problem for developing of these devices is the presence of interfacial defects that can cause Fermi level pinning or inefficient Fermi level response. Vacancies, antisite defects, or incomplete dimerization of the III-V surface can cause unsaturated bonds and form electrically active traps that may appear even before high-κ dielectric growth or are generated during the deposition [5]. On the other hand, the measured interface state densities are also deeply affected by the indium concentration. While indium content increases, the amount of air-grown Ga_2O_3 decreases probably due to the increased size of In atom reducing the available space for oxygen to bond to the interfacial gallium atoms [6]. High interface trap states would inhibit control over the charge carriers in the channel and the realization of MOSFETs with good performance. Therefore, the most important thing is to reduce D_{it}. Various passivation techniques and surface pre- or post-treatments [7-15] have been considerably researched in the last several decades. Moreover, traps present in the bulk of a high-κ oxide layer may also have a great impact on the performance

owing to their potential to increase gate leakage current, scattering carriers in the channel, and threshold voltage shift of the device [16]. In addition, the prospects of III-V devices are brightening with the introduction of ALD for high-κ gate dielectric. Its precise thickness controllability is attributed to its surface-saturation controlled, layer by layer deposition kinetics [17]. Films deposited by ALD are conformal, pin-hole free, which normally can be further improved by thermal annealing. It is also noted that "self-cleaning" interfacial oxide reaction has been observed on III-V compound semiconductors such as GaAs [18-19], InGaAs [20].

Al_2O_3 is the most commonly used as a gate dielectric for III-V semiconductors due to its less Fermi level pinning and thermal stability than HfO_2. Furthermore, trimethylaluminium ($Al(CH_3)_3$, "TMA") is generally used as a metal precursor, which is known to have more effective self-cleaning capability for removing native oxides on III-V surface than tetrakis(ethylmethylamino)hafnium (TEMA-Hf) used for the HfO_2 deposition [21]. Here, we focus our study on the interface between $In_{0.53}Ga_{0.47}As$ and Al_2O_3. For the sake of further improving oxide quality and its interface, several methods of thermal annealing have been applied to gate dielectric such as PDA, PMA and post-metallization FGA. Surface orientation of III-V channel is also an important parameter in controlling MIS properties. (111)A-oriented $In_{0.53}Ga_{0.47}As$ has been investigated in different PDA conditions with FGA and is compared with (100)-oriented $In_{0.53}Ga_{0.47}As$. Capacitance-Voltage (*C*-*V*) measurements are traditionally utilized to characterize MOS devices and materials; besides, we use conductance method to extract interface states, which can be determined directly from the experiment [22]. In addition to studies on electrical characteristics, some chemical characteristics have been discussed.

2.2 Experimental Procedures

2.2.1 $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) MOSCAPs Pretreated with Trimethylaluminium

P-type (Zn-doped, 4×10^{18} cm^{-3}) InP (100) wafers were used as the starting substrates. P-type (Zn-doped, 1×10^{17} cm^{-3}) $In_{0.53}Ga_{0.47}As$ (100) of 500 nm thick was grown as a buffer layer, followed by a 300-nm p-type $In_{0.53}Ga_{0.47}As$ (100) channel layer (Zn-doped, 1.23×10^{16} cm^{-3}). Similarly, the n-type (100)-oriented $In_{0.53}Ga_{0.47}As$ was grown on an $In_{0.53}Ga_{0.47}As$ buffer layer on InP wafers. Because of air exposure, all samples had initial native oxides on the $In_{0.53}Ga_{0.47}As$ surface. To remove these native oxides, suitable surface pretreatment must be carried out prior to gate dielectric deposition. $In_{0.53}Ga_{0.47}As$ surfaces were initially rinsed for 5 minutes each in acetone (ACE), isopropanol (IPA), followed by the dilute HCl solution ($HCl:H_2O$ = 1:10) for 2 minutes. Then the samples were transferred to ALD chamber as soon as possible. TMA treatment was performed for 10 cycles with a period of 0.06 s for a TMA pulse and 10 s for a N_2 pulse at 250 ^oC before the subsequent Al_2O_3 deposition [23]. The TMA-treated $In_{0.53}Ga_{0.47}As$ surfaces were then *in-situ* coated with ALD-Al_2O_3 films for 100 cycles, using alternating pulsed of TMA and H_2O precursors at 250 ^oC and N_2 as a purging gas to carry redundant reactants away. After that, the samples underwent PDA in N_2 ambience with different annealing conditions, for instance, As-deposited, and 300 ^oC, 400 ^oC, and 500 ^oC for 120 s. Circular MOSCAPs formation was done by sputter deposition of 50 Å of Ti and 500 Å of Pt through a shadow mask. The area of gate electrode examined by optical microscopy was 4×10^{-4} cm^2. Backside ohmic contacts were formed by evaporation. Finally, some of the samples (no PDA) were completed by post-metallization annealing (PMA) in a N_2 flow at 300 ^oC for 30 min,

and the others were carried out by forming gas annealing (FGA), which consists of a continuous flow of 5% H_2/95% N_2 ambience at 300 ^oC for 30 min.

The process flow and MOSCAPs structure are shown in **Fig. 2.1** and **Fig. 2.2**. The cross-sectional TEM image of the as-deposited Al_2O_3 on $In_{0.53}Ga_{0.47}As$ epitaxial layers with TMA treatment (10 cycles) and FGA is shown in **Fig. 2.3**.

2.2.2 $Al_2O_3/In_{0.53}Ga_{0.47}As$ (111)A MOSCAPs Pretreated with Trimethylaluminium

P-type (Zn-doped) InP (111)A wafers were used as the starting wafers. P-type (Zn-doped) $In_{0.53}Ga_{0.47}As$ (111)A of 500 nm thick was grown as a buffer layer, followed by a 300-nm p-type $In_{0.53}Ga_{0.47}As$ (111)A channel layer (Zn-doped, 3.43×10^{17} cm^{-3}). Due to air exposure, all samples had initial native oxides on the $In_{0.53}Ga_{0.47}As$ surface. To remove these native oxides, appropriate surface pretreatment must be carried out prior to gate dielectric deposition. $In_{0.53}Ga_{0.47}As$ surfaces were initially rinsed for 5 minutes each in acetone (ACE), isopropanol (IPA), followed by the dilute HCl solution ($HCl:H_2O$ = 1:10) for 2 minutes. Then the samples were transferred to ALD chamber as soon as possible. TMA treatment was performed for 10 cycles with a period of 0.06 s for a TMA pulse and 10 s for a N_2 pulse at 250 ^oC before the subsequent Al_2O_3 deposition [23]. The TMA-treated $In_{0.53}Ga_{0.47}As$ surfaces were then *in-situ* coated with ALD-Al_2O_3 films for 100 cycles, using alternating pulsed of TMA and H_2O precursors at 250 ^oC and N_2 as a purging gas to carry redundant reactants away. After that, the samples underwent PDA in N_2 ambience with different annealing conditions, for example, As-deposited, and 300 ^oC, 400 ^oC, and 500 ^oC for 120 s. Circular MOSCAPs formation was done by sputter

deposition of 50 Å of Ti and 500 Å of Pt through a shadow mask. The area of gate electrode examined by optical microscopy was 4×10^{-4} cm^2. Backside ohmic contacts were formed by evaporation of Ti/Pt (50/500 Å). Finally, all the samples were finished by forming gas annealing (FGA), which consists of a continuous flow of 5% H_2/95% N_2 ambience at 300 ^oC for 30 min.

The process flow and MOSCAPs structure are shown in **Fig. 2.4** and **Fig. 2.5**.

2.3 Electrical Characteristics of ALD-TMA/$In_{0.53}Ga_{0.47}As$ (100) and Interfacial Chemistry

It has been taken a long time to develop MOS devices with various oxides on III-V compound semiconductors. The electrical characteristics of these MOSCAPs is closely related to processing conditions such as wafer preparation, passivation technique, dielectric deposition technique, PDA, PMA, FGA, etc. In this section, the electrical behaviors of Al_2O_3 on $In_{0.53}Ga_{0.47}As$ with respect to interfacial chemistry had been demonstrated. Capacitance-Voltage (*C-V*) and conductance-voltage (*G-V*) measurements were measured by HP4284A *LCR* meter at the temperature of 300K. Nevertheless, application of the technique to III-V systems requires considerable care, as described extensively by Passlack [24].

We quantitatively define frequency dispersion ratio ΔC. The equations of ΔC are as follows:

$\Delta C(@V_G = -2\ V) \equiv \{[C(@1kHz) - C(@100kHz)]/C(@1kHz)\}\times100\%$ p-type, **(2.1)**

$\Delta C(@V_G = 2\ V) \equiv \{[C(@1kHz) - C(@100kHz)]/C(@1kHz)\}\times100\%$ n-type, **(2.2)**

where ΔC is the frequency dispersion of capacitance measured in 1 kHz and 100 kHz at V_G = 2 or V_G = -2 volt. The overviews of frequency dispersion of the samples are

shown in **Table 2.1**.

2.3.1 *C-V* Measurements of MOSCAPs w/ or w/o FGA

The CV responses at room temperature (300K) with ac signal frequencies from 100 kHz to 100 Hz for the *p*-type and *n*-type Pt/Ti/Al_2O_3 (As-deposited)/$In_{0.53}Ga_{0.47}As$ MOSCAPs with or without FGA are shown in **Fig. 2.6 (a) (c)** and **Fig. 2.7 (b) (d)**, respectively. It is noted that the *C-V* curves for *p*-type and *n*-type MOSCAPs are remarkably improved by FGA. The **Table 2.1** shows that the frequency dispersion of *p*-type MOSCAPs without FGA is 64.39%. After FGA, the frequency dispersion at V_G = -2 V dramatically reduces to 8.96%. Moreover, the stretch-out of *C-V* curves has also been improving after FGA. Correspondingly, the frequency dispersion and stretch-out of *C-V* curves for *n*-type MOSCAPs received FGA become well. In general, the stretch-out and frequency dispersion of the *C-V* curves are mainly caused by the existence of interface states. The higher the D_{it}, the larger the frequency dispersion of the *C-V* curves and stretch-out. Therefore, we infer that the interface between gate dielectric and substrate might be restored by FGA, which is well known for passivating P_b-like defects in SiO_2/Si and high-κ/SiO_x/Si systems [25, 26]. Then, we adjust the process flow, doing FGA subsequent to gate oxide deposition, to confirm whether FGA can reduce interface defects. However, we found that there is no marked difference in *C-V* curves between MOSCAPs without FGA and MOSCAPs with FGA subsequent to gate oxide deposition (not shown). FGA must be done after the deposition of gate metal probably for repairing the damage caused by sputter or improving the interface between gate dielectric and gate electrode.

In the next section, we will discuss the discrepancy between FGA and PMA.

2.3.2 *C-V* and *G-V* Measurements of MOSCAPs w/ FGA or PMA

Fig. 2.8 (a) (c) and **Fig. 2.9 (b) (d)** show multifrequency *C-V* curves of MOSCAPs with a thick (~11 nm) Al_2O_3 film on *p*- and *n*-type TMA treated (100)-oriented $In_{0.53}Ga_{0.47}As$ with FGA or with PMA, respectively, measured at 300K. For the *p*-type, both two samples never reach strong accumulation, which indicates a high D_{it} close to the valence band edge. The frequency dispersion of MOSCAPs with PMA is 12.34% larger than MOSCAPs with FGA, but much smaller than MOSCAPs without any post-metallization thermal annealing, shown in **Table 2.1**. A hump is seen at positive bias in both two samples, which may indicate the response of D_{it}. For the *n*-type MOSCAPs, accumulation is achieved at positive gate bias. The frequency dispersion of MOSCAPs with PMA is 8.08% larger than MOSCAPs with FGA, also shown in **Table 2.1**. At negative gate voltages the total capacitance changes with gate bias and frequency, which may also indicate the response of interface states.

Fig. 2.10 (a) (c) and **Fig. 2.11 (b) (d)** show conductance maps of Al_2O_3/TMA-treated $In_{0.53}Ga_{0.47}As$ MOSCAPs with FGA or with PMA, on both *p*- and *n*-type (100)-oriented $In_{0.53}Ga_{0.47}As$, respectively, at temperature 300 K. These maps show the magnitude of normalized conductance $(G/\omega)/Aq$ as a function of ac frequency *f* and the gate voltage V_G. For the *p*-type MOSCAPs, both two plots show that a distinct signal exists at the gate voltage between 0 and 1 volt and at frequency between 100 Hz and 10 kHz. We speculate that this energy loss is caused by interface states due to its gate-voltage dependent and frequency-dependent conductance. For the *n*-type MOSCAPs, there is a conspicuous variation in color appearing at the negative gate voltage in both two graphs, which implies the dramatic energy loss.

Similarly, the *G-V* response to this energy loss is made by interface states owing to its gate-voltage dependent and frequency-dependent conductance. Additionally, the color variation at negative gate bias in **Fig. 2.11 (b)** is less dramatic than in **Fig. 2.11 (d)**.

The frequency dispersion of the accumulation capacitance can be attributed to tunneling of carriers between the substrate and defect states in the ALD-Al_2O_3 dielectric. The term "border traps" is referred to near-interfacial oxide traps that can exchange charge with substrate or gate, respectively [27]. While filling and emptying of interface states is a thermally activated process, tunneling of charges into border traps depends only on the measurement frequency and the distance of the defect states from the oxide/semiconductor interface. Some related studies have reported that the dispersion in the accumulation capacitance of such MOSCAPs is consistent with a tunneling mechanism for charge trapping, insensitive to temperature [28, 29]. Border traps that are close to conduction band edge of semiconductor contribute most effectively to the dispersion in accumulation, for *n*-type channel. **Fig. 2.12** shows schematically the tunneling process between border traps and conduction band in an *n*-doped MOSCAP operated in accumulation. Our results are generally consistent with previous reports of hydrogen passivation of $Al_2O_3/In_{0.53}Ga_{0.47}As$, mainly passivating border traps in the Al_2O_3 layer [30]. Since interface states nearly respond immediately in deep accumulation, the decreased dispersion in accumulation observed in **Fig. 2.8 (a)** and **Fig. 2.9 (c)** may result exclusively from passivation of border traps. Nonetheless, the response of interface states observed at V_G=0~ -2 volts still exists but less dramatic after FGA, shown in **Fig. 2.11 (b)**, and also the evidence of interface states observed at V_G=0~ 1 volt for *p*-type MOSCAPs, shown in **Fig. 2.10 (a)**, does not disappear after FGA. Therefore, we suppose that hydrogen is unable to completely reduce all interface states. Their binding energies are 2.52 eV for In-H, < 2.84 eV for Ga-H, and 2.84 eV for As-H [31]. Other researches consider that annealing in

hydrogen can remove most of the fixed oxide charge and interface states [32-34]. The presence of positive bulk fixed charge and negative interfacial fixed charge is identified as oxygen and aluminum dangling bonds (DBs), respectively. **Fig. 2.13** shows the band alignment between Al_2O_3 and relevant semiconductors, and position of charge-state transition levels for dangling bonds in the oxide from the reference [32]. After FGA, O DBs and Al DBs are neutralized by hydrogen, which the resulting binding energies are 1.3 eV for O-H and 1.4 eV for Al-H, respectively. However, some groups consider that the previously reports of FGA cannot be solely attributed to hydrogen passivation [35]. Hydrogen passivation of dangling bonds and border traps is responsible for improving the interfacial properties, while the thermal budget is responsible for minimizing the fixed charge. According to their opinions on the thermal effects of annealing, the presence of sufficient thermal energy can reconstruct the bonds to fill vacancies and to passivate dangling bond throughout the oxide. Another possibility is that PMA may provide enough thermal energy to break the O-H hydroxyl groups existing as a byproduct during the deposition of Al_2O_3. Hence, free hydrogen dissociated from these O-H groups can also passivate dangling bonds, but the amount of hydrogen available would be limited by the presence of O-H bonds in the film.

In summary, FGA was found to suppress frequency dispersion in accumulation, which suggests that hydrogen could be a promising candidate as the method for passivation of border traps. In addition, it can also reduce some, but not all, interface states. Hydrogen annealing of these devices at 300 ^{o}C for 30 min has demonstrated better *C-V* and *G-V* characteristics, and we'll further discuss the impact of PDA on the electrical characteristics of these MOSCAPs in the next section.

2.3.3 Electrical and Chemical Characteristics of MOSCAPs w/ FGA under Various PDA Conditions

Fig. 2.8 (a), Fig. 2.14 (a) (b) (c) and **Fig. 2.9 (b)**, **Fig. 2.15 (a) (b) (c)** show multifrequency *C-V* curves of MOSCAPs with a Al_2O_3 film on *p*- and *n*-type TMA treated (100)-oriented $In_{0.53}Ga_{0.47}As$ after post-metallization FGA under different PDA conditions, respectively, measured at 300K. For *p*-type, the MOSCAPs with PDA at 500 ^oC for 120 s exhibit the worst electrical characteristics. Although the capacitance value at V_G= -2 volts of MOSCAPs with PDA 500 ^oC for 120 s is the largest, the frequency dispersion of the samples with PDA 500 ^oC for 120 s severely degrades not only near accumulation (ΔC (@V_G = -2 V) =16.91%) but also in depletion. It is noted that the response of interface traps at V_G= 0 to $V_{G=}$ 1 volt is severely getting large as the temperature of PDA increases; therefore, for our $In_{0.53}Ga_{0.47}As$ substrate, the limited temperature of post deposition annealing is 300 ^oC. The minority carrier response of MOSCAPs with PDA 500 ^oC for 120 s is obviously seen at V_G= 1 to V_G=2 volts. For the *n*-type MOSCAPs, the frequency dispersion of MOSCAPs with PDA 500 ^oC for 120s is 8.99% larger than MOSCAPs with other PDA conditions. All the samples under various PDA conditions demonstrated the response of interface states at negative gate voltages due to bias-dependent and frequency-dependent capacitance. All of the frequency dispersion values under various PDA conditions are summarized in **Table 2.1**.

Fig. 2.10 (a), **Fig. 2.16 (a) (b) (c)** and **Fig. 2.11 (b)**, **Fig. 2.17 (a) (b) (c)** show conductance maps of Al_2O_3/TMA-treated $In_{0.53}Ga_{0.47}As$ MOSCAPs with FGA under different PDA conditions, on both *p*- and *n*-type (100)-oriented $In_{0.53}Ga_{0.47}As$, respectively, at temperature 300K. These maps show the magnitude of normalized

conductance *(G/ω)/Aq* as a function of ac frequency *f* and the gate voltage V_G. For the *p*-type MOSCAPs, all plots show that a distinct signal exists at the positive gate voltage and lower frequency. The color variation in this region is getting dramatic as the temperature of PDA is above 400 ^oC. We speculate that the amount of interface states considerably increases as the temperature of PDA is getting higher. For the plot of PDA 500 ^oC for 120 s, there is an additional signal existing at gate voltage between -2 and -1 volt and higher frequency; furthermore, we also observe that the conductance is constant at gate voltage between 1 and 2 volts, indicating minority carrier response. For the *n*-type MOSCAPs, there is a conspicuous variation in color appearing at the negative gate voltage in all graphs, which implies that energy loss is dramatically rising. Similarly, the *G-V* response to this energy loss is made by interface states owing to its gate-voltage dependent and frequency-dependent conductance. Additionally, the signal existing between V_G= 1 and V_G= 2 volts and higher frequency becomes distinct as the temperature of PDA increases.

Fig. 2.18 (a) (b), and **(c)** show X-ray photoelectron spectroscopy of ALD-TMA (10 cycles)/Al_2O_3 (10 cycles) on (100)-oriented $In_{0.53}Ga_{0.47}As$ with post-metallization FGA under various PDA conditions. XPS scans of Ga $2p_{3/2}$, In $3d_{5/2}$, and As $2p_{3/2}$ core levels are taken. From **Fig. 2.18 (a)** and **(b)**, we observe that there is no significant change in Ga $2p_{3/2}$ and In $3d_{5/2}$ spectra. The As $2p_{3/2}$ spectra, shown in **Fig. 2.18 (c)**, demonstrates that As-As bonds are present in these PDA conditions. It is noted that the concentration of As-As states dramatically increases under PDA 500 ^oC. We also find that a lower binding energy peak, which is labeled As- in the spectra, is detected on the samples with PDA 500 ^oC for 120s. This may be an indication of breaking of As-As states at the surface, creating an arsenic dangling bond. In addition, the ratio of As_2O_3 to As_2O_5 at PDA 500 ^oC is the lowest. **Table 2.3** shows the ratio of the fitted area of the As-As and As- components and As_2O_3 to As_2O_5 from the As $2p_{3/2}$ spectra

for the $In_{0.53}Ga_{0.47}As$ (100).

The results suggest that the considerable existence of As-As states or As- states and As_2O_5 at the interface should be avoided, causing the degradation of electrical characteristics. The reason for the degradation of *C-V* characteristics with PDA 500 ^oC for 120 s may be the precipitation of arsenide and lower ratio of As_2O_3 to As_2O_5 (As_2O_3 to As_2O_5). High temperature annealing results in the excess arsenic atoms produced either the decomposition of $In_{0.53}Ga_{0.47}As$ itself or the chemical transformation of the oxide species through reactions with the $In_{0.53}Ga_{0.47}As$ channel layer. The elemental arsenide overlayer acted as a metallic contamination source nearby the interface between oxide and substrate increases the surface recombination velocity, deteriorating insulator properties [36]. In addition, the possibility that a little amount of arsenic oxides diffused into the Al_2O_3 during post deposition annealing at temperature above 300 ^oC cannot be excluded.

2.4 Electrical Characteristics of ALD-TMA/$In_{0.53}Ga_{0.47}As$ (111)A and Interfacial Chemistry

There have been few studies regarding the MIS properties on the (111) surface of III-V semiconductors. Some previous research showed that the electrical characteristics of (111)A-oriented $In_{0.53}Ga_{0.47}As$ and (111)A-oriented GaAs MIS capacitors with Al_2O_3 dielectrics deposited by ALD were comparable to or even better than those on the (100)-oriented $In_{0.53}Ga_{0.47}As$ and (100)-oriented GaAs MIS capacitors [37-39]. Besides, since the former approach has succeeded in forming uniform and dislocation-free InGaAs layers on Si (111), the characteristics of

MISFET on the (111)-oriented InGaAs are of great interest [40].

Fig. 2.19 (a) (b) (c) (d) show multifrequency *C-V* curves of MOSCAPs with a Al_2O_3 film on *p*-type TMA treated (111)A-oriented $In_{0.53}Ga_{0.47}As$ after post-metallization FGA under different PDA conditions, measured at 300K. The frequency dispersion at V_G= -2 slightly improves at PDA of 300 ^oC and 400 ^oC but degrades at PDA of 500 ^oC, shown in **Table 2.2**. At positive gate bias, the capacitance remarkably increases at lower frequency compared to our previous *C-V* curves of *p*-type $In_{0.53}Ga_{0.47}As$ MOSCAPs with (100) orientation, shown in **Fig. 2.8 (a)** and **Fig. 2.14 (a) (b) (c)**. We suppose that the inversion response appears at more positive gate voltages and lower frequency due to the constant capacitance.

Fig. 2.20 (a) (b) (c) (d) show conductance maps of Al_2O_3/TMA-treated $In_{0.53}Ga_{0.47}As$ MOSCAPs with FGA under different PDA conditions, on *p*-type (111)A-oriented $In_{0.53}Ga_{0.47}As$ at temperature 300K. These maps show the magnitude of normalized conductance $(G/\omega)/Aq$ as a function of ac frequency *f* and the gate voltage V_G. Under various PDA conditions with FGA, we could easily observe the minority carrier response at more positive gate bias in all graphs, and the as-deposited one with FGA demonstrates the strongest minority carrier response. The response of interface states also exists at gate voltage between -1 and 0 volt.

Fig. 2.21 (a) (b), and **(c)** show X-ray photoelectron spectroscopy of ALD-TMA (10 cycles)/Al_2O_3 (10 cycles) on (111)A-oriented $In_{0.53}Ga_{0.47}As$ with post-metallization FGA under various PDA conditions. XPS scans of Ga $2p_{3/2}$, In $3d_{5/2}$, and As $2p_{3/2}$ core levels are taken. From **Fig. 2.21 (a)** and **(b)**, we observe that there is no significant change in Ga $2p_{3/2}$ and In $3d_{5/2}$ spectra. The As $2p_{3/2}$ spectra, shown in **Fig. 2.21 (c)**, demonstrates that the As- component dramatically increases under PDA 500 ^oC for 120 s. Furthermore, the ratio of As_2O_3 to As_2O_5 slightly increases at PDA 300 ^oC but becomes low at PDA 400 ^oC and 500 ^oC. **Table 2.4**

shows the ratio of the fitted area of the As-As and As- components and As_2O_3 to As_2O_5 from the As $2p_{3/2}$ spectra for the $In_{0.53}Ga_{0.47}As$ (111)A.

2.5 Conductance Method

Methods of quantifying D_{it}, the trap level energy position and the degree of Fermi level (un)pinning are important in the development of high quality interface between high-κ dielectric and III-V materials [41-43]. It is often impractical to fabricate MOSFET for III-V devices because the transistor fabrication process may introduce other issues. Therefore, MOSCAP structures are commonly used to study the dielectric/substrate interface, dating back to 1960s. The conductance method including the effects of the energy distribution of interface states in the bandgap and surface potential fluctuation (SPF), which has been established by Nicollian and Geotzberger, is a powerful and sensitive tool to determine D_{it}. **Fig 2.22 (a)** shows that a *n*-type MOSCAP applies to a small amplitude (~25 mV) ac signal with frequency *f* (typically between 1 MHz and 100Hz) superimposing on a dc gate bias, V_g. Also shown are the conduction and valence band DOS, D_{dos}, an arbitrary interface states density distribution, the Fermi level E_F and the intrinsic level E_I. **Fig. 2.22 (a)** assumes that the band diagram of this MOSCAP is in depletion region. The gate voltage, inducing a space charge and band bending,ψ_s ,determines the Fermi level position at the interface. A periodic change in ψ_s is caused by the ac small signal and the Fermi level at the interface oscillates around the energy level position determined by the dc gate bias. Only traps with energy levels that are near the Fermi level are able to change their occupancy. An equivalent circuit model for a MOSCAP with interface states in depletion region, including the gate oxide capacitance, C_{ox}, the

semiconductor capacitance, $C_{dos}(\omega,\psi_s)$, interface trap capacitance, $C_{it}(\omega,\psi_s)$, equivalent parallel conductance, $G_p(\omega,\psi_s)$ and a series resistance, R_s, is shown in **Fig. 2.22 (b)**. The circuit model shown in **Fig. 2.22 (b)** assumes that the minority carrier response is negligible. **Fig. 2.22 (c)** shows the equivalent circuit of impedance analyzer with the measured capacitance, C_m, and conductance, G_m. The frequency dependence is related to the characteristic trap response time,

$$\tau = \frac{2\pi}{\omega},$$

where ω is the angular frequency,

$\omega = 2\pi f$ (f=measurement frequency)

The interface trap capacitance is related to the interface states density by

$$C_{it} = q^2 D_{it},$$

where q is the elemental charge

The trap response time for electron or hole is given by Shockley-Read-Hall statistics of capture and emission rate:

$$\tau_e = \left(\sigma \upsilon_{th,e} N_c\right)^{-1} \exp\left[\frac{E_C - E_t}{k_B T}\right]$$
$$\tau_h = \left(\sigma \upsilon_{th,h} N_v\right)^{-1} \exp\left[\frac{E_t - E_v}{k_B T}\right], \quad \textbf{(2.3)}$$

where E_t is the trap energy in the band gap, σ is the capture cross section, ν_{th} is the average thermal velocity of majority carriers, N is the effective density of states of the majority carrier band, k_B is the Boltzmann constant, and T is the temperature.

The conductance method is based on analyzing the loss that is caused by the change in the trap level charge state. G_p/ω is given in terms of the measured capacitance, C_m, the oxide capacitance, C_{ox}, and the measured conductance, G_m, by comparison the circuit of **Fig. 2.22 (b)** and **Fig. 2.22 (c)**, shown as follows:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad \textbf{(2.4)}$$

For continuum trap level, the time constant dispersion must be taken into account and the normalized conductance is shown as follows:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})^2\right] \quad \textbf{(2.5)}$$

Maximum loss occurs when interface traps are in resonance with the applied ac signal. For **Eq. (2.3)** we find

$$D_{it} \approx \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{\max} \text{ as } \omega\tau_{it} \approx 2 \quad \textbf{(2.6)}$$

where A is the device area. E_t can be determined from the frequency at $(G_p/\omega)_{max}$ and applying **Eq. (2.5)**. **Fig. 2.23 (a) (b)** show trap level position calculated from **Eq. (2.3)** using the values for the average thermal velocity and the band DOS for $In_{0.53}Ga_{0.47}As$ and a capture cross section $\sigma = 1\times10^{-17}$ cm^2. The characteristics trap frequency as a function of temperature determines the part of interface traps in the band gap observable in the MOS admittance characteristic. **Fig. 2.23 (a)** shows the characteristics trap frequency as the function of trap energy in the band gap under different temperature (300K, 250K, 200K, 150K, 100K, and 77K). Due to typical measurement frequency between 100 Hz and 1M Hz, it's impossible to extract the interface state density over the whole band gap at room temperature. However, by varying the temperature, the complete D_{it} profiles can be done. For the band gap around 0.74 eV of $In_{0.53}Ga_{0.47}As$, traps near midgap could be observed at room temperatures. The traps closer to the band edges could be probed by measuring the impedance at lower temperature because of increase of the trap response time. **Fig. 2.23 (b)** shows the traps energy as a function of temperature at frequency 100 Hz (orange line) and 1 MHz (dark blue line). It also demonstrates the measurement

windows at given temperature and the limited range of typical measurement frequency.

2.5.1 Comparison between FGA and PMA

Fig. 2.24 (a) (b) and **Fig. 2.25 (a) (b)** show conductance maps of Al_2O_3/TMA-treated $In_{0.53}Ga_{0.47}As$ MOSCAPs with FGA or with PMA, on both *p*- and *n*-type (100)-oriented $In_{0.53}Ga_{0.47}As$, respectively, at temperature 300K. These maps show the magnitude of normalized parallel conductance $(G_p/\omega)/Aq$ as a function of ac frequency *f* and the gate voltage V_G. The D_{it} is estimated by multiplying the peak value, $[(G_p/\omega)/Aq]_{max}$, with a factor of 2.5[see **Eq. 2.6**]. In **Fig. 2.24 (b)**, there is a remarkable response appearing at V_G= -2 volts and frequency between 1 kHz and 100 Hz. We speculate that this response might be slow traps or border traps [**section 2.3.2**]. The samples with FGA, shown in **Fig. 2.24 (a)**, don't show the response at the same region, which indicates H_2 annealing is able to passivate these slow traps and reduces the frequency dispersion in accumulation. For *n*-type MOSCAPs, we also observe that the slow traps are effectively passivated by hydrogen annealing and lower interface states exist in the samples with FGA [**Fig. 2.25(a)**].

Fig. 2.26 (a) (b) and **Fig. 2.27 (a) (b)** show the parallel conductance curves of Al_2O_3/TMA-treated $In_{0.53}Ga_{0.47}As$ MOSCAPs with FGA or with PMA, on both *p*- and *n*-type (100)-oriented $In_{0.53}Ga_{0.47}As$, respectively, at temperature 300K by using **Eq. 2.4**. The G_p/ω-*f* curves from V_G= -1 to 1 volt for *p*-type and V_G= 0.5 to -1.5 volts for *n*-type are demonstrated here, and D_{it} can be obtained by multiplying peak value with a factor of 2.5. It is clearly known that MOSCAPs with FGA have lower interface states than MOSCAPs with PMA. According to **Eq. 2.3**, the frequency corresponding

to peak value can transfer to trap position in band gap; consequently, D_{it} profiles can be done by the conductance method. The D_{it} profiles of MOSCAPs with FGA and with PMA are shown in **Fig. 2.28 (a) (b)**, assuming the capture cross section to be 10^{-17} cm^2. We can only observe the interface states near midgap because of material properties and measurement temperature (300K). This result corresponds to our previous graph, **Fig 2.23 (a) (b)**. It is noted that the interface states near midgap can be reduced slightly about 22.28% (E_t= 0.428 eV) by hydrogen annealing,

2.5.2 MOSCAPs with FGA under Various PDA Conditions

Fig. 2.29 (a) (b) (c) and **Fig. 2.30. (a) (b) (c)** show parallel conductance maps of Al_2O_3/TMA-treated $In_{0.53}Ga_{0.47}As$ MOSCAPs with FGA under different PDA conditions, on both *p*- and *n*-type (100)-oriented $In_{0.53}Ga_{0.47}As$, respectively, at temperature 300K. These maps show the magnitude of normalized parallel conductance $(G_p/\omega)/Aq$ as a function of ac frequency *f* and the gate voltage V_G. The D_{it} is estimated by multiplying the peak value, $[(G_p/\omega)/Aq]_{max}$, with a factor of 2.5[see **Eq. 2.6**]. For *p*-type MOSCAPs, all plots show that a distinct response of D_{it} exists at the gate voltage between 0 and 1 volt and lower frequency. The color variation in this region is getting dramatic as the temperature of PDA is above 400 ^oC. This indicates D_{it} dramatically increases, causing higher frequency dispersion in this region. For the samples with PDA 500 ^oC for 120 s, we also see the minority carrier response at gate voltage between 1 and 2 volt; furthermore, we speculate that the response appearing at V_G= -2 volts and lower frequency may be the slow traps, resulting in higher frequency dispersion at V_G= -2 volts. For the *n*-type MOSCAPs, the response of D_{it} is obviously seen at gate voltage between 0 and -2 volts and. In addition, we also observe slight

response of slow traps appearing on the samples with PDA 500 ^{o}C for 120 s. Consequently, in order to retain our interface and oxide quality, higher PDA temperature should be avoided. PDA of 500 ^{o}C seriously degrades electrical characteristics due to the presence of border traps and higher D_{it}. We suppose that higher interface traps appearing at PDA 500 ^{o}C might be the precipitation of arsenide or As- states and the considerable existence of As_2O_5, and border traps might be the diffusion of arsenic oxides into Al_2O_3 during higher temperature of PDA, discussed in previous **section 2.3.3**.

Fig. 2.31 (a) (b) (c) and **Fig. 2.32 (a) (b) (c)** show parallel conductance curves of Al_2O_3/TMA-treated $In_{0.53}Ga_{0.47}As$ MOSCAPs with FGA under different PDA conditions, on both *p*- and *n*-type (100)-oriented $In_{0.53}Ga_{0.47}As$, respectively, at temperature 300K. The G_p/ω-*f* curves from V_G= -1 to 1 volt for *p*-type and V_G= 0.5 to -1.5 volts for *n*-type are demonstrated here, and D_{it} can be obtained by multiplying peak value with a factor of 2.5. It is found that the peak value is getting larger as the temperature of PDA increases for *p*-type. For *n*-type MOSCAPs, the peak value is almost the same but its position is nearly pinned at the frequency between 10 kHz and 1 kHz when the temperature of PDA is above 400 ^{o}C. **Fig. 2.33 (a) (b) (c)** show the D_{it} profiles of $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) with post-metallization FGA under various PDA conditions, assuming the capture cross section to be 10^{-17} cm^2. It is obviously seen that the higher PDA temperature is, the higher D_{it} exist close to midgap. D_{it} increases 322.65% at $E_{t=}$ 0.377 eV after PDA 500 ^{o}C for 120 s, which indicates the degradation of interface quality.

2.5.3 Comparison between the orientation of (100) and (111)A

Fig. 2.34 (a) (b) (c) (d) show parallel conductance maps of Al_2O_3/TMA-treated $In_{0.53}Ga_{0.47}As$ MOSCAPs with FGA under different PDA conditions on *p*-type (111)A-oriented $In_{0.53}Ga_{0.47}As$ at temperature 300K. It is noted that the response of slow traps only appears in the samples only with FGA, shown in **Fig. 2.34 (a)**. This response disappears at other PDA temperature. Compared to **Table 2.2**, it seems that the electrical characteristics of MOSCAPs under PDA 300 ^oC with FGA is the best in all the samples for (111)A orientation. Even though we don't observe the slow trap response at the samples with PDA 400 ^oC and 500 ^oC, there's been an upward trend in the frequency dispersion at V_G= -2 volts. In addition, the minority carrier response is strong in all samples, especially for only FGA one.

Fig. 2.35 (a) (b) (c) (d) show parallel conductance curves of Al_2O_3/TMA-treated $In_{0.53}Ga_{0.47}As$ MOSCAPs with FGA under different PDA conditions on *p*-type (111)A-oriented $In_{0.53}Ga_{0.47}As$ at temperature 300K. We observe that the interface states are reduced after PDA. However, the peak position is weakly pinned at frequency around 10 kHz for MOSCAPs with PDA temperature above 400 ^oC. **Fig. 2.36** shows the D_{it} profiles of $Al_2O_3/In_{0.53}Ga_{0.47}As$ (111)A with post-metallization FGA under various PDA conditions, assuming the capture cross section to be 10^{-16} cm^2. The interface states can be reduced about 67% at the trap energy of 0.347 eV after PDA 300 ^oC for 120 s. The proper temperature of PDA is very important; otherwise higher temperature could damage the gate oxide and degrade the interface between gate dielectric and substrate, causing higher frequency dispersion, higher D_{it}, and Fermi level pinning. Eventually, we demonstrate the D_{it} profiles of the best PDA

conditions for the orientation of (100) and (111)A. In comparison with the orientation of (100), we find that the interface states of (111)A are even larger. The overviews of D_{it} values of MOSCAPs under various thermal treatments are shown in **Table 2.5**.

2.6 Summary

The conductance method is a basic and useful tool for interface engineering. It can extract interface states over band gap directly from impedance measurements of MOSCAPs by varying the temperature. Analyzing $Al_2O_3/In_{0.53}Ga_{0.47}As$ interfaces with the conductance method, we can clearly find the best oxide and interface qualities under various process conditions and different substrate orientations. Our primary purpose in this chapter is to design the optimum process conditions for gate stack, also corresponding to fabrication of *p*-MOSFETs later.

Firstly, we study the effect of different thermal annealing. Compared to PMA, frequency dispersion in accumulation can be efficiently reduced by FGA. In addition, midgap traps have been slightly decreased after FGA. Subsequently, MOSCAPs under different PDA with FGA have also been discussed. It is noted that MOSCAPs under PDA 500 ^{o}C for 120 s with FGA show the worst electrical characteristics. Furthermore, higher PDA temperature is, the higher D_{it} exists near midgap. The reason for the degradation of electrical characteristics may be the lower ratio of As_2O_3 to As_2O_5 and the existence of As-As states or As- states, which is shown in our XPS analysis.

Next, in our experiment, the electrical characteristics of $In_{0.53}Ga_{0.47}As$ (100) is better than $In_{0.53}Ga_{0.47}As$ (111)A, such as lower frequency dispersion and lower D_{it}, Hence, the (100)-oriented substrate would be used to fabricate MOSFETs.

Furthermore, the reason for studying different PDA conditions is the lift-off process used in gate patterning of MOSFETs. Because the developer solution used in this lift-off process is capable of etching Al_2O_3, we manage to strengthen our gate oxide by thermal annealing or other methods. In general, Al_2O_3 would be strong as the PDA temperature becomes high. However, excess thermal budget is not suitable for $In_{0.53}Ga_{0.47}As$ substrates, probably resulting in degradation of electrical characteristics. Therefore, we have to find the optimum process conditions not only for anti-etch gate dielectric but also for lower D_{it}. In our study, the MOSCAPs with PDA 300 ^{o}C for 120 s have demonstrated quite good electrical characteristics. Other methods like depositing thin HfO_2 on Al_2O_3 can be considered.

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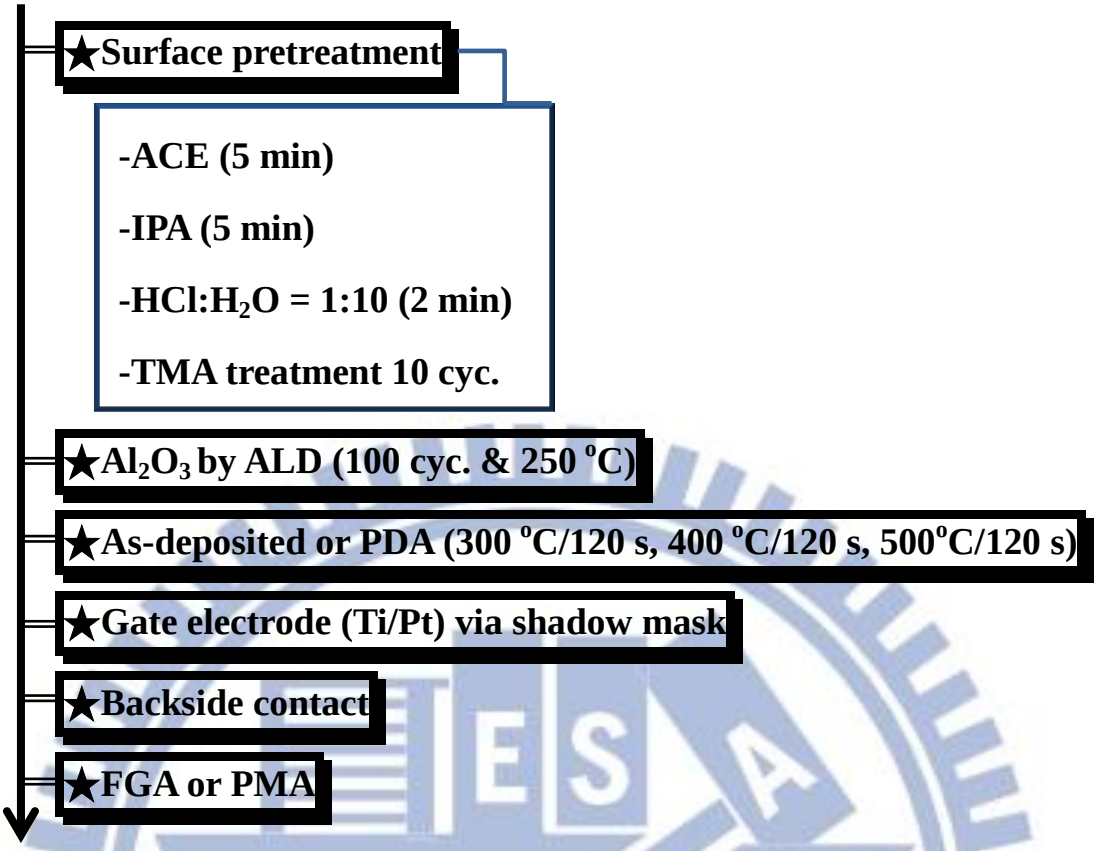


Fig. 2.1 Process flow of (100)-oriented $In_{0.53}Ga_{0.47}As$ channel MOSCAPs with different thermal treatments

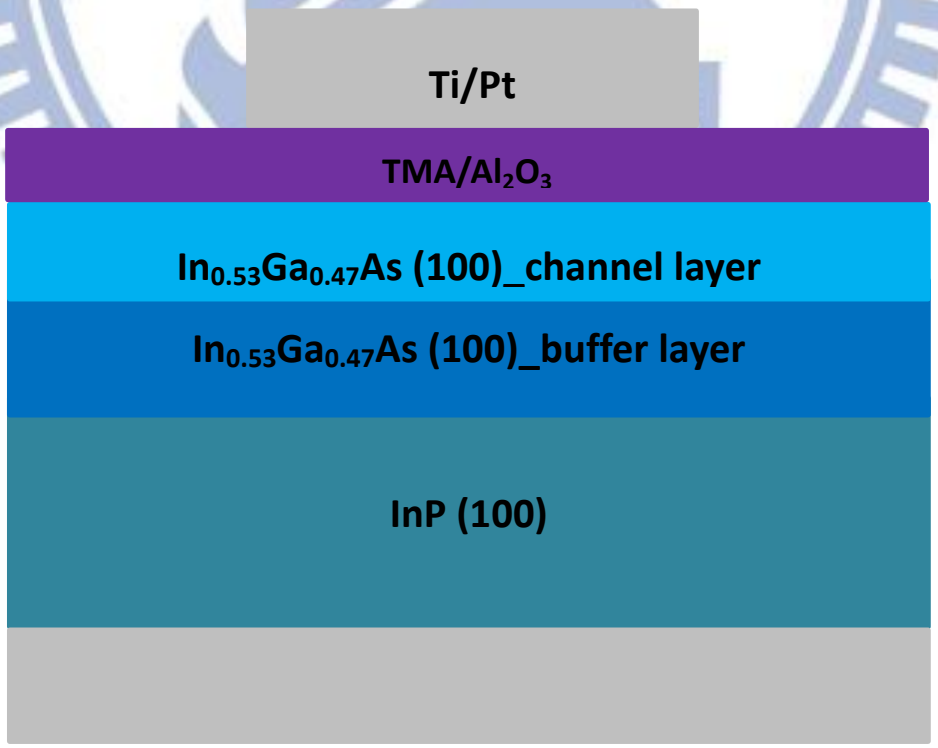


Fig. 2.2 MOSCAPs structure with ALD-TMA/Al_2O_3/$In_{0.53}Ga_{0.47}As$ (100)

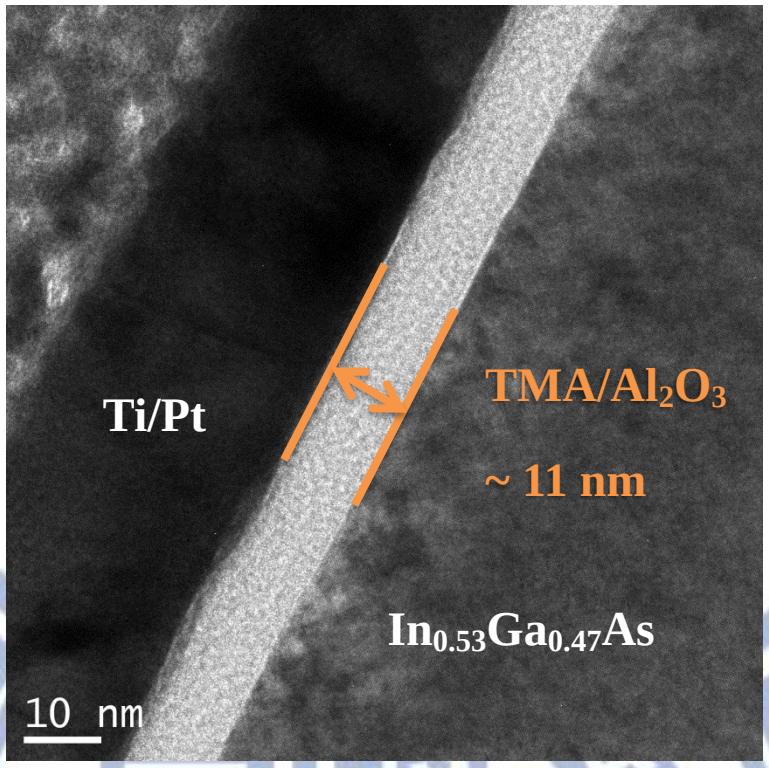


Fig. 2.3 TEM image of the as-deposited ALD-TMA/Al_2O_3 on $In_{0.53}Ga_{0.47}As$ with FGA

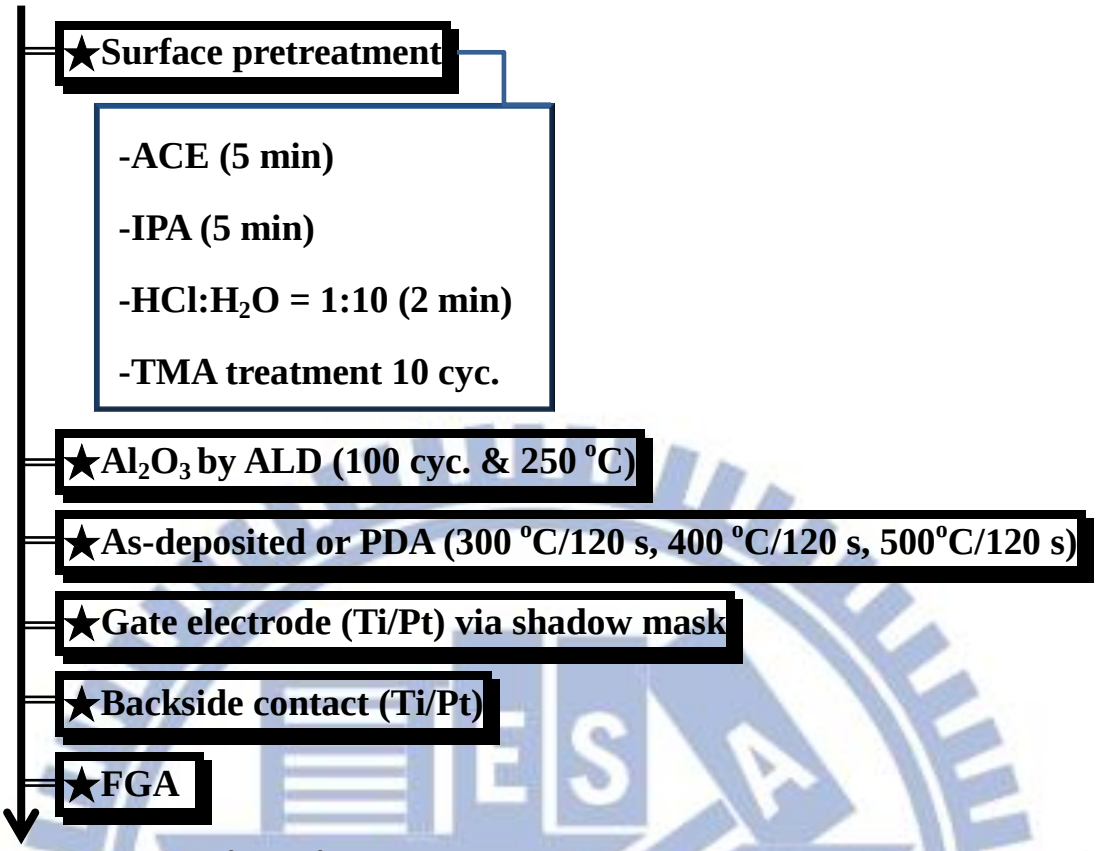


Fig. 2.4 Process flow of (111)A-oriented *p*-$In_{0.53}Ga_{0.47}As$ channel MOSCAPs with different PDA conditions

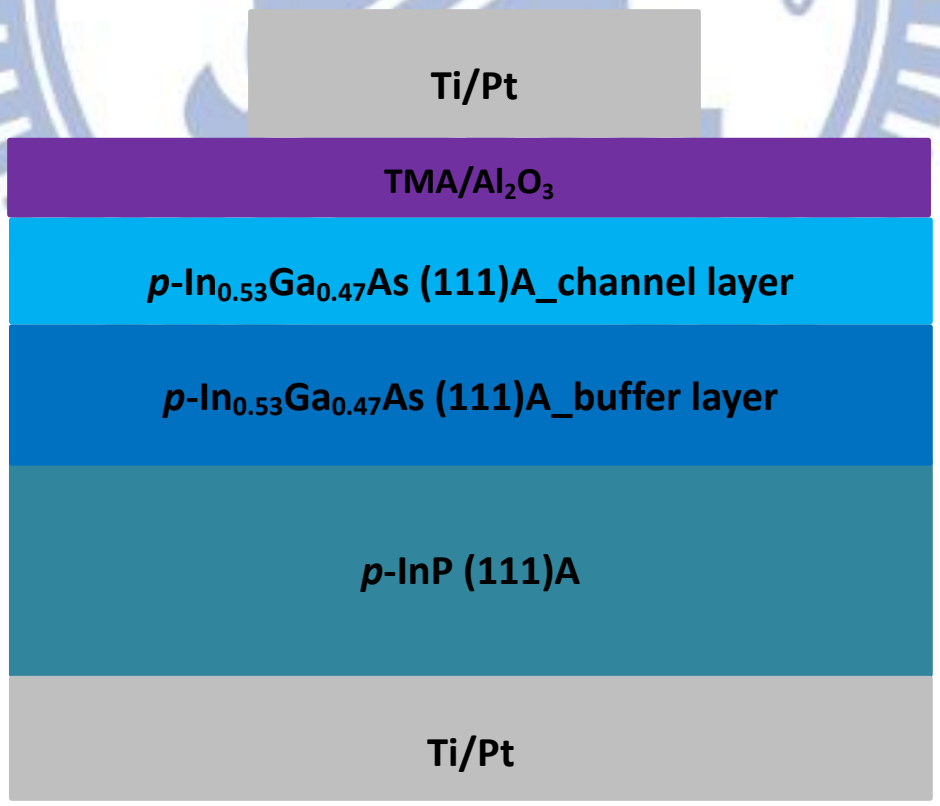
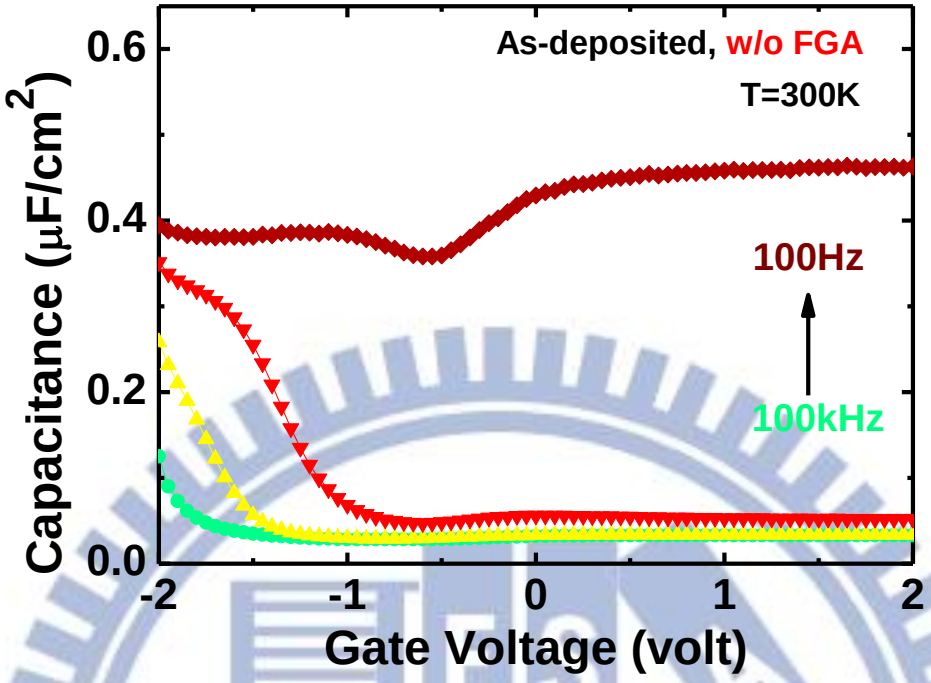
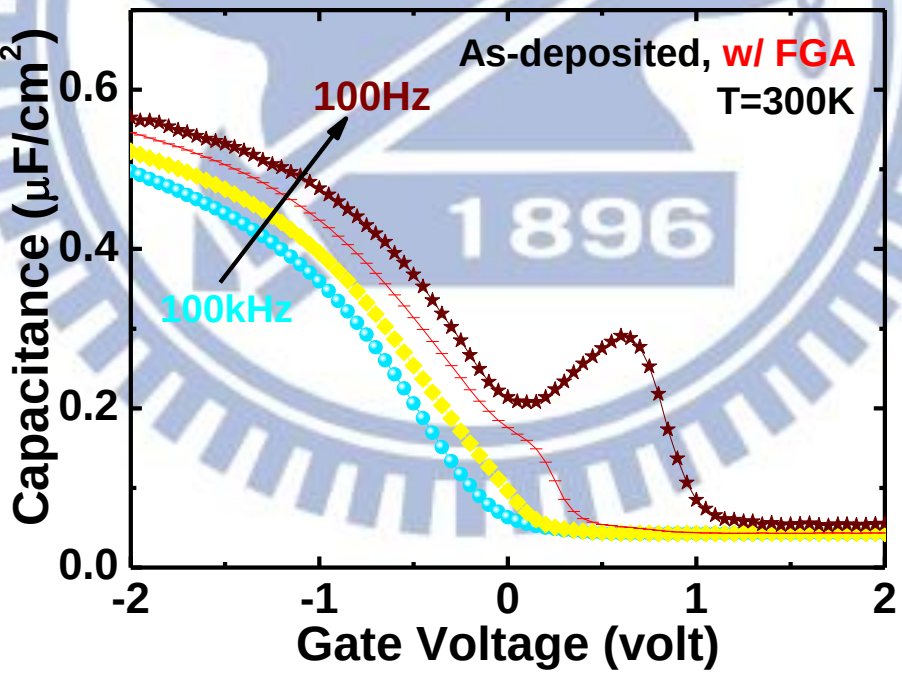


Fig. 2.5 MOSCAPs structure with ALD-TMA/Al_2O_3/$In_{0.53}Ga_{0.47}As$ (111)A



(a)



(c)

Fig. 2.6 Frequency-dependent *C-V* characteristics (100 kHz to 100 Hz, 300K) for *p*-type Pt/Ti/TMA+Al_2O_3/$In_{0.53}Ga_{0.47}As$ (100) MOSCAPs (as-deposited) **(a)** w/o FGA and **(c)** w/ FGA

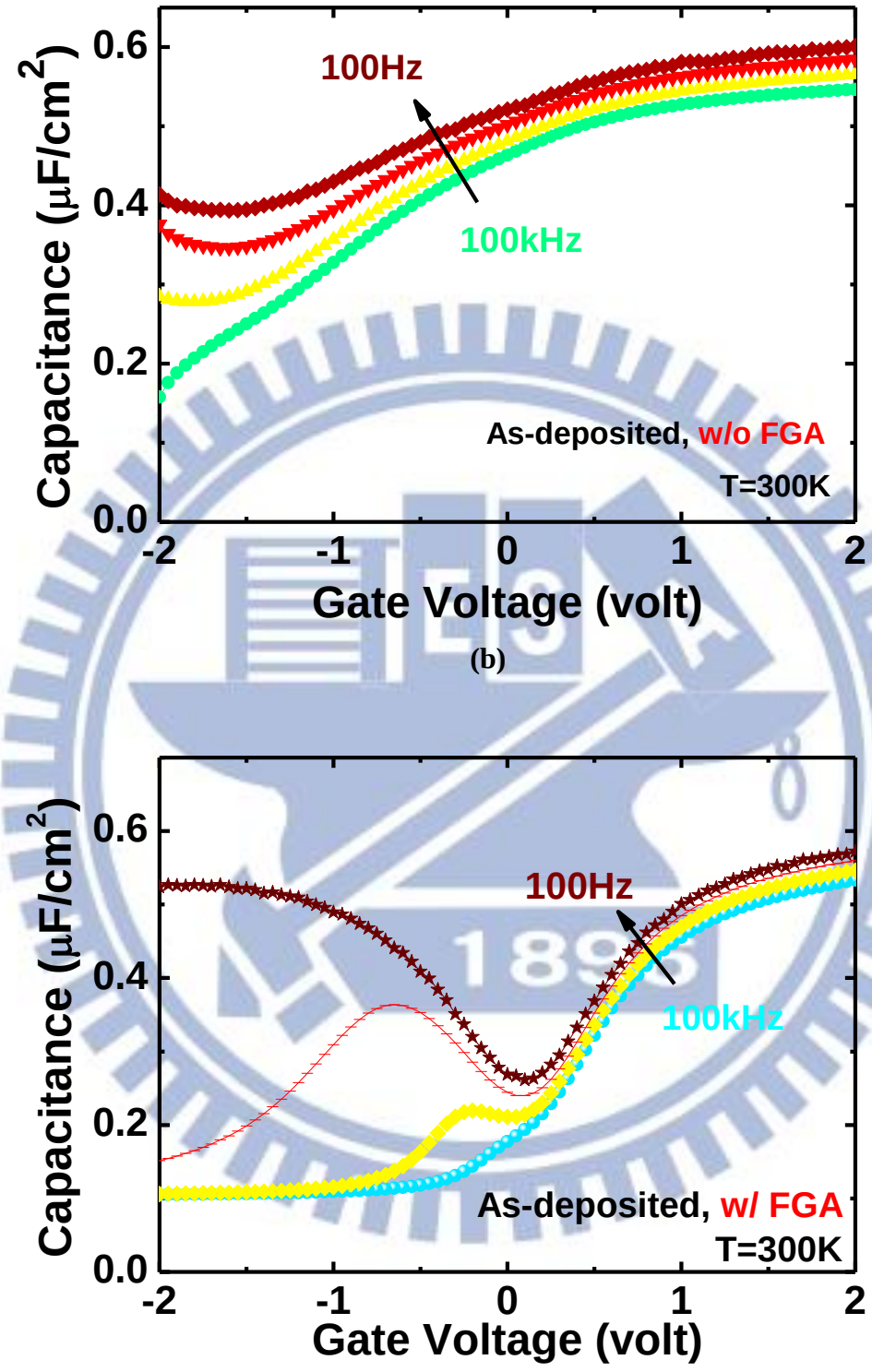
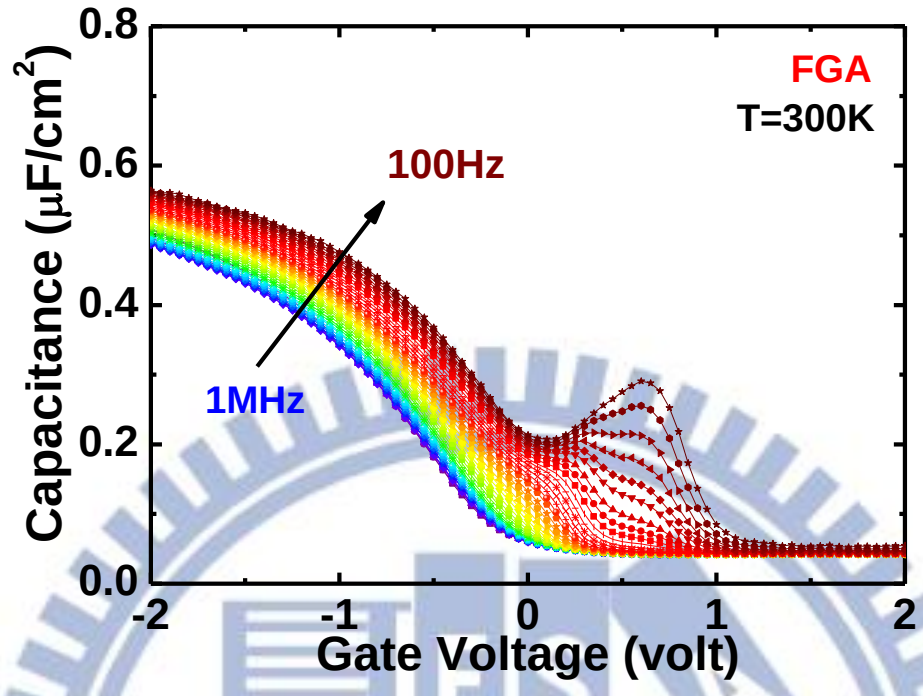
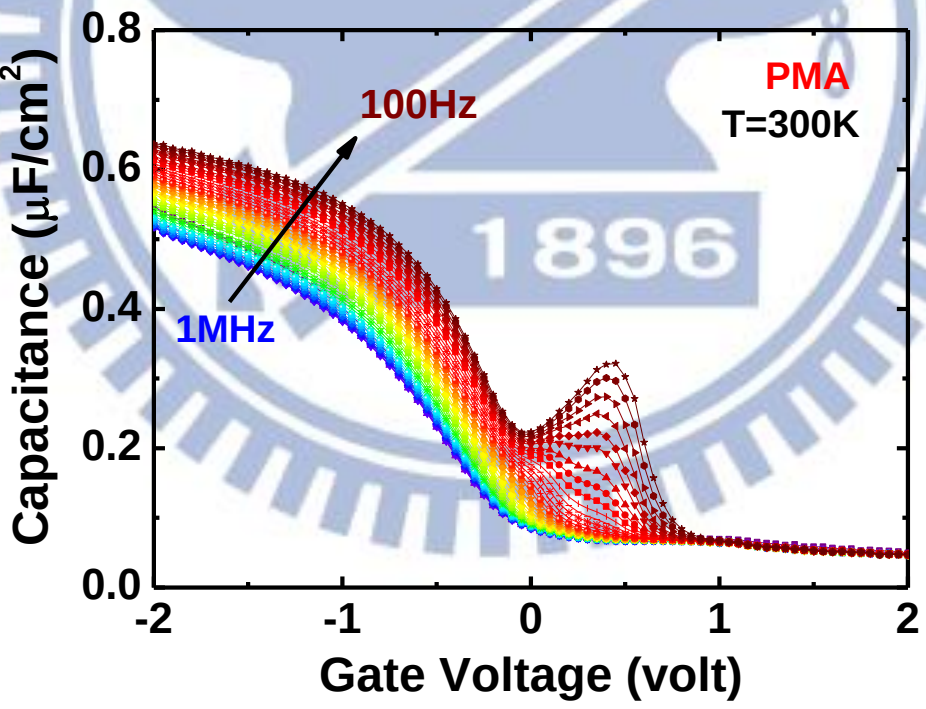


Fig. 2.7 Frequency-dependent *C-V* characteristics (100 kHz to 100 Hz, 300K) for *n*-type Pt/Ti/TMA+Al_2O_3/$In_{0.53}Ga_{0.47}As$ (100) MOSCAPs (as-deposited) **(b)** w/o FGA and **(d)** w/ FGA

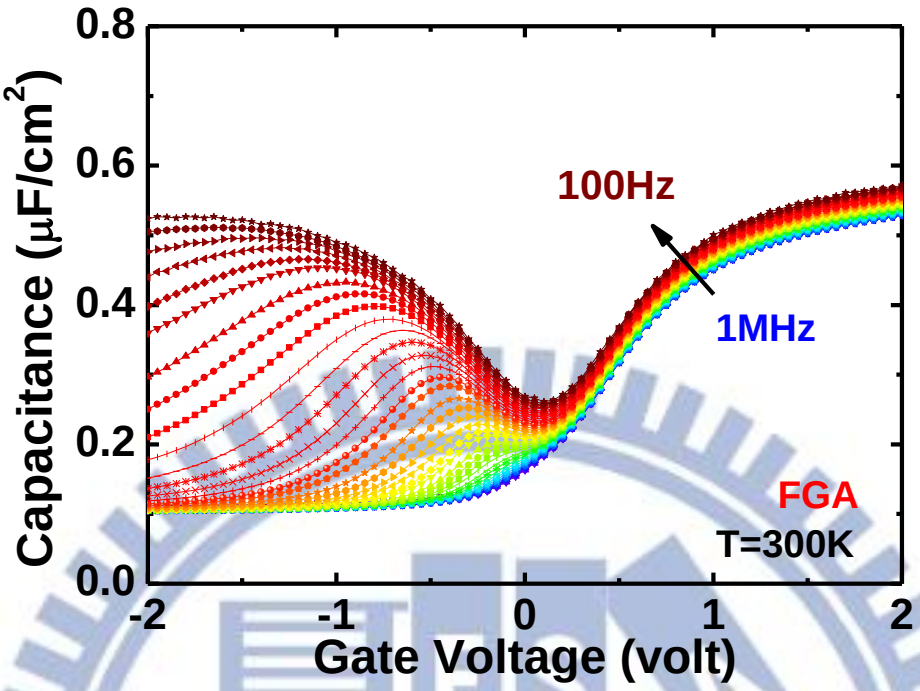


(a)

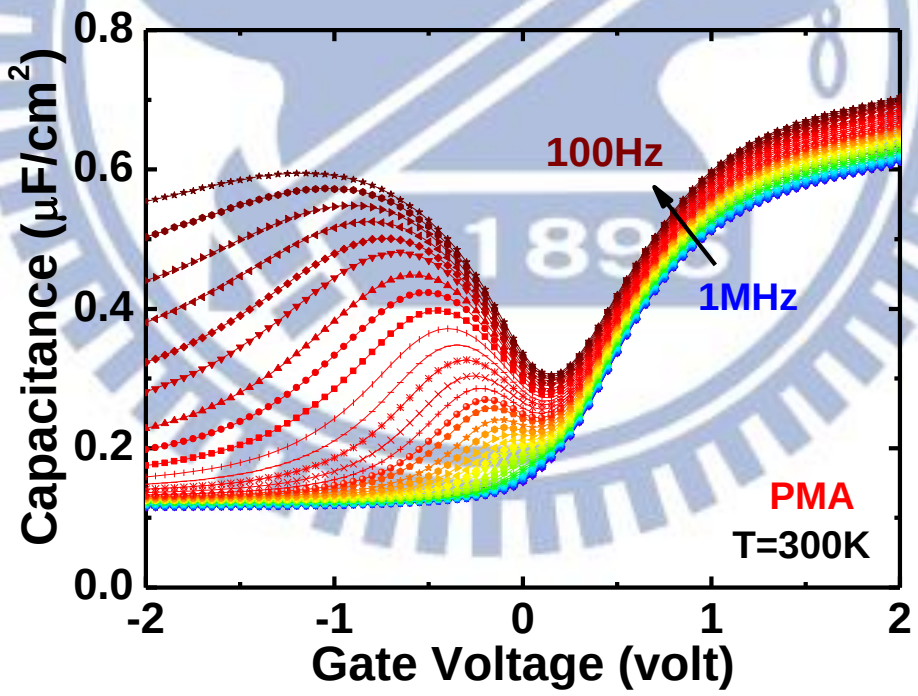


(c)

Fig. 2.8 Multifrequency *C-V* curves (1 MHz to 100 Hz, 300K) for *p*-type Pt/Ti/TMA+Al_2O_3/$In_{0.53}Ga_{0.47}As$ (100) MOSCAPs (as-deposited) with **(a)** FGA and **(c)** PMA

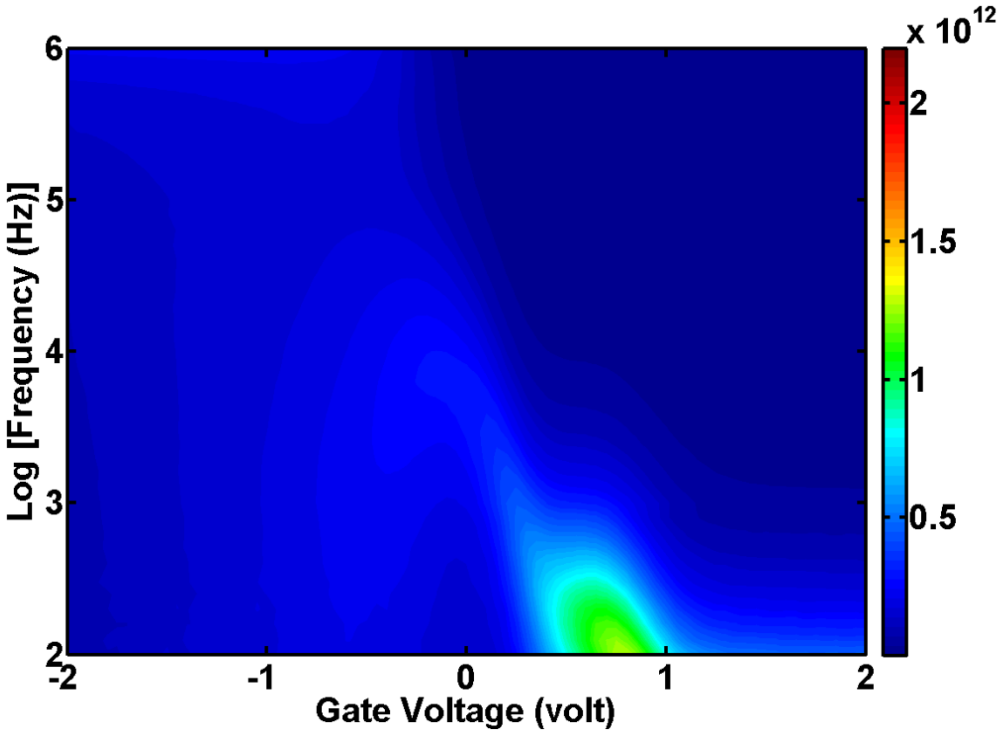


(b)

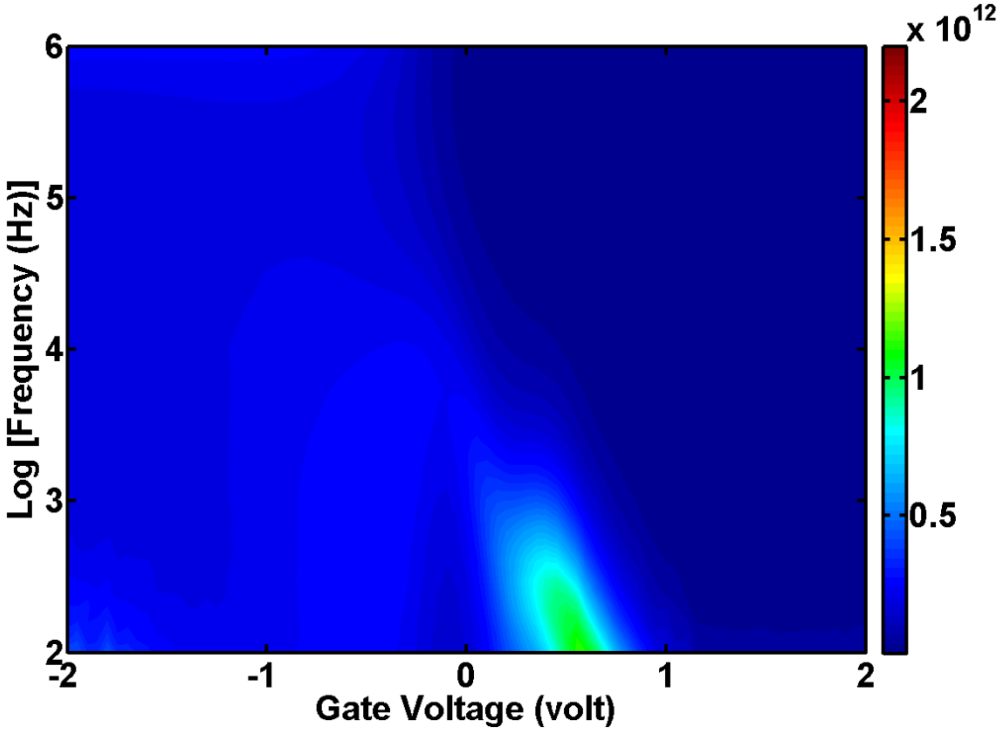


(d)

Fig. 2.9 Multifrequency *C-V* curves (1 MHz to 100 Hz, 300K) for *n*-type Pt/Ti/TMA+Al_2O_3/$In_{0.53}Ga_{0.47}As$ (100) MOSCAPs (as-deposited) with **(b)** FGA and **(d)** PMA

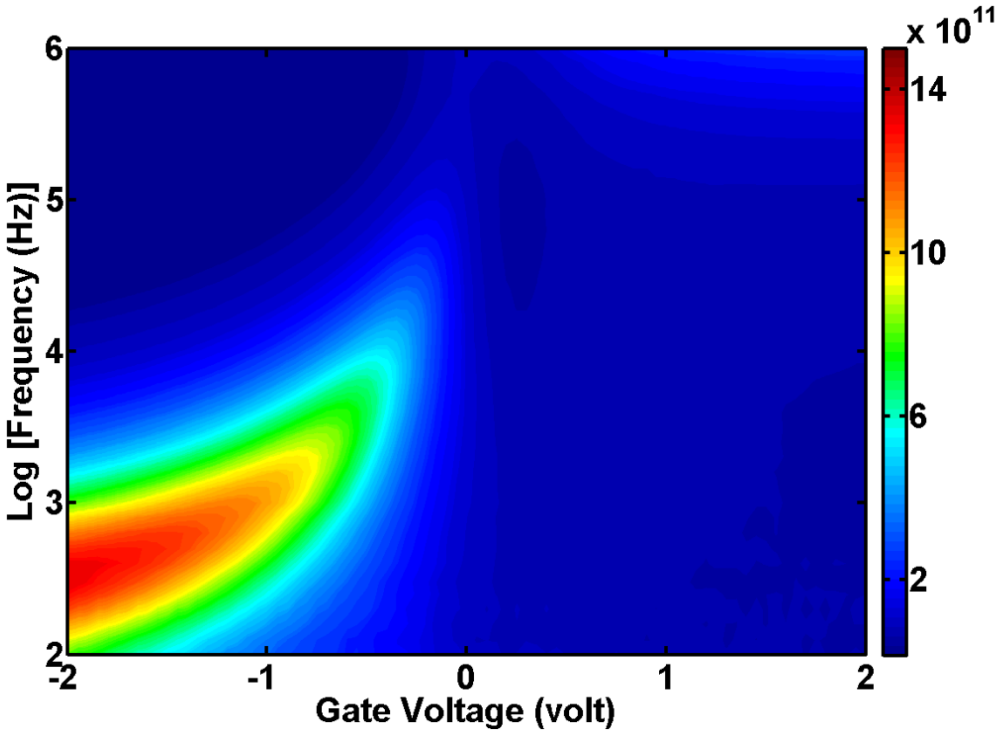


(a)

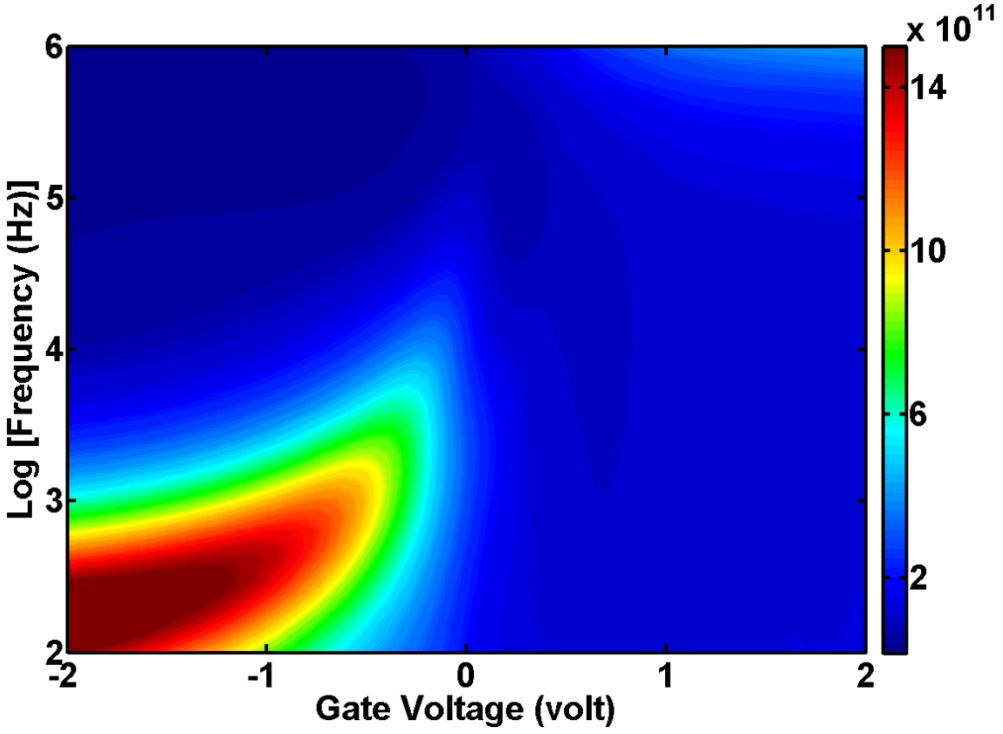


(c)

Fig. 2.10 Map of the normalized conductance, $(G/\omega)/Aq$, as a function of gate bias V_G and frequency f measured at 300K for MOSCAPs with Al_2O_3 (as-deposited) on p-type $In_{0.53}Ga_{0.47}As$ (100) after **(a)** FGA and **(c)** PMA



(b)



(d)

Fig. 2.11 Map of the normalized conductance, $(G/\omega)/Aq$, as a function of gate bias V_G and frequency f measured at 300K for MOSCAPs with Al_2O_3 (as-deposited) on n-type $In_{0.53}Ga_{0.47}As$ (100) after **(b)** FGA and **(d)** PMA

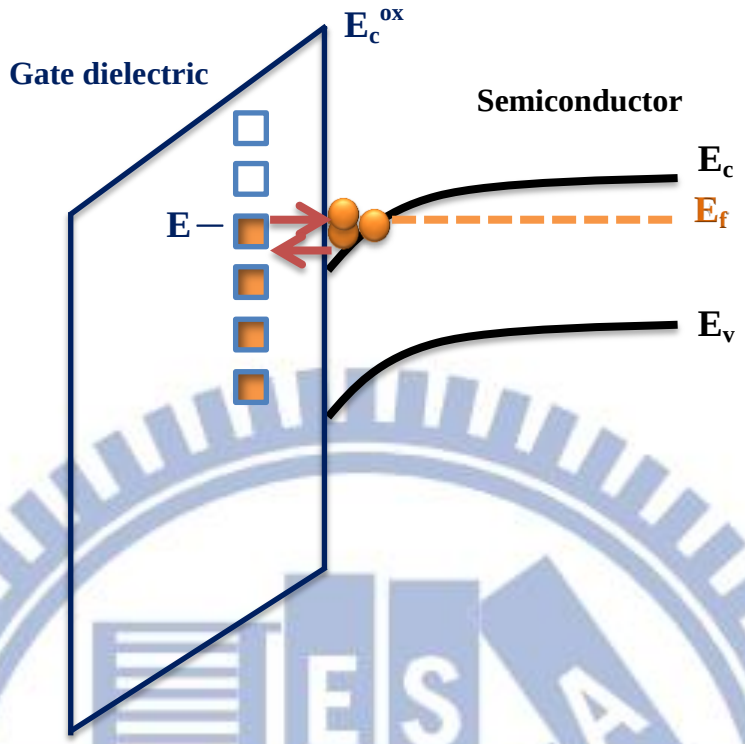


Fig. 2.12 Schematic diagram of tunneling between border traps in gate dielectric and conduction band of semiconductor

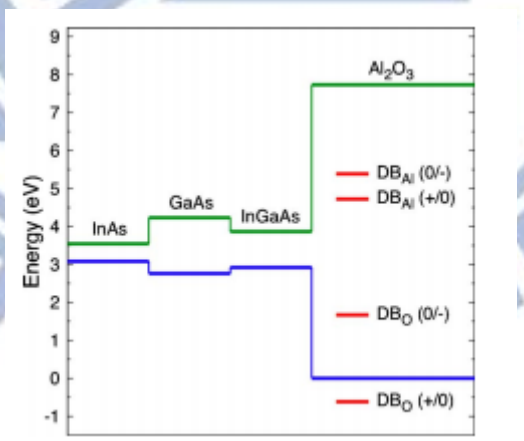
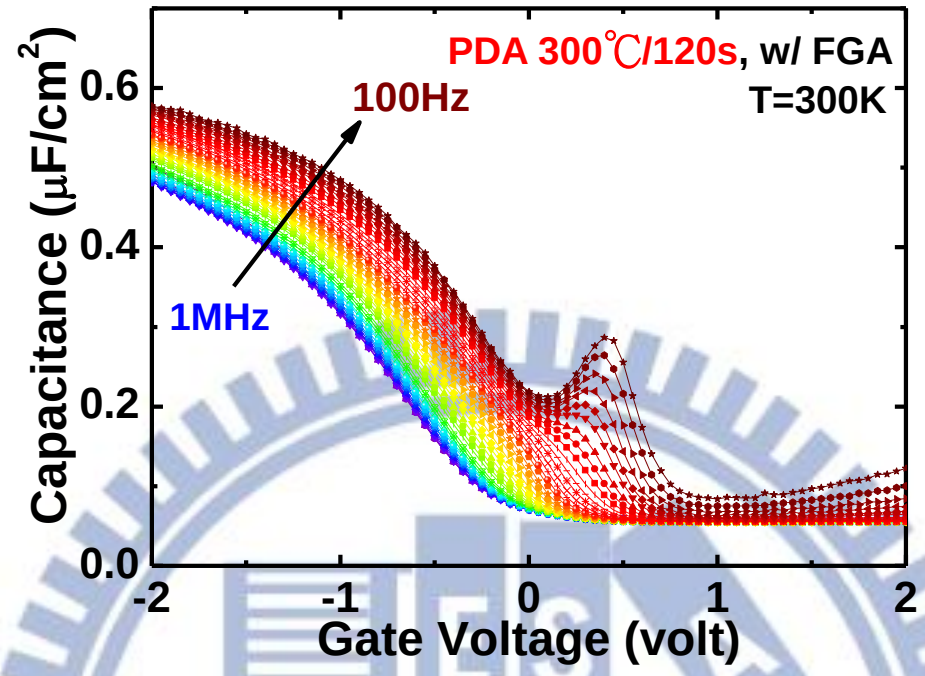
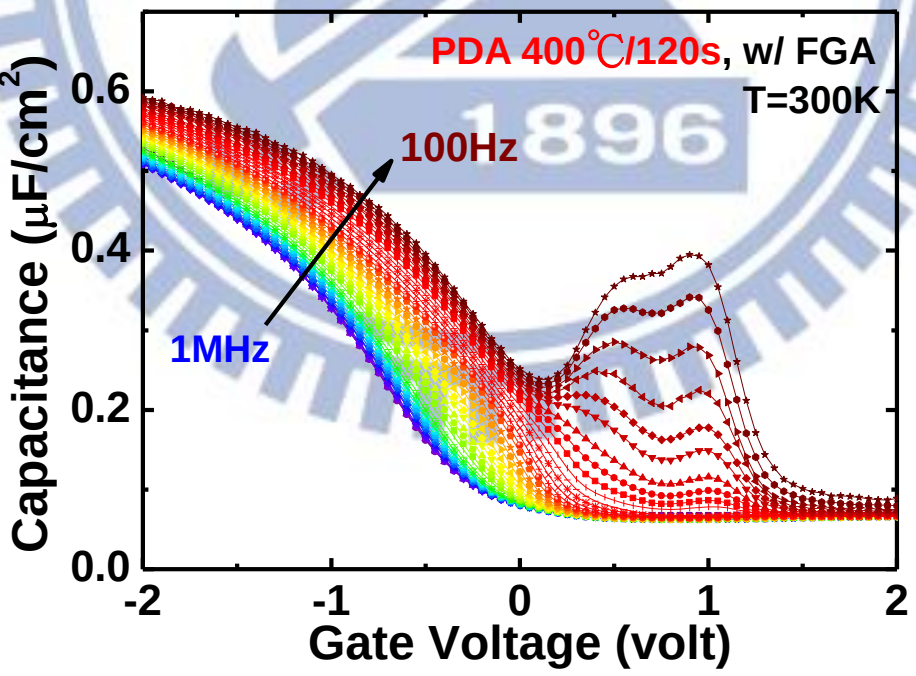


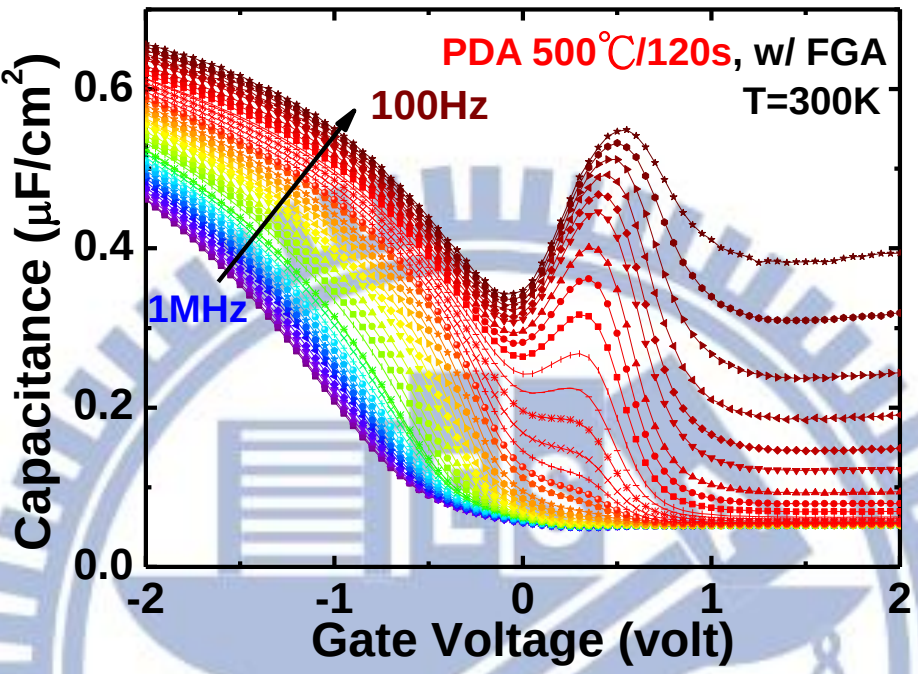
Fig. 2.13 Band alignment between Al_2O_3 and common III-V compound semiconductors, and position of charge-state transition levels for dangling bonds in the oxide


PDA 300℃/120s, w/ FGA
T=300K
100Hz
1MHz
Capacitance (μF/cm²)
0.0
0.2
0.4
0.6
-2
-1
0
1
2
Gate Voltage (volt)

(a)

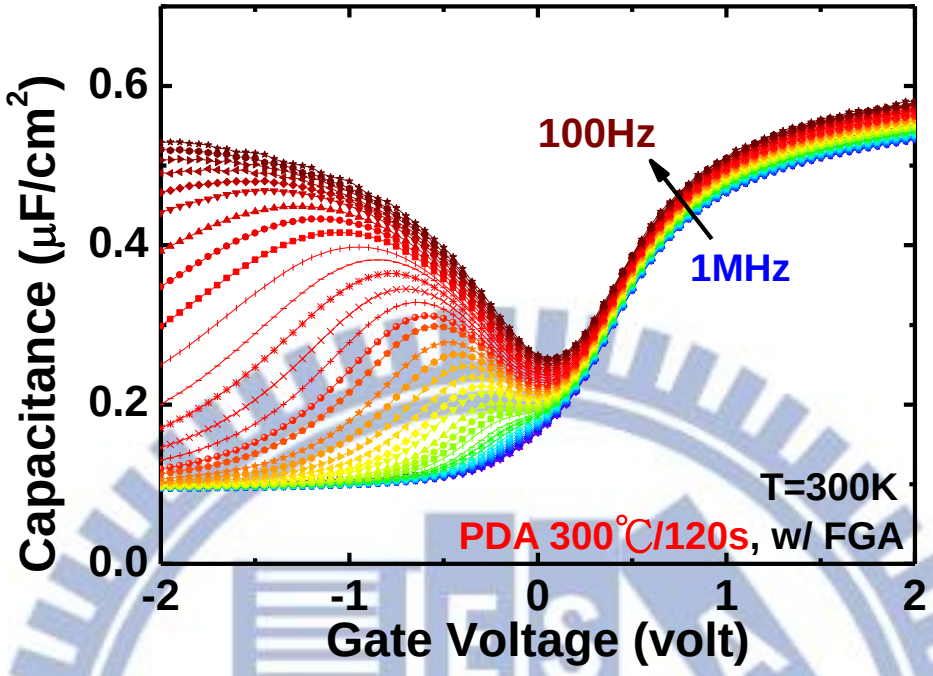

PDA 400℃/120s, w/ FGA
T=300K
100Hz
1MHz
Capacitance (μF/cm²)
0.0
0.2
0.4
0.6
-2
-1
0
1
2
Gate Voltage (volt)

(b)

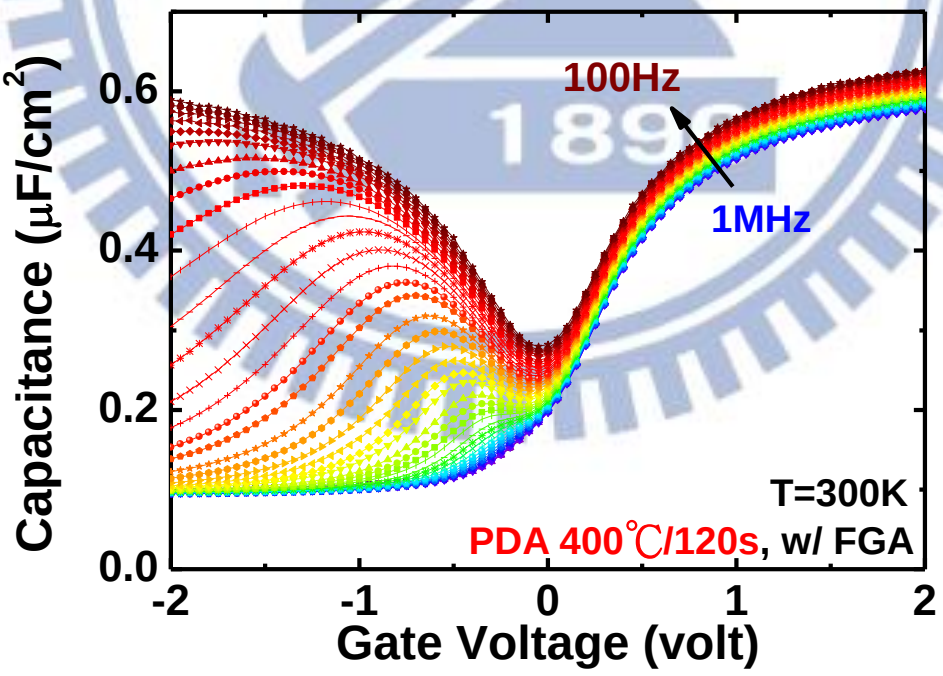


(c)

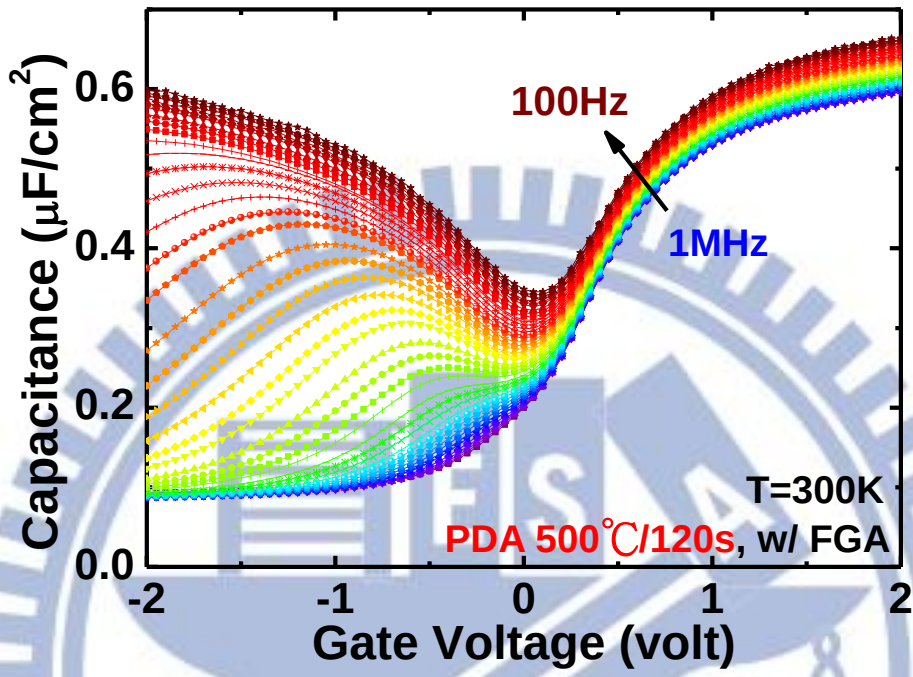
Fig. 2.14 Multifrequency *C-V* curves (1 MHz to 100 Hz, 300K) for *p*-type Pt/Ti/TMA+Al_2O_3/$In_{0.53}Ga_{0.47}As$ (100) MOSCAPs after post-metallization FGA under different PDA conditions in N_2 ambience for 120 s **(a)** 300 ^oC **(b)** 400 ^oC **(c)** 500 ^oC


Capacitance (μF/cm²)
0.0
0.2
0.4
0.6
-2
-1
0
1
2
Gate Voltage (volt)
100Hz
1MHz
T=300K
PDA 300℃/120s, w/ FGA

(a)

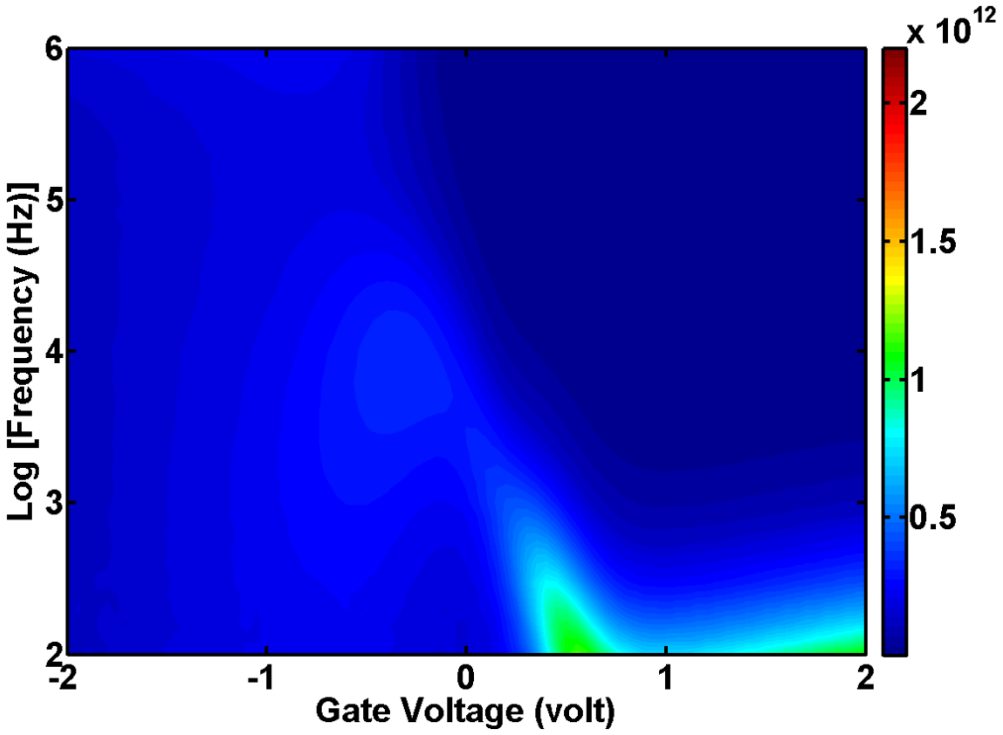

Capacitance (μF/cm²)
0.0
0.2
0.4
0.6
-2
-1
0
1
2
Gate Voltage (volt)
100Hz
1MHz
T=300K
PDA 400℃/120s, w/ FGA

(b)

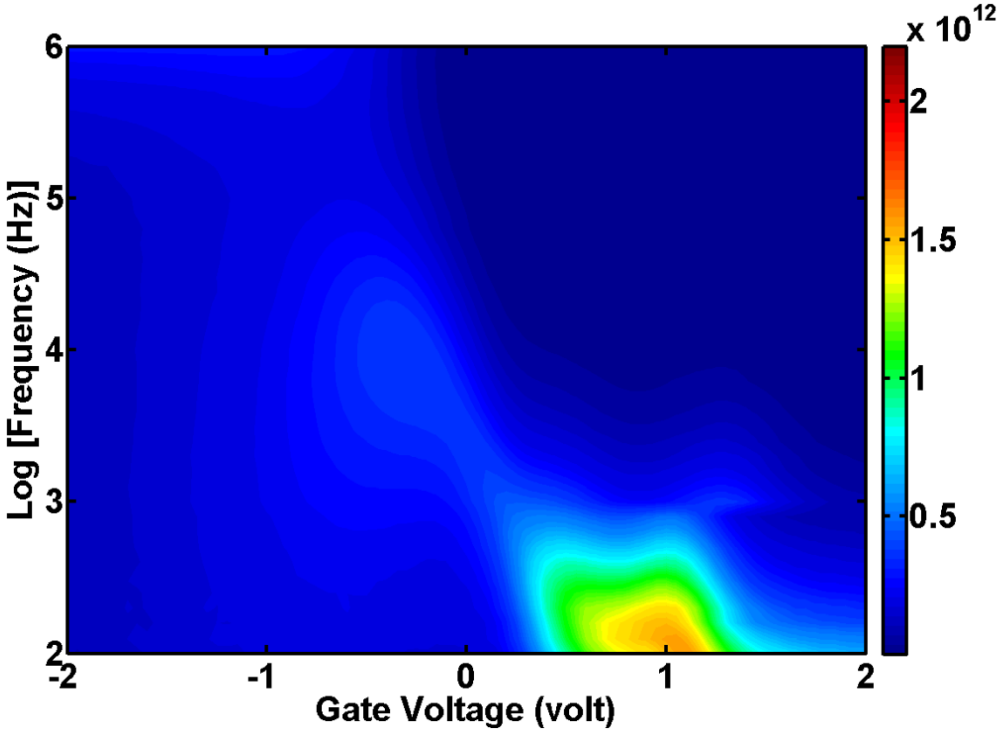


(c)

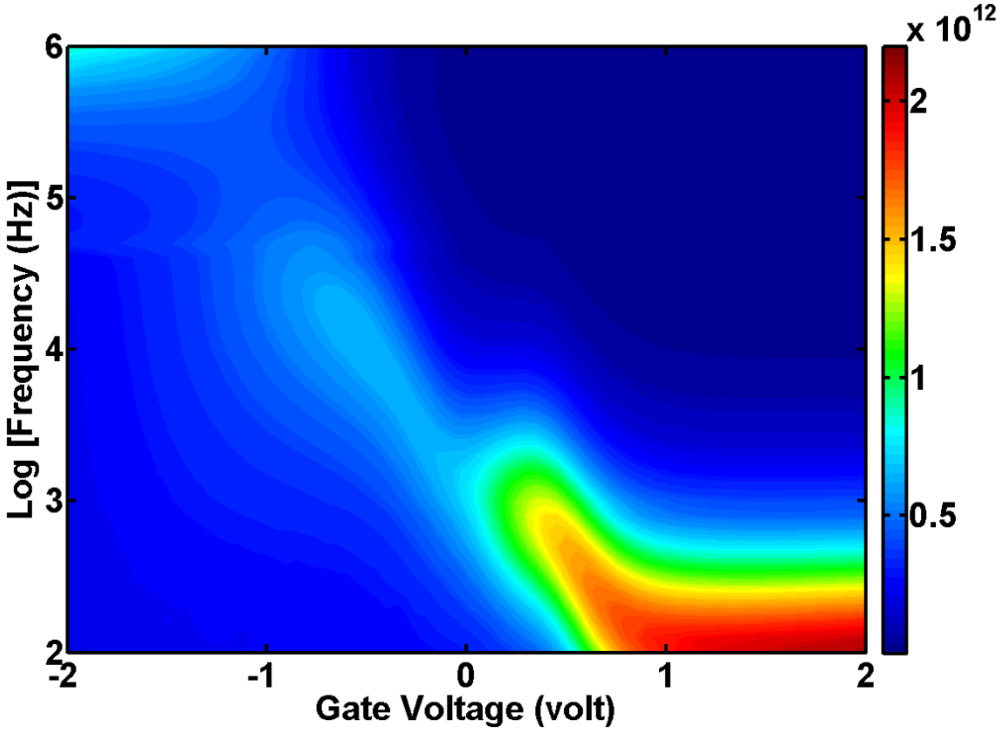
Fig. 2.15 Multifrequency *C-V* curves (1 MHz to 100 Hz, 300K) for *n*-type Pt/Ti/TMA+Al_2O_3/$In_{0.53}Ga_{0.47}As$ (100) MOSCAPs after post-metallization FGA under different PDA conditions in N_2 ambience for 120 s **(a)** 300 ^oC **(b)** 400 ^oC **(c)** 500 ^oC


x 10^12
2
1.5
1
0.5
6
5
4
3
2
Log [Frequency (Hz)]
-2
-1
0
1
2
Gate Voltage (volt)

(a)

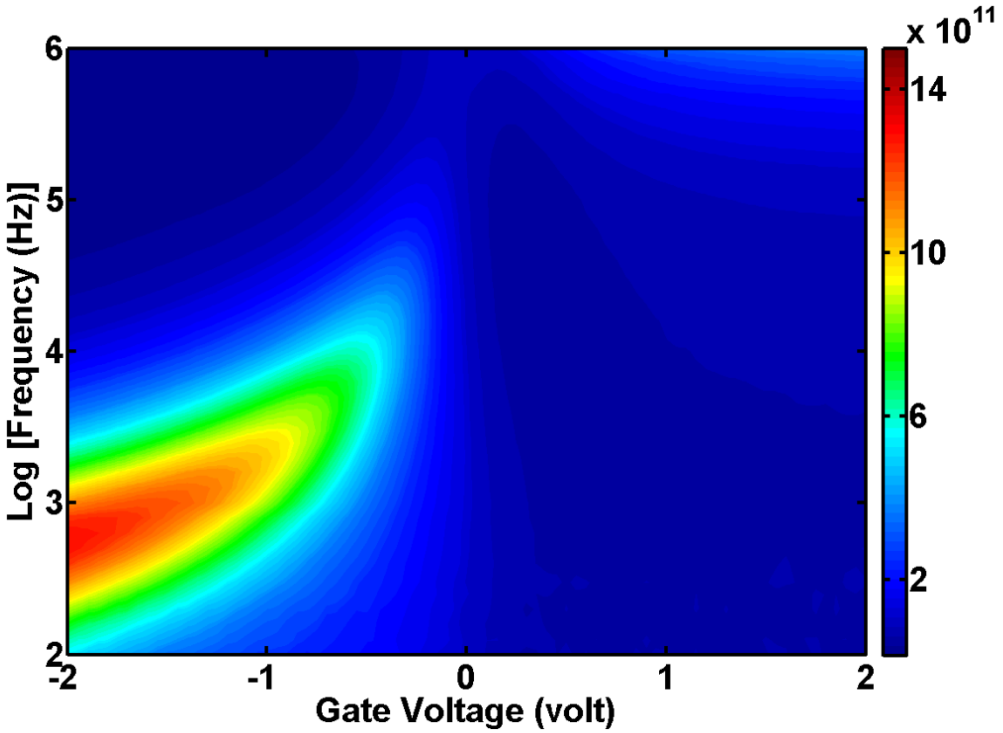

x 10^12
2
1.5
1
0.5
6
5
4
3
2
Log [Frequency (Hz)]
-2
-1
0
1
2
Gate Voltage (volt)

(b)

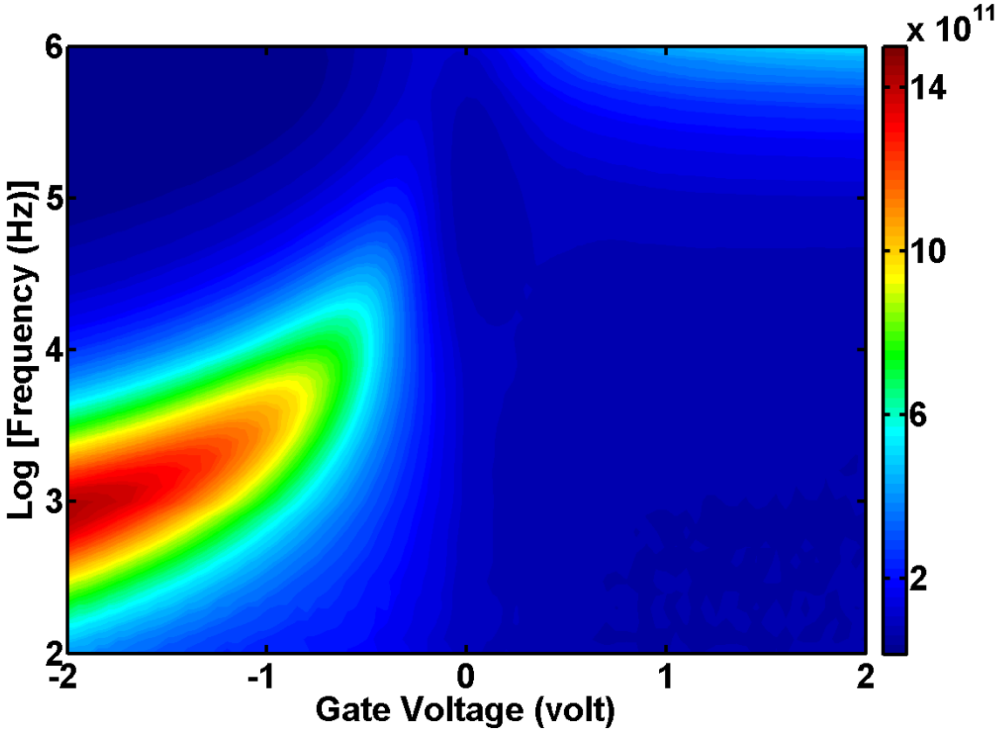


(c)

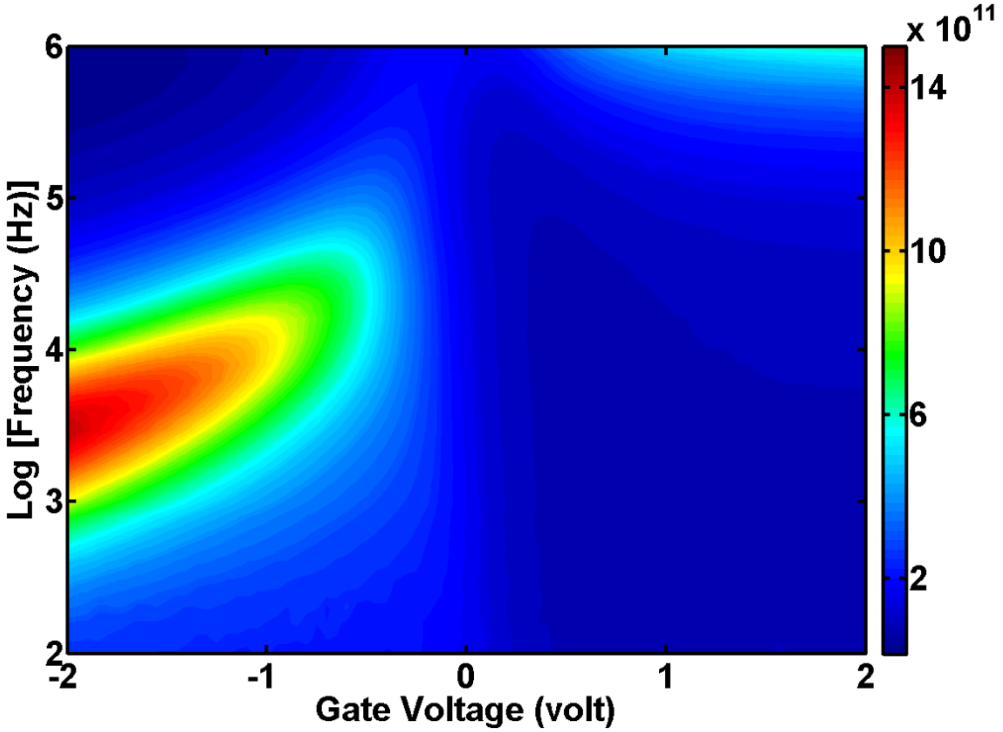
Fig. 2.16 Map of the normalized conductance, $(G/\omega)/Aq$, as a function of gate bias V_G and frequency f measured at 300K for MOSCAPs with ALD-TMA/Al_2O_3 on p-type $In_{0.53}Ga_{0.47}As$ (100) after post-metallization FGA under different PDA conditions in N_2 ambience for 120 s **(a)** 300 ^oC **(b)** 400 ^oC **(c)** 500 ^oC


x 10^11
14
10
6
2
Log [Frequency (Hz)]
6
5
4
3
2
-2
-1
0
1
2
Gate Voltage (volt)

(a)

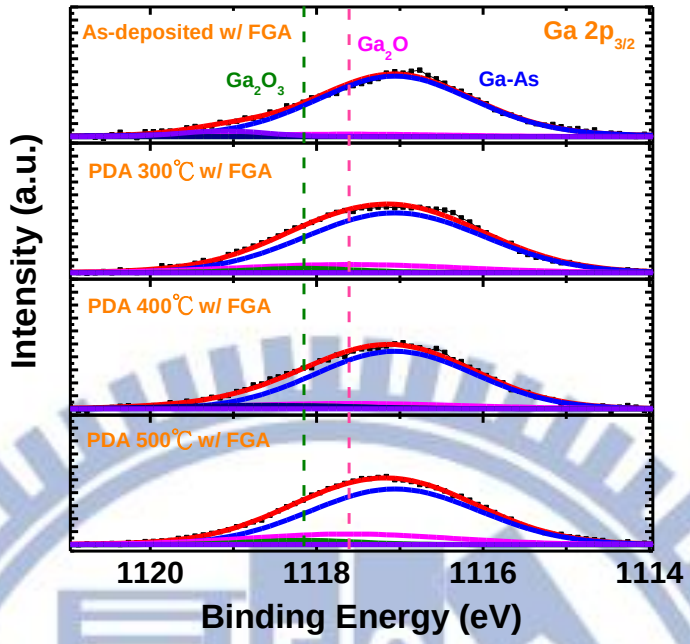

x 10^11
14
10
6
2
Log [Frequency (Hz)]
6
5
4
3
2
-2
-1
0
1
2
Gate Voltage (volt)

(b)

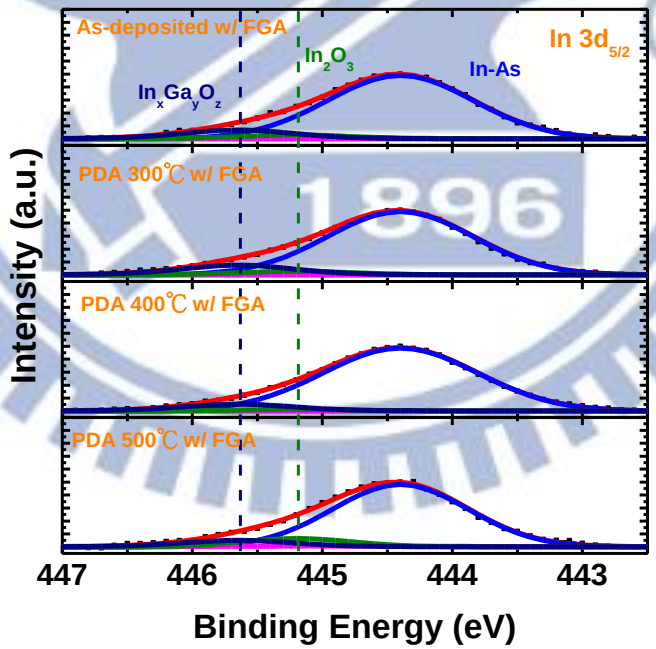


(c)

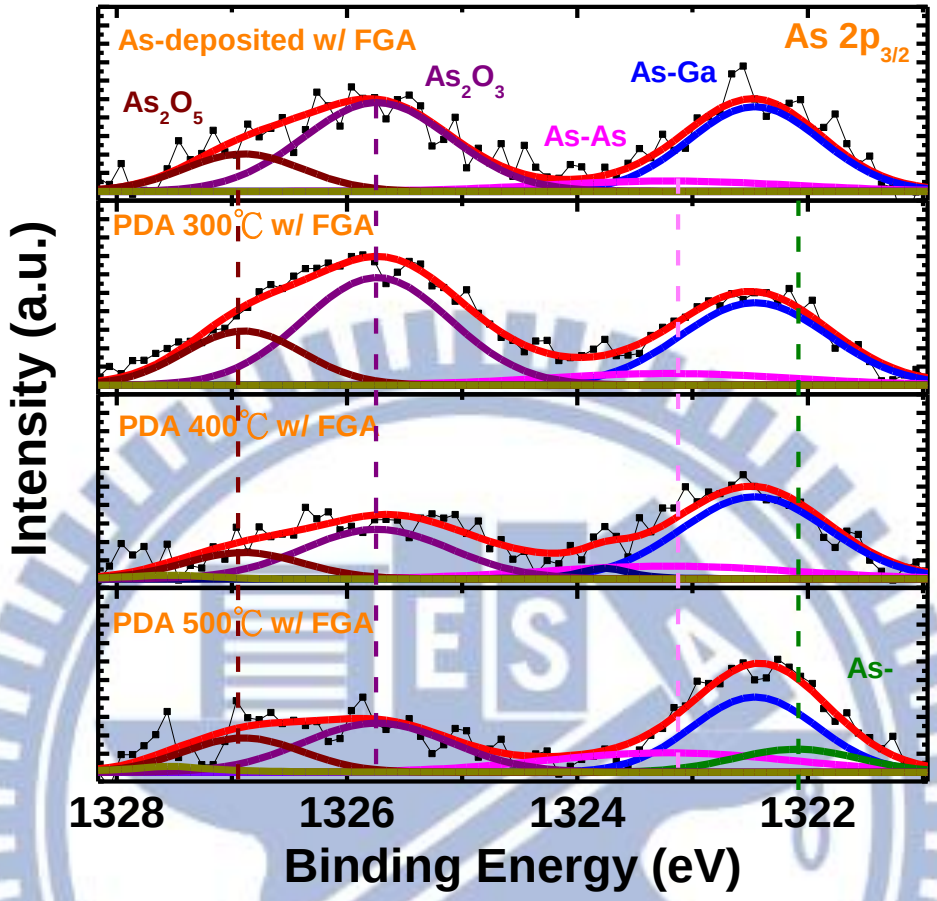
Fig. 2.17 Map of the normalized conductance, $(G/\omega)/Aq$, as a function of gate bias V_G and frequency f measured at 300K for MOSCAPs with ALD-TMA/Al_2O_3 on n-type $In_{0.53}Ga_{0.47}As$ (100) after post-metallization FGA under different PDA conditions in N_2 ambience for 120 s **(a)** 300 ^oC **(b)** 400 ^oC **(c)** 500 ^oC


As-deposited w/ FGA
Ga 2p3/2
Ga2O
Ga2O3
Ga-As
PDA 300℃ w/ FGA
PDA 400℃ w/ FGA
PDA 500℃ w/ FGA
Intensity (a.u.)
1120
1118
1116
1114
Binding Energy (eV)

(a)

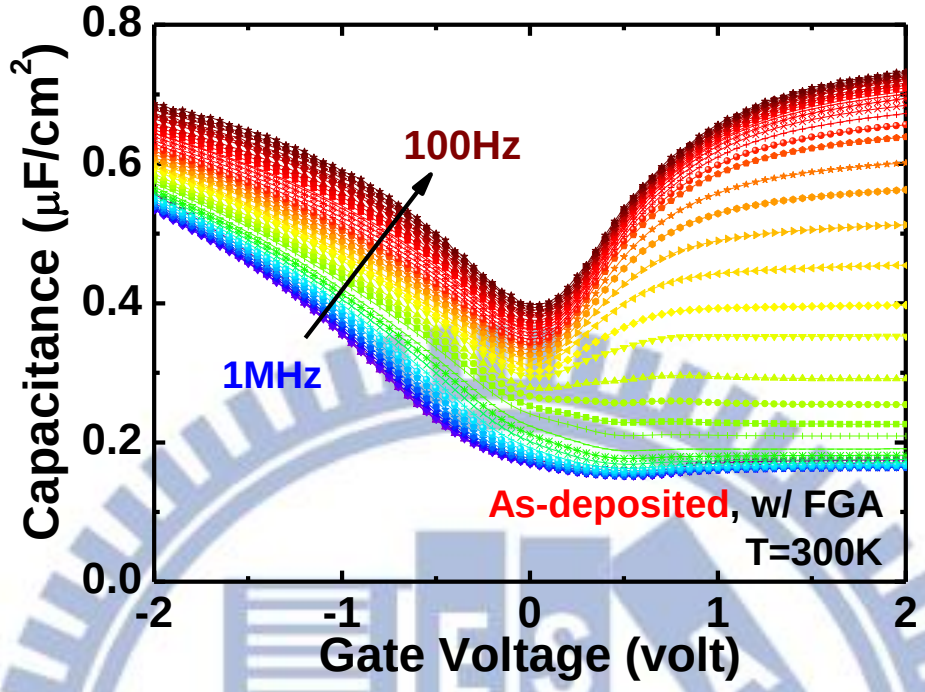

As-deposited w/ FGA
In 3d5/2
In2O3
In-As
InxGayOz
PDA 300℃ w/ FGA
PDA 400℃ w/ FGA
PDA 500℃ w/ FGA
Intensity (a.u.)
447
446
445
444
443
Binding Energy (eV)

(b)

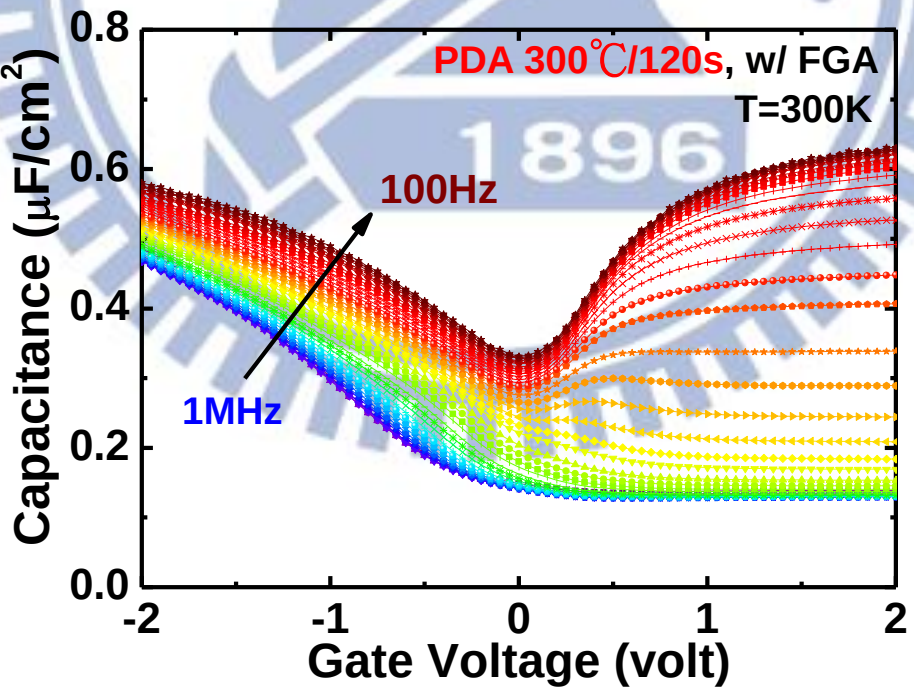


(c)

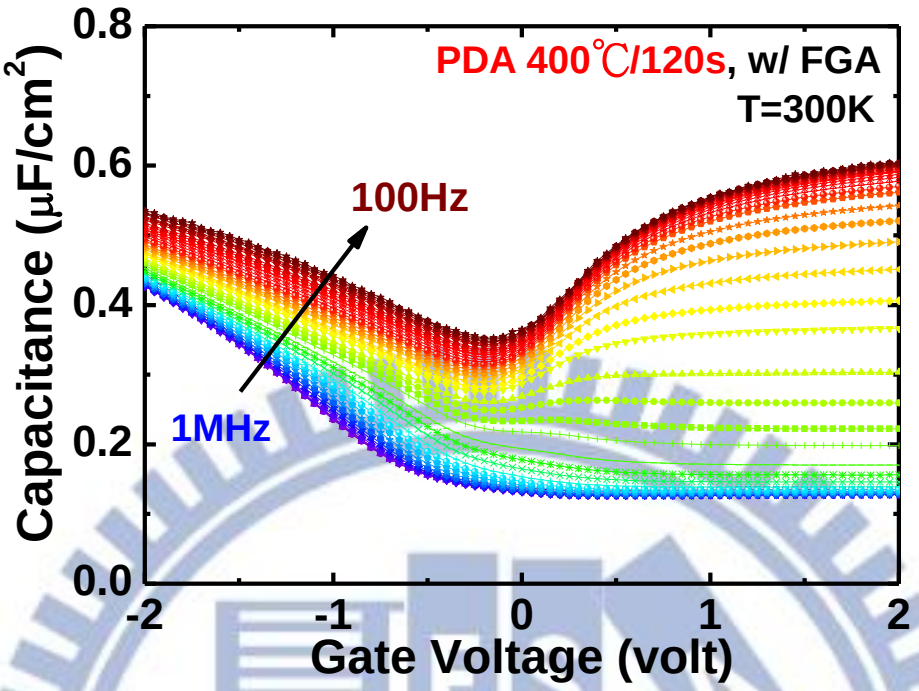
Fig. 2.18 X-ray photoelectron spectroscopy of ALD-TMA (10 cycles)/Al_2O_3 (10 cycles) on (100)-oriented $In_{0.53}Ga_{0.47}As$ with post-metallization FGA under various PDA conditions **(a)** Ga $2p_{3/2}$ **(b)** In $3d_{5/2}$ **(c)** As $2p_{3/2}$


0.8
0.6
0.4
0.2
0.0
Capacitance (μF/cm²)
100Hz
1MHz
As-deposited, w/ FGA
T=300K
-2
-1
0
1
2
Gate Voltage (volt)

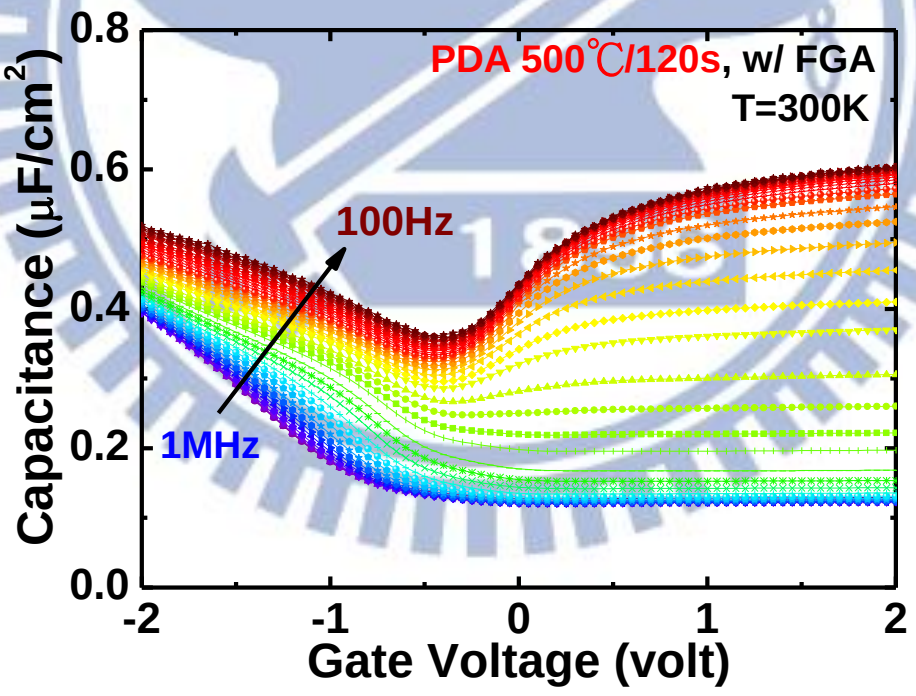
(a)


0.8
0.6
0.4
0.2
0.0
Capacitance (μF/cm²)
PDA 300℃/120s, w/ FGA
T=300K
100Hz
1MHz
-2
-1
0
1
2
Gate Voltage (volt)

(b)



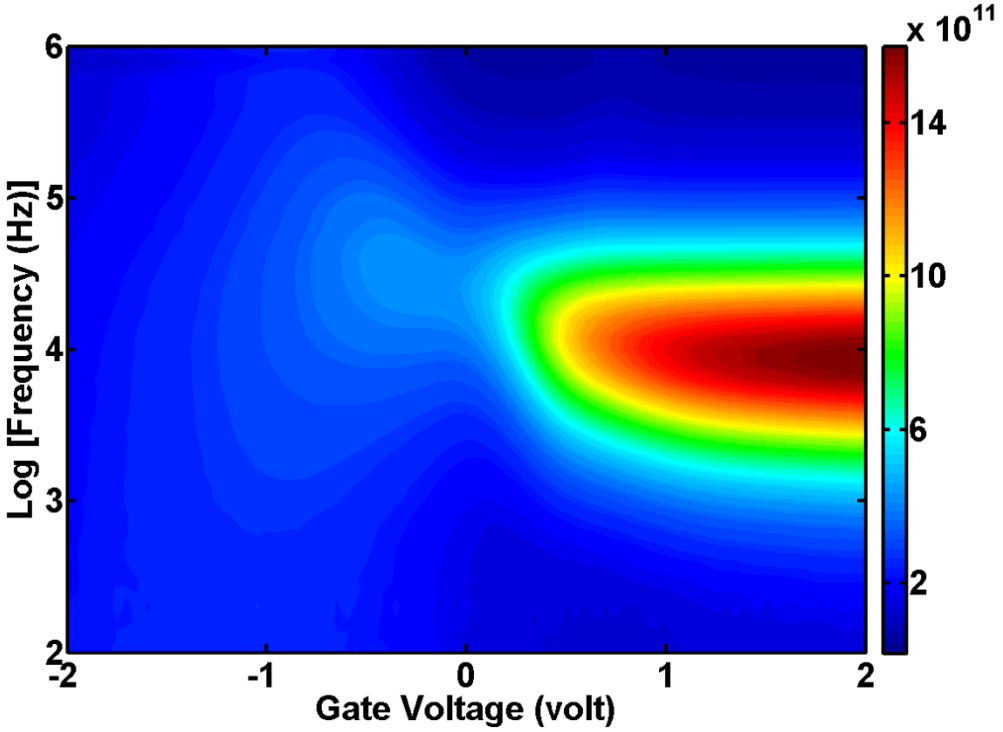
(c)



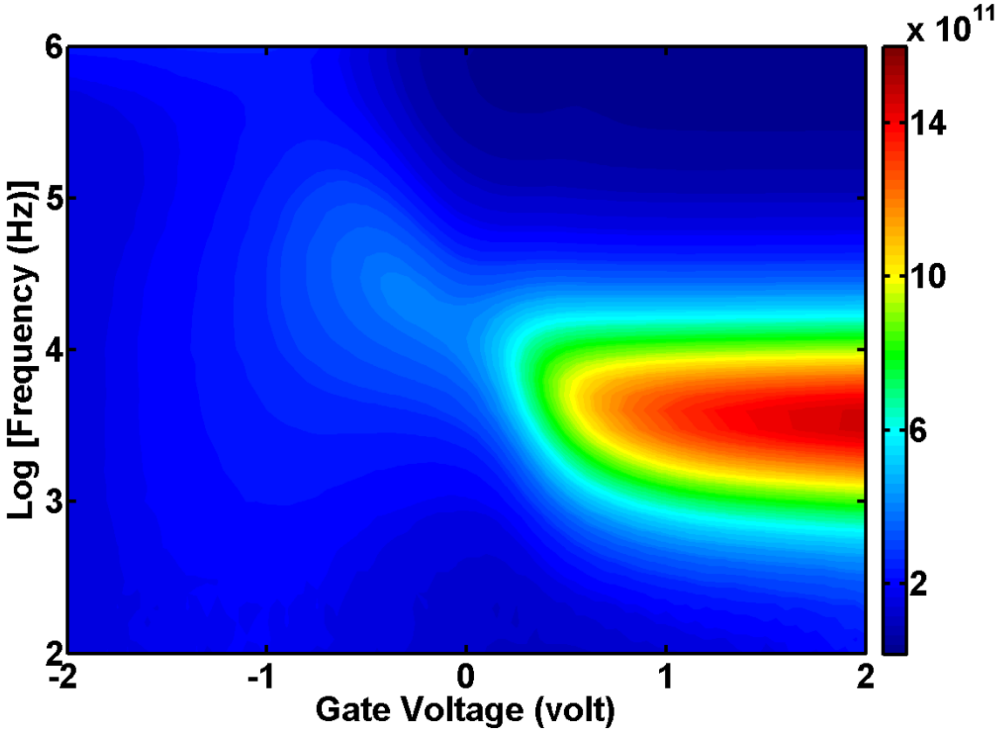
(d)

Fig. 2.19 Multifrequency *C-V* curves (1 MHz to 100 Hz, 300K) for *p*-type Pt/Ti/TMA+Al_2O_3/$In_{0.53}Ga_{0.47}As$ (111)A MOSCAPs after

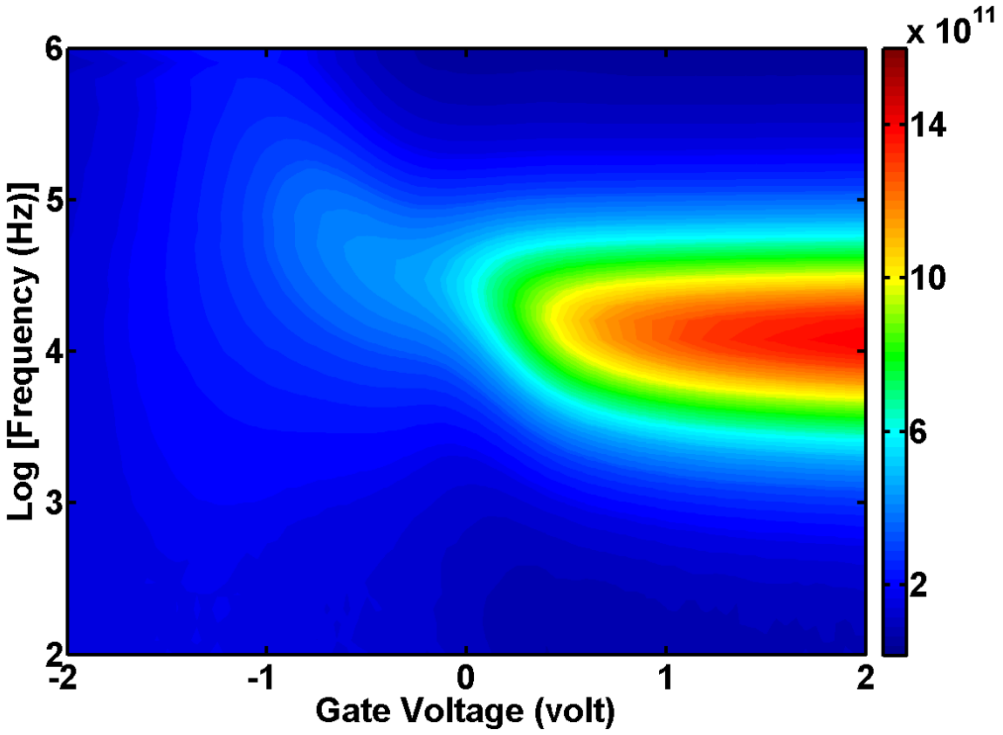
post-metallization FGA under different PDA conditions in N_2 ambience for 120 s **(a)** as-deposited **(b)** 300 ^{o}C **(c)** 400 ^{o}C **(d)** 500 ^{o}C



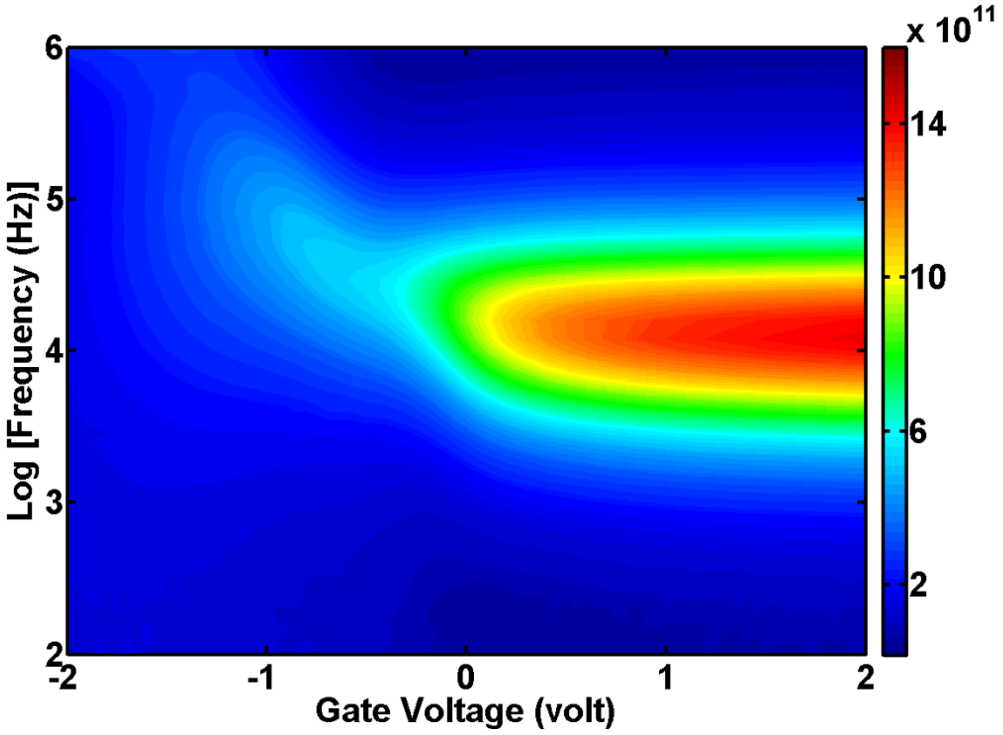
(a)



(b)



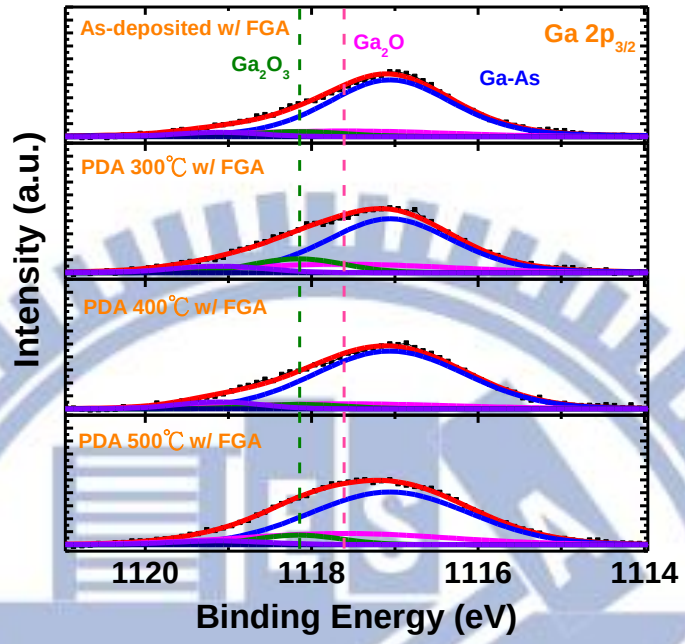
(c)



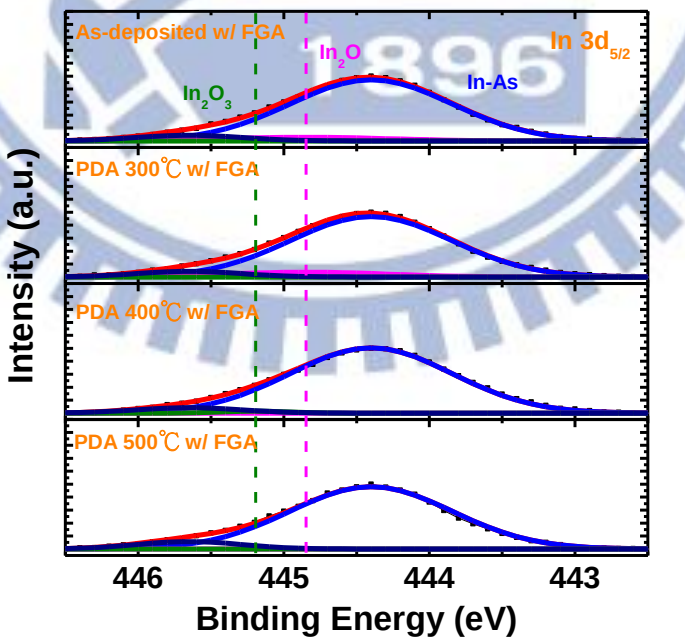
(d)

Fig. 2.20 Map of the normalized conductance, $(G/\omega)/Aq$, as a function of gate bias V_G and frequency f measured at 300K for MOSCAPs with ALD-TMA/Al_2O_3 on p-type $In_{0.53}Ga_{0.47}As$ (111)A after post-metallization FGA under different

PDA conditions in N_2 ambience for 120 s **(a)** as-deposited **(b)** 300 ^{o}C **(c)** 400 ^{o}C **(d)** 500 ^{o}C



(a)



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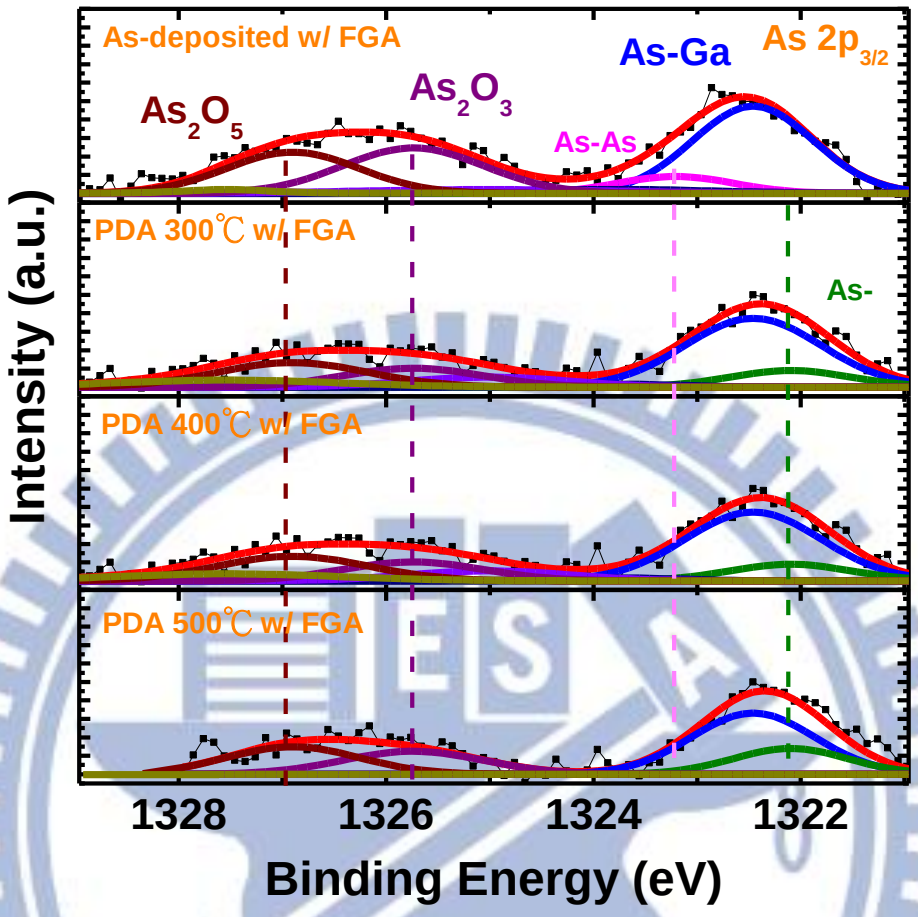


(c)

Fig. 2.21 X-ray photoelectron spectroscopy of ALD-TMA (10 cycles)/Al_2O_3 (10 cycles) on (111)A-oriented $In_{0.53}Ga_{0.47}As$ with post-metallization FGA under various PDA conditions **(a)** Ga $2p_{3/2}$ **(b)** In $3d_{5/2}$ **(c)** As $2p_{3/2}$

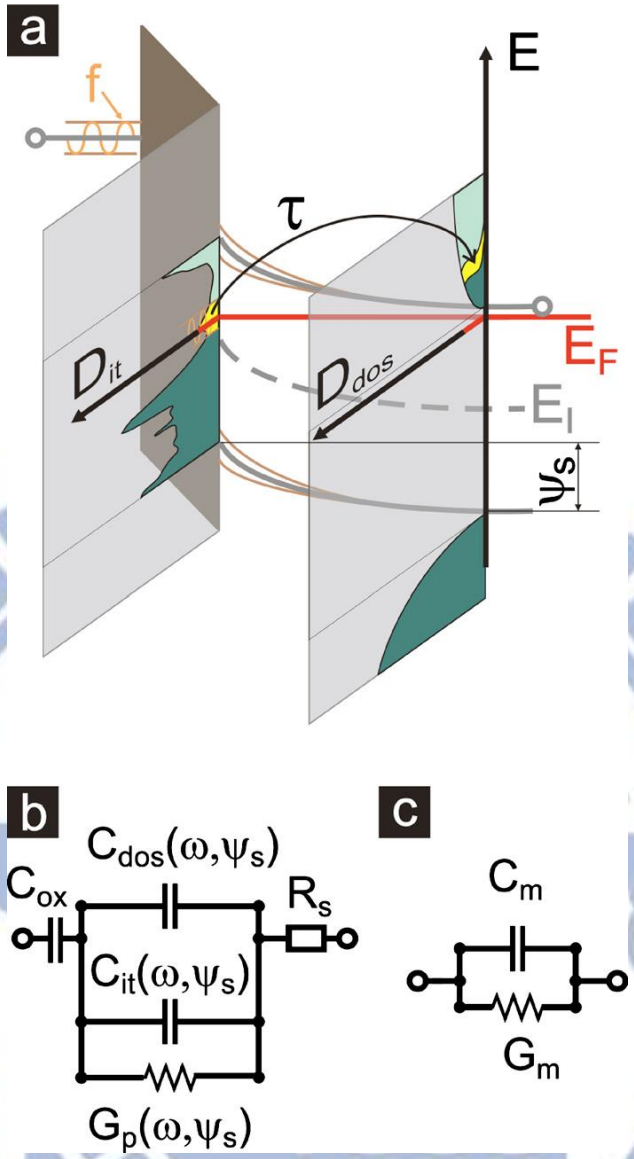
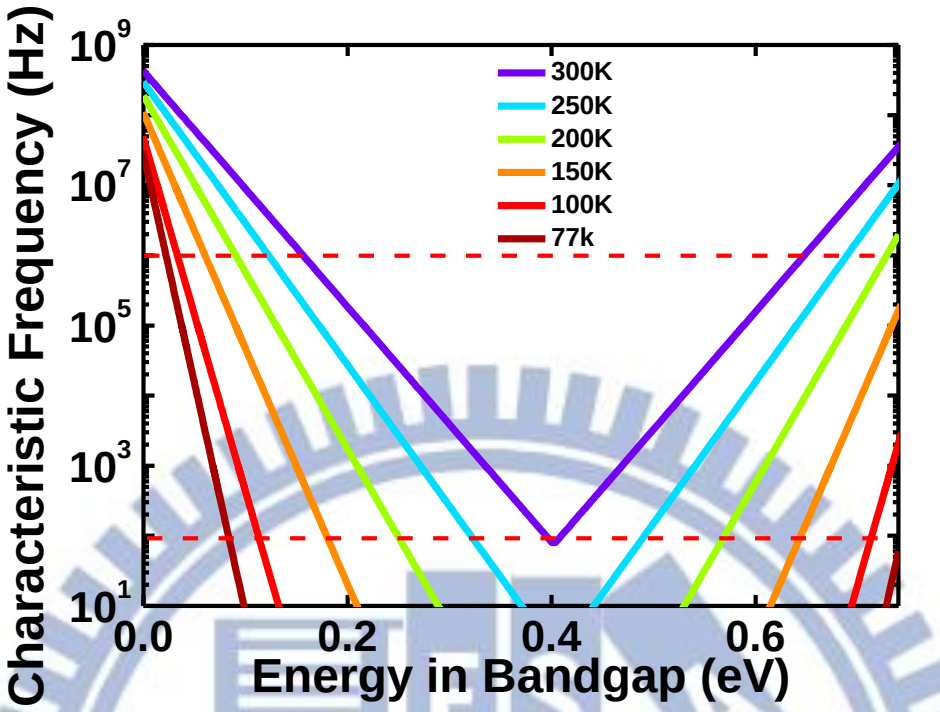
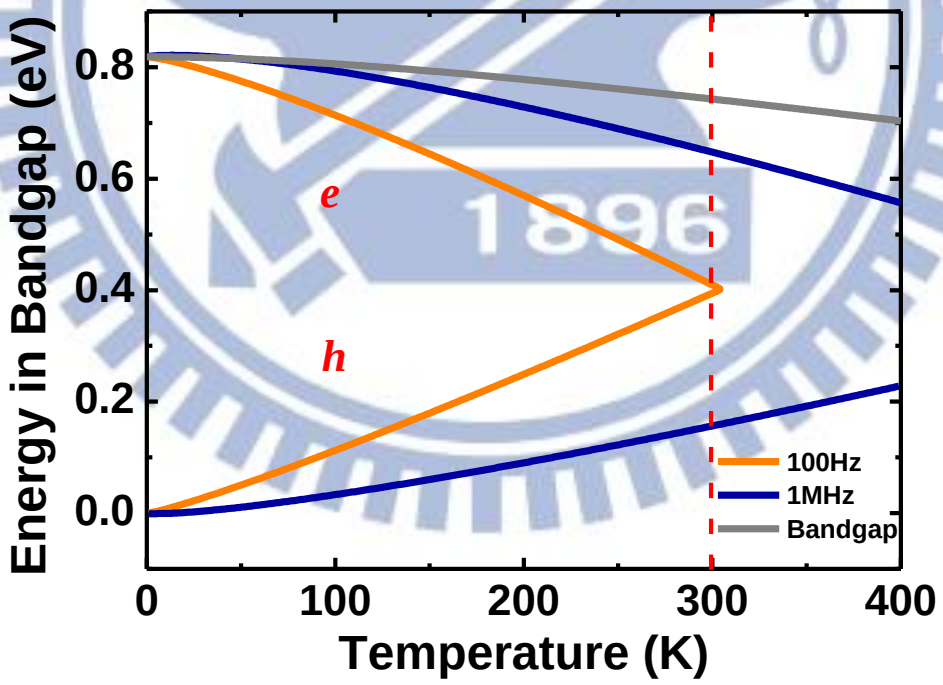


Fig. 2.22 The band diagram of a *n*-type MOSCAP in depletion is shown in **(a)**. A small ac signal of frequency *f* superimposing on a dc gate bias V_G is applied, inducing band bending ψ_s in the semiconductor and interface trap response with time constant τ. **(b)** Equivalent circuit of MOSCAP in depletion. **(c)** Measured circuit.

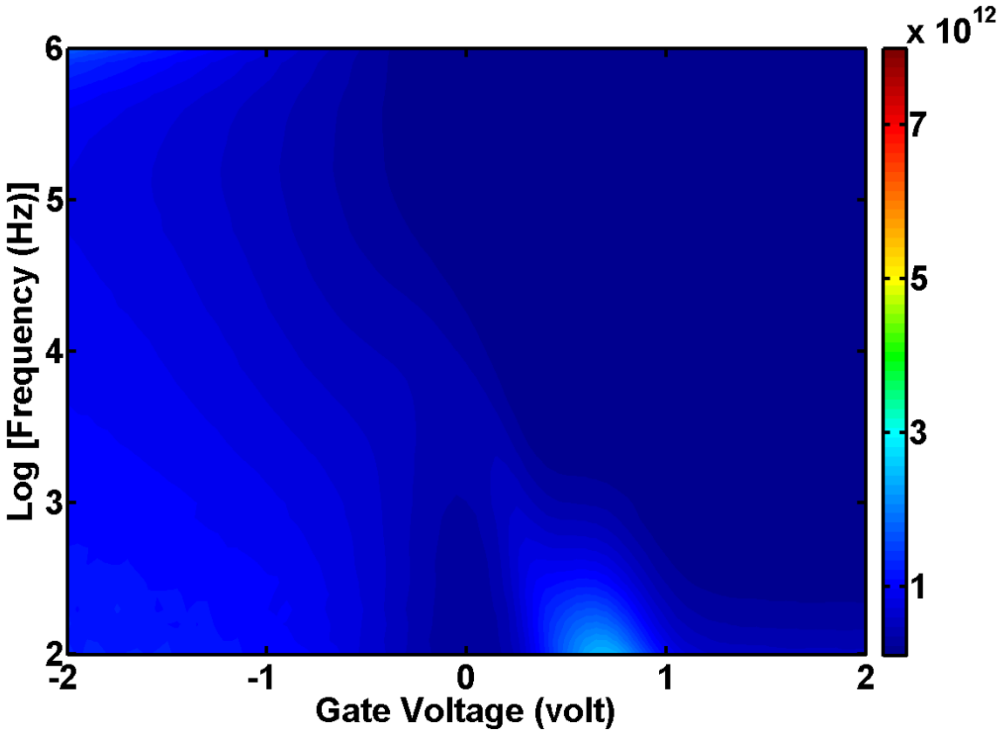


(a)

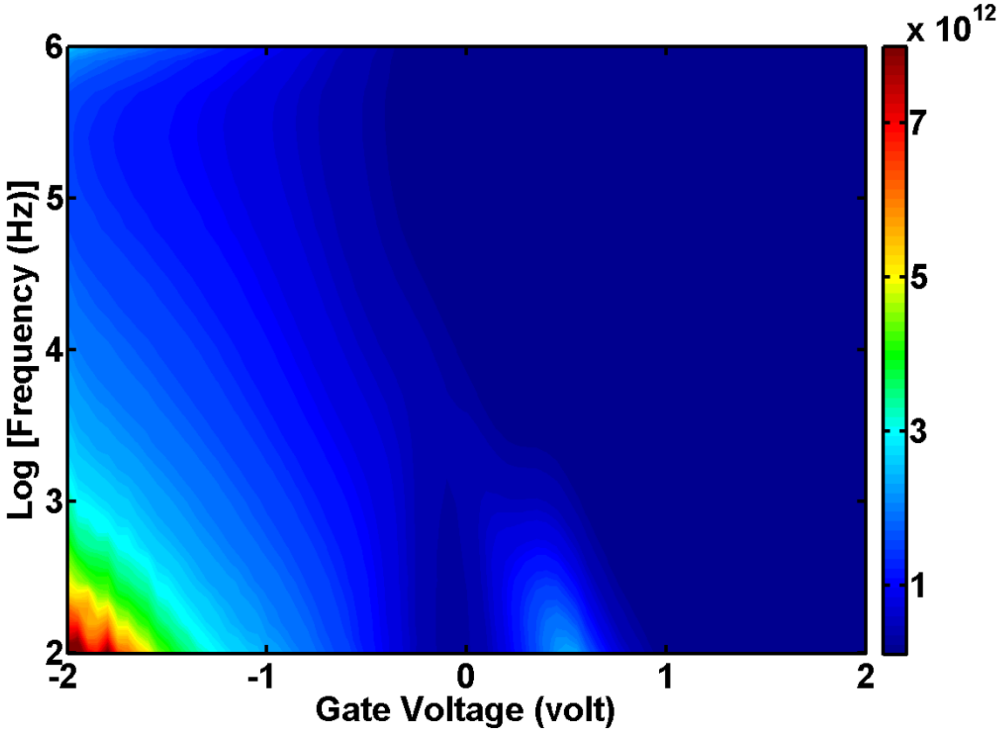


(b)

Fig. 2.23 (a) & **(b)** Charge trapping characteristics for $In_{0.53}Ga_{0.47}As$ under different temperature and corresponding measurement window with 100 Hz and 1 M Hz *C-V* measurement frequency

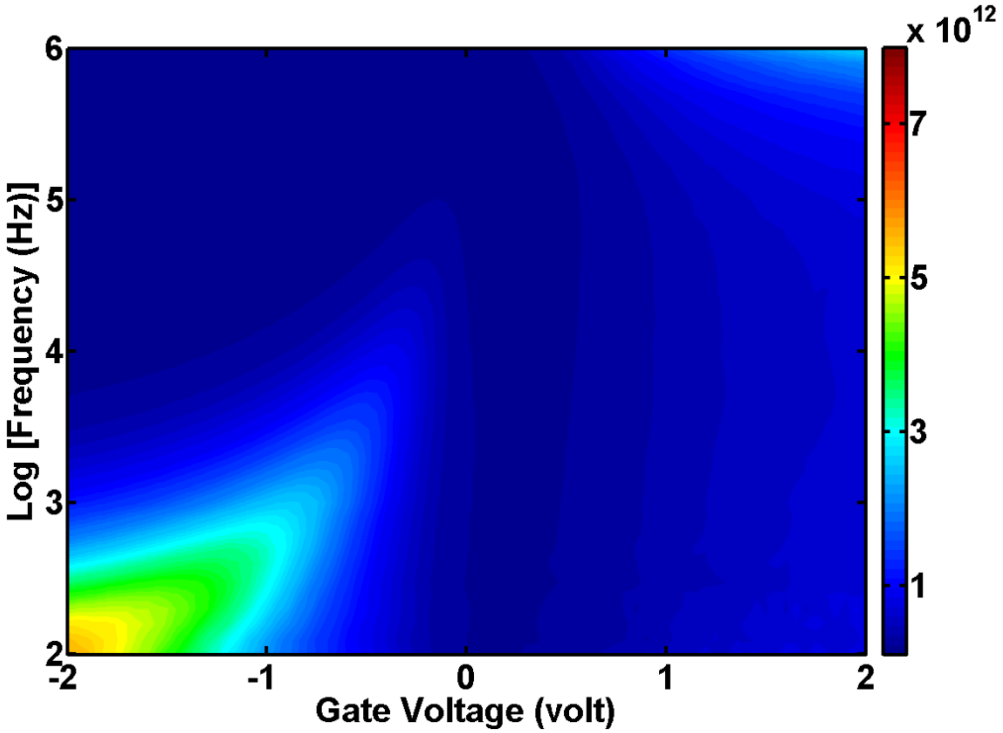


(a)

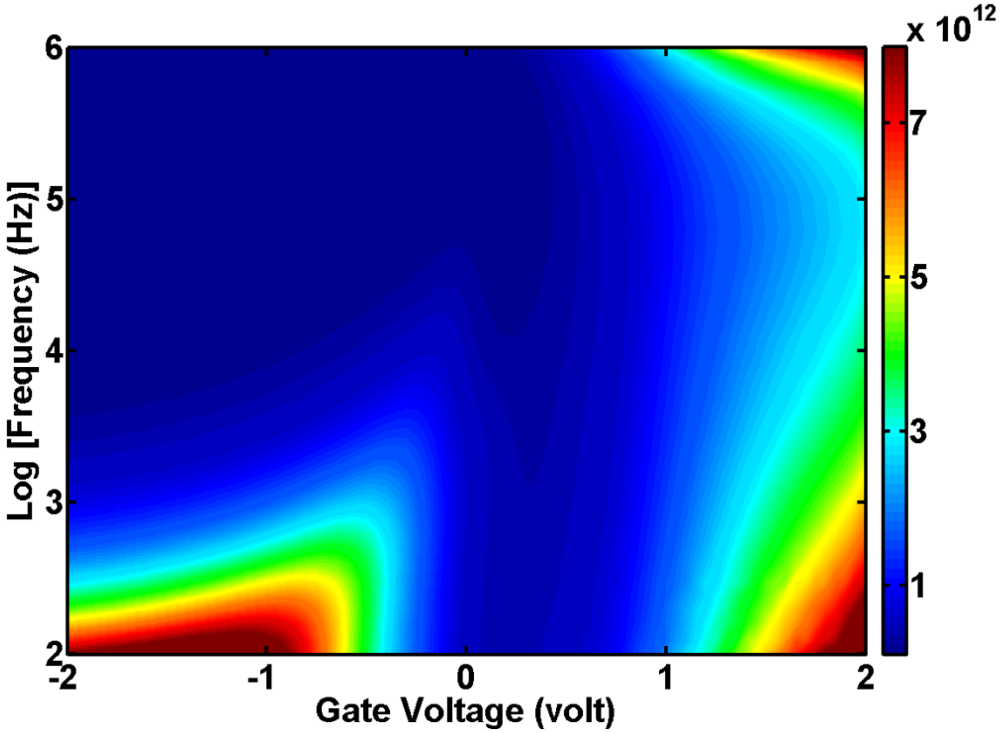


(b)

Fig. 2.24 Map of the normalized parallel conductance, $(G_p/\omega)/Aq$, as a function of gate bias V_G and frequency f measured at 300K for MOSCAPs with Al_2O_3 (as-deposited) on p-type $In_{0.53}Ga_{0.47}As$ (100) after **(a)** FGA and **(b)** PMA



(a)



(b)

Fig. 2.25 Map of the normalized parallel conductance, $(G_p/\omega)/Aq$, as a function of gate bias V_G and frequency f measured at 300K for MOSCAPs with Al_2O_3 (as-deposited) on n-type $In_{0.53}Ga_{0.47}As$ (100) after **(a)** FGA and **(b)** PMA

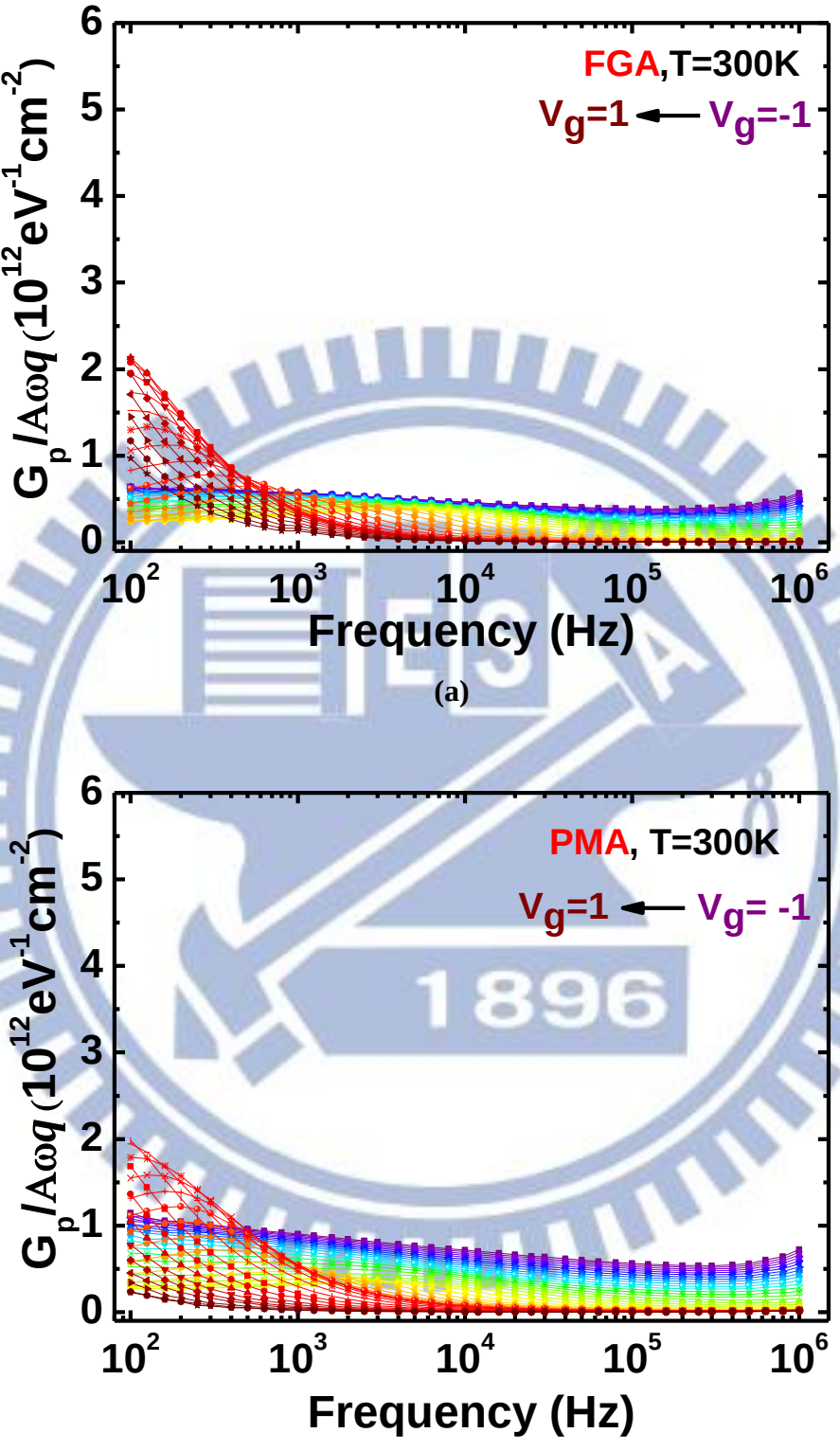


Fig. 2.26 Parallel conductance curves of MOSCAPs with Al_2O_3 (as-deposited) on *p*-type $In_{0.53}Ga_{0.47}As$ (100) after **(a)** FGA and **(b)** PMA for V_G= -1 to 1 volt. The measurement is performed at 300K.

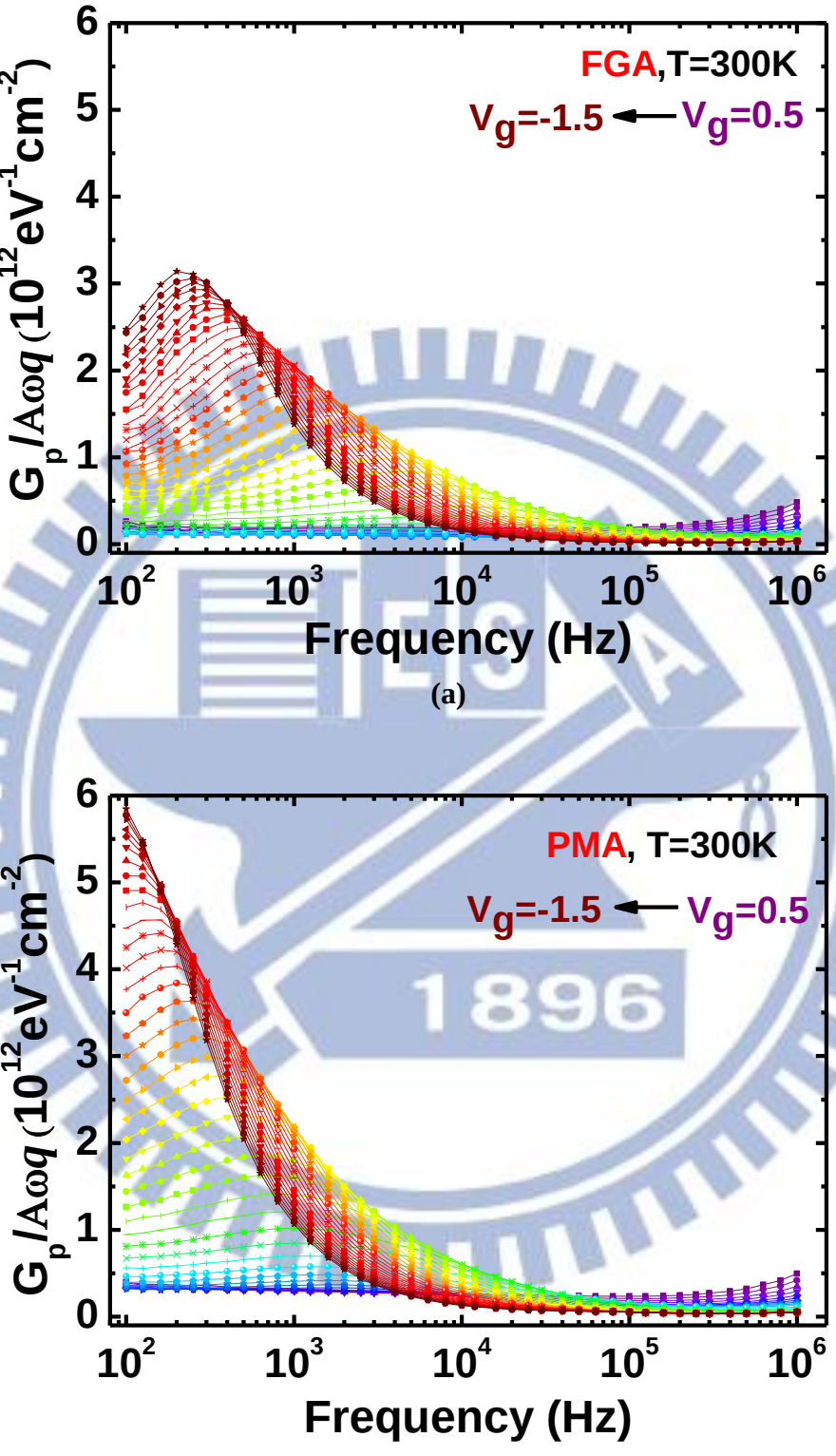


Fig. 2.27 Parallel conductance curves of MOSCAPs with Al_2O_3 (as-deposited) on *n*-type $In_{0.53}Ga_{0.47}As$ (100) after **(a)** FGA and **(b)** PMA for V_G= 0.5 to -1.5 volts. The measurement is performed at 300K.

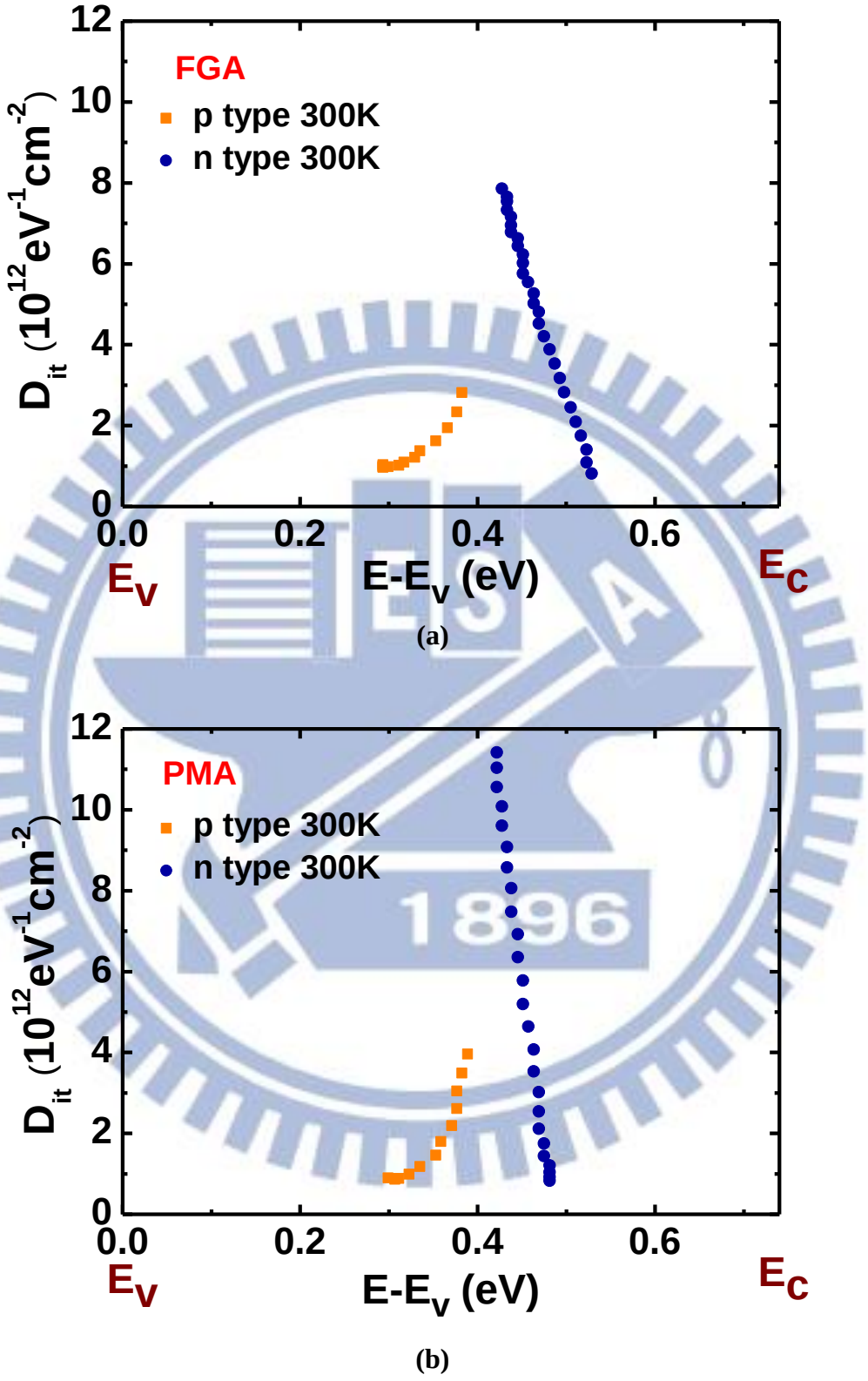
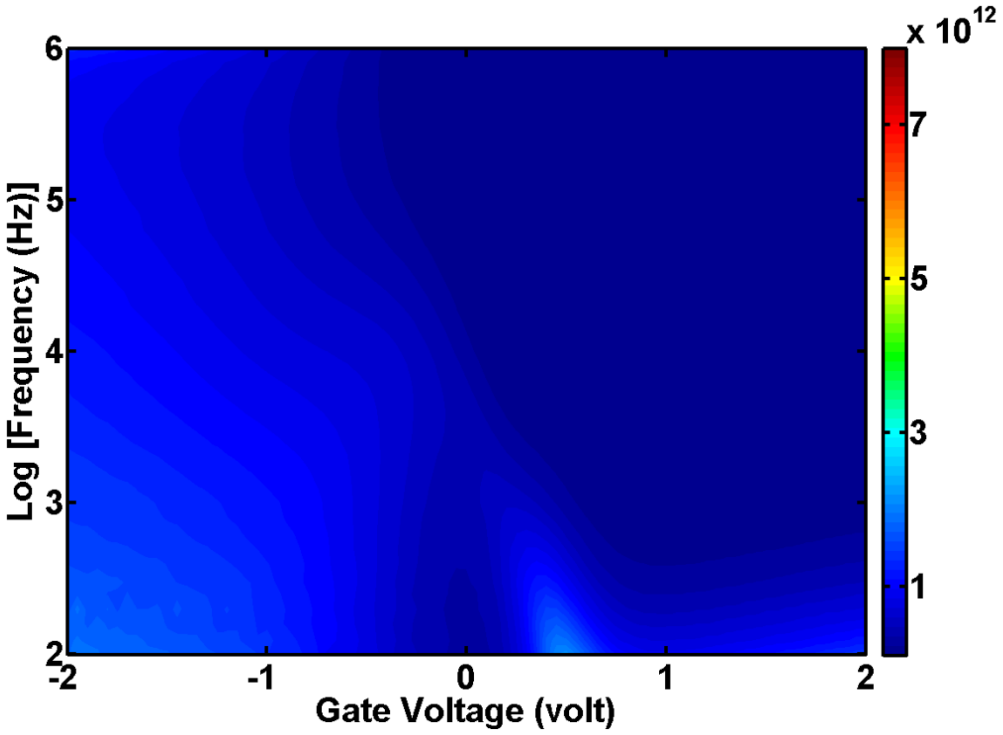
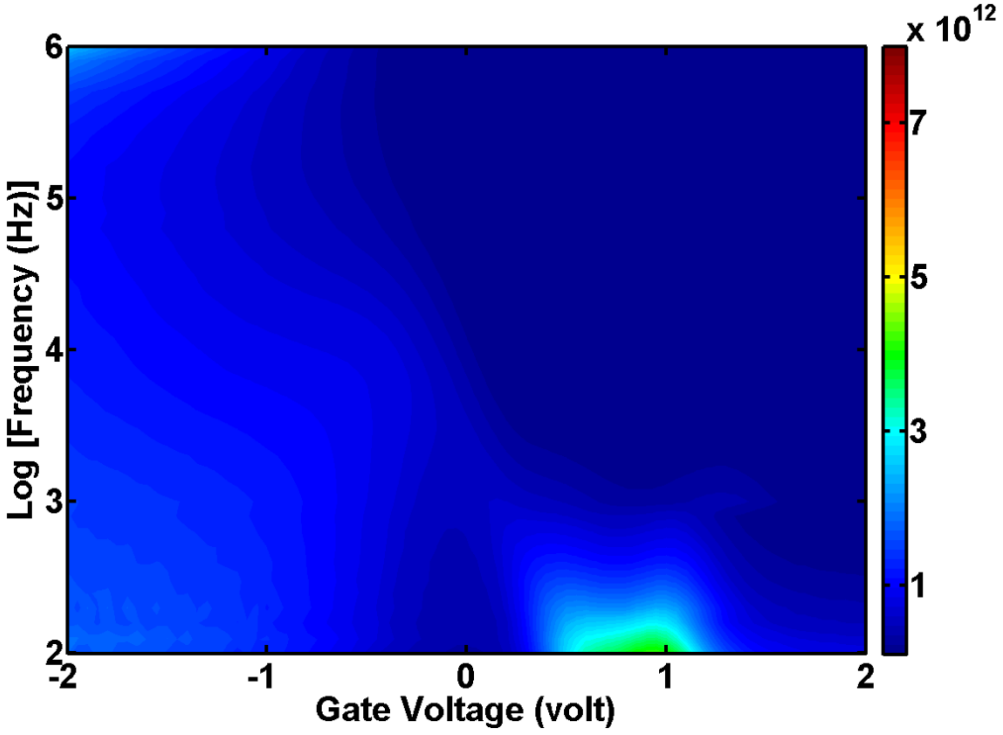


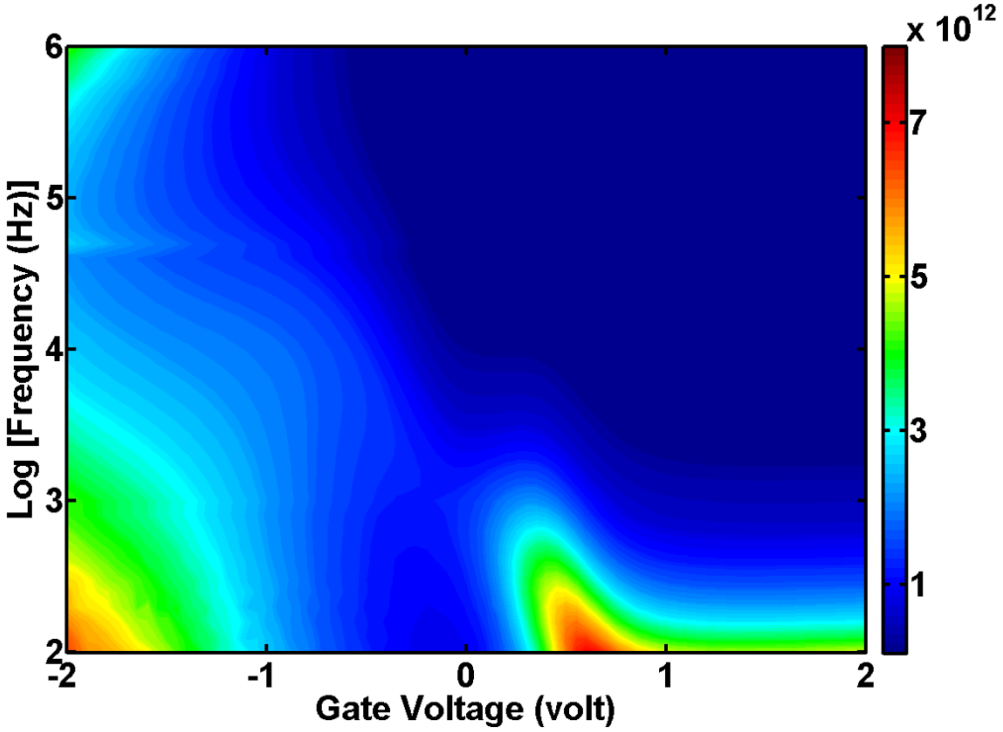
Fig. 2.28 $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) interface state distribution as determined from conductance method, showing that MOSCAPs with **(a)** FGA and **(b)** PMA. The measurement is performed at 300K.


x 10^12
7
5
3
1
6
5
4
3
2
Log [Frequency (Hz)]
-2
-1
0
1
2
Gate Voltage (volt)

(a)

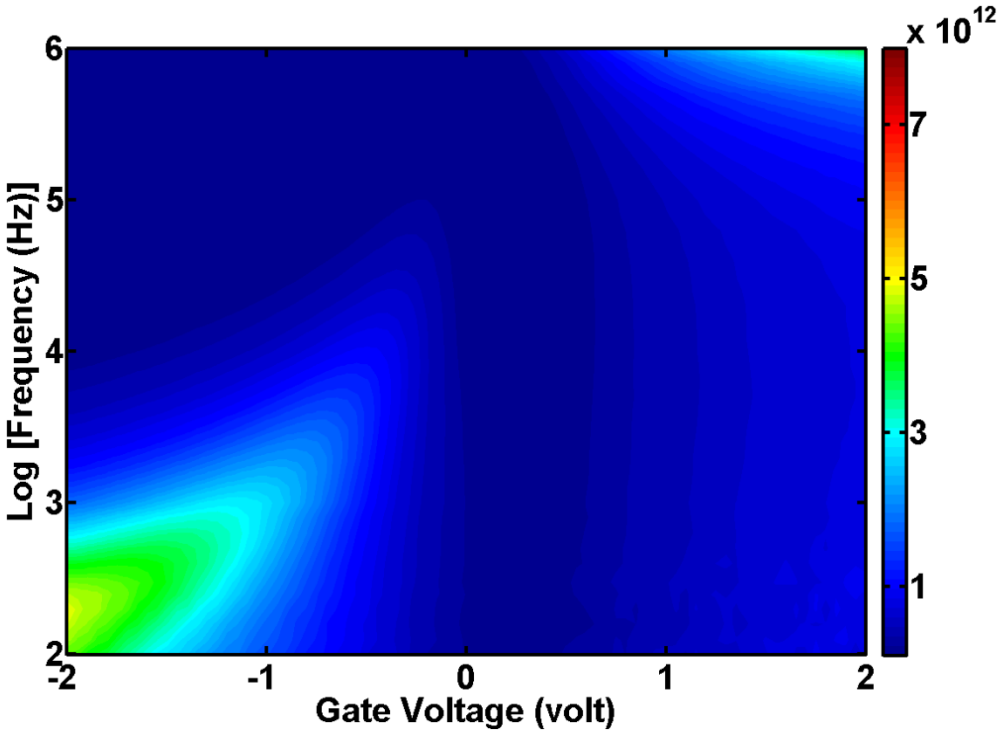

x 10^12
7
5
3
1
6
5
4
3
2
Log [Frequency (Hz)]
-2
-1
0
1
2
Gate Voltage (volt)

(b)

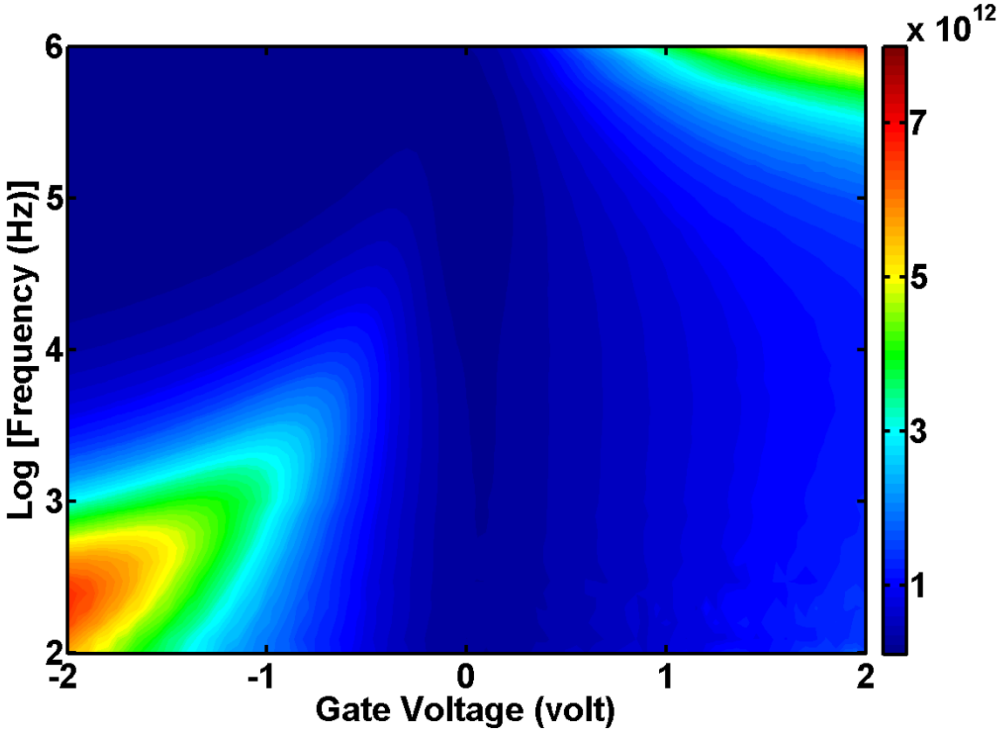


(c)

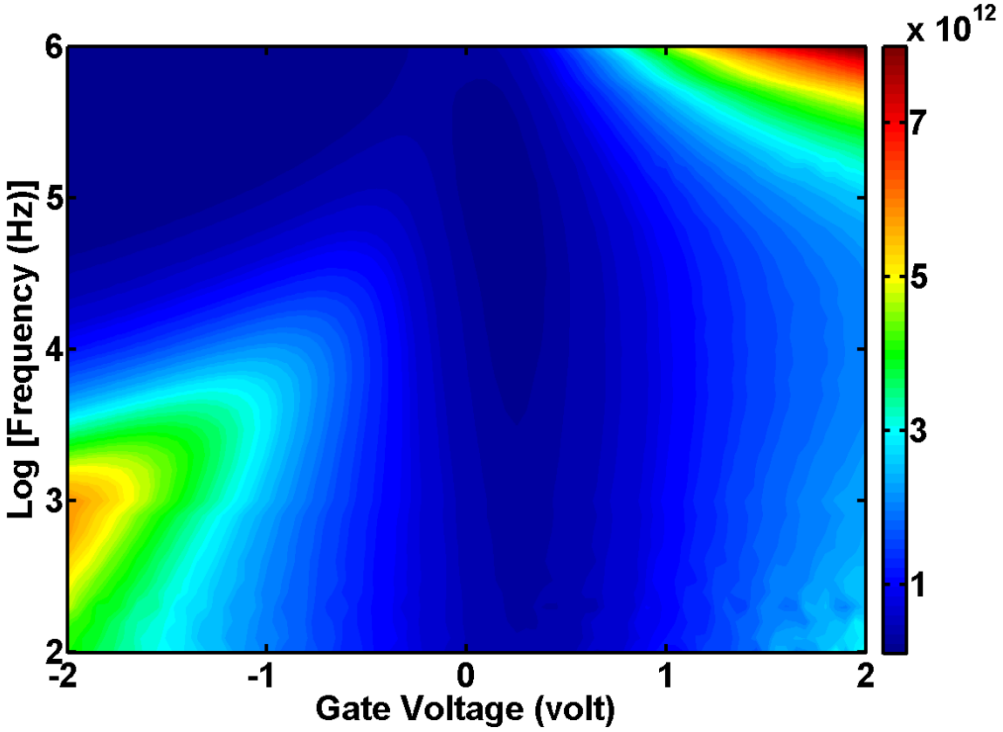
Fig. 2.29 Normalized parallel conductance, $(G_p/\omega)/Aq$, as a function of gate bias V_G and frequency f measured at 300K for MOSCAPs with ALD-TMA/Al_2O_3 on p-type $In_{0.53}Ga_{0.47}As$ (100) after post-metallization FGA under different PDA conditions in N_2 ambience for 120 s **(a)** 300 ^oC **(b)** 400 ^oC **(c)** 500 ^oC.


x 10^12
7
5
3
1
6
5
4
3
2
Log [Frequency (Hz)]
-2
-1
0
1
2
Gate Voltage (volt)

(a)

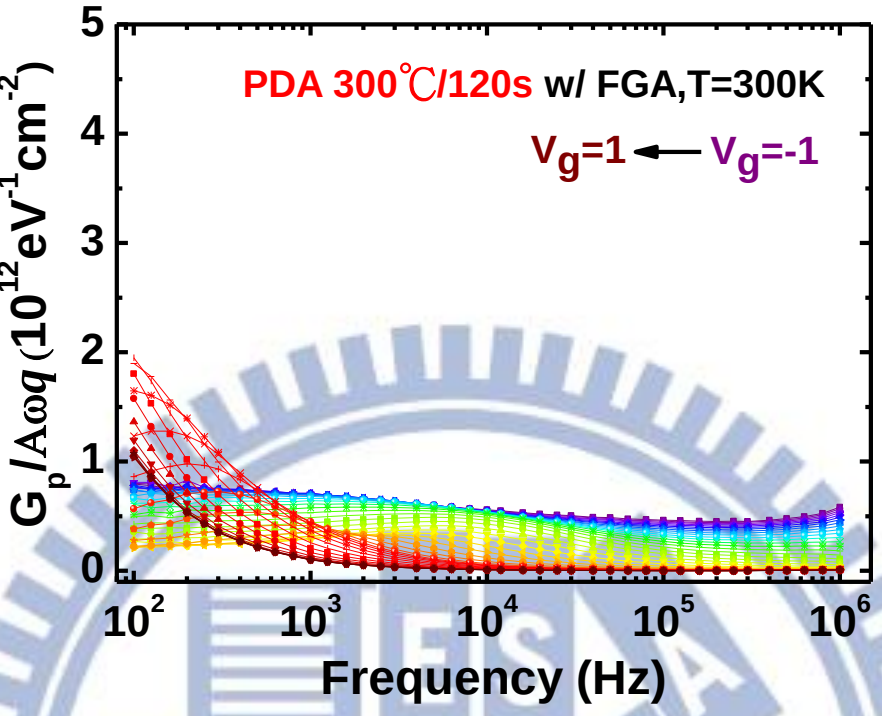

x 10^12
7
5
3
1
6
5
4
3
2
Log [Frequency (Hz)]
-2
-1
0
1
2
Gate Voltage (volt)

(b)

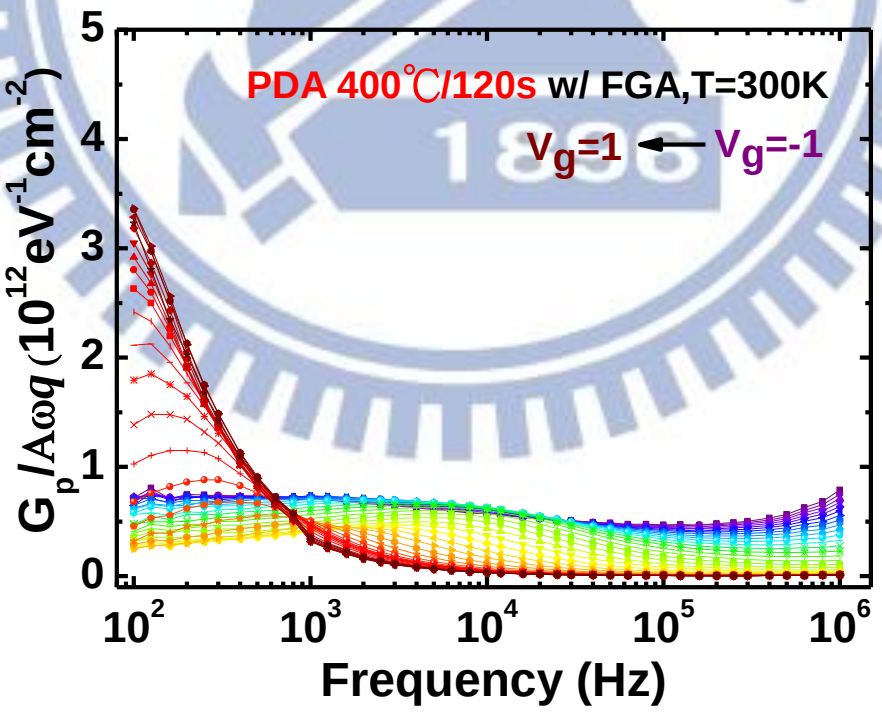


(c)

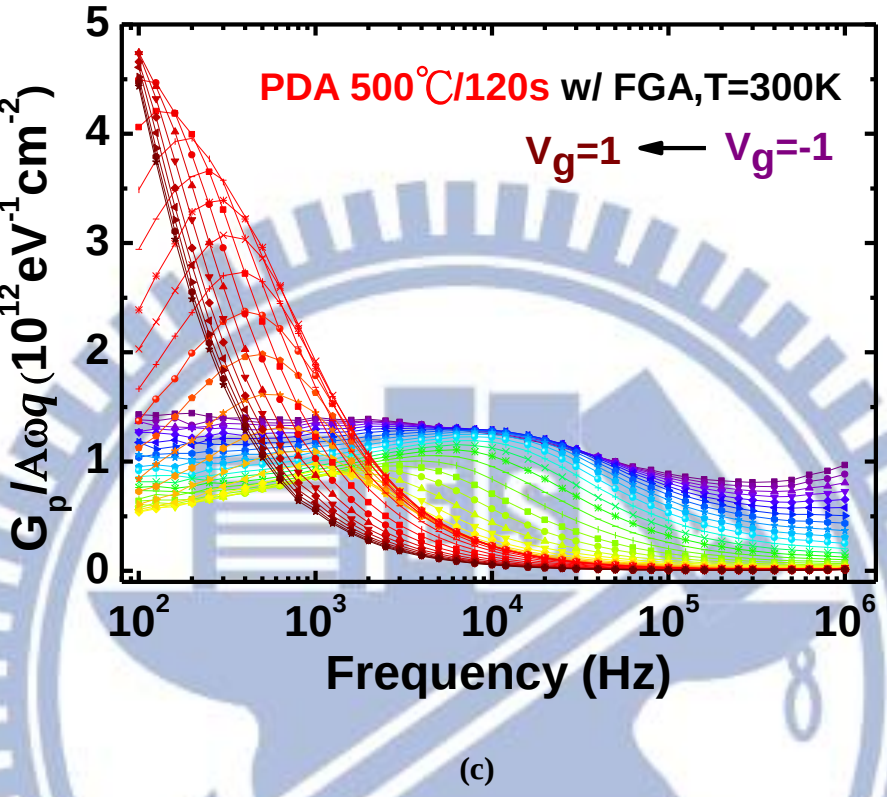
Fig. 2.30 Normalized parallel conductance, $(G_p/\omega)/Aq$, as a function of gate bias V_G and frequency f measured at 300K for MOSCAPs with ALD-TMA/Al_2O_3 on n-type $In_{0.53}Ga_{0.47}As$ (100) after post-metallization FGA under different PDA conditions in N_2 ambience for 120 s (**a)** 300 ^oC **(b)** 400 ^oC **(c)** 500 ^oC.


PDA 300℃/120s w/ FGA,T=300K
V_g=1 ← V_g=-1
$G_p/A\omega q$ ($10^{12}eV^{-1}cm^{-2}$)
Frequency (Hz)

(a)

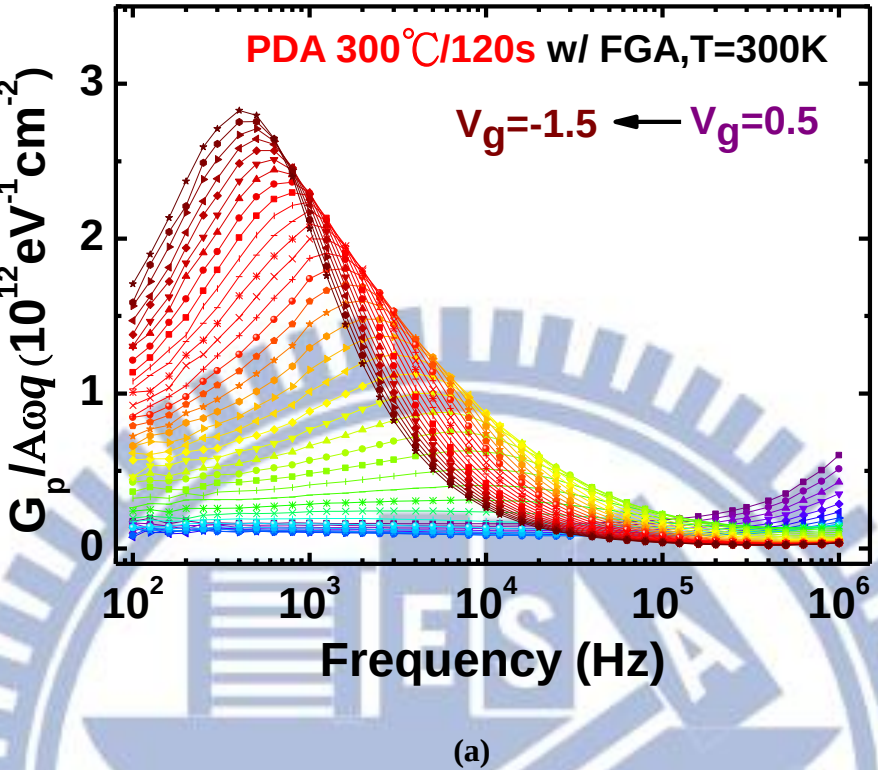

PDA 400℃/120s w/ FGA,T=300K
V_g=1 ← V_g=-1
$G_p/A\omega q$ ($10^{12}eV^{-1}cm^{-2}$)
Frequency (Hz)

(b)

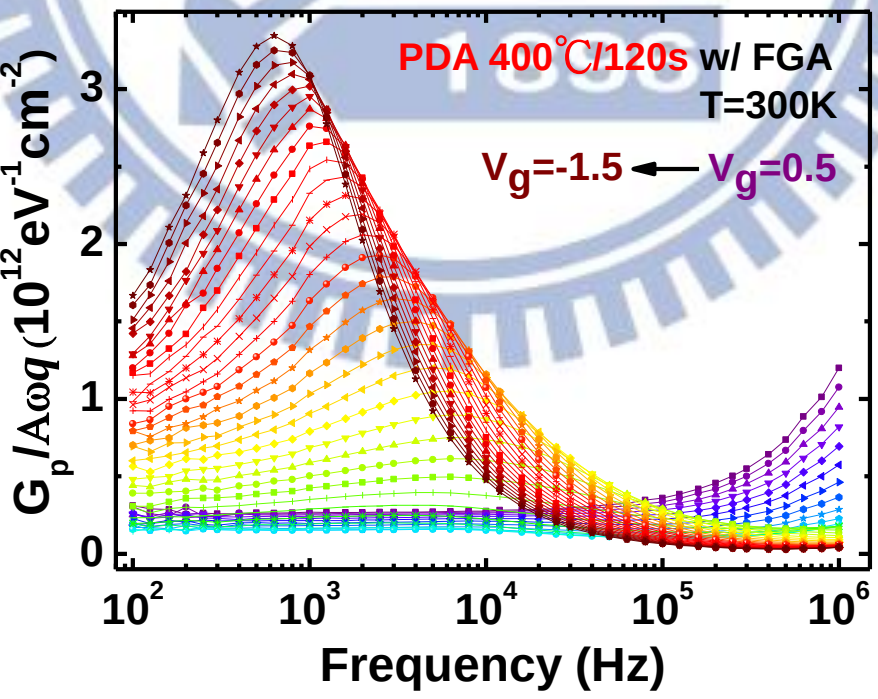


(c)

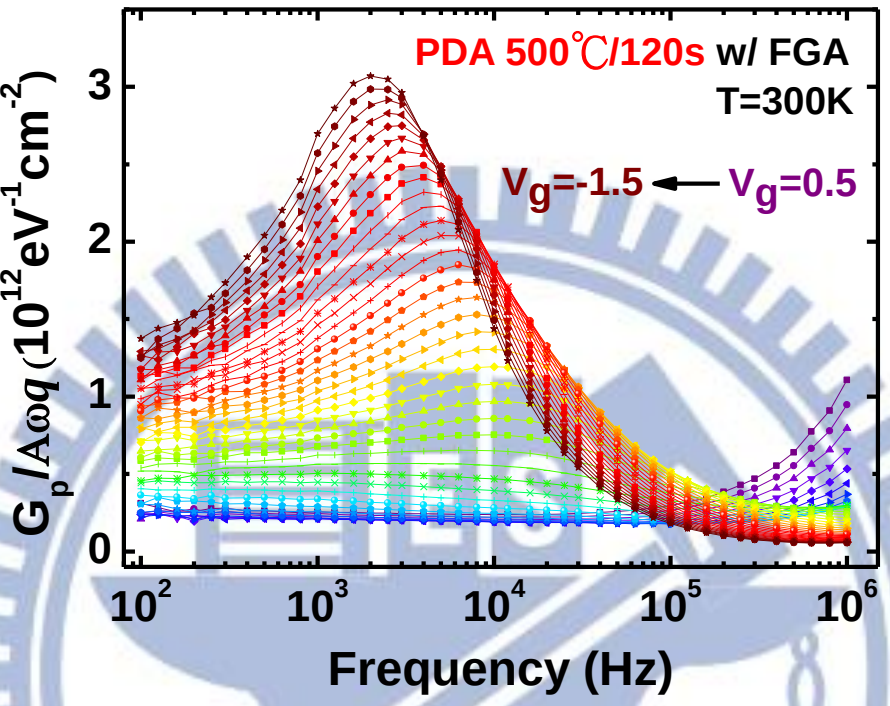
Fig. 2.31 Parallel conductance curves of MOSCAPs with Al_2O_3 on *p*-type $In_{0.53}Ga_{0.47}As$ (100) with post-metallization FGA and under different PDA conditions for V_G= -1 to 1 volt (**a)** 300 ^oC **(b)** 400 ^oC **(c)** 500 ^oC. The measurement is performed at 300K.


PDA 300℃/120s w/ FGA,T=300K
V_g=-1.5 ← V_g=0.5
$G_p/A\omega q$ ($10^{12}eV^{-1}cm^{-2}$)
Frequency (Hz)

(a)

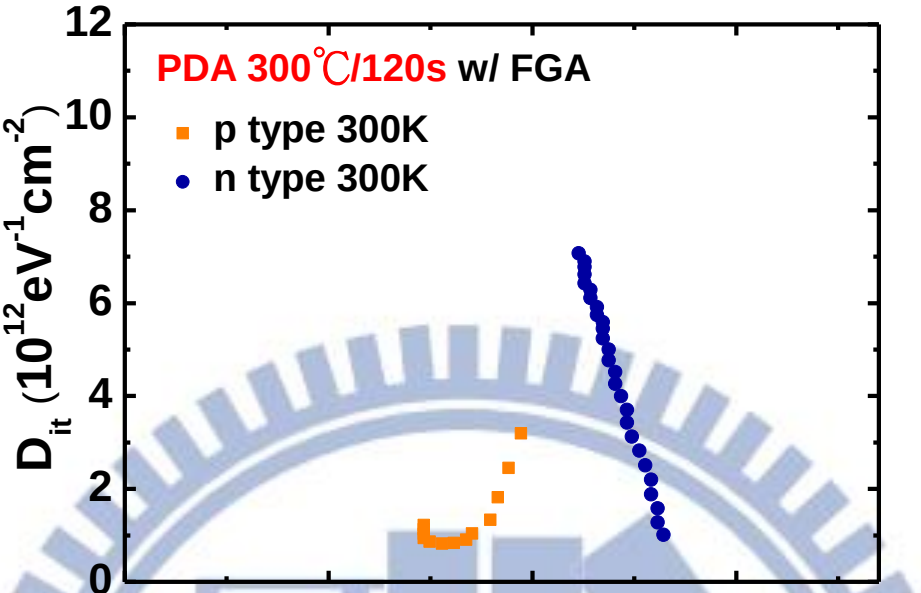

PDA 400℃/120s w/ FGA
T=300K
V_g=-1.5 ← V_g=0.5
$G_p/A\omega q$ ($10^{12}eV^{-1}cm^{-2}$)
Frequency (Hz)

(b)

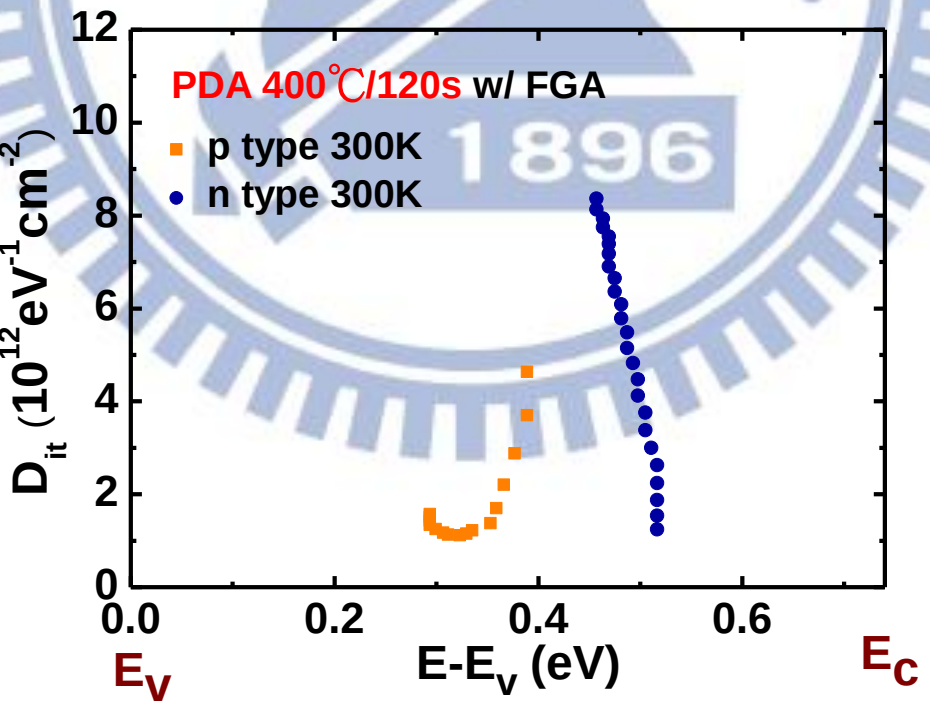


(c)

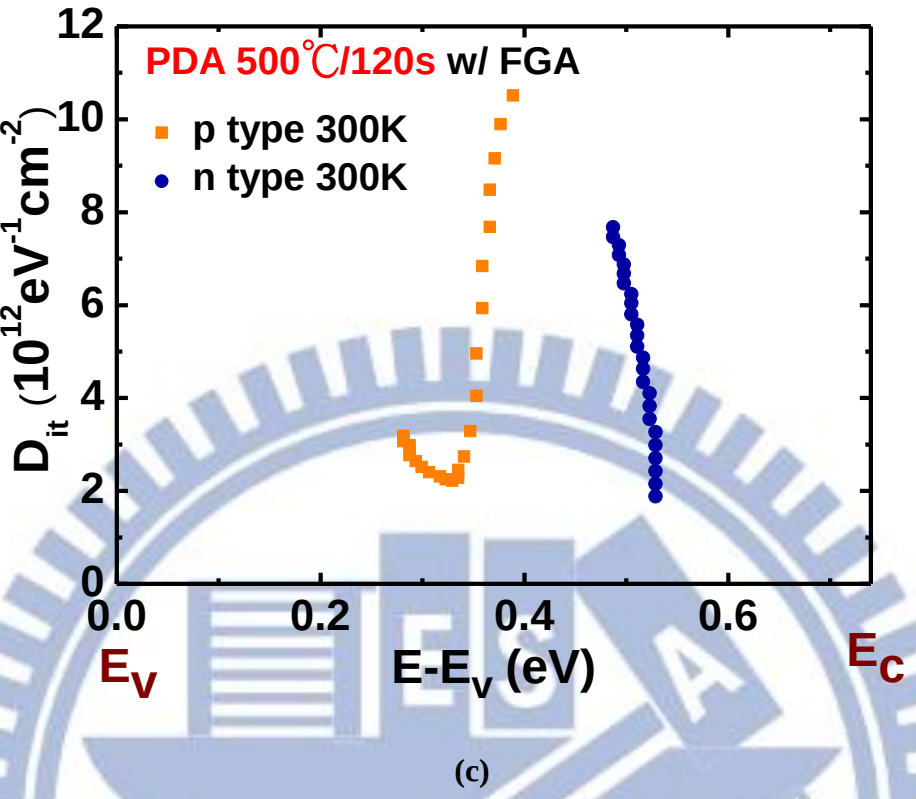
Fig. 2.32 Parallel conductance curves of MOSCAPs with Al_2O_3 on *n*-type $In_{0.53}Ga_{0.47}As$ (100) with post-metallization FGA and under different PDA conditions for V_G= 0.5 to -1.5 volts.(**a**) 300 °C (**b**) 400 °C (**c**) 500 °C. The measurement is performed at 300K.


PDA 300℃/120s w/ FGA
p type 300K
n type 300K
D_{it} ($10^{12}eV^{-1}cm^{-2}$)
E-E_V (eV)
E_V
E_C

(a)

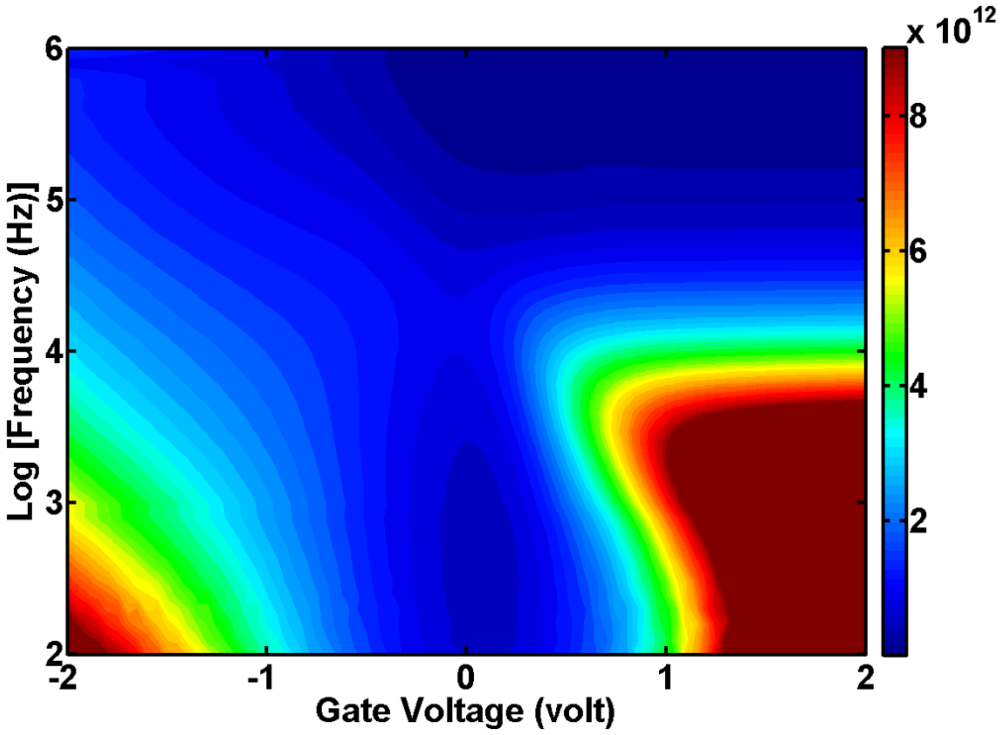

PDA 400℃/120s w/ FGA
p type 300K
n type 300K
D_{it} ($10^{12}eV^{-1}cm^{-2}$)
E-E_V (eV)
E_V
E_C

(b)

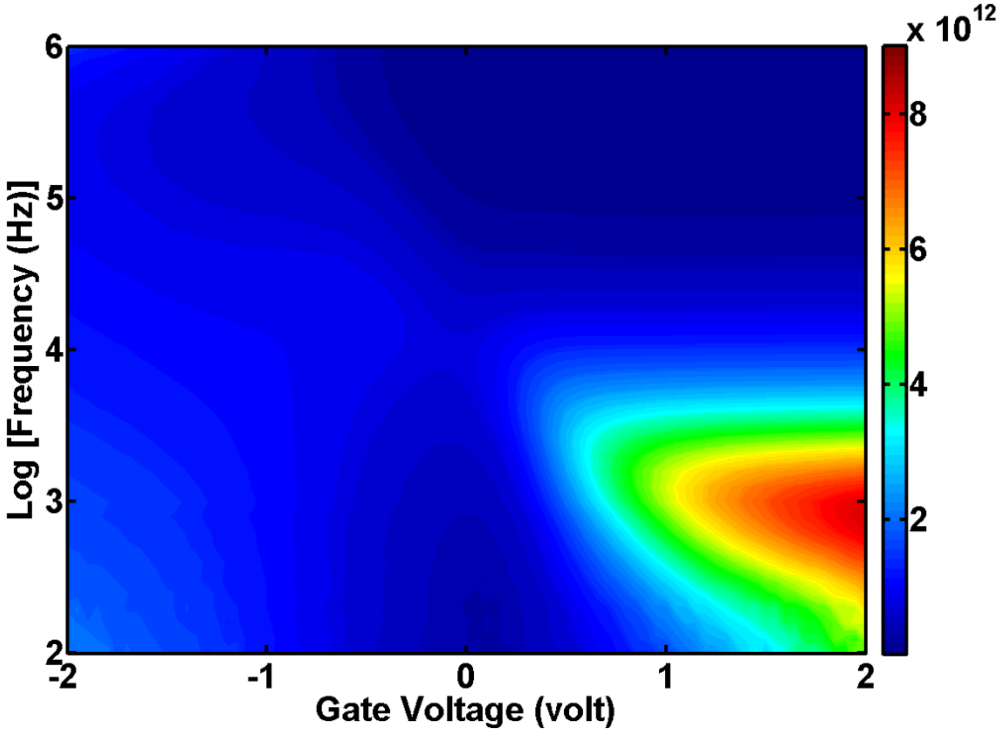


(c)

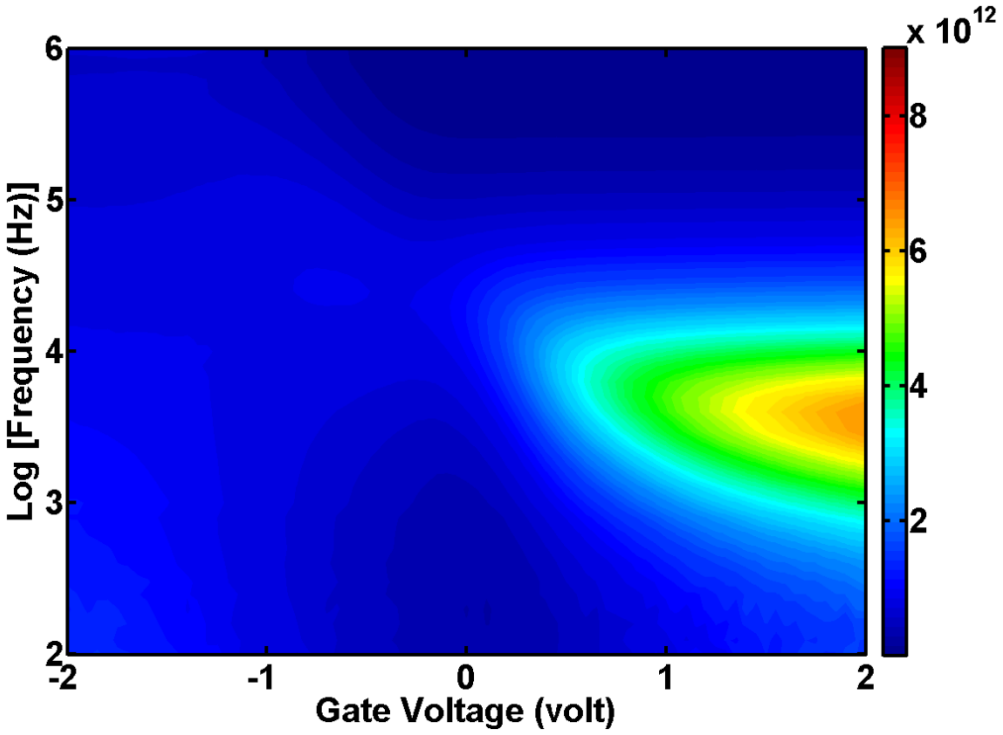
Fig. 2.33 $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) interface state distribution as determined from conductance method, showing that MOSCAPs with post-metallization FGA and under different PDA conditions (**a)** 300 °C **(b)** 400 °C **(c)** 500 °C for 120s. The measurement is performed at 300K.


x 10^12
8
6
4
2
6
5
4
3
2
Log [Frequency (Hz)]
-2
-1
0
1
2
Gate Voltage (volt)

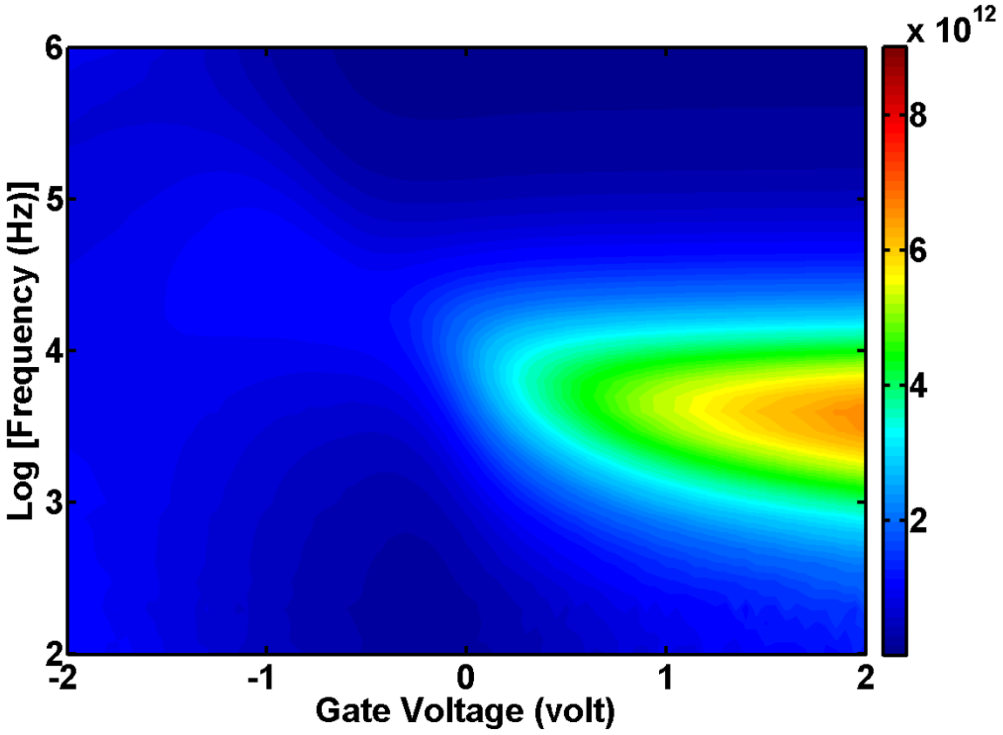
(a)


x 10^12
8
6
4
2
6
5
4
3
2
Log [Frequency (Hz)]
-2
-1
0
1
2
Gate Voltage (volt)

(b)



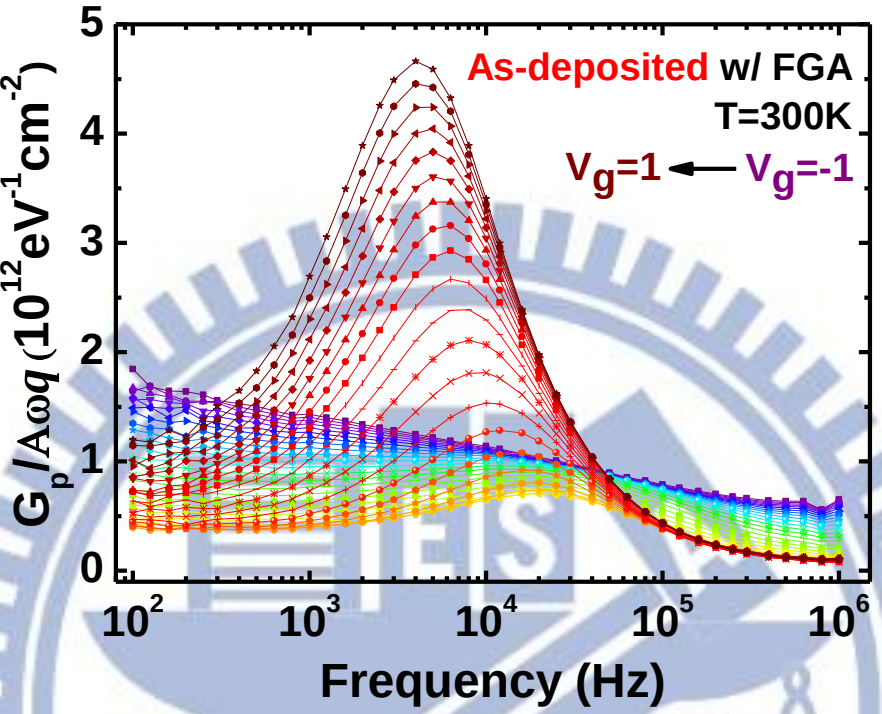
(c)



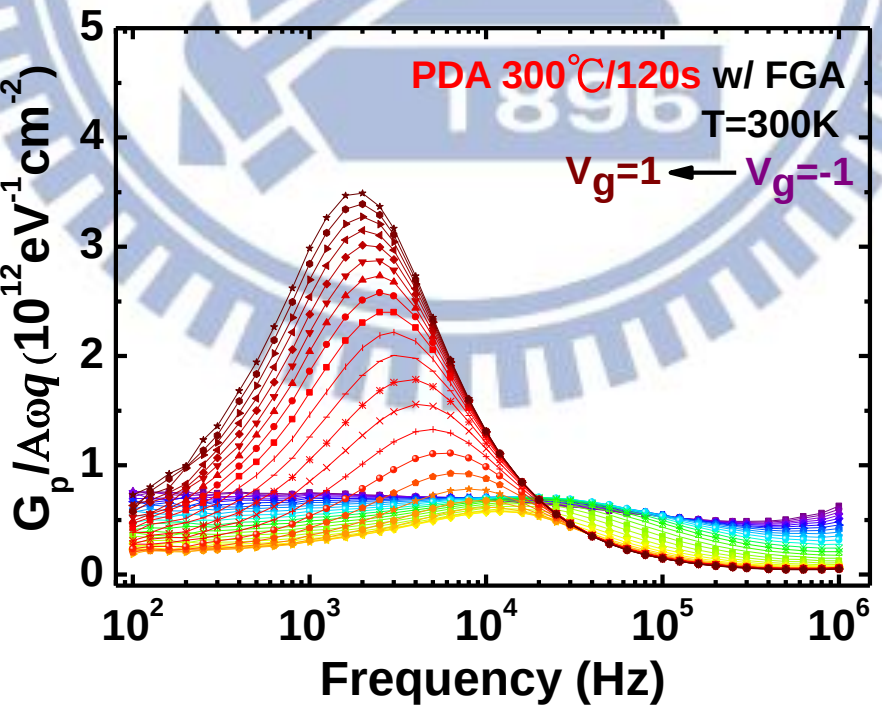
(d)

Fig. 2.34 Normalized parallel conductance, $(G_p/\omega)/Aq$, as a function of gate bias V_G and frequency f measured at 300K for MOSCAPs with ALD-TMA/Al_2O_3 on p-type $In_{0.53}Ga_{0.47}As$ (111)A after post-metallization FGA under different

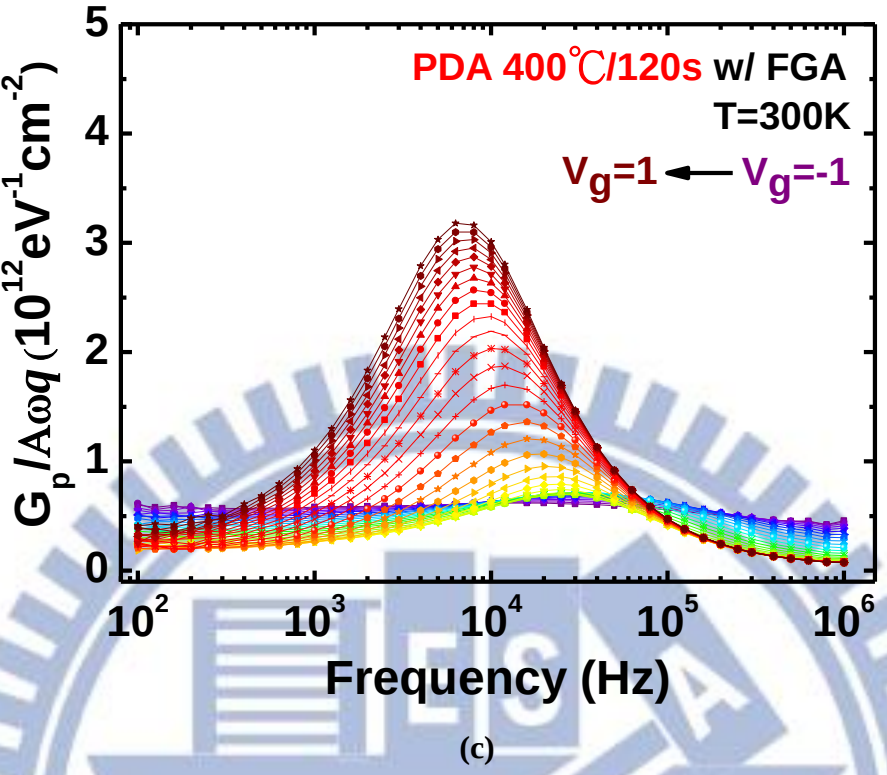
PDA conditions in N_2 ambience for 120 s **(a)** as-deposited **(b)** 300 ^{o}C **(c)** 400 ^{o}C **(d)** 500 ^{o}C.



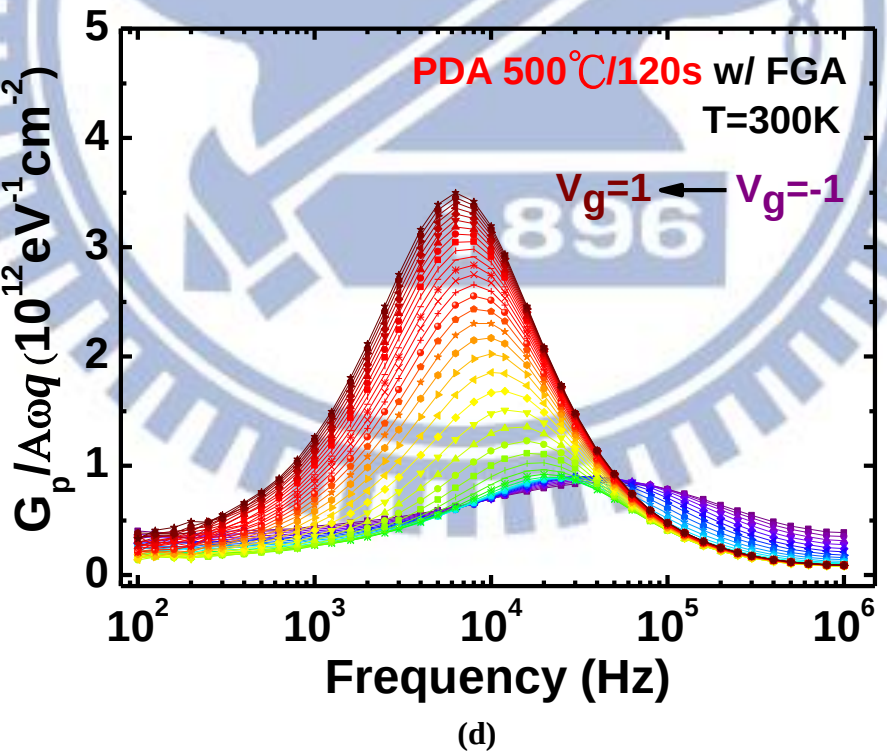
(a)



(b)



(c)



(d)

Fig. 2.35 Parallel conductance curves of MOSCAPs with Al_2O_3 on *p*-type $In_{0.53}Ga_{0.47}$-As (111)A with post-metallization FGA and under different PDA conditions for V_G= -1 to 1 volt. **(a)** as-deposited **(b)** 300 °C **(c)** 400 °C **(d)** 500 °C.

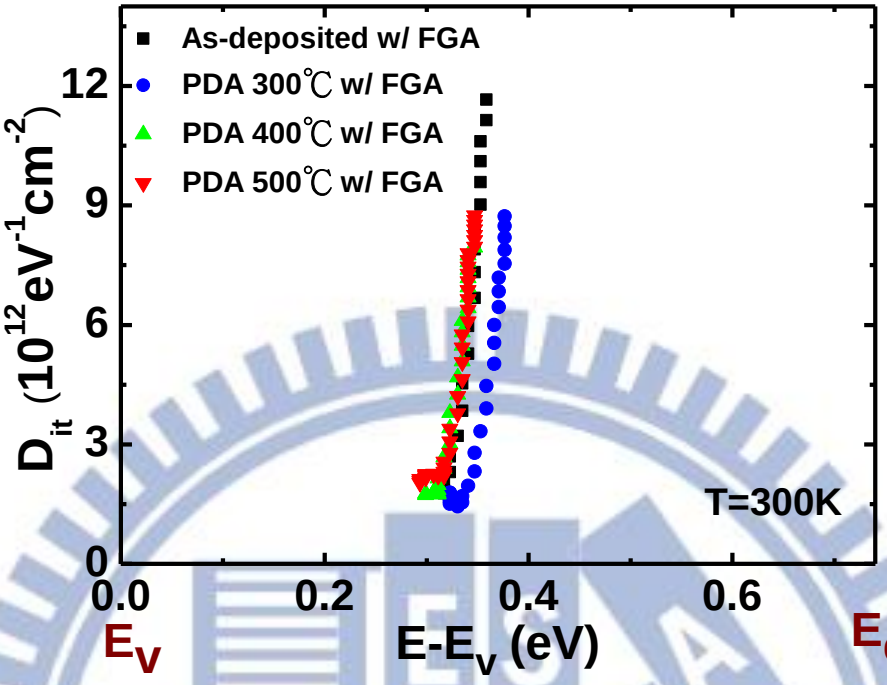


Fig. 2.36 D_{it} profiles of $Al_2O_3/In_{0.53}Ga_{0.47}As$ (111)A MOSCAPs with FGA and under different PDA conditions. The measurement is performed at 300K.

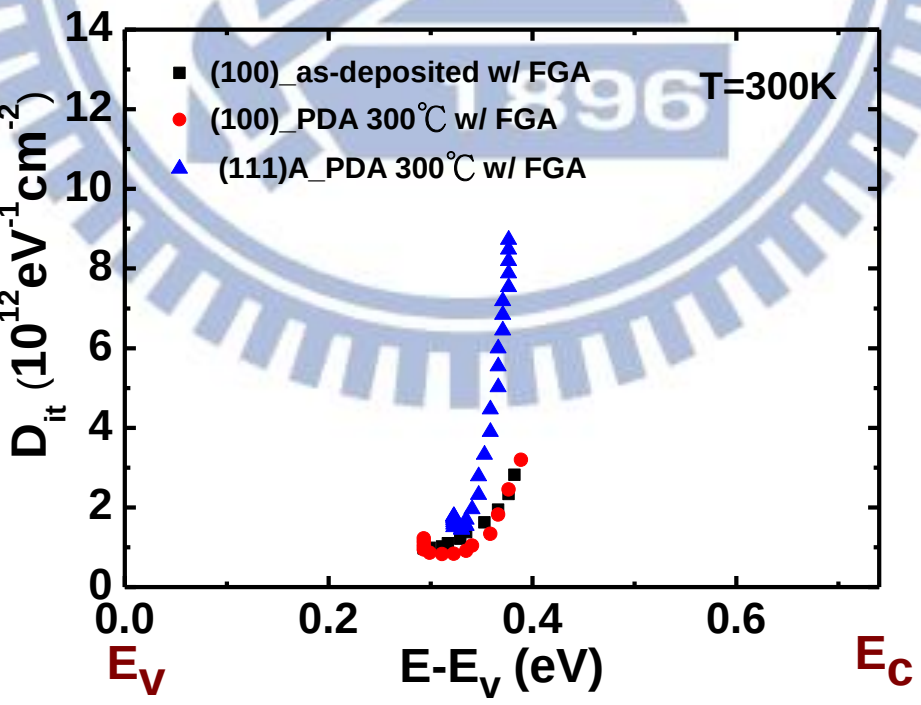


Fig. 2.37 The comparison of D_{it} profiles between (100) and (111)A

(100)	As-deposited	PDA 300℃/120s	PDA 400℃/120s	PDA 500℃/120s
P w/o FGA	64.39%			
P w/ FGA	8.96%	10.81%	9.16%	16.91%
P w/ PMA	12.34%			
N w/o FGA	6.49%			
N w/ FGA	4.77%	5.29%	4.78%	5.99%
N w/ PMA	8.08%			

Table 2.1 The overviews of frequency dispersion of ALD-TMA/Al_2O_3 (100)-oriented $In_{0.53}Ga_{0.47}As$ MOSCAPs (@V_G = -2 for *p*-type or 2 volt for *n*-type)

(111)A	As-deposited	PDA 300℃/120s	PDA 400℃/120s	PDA 500℃/120s
P w/o FGA	14.57%	12.72%	13.52%	15.89%

Table 2.2 The overviews of frequency dispersion of ALD-TMA/Al_2O_3 (111)A-oriented *p*-$In_{0.53}Ga_{0.47}As$ MOSCAPs at V_G = -2

Area ratio	As-As/As-Ga	As-/As-Ga	As_2O_3/ As_2O_5
As-deposited	0.226		2.959
300°C /120s	0.233		2.484
400°C /120s	0.260		2.358
500°C/120s	0.509	0.305	1.792

Table 2.3 Ratio of the fitted area of the As-As and As- components and As_2O_3 to As_2O_5 from the As $2p_{3/2}$ spectra for the $In_{0.53}Ga_{0.47}As$ (100) samples at different PDA conditions

Area ratio	As-As/As-Ga	As-/As-Ga	As_2O_3/ As_2O_5
As-deposited	0.185		1.176
300°C /120s	0.024	0.109	1.862
400°C /120s		0.287	0.838
500°C/120s		0.441	0.891

Table 2.4 Ratio of the fitted area of the As-As and As- components and As_2O_3 to As_2O_5 from the As $2p_{3/2}$ spectra for the $In_{0.53}Ga_{0.47}As$ (111)A samples at different PDA conditions

D_{it} ($10^{12}eV^{-1}cm^{-2}$)	p-type (100) @ E_t= 0.382 eV	n-type (100) @ E_t= 0.428 eV	
PMA	3.49	10.1	
FGA	2.81	7.85	
D_{it} ($10^{12}eV^{-1}cm^{-2}$)	p-type (100) @ E_t= 0.377eV	n-type (100) @ E_t= 0.487 eV	p-type (111)A @ E_t= 0.347 eV
As-deposited+FGA	2.34	3.53	8.43
300°C /120s+FGA	2.45	4.00	2.78
400°C /120s+FGA	2.88	5.48	7.95
500°C/120s+FGA	9.89	7.68	8.75

Table 2.5 The overviews of D_{it} values of ALD-TMA/Al_2O_3 (100)-oriented and (111)A-oriented $In_{0.53}Ga_{0.47}As$ under different thermal treatments

Chapter 3

Self-Aligned Metal Source/Drain $In_{0.53}Ga_{0.47}As$ n-MOSFETs using Ni-InGaAs Alloy

3.1 Introduction

Lately, the performance improvement accompanied by device scaling has become tough owing to the increase in leakage current, short channel effects, and so on. In order to solve this scaling problem, several groups are dedicated to application of new materials for future generations [1-2]. Indium Gallium Arsenide (InGaAs) is considered to be a potential channel material for its high electron mobility. One of the challenges to achieve high drive current in MOSFETs is to develop stable and low-resistance ohmics contact to InGaAs. High S/D resistance results from low dopant solubility of III-V compound semiconductors, and metal S/D structure is one of the hopeful methods to reduce S/D resistance. In addition, self-alignment of the S/D contacts to the gate electrode is desirable for reduction of S/D access resistances and for achieving reduced transistor footprint [3]. In this respect, the requirements of S/D for scaled III-V MOSFETs can be satisfied by the self-aligned metal S/D using an alloy layer formed by the reaction of III-V and metals (**Fig. 3.1**), like silicides, with low sheet resistance and low Schottkey Barrier Height (SBH) against III-Vs. A self-aligned metallization process is also simple and similar to the salicidation process in Si CMOS technology

In this chapter, we made attempt to fabricate the self-aligned Ni-InGaAs

metallization process for InGaAs channel *n*-MOSFETs. The self-aligned metallization process consists of conversion of sputtered nickel (Ni) on InGaAs into a uniform Ni-InGaAs film by rapid thermal annealing (RTA), and removal of unreacted Ni by selective wet etching. The most critical parts of this technique is the selective etch of Ni over Ni-InGaAs, which can be quantified as the ratio of the etch rates of Ni and Ni-InGaAs, i.e.

$$S = \frac{r_{Ni}}{r_{Ni-InGaAs}} \qquad \textbf{[3.1]}$$

where r_{Ni} and $r_{Ni\text{-}InGaAs}$ are the etch rates of Ni and Ni-InGaAs respectively.

Many etch chemistries etch Ni at a rapid rate, such as Hydrochloric (HCl), Nitric Acid (HNO_3), Aqua-Regia [$HCl:HNO_3:H_2O$ (3:1:2)], Sulfuric Peroxide Mixture (SPM) [$H_2SO_4:H_2O_2$ (4:1)], $HCl:H_2O_2$ (4:1), $HCl:HNO_3$ (5:1), and $HF:HNO_3$ (1:1). Here, we focus on HCl and HNO_3 solutions performed at different temperature, and prefer the high selectivity etchant that etches Ni quickly but etches Ni-InGaAs slowly. The results are shown in **Table 3.1**, which is from reference [4]. The concentrated HCl (25 $^{\circ}$C) etching the Ni film at a rapid rate of approximately 61 nm/minute gives the highest selectivity of approximately 15.6. The consequences of this reference could be useful for the process of $In_{0.53}Ga_{0.47}As$ channel *n*-MOSFETs with self-aligned Ni-InGaAs S/D.

3.2 Transistor Fabrication

The process flow for transistor fabrication and device structure of $In_{0.53}Ga_{0.47}As$ channel *n*-MOSFETs with self-aligned Ni-InGaAs alloy are illustrated in **Fig. 3.2**. The starting substrates are *p*-type (Zn-doped, ~4×10^{18} cm^{-3}) InP wafers. A 500 nm thick

p-$In_{0.53}Ga_{0.47}As$ (Zn-doped, ~1×10^{17} cm^{-3}) buffer layer and a 300 nm thick *p*-$In_{0.53}Ga_{0.47}As$ (Zn-doped, ~1.23×10^{16} cm^{-3}) channel layer are sequentially grown. In the beginning, 100 cycles thick Al_2O_3 and 420 nm thick SiO_2 isolation layer were deposited on the substrates, and then the active area (AA) was patterned by optical lithography. After cleaned by acetone, IPA, and diluted HCl, the substrates were transferred to ALD chamber for the deposition of gate oxide. Then, 10 cycles TMA treatment was performed before the subsequent 100 cycles Al_2O_3 and 50 cycles HfO_2 deposition at 250 ^oC. After the deposition of gate oxide, the samples were followed by PDA 300 ^oC for 120 s in N_2. Ti/Pt (5 nm/ 100 nm) gate deposition by sputter and gate patterning were carried out. Following gate stack formation, a 30 nm Ni was also deposited by sputter and RTA was performed at 250 ^oC for 30 s and 300 ^oC for 60 s in N_2 for the formation of Ni-InGaAs as S/D regions. Concentrated HCl was able to remove unreacted Ni with its good selectivity between Ni and Ni-InGaAs alloys. Subsequently, 100 nm SiO_2 was deposited as the passivation layer and contact holes were patterned by optical lithography. Finally, Ti/Pt for the S/D pad and back contact electrode was sputtered.

3.3 Failure analysis

The reason why the devices can't work may be the junction parts of MOSFETs. Even though we found the good rectifying behaviors (on/off ratio~ 10^5), shown in **Fig. 3.3**, from our junction characteristics (*I-V* curves), it might not be the characteristics of Ni-InGaAs/$In_{0.53}Ga_{0.47}As$ junction. We speculate that this Schottky junction characteristics might be the Pt(metal pad)/*p*-$In_{0.53}Ga_{0.47}As$ diode. Ideally, we can verify that whether the Ni-InGaAs is formed by SBH. In ideal case, the SBH for

electron of Ni-InGaAs/$In_{0.53}Ga_{0.47}As$ and Pt/$In_{0.53}Ga_{0.47}As$ contact is 0.7 eV and 1.1 eV, respectively. However, we observed that SBH is relatively independent of the work function of the metal from reference [2], shown in **Fig. 3.4**. The relative constancy of the barrier height with various work function metals is sometimes attributed to Fermi level pinning, where the Fermi level is almost pinned at the charge neutrality level (CNL). The CNL for $In_{0.53}Ga_{0.47}As$ is near the conduction band, shown in **Fig. 3.5**, which also indicates that the SBH is almost pinned in the vicinity of the conduction band edge. The thermionic current-voltage relationship of Schottky barrier diode, neglecting series and shunt resistance, is given by

$$I = I_S(e^{\frac{qV}{\eta k_B T}} - 1)$$
$$I_S = AA^*T^2 e^{\frac{-q\Phi_B}{k_B T}} \quad \textbf{[3.2]}$$
$$A^* = \frac{4\pi q k_B^2 m^*}{h^3}$$

Where I_s is the saturation current, A the diode area, A^* Richardson's constant, Φ_B the effective barrier height, and η the ideal factor. Among the current-voltage methods, the ideal factor η and the effective barrier height Φ_B are determined by the slope of the semilog I versus V curve and its intercept of zero bias (V=0), respectively. For the samples with RTA 250 ^oC for 30 s, η is 1.28 and Φ_B is 0.16 eV, while η is 1.21 and Φ_B is 0.14 eV for the sample with RTA 300 ^oC for 60 s. This result corresponds to the fact that E_F is pinned near the conduction band edge for the CNL of $In_{0.53}Ga_{0.47}As$. Therefore, other methods such as TEM and energy dispersive X-ray (EDX) are used to judge whether Ni-InGaAs is formed. **Fig. 3.6** shows the cross-sectional TEM image of self-aligned metal S/D structure. There is no obvious color difference at the S/D region part of substrate, which can distinguish Ni-InGaAs from $In_{0.53}Ga_{0.47}As$ substrates. Evidence which Ni-InGaAs may not be formed is also seen by EDX analysis, demonstrated in **Fig. 3.7 (a)** and **(b)**. The positions 1 and 2 where we did

EDX analysis are shown in **Fig. 3.6**. It is noted that the amounts of Ni in both graphs are few, which indicates that there is no formation of Ni-InGaAs at this region. One of the possible reasons that the Ni-InGaAs cannot be formed is the thin native oxides existing between Ni and $In_{0.53}Ga_{0.47}As$ channel layer. Before loading to the sputter, the samples were cleaned by diluted HCl for 2 min. We suppose that the regrowth of native oxides happened during the loading time. Hence, surface pre-clean before deposition of Ni might be a critical point in order to avoid this uncertainty.

3.4 Summary

The good rectifying characteristics of Pt/*p*-$In_{0.53}Ga_{0.47}As$ contacts results from E_F pinning near the conduction band edge even though its ideal SBH for electron is 1.1 eV. In addition, the critical reason why devices are unable to work is the non-formation of Ni-InGaAs alloy, verified by EDX analysis. The native oxides existing between the Ni and $In_{0.53}Ga_{0.47}As$ substrate should be avoided, which may inhibit the formation of Ni-InGaAs alloy.

Reference (Chapter 3)

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[3] Xingui Zhang, Ivana, Hua Xin Guo, Xiao Gong, Qian Zhou and Yee-Chia Yeoz, "A Self-Aligned Ni-InGaAs Contact Technology for InGaAs Channel *n*-MOSFETs," *J. Electrochem. Soc.*, vol. **159**, p. H511, 2012.

[4] Sujith Subramanian, Ivana, Qian Zhou, Xingui Zhang, Mahendran Balakrishnan and Yee-Chia Yeo, "Selective Wet Etching Process for Ni-InGaAs Contact Formation in InGaAs N-MOSFETs with Self-Aligned Source and Drain," *J. Electrochem. Soc.*, vol. **159**, p. H16, 2012.

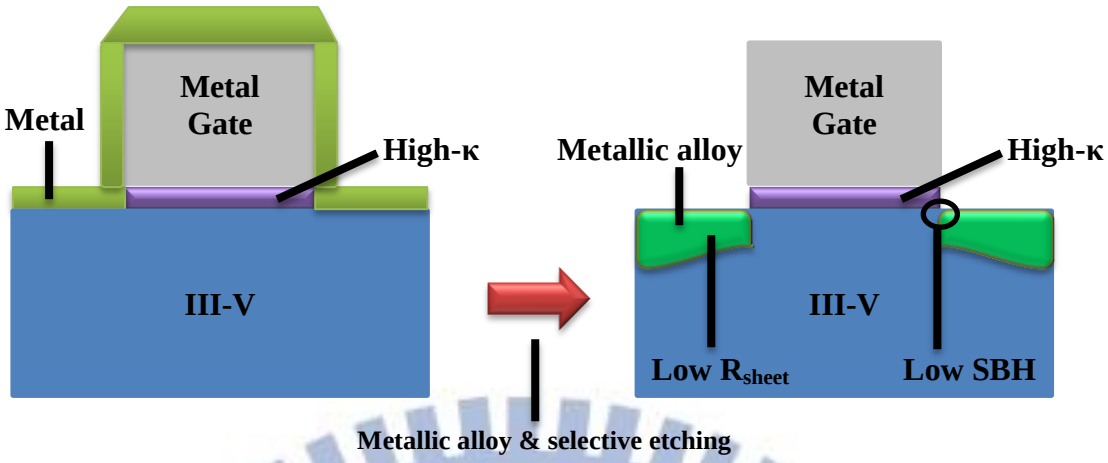


Fig. 3.1 Schematic cross-sectional image and technology requirements of future III-V MOSFETs

Process Flow

- 4200Å SiO_2 field oxide and define AA
- Surface pre-clean
  -Acetone (5min.), IPA (5 min.), HCl (2 min.)
- ALD：TMA treatments (10 cycles) + Al_2O_3 (100 cycles) + HfO_2 (50 cycles)
- PDA 300 ^oC for 120 s in N_2
- Ti/Pt deposition and gate patterning
- Ni-InGaAs S/D formation
  -S/D Ni deposition
  -RTA 250 ^oC for 30 s or 300 ^oC for 60 s
  -removal of unreacted Ni (selective etching by HCl)
- contact hole and metal pad (Ti/Pt)
- back contact (Ti/Pt)

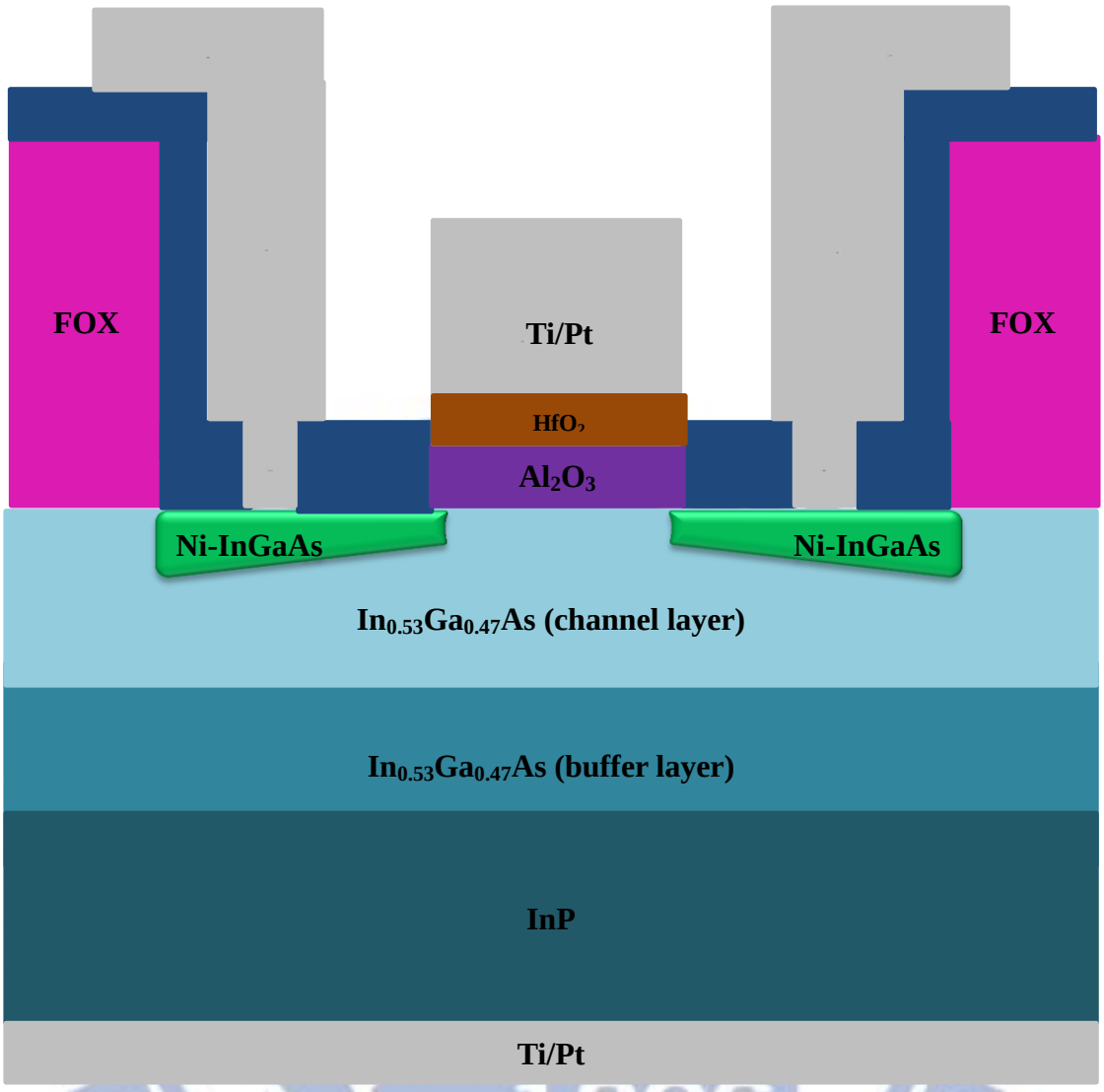


Fig. 3.2 Process flow and device structure of $In_{0.53}Ga_{0.47}As$ channel *n*-MOSFET with self-aligned Ni-InGaAs source and drain

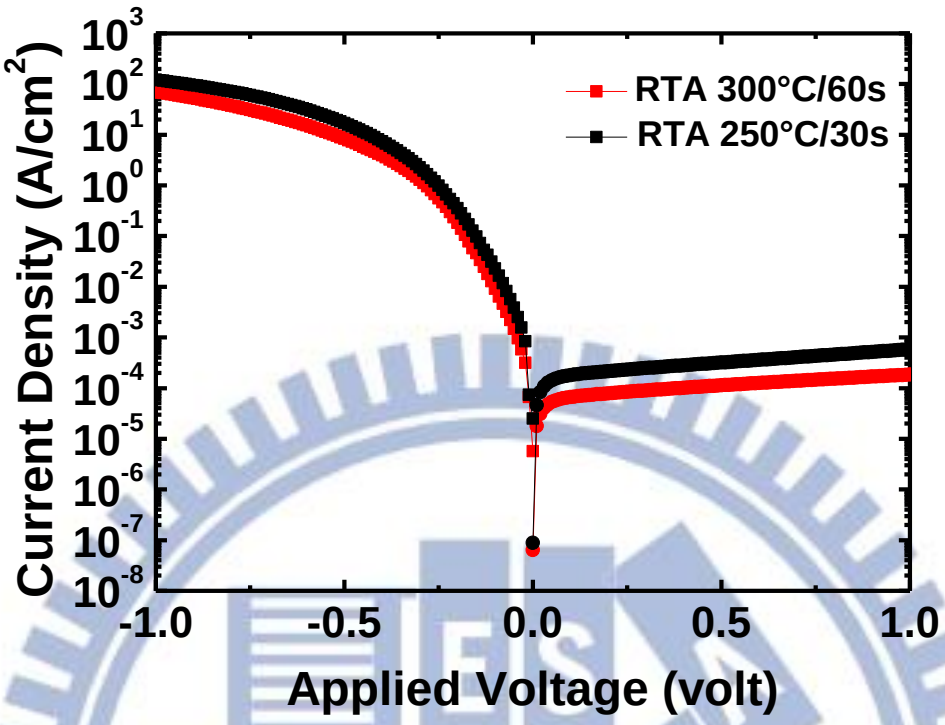


Fig. 3.3 *I-V* characteristics of metal/p-InGaAs diodes with different RTA conditions

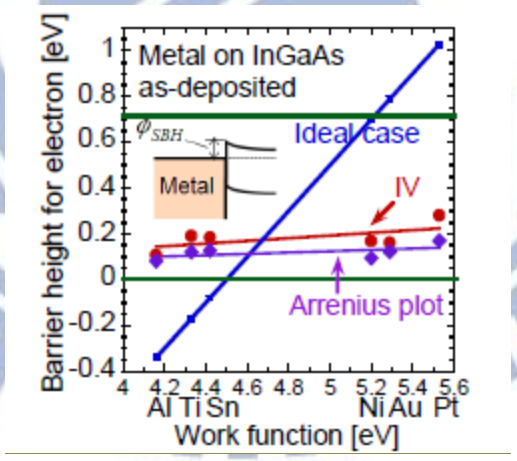


Fig. 3.4 Schottky barrier height (SBH) for electron of a variety of metals/$In_{0.53}Ga_{0.47}As$ contacts from [2]

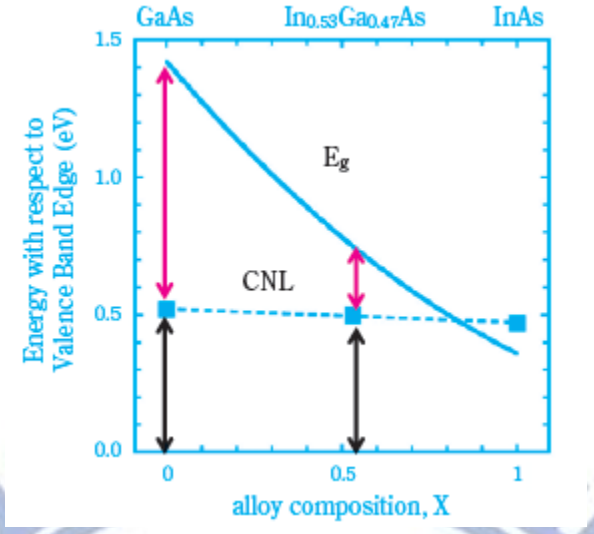


Fig. 3.5 Energy level for charge neutrality level (CNL) in $In_xGa_{1-x}As$

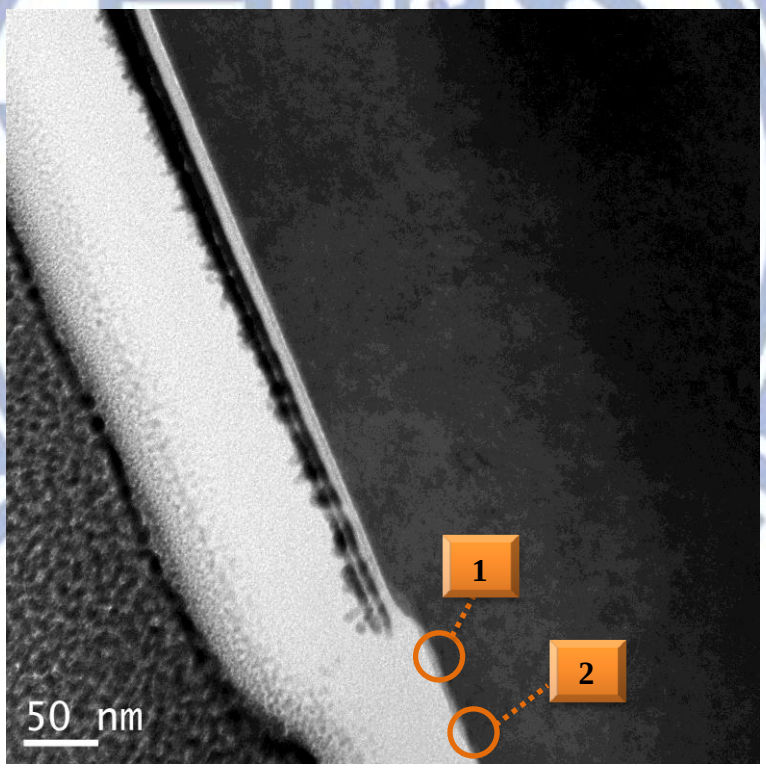
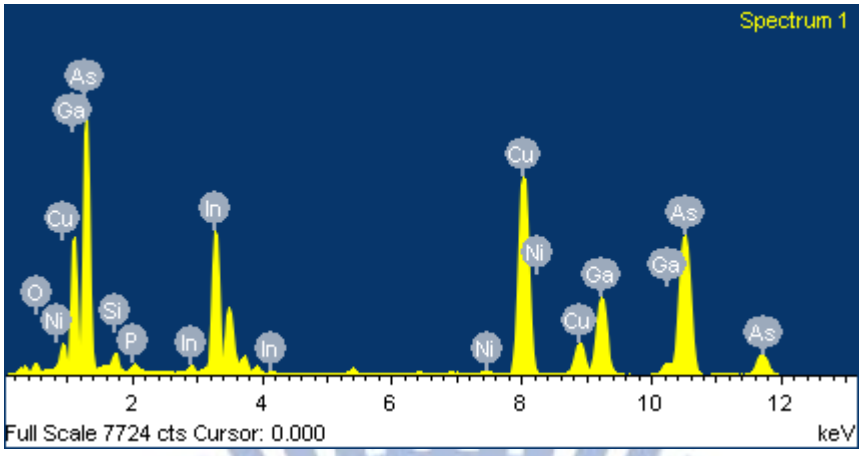
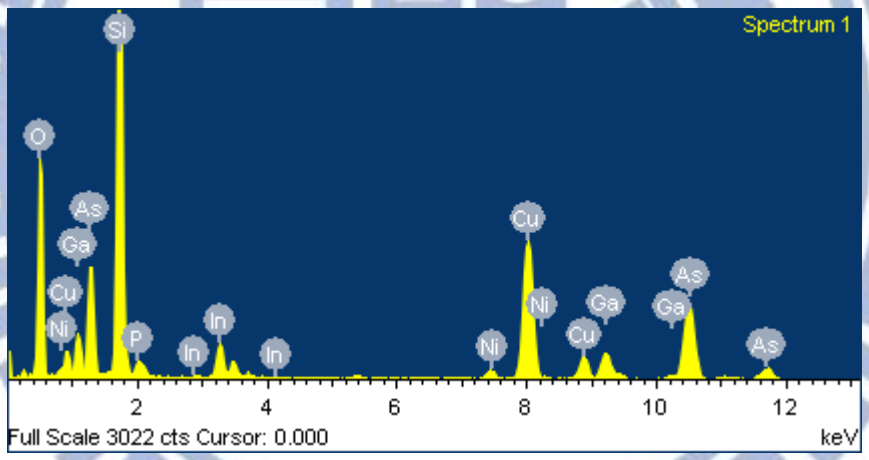


Fig. 3.6 The cross-section TEM image of self-aligned metal S/D structure. 1 and 2 show the positions where EDX analysis was done.



Element	In	Ga	As	Ni	O	Si	P	Cu
Weight (%)	28.30	12.57	29.82	**0.36**	0.98	0.86	0.37	26.74
Atomic (%)	18.18	13.30	29.37	**0.45**	4.50	2.27	0.87	31.05

(a)



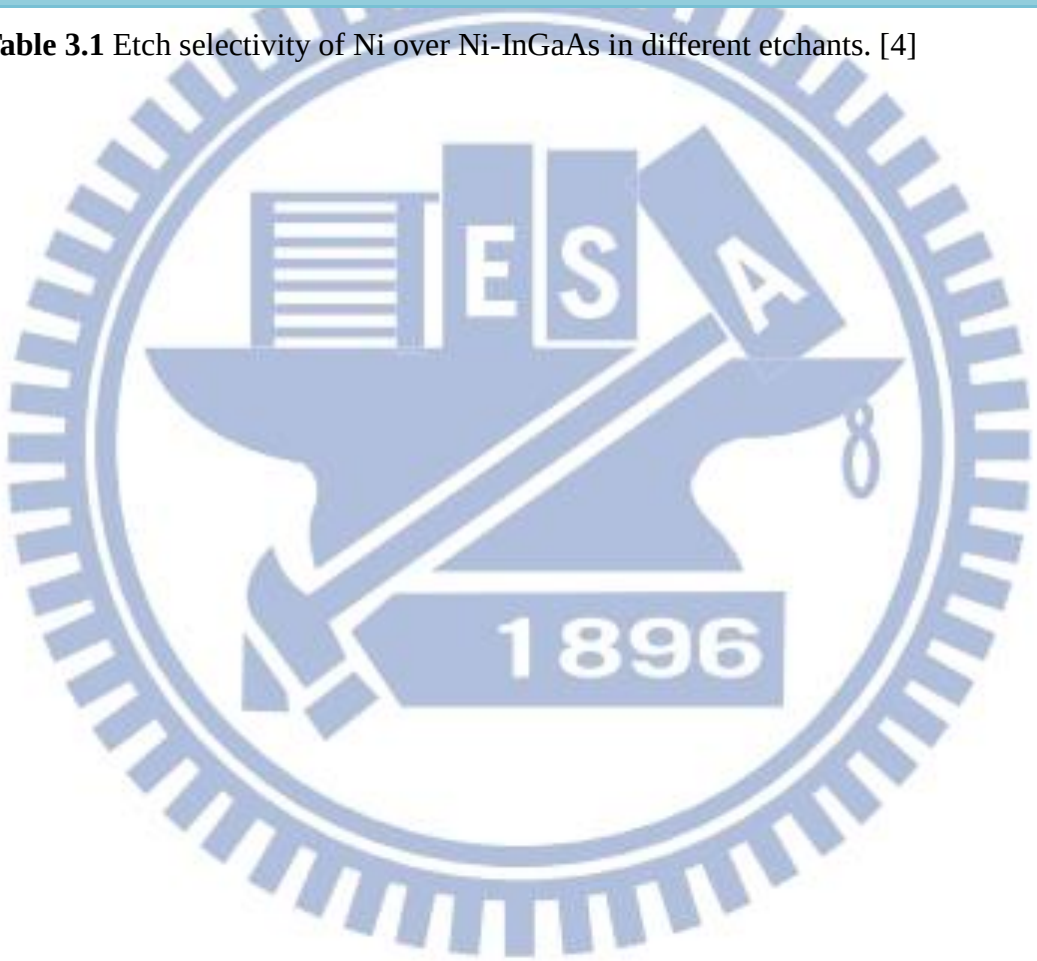
Element	In	Ga	As	Ni	O	Si	P	Cu
Weight (%)	7.44	3.93	16.60	**1.01**	22.05	28.24	0.50	20.22
Atomic (%)	2.10	1.83	7.20	**0.56**	44.77	32.66	0.53	10.34

(b)

Fig. 3.7 (a) and **(b)** show the EDX analysis at position 1 and 2, where the amounts of Ni are few.

Chemical	Selectivity *S* ($r_{Ni}/r_{Ni\text{-}InGaAs}$)
HNO_3 (1:10) 25 °C	4.6
HNO_3 (1:20) 25 °C	4.4
36% HCl 25 °C	15.6
HCl (1:10) 25 °C	2.3
HCl (1:10) 50 °C	1.2
HCl (1:10) 70 °C	1.8
HCl (1:10) 90 °C	2.2

Table 3.1 Etch selectivity of Ni over Ni-InGaAs in different etchants. [4]



Chapter 4

Conclusion

In this thesis, Ti-Pt/Al_2O_3/$In_{0.53}Ga_{0.47}As$(100) MOS capacitors with different conditions of thermal treatments such as PMA, FGA, and PDA were investigated. FGA is able to effectively suppress frequency dispersion in accumulation (*p*-type: 12.34%→8.96% & *n*-type: 8.08%→4.77%) and reduce some, but not all, midgap traps (D_{it} (E_t=0.382 eV): ↓ 19.48% & D_{it} (E_t=0.428 eV): ↓ 22.28%), compared to PMA. Then, we discuss MOSCAPs under various PDA conditions with FGA to find the highest temperature limit of our gate stack. It is noted that MOSCAPs under PDA 500 ^oC for 120 s with FGA demonstrate the worst electrical characteristics such as extremely high frequency dispersion in accumulation (*p*-type: 8.96%→16.91% & *n*-type: 4.77%→5.99%) and higher midgap traps (D_{it} (E_t=0.377 eV): ↑ 322.65% & D_{it} (E_t=0.487 eV): ↑ 117.56%) causing E_F pinning. The XPS spectra of As $2p_{3/2}$ show that the area ratio of As_2O_3 to As_2O_5 becomes lower as the PDA temperature gets higher; therefore, lower extent of the As_2O_3 passivation of the Al_2O_3/$In_{0.53}Ga_{0.47}As$ causes the degradation of interface between Al_2O_3 and $In_{0.53}Ga_{0.47}As$.

Next, Ti-Pt/Al_2O_3/*p*-$In_{0.53}Ga_{0.47}As$(111)A MOS capacitors under various PDA temperature with FGA were studied. The electrical characteristics of the capacitors can be improved by PDA 300 ^oC for 120 s with FGA, for example, the reduction of frequency dispersion in accumulation (14.57%→12.72%) and midgap traps (D_{it} (E_t=0.347eV): ↓ 67%). The XPS spectra of As $2p_{3/2}$ show that the area ratio of As_2O_3 to As_2O_5 is the highest for the MOSCAPs under PDA 300 ^oC for 120 s with FGA, which indicates the lowest interface traps in all the samples. Subsequently, we

compare MOSCAPs with orientation (111)A to orientation (100). It is seen that MOSCAPs with (100)-oriented $In_{0.53}Ga_{0.47}As$ substrates demonstrate better electrical characteristics than MOSCAPs with (111)A orientation. Despite the fact that $Al_2O_3/In_{0.53}Ga_{0.47}As$ (111)A interface has lower As atoms of oxidation states than $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) interface, the area ratio of As_2O_5 to As_2O_3 of orientation (111)A is still higher than that (100). Hence, D_{it} of (111)A is much higher than that of (100).

Finally, the failure of self-aligned Ni-InGaAs S/D $In_{0.53}Ga_{0.47}As$ *n*-MOSFETs is attributed to the non-formation of Ni-InGaAs according to the TEM images and EDX analysis. Surface pre-clean before the Ni deposition is very important, avoiding the regrowth of native oxides during the loading time preventing the formation of Ni-InGaAs. In the future, we hope our device can be successfully fabricated by solving these problems mentioned above. In addition, we suggest that the gate oxide, Al_2O_3, could be replaced by Al_2O_3 (thin)/HfO_2 (thick) double layers or other high-κ oxides such as ZrO_2, which EOT can further be scaled down. Devices with Si- or Ge-doped S/D with Ni-InGaAs contact are also a promising method to suppress the junction reverse leakage current significantly.

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原子層沉積三氧化二鋁介電層於砷化銦鎵金氧半電容之電性與化性的研究

Study on Electrical and Chemical Characteristics of Indium Gallium Arsenide Metal-Oxide-Semiconductor Capacitors with Atomic-Layer-Deposited Al_2O_3 Gate Dielectric