Chapter 1

Introduction

1.1 Background and Motivation

With the down-scaling of device dimensions, the atomic-level fluctuations such as random dopant fluctuation (RDF) [1], [2] and line edge roughness (LER) [3]–[6] have become critical for nanoscale CMOS [7], [8], [9]. More importantly, random variation may hinder the scaling of supply voltage and therefore aggravate the power dissipation problem [7], [8], [9]. The thinner EOT provided by high-k metal-gate can mitigate the threshold-voltage (V_{th}) variability [8], [10] from most sources of random variation (e.g., random-dopant fluctuations, see Fig.1.1 [4], and line-edge roughness, see Fig.1.2 [4]). However, metal-gate creates a new source of random V_{th} variations, and this variation depends on the work-function of the orientation of metal crystal grain (see Fig.1.3 [11]). Because of different surface atom density corresponding to different orientation, the variation in the grain orientation results in the work-function variation (WFV) [12].

According to the ITRS roadmap [13], FinFET and Ultra-Thin-Body (UTB) SOI devices are important device structures for CMOS scaling because of their short-channel-effect immunity and robustness against random dopant fluctuations. The 3D FinFET architecture has been adopted by Intel in 22nm generation [14], and STMicroelectronics has presented its 28nm CMOS platform with UTB fully depleted

SOI [15]. However, the variability of FinFET and UTB SOI devices is different from bulk metal-oxide-semiconductor field-effect-transistor (MOSFET) devices. For lightly-doped FinFET and UTB SOI devices, fin-LER and gate-LER have been significant variation sources, respectively [16], [17]. Recently, Japanese AIST has investigated FinFET variability sources systematically [11], [18], and the variability has been compared with the bulk MOSFET. For lightly doped of undoped FinFET, WFV has been reported to dominate the overall V_{th} variation, and the importance of WFV increases with decreasing of gate area and increasing grain size. Furthermore, Fan et al. [19], [20] studied UTB SOI SRAM and FinFET SRAM, and indicated that the WFV and LER might be the dominate variation sources for subthreshold application. In additional, tunneling FET (TFET) is also a promising device for future technology node. TFET deivce uses electron band-to-band tunneling for device turn on. Compare with the conventional diffusion mechanism, the TFET device employ different turn-on mechanism. Therefore, TFET device provides smaller subthreshold swing (below 60mv/dec. at room temperature), and TFET can be operated with lower VDD. However, Intel has reported that WFV will be a critical I_{off} variation source in TFET device [21].

To investigate the impact of WFV on nanoscale devices, an adequate WFV simulation method is needed. As reported in previous papers [12], [22]-[24], several approaches were adopted to estimate the effects of work-function variation (WFV). For example, Dadgour *et al*. [12], [22] derived a model considering the number fluctuation of metal grains. This model only considers the number fluctuation of two different grains for a given grain number (N_{grain}) and can be expressed as:

$$\sigma V_{th} = \sqrt{\frac{1}{N_{grain}}\left(\sum_{i=0}^{N_{grain}}(P_i\Phi_i^2) - \sum_{i=0}^{N_{grain}}(P_i\Phi_i)^2\right)} \quad (1.1)$$

$$\text{with } P_i = \frac{N_{grain}}{i!(N_{grain}-i)!}(P_1)^i(P_2)^{N_{grain}-i} \quad (1.2)$$

$$\text{and } \Phi_i = \frac{i}{N_{grain}}(\psi_1)\frac{N_{grain}-i}{N_{grain}}(\psi_2), \quad (1.3)$$

where ψ_1 and P_1 are the work function and probability of metal grain for orientation 1, and ψ_2 and P_2 are the work function and probability of metal grain for orientation 2. To improve the number fluctuation model, Cheng *et al*. [23] studied WFV by 3D simulation and described metal grain by square pattern. However, this simulation method can not exactly describe the shape of metal-grain due to its uniform square pattern. In addition, Brown *et al.* [24] investigated WFV by digitalizing the metal grain pattern. The digitalized method constructs metal grain by small (e.g., 1nm resolution) and discrete units. However, this method exhibits poor simulation efficiency, and the accuracy depends on the resolution of unit.

In this study, using a novel Voronoi approach to accurately and efficiently account for the grain pattern of the metal gate, we study the impact of WFV on nanoscale devices, and compare the immunity of FinFET and UTB SOI devices to WFV. In addition, tunneling FET (TFET) [25], [26] is also a promising device structure for future technology generations due to its smaller subthreshold swing (below 60mv/dec. at room temperature), and capability to be operated at lower supply voltage. In this work, we will also compare the impact of WFV between TFET and FinFET devices with our proposed Voronoi approach.

1.2 Organization

The thesis is organized as follows: Chapter 2 describes the methodology we use to simulate WFV. Moreover, the characteristics of WFV and its impact on threshold voltage variation are examined. In Chapter 3, the immunity of FinFET and UTB SOI MOSFETs to WFV is compared and explained. In addition, we study the

impact of WFV on TFET. The conclusion is drawn in Chapter 4.

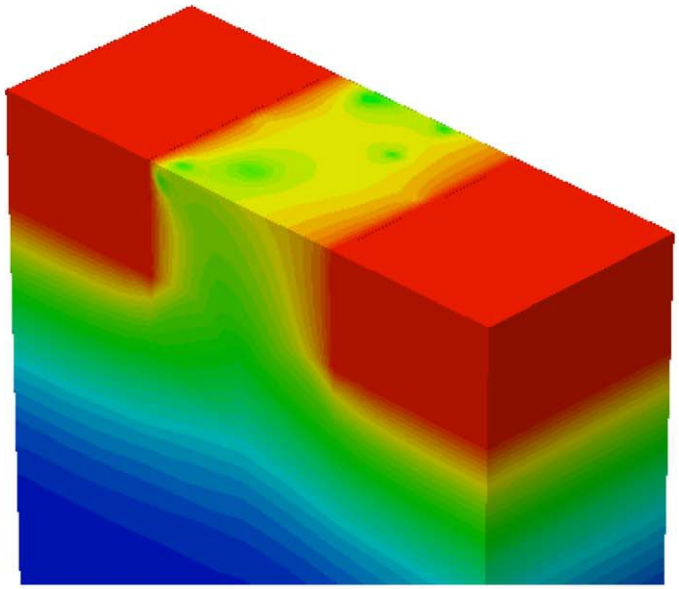


Fig.1.1 Schematic illustrating the phenomenon of random dopant fluctuations [4].

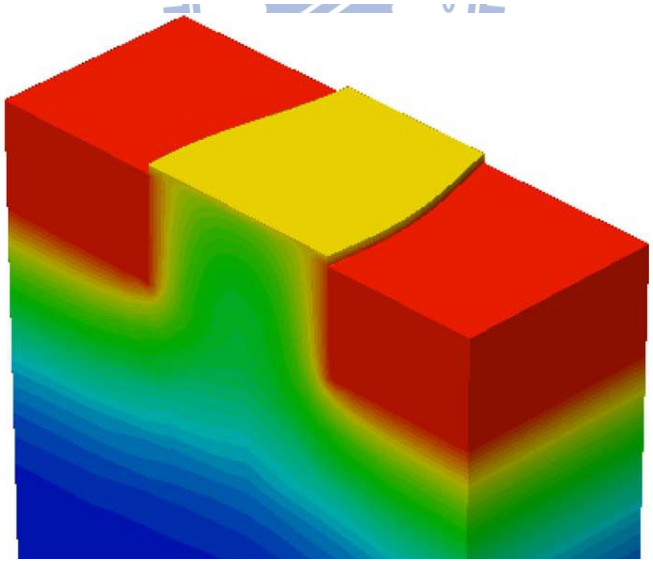


Fig.1.2 Schematic illustrating the phenomenon of gate line edge roughness [4].

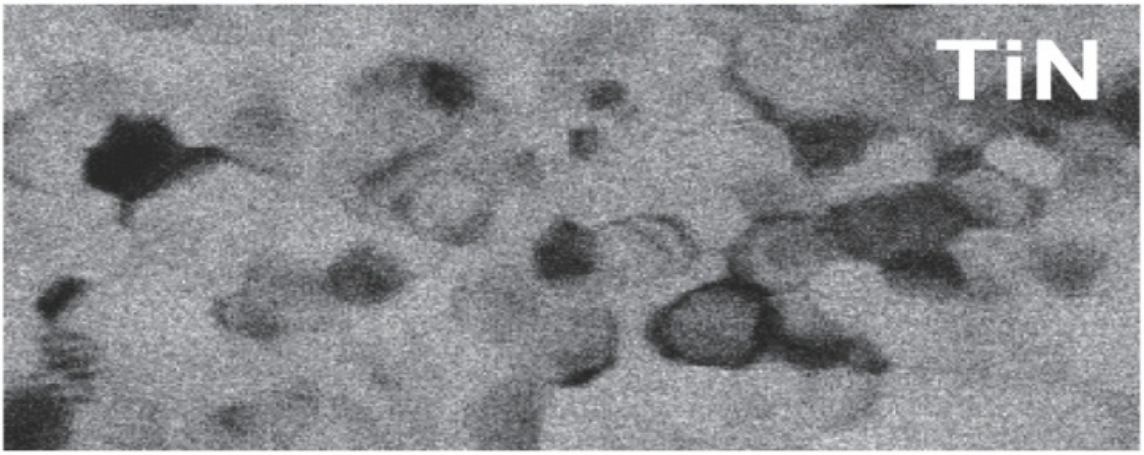


Fig.1.3 Plane view TEM of TiN metal gates. Each grain with different work function induces the WFV [11].

Chapter 2

Simulation and Characteristics of Work-Function Variation

2.1 Introduction

Scaling down of metal-oxide-semiconductor field-effect-transistor (MOSFET) devices beyond 45nm requires high-k/metal-gate [27]. However, metal gate introduces a new source of random V_{th} variations due to the variation in the orientation of metal crystal grains. Because of different surface atom density corresponding to different orientation, the variation in the orientation results in the work-function variation of nanoscale devices [12].

As reported in previous papers [12], [22]-[24], several approaches were adopted to estimate the effects of work-function variation (WFV). For example, Dadgour *et al*. [12], [22] derived a model considering the number fluctuation of metal grains. This model only considers the number fluctuation of two different grains for a given grain number (N_{grain}) and can be expressed as:

$$\sigma V_{th} = \sqrt{\frac{1}{N_{grain}}\left(\sum_{i=0}^{N_{grain}}(P_i\Phi_i^2) - \sum_{i=0}^{N_{grain}}(P_i\Phi_i)^2\right)} \quad (2.1)$$

$$\text{with } P_i = \frac{N_{grain}}{i!(N_{grain}-i)!}(P_1)^i(P_2)^{N_{grain}-i} \quad (2.2)$$

$$\text{and } \Phi_i = \frac{i}{N_{grain}}(\psi_1)\frac{N_{grain}-i}{N_{grain}}(\psi_2), \quad (2.3)$$

where ψ_1 and P_1 are the work function and probability of metal grain for orientation 1, and ψ_2 and P_2 are the work function and probability of metal grain for orientation 2. To improve the number fluctuation model, Cheng *et al*. [23] studied WFV by 3D TCAD simulation and described metal grain by square pattern. However, this simulation method can not exactly describe the shape of metal-grain due to its uniform square pattern (Fig. 2.1). In addition, Brown *et al.* [24] investigated WFV by digitalizing the metal grain pattern. The digitalized method constructs metal grain by small (e.g., 1nm resolution) and discrete units (Fig. 2.2). However, this method exhibits poor simulation efficiency, and the accuracy depends on the resolution of unit.

In this chapter, we propose a novel Voronoi method that can physically consider the interaction between neighboring grains to investigate the impact of WFV on nanoscale devices. We describe the structure and definition of Voronoi method in section 2.2. Moreover, we compare our Voronoi simulation method with other methods and show the characteristics of WFV in FinFET devices in section 2.3.

2.2 Voronoi Method

The Voronoi diagram is named after Georgy Feodosevich Voronoy [28], [29] and constructed by the set of all perpendicular bisector for a given point set. Voronoi diagram has been used to investigate cells, metal grains, and solid state physics [30]. With the assumption that the grain growth rate of each grain is the same for describing metal grain, the grain boundary will locate at the perpendicular bisector of neighboring grain seeds in the Voronoi diagram.

Fig. 2.3 shows the first step for constructing Voronoi diagram. We place the grain seeds randomly and the number of grain seed is determined by the size of grain. The number of grain seed can be expressed as:

$$N_{grain} = \frac{Area}{\pi(\frac{Size_{grain}}{2})^2} . \qquad (2.4)$$

In Fig. 2.4, we connect each seed by straight dash line. Fig. 2.5 shows that we can construct perpendicular bisectors of dash lines, and the perpendicular bisector of each dashed line constructs the grain boundary. Finally, we can construct the Voronoi pattern after the grain seeds and dash lines are removed. From Fig. 2.6, we can see that the irregular shape of grain can physically reflect the grain patterns. The boundaries of Voronoi pattern are used for efficient TCAD simulation..

In this study, we employ TiN as the gate material for both FinFET and UTB SOI MOSFETs. For TiN metal gate, two possible grain orientations (<200> and <111> [22]) with distinct work function and probability should be considered. Table 2.1 summarizes the two-orientation characteristic of the TiN metal gate. To generate various metal-gate grain patterns for macroscopically identical devices, four factors regarding the grain should be considered: (1) seed position (2) shape (3) size (4) orientation. Fig. 2.7(a) shows the simulation flow of our proposed Voronoi approach to simulate WFV. First, the assigned average grain size is used to estimate the number of grains (seeds) for constructing the random Voronoi grain pattern. The determined seeds are randomly placed in the metal gate region (black solid points in Fig. 2.7(b)) and the distributions of seed position are different for each device. With the seed location shown in Fig. 2.7(b), the Voronoi pattern is constructed by connecting the solid lines that are the perpendicular bisector of each dashed line. Fig. 2.8 shows the generated Voronoi pattern for the simulation of WFV in the metal gate region. Notice that in addition to the shape of metal grain, the effective work function for each grain

varies with orientation. Furthermore, Fig.2.9 shows our simulation method is mesh-independent due to the manually-defined pattern. Therefore, this method can maintain efficiency and accuracy simultaneously with rough meshes (mesh size of metal gate ≈ 1.5nm in this work).

To reduce the load for 3D WFV simulation, we can further merge the neighboring grains with the same orientation. Fig.2.10 demonstrates the merging of grains. We can reduce the usage of vector for polygons by dynamic programming for reducing the cost of memory. Note that the grain which is surrounded by grains with different orientation should be preserved (Fig.2.11), so we will not merge the grains to from a circle.

2.3 Results and Discussion

Based on our Voronoi approach, we perform atomistic Monte Carlo simulation to investigate the impact of WFV on FinFET devices [31] (Fig. 2.12). Fig. 2.13 shows the I_d-V_g dispersion for FinFET devices with WFV. As can be seen, the resulting V_{th} dispersion is asymmetric and skews at high V_{th}. The deviation from Gaussian distribution is due to the difference in the orientation probability (see Table 2.1) of the TiN metal gate. The <200> orientation with larger work function possesses higher probability, thus distorting the V_{th} dispersion to higher value. It should be note that different from the method proposed in this work, the Square grain method [23] that uses the square pattern for each grain (Fig. 2.1(a)) exhibits abrupt electric field change near the grain boundary. Fig. 2.14(a) shows the significant change in electric field at channel surface using the Square grain method, while the irregular grain shapes by

using the Voronoi method can faithfully account for the interaction between neighboring grains and thus smooth the electric field near the grain boundary (Fig. 2.14(b)). Furthermore, Fig. 2.15 and Fig. 2.16 compare the contour plots of electric field at channel surface with Voronoi and square method for grain size = 10nm. Compared with Fig. 2.15, Fig. 2.16 shows significant electric field change between the grains with different work function.

In Fig. 2.17, we compare the V_{th} dispersion of the Voronoi and Square method for FinFET devices with various grain sizes. It can be seen that as the grain size increases, the V_{th} variation becomes broader and the distribution extends to the V_{th} extreme values bounded by the work function difference between the two orientations (0.2 eV). Besides, obvious discrete V_{th} dispersion is observed for the Square method whereas the Voronoi method is still able to reflect the continuous V_{th} dispersion at grain size = 25nm.

In addition to these two simulation approaches, the model in (i.e., Eqn. (1)) that only considers the number fluctuation of the two different grains is also examined. Fig. 2.18 shows a comparison of the WFV-induced V_{th} variations among the three methods. It can be seen that the model in [12], [22] (Eqn.(1)) shows higher sensitivity to grain number (i.e., grain size) because it merely considers the grain number fluctuation, while the other two simulation methods show a saturated trend in V_{th} variation [23] as the grain size approaches the size of device gate area. In addition, the discrepancy between the Voronoi and Square methods increases with increasing grain size, and the V_{th} variation predicted by the Square method overestimates the influence of WFV-induced variability.

The accuracy of the digitalized method [24] is similar to Voronoi method with high resolution. However, the high resolution of the digitalized method would make efficiency degrade. In Fig. 2.19, we compare the time efficiency between Voronoi

method and digitalized method for FinFET devices. It can be seen that Voronoi method can maintain accuracy and efficiency simultaneously, whereas digitalized method involves a trade-off between accuracy and efficiency.

2.4 Summary

We have proposed a new methodology using Voronoi diagram to describe the metal grain variation for WFV simulation. The Voronoi method is capable of considering the impacts of metal-grain position, shape, size, and orientation. Based on our Voronoi method, we investigate the characteristics of WFV in FinFET devices. From the obtained V_{th} dispersion, we can see that our simulation method can faithfully reflect the characteristic variation of metal grains. Using the Voronoi method, we will compare the immunity of WFV between FinFET and UTB SOI devices in Chapter 3.

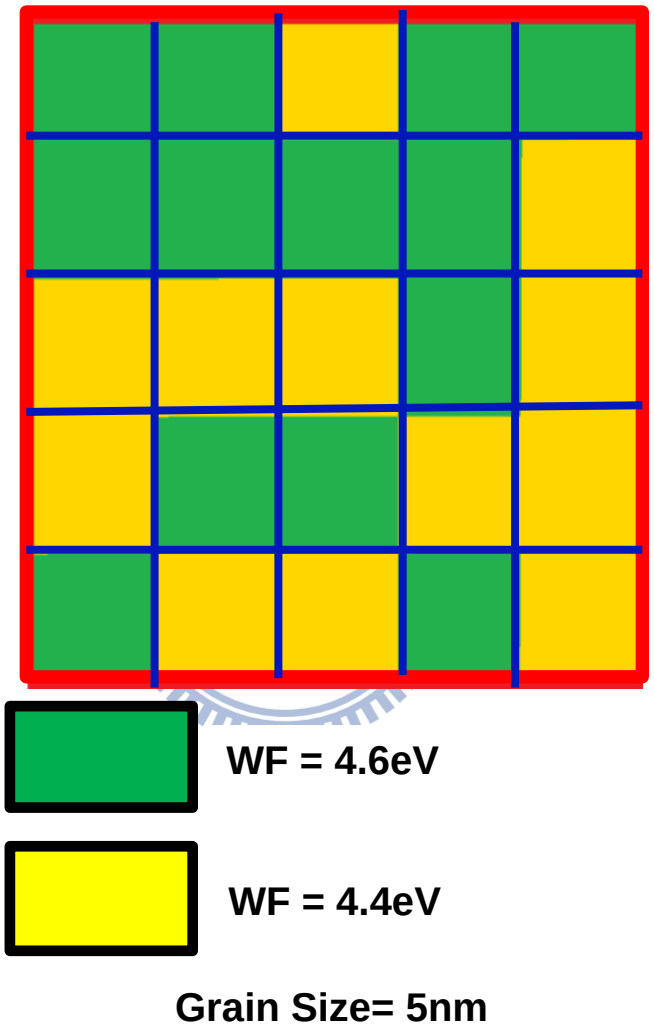


Fig.2.1 Demonstration of square method for determining the WFV pattern.

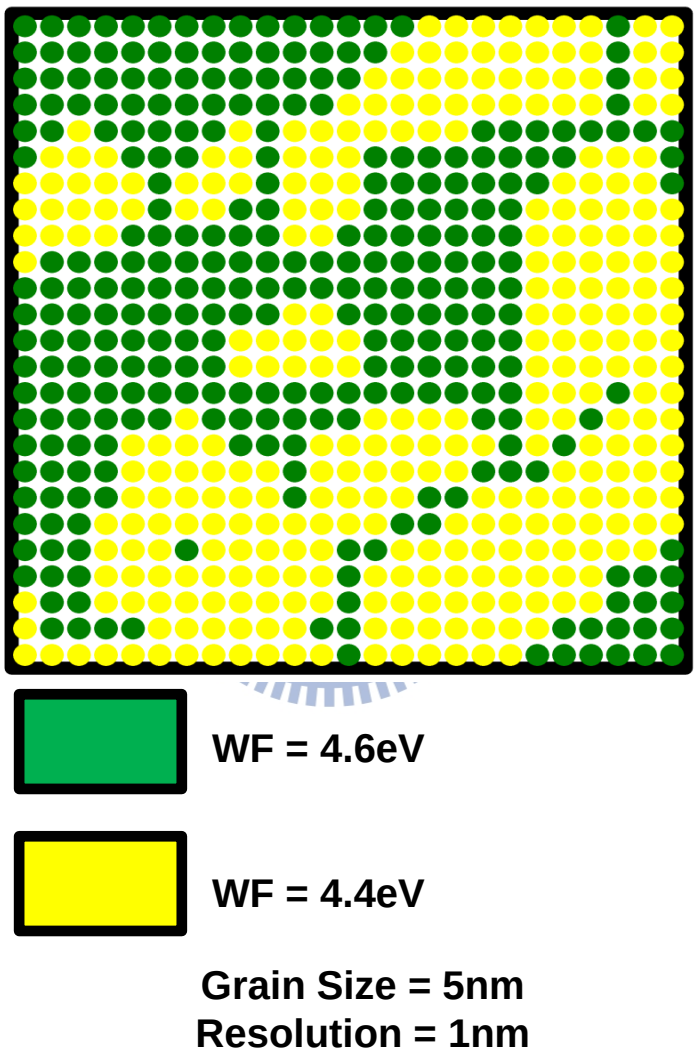
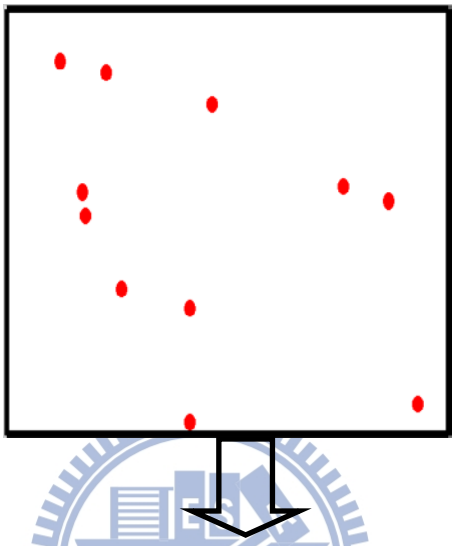


Fig.2.2 Demonstration of digitalized method for determining the WFV pattern.

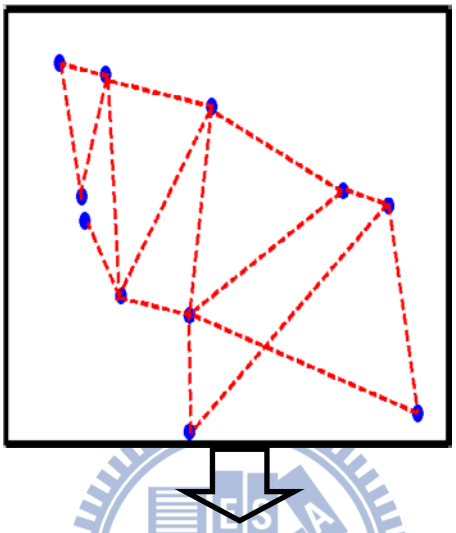


1.Randomly place grain seed

Seed number is determined by grain size

$$N_{grain} = \frac{Area}{\pi(\frac{size_{grain}}{2})^2}$$

Fig.2.3 Step1 for constructing Voronoi pattern.



2. Connect each seed by straight line

Fig.2.4 Step2 for constructing Voronoi pattern.

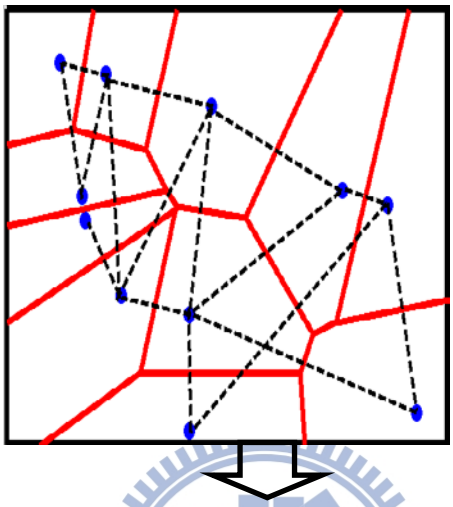
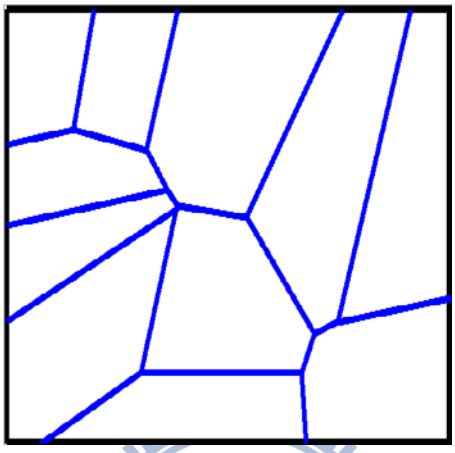


Fig.2.5 Step3 for constructing Voronoi pattern.



4. Final Voronoi Pattern (grain pattern)

Fig.2.6 Step4 for constructing Voronoi pattern.

Table 2.1 Grain orientations with corresponding probability and work function for a TiN metal gate [22].

TiN metal gate		
Orientation	**<200>**	**<111>**
WF [eV]	**ψ1 = 4.6**	**ψ2 = 4.4**
Probability [%]	**60**	**40**

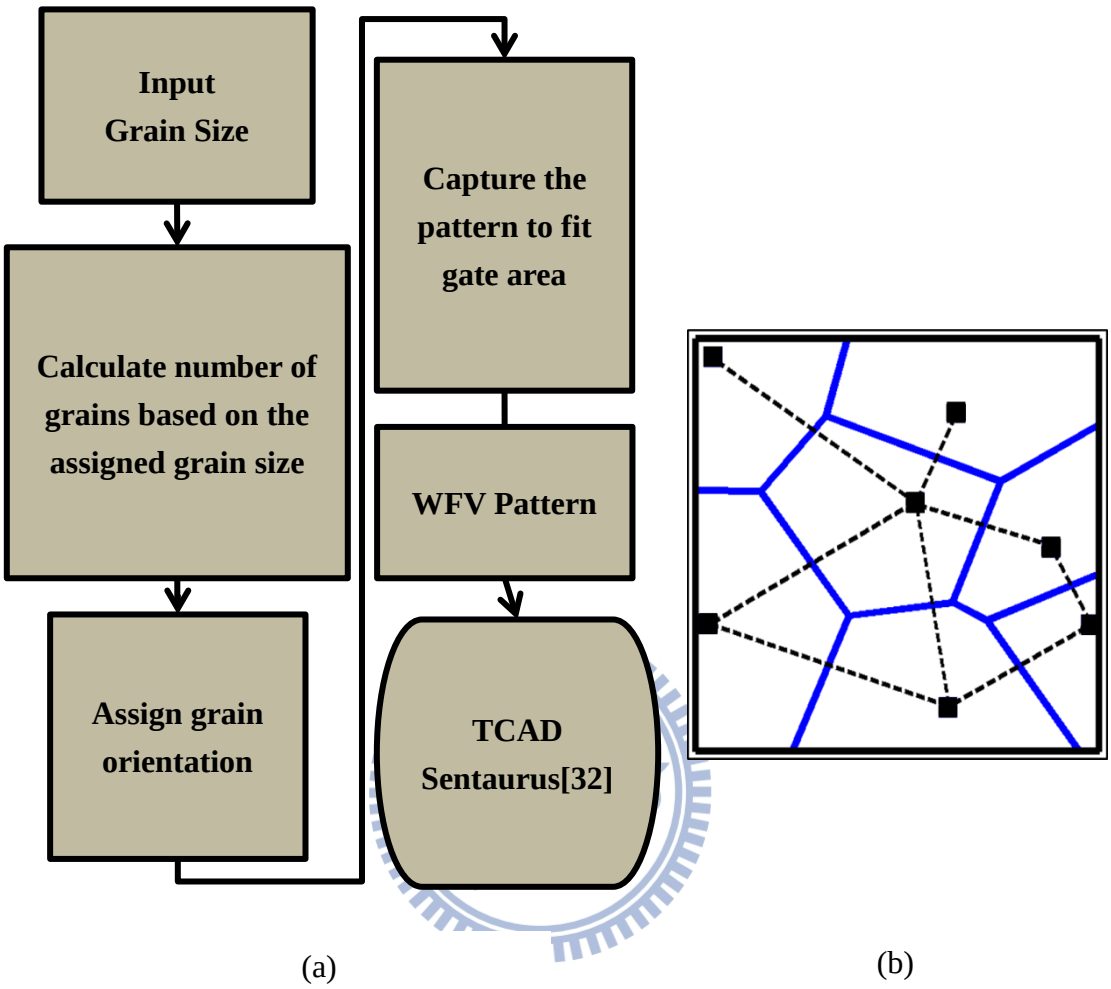


Fig.2.7 (a) Flow chart for determining the WFV pattern (N_{grain} = (Area)/(π×(grain size/2)^2)) (b) Formation of the Voronoi pattern. The solid lines are the perpendicular bisector of dashed lines that connect each grain seed.

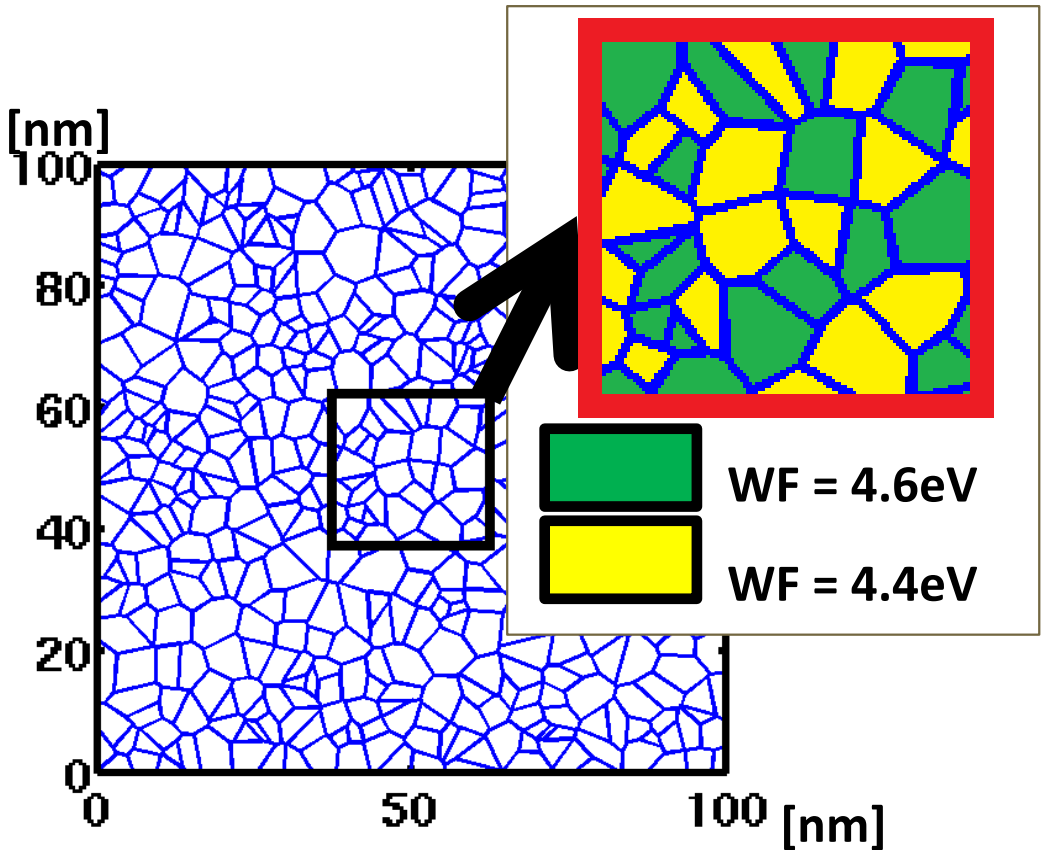


Fig.2.8 The Voronoi pattern is captured for in TCAD simulation.

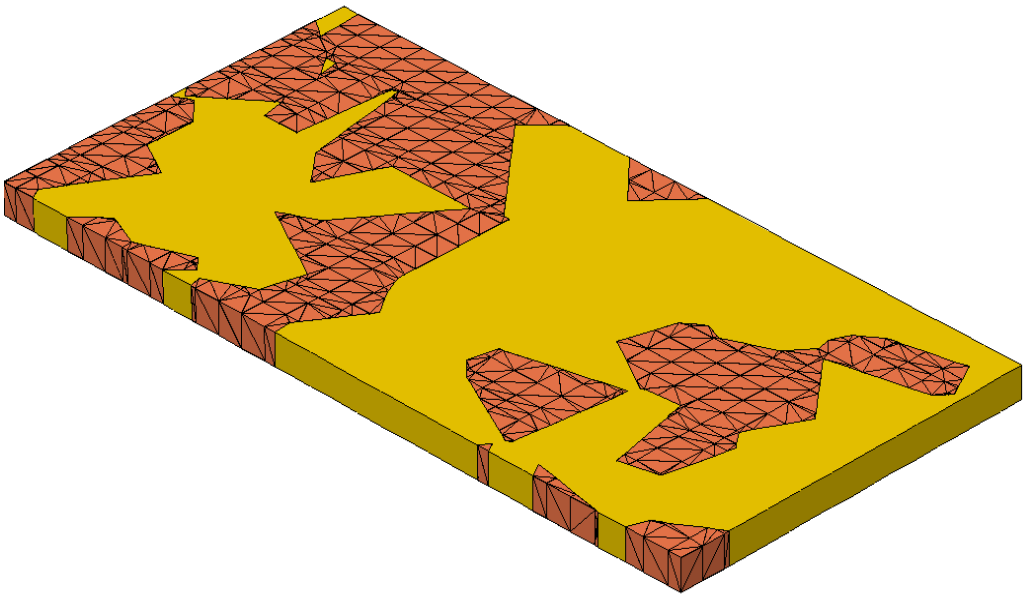


Fig.2.9 The independency of meshes with manually assign Voronoi pattern.

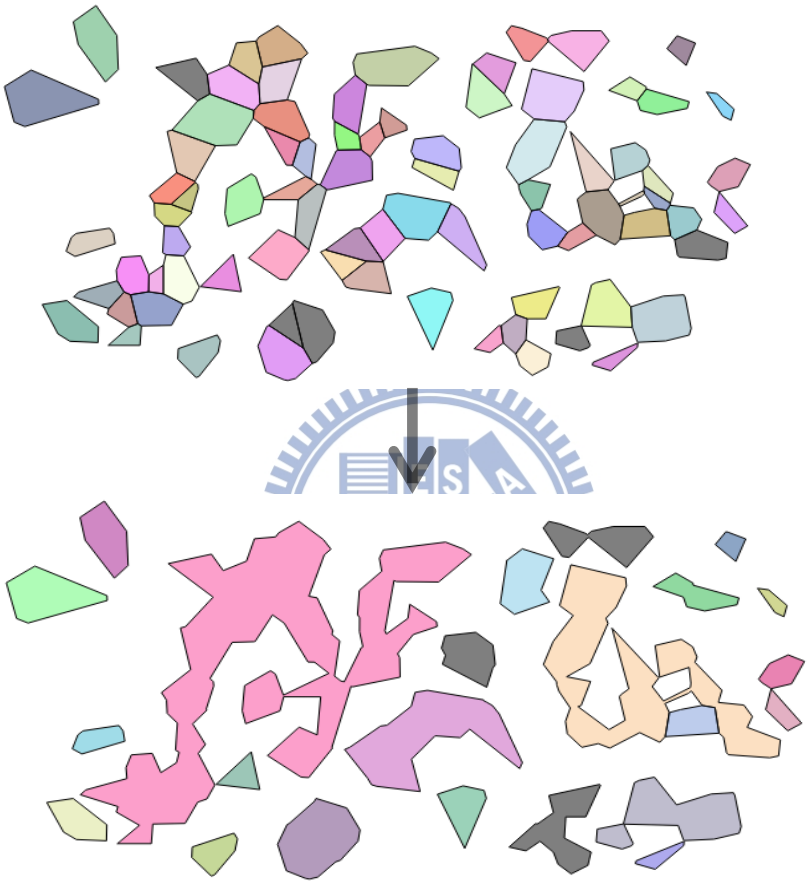


Fig.2.10 Demonstration of merging the neighboring grains with the same orientation.

(a) (b) (c)

Fig.2.11 Cases of merging metal grains for accuracy: (a) unmerged (b) correctly merged (c) wrongly merged.

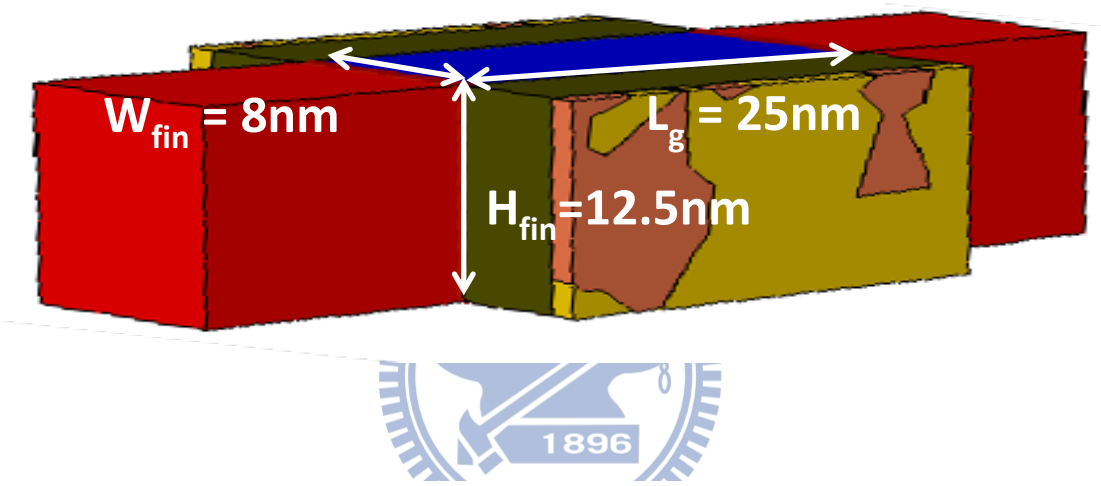


Fig.2.12 Schematic sketch of the FinFET structure with WFV investigated in this study (EOT = 0.65nm, N_{ch} = $10^{17}cm^{-3}$).

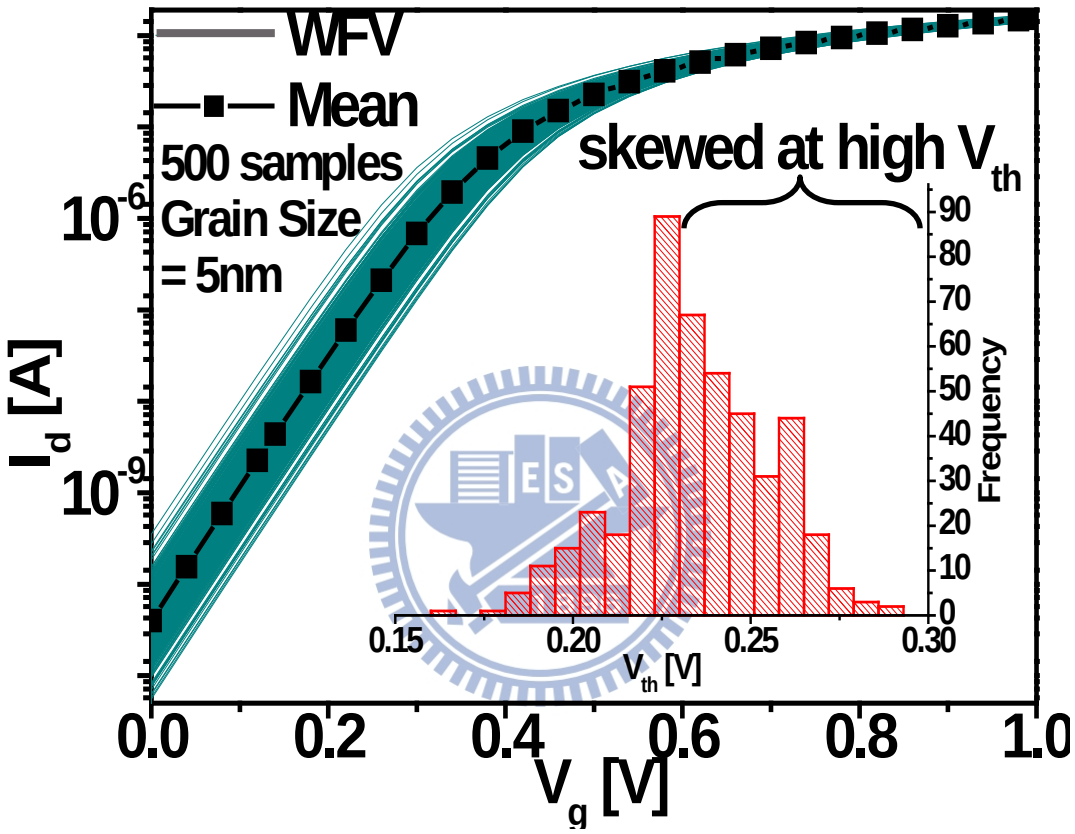


Fig.2.13 The dispersion of I_d-V_g curves (at V_{ds} = 0.05 V) and skewed V_{th}.

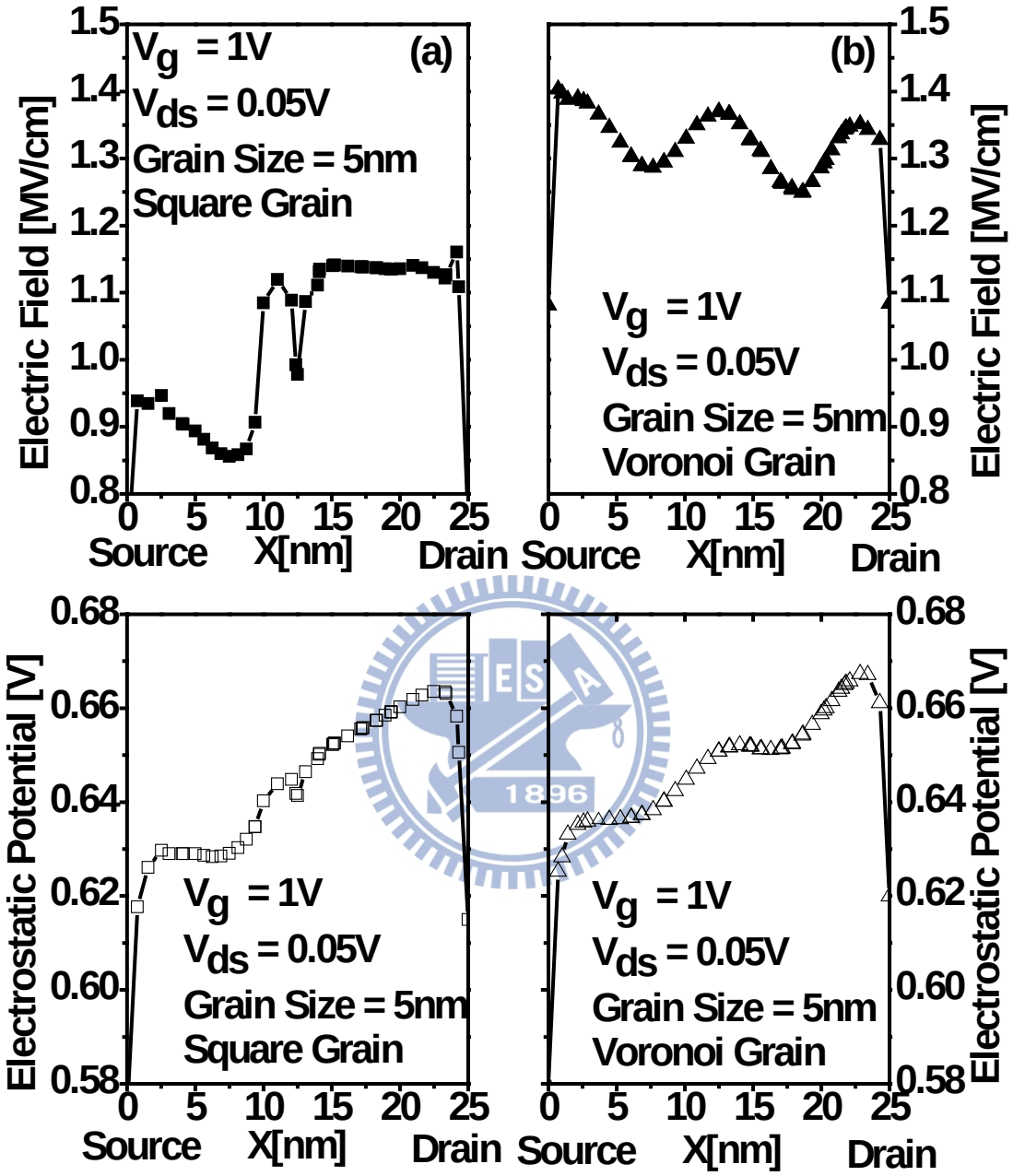


Fig.2.14 Electric field and electrostatic potential at channel surface with two kinds of WFV simulation methods: (a) Square, (b) Voronoi.

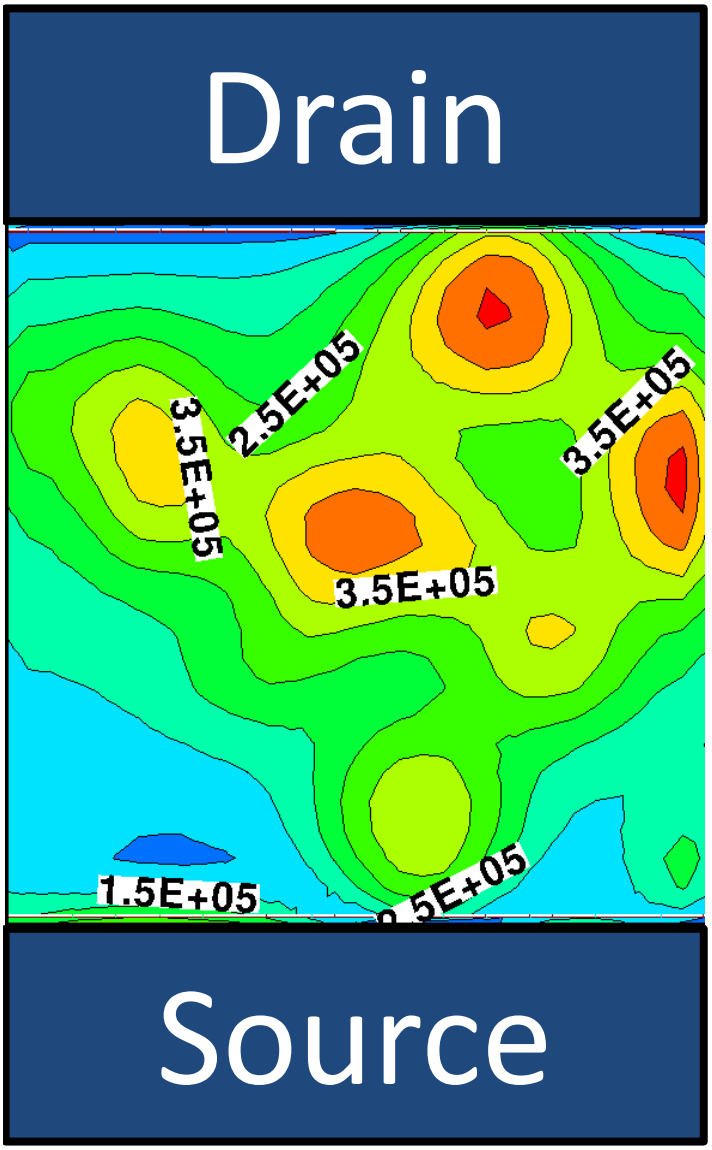


Fig.2.15 Electric field at channel surface with Voronoi WFV simulation methods (grain size = 10nm).

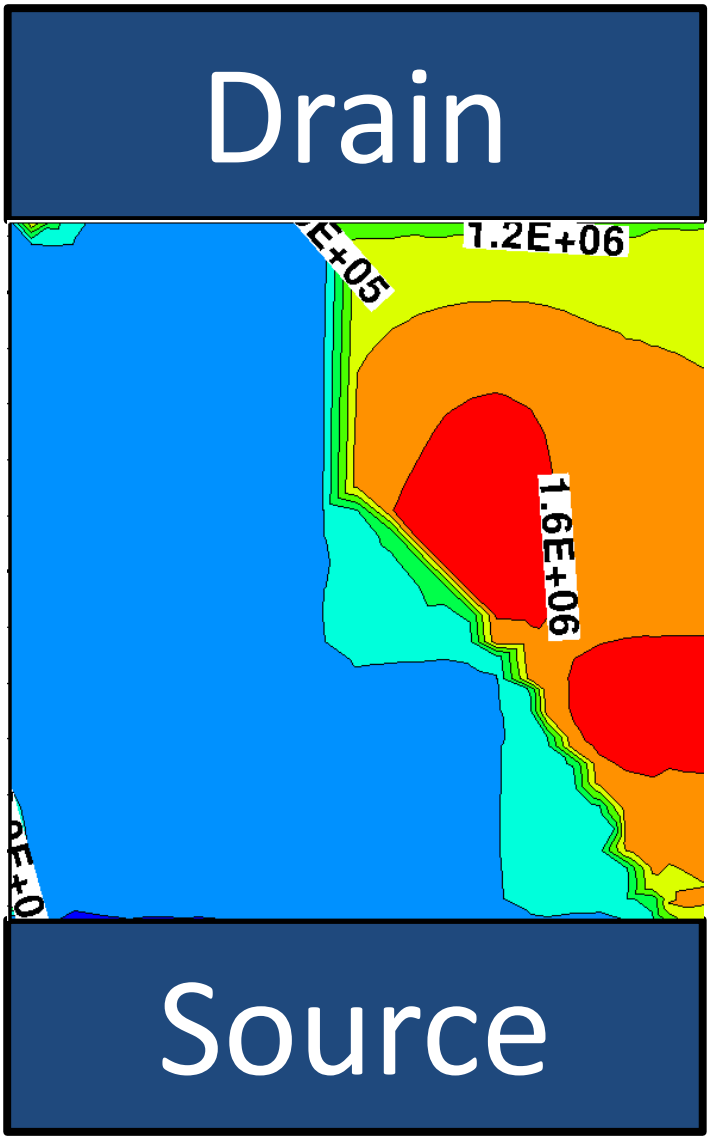


Fig.2.16 Electric field at channel surface with Square WFV simulation methods (grain size = 10nm).

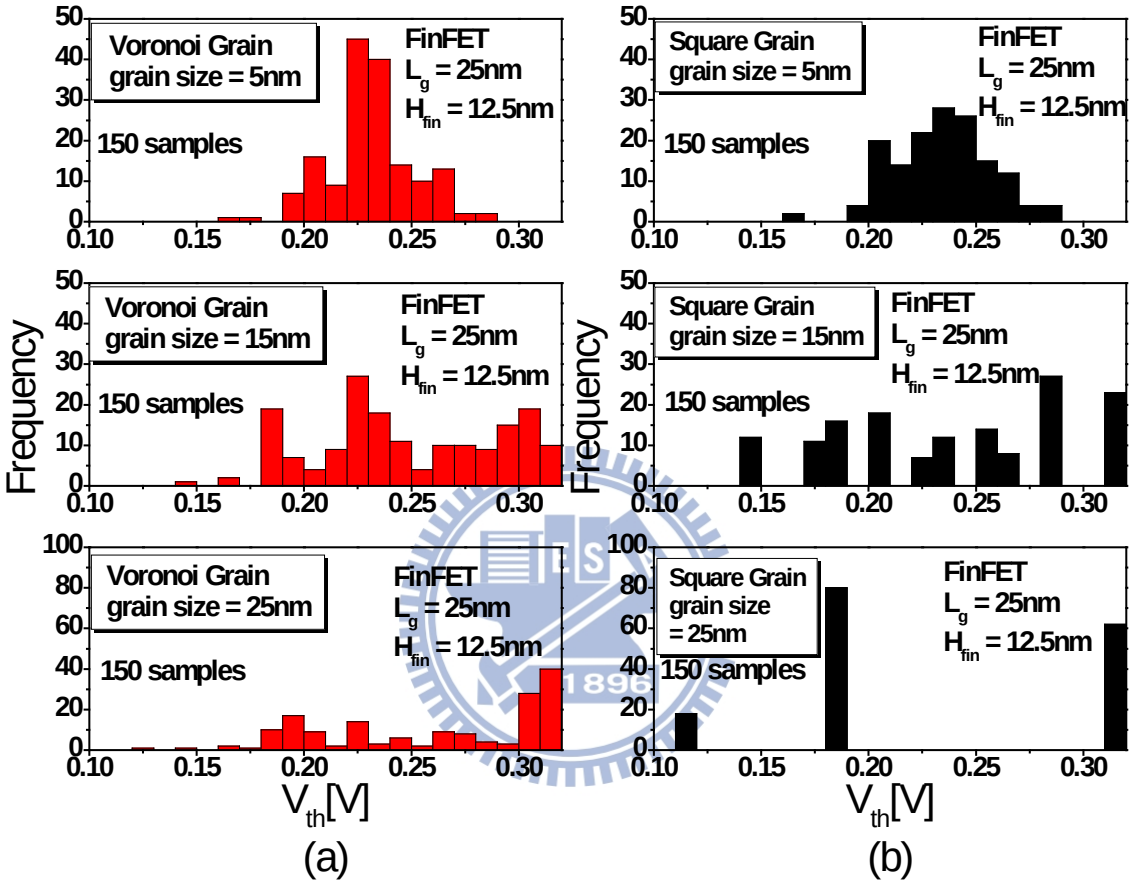


Fig.2.17 V_{th} dispersion from (a) Voronoi grain method and (b) Square grain method with various grain sizes. For the cases with larger grain sizes (15nm, 25nm), unrealistic discrete bars are observed in (b).

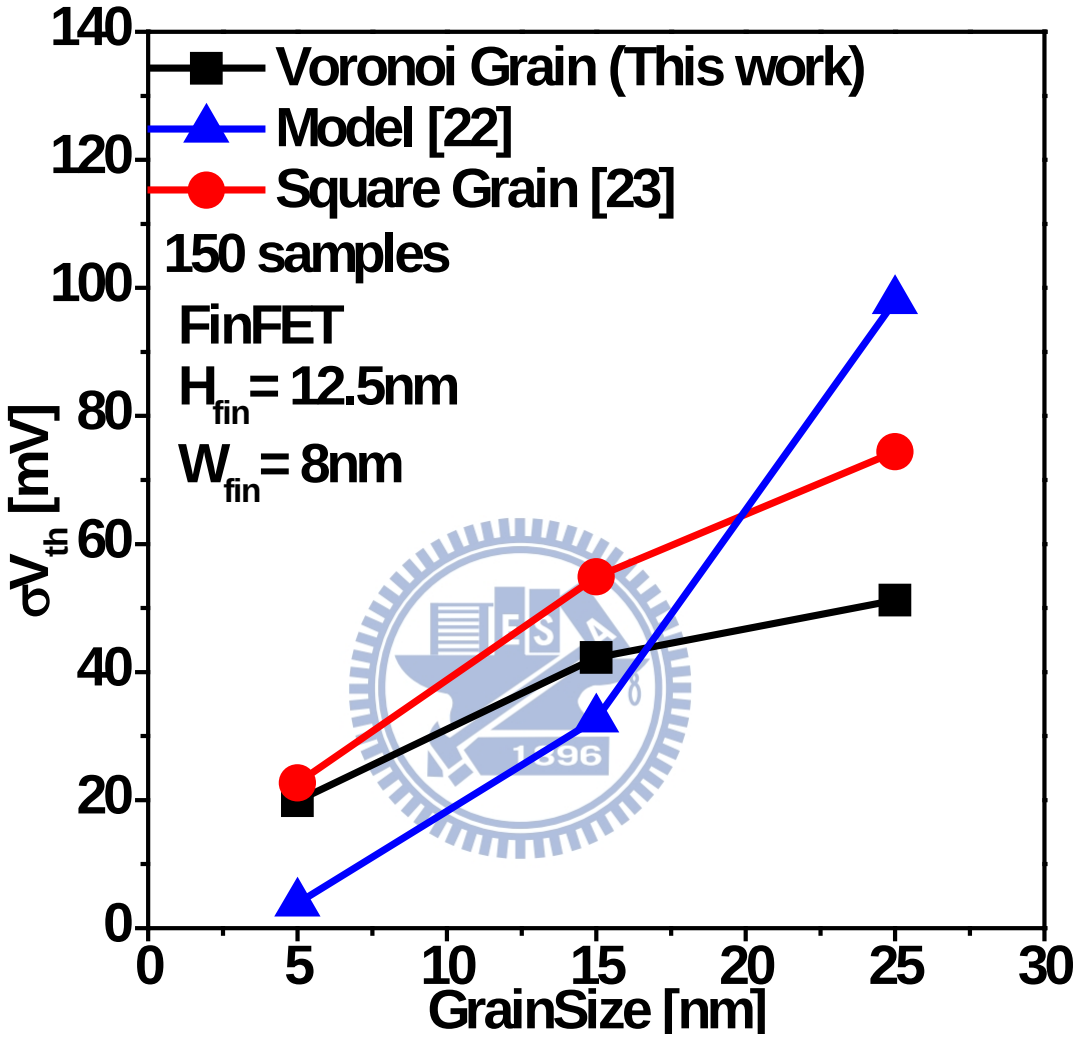


Fig.2.18 Comparison of WFV-induced V_{th} variation FinFET devices for the three methods.

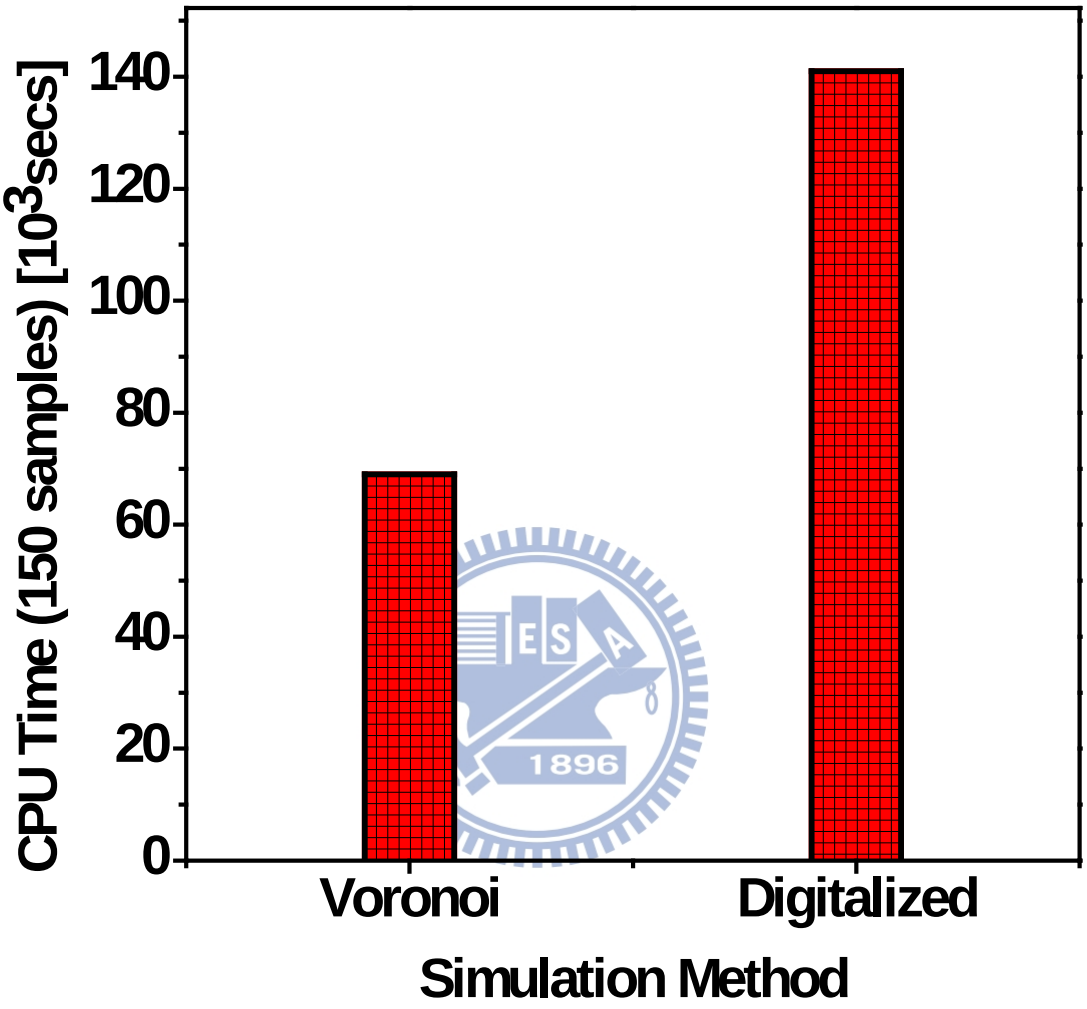


Fig.2.19 Comparison of time consumption for the Voronoi and digitalized methods.

Chapter 3

A Comparative Study of Work Function Variation in FinFET and Ultra-Thin-Body SOI Devices

3.1 Introduction

With the scaling of conventional bulk MOSFETs, variations in transistors due to random dopant fluctuation (RDF) affect the functionality of VLSI circuits [33]. New device structures utilizing lightly-doped channel, such as FinFET and ultra-thin-body (UTB) SOI devices, have been proposed. According to the ITRS roadmap [13], FinFET and UTB SOI devices are the important device structures for CMOS scaling.

However, the variability of FinFET and UTB SOI devices is different from bulk MOSFET devices. Japanese AIST has investigated FinFET variability sources systematically [11], [18], and the variability has been compared with the bulk MOSFET. For undoped FinFET with high-k metal gate, work function variation has been reported to dominate the overall V_{th} variation, and the importance of work function variation (WFV) increases with decreasing of gate area and increasing grain size. Whether the WFV will impact the variability of FinFET and UTB SOI devices differently has rarely been known and merits investigation.

In this chapter, we will compare the impact of WFV on FinFET and UTB SOI devices by using our proposed simulation method in Chapter 2. We compare the immunity to WFV between UTB SOI and FinFET devices in section 3.2. In addition, tunneling FET (TFET) is also a promising device structure for future technology generations due to its smaller subthreshold swing (below 60mv/dec. at room temperature) and capability to be operated at using low supply voltage. In section 3.3, we will also compare the impact of WFV between TFET and FinFET devices with our proposed Voronoi approach.

3.2 Comparison between FinFET and UTB SOI MOSFETs

Using our proposed Voronoi method, we investigate and compare the impact of WFV on FinFET and UTB SOI devices [31]. Fig. 3.1 shows the schematic of FinFET and UTB SOI devices designed with the same total gate area (W_{total} = 25nm) and comparable electrostatic integrity (S.S. ≈ 70 mV/dec) for fair comparison. Other pertinent device parameters are listed in Table 3.1.

Fig. 3.2 compares the WFV-induced V_{th} variation between the two device structures with different grain sizes. As can be seen, the UTB SOI MOSFET is more vulnerable to WFV (larger V_{th} variation) and the difference between UTB and FinFET devices increases with increasing grain size. This can be explained as follows. In the extreme case with grain size close to the device gate area, the possible grain number inside the gate area is close to one and the FinFET device with double-gate structure possesses three possible work-function combinations as illustrated in Fig. 3.3. For the

UTB SOI MOSFET with single-gate structure, however, only two work-function combinations are allowed as shown in Fig. 3.4. In other words, the FinFET device with one more possible work-function combination possesses more averaging effect in WFV, and thus better immunity to WFV than the UTB counterpart.

To further support our explanation, we compare the V_{th} variation for devices with different gate number. From the Fig. 3.5, we can see that quad-gate device shows better immunity to WFV than the FinFET counterpart because of more WF combinations. Fig. 3.6 shows that increasing the number of gate from single-gate UTB SOI to quad-gate device is beneficial to suppressing the impact of WFV. The number of work function combinations (N_{WF}) in the extreme case that the grain size is close to the gate area can be expressed as

$$N_{WF} = \frac{\left(N_{gate}+(N_{orientation}-1)\right)!}{(N_{gate})!*(N_{orientation}-1)!}, \quad (3.1)$$

where N_{gate} and $N_{orientation}$ are number of gates and number of orientations, respectively.

The importance of WFV can be demonstrated Fig. 3.7 where the impact of Fin Line-Edge-Roughness (Fin LER) [34]–[37] on V_{th} variation is compared with that of WFV under various EOT. To assess the Fin LER in FinFET devices, the rough line edge patterns are generated using Fourier synthesis [36] with correlation length = 30nm and rms amplitude = 1.5nm [34] for FinFET MOSFETs. It can be seen that while the Fin-LER induced V_{th} variation can be mitigated by smaller EOT and hence improved EI, the impact of WFV can not be suppressed by EOT scaling.

3.3 Comparison between FinFET and TFET

In addition, tunneling FET (TFET) [25], [26], [38], [39] is also a promising device structure for future technology generations due to its smaller subthreshold swing (below 60mv/dec. at room temperature), and capability to be operated at very low supply voltage. In section 3.3.1, we describe the operation of a basic p-i-n TFET. In section 3.3.2, we will compare the impact of WFV between TFET and FinFET devices with our proposed Voronoi approach.

3.3.1 Operation of TFET

A basic p-i-n TFET structure and its principle of operation is illustrated in Fig. 3.8 and Fig. 3.9. The device structure is equivalent to a gated p-i-n diode operated in reverse-bias mode. If no V_g is applied, the source-channel barrier prevents the flow of drain current. With a certain amount of V_g the band-to-band tunneling current is induced. This is because the tunneling junction between P^+ source and channel is formed by the band bending cause by gate coupling. This device can reduce power dissipation because its subthreshold swing can be smaller than 60mV/dec. at room temperature. Therefore, we can operate the TFET device with very low supply voltage due to smaller SS. In the following section, we will investigate the impact of WFV on TFET devices.

3.3.2 Results and Discussion

To simulate TFET, we use the nonlocal tunneling model [32], [40] to consider the band-to-band tunneling mechanism, and we extract the relevant parameters for nonlocal tunneling model based on the experimental data from [38]. Fig. 3.10 shows the I_d-V_g calibration result.

To compare the impact of WFV between TFET and FinFET devices, Fig. 3.11 shows the schematics of FinFET and double gate (DG) TFET devices designed with the same total gate area (W_{total} = 25nm). In addition, Fig. 3.12 shows that we design the FinFET and DG TFET devices with comparable I_{off}. To achieve comparable I_{off} for these two device structures pertinent device parameters are listed in Table 3.2.

In Fig. 3.13, we compare the WFV-induced I_{off} variations in DG TFET devices between the square method and Voronoi method. We can see that there is still difference between our Voronoi simulation result and the square-method simulation result for TFET devices. Compared with our Voronoi simulation method, the square method will overestimate the impact of WFV, and the error increases with grain size. From now on, we will investigate WFV in double-gate (DG) TFET devices with Voronoi method.

Fig. 3.14 compares the I_d-V_g dispersion curves of the FinFET device and DG TFET device under WFV. As can be seen, the DG TFET device shows significant SS fluctuation, while the FinFET device exhibits better immunity to WFV-induced SS fluctuation. In other words, although the DG TFET exhibits better nominal SS, it shows poor SS dispersion in the presence of WFV.

In Fig. 3.15, we compare the WFV-induced current variation for the DG TFET and FinFET devices with various grain sizes. We can see that the WFV-induced normalized drain current variation shows significant V_g dependency in DG TFET

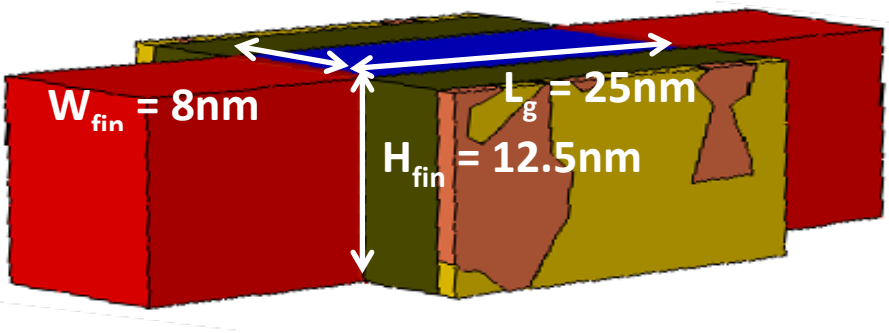
devices under V_{ds} = 0.5V. The current variation of the DG TFET device will be higher than the FinFET counterpart when V_g is below ~0.2V. However, the current variation of the DG TFET device will be lower than the FinFET counterpart as V_g is larger than ~0.3V.

Fig.3.16 shows the schematics of DG TFET and UTB SOI TFET devices, and we compare the immunity of WFV between DG TFET and UTB SOI TFET under the same total gate area (W_{total} = 25nm) and I_{off}. Fig. 3.17 shows that the DG TFET with double-gate structure exhibit better immunity to WFV than the UTB TFET counterpart, and the explanation is similar to the one given in section 3.2.1.

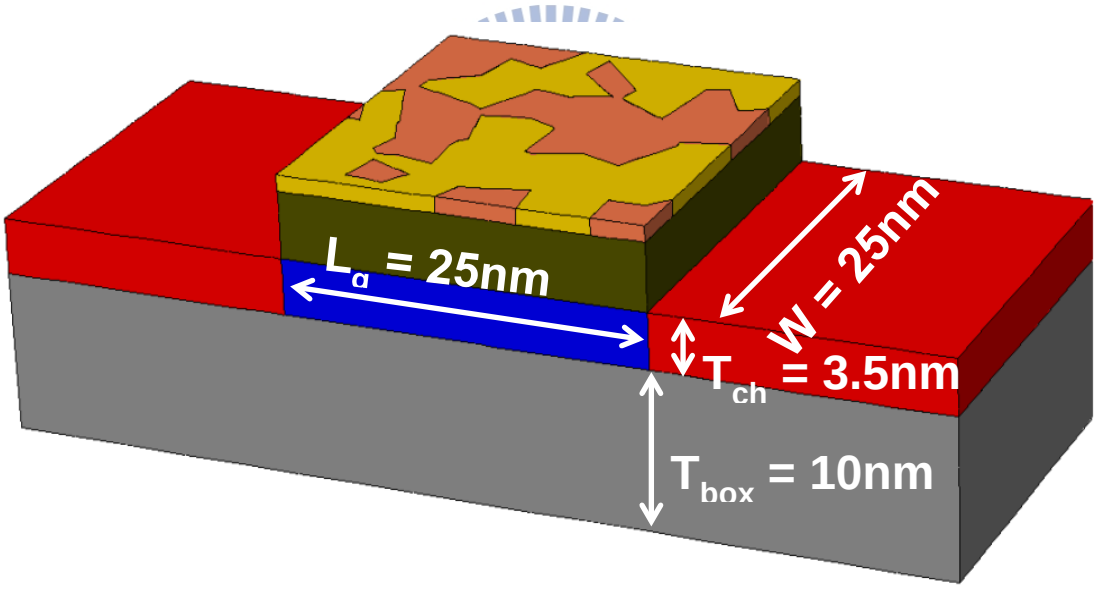
3.4 Summary

Based our Voronoi simulation method, we have investigated and compared the impact of WFV between FinFET and UTB SOI devices. Our study indicates that for a given electrostatic integrity and total effective gate area, the FinFET device exhibits better immunity to WFV than the UTB SOI counterpart. We further show that, unlike other sources of random variation, the WFV cannot be suppressed with EOT scaling.

In addition, we have also compared the impact of WFV between FinFET and DG TFET devices under comparable I_{off} and effective width. We found that, unlike the FinFET device, the DG TFET exhibits significant SS variation. Moreover, the normalized drain-current variation in DG TFET shows significant V_g dependency. Finally, the impact of WFV on TFETs also depends on the number of gate, and the DG TFET with double-gate structure shows better immunity to WFV than the UTB TFET counterpart. Our study may provide insights for nanoscale device design.



(a) FinFET



(b)UTB

Fig.3.1 Schematics of (a) FinFET, and (b) UTB SOI devices with identical effective width. L_g is the channel length, H_{fin} is the fin height, W_{fin} is the fin width, W is the channel width, and T_{ch} is the channel thickness.

Table 3.1 Device Parameters of FinFET and UTB SOI.

FinFET		UTB	
L_g [nm]	25	L_g [nm]	25
H_{fin}[nm]	12.5	W [nm]	25
W_{fin}[nm]	8	T_{ch} [nm]	3.5
EOT [nm]	0.65	EOT [nm]	0.65
N_{ch} [cm^{-3}]	10^{17}	N_{ch} [cm^{-3}]	10^{17}

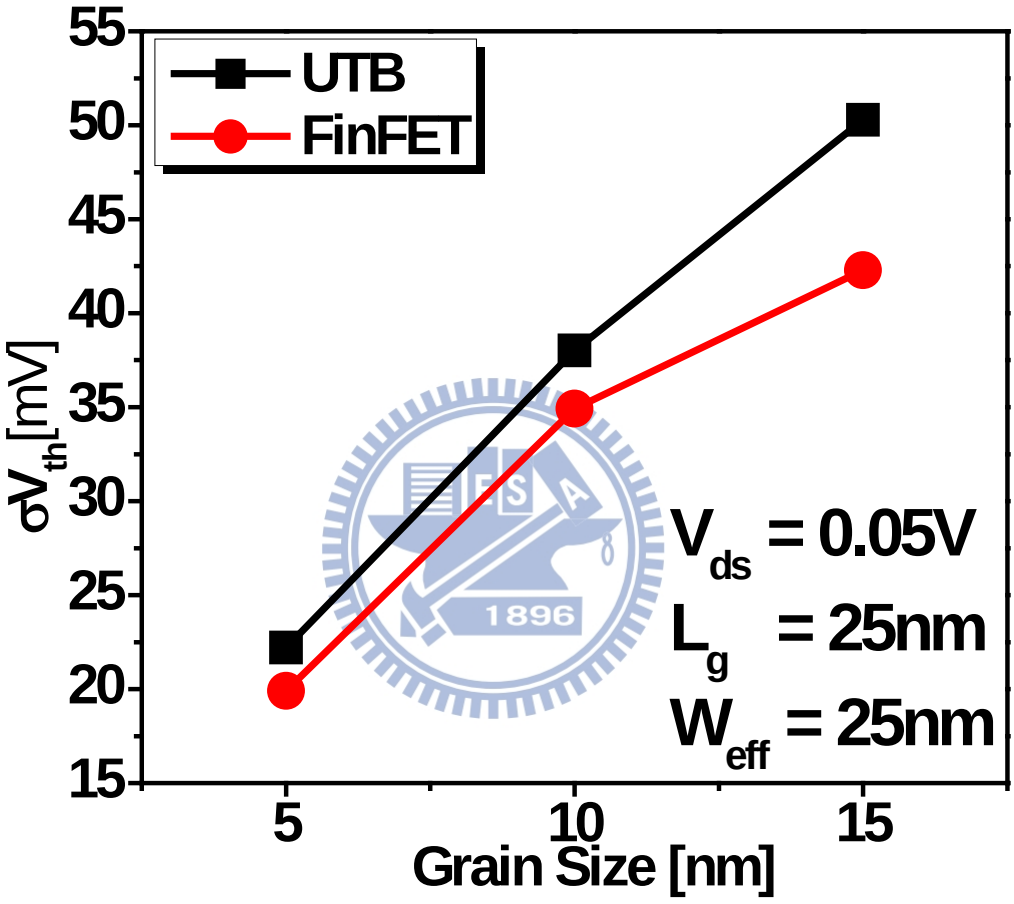


Fig.3.2 Comparison of V_{th} variations for FinFET and UTB SOI devices with various grain sizes.

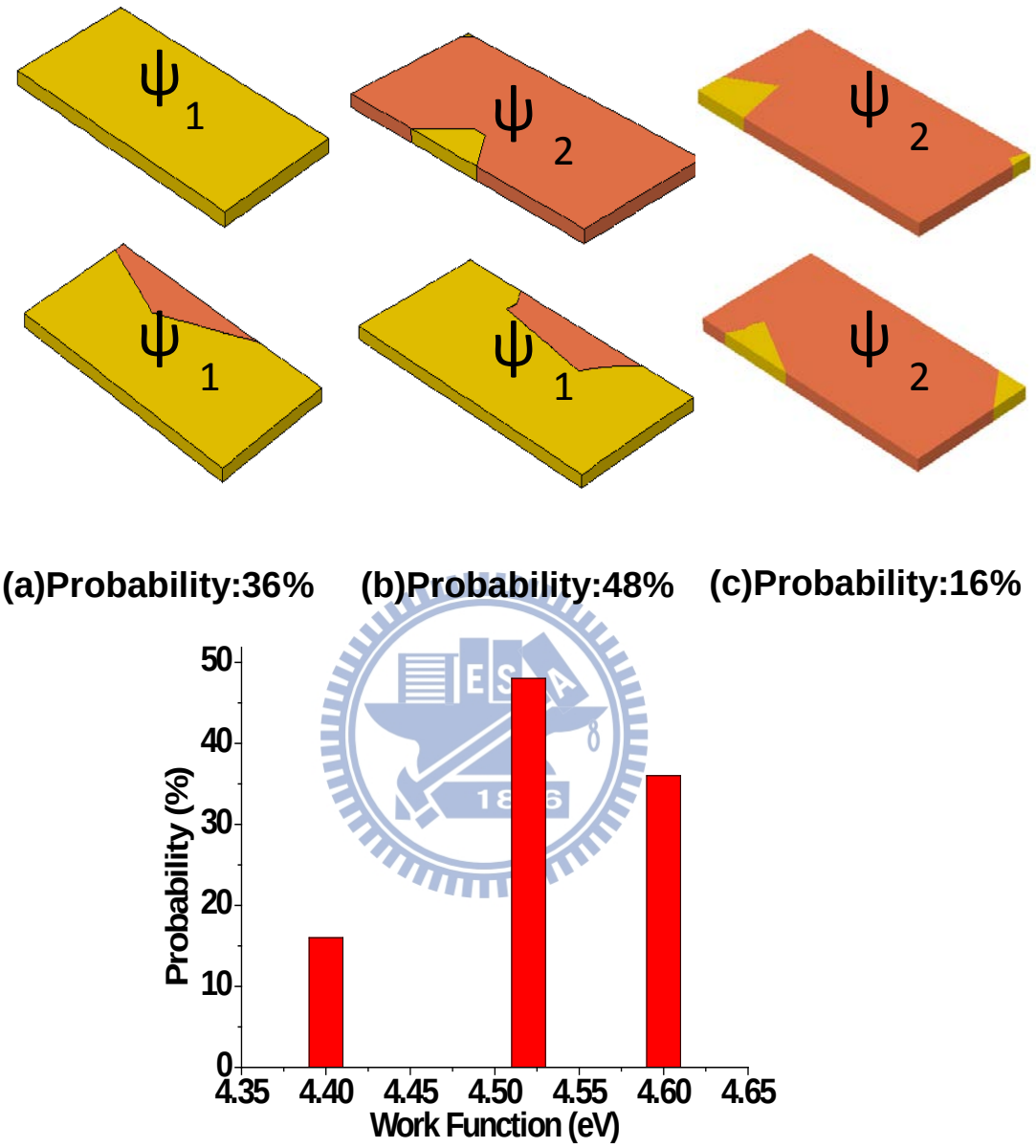


Fig.3.3 Extreme case of metal-gate patterns for FinFET: (a) both front-gate and back-gate WF = ψ1, (b) front-gate WF = ψ1 and back-gate side WF = ψ2, (c) both front-gate and back-gate WF = ψ2. Grain size = 25nm for each case.

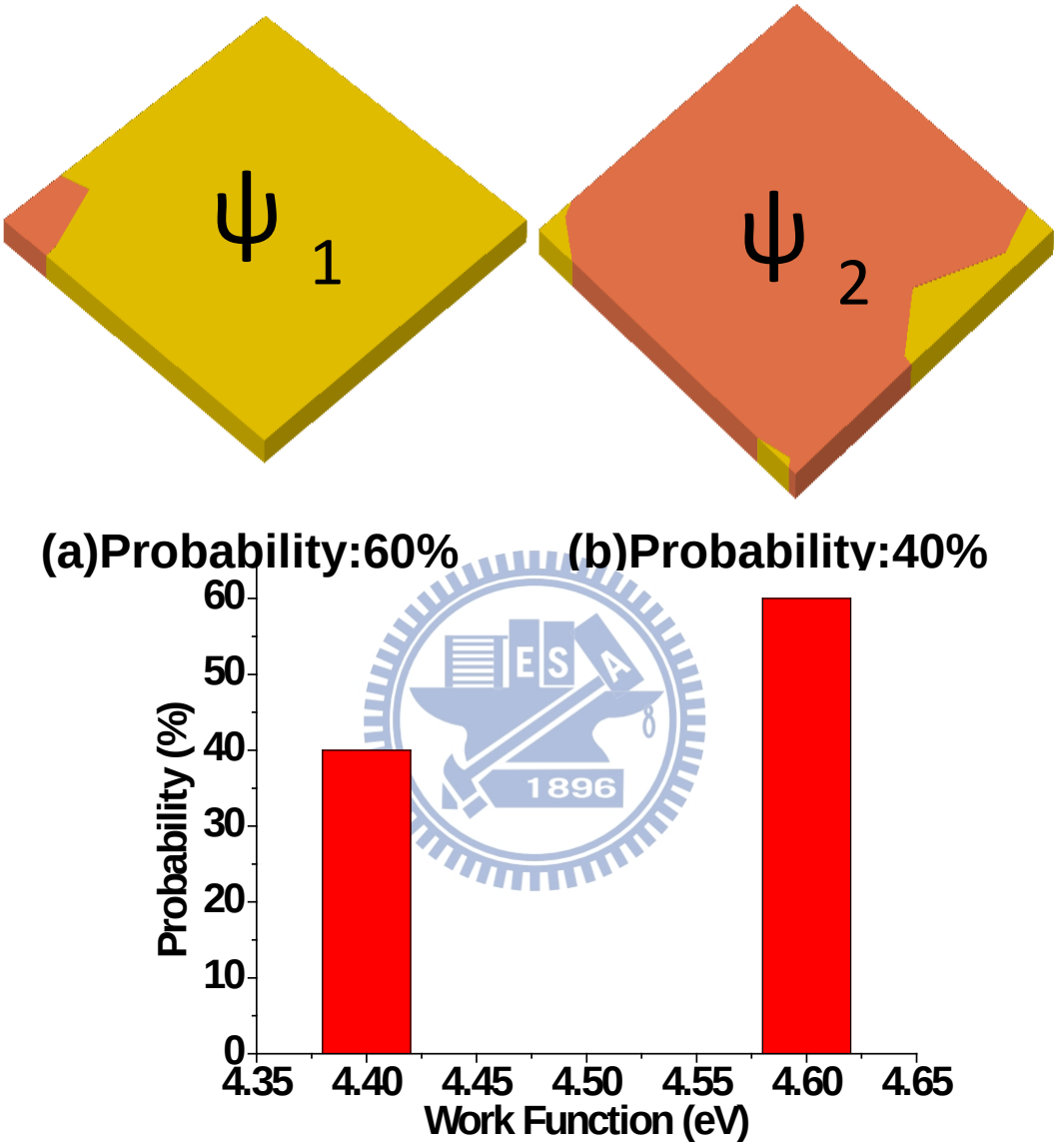


Fig.3.4 Extreme case of metal gate patterns for UTB:(a) WF = ψ1, (b) WF= ψ2. Grain size = 25nm for each case.

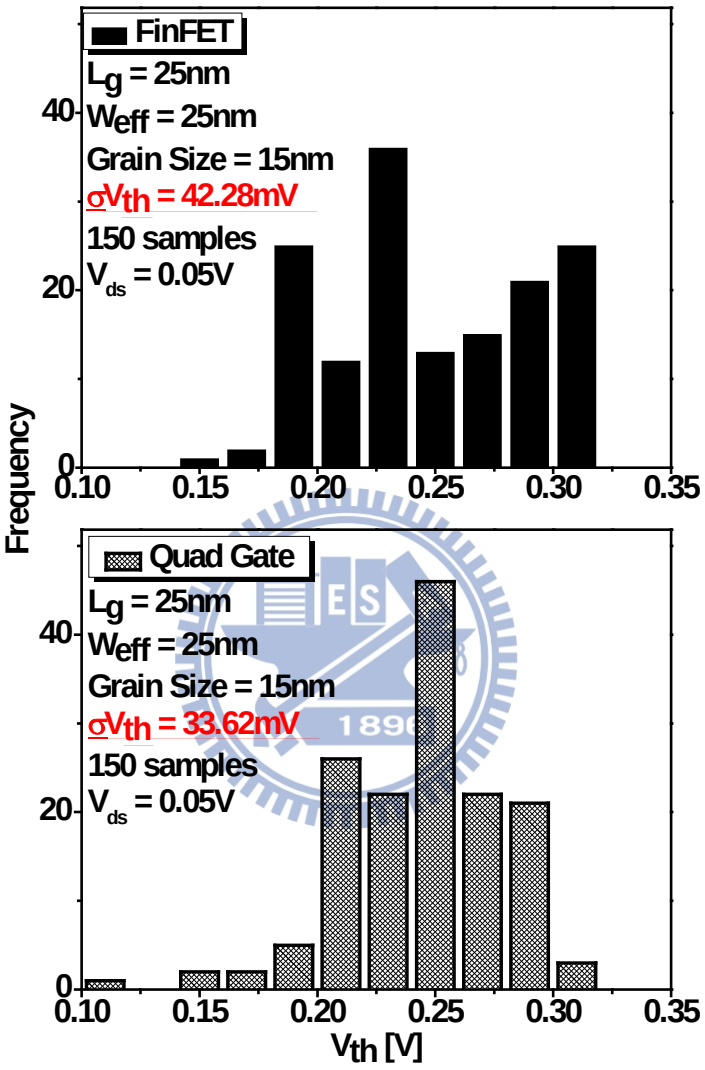


Fig.3.5 Comparison of V_{th} dispersion for FinFET and Quad-gate devices at grain sizes = 15nm. More Gaussian-like V_{th} distribution for Quad-gate can be seen.

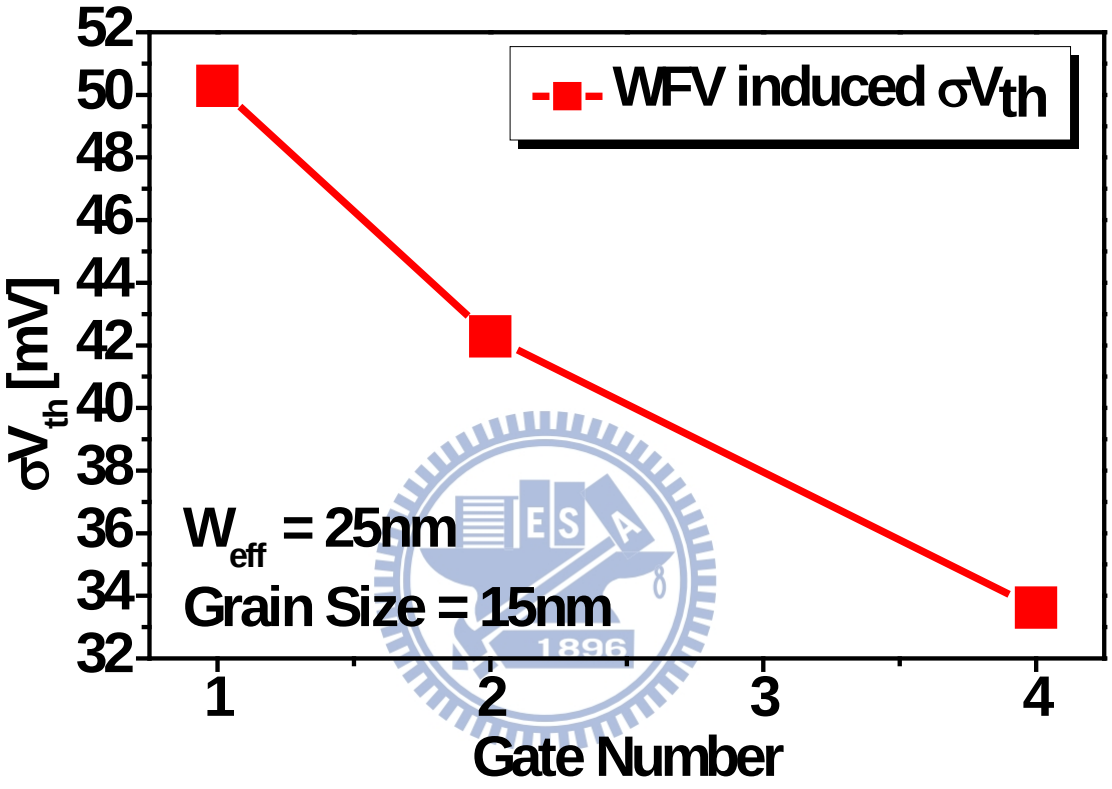


Fig.3.6 Comparison of V_{th} variations for Quad-gate, double-gate FinFET, and single-gate UTB SOI devices.

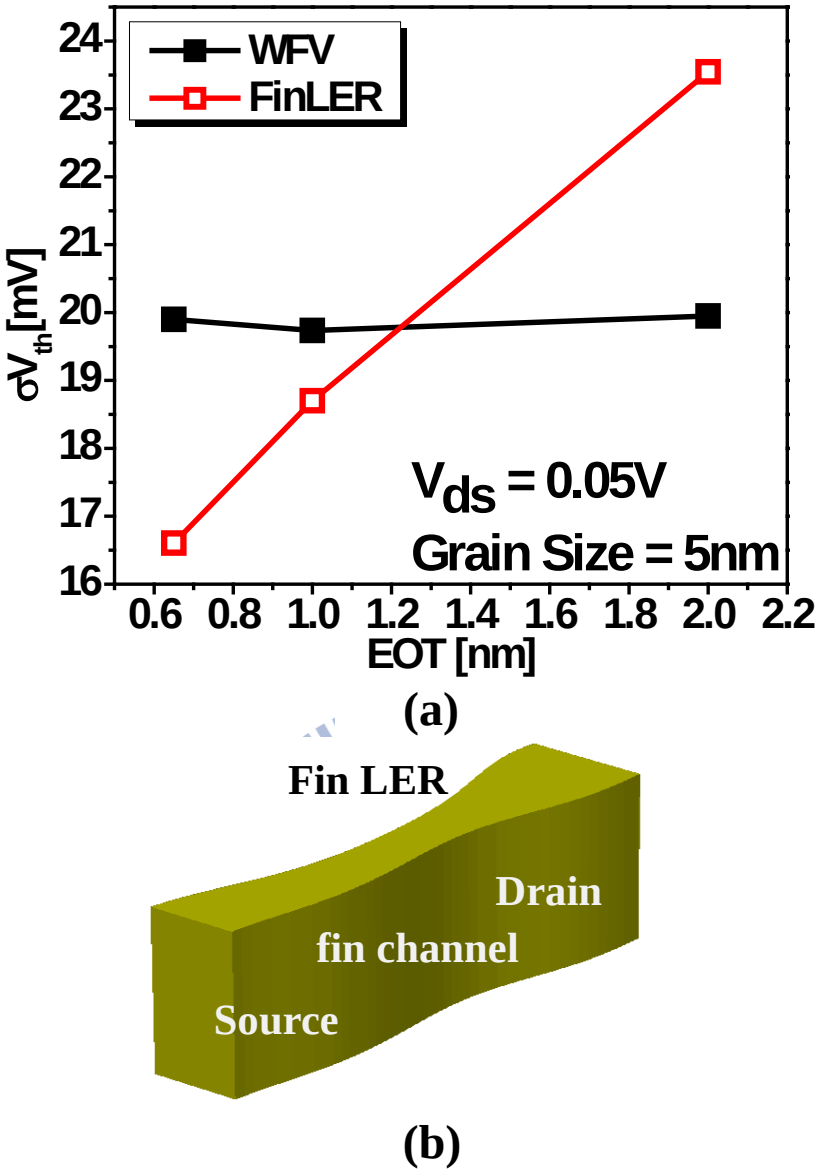


Fig.3.7 (a) Comparison of WFV and Fin-LER induced V_{th} variations for the FinFET device with L_g = 25nm and W_{eff} = 25nm. (b) Schematic illustrating the phenomenon of fin line edge roughness.

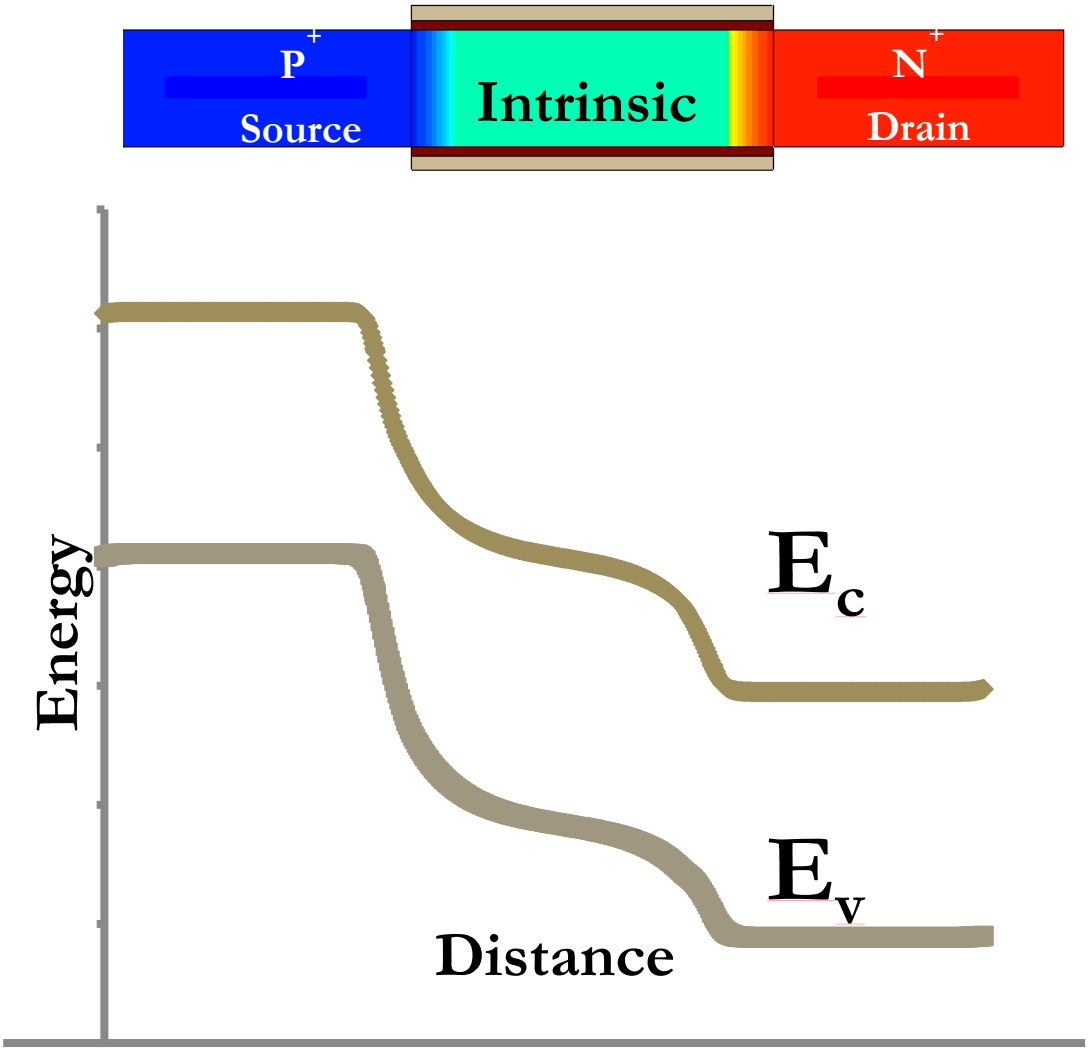


Fig.3.8 Schematic band diagram of a double-gate p-i-n TFET at off-state (V_d = 0.5V, V_g = 0V).

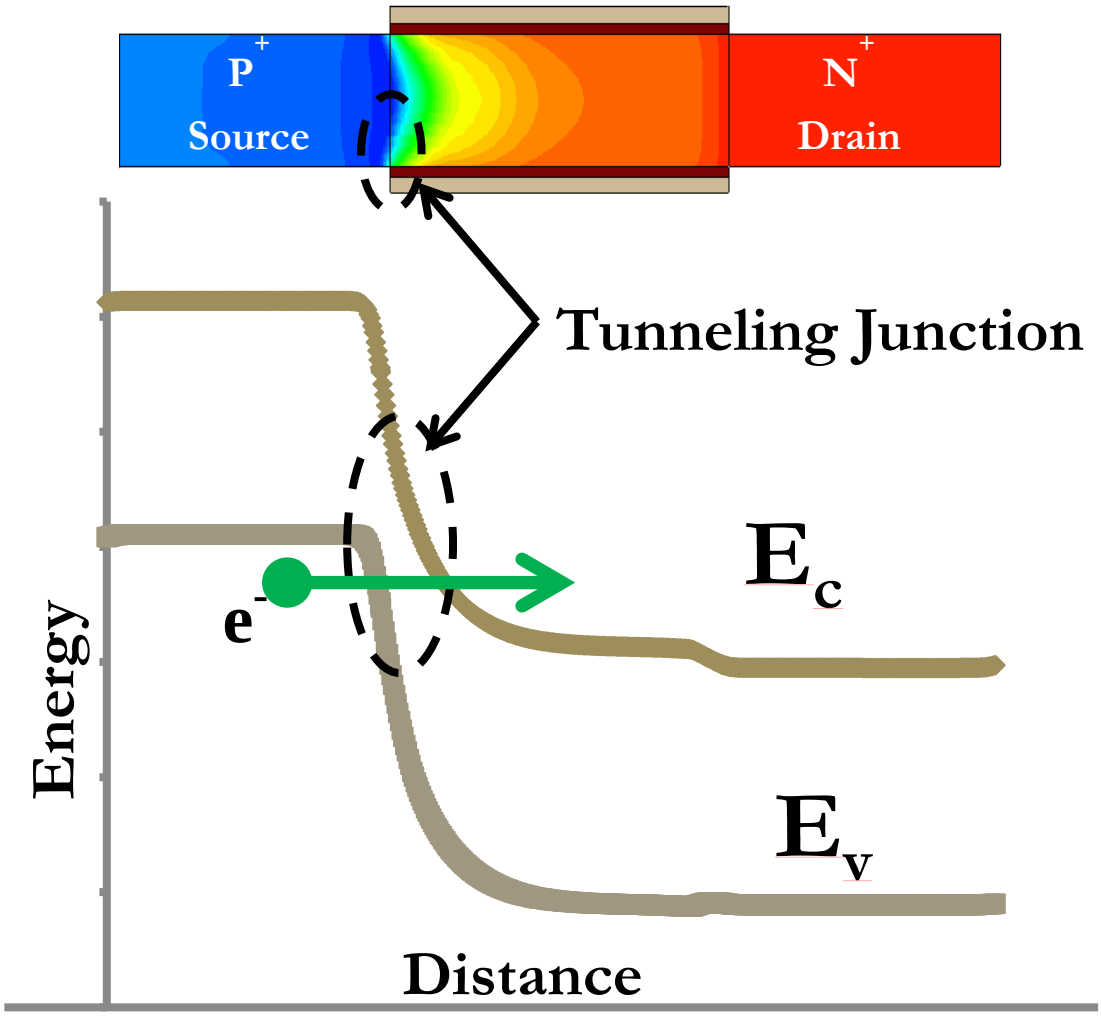


Fig.3.9 Schematic band diagram of a double-gate p-i-n TFET at on-state (V_d = 0.5V, V_g = 0.5V). The tunneling junction is indicated by ellipse.

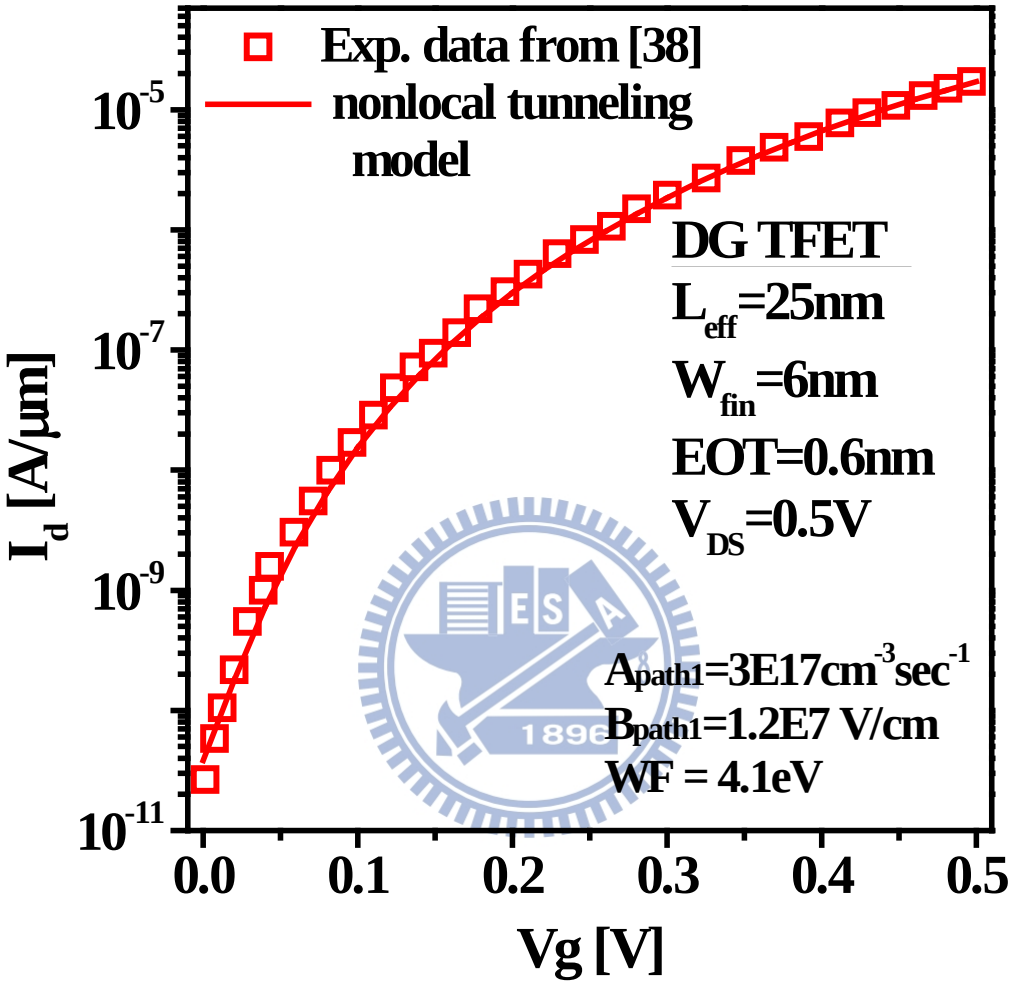


Fig.3.10 Calibration of TFET nonlocal tunneling model [32], [40] with published experimental data [38].

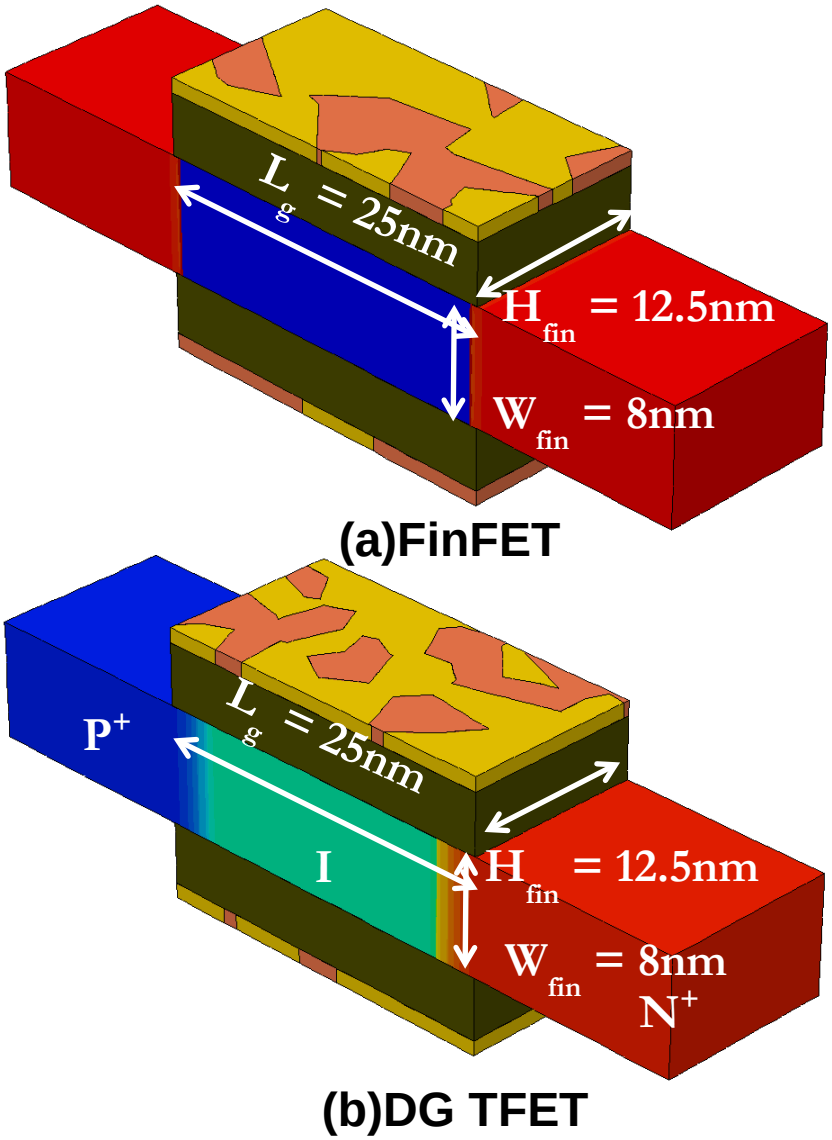


Fig.3.11 Schematic sketches of (a) the FinFET structure, and (b) the DG TFET structure with WFV in this study.

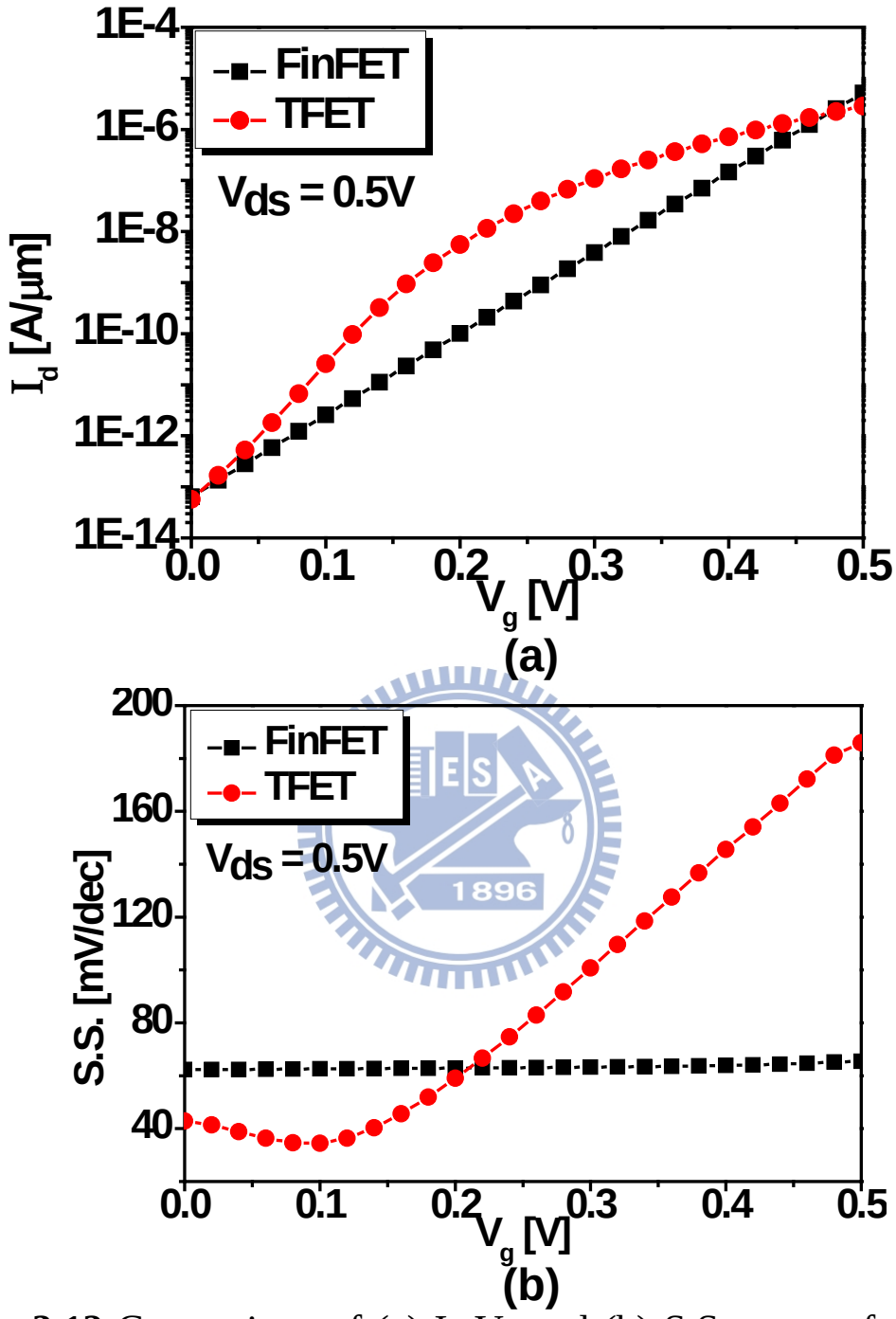


Fig.3.12 Comparison of (a) I_d-V_g and (b) S.S. curves for the FinFET device and DG TFET devices with L_g = 25nm, and W_{eff} = 25nm under comparable I_{off}.

Table 3.2 Device Parameters of FinFET and DG TFET.

	TFET	FinFET
N_{ch} [cm^{-3}]	10^{15} [39]	10^{17}
N_{source} [cm^{-3}]	$3*10^{20}$ [39]	$2*10^{20}$
N_{drain} [cm^{-3}]	10^{20} [39]	$2*10^{20}$
Doping Decay[nm/dec]	1	--
Apath [$cm^{-3}s^{-1}$]	$3*10^{17}$ [38]	--
Bpath [V/cm]	$1.2*10^{17}$ [38]	--
Phonon Energy [meV]	37 [32]	--
WF1(60%) [eV]	4.84	4.28
WF2(40%) [eV]	4.64	4.08

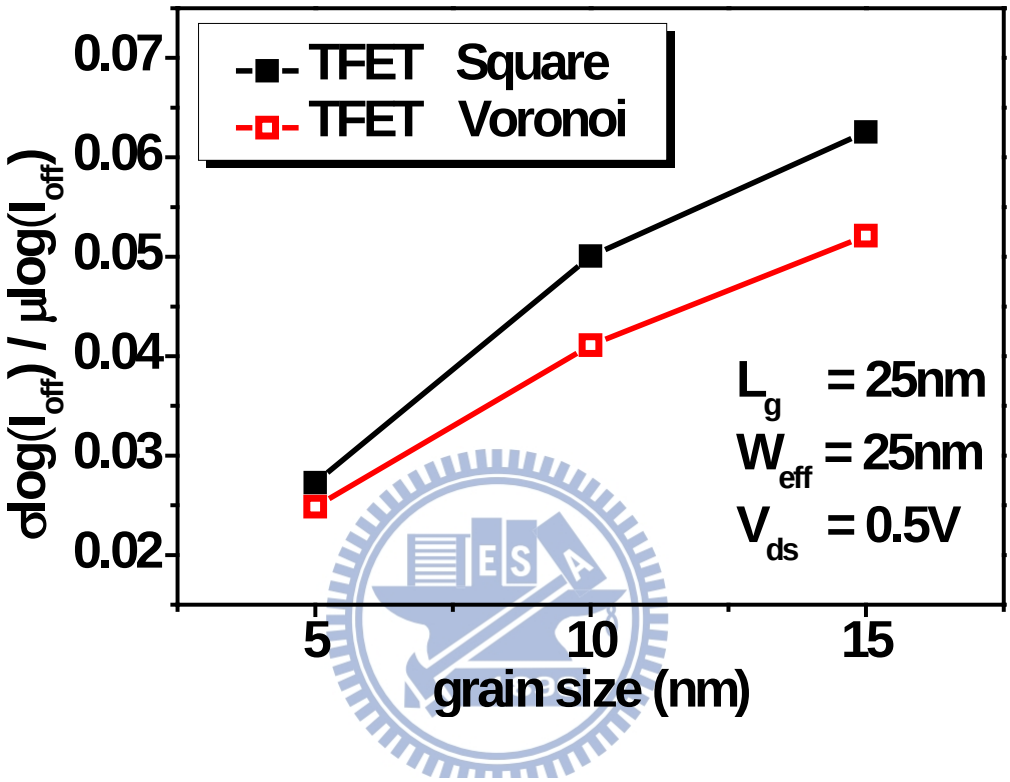


Fig.3.13 Comparison of WFV-induced I_{off} variations in DG TFET devices between the square method and Voronoi method.

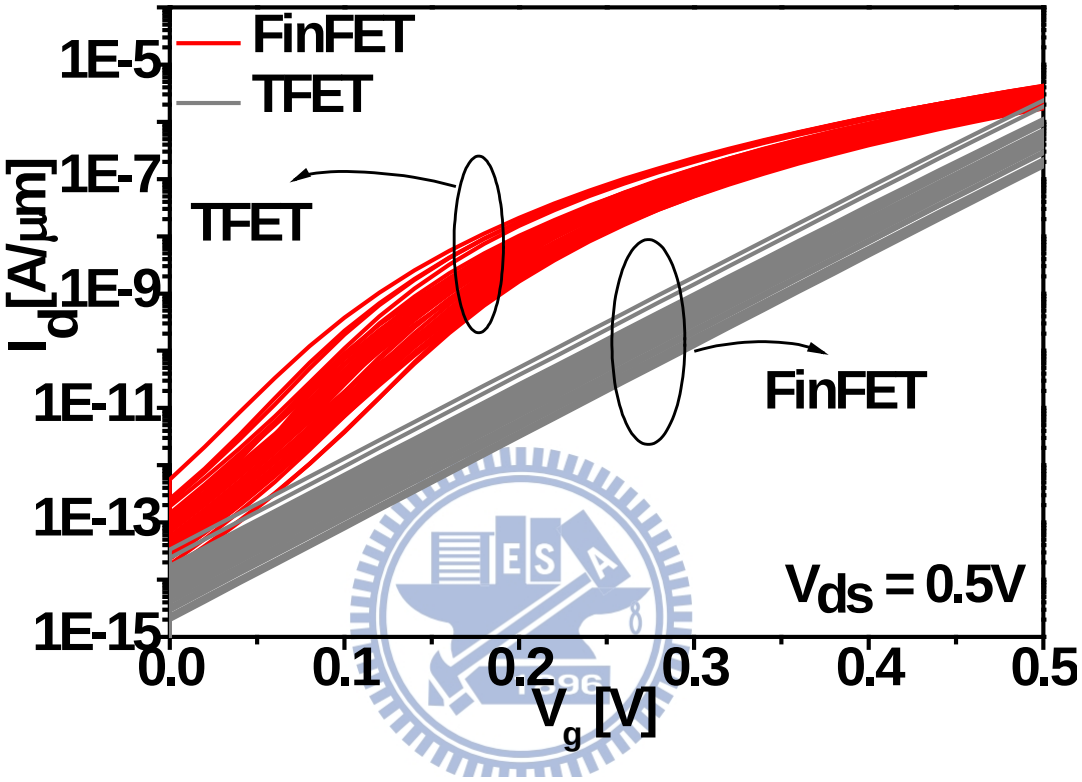


Fig.3.14 Comparison of I_d-V_g dispersion curves for the FinFET and DG TFET devices. Unlike FinFET, DG TFET shows significant S.S. fluctuation.

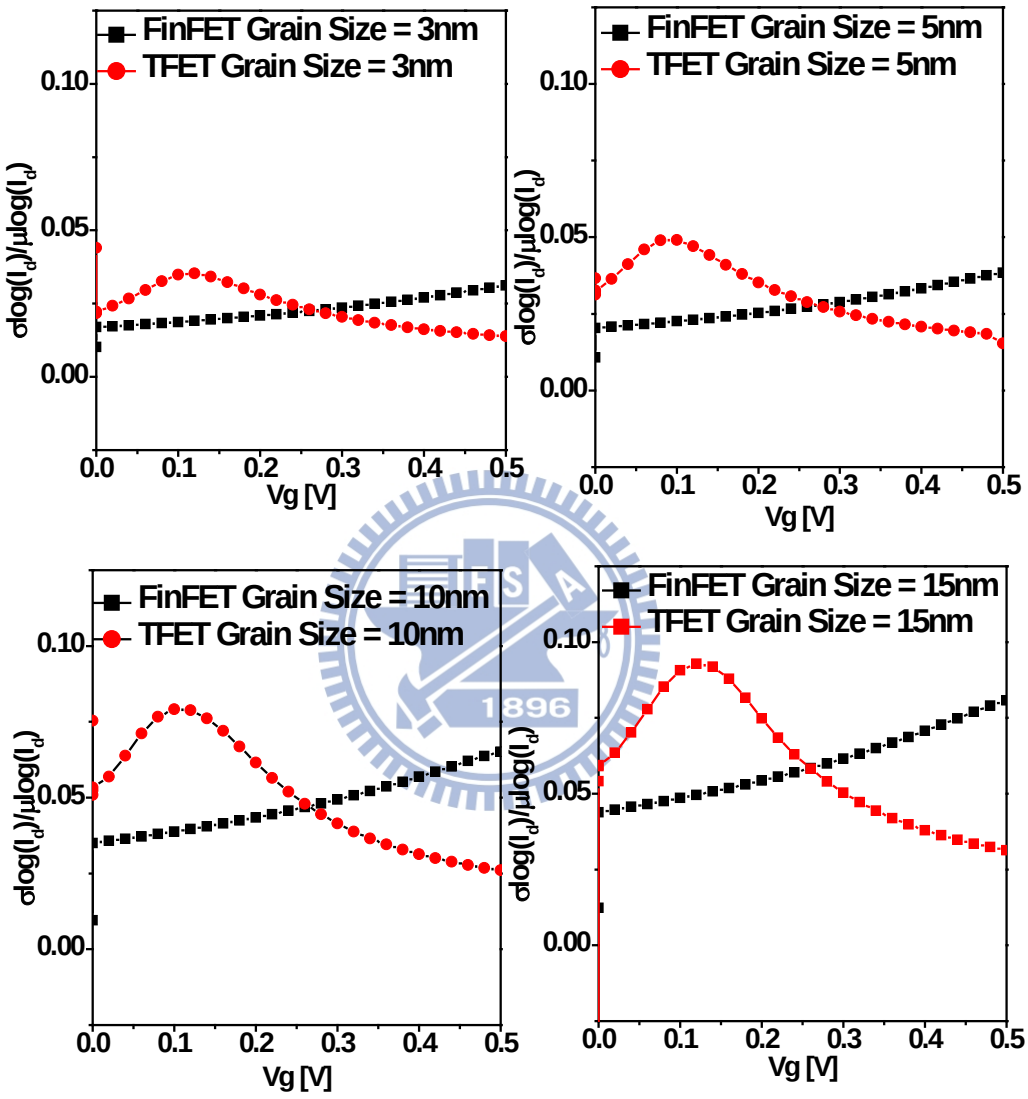
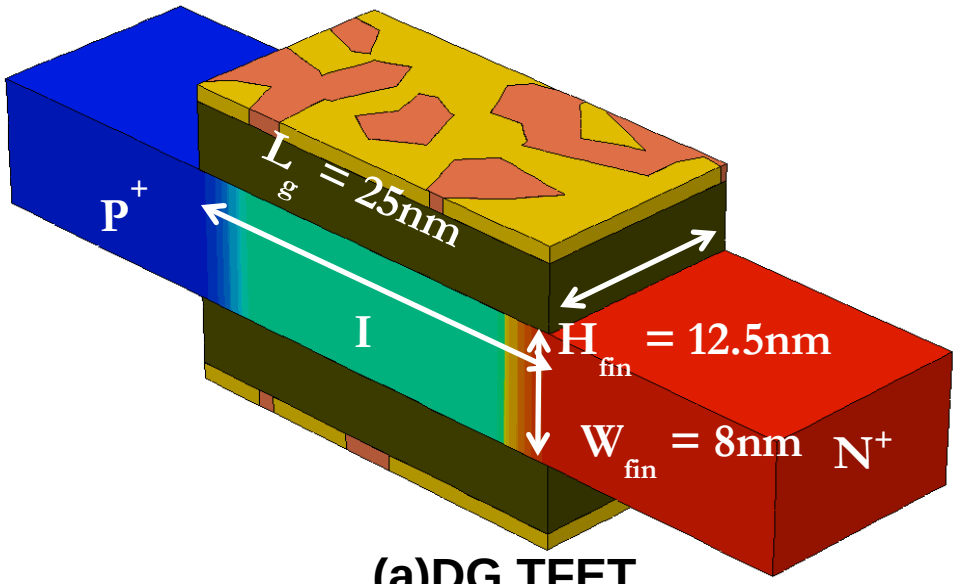
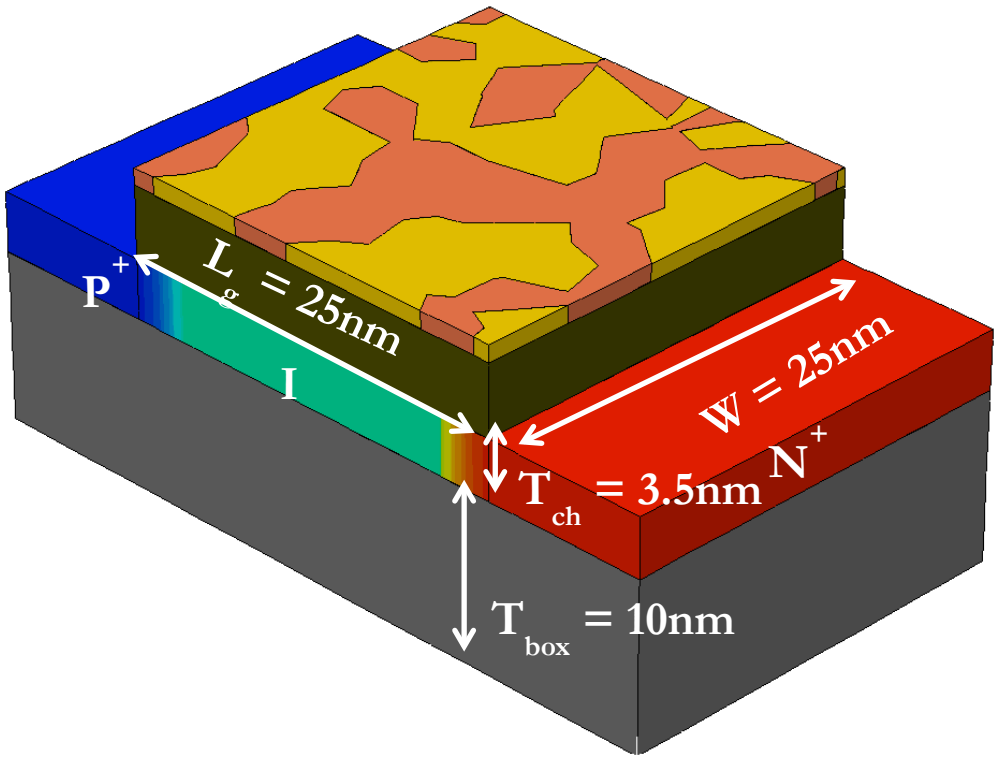


Fig.3.15 Comparison of the WFV-induced current variations for the DG TFET and FinFET devices with various grain sizes. It can be seen that DG TFET shows larger V_g dependence (V_{ds} = 0.5V).



(a)DG TFET



(b)UTB SOI TFET

Fig.3.16 Schematics of **(a)** DG TFET structure, and (b) UTB SOI TFET structure with WFV in this study.

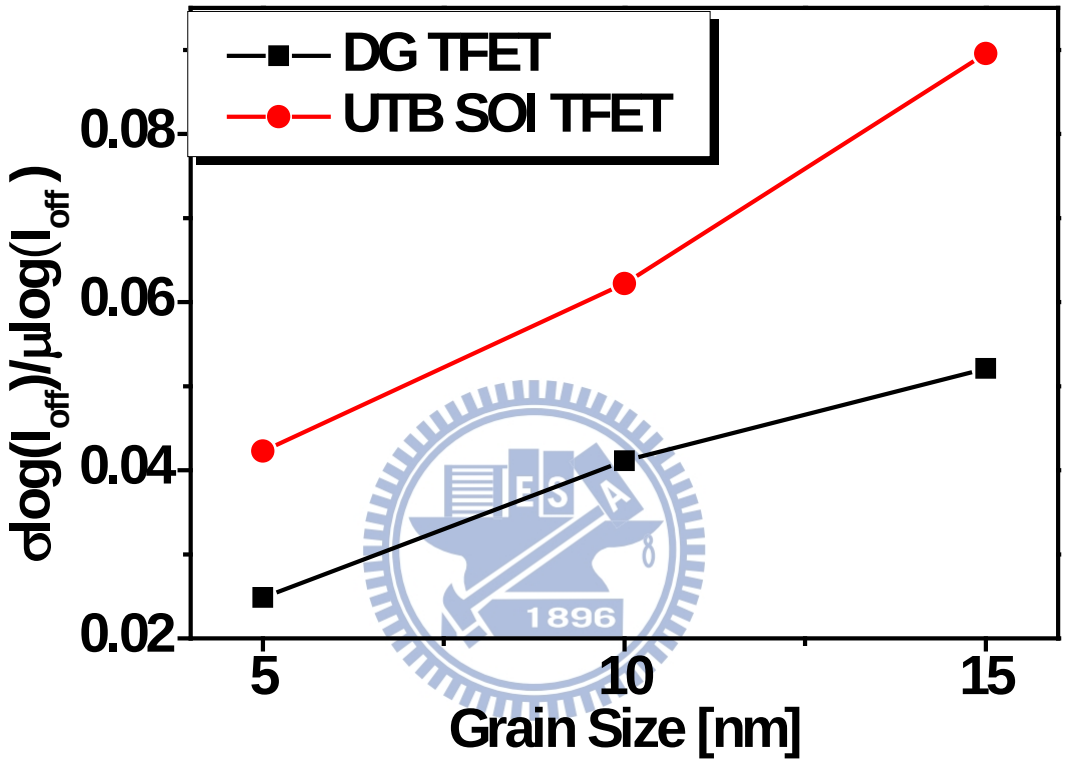


Fig.3.17 Comparison of WFV induced I_{off} variation for the DG TFET and UTB SOI TFET devices. DG TFET exhibits better immunity to WFV than the UTB SOI TFET counterpart.

Chapter 4

Conclusion

In this thesis, we have investigated and compared the impact of WFV on FinFET and UTB SOI devices using a novel Voronoi method [31] that can physically consider the interaction between neighboring grains. Compared with other simulation methods, our simulation method can maintain efficiency and accuracy simultaneously. The Voronoi method is capable of considering the impacts of metal-grain position, shape, size, and orientation. Based on our Voronoi method, we have investigated the characteristics of WFV in FinFET devices. From the obtained V_{th} dispersion, we can see that our simulation method can faithfully reflect the characteristic variation of metal grains.

Our study indicates that for a given electrostatic integrity and total effective gate area, the FinFET device exhibits better immunity to WFV than the UTB SOI counterpart. We have further showed that, unlike other sources of random variation, the WFV cannot be suppressed with EOT scaling. In addition, we have also compared the impact of WFV between FinFET and DG TFET devices under comparable Ioff and effective width. We found that, unlike the FinFET device, the DG TFET exhibits significant SS variation. Moreover, the normalized drain-current variation in DG TFET shows significant Vg dependency. Besides, the impact of WFV on TFETs also depends on the number of gates, and the DG TFET with double-gate structure shows better immunity to WFV than the UTB TFET counterpart.

Based on our Voronoi simulation method, the impact of WFV on FinFET and

UTB SOI SRAMs can be assessed [19], [20]. Besides, the Voronoi approach can be employed in describing the crystal grain of poly-silicon, and the impact of grain-boundary induced threshold-voltage variation in NAND Flash can also be evaluated [41].

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碩士論文題目：

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Investigation and Comparison of Work Function Variation for FinFET and UTB SOI Devices using Voronoi Approach