國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

在鍺通道金氧半場效電晶體上使用後沉積氧化製造二氧化鉿/三氧化二鋁/氧化鍺/鍺之閘極介電層堆疊結構的研究

Investigation of $HfO_2/Al_2O_3/GeO_x$/Ge Gate Stacks Fabricated by Post Deposition Oxidation on Ge-Channel MOSFETs

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碩 士 論 文

A Thesis

Submitted to Department of Electronics Engineering and Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

In Partial Fulfillment of the Requirements

For the Degree of Master

In Electronics Engineering

October 2012

Hsinchu, Taiwan, Republic of China

中 華 民 國 一 〇 一 年 十 月

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摘要

在這篇論文之中，首先我們研究了在原子層沉積三氧化二鋁介電層之後使用後沉積氧化方式，藉由快速升溫退火爐通氧氣退火在鍺介面上形成薄的 GeO_x 介電層之鍺 P 型金氧半電容。我們藉由後沉積氧化方式將等效氧化層厚度降至 1.41 奈米，並且使用及探討了電導法(conductance method)來萃取介面缺陷電荷密度。使用後沉積氧化方式之試片與一般直接熱成長二氧化鍺之試片比較起來有較小的介面缺陷電荷密度，而我們也研究了 GeO_x /Ge 之介面缺陷電荷密度與 GeO_x 厚度的關係。我們認為之所以用較高溫度的後沉積氧化方式會有較厚的 GeO_x 介電層以及較小的介面缺陷電荷密度是因為在較高溫度下會有較大的鍺三價波峰存在。介面缺陷電荷密度再經由 300 度 30 分鐘氫氣氮氣混合之熱退火可被降低，介面缺陷電荷密度的質在熱退火後下降了 16% ~ 44%。而在熱退火後我們也發現了平帶電壓往正的方向移動以及較小的電壓遲滯現象。我們最後決定選用二氧化

鉿/三氧化二鋁之閘極介電層以及使用後沉積氧化方式 520 度 3 分鐘這組條件來繼續進行元件的製造。

其次，我們研究了氫氣氮氣混合之熱退火對鍺的接面以及元件特性之影響，包含了 P 型金氧半場效電晶體以及 N 型金氧半場效電晶體。在熱退火之後，我們的 p^+n 接面以及 P 型金氧半場效電晶體的電流開關比分別是 4 orders 與 1.4×10^3，以及較佳的次臨界擺幅(165mV/dec)；而在 n^+p 接面以及 N 型金氧半場效電晶體方面，電流開關比分別是 3.5 orders 與 2.3×10^3，次臨界擺幅則是 151mV/dec。對 P 型以及 N 型兩者金氧半場效電晶體而言，在氫氣氮氣混合之熱退火後，源極汲極串聯阻抗上升，電洞載子遷移率提高，電洞載子遷移率波峰達到 375 cm^2/Vs。綜合比較 300 度 30 分鐘氫氣氮氣混合之熱退火對 P 型以及 N 型兩者金氧半場效電晶體的優缺點，在熱退火之後，平帶電壓會往正的方向移動，有較高的驅動電流，較佳的次臨界擺幅以及較高的電洞載子遷移率，然而源極汲極串聯阻抗卻會上升。

最後，我們研究了氫氣氮氣混合之熱退火對磊晶鍺在絕緣層上覆矽金氧半場效電晶體的影響，包含了磊晶 60 奈米鍺以及 30 奈米鍺在絕緣層上覆矽。對 P 型以及 N 型兩者金氧半場效電晶體而言，在熱退火之後，平帶電壓會往正的方向移動，較佳的次臨界擺幅，較高的驅動電流，較低的漏電流，較大的源極汲極串聯阻抗以及較高的電洞載子遷移率，電洞載子遷移率波峰達到 313 cm^2/Vs(磊晶 60 奈米鍺)以及 194 cm^2/Vs(磊晶 30 奈米鍺)。磊晶 30 奈米鍺在絕緣層上覆矽金氧半場效電晶體有較佳的次臨界擺幅，而磊晶 60 奈米鍺在絕緣層上覆矽金氧半場效電晶體則是有較大的驅動電流以及電洞載子遷移率。

Investigation of $HfO_2/Al_2O_3/GeO_x$/Ge Gate Stacks Fabricated by Post Deposition Oxidation on Ge-Channel MOSFETs

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ABSTRACT

In this thesis, firstly, germanium MOS capacitors using post deposition oxidation method to form a thin GeO_x interfacial layer by oxidizing Ge surface beneath an ALD Al_2O_3 layer using high-k RTO was fabricated and analyzed electrically. The EOT value was scaled down to 1.41 nm by PDO. Theory of the conductance method was discussed in detail, and utilizing it to extract the interface state density. The post oxidation deposition samples have less interface state density than thermal GeO_2 samples, and the D_{it} of GeO_x/Ge MOS interface controlled by the GeO_x thickness has been studied. We think the less interface state density is because of the thicker GeO_x interfacial layer and larger Ge^{3+} peak which the higher post deposition oxidation temperature grown. Interface state density was shown to be reduced through 300℃ 30 minutes forming gas annealing, the D_{it} value has been reduced 16% ~ 44%. The positive V_{FB} shift and lower C-V hysteresis is shown in the samples after FGA. The HfO_2/Al_2O_3 gate stack with PDO 520℃ 3min was selected to be the best condition to fabricate Ge MOSFETs.

Secondly, we investigated the effect of FGA on Ge junction and device characteristics, including both PMOSFET and NMOSFET. On/off ratio of our p^+n junction and PMOSFET reached 4 orders and 1.4×10^3 respectively, with better subthreshold swing (165mV/dec) obtained after FGA. And on/off ratio of our n^+p junction and NMOSFET reached 3.5 orders and 2.3×10^3 respectively, with better subthreshold swing (151mV/dec) obtained after FGA. For both PMOSFETs and NMOSFETs, the larger series resistance and higher hole mobility are observed after FGA, a peak hole mobility of 375 cm^2/Vs after FGA is obtained. Pros and cons of FGA at 300℃ 30 min on both PMOSFET and NMOSFET were summarized according to our experimental data. Positive V_{FB} shift, higher drive current, better subthreshold swing and higher hole mobility are obtained after FGA, while series resistance is increased after FGA.

Finally, we investigated the effect of FGA on epi-Ge on SOI MOSFETs characteristics, including epi-60nm Ge on SOI and epi-30nm Ge on SOI. For both PMOSFETs and NMOSFETs, the positive V_{th} shift, better subthreshold swing, higher on current, lower off current and higher R_{SD} are obtained after FGA. Also, the higher hole mobility is observed, a peak hole mobility of 313 cm^2/Vs for epi-60nm PMOSFET and 194 cm^2/Vs for epi-30nm NMOSFET after FGA are obtained. Epi-30nm Ge on SOI MOSFETs have better subthreshold swing, while epi-60nm Ge on SOI MOSFETs have larger on current and higher hole mobility.

誌謝

兩年多的研究所生涯，說長不長，說短不短，終於要告一段落了。這一篇論文能夠順利完成，首先要感謝我的指導老師－簡昭欣教授。老師不只在學業上給予我很大的幫助，在待人處事上也是教了我不少東西，老師總是不斷叮嚀我們在未來職場上應有的態度，生怕我們一時疏忽給了主管不好的印象。相信在老師的諄諄教誨下，我在未來職場上的路應該可以走得平順一些，也期許自己在公司裡能夠有好的表現，不辜負老師的期待。

政庭學長，感謝你在這兩年來的幫忙與指導，一直幫我解決實驗上遇到的問題，沒有你的幫忙，這些電容、元件是不可能做出來的，在這裡衷心的感謝你，也希望你接下來的實驗一切順利。哲偉學長，總是拿一些奇怪的東西問你，你也都不厭其煩的一一回答我，真的很謝謝你，畢業之後聽不到你打嘴砲了該怎麼辦啊。信淵學長，每次量測時都要麻煩你來解決各式各樣的怪問題，沒有你我的量測會變得很辛苦的，期待之後還有機會跟你一起打球。韋志學長，你一步一步的帶我做實驗，讓我從什麼都不會到現在可以獨立做出元件。宏碁學長，奈米中心的扛壩子，頂著你的光環讓我在實驗上沒遇到太多困難。家豪學長、宇彥學長、宗佑學長、昶智學長，感謝你們在大大小小事情上的幫忙。

小林、酷奇、就舉，並肩作戰的好友們，讓我在做實驗的時候不孤單，希望之後還能常常有機會一起吃飯。小龜、主元、邦聖、純敏，目前在正水深火熱的學弟妹們，希望你們到時候能準時畢業。

當然，最重要的是要感謝我的父母，沒有他們在背後默默的支持我，讓我無後顧之憂的專心在學業上衝刺，我想我不會有今天的成就，我一定會好好孝順你們的。

最後，凡是有幫助過我大大小小的人，我都由衷的感謝你們，也祝福所有的人都能心想事成。

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Chapter 1

Introduction

1.1 General Background

In 1947, the first transistors were fabricated in Bell Laboratories using bulk germanium as the semiconducting material by John Bardeen, Walter Brattain and William Shockley. Then, the integrated circuit which made of Germanium was invented by Jack Kilby in 1958. Germanium was the predominant material for solid-state devices through the 1950s and early 1960s. However, during the 1960s, the first metal oxide semiconductor field effect transistors (MOSFETs) fabricated by Dawon Kahng and Martin Atalla was made of silicon, and then germanium was largely replaced with silicon. There are many reasons why germanium was largely replaced with silicon, such as the larger bandgap of silicon resulting in lower leakage currents and the excellent quality and stability of thermal SiO_2 as a gate dielectric for silicon compared with the water soluble and thermal instable GeO_2 [1]. Therefore, Si-based MOSFETs have become the driving force for the semiconductor industry in the last four to five decades.

Recently, it has been increasingly difficult to further improve the performances of Si complementary metal–oxide–semiconductor (CMOS) devices through the conventional device scaling [2]. The physical dimensions have been continually reduced to double the number of transistors on a chip every eighteen months

according to Moore's Law [3]. The decrease in transistor dimensions has led to increase in microprocessor performance. With the reduction in device dimensions of MOSFETs, silicon dioxide films, which used as a gate dielectric, have been scaled down to keep the same control over the channel. Devices with thinner dielectric could improve the short channel effect. But beyond the 16nm node, CMOS technology using Si channel has encountered formidable challenges, as further scaling in the transistors may not provide device performance advantages [4]. In order to maintain Moore's Law, mobility enhancement has become a key technology. Ge has been considered as one promising candidate for replacing Si, because of not only its much higher intrinsic carrier mobility but also the compatibility with the conventional Si integration technologies.

1.2 Motivation

As shown in **Table 1.1**, the material properties of bulk Si, Ge, GaAs, and InAs at 300K are compared [5]. Germanium has better electron (3900 versus 1500 cm^2/Vs) and hole (1900 versus 450 cm^2/Vs) bulk mobility for Ge over Si. The lower bandgap (0.66eV versus 1.12eV) characteristic of Ge enables to lower the Schottky barrier height and contact resistance than Si. However, Ge has several practical problems. First, the lower bandgap of germanium resulting in higher leakage currents. Second, Ge oxides are water soluble and thermal instable, they are easy to rinsed of during the fabrication process. Third, it is difficult to achieve a high-quality oxide/Ge interface due to the bad surface properties of Ge.

Recently, the Ge PMOSFETs with high hole mobility values have been demonstrated with thermally grown GeO_2 gate stacks due to the high quality GeO_2/Ge

MOS interfaces [6]. However, the thick GeO_2 gate stacks may leads larger equivalent oxide thicknesses (EOTs). In order to scale down EOT, development of high-k/Germanium gate stack is necessary. High interface quality and small EOT is essential for Ge to be used as an alternative high mobility channel material for future technology nodes. Ge PMOSFETs have been realized with direct high-k/Ge gate stacks [7]. Because of the poor MOS interfaces, these Ge PMOSFETs show quite low mobility values. Therefore, it is necessary to develop high-k/Ge gate stacks with both thin EOT and low interface state density (D_{it}). Employing a thin GeO_2 interfacial layer (IL) is a promising solution [8].

1.3 Scope and Organization of the Thesis

The promising high-mobility substrate material, Ge, was investigated in this thesis. In this thesis, we focus on using post deposition oxidation method to form a thin GeO_x IL by oxidizing Ge surface beneath a thin atomic layer deposition (ALD) Al_2O_3 layer using high-k rapid thermal oxidation (RTO). The thesis is divided into five chapters and arranged as follows:

Chapter 1, a brief overview of background and motivation is described.

Chapter 2, Ge PMOS capacitors using post deposition oxidation method to form a thin GeO_x IL by oxidizing Ge surface beneath a ALD Al_2O_3 layer using high-k RTO was fabricated, the dependence of the GeO_x/Ge interface qualities on the post deposition oxidation conditions such as post deposition oxidation temperature and post deposition annealing ambient was investigated. Theory of the conductance method was discussed in detail, and utilizing it to extract the interface state density for

different sample. The effect of forming gas annealing (FGA) on PMOS capacitors was also investigated.

Chapter 3, both germanium NMOSFET and PMOSFET were fabricated using post deposition oxidation method to form a thin GeO_x IL by oxidizing Ge surface beneath a ALD Al_2O_3 layer using high-k RTO. Effect of FGA on both NMOSFET and PMOSFET junctions and device electrical characteristic was studied, including I_D-V_G, I_S-V_G, I_D-V_D, subthreshold swing and series resistance. The mobility extracted from split C-V of both NMOSFET and PMOSFET were investigated, with and without FGA.

Chapter 4, both germanium NMOSFET and PMOSFET were fabricated on epitaxial Ge on thin SOI substrates with two different structures, respectively. Effect of FGA on both NMOSFET and PMOSFET device electrical characteristic was studied, including I_D-V_G, I_S-V_G, I_D-V_D, subthreshold swing and series resistance. The mobility extracted from split C-V of both NMOSFET and PMOSFET were investigated, with and without FGA.

Chapter 5, we summarized all experimental results in this thesis, gave the conclusions and suggestions for future work.

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	Ge	Si	GaAs	InAs
Bandgap (eV)	0.66	1.12	1.42	0.35
Hole mobility (cm^2/V-S)	1900	450	400	460
Electron mobility (cm^2/V-S)	3900	1500	8500	33000
Conduction band DOS Nc (cm^{-3})	1.04E19	2.8E19	4.7E17	8.7E16
Valance band DOS Nv (cm^{-3})	6E18	1.04E19	7E18	6.6E18
Lattice constant (Å)	5.646	5.431	5.653	6.058
Dielectric constant	16	11.9	13.1	15.2
Melting point (°C)	937	1412	1240	942
Dopant activation limit (cm^{-3})	P : (4-6)E19	P : (1-2)E20	Si : (4-6)E18	Si : (1-3)E18

Table 0.1 Material properties of bulk Ge, Si, GaAs, and InAs at 300K are compared

Chapter 2

Ge PMOSCAP $HfO_2/Al_2O_3/GeO_x$/Ge Gate Stack Fabricated by Post deposition oxidation

2.1 Introduction

With the reduction in device dimension of silicon MOSFETs, gate dielectric had to scale down to keep the same control over the channel. In other words, the thickness of SiO_2 must continue to scale down with channel length. However, when the thickness of SiO_2 decrease to less than 1.6 nm, gate leakage current becomes significantly high due to direct tunneling. It appears that the continued scaling of silicon MOSFETs faced a physical obstacle. Replacing SiO_2 with physically thicker layer of new oxide with higher k had become essential to Si.

Recently, the successful of high-k dielectric on Si had helped the development of Ge MOSFET, because the gate dielectrics are no longer restricted to the thermal oxide. Development of high-k/Ge gate stack with high interface quality and small EOT is important for Ge to be used as a high mobility channel material. High-k gate dielectrics like Al_2O_3 [1] and HfO_2 [2] have been studied on Ge, showing promising results in terms of low EOT. Al_2O_3 has wide bandgap energy, large conduction and valance band offset, and high thermodynamic stability. Also, Al_2O_3 has higher dielectric constant value, it about 2.5 times than SiO_2. HfO_2 also has large bandgap

energy and band offset, and its dielectric constant value is even higher than Al_2O_3. However, there is a problem in formation of the gate dielectric on germanium substrate. Germanium oxide is thermally unstable and water soluble, eliminating the formation of GeO_x at the interface between high-k dielectric and Ge substrate is important to form high quality gate stack on Ge. While direct high-k/Ge gate stacks have poor interface quality, interface passivation become a key challenge to improve the interface of high-k/Ge gate stacks. Recently, Ge MOSFETs using thick thermally grown GeO_2/Ge gate stacks (EOT>20 nm) with low D_{it} have been reported to provide high hole and electron mobility [3]. To have gate stacks satisfying both thin EOT and low D_{it} is necessary, employing a thin GeO_2 interfacial layer is a promising solution [4]. However, because of the damages introduced by the high-k deposition, depositing high-k films directly on an ultrathin GeO_2/Ge MOS structure significantly degrades the MOS interface and generates large amounts of D_{it} [5]. It is very difficult to have thin EOT and low D_{it} simultaneously.

Using high-k RTO post deposition oxidation method to form a thin GeO_x IL by oxidizing Ge surface beneath a thin ALD Al_2O_3 layer is a promising solution. Al_2O_3 layer could be a protecting layer to prevent the damage introduced by the high-k deposition to the GeO_x IL, and it also could be an oxygen barrier that suppresses the growth of unnecessarily thick GeO_x IL [6]. It has been found that D_{it} at the GeO_x/Ge interface increases with a decrease in the thickness of the GeO_x IL.

In this chapter, the Ge PMOSCAPs are fabricated on Ge substrate with $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks by post deposition oxidation. The reason why we didn't use HfO_2/GeO_x/Ge gate stack is the intermixing between HfO_2 and GeO_x films, which may increase D_{it} [7], almost no intermixing between Al_2O_3 and GeO_x films. Therefore, Al_2O_3 layer prevent not only the damage introduced by the high-k deposition but also the intermixing between HfO_2 and GeO_x films. The dependence of

the GeO_x/Ge interface qualities on the post deposition oxidation conditions such as post deposition oxidation temperature and post deposition annealing ambient was investigated. Theory of the conductance method was discussed in detail, and utilizing it to extract the interface state density for different sample. The effect of forming gas annealing (FGA) on PMOS capacitors was also investigated.

2.2 Fabrication of ALD- $HfO_2/Al_2O_3/GeO_x$/Ge MOSCAP

(100)-oriented p-Ge substrates with resistivity ca. 0.01Ω·cm ~ 0.05Ω·cm were used for MOSCAP fabrication. Before gate dielectric formation, all of the samples were pre-cleaned by diluted HF (20:1) and DI water rinsing to remove the native oxide, followed by 10 cycles ALD-Al_2O_3 thin film grown on each sample at 250℃, a thin GeO_x layer being formed by RTO post deposition oxidation to passivate the Ge surface, with oxidation condition 520℃ 3min and 550℃ 3min. A 50 cycles HfO_2 layer was deposited by ALD at 250℃. Post deposition annealing at 500℃ 60sec with O_2 and N_2, respectively. Then,1000 Å Ti/Pt was deposited by sputter and the capacitors front electrodes were patterned through shadow mask, while a thermal coater 4000 Å Al layer was deposited as the backside contact.

Forming gas annealing (FGA) at 300℃ in a H_2/N_2 (5%) mixed ambient for 30 minutes was performed to investigate the effect of FGA on electrical characteristic.

The process flow and device structure are shown in **Fig. 2.1**, **Fig. 2.2**. And the overview of all samples are shown in **Table 2.1**, **Table 2.2**.

2.3 Characteristics of Ge MOSCAP

2.3.1 C-V Characteristics of Ge MOSCAP

Fig. 2.3 shows the multi frequency C-V of Ge MOSCAPs with different PDA condition. We can see that the MOSCAPs used post deposition oxidation GeO_x have smaller EOT than RTO thermal grown GeO_2, which means Al_2O_3 layer could be an oxygen barrier that suppresses the growth of unnecessarily thick GeO_x ILs. A negative flat band voltage (V_{FB}) shift is often observed for Ge MOS capacitors, its origin has not yet been addressed [8]. The positive V_{FB} shift is shown in post deposition oxidation GeO_x samples compared with thermal grown GeO_2. The larger EOT is shown in PDA O_2 condition compared with PDA N_2, we think that the larger EOT of PDA O_2 is due to the growth of thicker GeO_x ILs.

Fig. 2.4 shows the multi frequency C-V of Ge MOSCAPs with different post deposition oxidation condition. The EOT value was scaled down to 1.41nm for HfO_2/Al_2O_3 with post deposition oxidation GeO_x 520℃ 3min sample. We can see that the MOSCAPs with higher post deposition oxidation temperature have larger EOT and hump become much smaller in depletion region, we supposed that the higher post deposition oxidation temperature may increase GeO_x interfacial layer thickness, which lower the capacitance value but improve the interface quality. The smaller EOT of gate stacks HfO_2/Al_2O_3 than gate stacks Al_2O_3/Al_2O_3 is due to the higher dielectric constant of HfO_2.

The oxide capacitance, EOT, flat band voltage and C-V hysteresis of all conditions are shown in **Table 2.3**, **Table 2.4**.

Although the interfacial layer GeO_2 gave the low density of interface states and high comprehensive performance, a large amount of fixed charge was introduced at the interface, which caused flat band voltage shifting that has not been systematically investigated yet [9]. High density fixed charges would cause lower mobility by strong coulomb scattering and shift of the threshold voltage.

The large C-V hysteresis is observed for our samples, more specifically for HfO_2 gate stacks, is caused by bulk oxide traps and is not related to the passivation of the Ge interface [10].

Fig. 2.5 (a) shows the Ge 3*d* XPS spectra of Al_2O_3/GeO_x/p-Ge with PDO 520 ℃ 30sec, PDO 520 ℃ 3min, PDO 550 ℃ 3min and RTO thermal GeO_2 520 ℃ 30sec. We can see that with an increase in the post deposition oxidation time or temperature, the GeO_x peak become larger, which means the GeO_x layer becomes thicker. This peak energy is lower than the core level of Ge^{4+}, indicating that the interfacial oxides could include Ge suboxides. **Fig. 2.5 (b)** shows the deconvolution of GeO_x peak to the peak corresponding to each Ge oxidation state. We can see that with an increase in the post deposition oxidation time or temperature, the Ge^{3+} peak become larger but the Ge^{4+} peak remain the same. While the RTO thermal GeO_2 520 ℃ 30sec sample has a large Ge^{4+} peak, no significant components of lower oxidation states are detected.

2.3.2 Conductance Method

The conductance method, proposed by Nicollian and Goetzberger in 1967, is one of the most sensitive methods to determine D_{it} [11]. It is the most complete method, because it yields D_{it} in the depletion and weak inversion portion of the bandgap and the capture cross-sections for majority carriers . Although Terman and high-low

frequency capacitance methods could extract D_{it}, they will largely overestimate the D_{it} value on Ge because of the humps caused by "minority carrier response" in the C-V curve. Conductance method is based on measuring the equivalent parallel conductance G_P of an MOSCAP as a function of bias voltage and frequency, the C-V measurement applying gate bias a small sinusoidal voltage with frequency f and amplitude 25mV, the conductance is representing the loss mechanism due to interface trap capture and emission of carriers.

The simplified equivalent circuit of MOSCAP appropriate for the conductance method is shown in **Fig. 2.6 (a)**. It consists of the oxide capacitance C_{ox} , the semiconductor capacitance C_S, and the interface trap capacitance C_{it} . The circuit can be simplified as in **Fig. 2.6 (b),**

$$C_P = C_S + \frac{C_{it}}{1+(\omega\tau_{it})^2} \quad \textbf{(2.1)}$$

$$\frac{G_P}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \quad \textbf{(2.2)}$$

Where

$C_{it} = q^2 D_{it}$

$\omega = 2\pi f$ (f = measurement frequency)

and $\tau_{it} = R_{it}C_{it}$

The interface trap time constant, given by

$$\tau_{it} = \frac{1}{V_{th}\sigma N} e^{\frac{\Delta E}{kT}} \quad \textbf{(2.3)}$$

Equations **(2.1)** and **(2.2)** are for interface traps with a single energy level in the bandgap. But in reality, interface trap are continuously distributed across the bandgap. Capture and emission occurs primarily by traps located within a few kT/*q* above and below the Fermi level, leading to a time constant dispersion and giving the normalized conductance as

$$\frac{G_P}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln[1+(\omega\tau_{it})^2] \quad \textbf{(2.4)}$$

From **(2.2)** and **(2.4),** conductance method is easier to extract D_{it} than capacitance based method, because it does not require C_s. For **(2.4),** when G_P/ω is plotted as a function of ω, the maximum appears at $\omega \approx 2/\tau_{it,}$ and at that maximum

$$D_{it} = \frac{2.5}{q}\left(\frac{G_P}{\omega}\right)_{MAX} \quad \textbf{(2.5)}$$

G_P/ω plots are repeated at different gate voltage to determine D_{it} from the maximum G_P/ω and determine τ_{it} from ω at the peak conductance location on the ω-axis.

In the measurement, we assumed the device to consist of the parallel $C_m - G_m$ combination in **Fig. 2.6 (c)**. The circuit gives G_P/ω in terms of the measured capacitance C_m, the oxide capacitance C_{ox}, and the measured conductance G_m as

$$\frac{G_P}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad \textbf{(2.6)}$$

According to $\tau_{it} = \frac{1}{V_{th}\sigma N} e^{\frac{\Delta E}{kT}}$, the interface trap time constant as a function of temperature determines the part of interface traps in the bandgap observable in the MOS admittance characteristic. The traps located near to midgap could be observed at higher temperatures, while traps located near the band edges could be observed at lower temperature. And for small bandgap Ge, mid gap traps are able to be observed at room temperature. The behavior of the interface trap time constant at room temperature as a function of capture cross section is shown in **Fig. 2.7**, which determines the part of interface traps in the bandgap observable in the MOS admittance characteristic. The electron thermal velocity, hole thermal velocity, effective density of states of conduction band (N_c) and effective density of states of valence band (N_v) are all taken into account.

Fig. 2.8 shows the $2.5G_P/\omega q$ versus frequency of Ge MOSCAPs with different PDA condition. **Fig. 2.9** shows the $2.5G_P/\omega q$ versus frequency of Ge MOSCAPs with

different post deposition oxidation condition, and the measurement is performed at room temperature. The peak value of each $2.5G_P/\omega q$ curve equals to the interface state density, and the frequency corresponding to the maximum $2.5G_P/\omega q$ can be converted to energy in the bandgap by the equation $\Delta E = kT\ln\left(\frac{V_{th}\sigma N}{\pi f}\right)$. Therefore, the interface state density versus energy in the bandgap plots can be obtained by repeated at different gate voltages to scan trap energies.

The value of capture cross section is assumed to be around 10^{-16} cm^2 in this thesis. D_{it} profiles of each samples near midgap is shown in **Fig. 2.10**. We can see that in **Fig. 2.10 (a)**, the post oxidation deposition samples have less interface state density than RTO thermal GeO_2, while we observed that Ge 3*d* XPS spectra of thermal GeO_2 samples have large Ge^{4+} peak, which means it is not necessary to have a large Ge^{4+} peak to passivate high-k/Ge interface, the Ge^{3+} peak shows better interface quality than Ge^{4+} peak in our studies. Also, the O_2 PDA samples have less interface state density than N_2 PDA samples, we think the reason of less interface state density may because of thicker GeO_x grown after O_2 PDA.

Fig. 2.10 (b) shows that the higher temperature of post deposition oxidation samples have less interface state density than the lower temperature of post deposition oxidation samples. The D_{it} of GeO_x/Ge MOS interface controlled by the GeO_x thickness has been studied [4]. We think the less interface state density is because of the thicker GeO_x interfacial layer and larger Ge^{3+} peak which the higher post deposition oxidation temperature grown.

The results shows more interface state density in the midgap, this phenomenon is called “weak inversion response” [12]. In the weak inversion regime, the C-V and conductance behavior becomes more complex, as shown in **Fig. 2.11**. In the weak inversion regime interface traps can communicate with both the majority and minority

carrier bands, as shown on the band diagram of **Fig. 2.11 (a)**, due to the small minority carrier time constant as the Fermi level located near midgap, the traps being filled and emptied by the ac voltage near the Fermi level can communicate with the minority band sufficiently fast and provide minority carriers to the band. When this dual communication occurs it leads to a larger conductance response than the typical depletion response.

The presence of the weak inversion response within the typical 1kHz to 1MHz measurement frequency window depends on the bandgap energy, the capture cross section and the temperature. For the Si/SiO_2 interface this effect has been shown to be present at lower frequencies at room temperature, not to occur in the 1kHz to 1MHz frequency window. But for small bandgap materials like germanium, the weak inversion response will be shown to be present in the 1kHz to 1MHz window. Therefore, conductance method for Ge MOSCAPs will overestimate the interface state density.

From the interface trap time constant $\tau_{it} = \frac{1}{V_{th}\sigma N} e^{\frac{\Delta E}{kT}}$, the smaller bandgap material, larger capture cross section and higher temperature lead weak inversion response more significant. Thus, the low temperature measurement can alleviate the dual communication.

2.4 Effect of FGA on Electrical Characteristics

We employed low temperature 300℃ forming gas annealing in a H_2/N_2 (5%) mixed ambient for 30 minutes to improve the interface quality. **Fig. 2.12** shows the multi frequency C-V of Ge MOSCAPs with different post deposition oxidation condition

after FGA, we can see that the hump becomes smaller in depletion region, and EOT is slightly larger.

The oxide capacitance, EOT, flat band voltage and C-V hysteresis with different post deposition oxidation condition before and after FGA are shown in **Table 2.5** and **Table 2.6**. The positive V_{FB} shift and lower C-V hysteresis is shown in the samples after FGA, we supposed that the positive V_{FB} shift and lower C-V hysteresis is because forming gas annealing lowering both fix charge and oxide trap charge. $2.5G_P/\omega q$ versus frequency of Ge MOSCAPs with different post deposition oxidation condition after FGA is shown in **Fig. 2.13**, and the D_{it} profiles of each samples near midgap, with and without FGA, is shown in **Fig. 2.14**. We can see that the D_{it} of all samples are decreased after FGA, with a reduction of 16% to 44%, which means forming gas annealing could improve the high-k/Ge interface.

2.5 Conclusions

Ge PMOS capacitors using post deposition oxidation method to form a thin GeO_x IL by oxidizing Ge surface beneath an ALD Al_2O_3 layer using high-k RTO was fabricated, the dependence of the GeO_x/Ge interface qualities on the post deposition oxidation conditions such as post deposition oxidation temperature and post deposition annealing ambient was investigated. Theory of the conductance method was discussed in detail, including weak inversion response. The Ge 3*d* XPS spectra of Al_2O_3/GeO_x/p-Ge with PDO 520 ℃ 30sec, PDO 520 ℃ 3min, PDO 550 ℃ 3min and RTO thermal GeO_2 520 ℃ 30sec is shown, the increase of post deposition oxidation time or temperature will larger the Ge^{3+} peak. The Ge^{3+} peak shows better interface quality than Ge^{4+} peak in our studies.

The EOT value was scaled down to 1.41 nm and a lower D_{it} value was obtained by PDO. The larger EOT but lower D_{it} value was obtained by using O_2 annealing. The positive V_{FB} shift and lower C-V hysteresis is shown in the samples after FGA, and the D_{it} value has been reduced 16% ~ 44% after FGA. Finally, the HfO_2/Al_2O_3 gate stack with PDO 520℃ 3min, PDA 500℃ 60sec N_2 was choose to be the best condition to fabricate Ge MOSFETs.

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- Cyclic DHF clean of P-Ge
- RTO thermal GeO_2 (for sample a and b)
- 10 cycles ALD Al_2O_3
- PDO 520°C 3min GeO_x passivation (for sample c and d)
- 50 cycles ALD HfO_2
- PDA 500°C 60sec N_2/O_2
- Shadow mask define capacitor area
- Ti/Pt deposition
- Backside contact (Al)

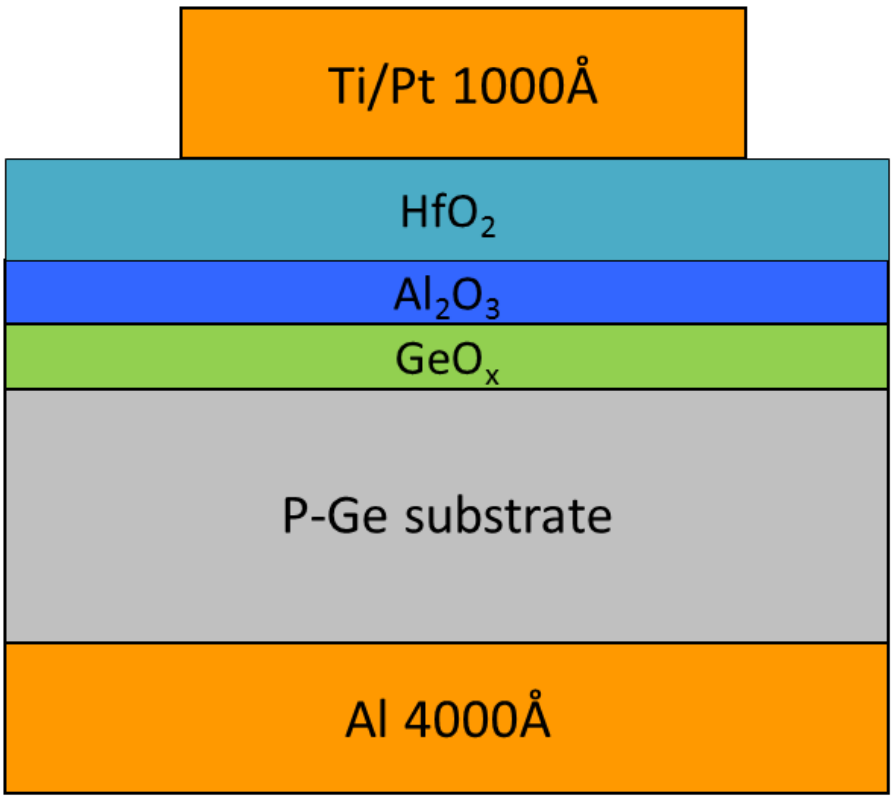


Fig. 0.1 The process flow and device structure with different PDA condition.

- Cyclic DHF clean of P-Ge
- 10 cycles ALD Al_2O_3
- PDO 520°C/550°C 3min GeO_2 passivation
- 50 cycles ALD Al_2O_3 (for sample A and B)
- 50 cycles ALD HfO_2 (for sample A and B)
- PDA 500°C 60sec N_2
- Shadow mask define capacitor area
- Ti/Pt deposition
- Backside contact (Al)
- FGA (300℃, 30min)

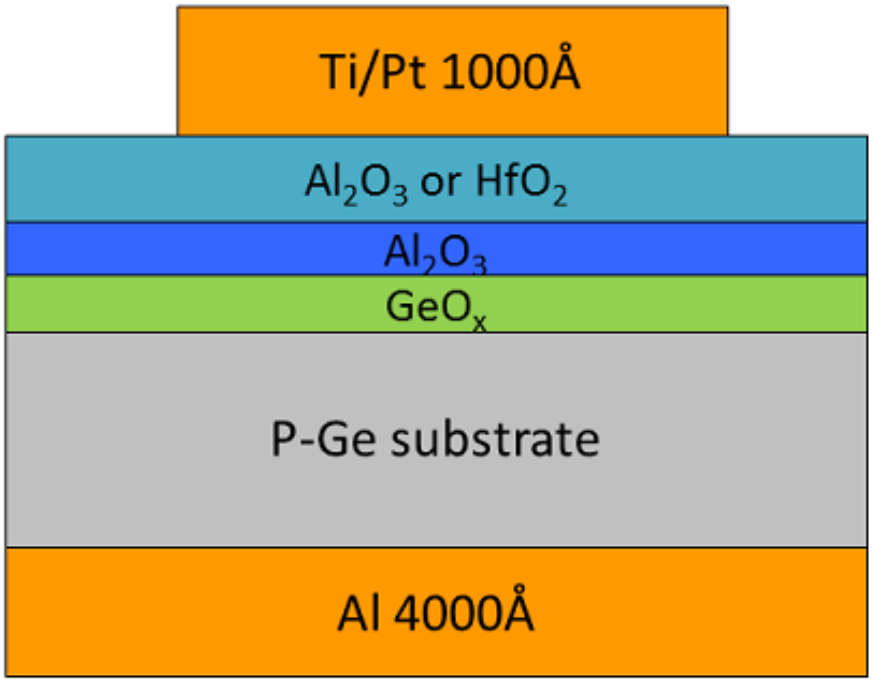


Fig. 0.2 The process flow and device structure with different post deposition oxidation condition.

No.	Thermal GeO_2	ALD Al_2O_3	PDO	ALD HfO_2	PDA
a	520℃ 30sec	10cycles	---	50cycles	500℃ 60sec N_2
b	520℃ 30sec	10cycles	---	50cycles	500℃ 60sec O_2
c	---	10cycles	520℃ 3min	50cycles	500℃ 60sec N_2
d	---	10cycles	520℃ 3min	50cycles	500℃ 60sec O_2

Table 0.1 The overview of a-d samples with different PDA condition.

No.	ALD Al_2O_3	PDO	ALD Al_2O_3	ALD HfO_2	PDA
A	10cycles	520℃ 3min	50cycles	---	500℃ 60sec N_2
B	10cycles	550℃ 3min	50cycles	---	500℃ 60sec N_2
C	10cycles	520℃ 3min	---	50cycles	500℃ 60sec N_2
D	10cycles	550℃ 3min	---	50cycles	500℃ 60sec N_2

Table 0.2 The overview of A-D samples with different RTO condition.

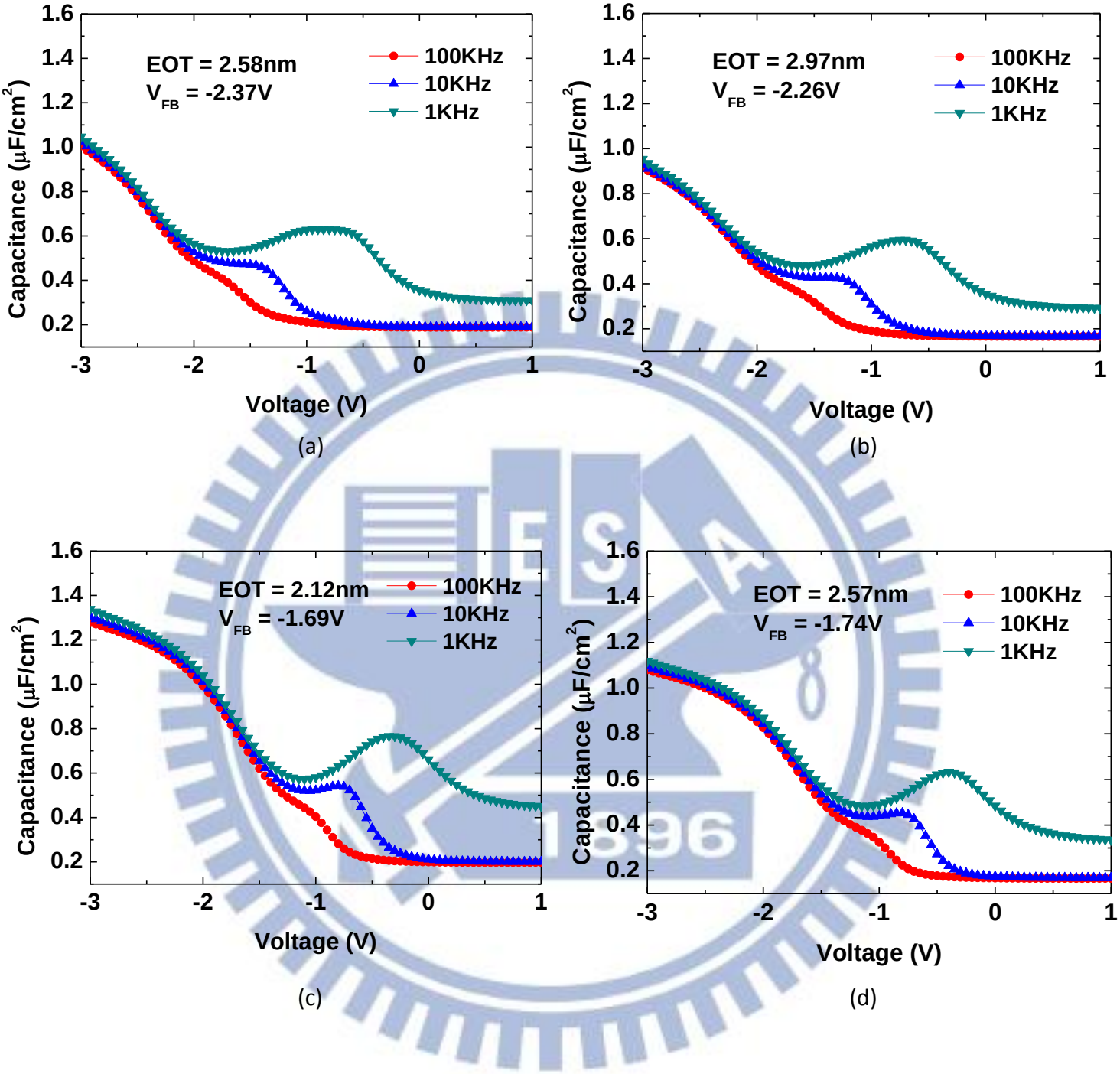


Fig. 0.3 The multi frequency C-V of Ge MOSCAPs with different PDA condition. (a) RTO thermal GeO_2 520℃ 30sec with PDA 500℃ 60sec N_2 (b) RTO thermal GeO_2 520℃ 30sec with PDA 500℃ 60sec O_2 (c) post deposition oxidation 520℃ 3min with PDA 500℃ 60sec N_2 (d) post deposition oxidation 520℃ 3min with PDA 500℃ 60sec O_2.

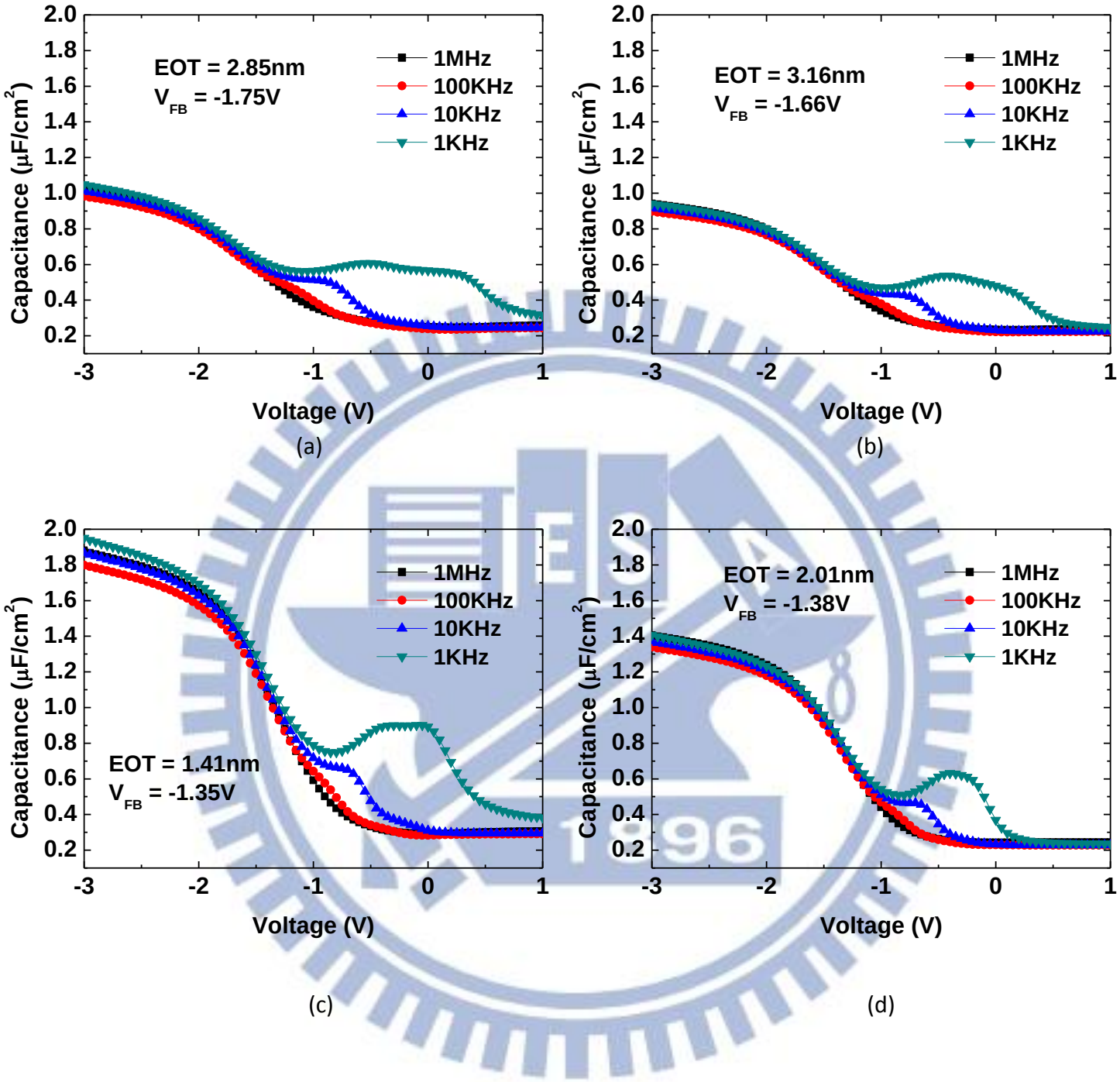


Fig. 0.4 The multi frequency C-V of Ge MOSCAPs with different post deposition oxidation condition. (a) Al_2O_3/Al_2O_3 with post deposition oxidation GeO_2 520℃ 3min (b) Al_2O_3/Al_2O_3 with post deposition oxidation GeO_2 550℃ 3min (c) HfO_2/Al_2O_3 with post deposition oxidation GeO_2 520℃ 3min (d) HfO_2/Al_2O_3 with post deposition oxidation GeO_2 550℃ 3min.

No.	C_{OX} (μF/cm^2)	EOT (nm)	V_{FB} (V)	Hysteresis (V)
a	1.34	2.58	-2.37	0.73
b	1.16	2.97	-2.26	0.7
c	1.63	2.12	-1.69	0.69
d	1.34	2.57	-1.74	0.7

Table 0.3 The C-V hysteresis with different PDA condition.

No.	C_{OX} (μF/cm^2)	EOT (nm)	V_{FB} (V)	Hysteresis (V)
A	1.21	2.85	-1.75	0.34
B	1.09	3.16	-1.66	0.36
C	2.45	1.41	-1.35	0.52
D	1.71	2.01	-1.38	0.49

Table 0.4 The C-V hysteresis with different post deposition oxidation condition.

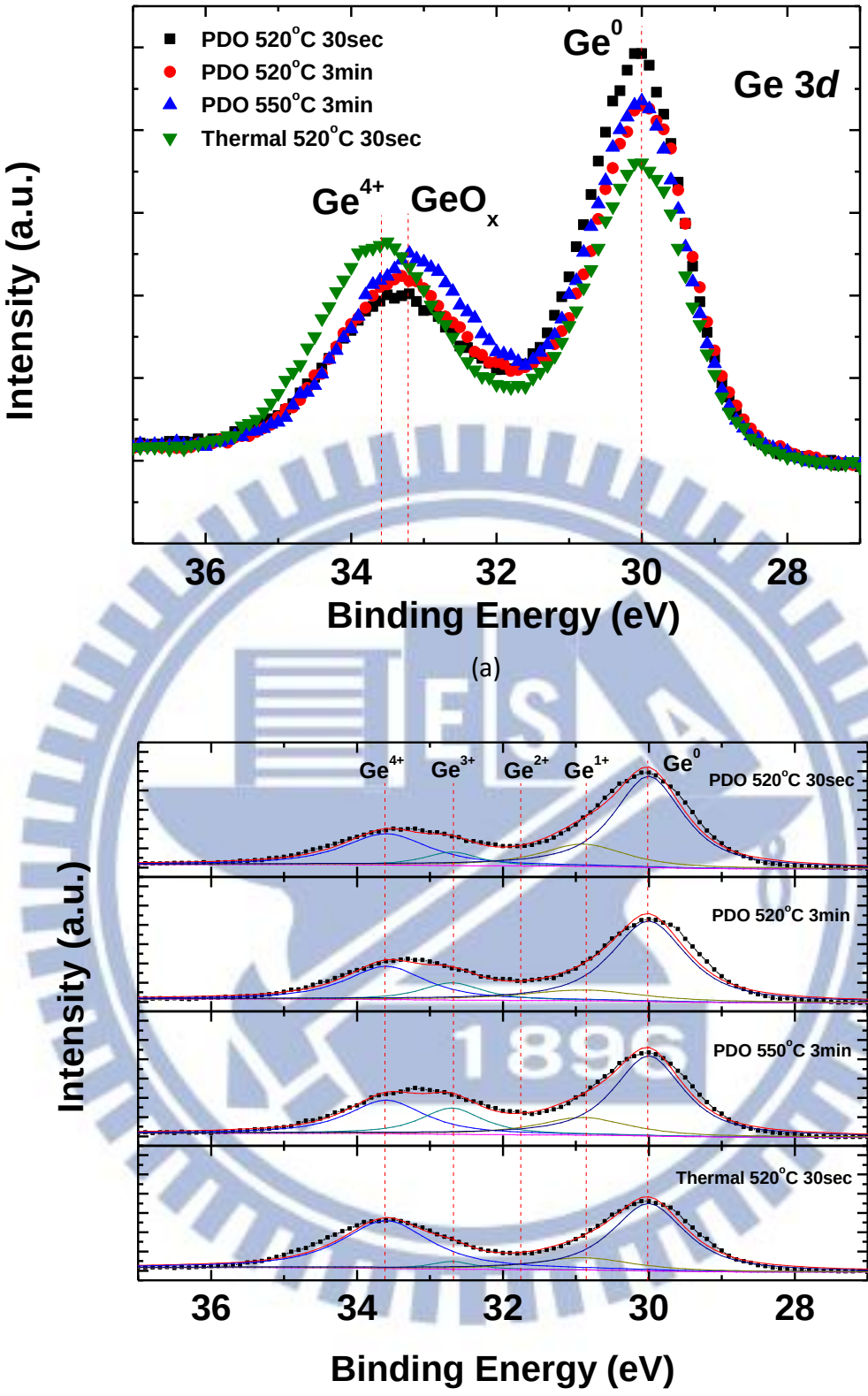


Fig. 0.5 The XPS spectra of Al_2O_3/GeO_x/p-Ge with different PDO and thermal grown GeO_x condition.

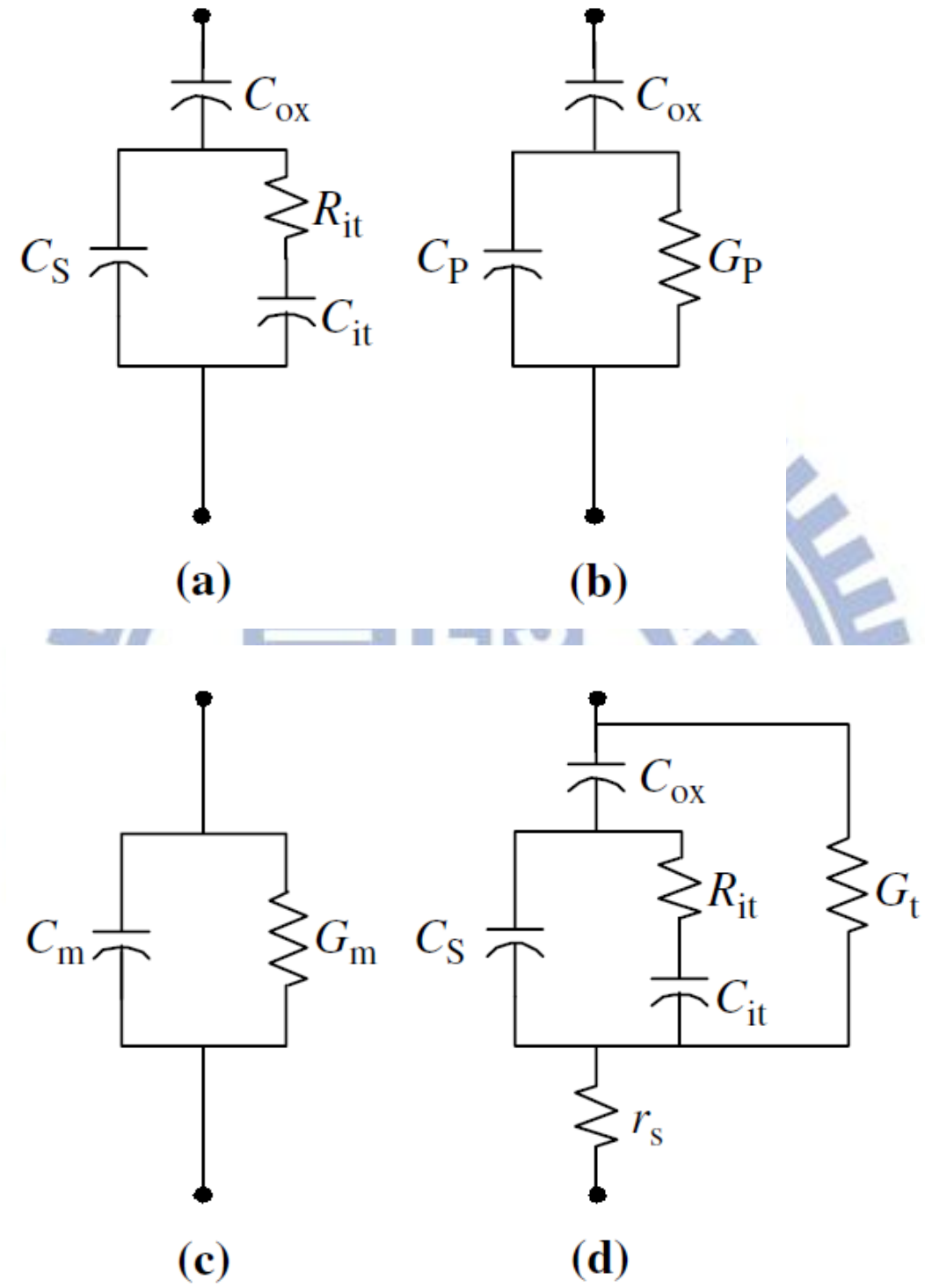


Fig. 0.6 Equivalent circuits for conductance measurements; (a) MOSCAP with interface trap time constant $\tau_{it} = R_{it}C_{it}$, (b) simplified circuit of (a), (c) measured circuit, (d) including series r_s resistance and tunnel conductance G_t .

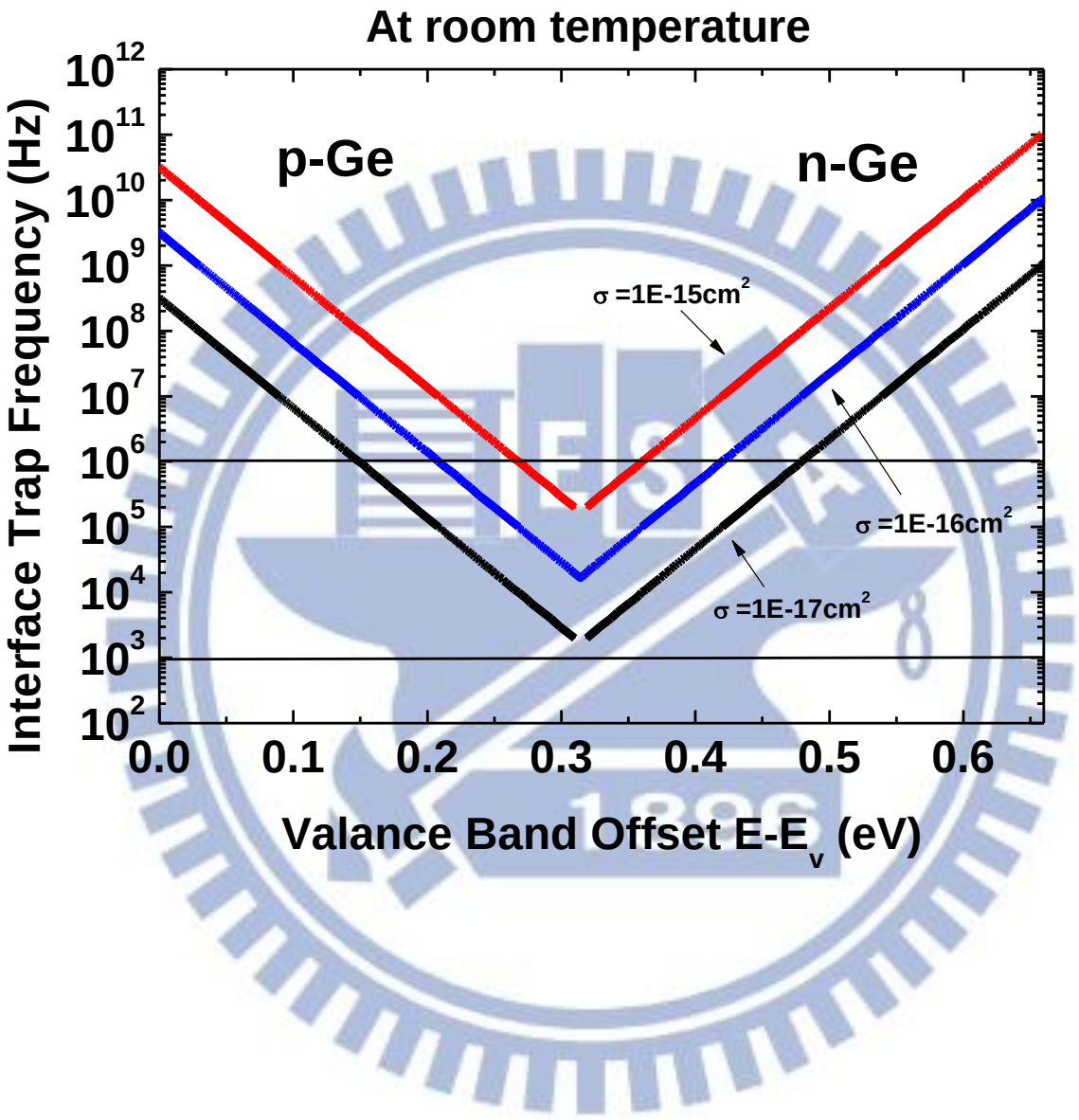


Fig. 0.7 The behavior of the interface trap time constant at room temperature as a function of capture cross section determines the part of interface traps in the bandgap observable in the MOS admittance characteristic.

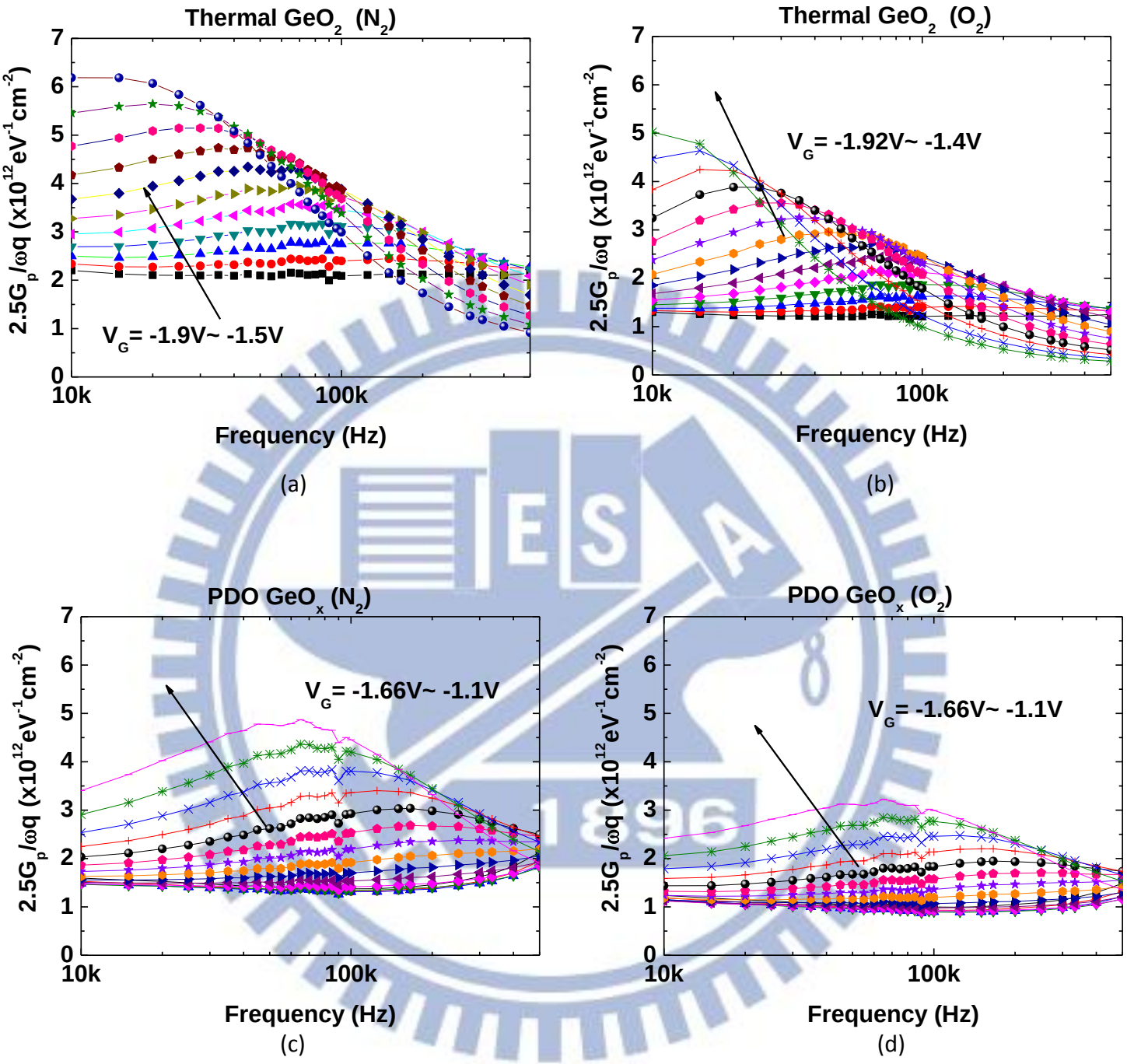


Fig. 0.8 $2.5G_P/\omega q$ versus frequency of Ge MOSCAPs with different PDA condition. (a) RTO thermal GeO_2 520℃ 30sec with PDA 500℃ 60sec N_2 (b) RTO thermal GeO_2 520℃ 30sec with PDA 500℃ 60sec O_2 (c) post deposition oxidation 520℃ 3min with PDA 500℃ 60sec N_2 (d) post deposition oxidation 520℃ 3min with PDA 500℃ 60sec O_2.

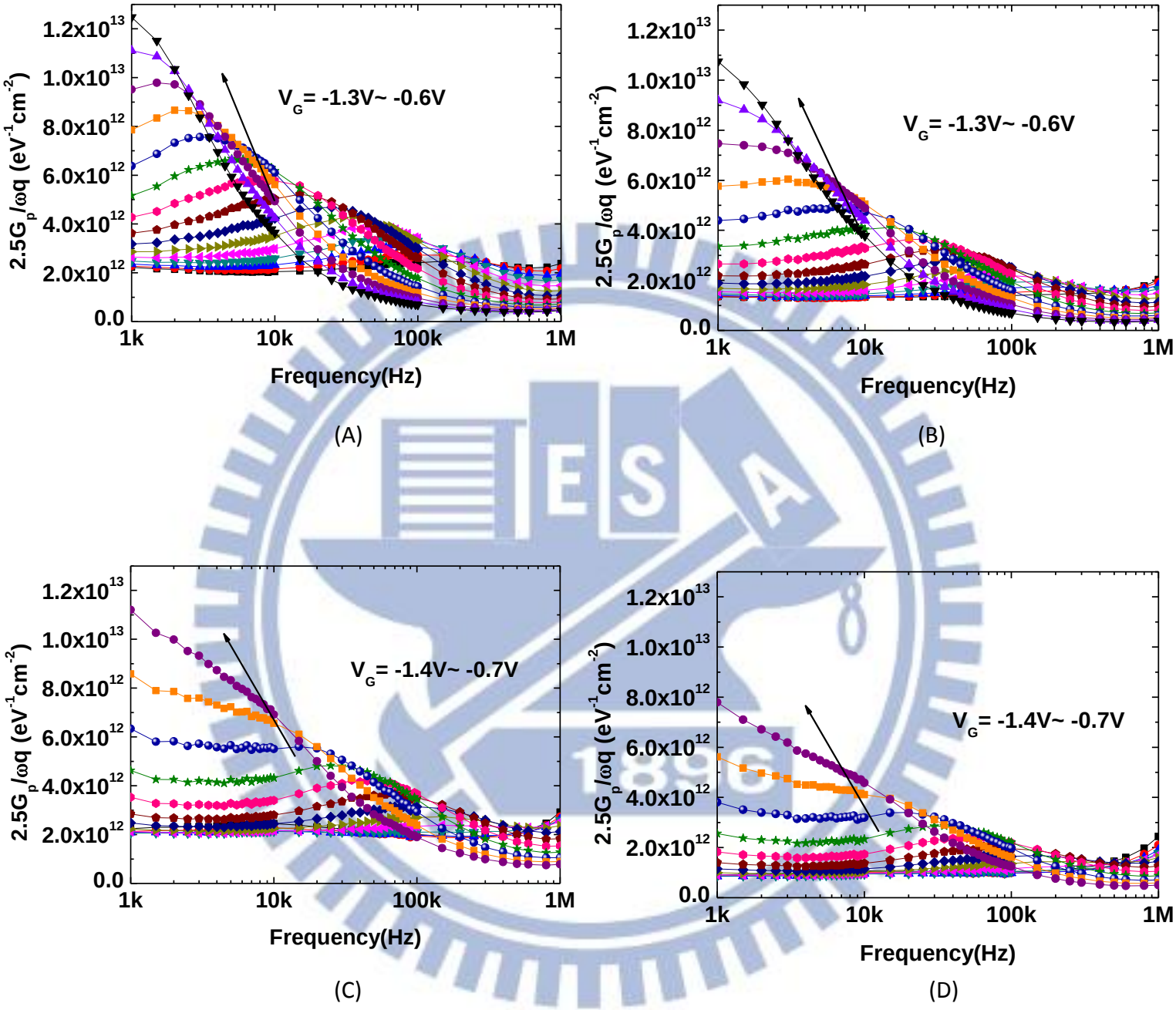


Fig. 0.9 $2.5G_P/\omega q$ versus frequency of Ge MOSCAPs with different post deposition oxidation condition. (A) Al_2O_3/Al_2O_3 with post deposition oxidation GeO_2 520℃ 3min (B) Al_2O_3/Al_2O_3 with post deposition oxidation GeO_2 550℃ 3min (C) HfO_2/Al_2O_3 with post deposition oxidation GeO_2 520℃ 3min (D) HfO_2/Al_2O_3 with post deposition oxidation GeO_2 550℃ 3min.

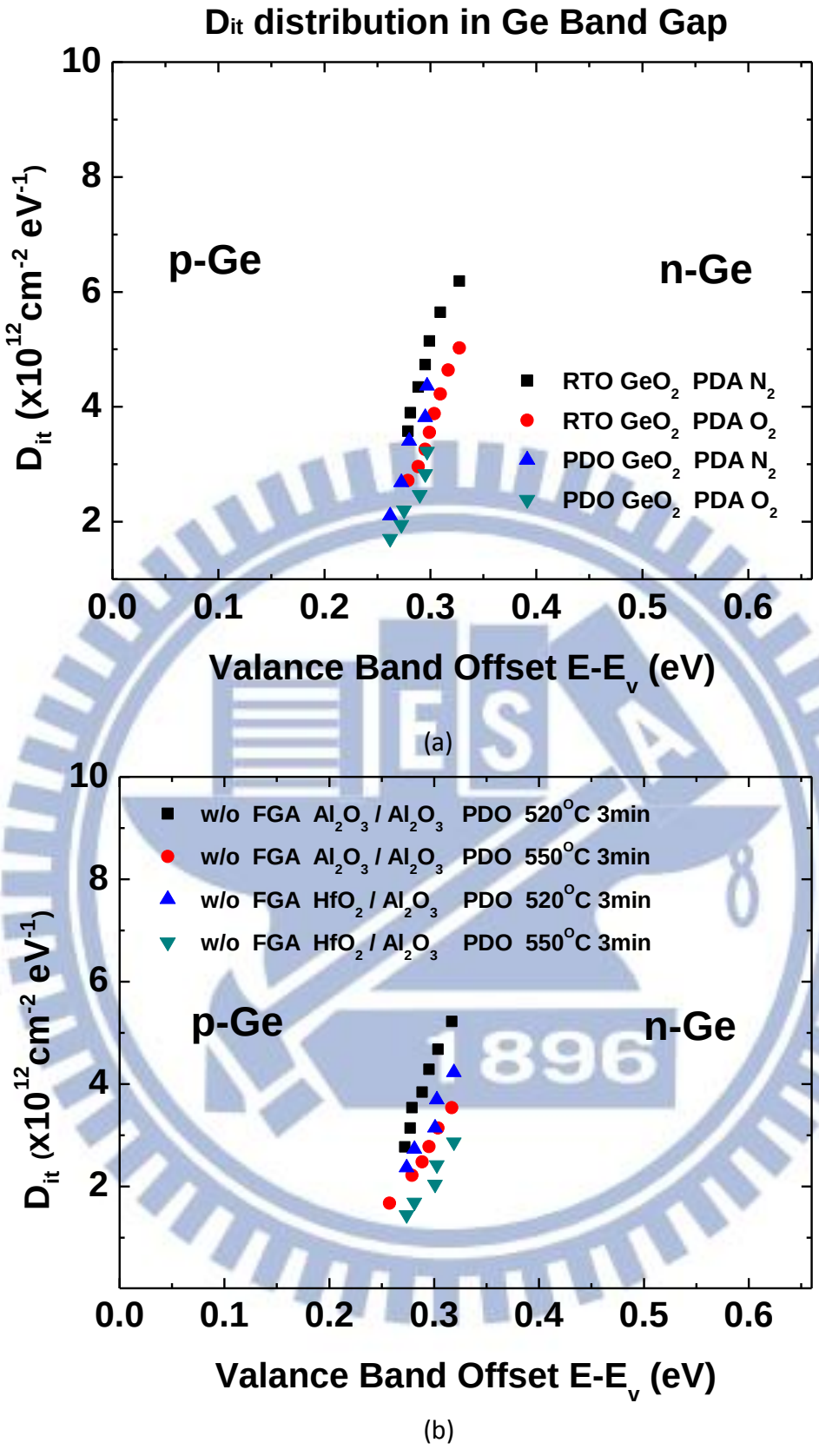


Fig. 0.10 D_{it} profiles of each samples near midgap (a) samples a b c d and (b) samples A B C D.

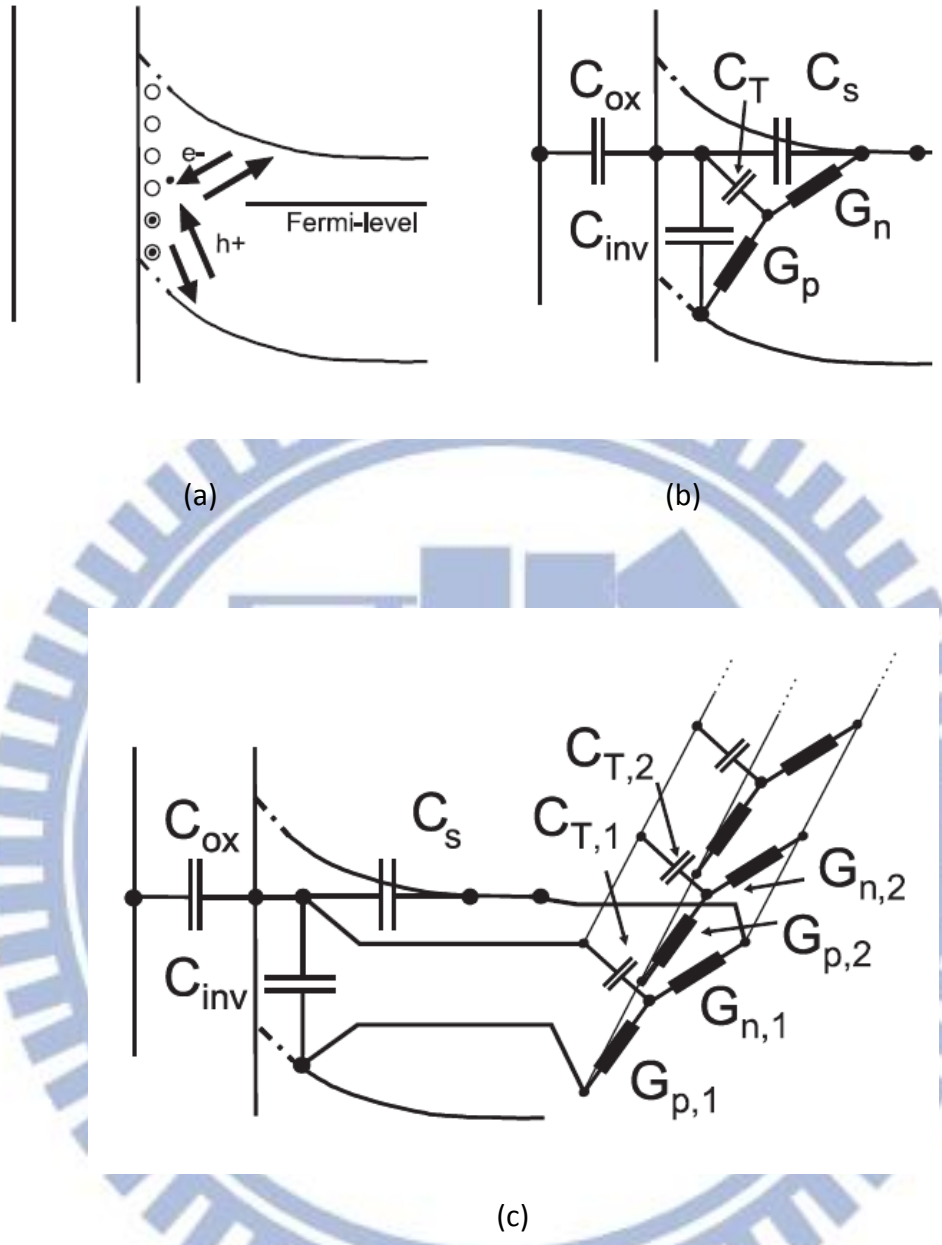


Fig. 0.11 A band diagram showing the weak inversion response (a) and the general equivalent circuits used to model the MOS capacitor C-V and G-V characteristics across the bandgap for an n-type capacitor. The first circuit (b) models one trap only: C_{ox} is the oxide capacitance, C_{inv} the inversion capacitance, C_{dep} the depletion (and accumulation) capacitance, C_T the trap capacitance and G_n and G_p electron and hole trap conductances. For a distribution a series of Y-circuits is used (c).

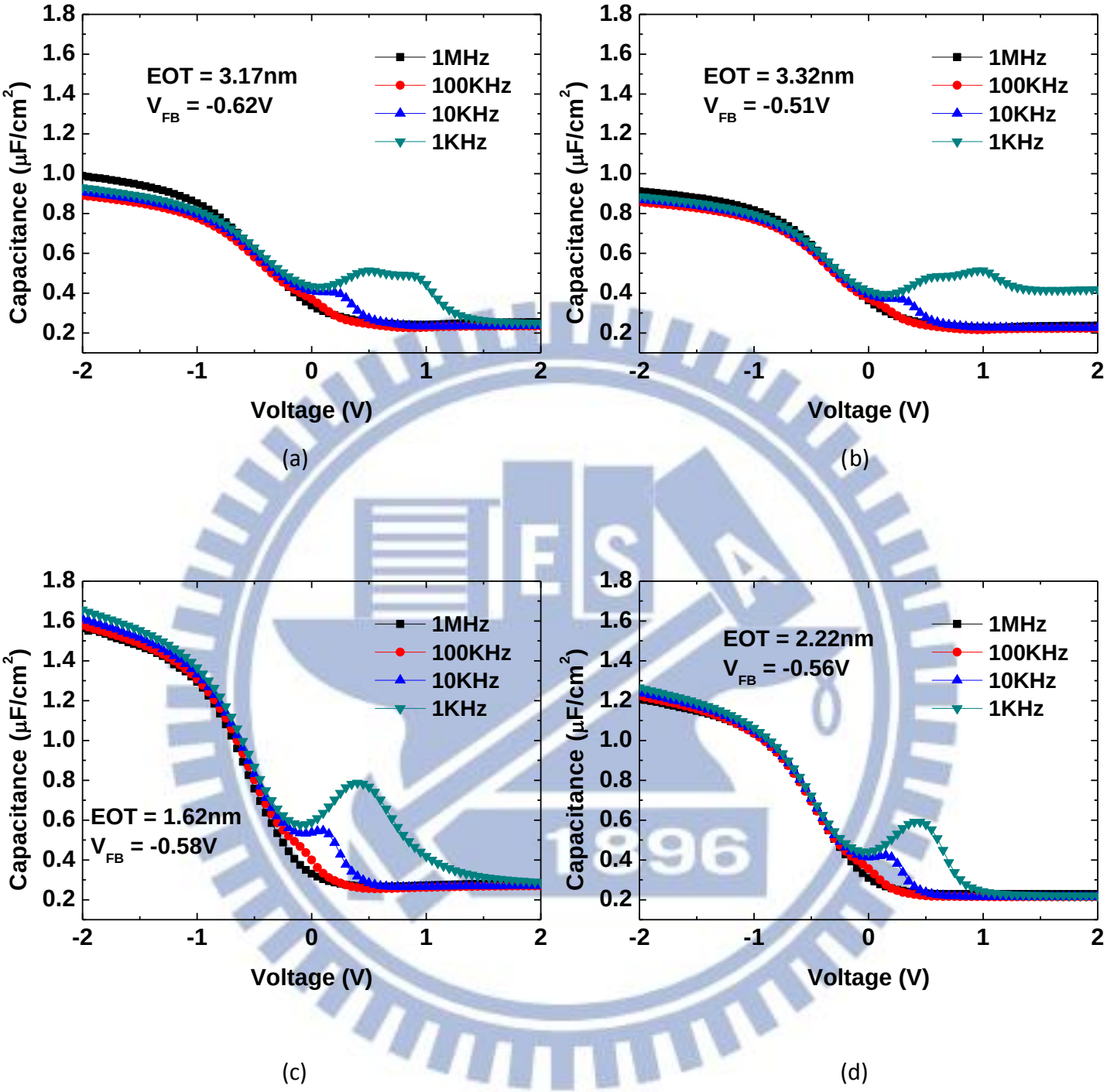


Fig. 0.12 The multi frequency C-V of Ge MOSCAPs with different post deposition oxidation condition after FGA. (a) Al_2O_3/Al_2O_3 with post deposition oxidation GeO_2 520℃ 3min (b) Al_2O_3/Al_2O_3 with post deposition oxidation GeO_2 550℃ 3min (c) HfO_2/Al_2O_3 with post deposition oxidation GeO_2 520℃ 3min (d) HfO_2/Al_2O_3 with post deposition oxidation GeO_2 550℃ 3min.

No.	C_{OX} (μF/cm^2)	EOT (nm)	V_{FB} (V)	Hysteresis (V)
A	**1.21**	**2.85**	**-1.75**	**0.34**
B	**1.09**	**3.16**	**-1.66**	**0.36**
C	**2.45**	**1.41**	**-1.35**	**0.52**
D	**1.71**	**2.01**	**-1.38**	**0.49**

Table 0.5 The C-V hysteresis with different post deposition oxidation condition before FGA.

No.	C_{OX} (μF/cm^2)	EOT (nm)	V_{FB} (V)	Hysteresis (V)
A	**1.09**	**3.17**	**-0.62**	**0.19**
B	**1.04**	**3.32**	**-0.51**	**0.18**
C	**2.13**	**1.62**	**-0.58**	**0.48**
D	**1.56**	**2.22**	**-0.56**	**0.43**

Table 0.6 The C-V hysteresis with different post deposition oxidation condition after FGA.

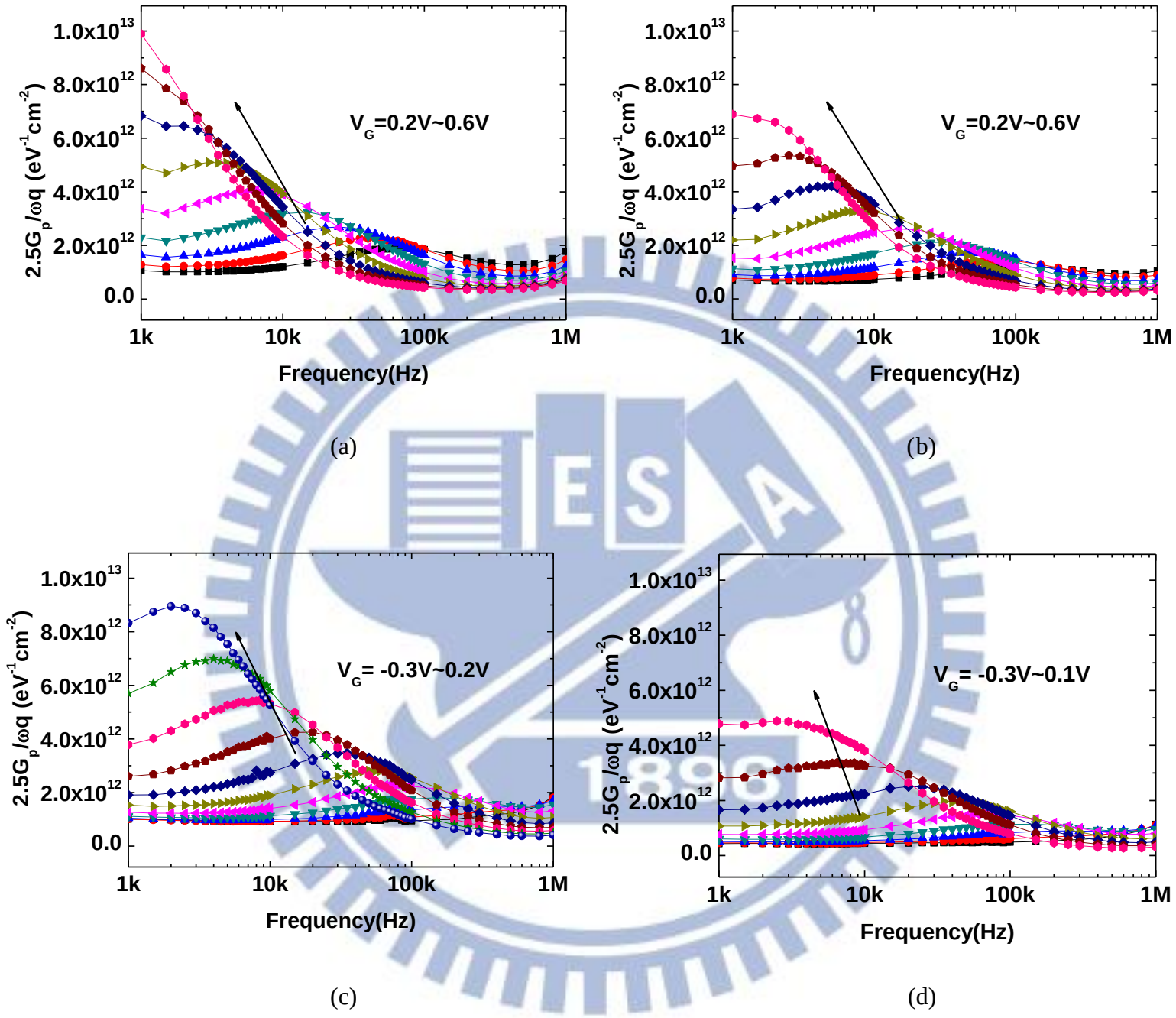
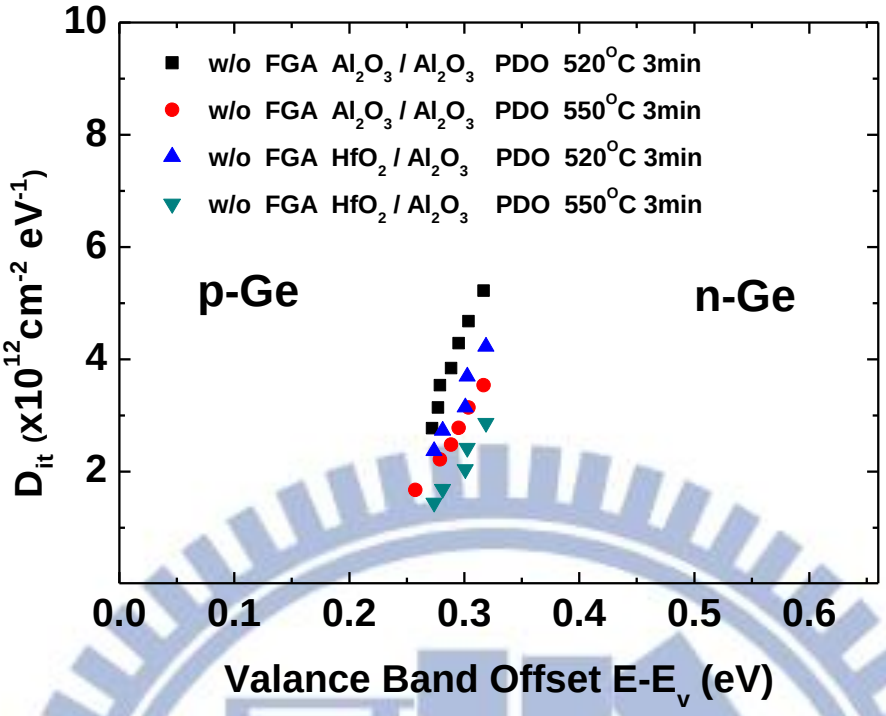
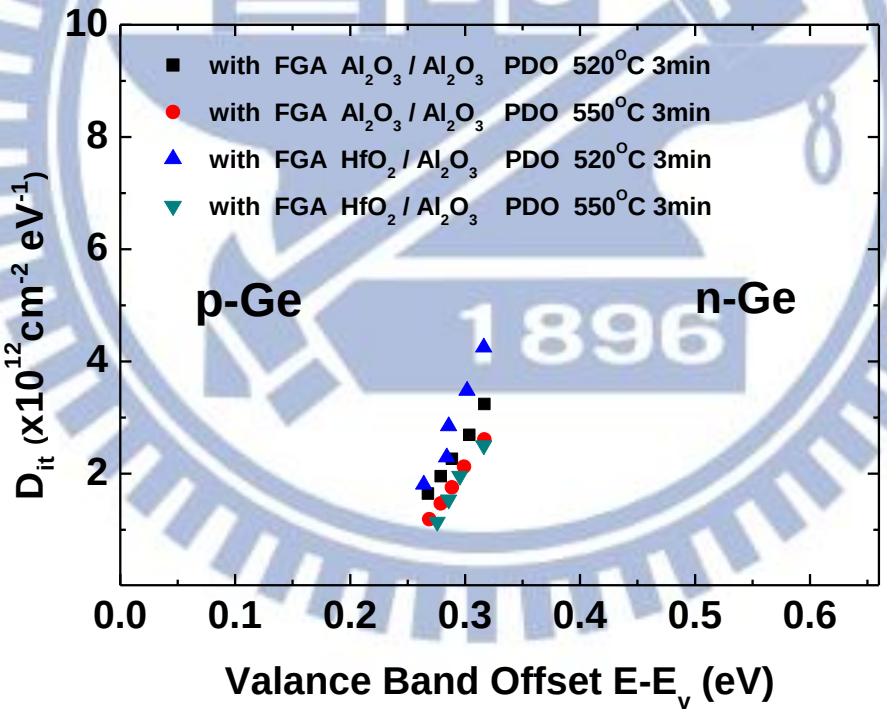


Fig. 0.13 $2.5G_P/\omega q$ versus frequency of Ge MOSCAPs with different post deposition oxidation condition after FGA. (a) Al_2O_3/Al_2O_3 with post deposition oxidation GeO_2 520℃ 3min (b) Al_2O_3/Al_2O_3 with post deposition oxidation GeO_2 550℃ 3min (c) HfO_2/Al_2O_3 with post deposition oxidation GeO_2 520℃ 3min (d) HfO_2/Al_2O_3 with post deposition oxidation GeO_2 550℃ 3min.



(a)



(b)

Fig. 0.14 D_{it} profiles of each samples near midgap (a) samples A B C D without FGA (b) samples A B C D with FGA.

Chapter 3

Germanium MOSFET with Atomic-Layer-Deposited $HfO_2/Al_2O_3/GeO_x$/Ge Gate Stack Fabricated by Post deposition oxidation

3.1 Introduction

Recently, it has been increasingly difficult to further improve the performances of Si complementary metal–oxide–semiconductor (CMOS) devices through the conventional device scaling [1]. To keep up with the performance growth which indicated by the ITRS roadmap[2], device engineers need to introduce more and more new materials [3], the high mobility semiconductor materials received interest in MOSFET applications to pursue much higher device performance. Germanium is an attractive candidate for channel material due to its high electron/hole mobility and the compatibility with the conventional Si integration technologies.

However, a major problem which has retarded scaling of Ge devices is interface passivation, unlike SiO_2 with a highly thermal stability, Ge native oxides are water soluble and thermal instable, it is difficult to achieve a high-quality oxide/Ge interface due to the bad surface properties of Ge. Another problem is Ge has a smaller bandgap than conventional Si substrate, which resulting in higher junction leakage currents.

Although Ge PMOSFETs with mobilities above 300 $cm^2V^{-1}s^{-1}$ have been reported recently [4], Ge NMOSFETs have exhibited poor drive currents and inversion mobilities lower than universal Si mobility. The two main mechanisms of NMOSFETs mobility and current drive degradation are the high interface state density D_{it} near the conduction band edge and the high source/drain parasitic resistance [5]. Moreover, the significant electron trapping due to the interfacial band alignment between the native oxide of Ge and the high-k dielectrics has been suggested as a factor limiting the performance and the reliability for Ge NMOSFETs [6]. Therefore, the passivation of the gate oxide/channel interface is needed to address the Ge NMOSFETs performance problem.

In this chapter, both germanium NMOSFET and PMOSFET were fabricated. Effects of forming gas annealing (FGA) on junction or device characteristics are discussed, including series resistance, subthreshold swing and mobility.

3.2 Fabrication of Gate-Last Ge MOSFET

(100)-oriented n-Ge substrate and (100)-oriented p-Ge substrate with resistivity ca. 0.6Ω·cm ~ 0.94Ω·cm and ca. 0.01Ω·cm ~ 0.05Ω·cm were used for Ge PMOSFET and Ge NMOSFET fabrication. All of the samples were pre-cleaned by successive diluted HF (20:1) and DI water rinsing to remove the native oxide, then a 420-nm-thick SiO_2 layer was capped for the field oxide by PECVD.

First, the source/drain region was opened through the first mask, followed by implantation of the Boron (1×10^{15} cm^{-2}, 20 keV) into the n-Ge and Phosphorous (1×10^{15} cm^{-2}, 20 keV) into the p-Ge, with dopant activation condition 500℃ 10 second and 600℃ 10 second, respectively. Next, active area (AA) was opened through the

second mask, after that, an 10 cycles ALD-Al_2O_3 thin film grown on each sample at 250℃, a thin GeO_x layer being formed by post deposition oxidation to passivate the Ge surface, with oxidation condition 520℃ 3min. A 50 cycles HfO_2 layer was deposited by ALD at 250℃, post deposition annealing was performed at 500℃ 60sec with N_2. Right after dry etching the contact hole on S/D region through the third mask, a 400nm Al metallization was performed which was then patterned to define metal pads through the fourth mask. Finally, a 400nm Al layer was deposited as the backside contact.

Forming gas annealing (FGA, 300℃, 30 min, H_2/N_2=5%) was performed to investigate the effect of FGA on electrical characteristics.

The process flow and device structure are shown in **Fig. 3.1.**

3.3 Effect of FGA on Ge MOSFET Electrical Characteristics

3.3.1 Ge junction Characteristic

Fig. 3.2 (a) (b) showed the junction of PMOSFET and NMOSFET, before and after performing 300℃ FGA, respectively. For PMOSFET, the reverse bias leakage current density (J_R) at -1V are 8.5×10^{-3} A/cm^2 before FGA and 1×10^{-2} A/cm^2 after FGA, while the forward bias current (J_F) at 1 V are 1.2×10^{2} A/cm^2 before FGA and 9.5×10^{1} A/cm^2 after FGA, on/off ratio about 4 orders is achieved. For NMOSFET, the reverse bias leakage current density at 1V are 1.1×10^{-2} A/cm^2 before FGA and 9.6×10^{-3} A/cm^2 after FGA, while the forward bias current at -1 V are 5.8×10^{1} A/cm^2 before FGA and 3.1×10^{1} A/cm^2 after FGA, on/off ratio about 3.5 orders is achieved.

The higher reverse leakage current compare to Si devices is because of the lower bandgap of germanium.

For both PMOSFET and NMOSFET, the forward bias current after FGA is lower. We think the reason for the decreasing forward bias current after FGA is the higher series resistance due to lower doping concentration caused by dopant diffusion.

3.3.2 Device Characteristic

The effects of FGA at 300 ^{o}C on the PMOSFET and NMOSFET are shown in **Fig. 3.3** and **Fig. 3.4**, where the I_D-V_G and I_S-V_G plots are displayed. For both PMOSFET and NMOSFET, the better subthreshold swing (165mV/dec for PMOSFET and 151mV/dec for NMOSFET) after FGA are observed, and the on/off ratio about 1.4×10^3 for PMOSFET and 2.3×10^3 for NMOSFET are obtained. We believe that the better subthreshold swing after FGA is due to the improved high-k/Ge interfaces, the lower D_{it} caused the smaller subthreshold swing. And the higher on currents are observed for both samples after FGA, which may due to the better interface quality and less coulomb scattering. The I_D-V_G plots of both PMOSFET and NMOSFET have higher off current compared with I_s-V_G plots, which because of the junction leakage. We can see a positive shift of V_{FB} after FGA, which may due to the reduction of oxide trap and fix charge.

Fig. 3.5 shows the effects of FGA at 300 ^{o}C on the I_D-V_D characteristics on both PMOSFET and NMOSFET. The PMOSFET has larger drive current after FGA, which exhibit higher performance. The NMOSFET has lower drive current after FGA at small drain voltage, but the drive current will become larger when drain voltage grows higher. We think the reason of lower drive current after FGA at small drain

voltage is the dopant diffusion causing lower dopant concentration, and the effective tunneling barrier becomes large, which the drain voltage need become higher to lower the effective tunneling barrier, shown in **Fig. 3.6 (a)**. **Fig. 3.6 (b)** shows measured resistance versus channel length on mask for PMOSFETs, we extract the source/drain series resistance (R_{SD}) by the Terada and Muta method:

$$R_m = R_{ch} + R_{SD} = \frac{L - \Delta L}{W_{eff}\mu_{eff}C_{ox}(V_g - V_{th})} + R_{SD} \quad \textbf{(3.1)}$$

Where R_{ch} is channel resistance and R_{SD} is source/drain series resistance.

For both PMOSFET and NMOSFET, R_{SD} is increased after FGA, we think it due to the more dopant diffusion and thus lower source/drain doping concentration.

To extract the effective mobility, the effective mobility gives

$$\mu_{eff} = \frac{g_d L}{W Q_{inv}} \quad \textbf{(3.2)}$$

Where the drain conductance is defined as

$$g_d = \frac{\partial I_D}{\partial V_{DS}} \mid V_{GS} = constant \quad \textbf{(3.3)}$$

And the measure of Q_{inv} from capacitance measurement

$$Q_{inv} = \int_{-\infty}^{V_{GS}} C_{GC}\, dV_{GS} \quad \textbf{(3.4)}$$

The mobile channel charge density is determined from the gate to channel capacitance, C_{GC}. Then C_{GC} is measured using the connection of **Fig. 3.7**, the capacitance meter is connected between the gate and the source/drain connected together with the substrate grounded. For $V_{GS} < V_T$ **(Fig. 3.7 (a))**, the channel region is accumulated and the overlap capacitances $2C_{ov}$ are measured. For $V_{GS} > V_T$ **(Fig. 3.7 (b))**, the surface is inverted and all three capacitances, $2C_{ov} + C_{ch}$, are measured.

Fig. 3.8 shows the effect of FGA at 300 ^{o}C on Q_{inv} and g_d for PMOSFET, we can see a positive shift of Q_{inv} and g_d curve after FGA, which may due to the reduction of oxide trap and fix charge.

Effective hole mobility versus inversion charge is plotted in **Fig. 3.9,** with and without FGA at 300 ^{o}C. The higher effective hole mobility is observed after FGA, which may due to the better interface quality and less coulomb scattering. We didn't show electron mobility, because the huge resistance causing large errors on I-V and C-V measurement, which lead the measured electron mobility much lower than real value.

The NMOSFET has shown poor drive current, there are a few mechanisms behind poor NMOS performance. High source/drain parasitic resistance, inversion charge loss due to trapping in the high-k gate dielectric and high interface trap density are identified as the mechanisms for Ge NMOS performance degradation [7].

Since p-type dopants in Ge could be activated at lower temperature with small redistribution, Ge PMOSFET demonstrations with metal gate electrode and high-k dielectric have not been an issue, but the relatively higher thermal budget required to n-type dope Ge causes significant junction diffusion, which lead to high source/drain parasitic resistance [8]. The voltage drop across the high source/drain parasitic resistance causes a huge reduction in the drain current, and the measured mobility by the split C-V appears to be lower than the real value.

The GeO_2 bandgap was found to be ~5.1eV, the valance band offset was ~3.8 eV, and the conduction band offset was ~0.6 eV. The low conduction band offset of GeO_2 is a potential problem, which can cause severe charge trapping in the bulk traps of Al_2O_3 and the slow traps at the GeO_2/Al_2O_3 interface. The low conduction band offset of GeO_2 and the band alignment is shown in **Fig. 3.10**, the electron trapping by the slow traps and the bulk traps in the NMOS inversion regime. The carriers trapped in the slow traps in the Ge NMOS inversion regime can cause a threshold-voltage shift. Depending on the energy levels of the slow traps, the reemission of carriers

may take longer than the gate voltage sweep speed, which will result in a flatband voltage V_{FB} shift in the C–V characteristics. Furthermore, the electron trapping takes place in the inversion regime of the NMOS retarding the formation of the inversion layer. The loss of inversion charge can cause lower Ion and a lower extracted mobility.

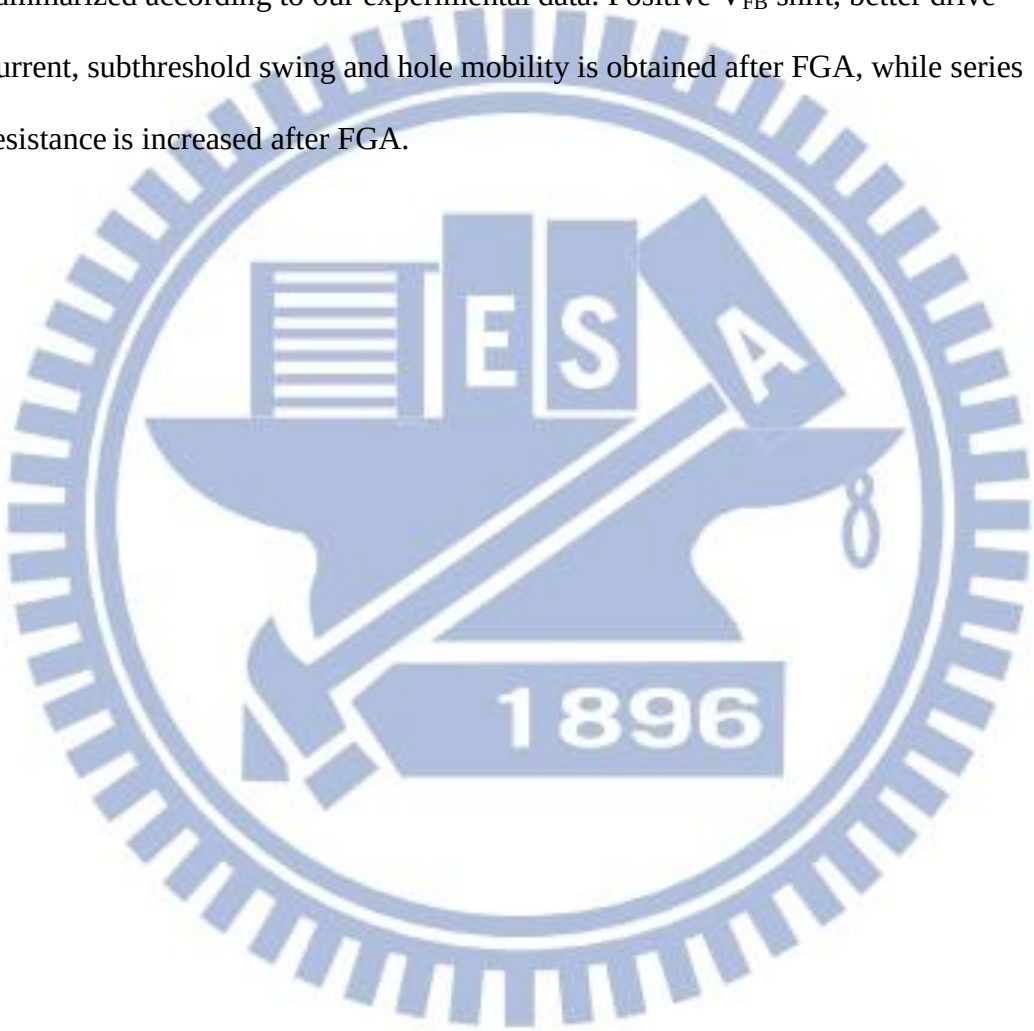
The charge neutrality level CNL close to the valence band edge and the acceptor type traps in the Ge bandgap have been proposed as intrinsic problems for Ge N-MOSFETs [9]. The CNL in Ge is estimated to be only 0.09–0.08 eV above the valance band maximum. As shown in **Fig. 3.11**, the charged acceptor and donor dangling bond states are both located in the lower part of the Ge gap at energies $E_{acc}=E_v+0.11$ eV and $E_{don}=E_v+0.05$ eV. In most cases, the Fermi level is above the acceptor and donor levels, which means that most of the acceptors are filled, building a large negative charge at the surface. This may cause excess Coulomb scattering thus degrading the channel mobility of Ge NMOSFET, it can be a significant problem for Ge NMOS if the interface trap density is above 10^{12} cm^{-2} eV^{-1} levels.

3.4 Conclusions

In Chapter 3, we investigated the effect of FGA on Ge junction and device characteristics. On/off ratio of our p^+n junction and PMOSFET reached 4 orders and 1.4×10^3 respectively (500℃ 10 sec dopant activation, W/L = 100μm/5μm), with better subthreshold swing (165mV/dec) obtained after FGA. And on/off ratio of our n^+p junction and NMOSFET reached 3.5 orders and 2.3×10^3 respectively (600℃ 10

sec dopant activation, W/L = 100μm/5μm), with better subthreshold swing (151mV/dec) obtained after FGA. For both PMOSFETs and NMOSFETs, R_{SD} is increased after FGA, The higher hole mobility is observed after FGA, a peak hole mobility of 375 cm^2/Vs after FGA is obtained.

Pros and cons of FGA at 300℃ 30 min on both PMOSFET and NMOSFET were summarized according to our experimental data. Positive V_{FB} shift, better drive current, subthreshold swing and hole mobility is obtained after FGA, while series resistance is increased after FGA.



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[9] P. Tsipas and A. Dimoulas, "Modeling of negatively charged states at the Ge surface and interfaces," Appl. Phys. Lett., vol. 94, pp. 012 114, 2009.

- Cyclic DHF clean of Ge
- 4200 Å SiO_2 isolation layer
- 1st litho. and B/P imp. (20keV, 1E15cm^{-2})
- Dopant activation (500°C 10s, 600°C 10s)
- 2nd litho. : define AA
- 10 cycles ALD Al_2O_3
- PDO 520°C 3min GeO_x passivation
- 50 cycles ALD HfO_2
- PDA 500°C 60sec N_2
- 3rd litho. : define contact hole
- Al deposition
- 4th litho. : define metal pad
- Backside contact (Al)
- FGA (300°C 30min)

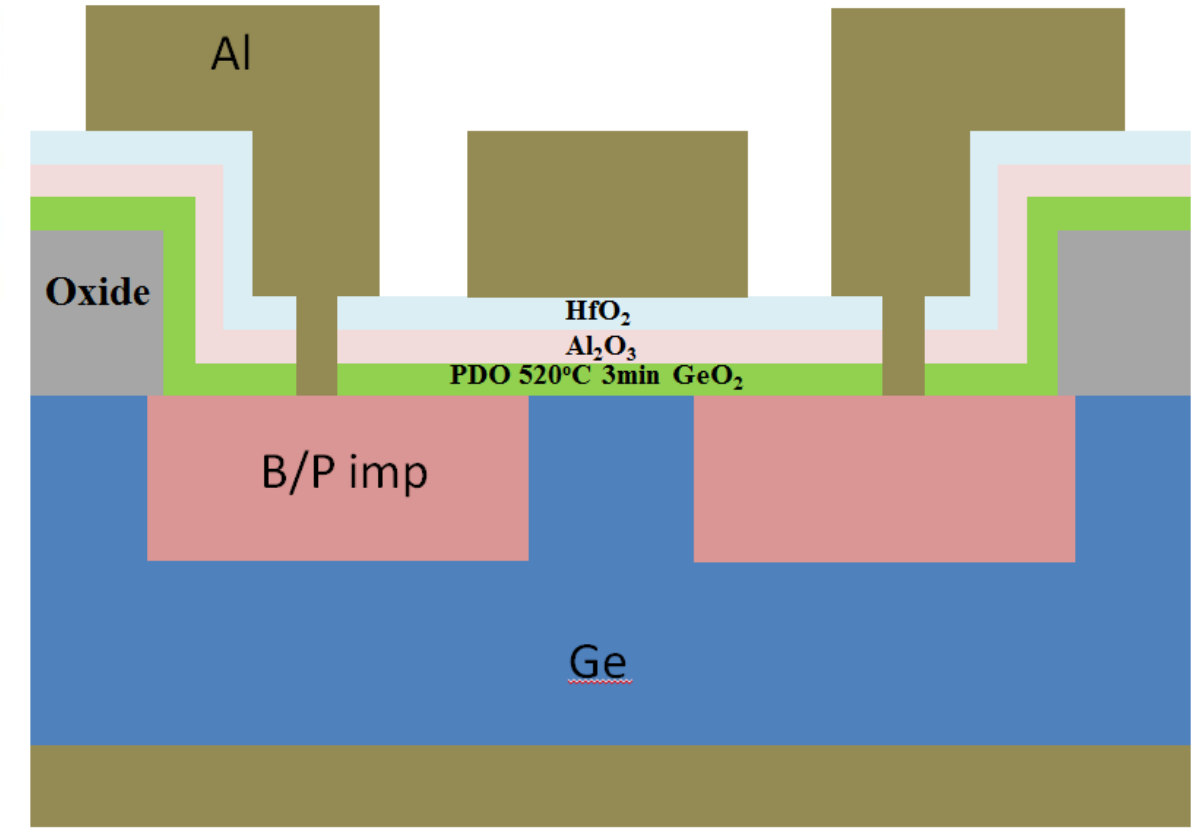
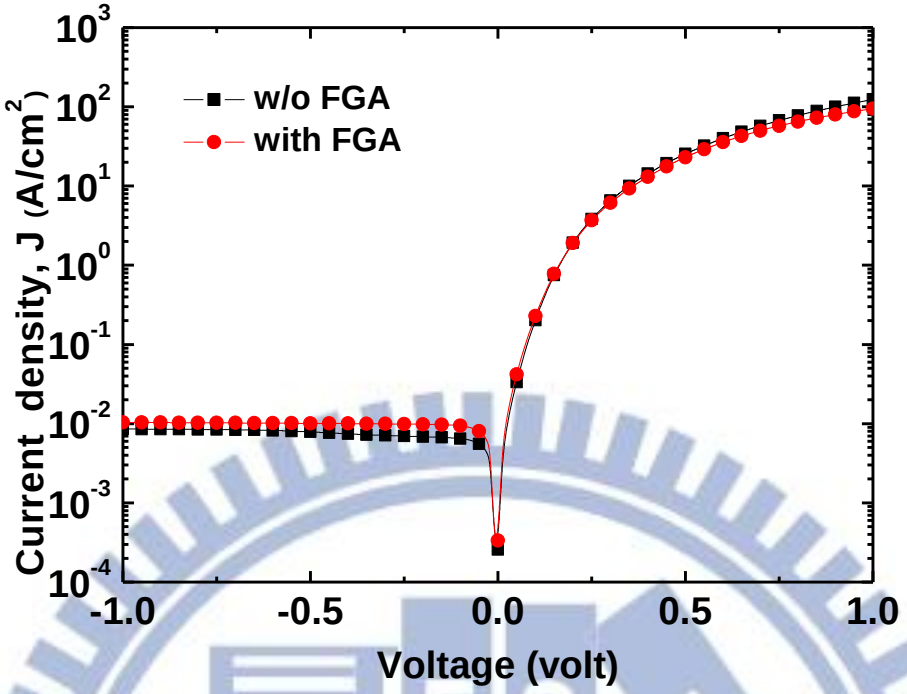
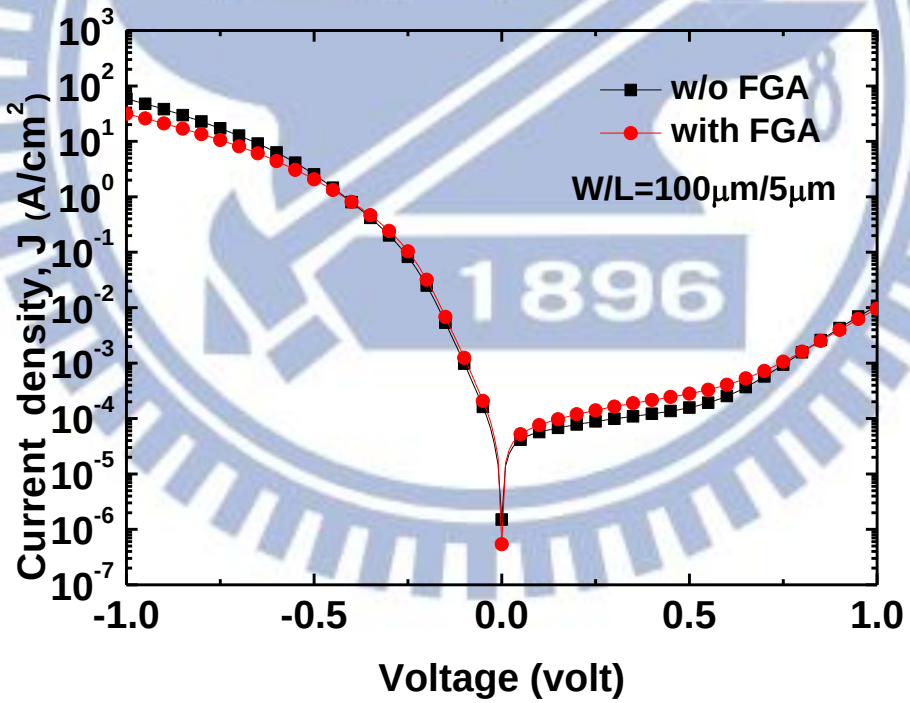


Fig. 0.1 The process flow and device structure of Ge MOSFET



(a)



(b)

Fig. 0.2 I–V characteristics of p^+n and n^+p junctions, before and after performing FGA. (a) p^+n junction (b) n^+p junction

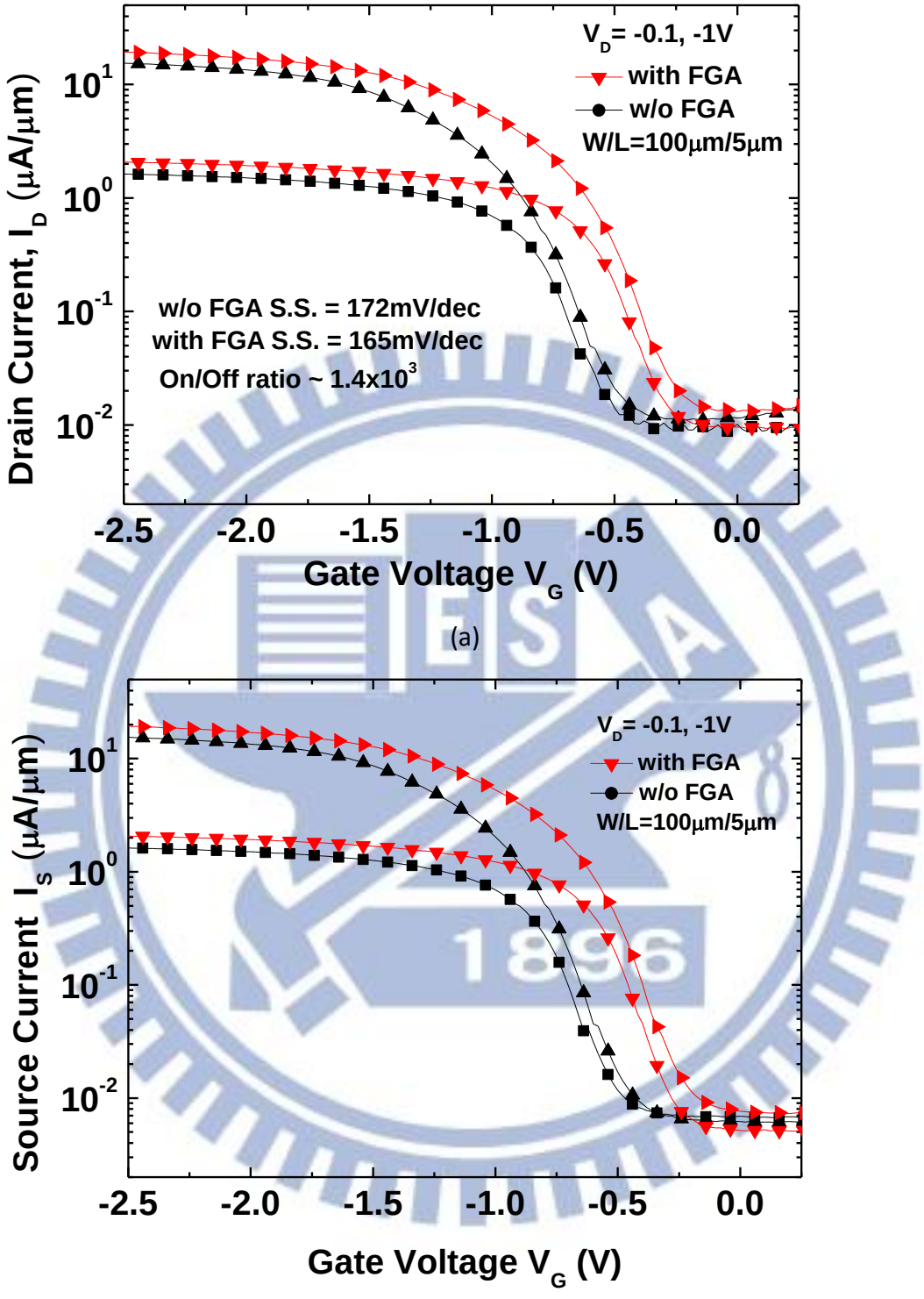
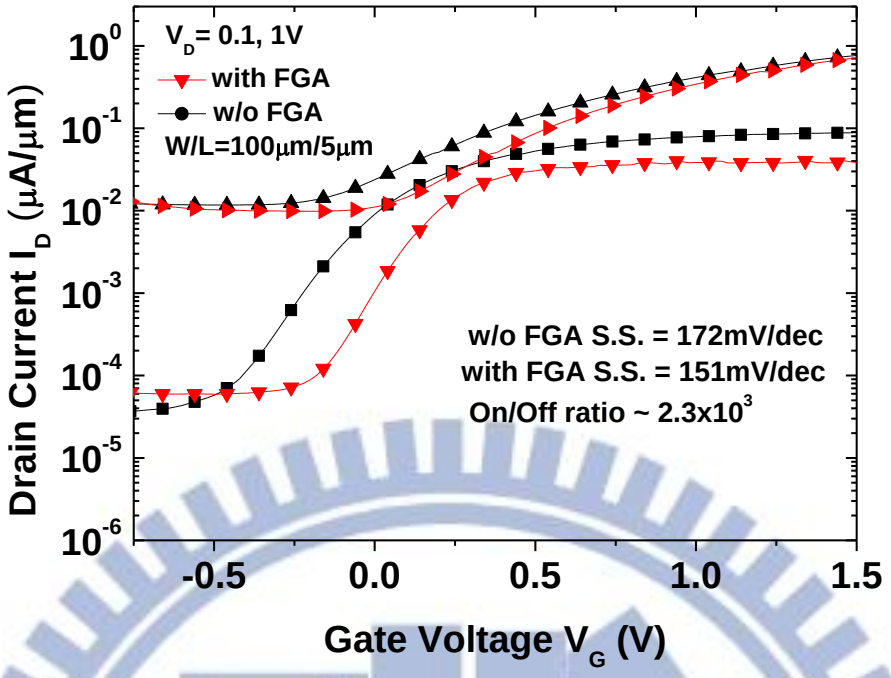
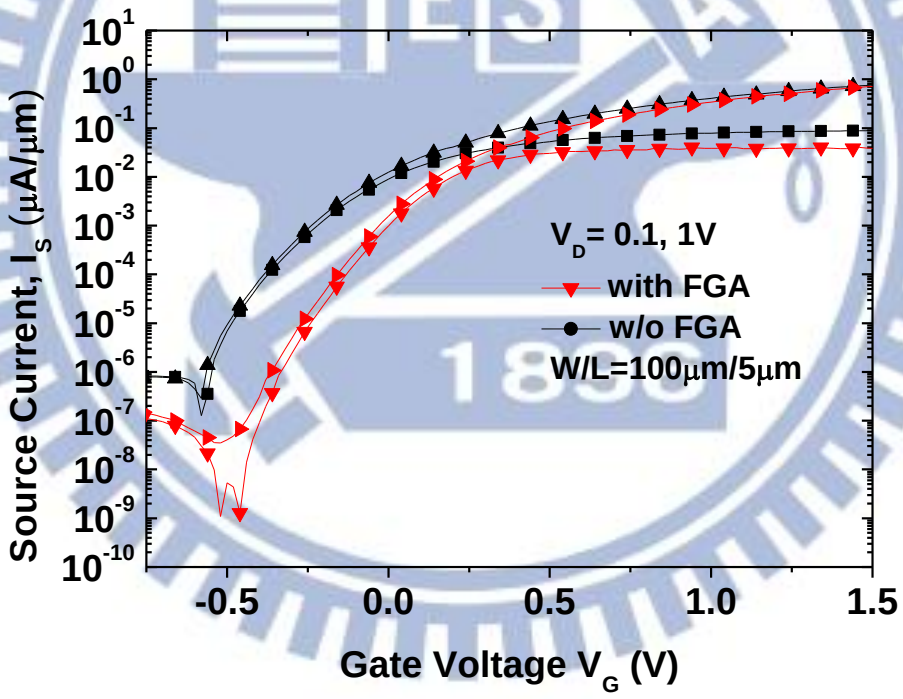


Fig. 0.3 Effects of FGA at 300 °C on the PMOSFET. (a) I_D-V_G characteristic. (b) I_S-V_G characteristic.

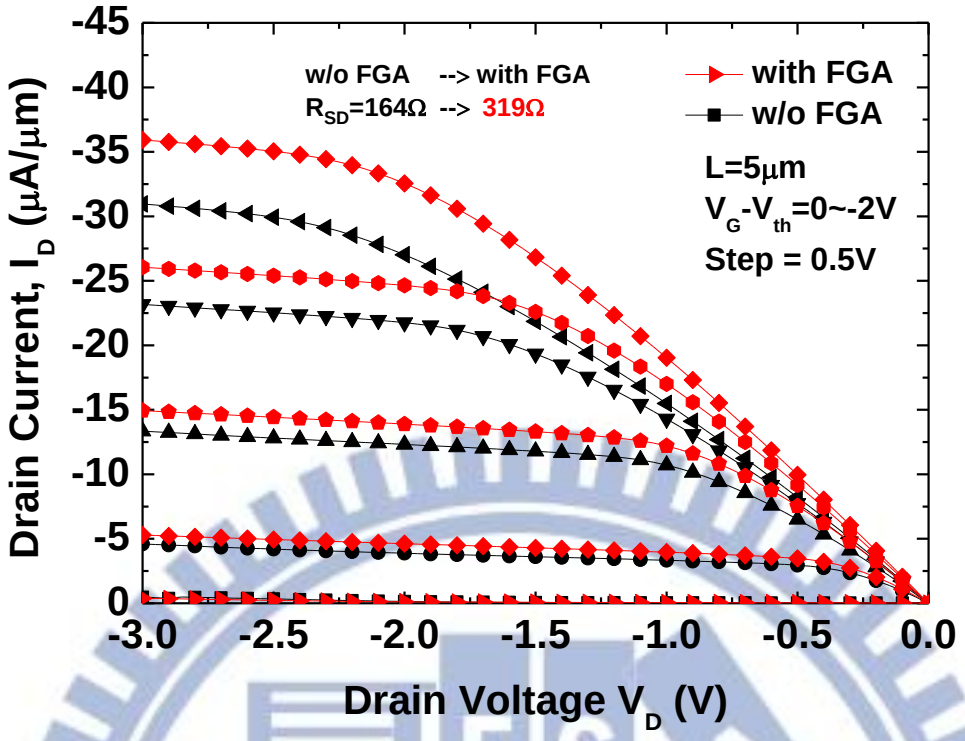


(a)

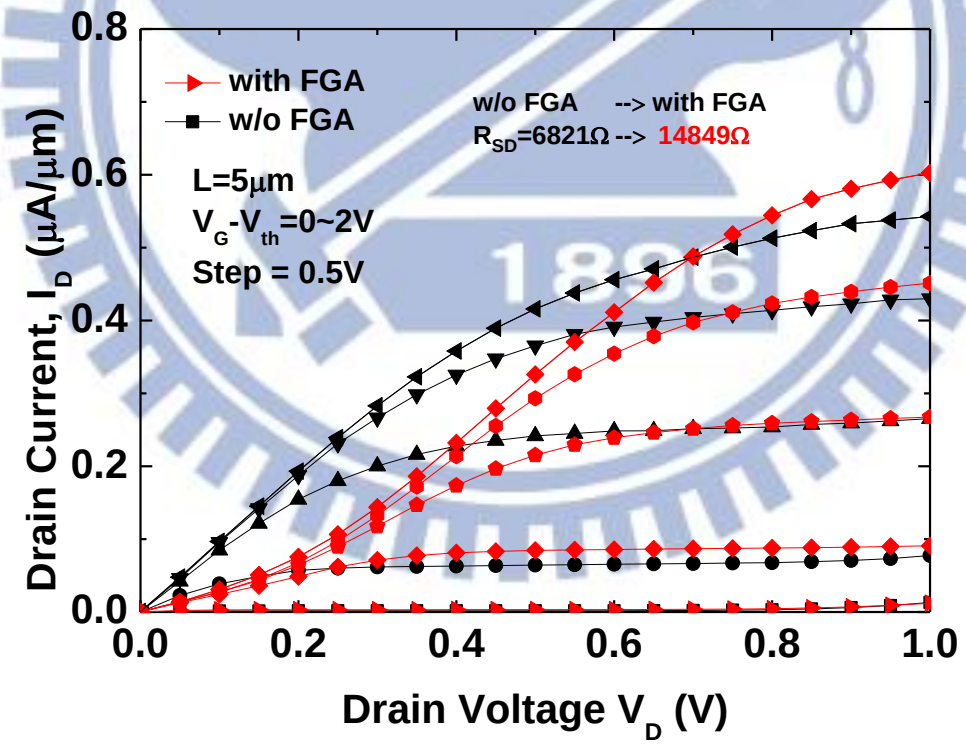


(b)

Fig. 0.4 Effects of FGA at 300 °C on the NMOSFET. (a) I_D-V_G characteristic. (b) I_S-V_G characteristic.



(a)



(b)

Fig. 0.5 Effects of FGA at 300 °C on the I_D-V_G characteristics (a) PMOSFET. (b) NMOSFET.

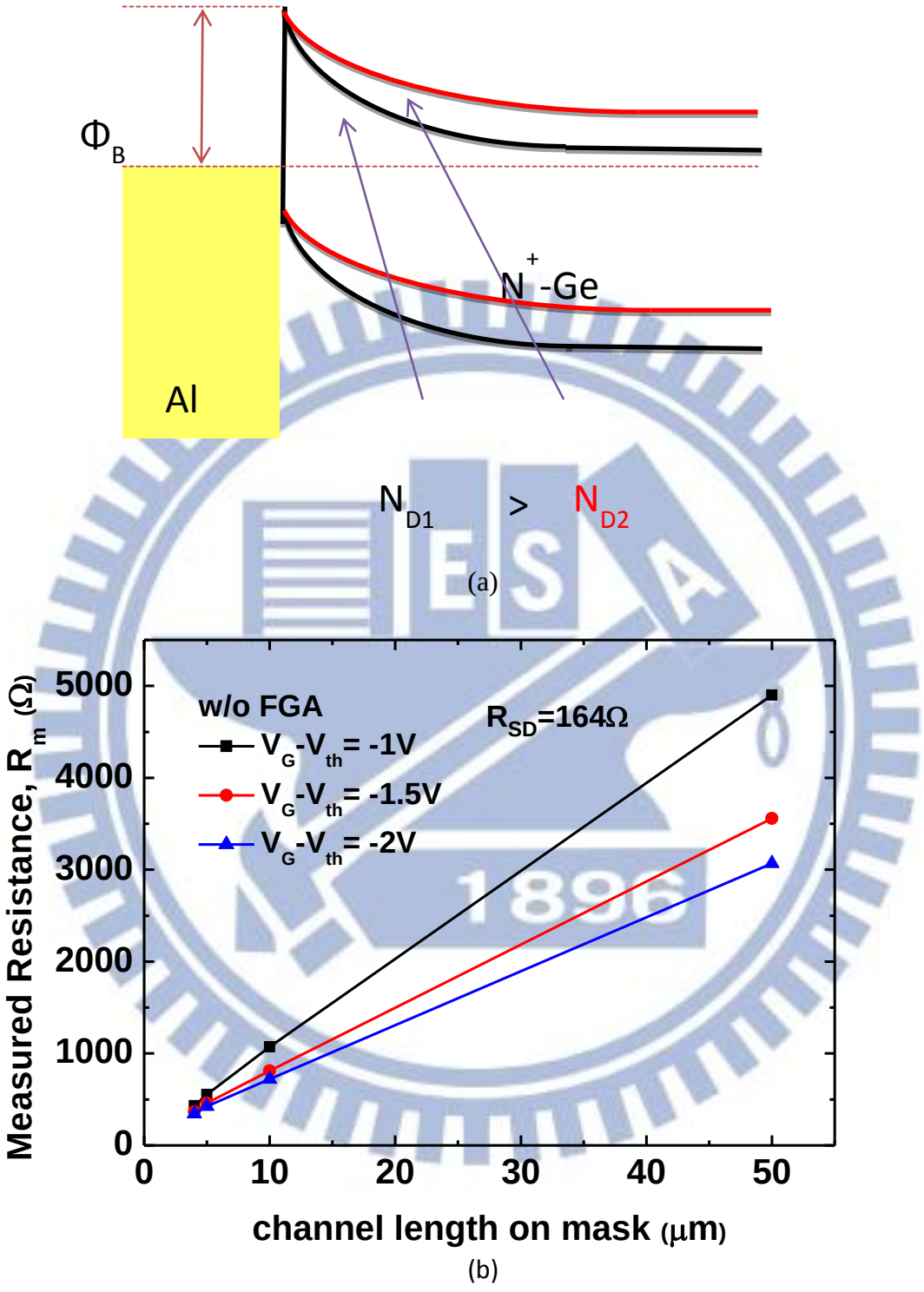
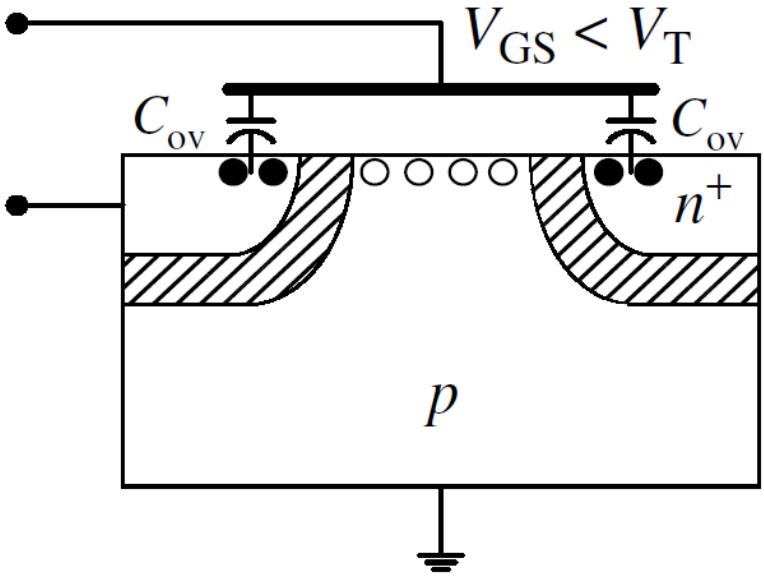
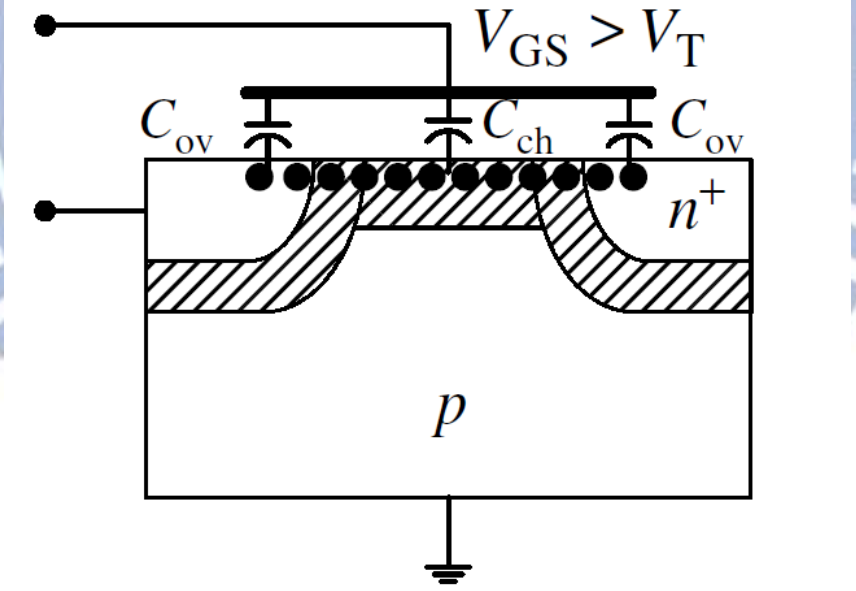


Fig. 0.6 (a)The schottky junction tunneling. (b)Series resistance from Terada and Muta method.

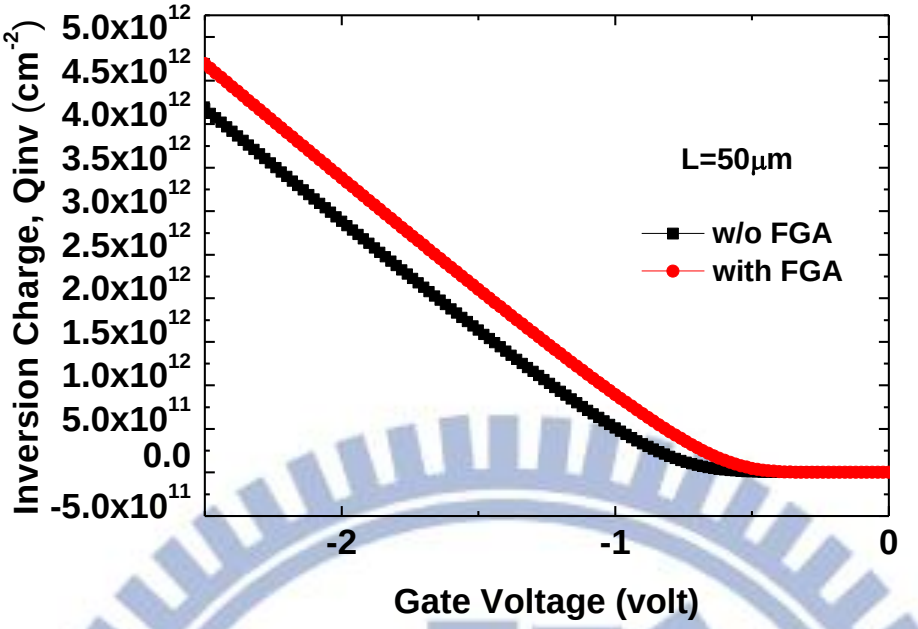


(a)

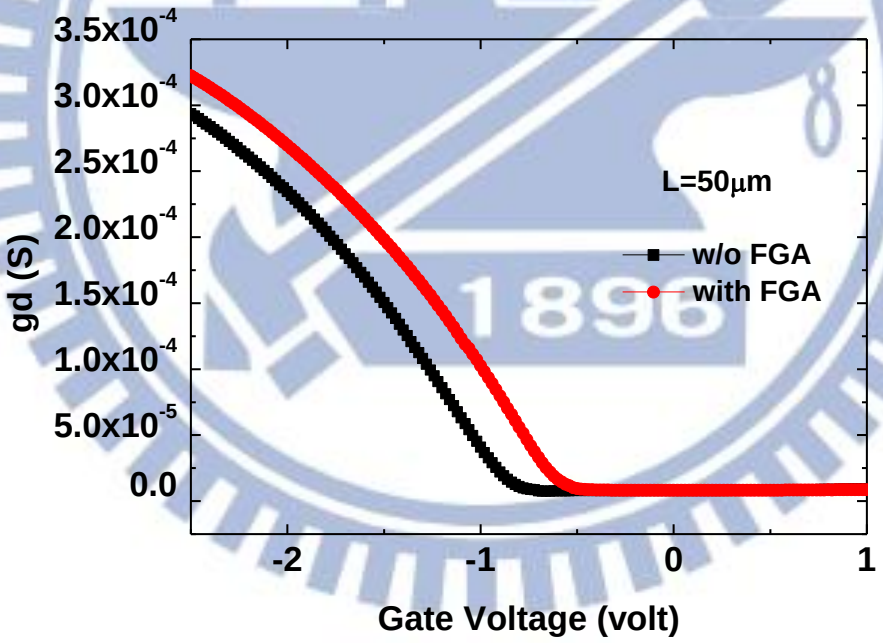


(b)

Fig. 0.7 Schematic for gate-to-channel capacitance measurements for (a) $V_{GS} < V_T$, (b) $V_{GS} > V_T$



(a)



(b)

Fig. 0.8 Effects of FGA at 300 °C on (a) Q_{inv} versus V_G plot and (b) g_d versus V_G plot.

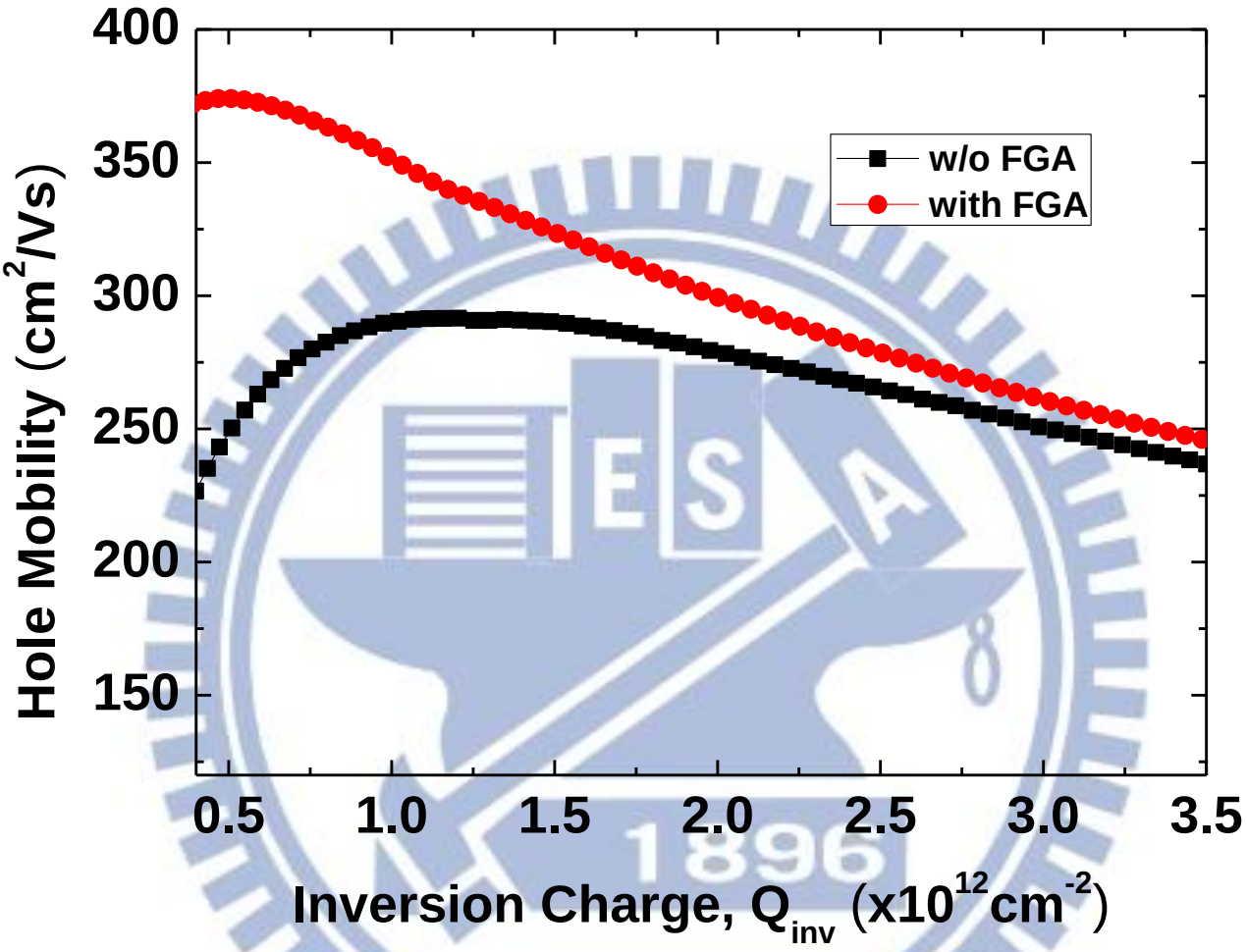
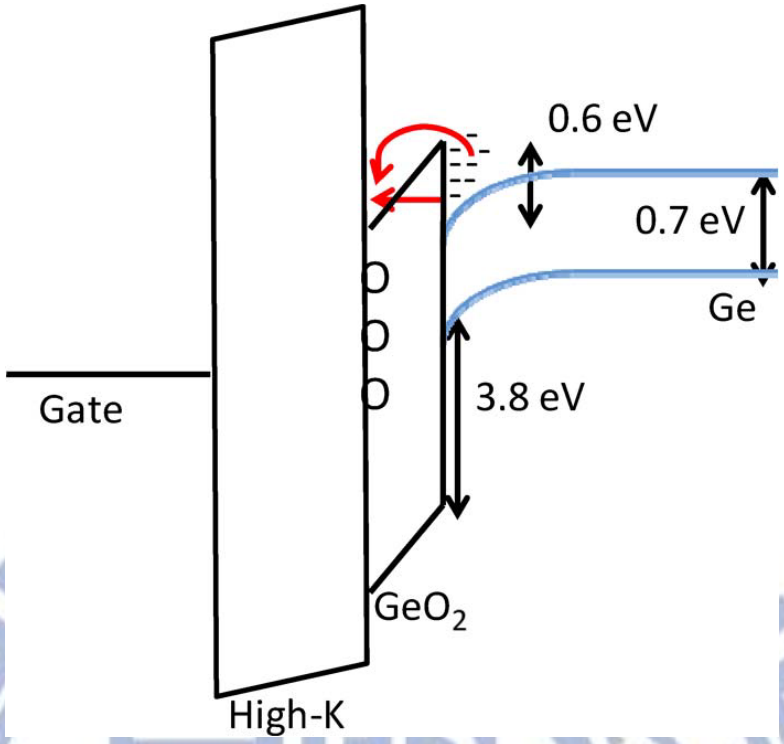
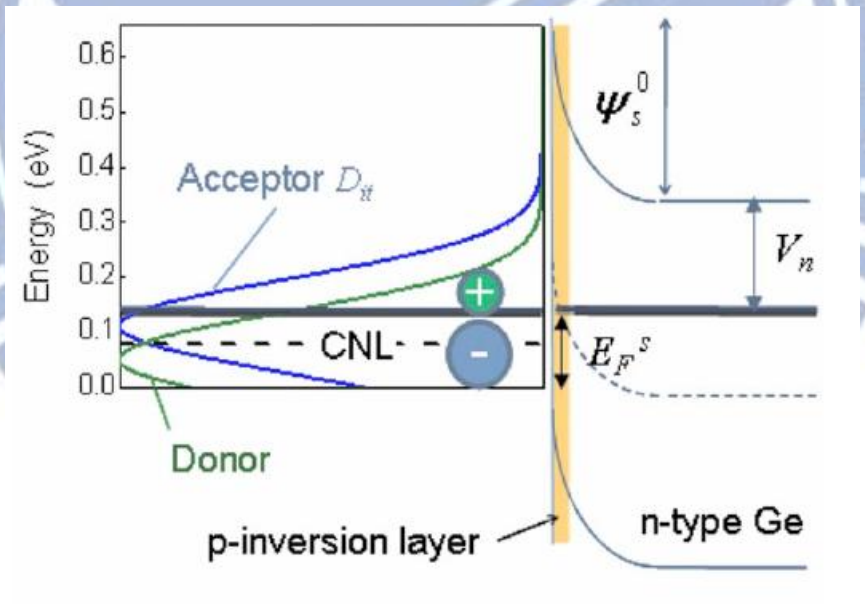


Fig. 0.9 Effective mobility versus inversion charge is plotted with and without FGA at 300 °C.



(a)



(b)

Fig. 0.10 (a) Schematics of the effect of the low conductance-band offset on the electron trapping by the slow traps and the bulk traps in the NMOS inversion regime. (b) D_{it} energy distribution of acceptor and donor DB surface states and surface band diagram of n-Ge.

Chapter 4

Epi-Ge on SOI MOSFET with Atomic-Layer-Deposited $HfO_2/Al_2O_3/GeO_x/Ge$ Gate Stack Fabricated by Post Deposition Oxidation

4.1 Introduction

Silicon-on-insulator (SOI), means place a thin layer of silicon on top of the insulator such as SiO_2. SOI CMOS process can be readily developed due to the compatibility with established bulk processing technology. The main advantage of SOI devices over bulk CMOS is the very low junction capacitance, the source and drain junction capacitance is almost entirely eliminated in SOI MOSFETs, hence SOI devices have faster switching speed which improve devices performance. When the silicon film is thicker than the maximum gate depletion width, it's called partially depleted SOI (PDSOI), the floating body effect in PDSOI reduced threshold voltage at high drain voltage [1]. When the silicon film is thin enough that the entire film is depleted before the threshold condition is reached, it's called fully depleted SOI (FDSOI). Floating body effect can be largely avoided in FDSOI devices, and the sub threshold slope of FDSOI MOSFETs can be near the ideal 60mV per decade at 300K.

For the small bandgap material Ge, the Ge MOSFET junction leakage is a real concern, thin body Ge-on-insulator (GOI) is one of the solution. The advantages of thin body GOI are low parasitic capacitance, immunity for short channel effects, and low junction leakage current [2].

In this chapter, both germanium NMOSFET and PMOSFET were fabricated on epitaxial Ge on thin SOI substrates with two different structures, respectively. Effect of forming gas annealing (FGA) on device characteristics is discussed, including series resistance, subthreshold swing and mobility.

4.2 Fabrication of Gate-Last Epi-Ge on SOI MOSFET

High resistivity SOI substrate (10-20 ohm-cm) with 50nm device layer was used in this work. The device layer was trimmed down to 20nm and 30nm by growing and etching thermal wet oxide. After standard cleaning and dilute HF dipping, trimmed SOI substrate was introduced to UHVCVD chamber and baked at 900℃ for 10 minutes. Next, 60nm and 30nm Ge layer was grown at 420℃ and PDA was carried out at 900℃ for 10 minutes in high-vacuum ambient..

Fig. 4.1 shows the X-ray diffraction (XRD) data for epitaxial Ge on SOI substrates. XRD peak is greater for epi-60nm Ge film, indicating higher quality and lesser the dislocation density.

Fig. 4.2 shows TEM images of epi-60nm Ge on SOI. Lower dislocation density with smooth surface is observed. And **Fig. 4.3** shows TEM image of epi-30nm Ge on SOI. High dislocation density exists in Ge film accompanying with high roughness**.** Since stress in thicker film is greater than that in thin film; higher stress enhances

dislocation movement during thermal annealing can be expected. Therefore, threading dislocations are moved and annihilated by PDA**.**

Fig. 4.4 shows two different epi-Ge on SOI substrate structures that we used, both structures were used for Ge PMOSFET and Ge NMOSFET fabrication. All of the samples were pre-cleaned by successive diluted HF (20:1) and DI water rinsing to remove the native oxide, then a 420-nm-thick SiO_2 layer was capped for the field oxide by PECVD.

First, the source/drain region was opened through the first mask, followed by implantation of the Boron (1×10^{15} cm^{-2}, 20 keV) into the n-Ge and Phosphorous (1×10^{15} cm^{-2}, 20 keV) into the P-Ge, with dopant activation condition 500℃ 10 second and 600℃ 10 second, respectively. Next, active area (AA) was opened through the second mask, after that, an 10 cycles ALD-Al_2O_3 thin film grown on each sample at 250℃, a thin GeO_x layer being formed by post deposition oxidation to passivate the Ge surface, with oxidation condition 520℃ 3min. A 50 cycles HfO_2 layer was deposited by ALD at 250℃, post deposition annealing was performed at 500℃ 60sec with N_2. Right after dry etching the contact hole on S/D region through the third mask, a 400nm Al metallization was performed which was then patterned to define metal pads through the fourth mask.

Forming gas annealing (FGA, 300℃, 30 min, H_2/N_2=5%) was performed to investigate the effect of FGA on electrical characteristics.

The process flow and device structure are shown in **Fig. 4.5.**

4.3 Effect of FGA on Epi-Ge on SOI MOSFET Electrical Characteristics

The effects of FGA at 300 ^{o}C on the PMOSFETs with epi-60nm Ge on SOI and epi-30nm Ge on SOI are shown in **Fig. 4.6**, where the I_D-V_G and I_S-V_G plots are displayed. For both epi-60nm Ge on SOI and epi-30nm Ge on SOI, the better subthreshold swing and positive Vth shift after FGA are observed. We believe that the better subthreshold swing is due to the improved high-k/Ge interfaces, the lower D_{it} caused the smaller subthreshold swing, and the positive Vth shift is because forming gas annealing lowering both fix charge and oxide trap charge. The higher on currents are observed for both samples after FGA, which may due to the less coulomb scattering. The I_D-V_G and I_S-V_G plots have same off current, which means that epi-Ge on SOI has no substrate leakage. The lower off current after FGA is observed, it is because of the effective reduction of defects such as the bulk defects in epi-Ge on SOI substrate.

Fig. 4.7 shows the effects of FGA at 300 ^{o}C on the I_D-V_G characteristics of PMOSFETs for both epi-60nm Ge on SOI and epi-30nm Ge on SOI. Both of them have larger drive current after FGA, which exhibit higher performance. Series resistance is increased after FGA, we think it due to the more dopant diffusion and thus lower source/drain doping concentration.

Effective hole mobility versus inversion charge is plotted in **Fig. 4.8,** with and without FGA at 300 ^{o}C. The higher effective hole mobility is observed after FGA, which may due to the better interface quality and less coulomb scattering.

The effects of FGA at 300 ^{o}C on the NMOSFETs with epi-60nm Ge on SOI and epi-30nm Ge on SOI are shown in **Fig. 4.9**, where the I_D-V_G and I_S-V_G plots are displayed. As the result in PMOSFETs, both epi-60nm Ge on SOI and epi-30nm Ge on SOI have better subthreshold swing, higher on currents, positive V_{th} shift and lower off current after FGA. The NMOSFET has lower drive current after FGA at small drain voltage, but the drive current will become larger when drain voltage grows higher. We think the reason of lower drive current after FGA at small drain voltage is the dopant diffusion causing lower dopant concentration, and the effective tunneling barrier becomes large, which the drain voltage need become higher to lower the effective tunneling barrier.

Fig. 4.10 shows the effects of FGA at 300 ^{o}C on the I_D-V_D characteristics of NMOSFETs for both epi-60nm Ge on SOI and epi-30nm Ge on SOI. Both of them have larger drive current after FGA as in PMOSFETs.

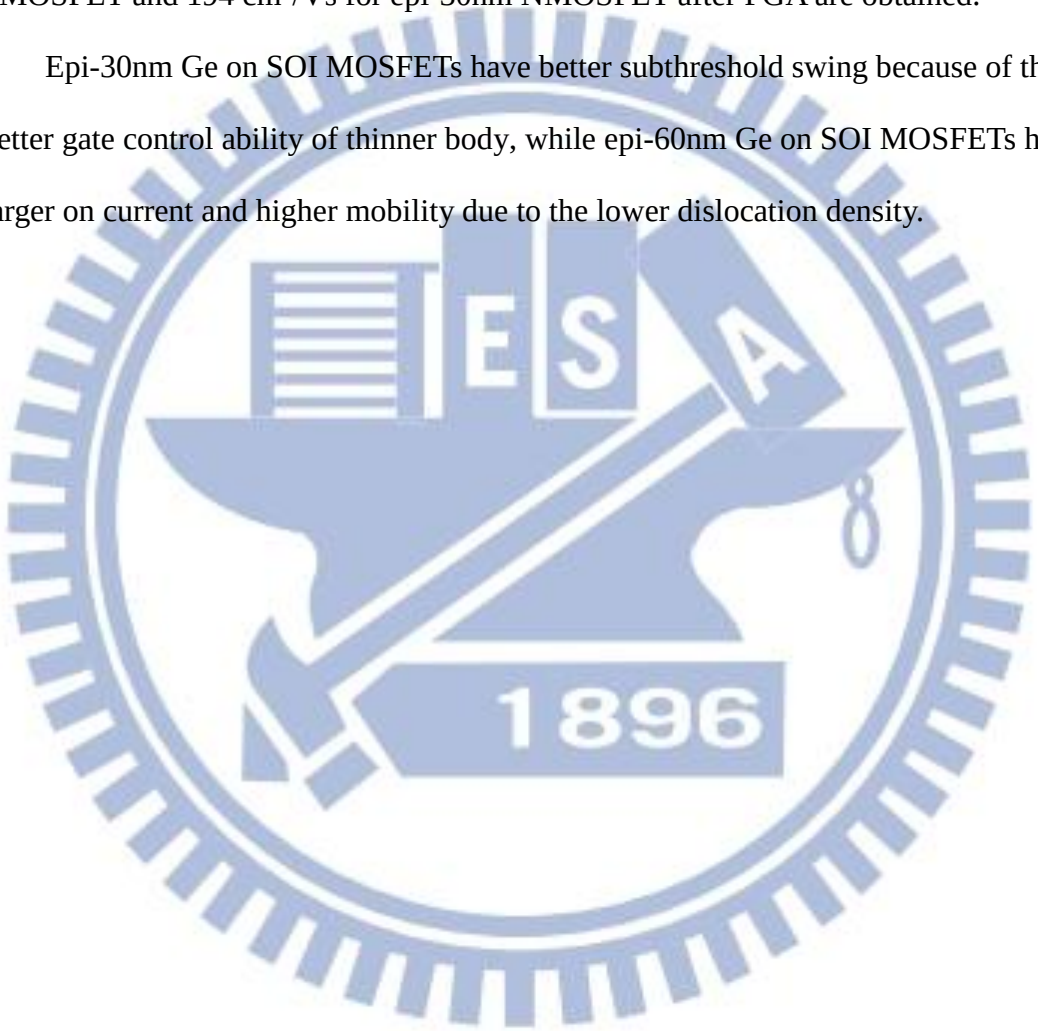
To compare the epi-60nm Ge on SOI and epi-30nm Ge on SOI MOSFETs in our experiment data, we found that epi-30nm Ge on SOI MOSFETs have better subthreshold swing because of the better gate control ability of thinner body, while epi-60nm Ge on SOI MOSFETs have larger on current and higher mobility due to the lower dislocation density.

4.4 Conclusions

In Chapter 4, we investigated the effect of FGA on epi-Ge on SOI MOSFETs characteristics. The positive V_{th} shift, better subthreshold swing (464mV/dec for epi-60nm PMOSFET, 307mV/dec for epi-30nm PMOSFET, 256mV/dec for epi-60nm

NMOSFET and 252mV/dec for epi-30nm NMOSFET) are obtained after FGA. The on/off ratio is about 7.2×10^{1} for epi-60nm PMOSFET, 3.3×10^{2} for epi-30nm PMOSFET, 3.4×10^{2} for epi-60nm NMOSFET and 3.7×10^{2} for epi-30nm NMOSFET. For both PMOSFETs and NMOSFETs, R_{SD} is increased after FGA, The higher hole mobility is observed after FGA, a peak hole mobility of 313 cm^2/Vs for epi-60nm PMOSFET and 194 cm^2/Vs for epi-30nm NMOSFET after FGA are obtained.

Epi-30nm Ge on SOI MOSFETs have better subthreshold swing because of the better gate control ability of thinner body, while epi-60nm Ge on SOI MOSFETs have larger on current and higher mobility due to the lower dislocation density.



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[1] Y. Taur, T. H. Ning, “Fundamentals of Modern VLSI Devices, Cambridge University Press,” Cambridge, pp. 11,1998.

[2] T. Maeda, K. Ikeda, S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, and S. Takagi, “High mobility Ge-on-insulator p-channel MOSFETs using Pt germanide Schottky source/drain,” IEEE Electron Device Lett., vol. 26, pp. 102–104, 2005.

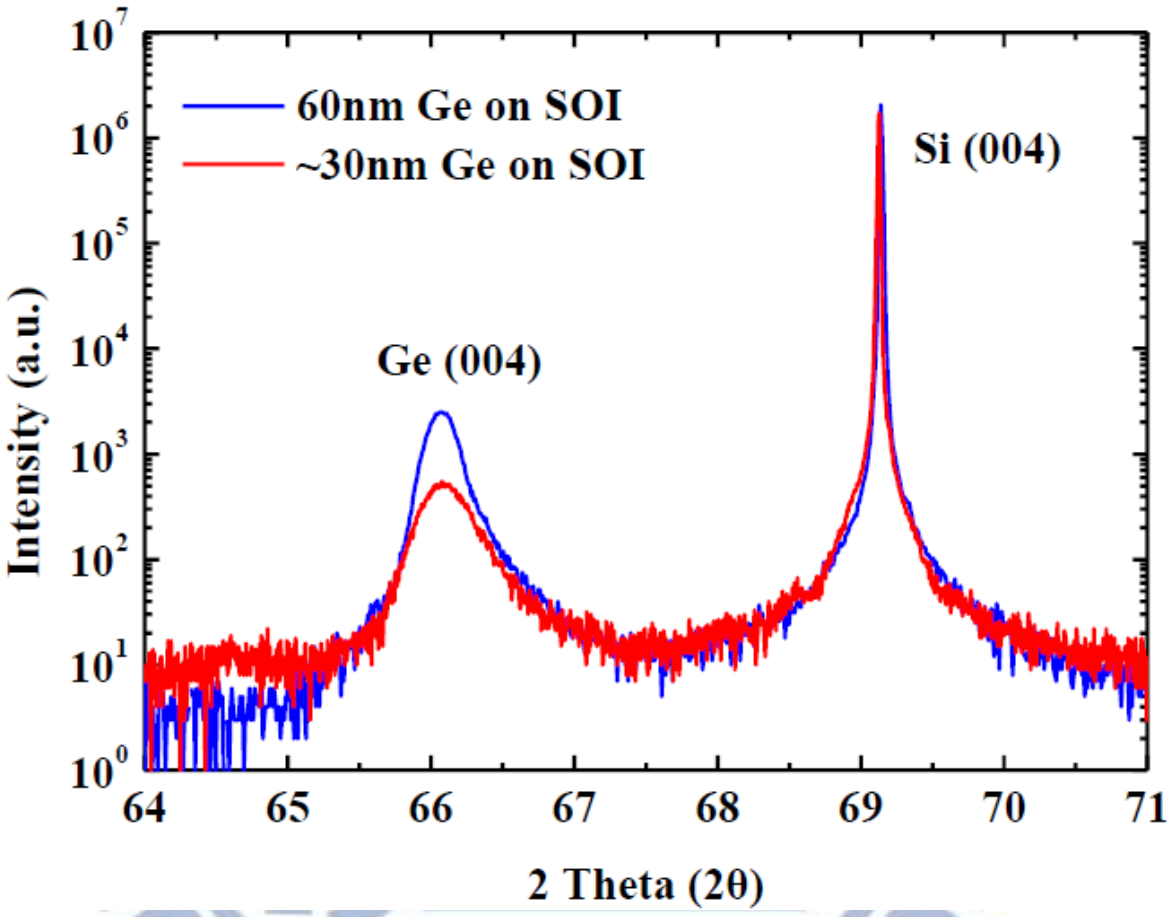


Fig. 0.1 XRD data of epitaxial Ge on SOI. Higher Ge (004) peak indicates 60nm Ge has higher quality on SOI.

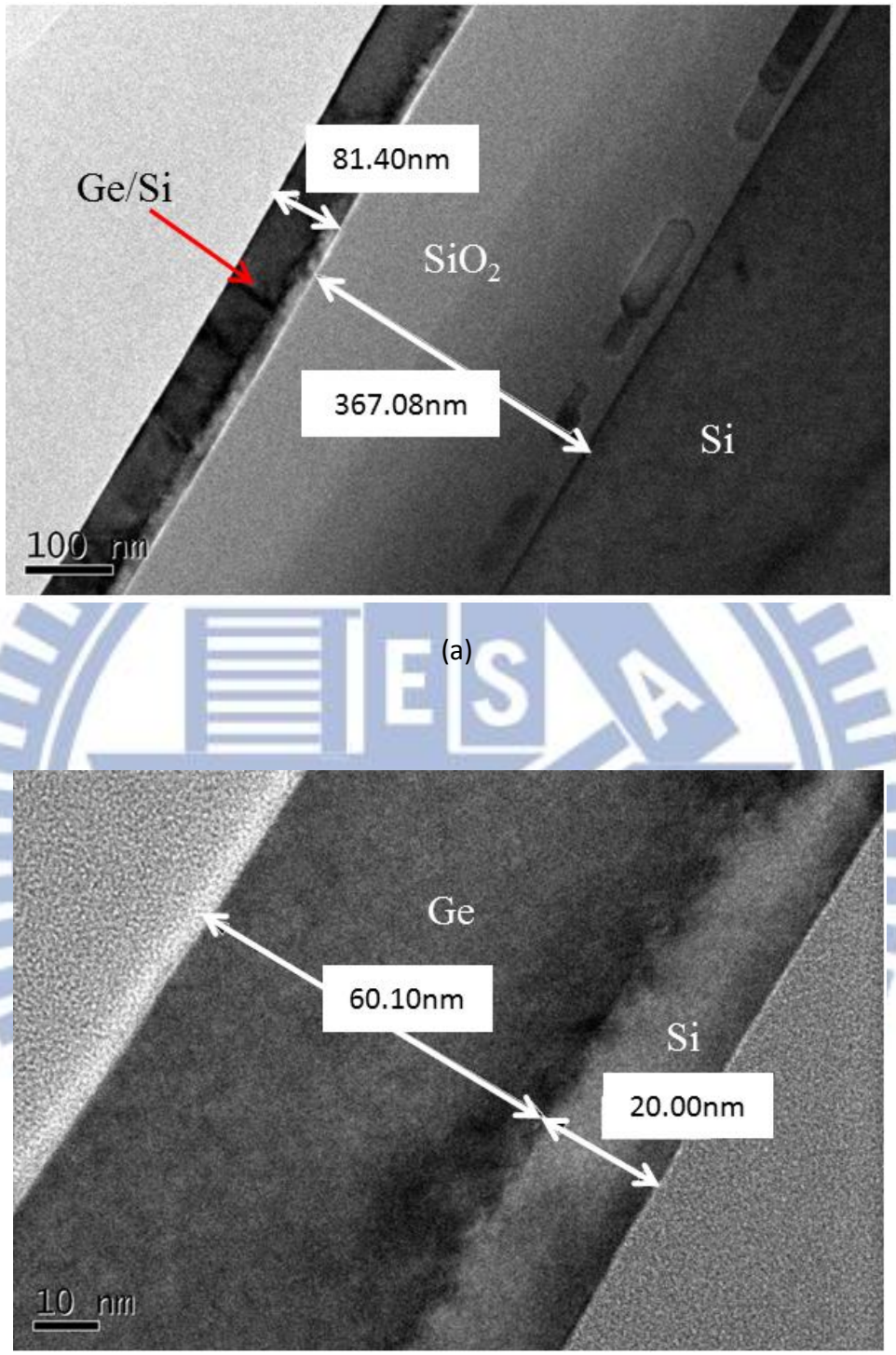
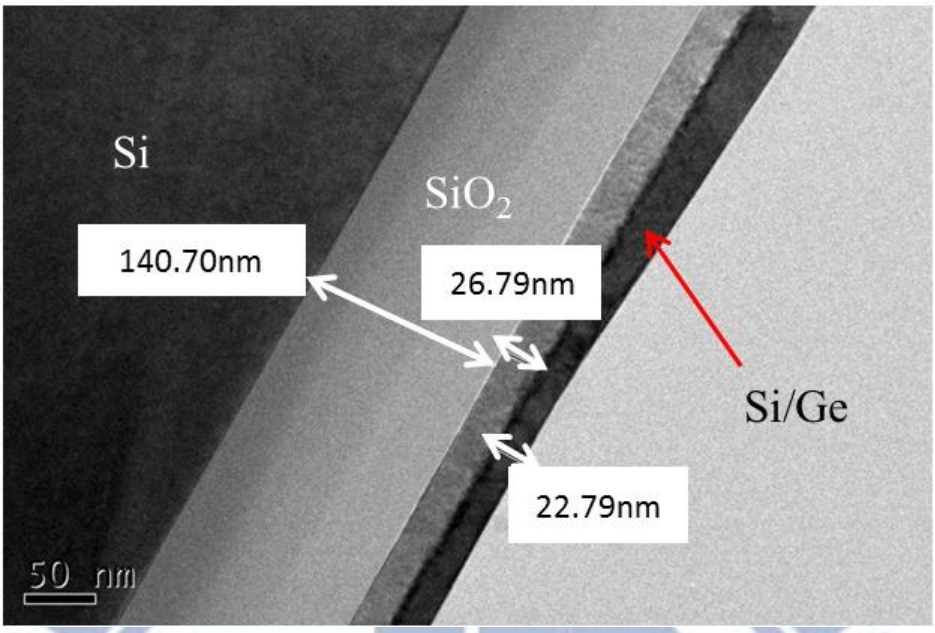
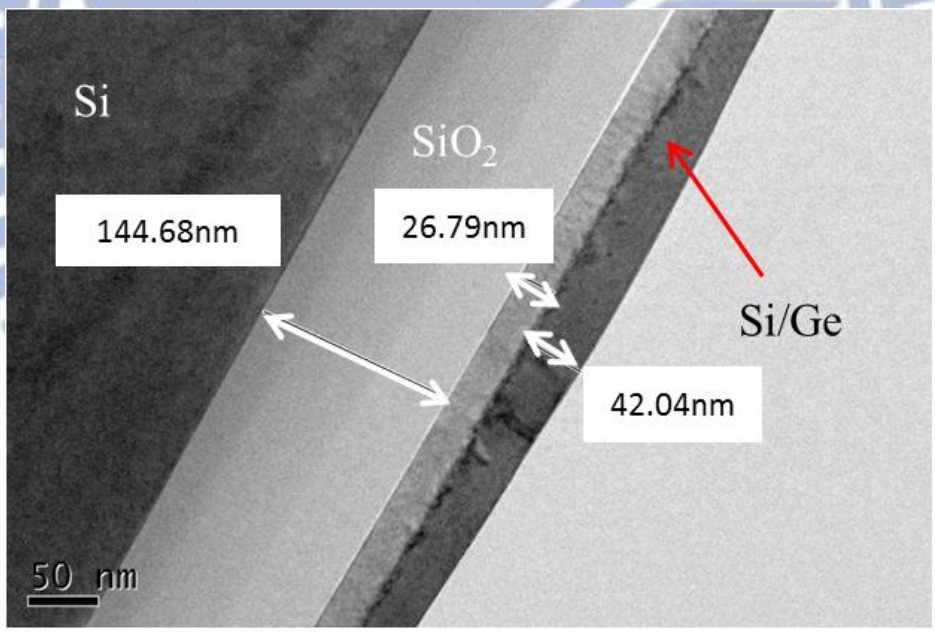


Fig. 0.2 (a) (b) TEM image of epi-60nm Ge on SOI. Lower dislocation density with smooth surface is observed.



(a)



(b)

Fig. 0.3 (a) (b) TEM image of epi-30nm Ge on SOI. High dislocation density exists in Ge film accompanying with high roughness.

(a)

(b)

Fig. 0.4 The two epi-Ge on SOI substrate structures. (a) epi-60nm Ge on SOI. (b) epi-30nm Ge on SOI.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- Cyclic DHF clean of GSOI
- 4200 Å SiO_2 isolation layer
- 1st litho. and B/P imp. (20keV, 1E15cm^{-2})
- Dopant activation (500°C 10s, 600°C 10s)
- 2nd litho. : define AA
- 10 cycles ALD Al_2O_3
- PDO 520°C 3min GeO_x passivation
- 50 cycles ALD HfO_2
- PDA 500°C 60sec N_2
- 3rd litho. : define contact hole
- Al deposition
- 4th litho. : define metal pad
- FGA (300°C 30min)

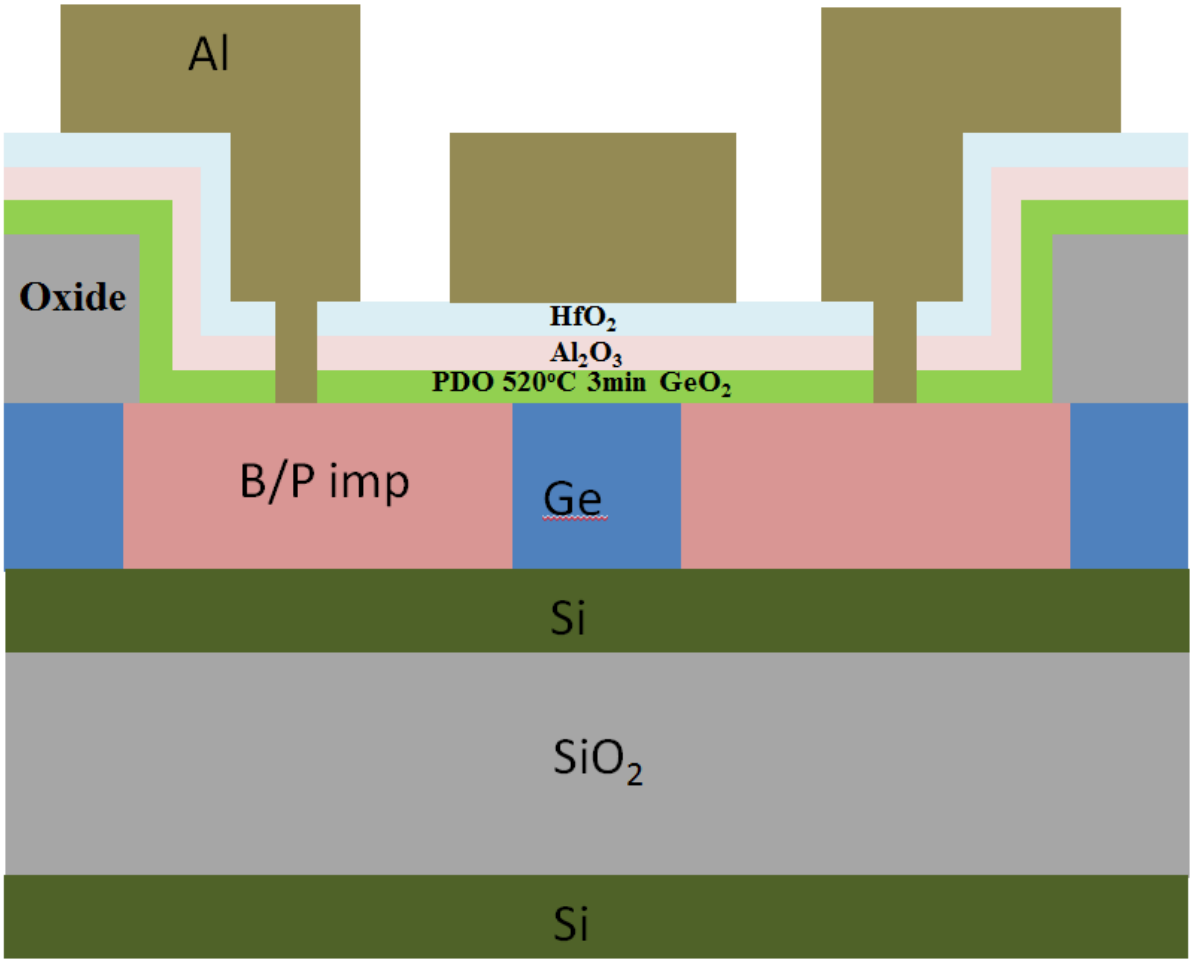


Fig. 0.5 The process flow and device structure of epi-Ge on SOI MOSFET

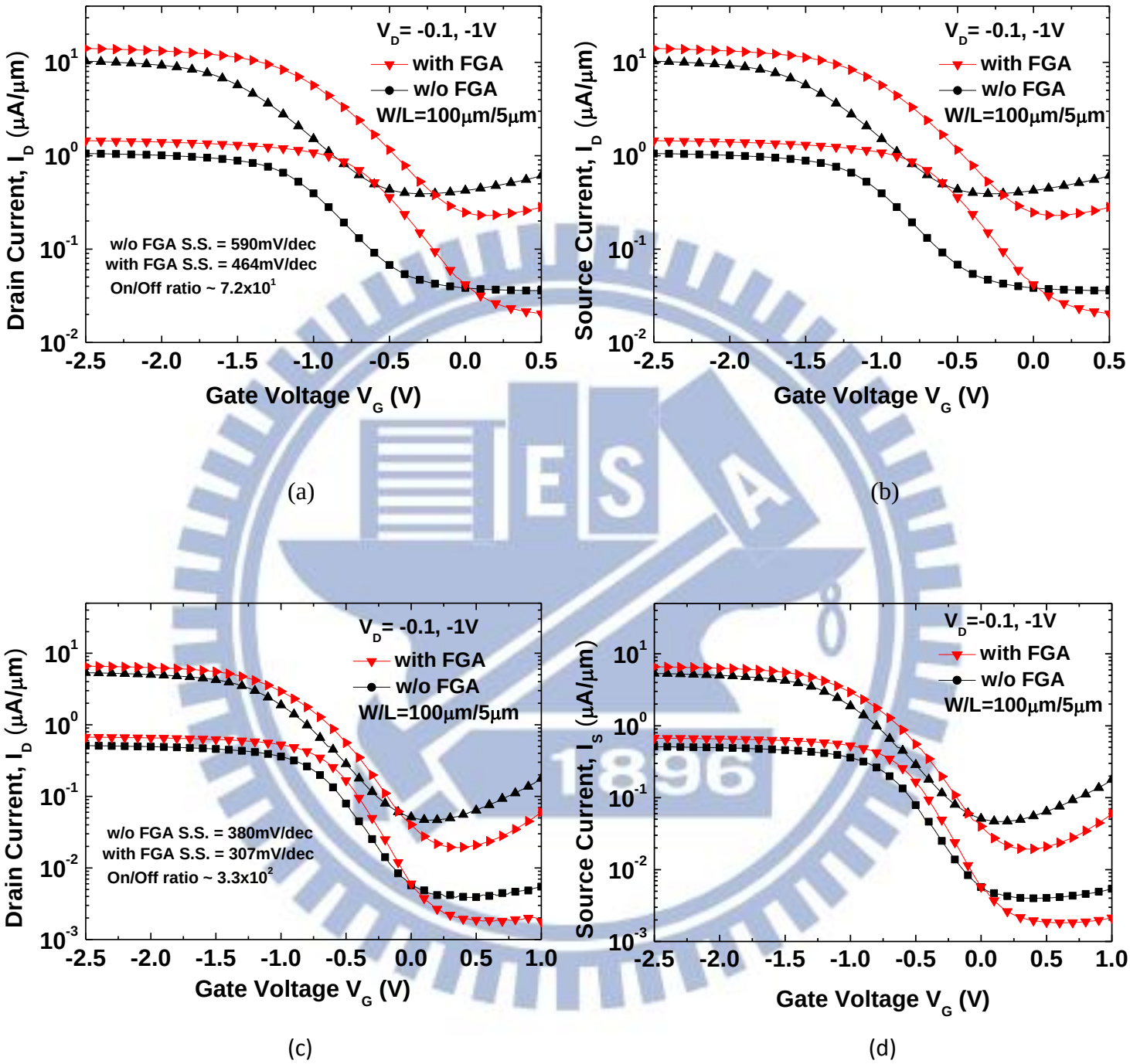
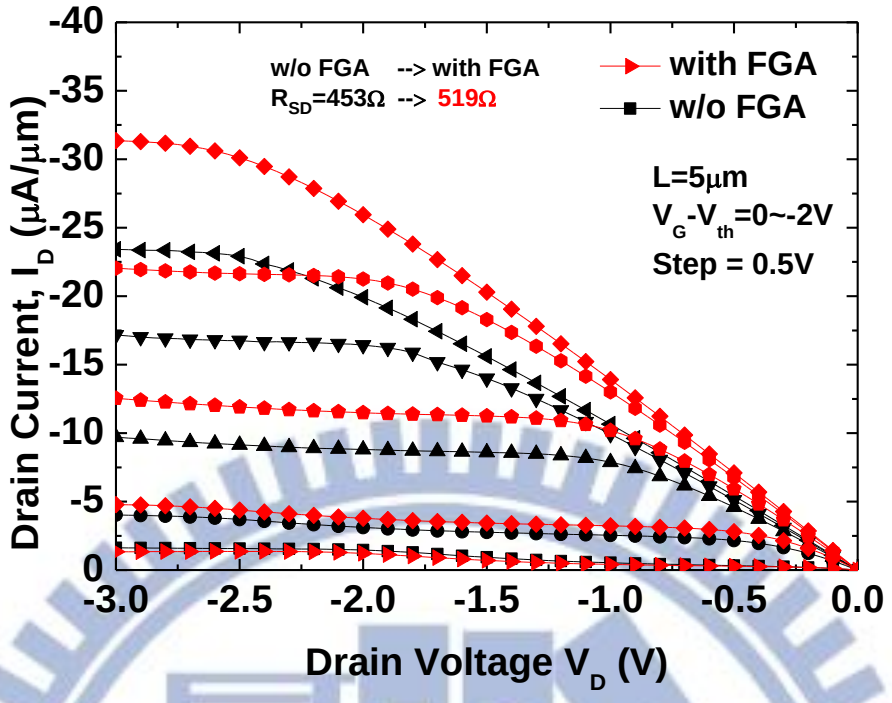
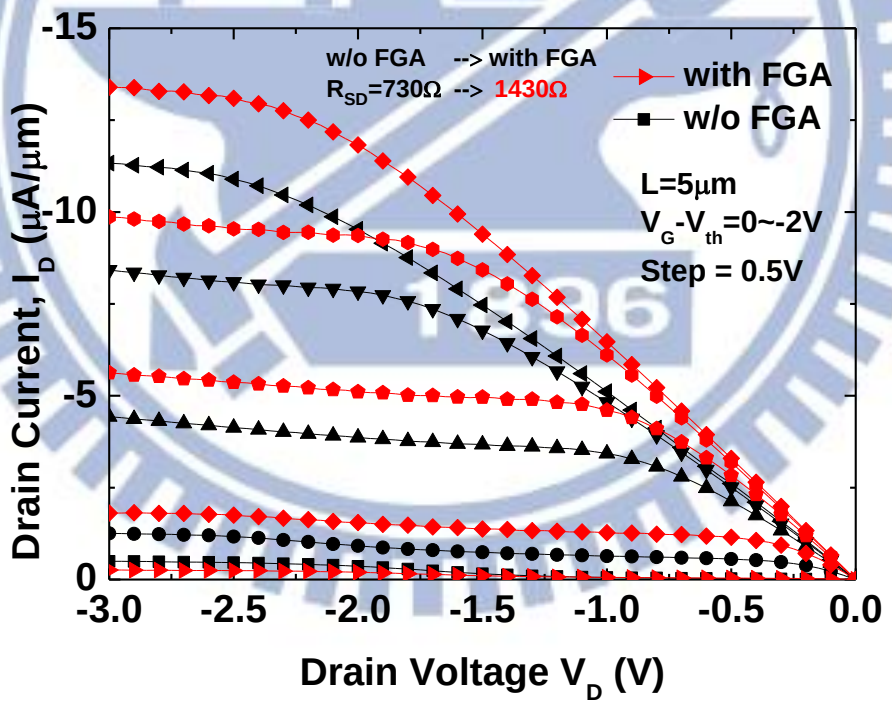


Fig. 0.6 Effects of FGA at 300 °C on the PMOSFET. (a) Epi-60nm Ge on SOI I_D-V_G characteristic. (b) Epi-60nm Ge on SOI I_S-V_G characteristic. (c) Epi-30nm Ge on SOI I_D-V_G characteristic. (d) Epi-30nm Ge on SOI I_S-V_G characteristic.



(a)



(b)

Fig. 0.7 Effects of FGA at 300 °C on the I_D-V_G characteristics of PMOSFETs (a) Epi-60nm Ge on SOI. (b) Epi-30nm Ge on SOI.

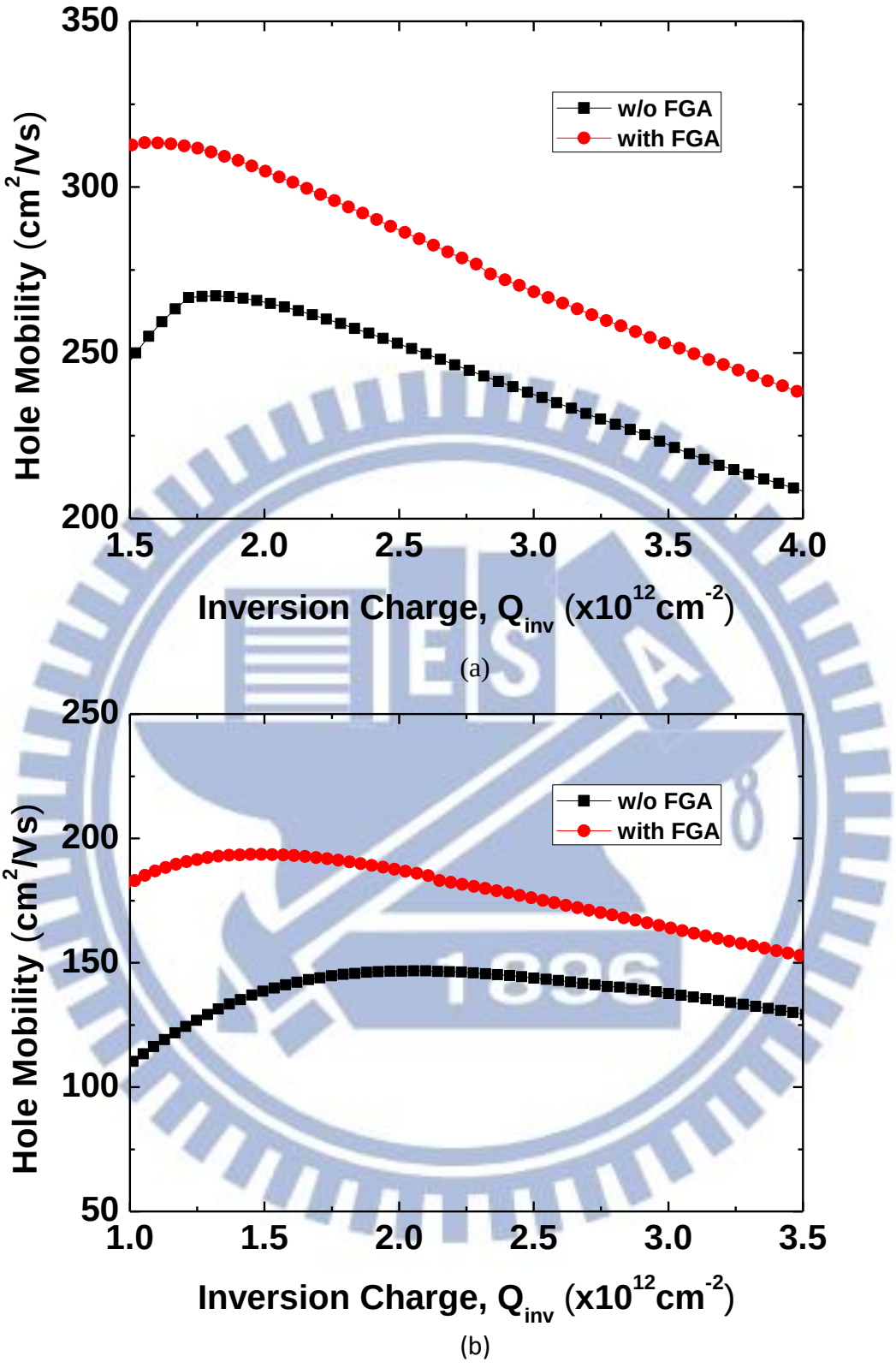


Fig. 0.8 Effective mobility versus inversion charge is plotted with and without FGA at 300 ^{o}C on PMOSFET. (a) Epi-60nm Ge on SOI. (b) Epi-30nm Ge on SOI.

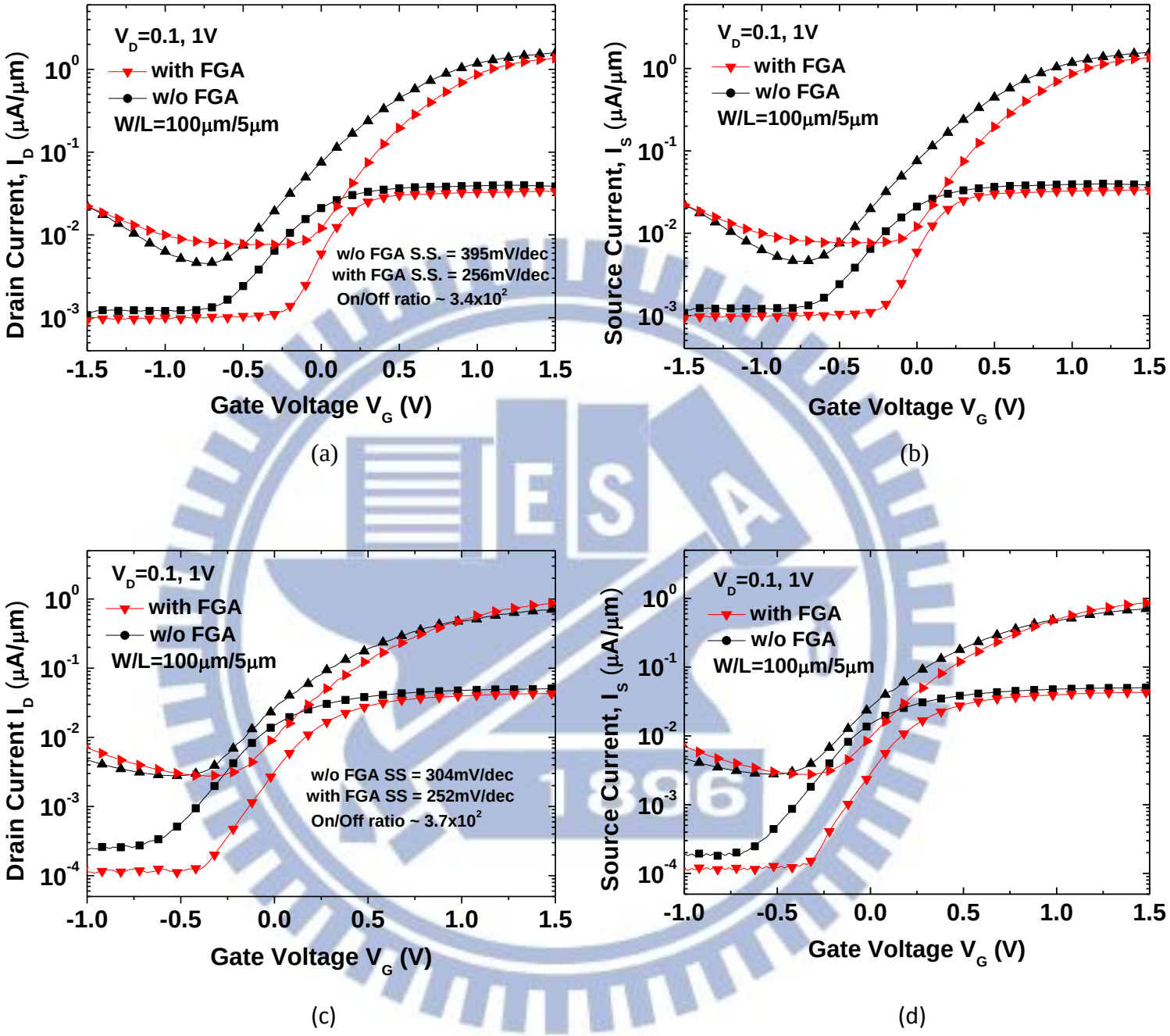
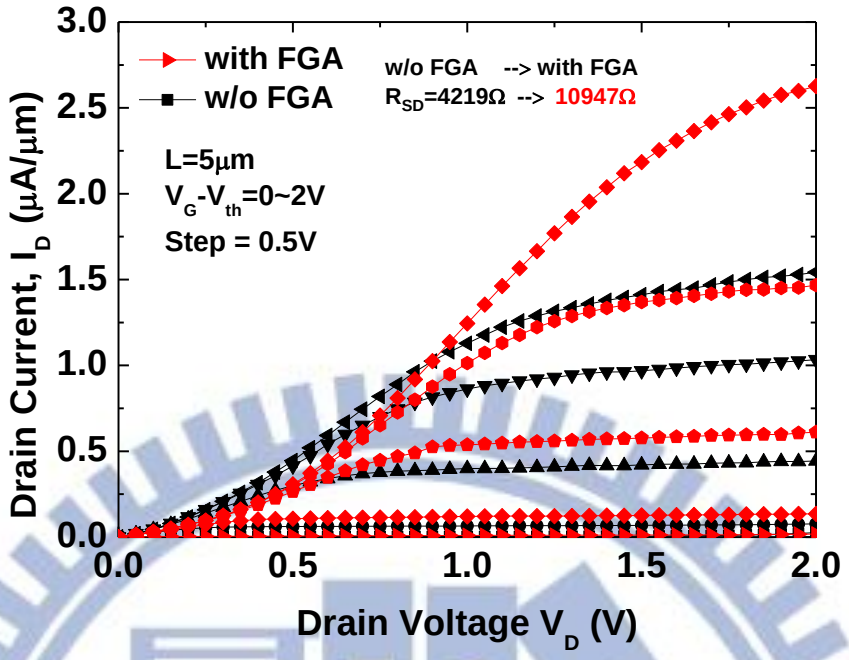
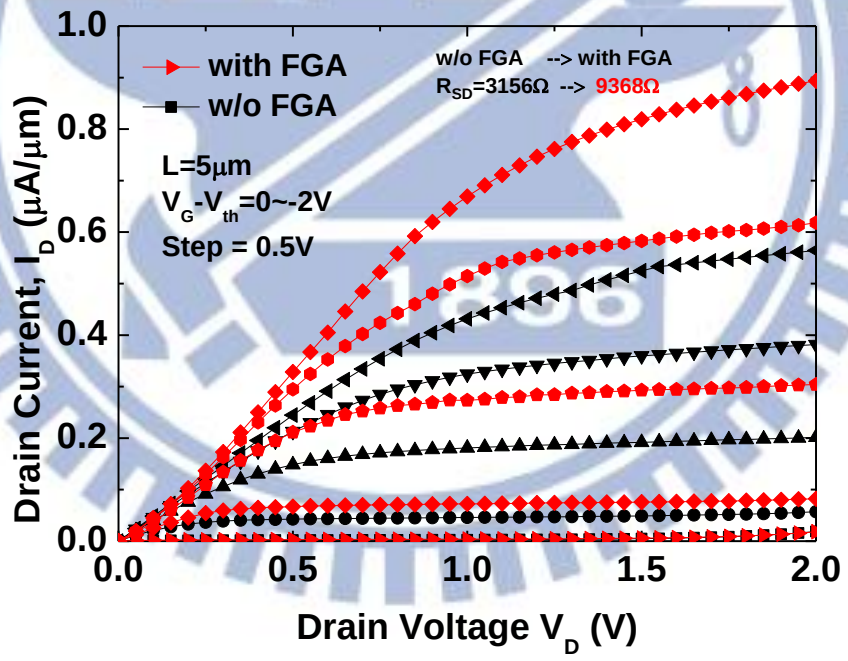


Fig. 0.9 Effects of FGA at 300 °C on the NMOSFET. (a) Epi-60nm Ge on SOI I_D-V_G characteristic. (b) Epi-60nm Ge on SOI I_S-V_G characteristic. (c) Epi-30nm Ge on SOI I_D-V_G characteristic. (d) Epi-30nm Ge on SOI I_S-V_G characteristic.



(a)



(b)

Fig. 0.10 Effects of FGA at 300 °C on the I_D-V_G characteristics of NMOSFET (a) Epi-60nm Ge on SOI. (b) Epi-30nm Ge on SOI.

Chapter 5

Conclusions

In this thesis, we had shown Ge PMOS capacitors using post deposition oxidation method to form a thin GeO_x IL by oxidizing Ge surface beneath an ALD Al_2O_3 layer using high-k RTO, the dependence of the GeO_x/Ge interface qualities on the post deposition oxidation conditions such as post deposition oxidation temperature and post deposition annealing ambient was investigated. The Ge 3*d* XPS spectra of Al_2O_3/GeO_x/p-Ge with PDO 520 ℃ 30sec, PDO 520 ℃ 3min, PDO 550 ℃ 3min and RTO thermal GeO_2 520 ℃ 30sec is shown, the increase of post deposition oxidation time or temperature will larger the Ge^{3+} peak, and the large Ge^{3+} peak could improve high-k/Ge interface, the Ge^{3+} peak shows better interface quality than Ge^{4+} peak in our studies. The EOT value was scaled down to 1.41 nm and a lower D_{it} value was obtained by PDO. The larger EOT but lower D_{it} value was obtained by using O_2 annealing. The positive V_{FB} shift and lower C-V hysteresis is shown in the samples after FGA, and the D_{it} value has been reduced 16% ~ 44% after FGA. Then, the HfO_2/Al_2O_3 gate stack with PDO 520℃ 3min was selected to be the best condition to fabricate Ge MOSFETs.

We have investigated the effect of FGA on Ge MOSFETs and epi-Ge on SOI MOSFETs. On/off ratio of our p^+n junction and Ge PMOSFET reached 4 orders and 1.4×10^3 respectively (500℃ 10 sec dopant activation, W/L = 100μm/5μm), with better subthreshold swing (165mV/dec) obtained after FGA. And On/off ratio of our

n^+p junction and Ge NMOSFET reached 3.5 orders and 2.3×10^3 respectively (600℃ 10 sec dopant activation, W/L = 100μm/5μm), with better subthreshold swing (151mV/dec) obtained after FGA. Also, the better subthreshold swing (464mV/dec for epi-60nm PMOSFET, 307mV/dec for epi-30nm PMOSFET, 256mV/dec for epi-60nm NMOSFET and 252mV/dec for epi-30nm NMOSFET) obtained after FGA. The on/off ratio is about 7.2×10^1 for epi-60nm PMOSFET, 3.3×10^2 for epi-30nm PMOSFET, 3.4×10^2 for epi-60nm NMOSFET and 3.7×10^2 for epi-30nm NMOSFET. For both Ge MOSFETs and epi-Ge on SOI MOSFETs, R_{SD} and hole mobility are increased after FGA, a peak hole mobility of 375 cm^2/Vs for bulk Ge PMOSFET, 313 cm^2/Vs for epi-60nm PMOSFET and 194 cm^2/Vs for epi-30nm PMOSFET after FGA are obtained. Epi-30nm Ge on SOI MOSFETs have better subthreshold swing because of the better gate control ability of thinner body, while epi-60nm Ge on SOI MOSFETs have larger on current and higher mobility due to the lower dislocation density.

Finally, pros and cons of FGA at 300℃ 30 min on both PMOSFET and NMOSFET were summarized according to our experimental data. Positive V_{th} shift, higher on current, better subthreshold swing and higher hole mobility are obtained after FGA, while series resistance is increased after FGA.

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碩士論文題目:

在鍺通道金氧半場效電晶體上使用後沉積氧化製造二氧化鉿/三氧化二鋁/氧化鍺/鍺之閘極介電層堆疊結構的研究

Investigation of $HfO_2/Al_2O_3/GeO_x$/Ge Gate Stacks Fabricated by Post Deposition Oxidation on Ge-Channel MOSFETs