國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

利用雙重微影成像法製作多晶矽鰭式場效電晶體元件之特性研究

A Study on the Device Characteristics of Polycrystalline Silicon FinFETs Fabricated with Double Patterning Technique

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黃調元 博士

中 華 民 國 一 〇 一 年 九 月

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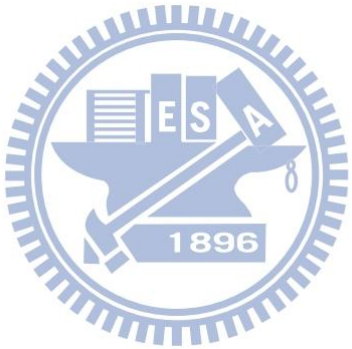
摘要

在本篇論文中，我們利用 I 射線(I-line)光學步進機與雙重微影成像法來製作 P 通道多晶矽鰭式場效電晶體(FinFET)。這種新穎的雙重微影成像技術不僅能夠製作出鰭寬度(fin width)與閘極長度(gate length)小到 80nm 的多晶矽鰭式場效電晶體且有控制良好的關鍵尺寸，並在製程上有不錯的均勻性。我們也利用準分子雷射退火(excimer laser annealing)製程來提高多晶矽通道的品質。

所製作之鰭寬度 80nm 的鰭式場效電晶體具有陡峭的次臨界擺幅(subthreshold swing, 255mV/dec)、高的開關電流比($\approx 10^9$)、與低的漏電流($<10^{-14}$A)，歸因於它較窄的鰭通道受到閘極良好的控制。另外，我們發現當元件的閘極長度等於或大於 0.4μm 時，晶界缺陷將顯著地影響次臨界擺幅；但是當閘極長度微縮至 0.2μm 或更小時，短通道效應(short channel effect)將主導次臨界擺幅的趨勢。

接著探討通道厚度 50nm 之低的高寬比(aspect ratio)元件。雖然低高寬比元件閘極的控制能力較差導致明顯的短通道效應；但是它們比通道厚度 100nm 之高的高寬比元件有較高的載子移動率與驅動電流，因其具有優良的準分子雷射退火結晶化條件。我們也探討了固相結晶法(solid phase crystallization)與準分子雷射退

火兩者之鰭式場效電晶體的元件特性之差別。雖然固相結晶元件的電性比準分子雷射退火元件還差，但是它們電性的均勻性較準分子雷射退火元件為佳。



A Study on the Device Characteristics of Polycrystalline Silicon FinFETs Fabricated with Double Patterning Technique

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Abstract

In this thesis, we have developed a novel method which employs an I-line stepper and double patterning (DP) technique to fabricate p-channel poly-Si FinFETs for the first time. This novel DP technique is capable of not only generating fin widths (W_{fin}) and gate lengths (L_g) of poly-Si FinFETs down to 80nm with good critical dimension control, but also providing good process uniformity. We also use the excimer laser annealing (ELA) process to achieve high-quality poly-Si channels.

The fabricated FinFETs with W_{fin} of 80nm have steep subthreshold swing (SS, 255mV/dec), high I_{on}/I_{off} current ratio ($\approx 10^9$), and low leakage current ($<10^{-14}$A) owing to its narrow fin which enabls a better gate control over the channel. In addition, we found that the grain-boundary defects would predominantly affect the SS of

devices when the L_g is equal to or larger than 0.4μm, but the short-channel effects (SCEs) dominate the trend of SS as devices are downscaled to L_g of 0.2μm and beyond.

The low aspect ratio (AR) devices with channel thickness (T_{Si}) of 50nm were also investigated and compared with devices with T_{Si} of 100nm. Although the low AR devices have poorer gate controllability and exhibit obvious SCEs, they have higher mobility and drive current over the high AR devices with T_{Si} of 100nm due to better crystallization results of ELA process. The differences in device characteristics between solid phase crystallization (SPC) and ELA FinFETs are also investigated. Although the SPC devices have poorer electrical characteristics than the ELA devices, they have better uniformity of electrical characteristics over the ELA devices.

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周涵宇

誌於風城交大

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Contents

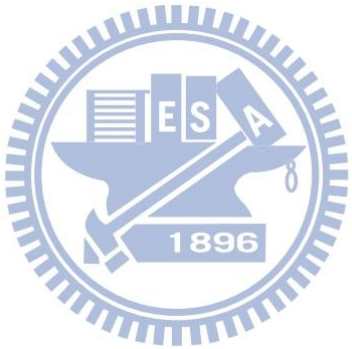

Figure Captions

Chapter 1

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Chapter 2

Chapter 1

Introduction

1.1 Overview of Multi-gate and FinFET Technology

The invention of transistors has resulted in a tremendous impact on human's life, and the semiconductor industry has been playing a key role for advancing the science and technology in the last few decades. To achieve high performance, high device density, low power dissipation, and low manufacturing cost of CMOS circuits, scaling down the semiconductor devices is necessary. According to Moore's Law, the number of devices on a circuit doubles approximately every two years [1]. Although the predicted period seems not so precise, overall the trend has continued for half a century. However, the 2010 update of International Technology Roadmap for Semiconductors (ITRS) has announced that device density doubles only every three years at the end of 2013 and many difficult challenges for further scaling are emerging [2]. As the gate length of MOS devices shrinks down and approaches the physical limitation (Fig. 1-1), several major challenges are lying ahead, such as short channel effects (SCEs), leakage currents, and reliability, etc. These problems will degrade the device characteristics. Therefore, non-classical device structures have been explored to deal with these issues aimed at enabling continued scaling [3].

There are many researches on novel device structures in recent years. The

multiple-gated (MG) structure in which the non-planar channel region is controlled by a gate wrapping around has been attracting much attention [4]. Devices adopting the MG structure can suppress the penetration of the drain electric field into the channel. Therefore, MG transistors can increase the gate controllability over the channel in order to suppress the SCEs. Among the MG transistors, Fin-type MOSFET (FinFET), which was proposed by Hisamoto in 1989 [5] and Hu in 1998 [6], is considered as one of the most promising devices. Several types of FinFET structures have been developed, such as double-gate (DG) [7], tri-gate (TG) [8], and Ω-gate [9]. The TG structure of a FinFET is shown in Fig. 1-2. In the scheme, the active channel is patterned to form a fin-like structure and the gate wraps both the top and side surface of the fin [10]. Such a scheme can reduce bulk leakage current due to good electrostatic control on channel potential. It can also promote the current density per unit planar width considering the adoption of vertical channel regions. Additionally, the quasi-planar structure of FinFETs is compatible with the conventional MOSFET process technology [11]. In 2011, Intel announced that it will use FinFETs in its 22 nm-node manufacturing of microprocessors in 2012 [12]. Therefore, the FinFET has been perceived as a promising device for the 22 nm technology node and beyond.

1.2 Double Patterning Technique

When the devices shrink in size, advanced lithography technique is essential to keep the Moore's Law. The resolution R of a lithography process follows the Rayleigh theory [13], which can be expressed as:

$$R = K_1 \times \frac{\lambda}{NA} \quad (1\text{-}1),$$

where K_1 is a system constant, λ is the wavelength of the light, and NA is the numerical aperture. We can modulate these variables of Rayleigh equation in order to achieve higher resolution for shrinking the feature size. Many lithographic technologies have been developed to reduce K_1 factor, such as off-axis illumination (OAI), phase shift mask (PSM), optical proximity correction (OPC), and immersion technology. Additionally, the reduction of wavelength can also improve resolution. For instance, the progress of light sources of lithography tools has evolved from G-line (436nm), I-line (365nm), KrF excimer laser (248nm), to ArF excimer laser (193nm). However, the finer resolution is acquired at the expense of incredible development cost. The e-beam and ion-beam lithography systems have also been proposed because of their capability to achieve a fine resolution, but the extremely low throughput prevents them from being adopted in practical manufacturing [14].

The double patterning (DP) technique is a potential way to improve resolution and theoretically it can cut the pitch in half with currently available tools. A typical DP process consists of twice lithographic and subsequent etching steps [15]. Although

DP has additional mask and etching process cost, it can maintain a good throughput. Actually the DP method with 193 nm immersion lithography has been adopted by the IC manufacturers in the 32 nm node in recent years [16]. However, these advanced lithography facilities for generating nano-scale patterns are very costly and not available for the studies conducted in academic organizations. Nonetheless, sub-100 nm patterns can also be readily achieved with an I-line stepper [17]. In this study, such DP technique using an I-line stepper is adopted to fabricate FinFETs.

1.3 Overview of Low Temperature Polycrystalline Silicon Thin Film Transistors (LTPS TFTs)

In the past decades, amorphous silicon thin film transistors (a-Si TFTs) had been used as the switching device of pixels in the active-matrix liquid-crystal displays (AMLCDs) [18]. A-Si TFTs possess low leakage current and low process temperatures. However, the carrier mobility of a-Si TFTs (<1 cm^2/V-s) is much lower than that of polycrystalline silicon (poly-Si) TFTs (10-500 cm^2/V-s) [19]. In order to integrate high-performance driver circuits on the same display panel, low-temperature-processed poly-Si TFTs were actively developed recently. Poly-Si TFTs have the advantages of high driving current, good device reliability, and low temperature process compatibility. Poly-Si TFTs are not only used in the application

of displays but also have the potential for construction of 3-dimentional integrated circuits [20].

In addition, the low temperature polycrystalline silicon (LTPS) fabrication process plays an important role in the crystallization of the poly-Si thin films from a-Si, and the quality of crystallized poly-Si thin films has a great influence on the performance of LTPS TFTs. In order to improve the quality of the poly-Si thin films and reduce the cost of process, there are several LTPS technologies developed, such as solid phase crystallization (SPC) [21], excimer laser annealing (ELA) [22], and metal induced lateral crystallization (MILC) [23]. The SPC and ELA methods are used in this work and will be introduced in the following sub-sections.

1.3.1 Solid Phase Crystallization (SPC)

The SPC is a commonly used method to transform the a-Si thin film into poly-Si thin film by thermal annealing. The annealing temperature is around 600℃ in N_2 ambient, and the process time is about 24 hours [24]. However, the annealing time is long and will limit the throughput of device fabrication. In addition, the quality of an SPC poly-Si thin film is affected by its small grain size because the abundant defects located in or close to the grain boundaries, such as intra-grain strained bonds and inter-grain dangling bonds, tend to impede the carrier transport and formation of the inversion channel layer.

1.3.2 Excimer Laser Annealing (ELA)

Recently, the ELA has become the most promising crystallization method in the fabrication of LTPS TFTs [25]-[26]. Types of the excimer lasers include ArF, KrF, and XeCl (wavelengths are193, 248, and 308nm, respectively) gaseous discharges. Due to the short pulse duration time (typically 10-30ns) of the irradiation and large absorption coefficients of a-Si thin film to UV lights, ELA process can confine the heat to the silicon thin film and avoids the thermal damage to the underlying glass substrate [27]. In the ELA process, the phase transformation from a-Si to poly-Si occurs by melting the silicon thin films. As the laser energy exceeds a threshold energy, the irradiated a-Si thin film melts and then solidifies into large grains in a very short time [28]. As a result, the high quality and large-grained poly-Si thin films can be achieved with less defects and high throughput.

1.4 Motivation

The aforementioned merits of FinFET structure, such as enhanced gate controllability and reduction of the total amount of defects contained in the tiny fin channel, are expected to improve the performance of LTPS devices. As the conduction width of a FinFET is approximately the sum of the side and the top surface dimensions, this vertical feature can be optimized by increasing the aspect ratio of the fins to an extent without complicating the process integration too much.

Moreover, FinFETs will show improved SCE control when the fin width is scaled, and the improvement in device density might also be achieved [29].

In this work, we have developed a method which employs an I-line stepper and double patterning (DP) technique to fabricate p-channel poly-Si FinFETs for the first time. Both the fin and gate are defined by DP lithography and conventional dry etching. Since defects in the poly-Si channel will adversely affect device characteristics, to reduce the defects, we use the ELA process to achieve high quality of poly-Si thin films with low-temperature process.

1.5 Thesis Organization

This thesis is divided into four chapters. In Chapter 1, the background and motivation of poly-Si FinFETs technology are already given above. In Chapter 2, the process flow of FinFETs is described in detail. We monitored the DP process with in-line SEM analysis during the device fabrication. In Chapter 3, we present the electrical characteristics of the fabricated P-channel FinFETs. The characteristics of FinFETs with various channel dimensions and crystallization method are compared and discussed. Finally, in Chapter 4, we conclude the results and suggest the future work.

Chapter 2

Device Structure and Process Flow

2.1 Device Fabrication and Process Flow

The process steps of FinFET fabrication are described as follows, and the fabrication process for the proposed device is shown in Fig. 2-1. First, a 1000nm-thick wet oxide was grown on six-inch silicon wafers to serve as the buried oxide. Next, an a-Si layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550℃ (Fig. 2-1(a)), and the a-Si thickness was split into 50nm and 100nm. Then, the 50 nm-thick a-Si thin films and part of the 100 nm-thick ones were transformed into polycrystalline by excimer laser annealing (KrF, 480 mJ/cm^2), and the remaining 100nm-thick a-Si thin film was transformed into polycrystalline by solid phase crystallization at 600℃ in N_2 ambient for 24 hours (Fig. 2-1 (b)). Afterwards, the poly-Si thin film was defined by the A1 and A2 masks with the double patterning (DP) technique (Figs. 2-1 (c) to (e)) to form the active channel regions.

A TEOS-oxide layer was then deposited as gate oxide by LPCVD (Fig. 2-1 (f)), and the gate oxide thickness was either 10nm or 30nm. Subsequently, a 120nm-thick *in-situ* n^+ poly-Si layer was deposited by LPCVD to serve as the gate electrode (Fig. 2-1 (g)). Afterwards, the gate electrode was defined by the G1 and G2 masks with another double patterning process (Figs. 2-1 (h) to (j)).

The first BF_2^+ ion implantation was used to dope the sidewalls of p^+ source/drain for p-channel FinFETs with 10-nm thick gate oxide (at 30keV, 1×10^{14} cm^{-2}, tilt angle =60°) or 30-nm thick gate oxide (at 54keV, 1×10^{14} cm^{-2}, tilt angle =60°), as shown in Fig. 2-1 (k). A 55nm-thick TEOS-oxide layer was deposited by LPCVD (Fig. 2-1 (l)), followed by a dry etching step to form the spacer (Fig. 2-1 (m)), whose width is about 38nm. Afterwards, the second self-aligned BF_2 ion implantation was used to dope the topside of p^+ source/drain with split of 10-nm thick gate oxide (at 25keV, 5×10^{15} cm^{-2}, tilt angle =0°) and split of 30-nm thick gate oxide (at 46keV, 5×10^{15} cm^{-2}, tilt angle =0°), respectively, as shown in Fig. 2-1 (n), followed by rapid thermal annealing (RTA) at 850℃ for 5 seconds. Finally, the passivation layer deposition, contact hole opening, metallization, and H_2 sintering processes were done to complete the fabrication of FinFETs.

The split conditions of the fabricated FinFETs are summarized in Table 2-1. Dimensions of both designed gate length (L_{mask}) and fin width (W_{mask}) with double patterning process are shown in Table 2-2.

2.2 Feasibility of Double Patterning Technique

As described in previous section that both the fins and gates were defined by the DP technique. We use an I-line stepper (Table 2-3) to generate photoresist (PR)

patterns, and employed an in-line scanning electron microscope (SEM) and transmission electron microscopy (TEM) to check the fabricated structures of the fins and gates. In Fig. 2-1 (c), the PR pattern generated by the A1 mask is used to preliminarily define the active channel region with the first etching process, and then the PR pattern generated by the A2 mask covers portion of the active channel region (e.g., the bottom half of the active region, as shown in the top view of Fig. 2-1 (d)). After the second etching process, the overlapped region of A1 and A2 masks defines the final fin channel (Fig. 2-1 (e)).

Figures 2-2 (a) to (d) show the in-line SEM images of the etched poly-Si fins achieved with the DP method. These images obviously evidence that the DP can reliably shrink the poly-Si fin width down to sub-100 nm scale. The results and variations of fin widths are shown in Fig. 2-3 by measuring samples of different designed fin width (W_{mask}) taken from different locations of the Si wafers. These results confirm that the DP method is capable of not only generating fins with width down to 80 nm and good critical dimension (CD) control, but also providing good process uniformity.

We use another DP process to define the gated region. In Fig. 2-4 (a), the remained poly-Si in the right side is defined using the G1 mask. PR generated by the G2 mask subsequently covers the left side, as shown in Fig. 2-4 (b). In this figure we

can obviously see that a misalignment between the PR and underlying poly-Si occurs in the circled region. An enlarged view of this region is shown in Fig. 2-4 (c), from which we can see that the misalignment is around 84nm, much larger than the overlay spec. of the I-line stepper (Table 2-3). This indicates that the dimensions of the patterns on G1 and G2 masks may deviate from the designed values and lead to the observed misalignment. The aforementioned glitch is likely to be resulted during the manufacturing of the masks considering the fact that the etching of the patterns was done with manual wet processing. Fortunately this issue can be addressed by shifting the wafer stage of the stepper by -80nm along the horizontal direction in the figure during exposure to compensate for the misalignment. Results after implementing the measure are shown in Figs. 2-4 (d) to (e). Obviously the above method works well from the good alignment shown in the figures.

Figures 2-5 (a) to (d) show the in-line SEM images of the poly-Si gates of different dimensions patterned with the 2nd DP process. The variations of gate lengths taken from different locations of the Si wafers are shown in Fig. 2-6. Still, good controls over the gate CD down to 80 nm and uniformity are achievable.

In the gate DP process, we find that the widths of the fin channel beneath the gate electrode will affect the resulted gate lengths. Table 2-4 summarizes the measured gate lengths of the same designed gate length (L_{mask}) formed on fins of

different widths. The data were collected from structures located in the same die. It is seen that the measured gate length decreases as fin width increases. In-line SEM images of a set of samples with L_{mask} of 200 nm are shown in Fig. 2-7. This finding is postulated to be related to the different surface morphology of the PR spun on the gate lying over the channel of various widths. As shown in Fig. 2.8, the thickness of the PR gets thinner as the channel width is increased due the action of spinning. A thinner PR would lead to a finer pattern after exposure, as the finding shown above.

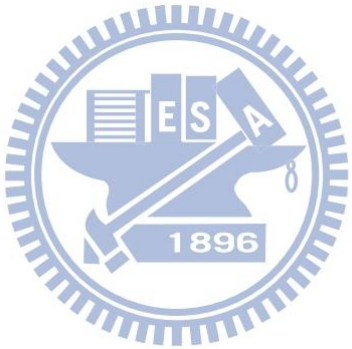
Fig. 2-9 shows the cross-section TEM graph of an ELA poly-Si channel, and the measured channel fin width (W_{fin}) and thickness (T_{Si}) are 132nm and 94nm, respectively, which are smaller than the grain size of ELA poly-Si channel (0.3~0.5μm) [30]. With such a fine channel structure, it is expected that no or only one single grain boundary will be contained in the channel region as the channel length is scaled below half a micron regime. The fabricated devices would thus exhibit high performance but with a high fluctuation.

With in-line SEM and TEM analysis, we can confirm the capability of this novel lithography technique in the fabrication of sub-100 nm FinFET devices.

2.3 Electrical Measurement Setup

In this study, electrical characterizations of the fabricated devices were

performed by a measurement system which consists of an HP-4156A semiconductor parameter for I-V measurements, an Agilent-E5250A switch, and a temperature regulated hot-chuck for keeping the wafer temperature stable. Interactive Characterization Software (ICS) is used to set up all measurement conditions and extract the electrical parameters of the devices.



Chapter 3

Results and Discussion

3.1 Basic Electrical Characteristics of P-channel FinFETs

From the I_d-V_g transfer curve measured at V_d = -0.5V, the characteristics of P-channel FinFET can be extracted as follows:

Threshold voltage (V_{th}) is defined by using the constant current method to be the gate voltage (V_g) needed to achieve the drain current (I_d) of 50nA×(W_{eff}/L_g):

$$V_{th} = V_G @ I_D = 50nA \times \frac{W_{eff}}{L_g} \quad (3\text{-}1),$$

where W_{eff} and L_g are effective conduction width and gate length, respectively. The effective conduction width (W_{eff}) of a channel is the sum of channel fin width (W_{fin}) and twice the channel thickness ($2\times T_{Si}$), as shown in Fig. 3-1.

Subthreshold swing (SS) can be extracted from the subthreshold current with the following form:

$$SS = \frac{\partial V_g}{\partial(\log I_d)} \quad (3\text{-}2).$$

Figure 3-2 shows the characteristics of electrical measurements performed on a device with a narrow W_{fin} of 80 nm. The device has a steep SS (255mV/dec), a high I_{on}/I_{off} current ratio ($\approx 10^9$), and low leakage current ($<10^{-14}$A) owing to its narrow fin enabling a better gate control over the channel. Figure 3-2 (a) also shows good control over the short channel effect (SCE) with negligible drain induced barrier lowering

(DIBL).

Figure 3-3 shows the transfer characteristics of the fabricated devices with gate length of 0.2μm and various fin widths. Devices with narrow W_{fin} of 0.08 and 0.1μm can achieve low SS. However, the V_{th} becomes more positive and the subthreshold current increases when the fin's width increases to 0.2μm or wider. For these wider dimensions, the "fin" channel actually becomes quasi-planar and thus the gate controllability is degraded [31]. As a result, a significant amount of sub-surface punch-through current would conduct and lead to a high subthreshold leakage.

Figure 3-4 and Fig. 3-5 show the transfer characteristics of the fabricated devices with gate length of 0.4μm and 1μm, respectively, and various W_{fin}. The leakage current of these long channel devices is much lower than that of the device with gate length of 0.2μm because of reduced SCE. In Fig. 3-4, the SS decreases as W_{fin} decreases because of better gate controllability. In Fig. 3-5, the leakage current increases as W_{fin} increases owing to the larger sub-surface leakage current.

Figure 3-6 shows the transfer characteristics of devices having the W_{fin} of 80 nm with various gate lengths (L_g). The devices with longer gate lengths of 0.2, 0.4, and 1μm have good I_{on}/I_{off} current ratio of about 10^8 to 10^9. Nonetheless, the I_{on}/I_{off} current ratio is smaller than 10 when the L_g is equal to or smaller than 0.1μm. Obviously here the short-channel effects are significant, implying dopant diffusion from S/D into the

channel occurs [32]. To improve the transfer characteristics of the short-channel devices, it requires a refined S/D annealing scheme with a tighter control over the thermal budget to suppress the undesirable dopant diffusion.

In Fig. 3-6, the SS of L_g of 0.4μm device is better than that of the L_g of 1μm device, which is in conflict with the trend of SCE. The following equation is the relation between the SS and the effective trap-state concentration (N_{trap}) for poly-Si TFTs:

$$SS = \ln 10 \times \frac{kT}{q} \times (1 + \frac{C_T}{C_{ox}}) \quad (3\text{-}3),$$

where $C_T = qN_{trap}W_d$, and W_d is the effective depletion width. The grain size of ELA poly-Si channel is about 0.3~0.5μm [30] which is comparable to the devices with L_g of 0.4μm. Therefore, the number of the grain boundaries could be small and even zero. This would reduce the trap-state concentration and result in better SS over the devices with L_g of 1μm. The V_{th} roll-off is shown in Fig. 3-7. Since the V_{th} roll-off from L_g of 1μm to L_g of 0.4μm devices is unobvious, the grain boundary defects would predominantly affect the SS in the devices. Fig. 3-8 shows the SS of the devices with various W_{fin} as a function of L_g. As it can be seen in the figure that the SS of the devices with L_g of 0.4μm is very sensitive to W_{fin} and tends to decrease as W_{fin} is shortened. Two reasons are responsible for such a trend. One is the phenomenon pointed out in last chapter that a wider fin would result in a shorter

printed channel length. The other is the greatly enhanced gate controllability over the channel as the fin is scaled to nano-scale. In Fig. 3-7 the V_{th} roll-off is obvious because of SCE, and the SS is the worst in Fig. 3-8. From Fig. 3-9, we confirm that the devices with L_g of 0.2μm exhibit large DIBL, contrary to the devices with $L_g \geqq$ 0.4μm whose DIBL is negligible. The results evidence that SCE dominates the trend of SS as devices are downscaled to L_g of 0.2μm and beyond.

The dimension of W_{fin} of 0.08μm is much smaller than the ELA poly-Si grain size (0.3~0.5μm). As mentioned above, the SS of W_{fin} of 0.08μm devices at L_g of 0.4μm is much lower than the devices with W_{fin} of 0.4μm and 1μm in Fig. 3-8. Meanwhile, in Fig. 3-7 and Fig. 3-8, the standard deviations of both V_{th} and SS characteristics increase as the W_{fin} decreases at the same L_g, and also increases as L_g decreases at the same W_{fin}. Although a decrease in W_{fin} tends to better device performance from the presented results, the uniformity of device characteristics suffers owing to the fluctuation in structural parameters like W_{fin} and the grain size of ELA poly-Si.

3.2 Device Characteristics of Various Channel Structure

Characteristics of devices with thin channel thickness (T_{Si}) of 50nm are presented and discussed in this section. Figure 3-10 shows the transfer characteristics

of the devices with gate length of 1μm and various fin widths. The SS decreases as W_{fin} decreases because of better gate controllability. Most of trap centers located at or near the grain boundaries are charged positively as the surface potential of the channel becomes inverted, and the threshold voltage can be expressed as [33]

$$V_{th} = V_{FB} + 2\phi_F + \frac{qN_{trap}W_d}{C_{ox}} \quad (3\text{-}4),$$

where N_{trap} and W_d are trap state density and effective depletion width, respectively. In Fig. 3-10 of these long channel devices, the V_{th} becomes more negative as the W_{fin} increases because wider W_{fin} contains more poly-Si grain boundaries (and thus higher N_{trap}). A reduction in N_{trap} as W_{fin} decreases also reflects on the higher on-current shown in the figure.

The low aspect ratio (AR, equal to T_{Si}/W_{fin}) of the channel at a fixed T_{Si} leads to the poorer gate control over the channel potential [31]. This trend is obviously shown in Fig. 3-11, in which the transfer characteristics of the devices with gate length of 0.4μm and various fin widths are compared. As compare with the results shown in Fig. 3-4 (b) for devices with T_{Si} of 100nm, the SS and subthreshold leakage increase at the same W_{fin} because the devices with low AR have worse gate controllability [31]. The trend is more obvious as $W_{fin} \geqq 0.4\mu m$.

Figure 3-12 shows the V_{th} of the devices with various W_{fin} as a function of L_g. As compared with Fig. 3-7, The V_{th} roll-off for devices from L_g of 1μm to L_g of 0.4μm is

obvious because of worsened gate controllability. Meanwhile, in Fig. 3-12, the drop in V_{th} with decreasing channel length is more obvious for devices with W_{fin} of 0.4 and 1μm than that for devices with W_{fin} of 0.08 and 0.2μm. Figure 3-13 shows typical transfer characteristics of devices measured at V_d = -0.5 and -1.5 V with gate length of 0.4μm and fin widths (W_{fin}) ranging from 0.08 to 1μm. From the figure, we can see the devices with W_{fin} of 0.4μm and 1μm exhibit larger DIBL. This confirms that devices with wider W_{fin} suffer more serious SCE because of poorer gate controllability.

Figure 3-14 shows the SS for the devices with various W_{fin} as a function of L_g. The SS for devices with L_g of 0.4μm is better than that for devices with L_g of 1μm at W_{fin} of 0.08 and 0.2μm. From eq. 3-3, the grain boundary defects would predominantly affect the SS in these devices with a narrow W_{fin}. In contrast, for device at W_{fin} of 0.4 and 1μm, the SS for devices with L_g of 0.4μm is higher than that for devices with L_g of 1μm, which is different form that shown in Fig. 3-8 for devices with T_{Si} of 100nm. From Fig. 3-13, the devices with wide W_{fin} of 0.4 and 1μm at low AR with T_{Si} of 50nm have large DIBL. Fig. 3-14 evidences that SCE dominates the trend of SS in these devices with wide W_{fin} and low AR.

Figure 3-15 compares the electrical characteristics of two devices with the same effective fin width ($W_{eff} = W_{fin} + 2T_{Si}$) at gate length of 0.4μm. W_{fin} (T_{Si}) for the two

devices are 100 (100) and 200 (50), respectively. The device with T_{Si} of 100nm has steeper SS and lower subthreshold leakage than the device with T_{Si} of 50nm due to improved gate controllability, but the on-current is lower than the device with T_{Si} of 50nm. We further extract the field-effect mobility (μ_{FE}) of devices with different T_{Si}, and the μ_{FE} is determined by

$$\mu_{FE} = \frac{L_g G_m}{W_{eff} C_{ox} V_d} \quad (3\text{-}5),$$

where G_m is the maximum transconductance and C_{ox} is the gate capacitance per unit area. As shown in Fig. 3-16, the μ_{FE} of the device with T_{Si} of 50nm is larger than that of the device with T_{Si} of 100nm. The reason is postulated to be related to the ELA condition [34]. Note that we used the same excimer laser energy (480mJ/cm^2) to crystallize the a-Si films of different thickness. In the thicker T_{Si} film of 100nm, the laser energy might cause only surface melting of the a-Si layer rather than the entire layer (i.e., melting depth < film thickness) [35], as schematically shown in Figs. 3-17 (a) to (c). This results in a smaller grain size and low quality of poly-Si film [36]. In the thinner T_{Si} film of 50nm, the laser energy causes near-complete-melting of the thin film consisting of un-melted discrete silicon islands (i.e., melting depth $\approx$ film thickness) [37], as shown in Figs. 3-17 (d) to (f). Because the distance between the nucleation sites of silicon islands is long, the grain size of the poly-Si in this regime is larger than the poly-Si with partial-melting transformation regimes. Therefore, the

mobility and on-current for devices with T_{Si} of 50nm are higher than those for the devices with T_{Si} of 100nm.

Figure 3-18 extracts the source/drain series resistance (R_{SD}) of these devices with different T_{Si} by the total resistance method [38]:

$$R_m = \frac{V_d}{I_d} = R_{SD} + R_{channel} \quad (3\text{-}6),$$

where R_m is the measured resistance, and $R_{channel}$ is the channel resistance. The R_{SD} for the devices with T_{Si} of 100nm is about 21kΩ, which is larger than that for the devices with T_{Si} of 50nm (~10kΩ). Note that the implantation and annealing process condition of devices with different T_{Si} are the same as mentioned in last chapter. The reduction in R_{SD} for devices with T_{Si} of 50nm is another reason for the higher on-current and mobility as compared with devices with T_{Si} of 100nm, and is attributed partly to the larger grain size of the 50 nm-thick channel.

Figure 3-19 shows the transfer characteristics of the devices with W_{eff} of 0.3 and 0.6μm and at the same L_g of 0.4μm. The device with W_{eff} of 0.3μm has better SS and lower subthreshold leakage than the device with W_{eff} of 0.6μm because of better gate controllability. The on-current of the device with W_{eff} of 0.3μm is larger than that of the device with W_{eff} of 0.6μm because the thinner T_{Si} contains less defects.

3.3 FinFETs with Different Crystallization Method of SPC

and ELA

A comparison in the device characteristics between SPC and ELA devices is discussed in this section. Figure 3-20 shows the electrical characteristics of the fabricated devices which have T_{si} = 100 nm, W_{fin} of 80nm, and T_{ox} = 10 or 30 nm. Because the grain size of SPC poly-Si is smaller than that of ELA [39], the SPC channel has more grain boundaries (GB) and thus more defects than the ELA channel. As a result, the SS of SPC devices are worse than that of the ELA devices (refer to eq. 3-3), as shown in Fig. 3-20 (a). Also, the subthreshold leakage of SPC devices is higher than that of the ELA devices. In Fig. 3-20 (b), the SPC device has lower drive current than the ELA device with the same T_{ox} of 10nm. The drive current of the ELA device with T_{ox} of 30nm is the lowest because of the much thicker gate oxide. The field-effect mobility of the SPC device is lower than that of the ELA one, as shown in Fig. 3-21, obviously due to more grain boundary defects contained.

Figure 3-22 shows the V_{th} roll-off characteristics of SPC and ELA devices with W_{fin} of 80nm as a function of L_g. The V_{th} of SPC devices with T_{ox} of 10nm, which is comparable to the V_{th} of ELA devices with T_{ox} of 30nm, becomes more negative than that of the ELA devices with the same T_{ox} of 10nm due to more poly-Si grain boundaries in the SPC channel (eq. 3-4). Nonetheless, the V_{th} roll-off is comparable for the SPC and ELA samples with same T_{ox} of 10nm. As T_{ox} increases to 30nm,

worse V_{th} roll-off is observed. Figure 3-23 shows the SS of SPC and ELA devices with W_{fin} of 80nm as a function of L_g. Since the V_{th} roll-off from L_g of 1μm to L_g of 0.4μm is not obvious in Fig. 3-22, the grain boundary defects would predominantly affect the SS in the devices with W_{fin} of 80nm (eq. 3-3). Obviously here the SS of SPC devices with L_g of 0.4μm is much poorer than those of the ELA devices with L_g of 0.4μm, as shown in Fig. 3-23. As L_g is below 0.4 um, the SS obviously increases for all devices due to serious SCE.

However, the standard deviations of both V_{th} and SS of SPC devices are lower than those of the ELA devices with the same W_{fin} of 80nm, as shown in Fig. 3-22 and Fig. 3-23. This is ascribed to the tiny grain size of the SPC poly-Si which is less than 0.1μm [39], much smaller than the grain size of ELA (0.3~0.5μm). Although an increase in grain size of ELA poly-Si tends to better device performance, the uniformity of device characteristics suffers owing to the fluctuation in structural parameters and the grain size.

Chapter 4

Conclusion and Future Work

4.1 Conclusion

In this study, we have developed a novel method which employs an I-line stepper and double patterning (DP) technique to fabricate p-channel poly-Si FinFETs for the first time. We also use the ELA process to achieve high quality of poly-Si channel. With the aid of DP technique, various devices with different fin widths (W_{fin}) and gate lengths (L_{gate}) were fabricated and characterized in our study. The effects of grain size, channel dimensions, and crystallization methods (SPC and ELA) on the device characteristics were investigated.

From the in-line SEM characterization, this novel DP technique is capable of not only generating W_{fin} and L_{gate} of poly-Si FinFETs down to 80nm with good critical dimension control, but also providing good process uniformity. During the gate DP process, we found that the widths of the fin channel beneath the gate electrode will affect the resulted gate lengths. This phenomenon would affect the SCE of the devices with shorter L_{gate}.

Most of the fabricated FinFETs have steep subthreshold swing (SS), high I_{on}/I_{off} current ratio, and low leakage current owing to its narrow fin enabling a better gate control over the channel. As the W_{fin} of devices increases, the gate controllability

becomes poor and the sub-surface leakage current increases, resulting in poor SS. In addition, we found that the SS of L_g of 0.4μm device is better than that of the L_g of 1μm device because the grain-boundary defects would predominantly affect the SS in these devices. However, the devices with L_g of 0.2μm exhibit large DIBL. Thus the SCE dominates the trend of SS as devices are downscaled to L_g of 0.2μm and beyond.

The low aspect ratio (AR) devices with channel thickness (T_{Si}) of 50nm were investigated. As compared with the high AR devices with T_{Si} of 100nm, these low AR devices have larger SS, higher subthreshold leakage, and larger DIBL due to poorer gate control over the channel potential. Nevertheless, since the laser energy of ELA process causes near-complete-melting of the thin film with 50nm, large grain size and high quality of poly-Si film with 50nm are achieved. As a result, we found that the devices with T_{Si} of 50nm have higher mobility, lower source/drain series resistance, higher drive current over the devices with T_{Si} of 100nm.

The difference of electrical characteristics of SPC and ELA FinFET devices was investigated. The SPC devices have poorer SS, higher subthreshold leakage, more negative threshold voltage (V_{th}), lower field-effect mobility, and lower drive current than the ELA devices due to more grain-boundary defects contained in the SPC channel. However, the SPC devices have better uniformity of device characteristics than the ELA devices, ascribed to the tiny grain size of SPC poly-Si which is much

smaller than the channel structural parameters.

4.2 Suggestions for Future Work

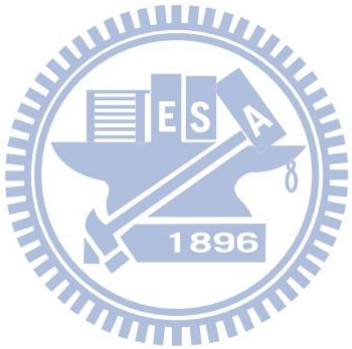
In this work, we have successfully fabricated p-channel poly-Si FinFETs with a novel DP technique. However, some issues still exist, and directions for the future work are discussed as follows.

During the gate DP process, we find that a wider fin channel beneath the gate electrode would result in a shorter printed channel length. This phenomenon would further affect the SCE of the devices with wider fin channel. More efforts are needed to comprehend the root cause of this phenomenon.

The devices with longer gate lengths of 0.2, 0.4, and 1μm have good I_{on}/I_{off} current ratio. However, the I_{on}/I_{off} current ratio is smaller than 10 when the L_g is equal to or smaller than 0.1μm, implying dopant diffusion from S/D into the channel occurs. It requires a refined S/D annealing scheme with a tighter control over the thermal budget to suppress the undesirable dopant diffusion.

As the fin width of ELA FinFETs is scaled down to sub-100 nm regime, the devices would thus exhibit high performance but with a high fluctuation of electrical characteristics. On the other hand, the SPC FinFETs with tiny grain size would reduce the fluctuation but the device performance suffers. As a result, the fluctuation in

structural parameters and the grain size of poly-Si should be optimized.



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Figures:

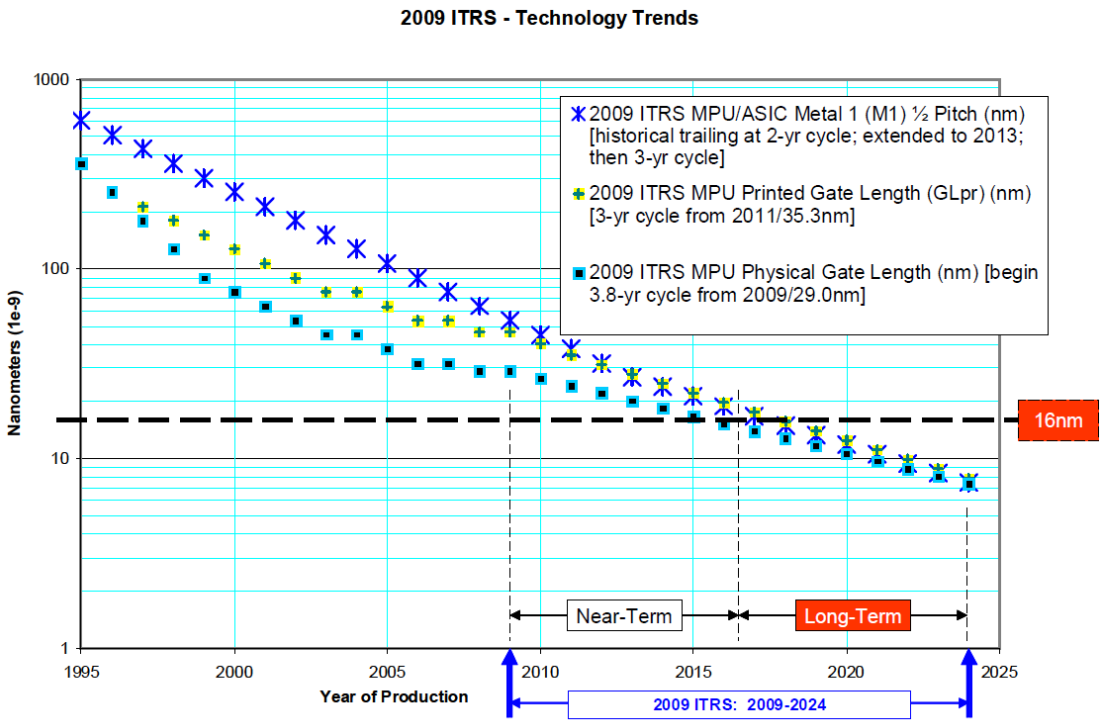


Fig. 1-1 2009 ITRS gate length trends of microprocessor unit (MPU) [2].

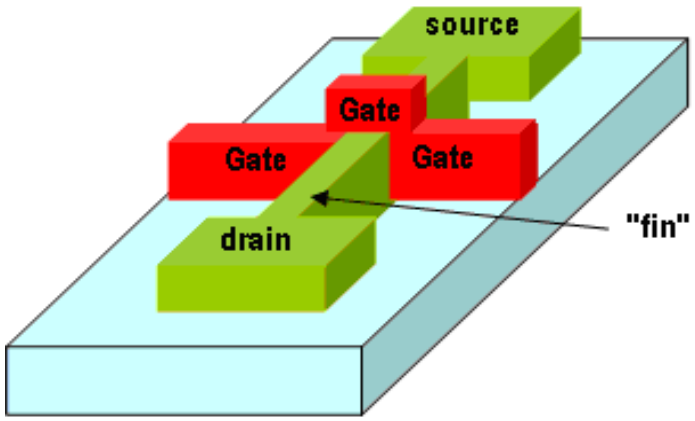
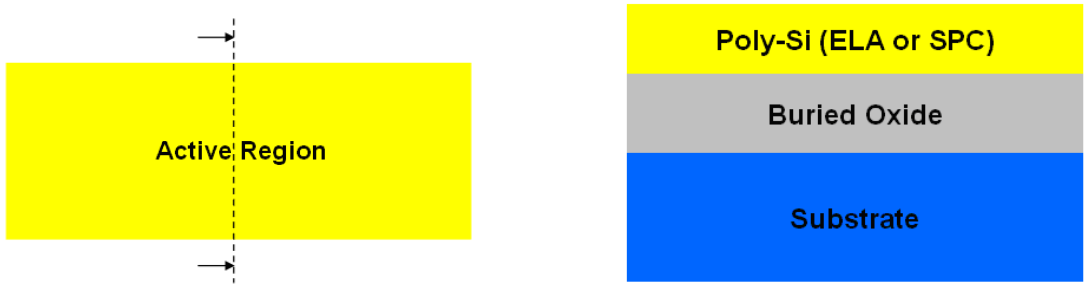
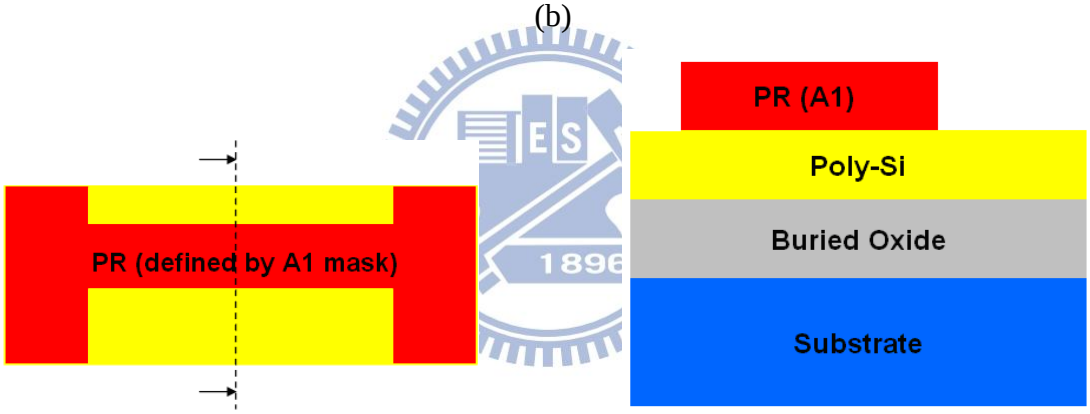


Fig. 1-2 The 3-D view of a TG FinFET structure [10].

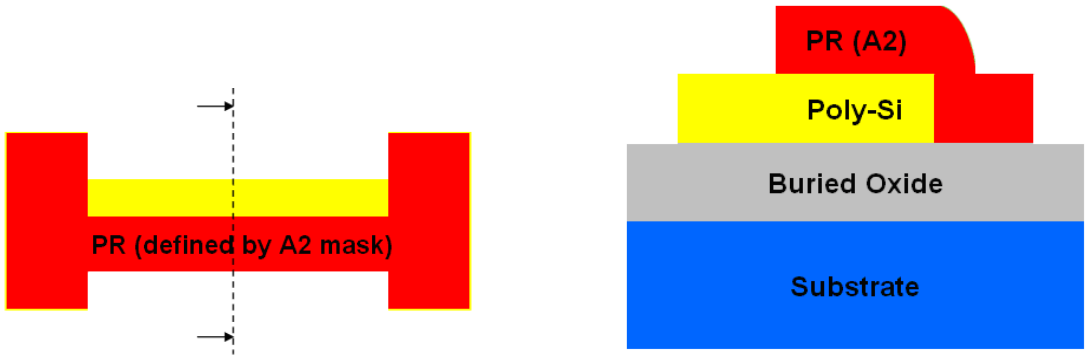
(a)



(b)

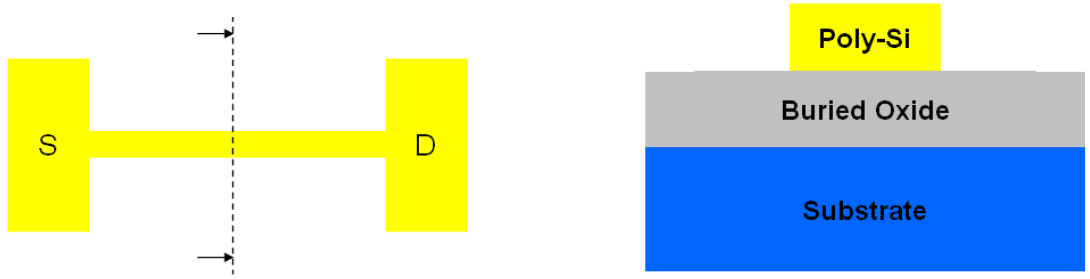


(c)

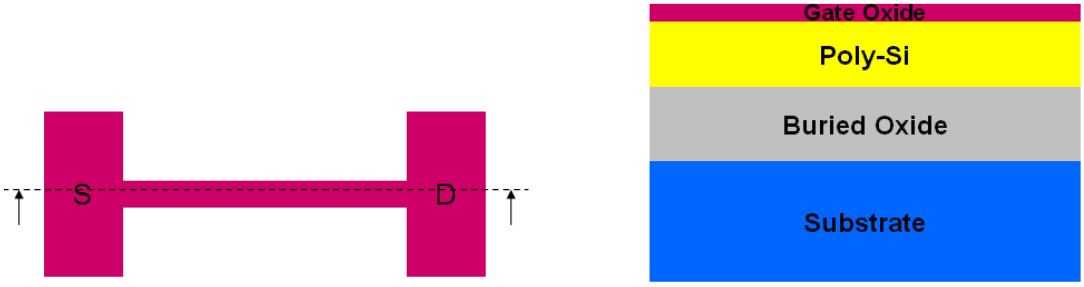


(d)

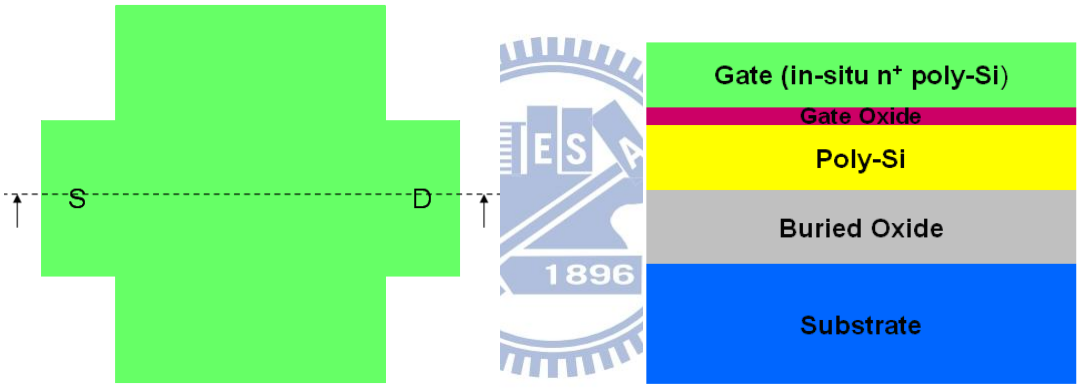
Fig. 2-1 (a)-(n) Process flow of p-channel FinFETs with double patterning technique. The left-hand-side figures are top views, and the right-hand-side figures are cross-sectional views.



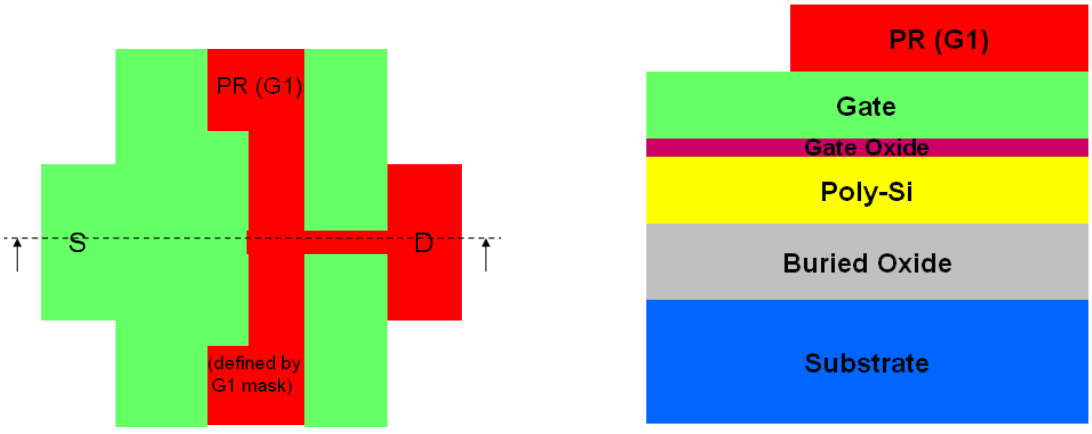
(e)



(f)

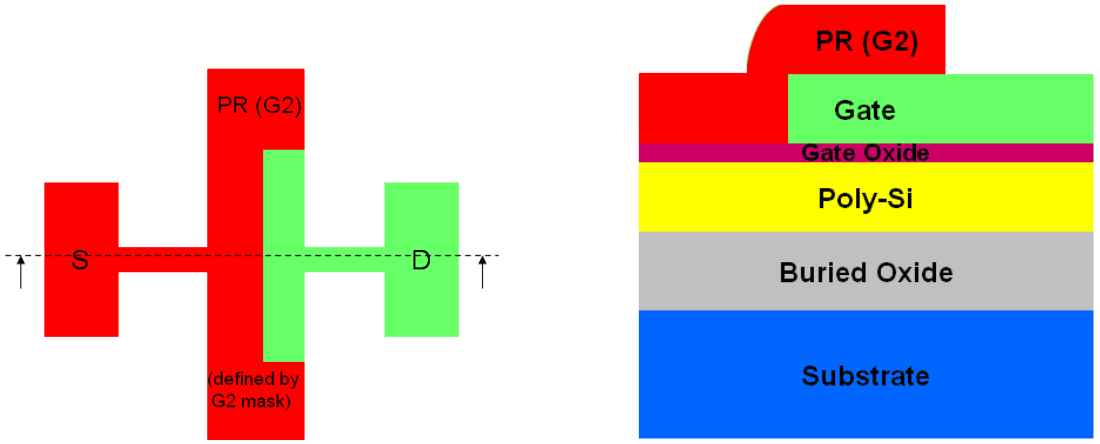


(g)

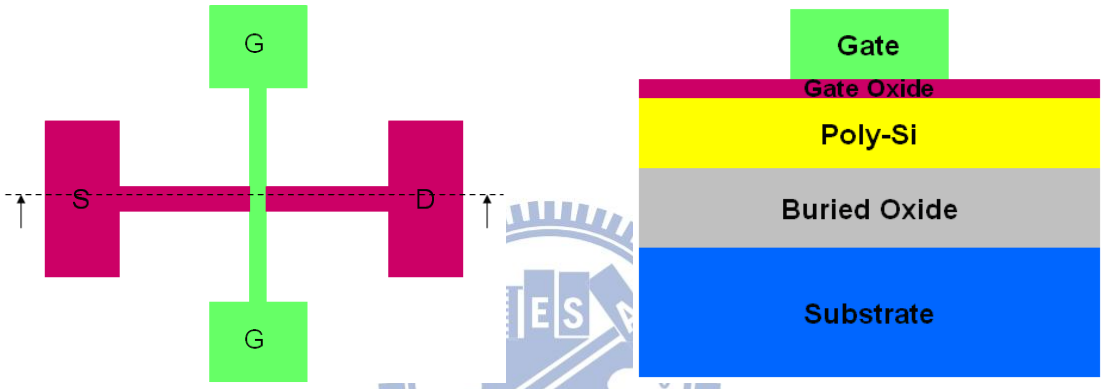


(h)

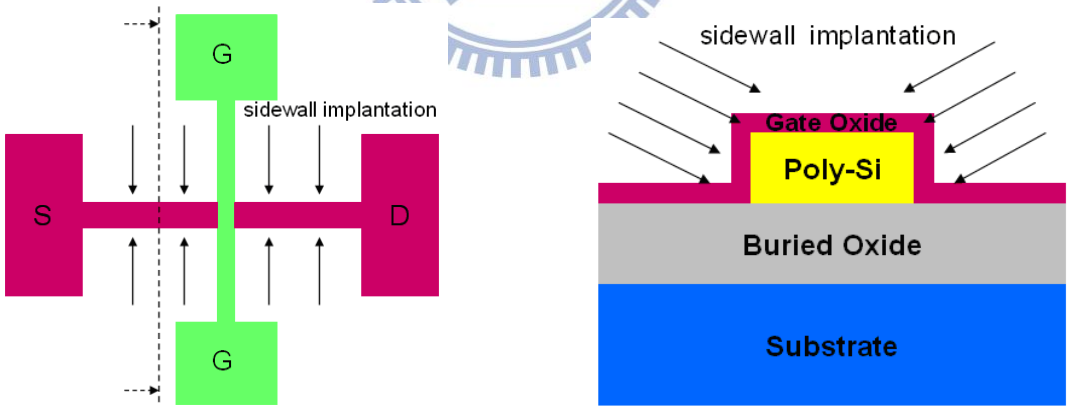
Fig. 2-1 (a)-(n) Process flow of p-channel FinFETs with double patterning technique. The left-hand-side figures are top views, and the right-hand-side figures are cross-sectional views.



(i)

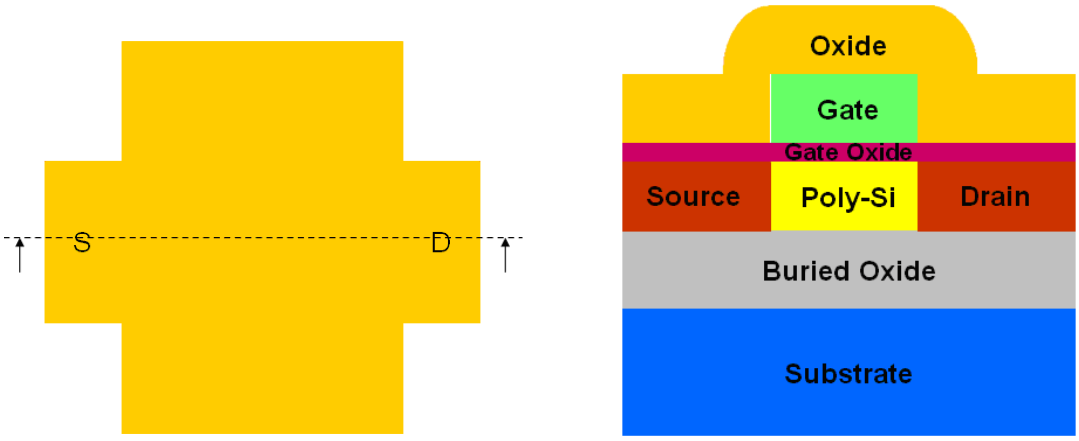


(j)

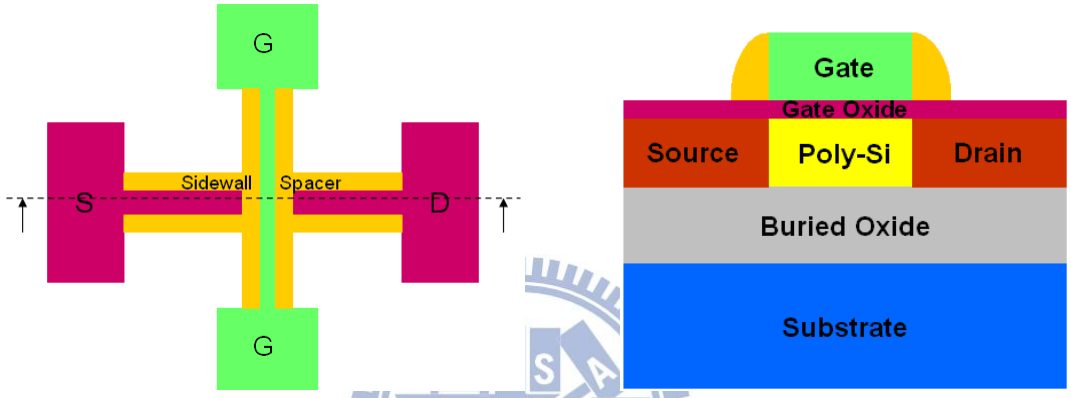


(k)

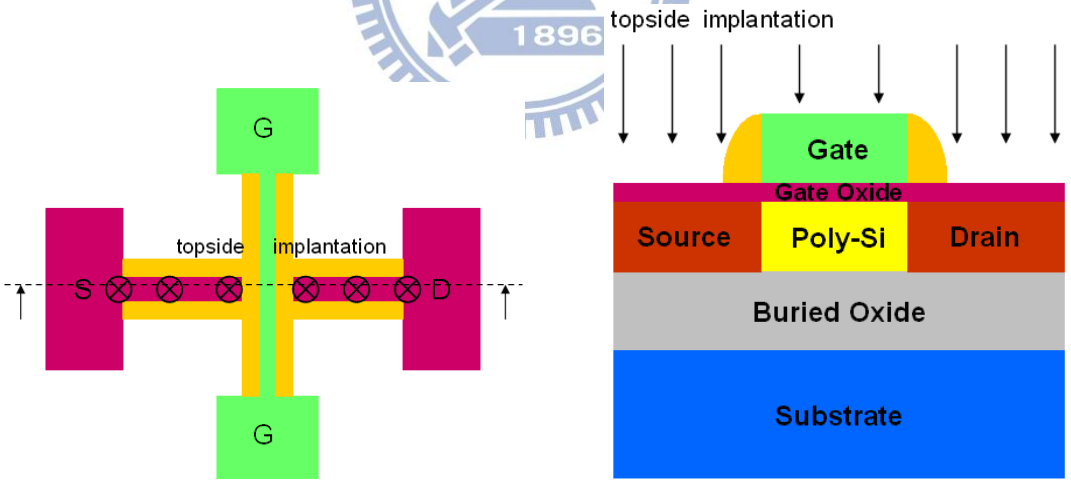
Fig. 2-1 (a)-(n) Process flow of p-channel FinFETs with double patterning technique. The left-hand-side figures are top views, and the right-hand-side figures are cross-sectional views.



(l)



(m)



(n)

Fig. 2-1 (a)-(n) Process flow of p-channel FinFETs with double patterning technique. The left-hand-side figures are top views, and the right-hand-side figures are cross-sectional views.

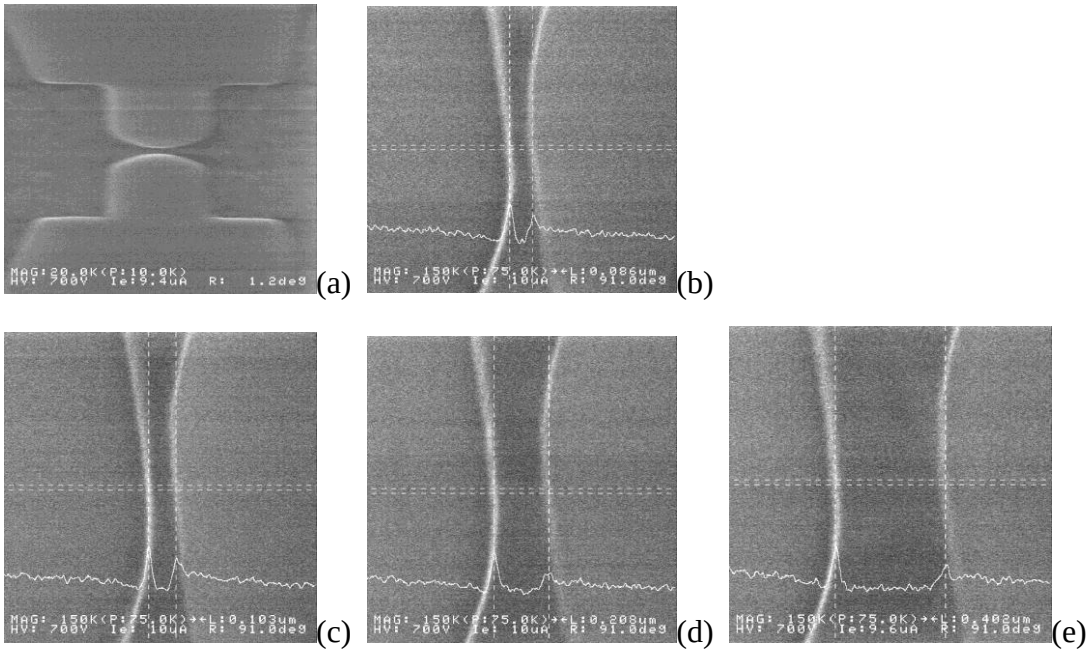


Fig. 2-2 (a) In-line SEM images of a fabricated device after definition of the poly-Si fin channel with a DP process. Enlarged views of measured (designed) dimension of patterned fins of (b) 86nm (80nm), (c) 103nm (100nm), (d) 208nm (200nm), and (e) 402nm (400nm).

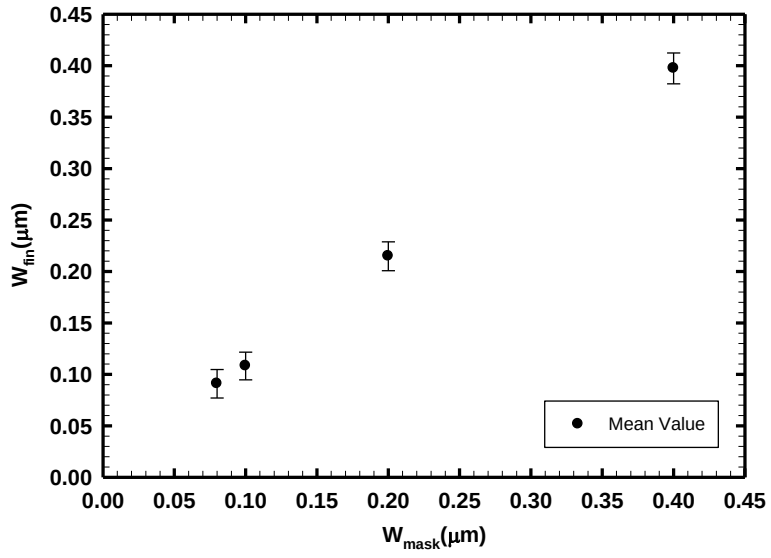


Fig. 2-3 Practical fin width (W_{fin}) extracted by in-line SEM versus the designed fin width (W_{mask}). The error bar is the standard deviation (1-σ) of the measured data.

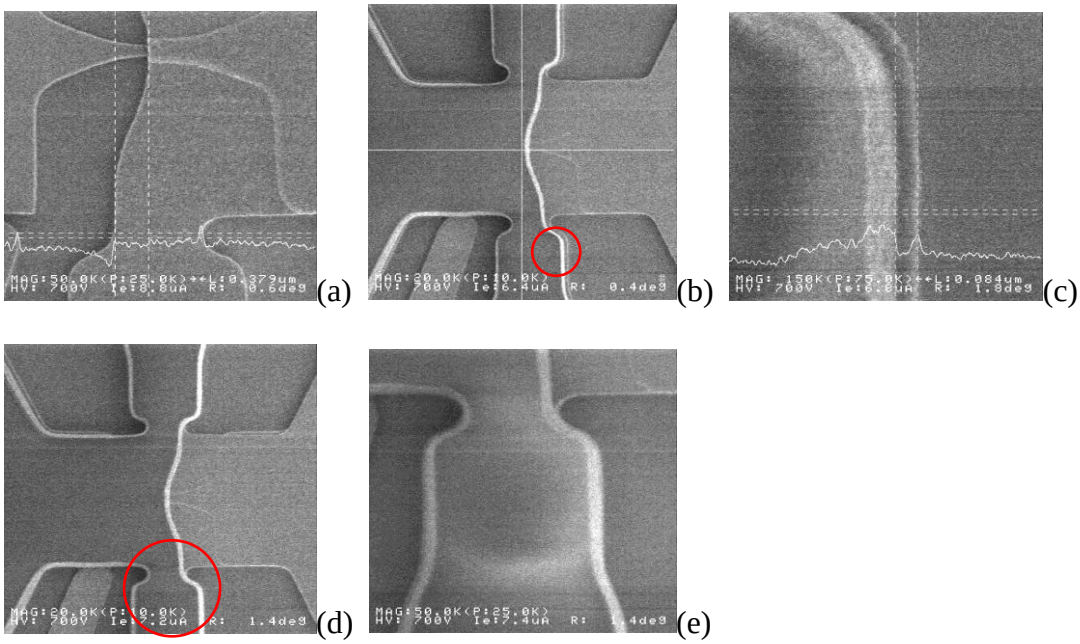


Fig. 2-4 In-line SEM images of fabricated gate structures. (a) After etching of poly-Si with photoresist (PR) patterns generated by G1 mask. (b) The PR pattern generated by the G2 mask and (c) an enlarged view of the circled region in (b) showing a significant misalignment. (d) The PR pattern generated by the G2 mask after calibrating the wafer stage and (e) an enlarged view of the circled region in (d) showing negligible misalignment.

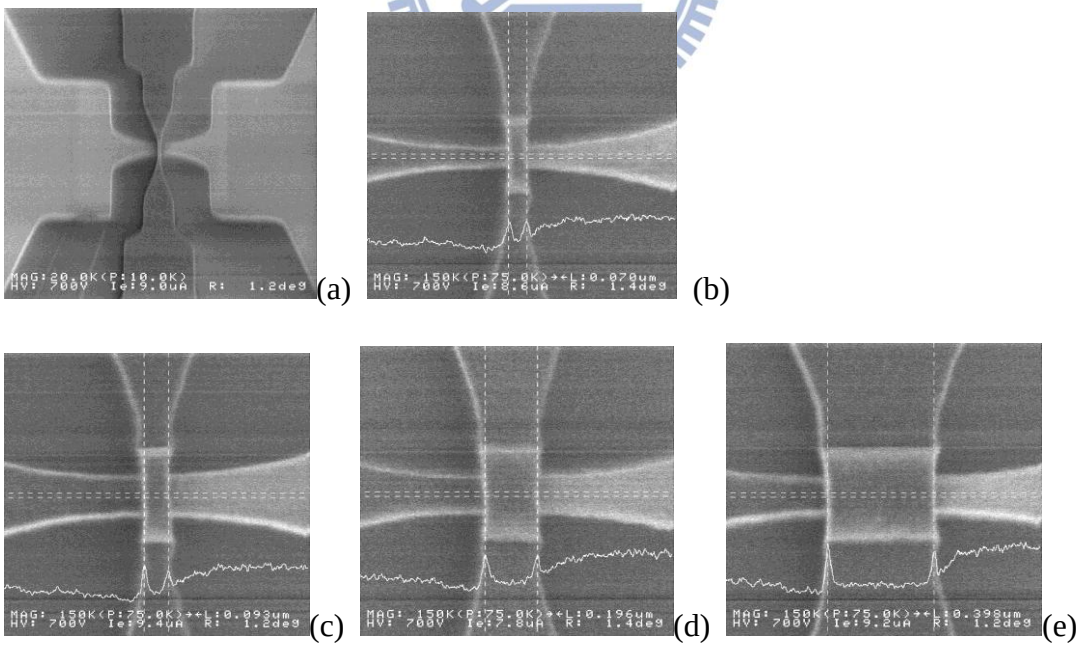


Fig. 2-5 (a) In-line SEM images of a fabricated device after definition of the poly-Si gate with a DP process. Enlarged views of measured (designed) dimension of patterned gates of (b) 70nm (80nm), (c) 93nm (100nm), (d) 196nm (200nm), and (e) 398 (400nm).

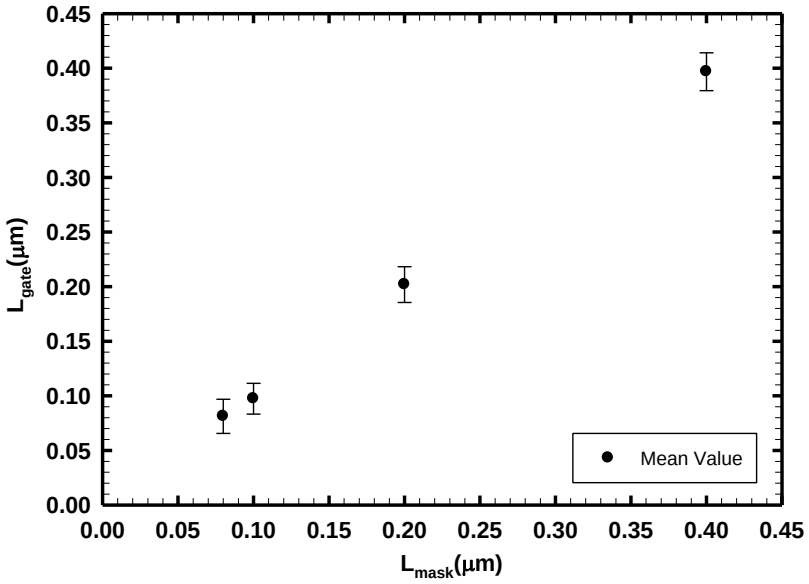


Fig. 2-6 Practical gate length (L_{gate}) extracted by in-line SEM versus the designed gate length (L_{mask}). The error bar is the standard deviation (1-σ) of the measured data.

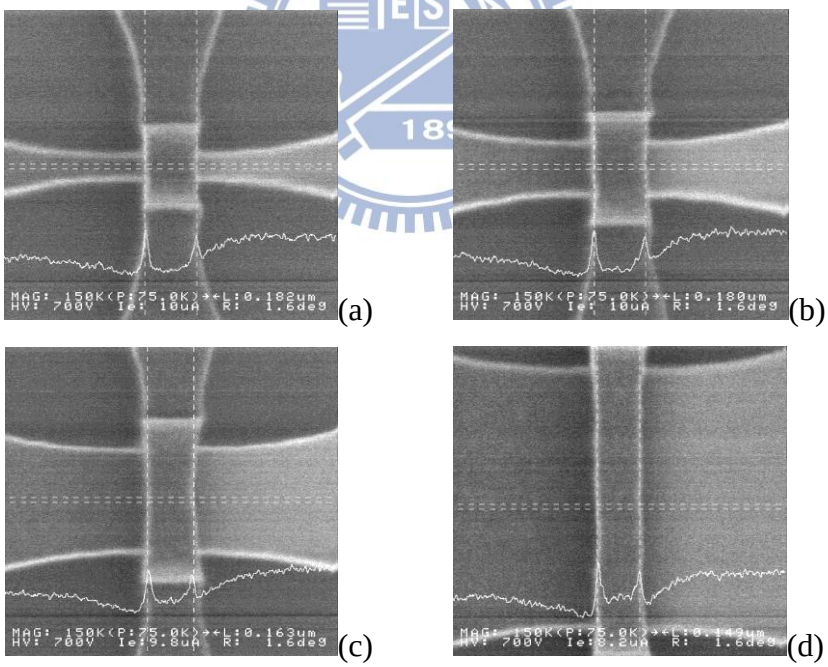


Fig. 2-7 Measured gate lengths (L_{gate}) of the gate with designed gate lengths (L_{mask}) of 200 nm varies with the widths of the fin channel (W_{fin}). (a) W_{fin} 80nm, L_{gate} 182nm, (b) W_{fin} 200nm, L_{gate} 180nm, (c) W_{fin} 400nm, L_{gate} 163nm, and (d)W_{fin} 1000nm, L_{gate} 149nm.

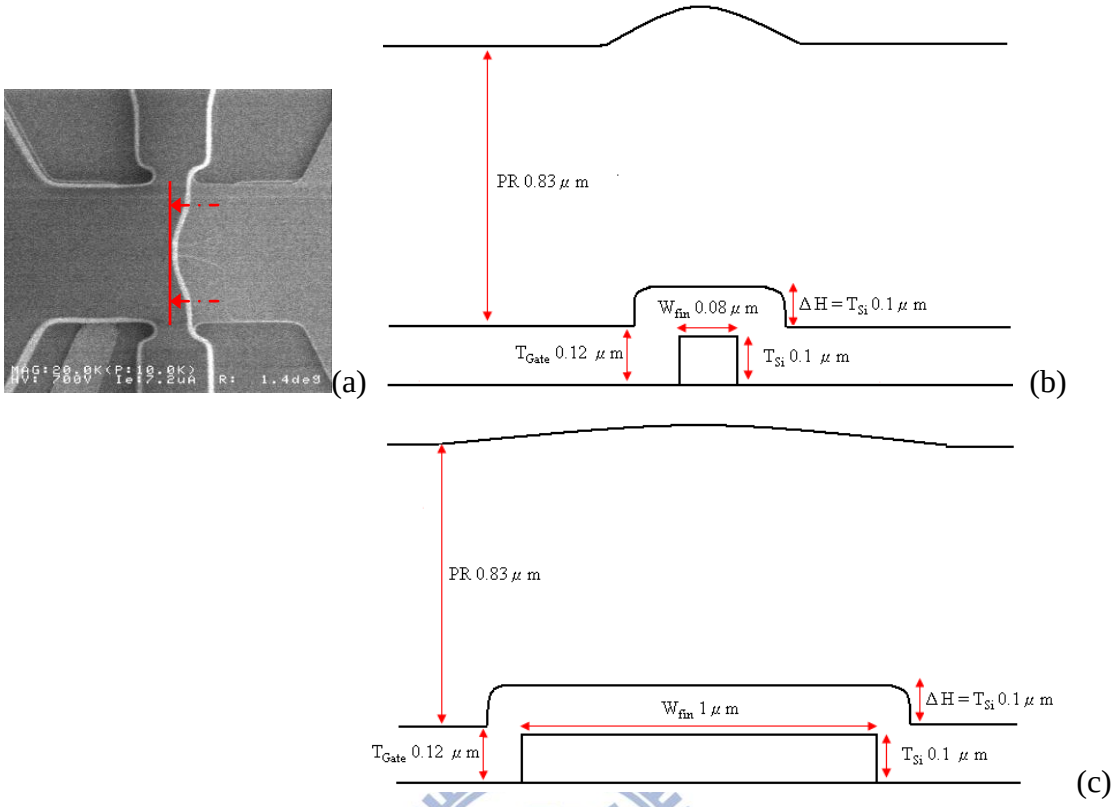


Fig. 2-8 Surface morphology of the PR spun on the gate lying over the channel of various widths. (a) An example showing the top view of the PR pattern generated with the G2 lithography process. The red line indicates the overlapped region of the PR patterns (left side) and the remained poly-Si defined by G1 mask (right side). (b) and (c) are the cross-sectional views of the surface morphology of red line in (a) with different channel widths. (c) The thicker channel width causes a thinner PR during the action of spinning.

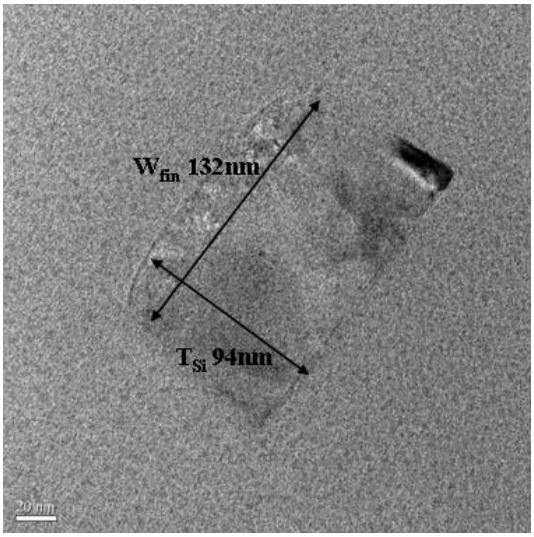


Fig. 2-9 Cross-section TEM graphs of ELA poly-Si channel with designed W_{mask} = T_{Si} = 100nm. Practical fin widths (W_{fin}) and channel thickness (T_{Si}) were measured to be 132nm and 94nm, respectively.

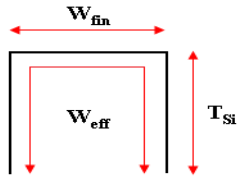
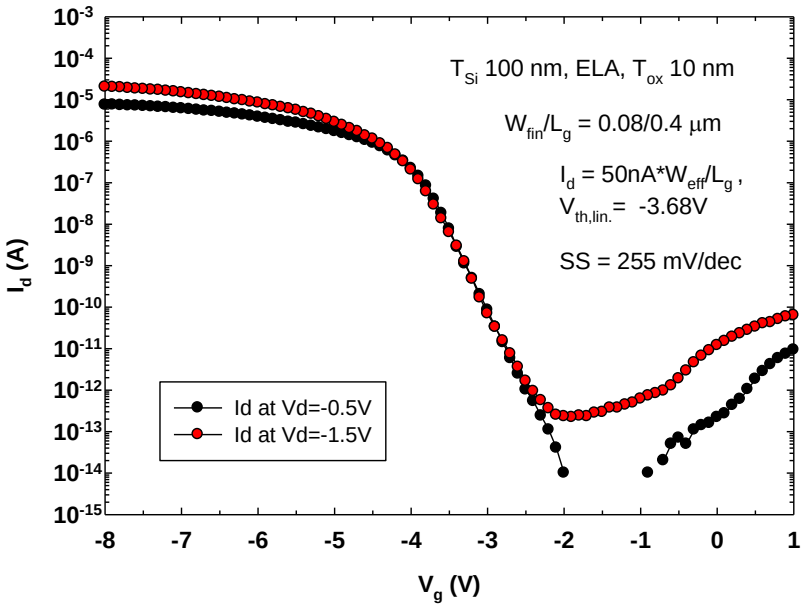
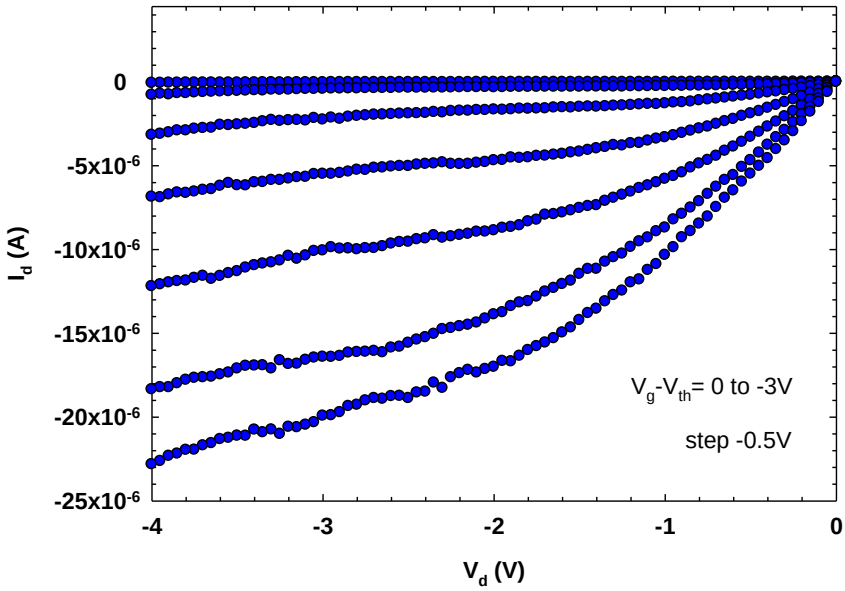


Fig. 3-1 The effective conduction width ($W_{eff} = W_{fin} + 2\times T_{Si}$) of a channel.

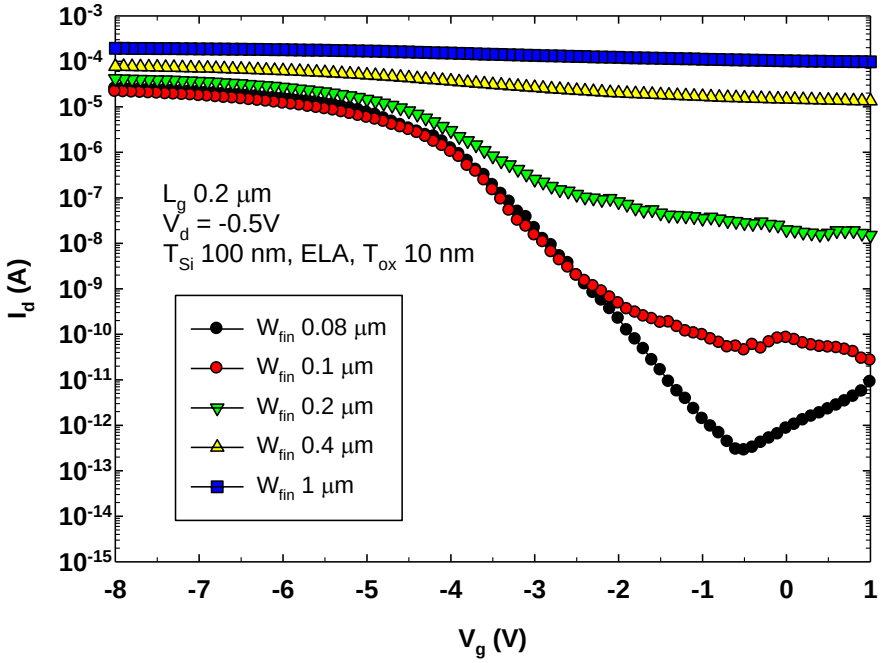


(a)

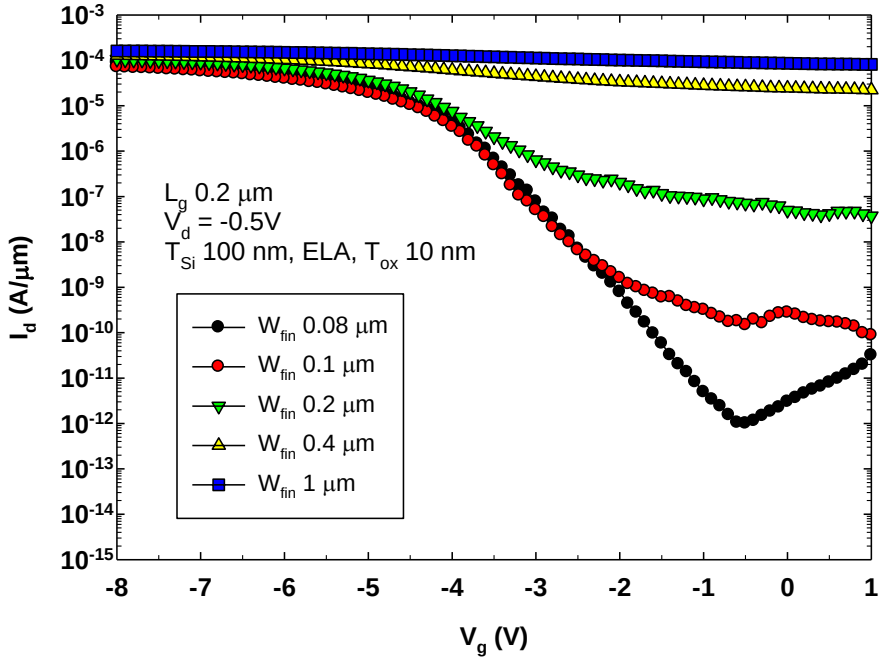


(b)

Fig. 3-2 Electrical characteristics of (a) I_d-V_g and (b) I_d-V_d with fin width of 0.08μm and gate length of 0.4μm.

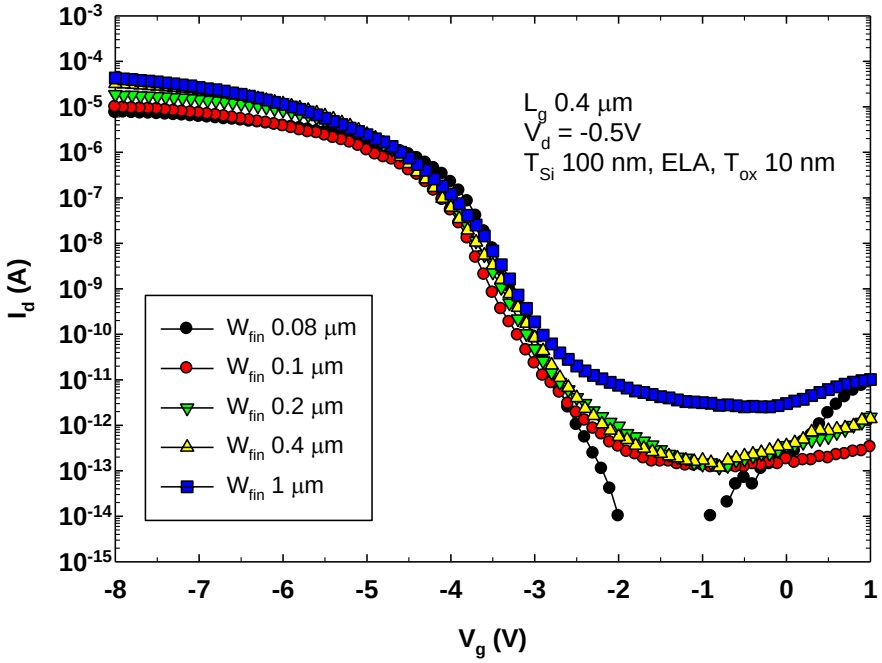


(a)

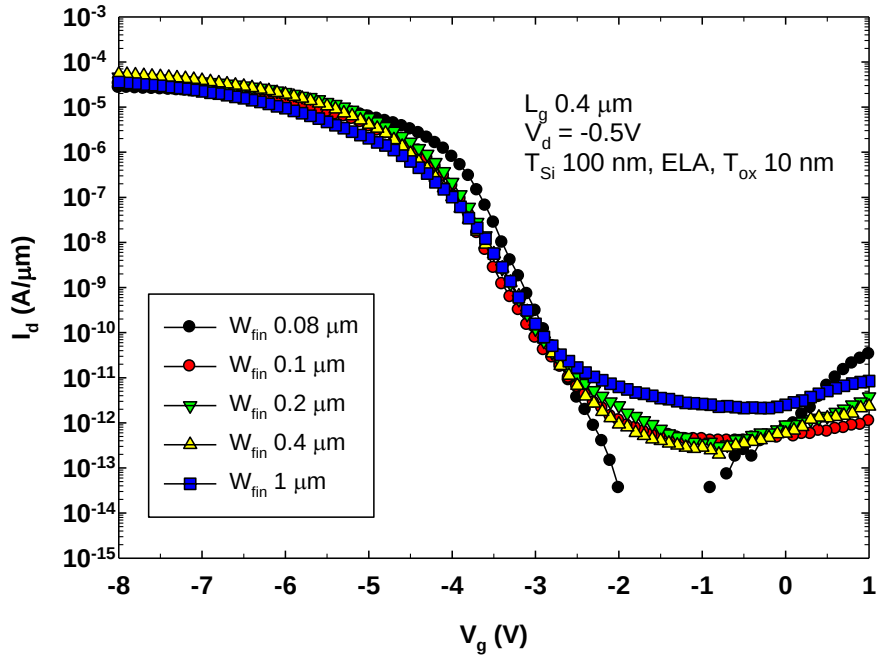


(b)

Fig. 3-3 Transfer characteristics of devices with gate length of 0.2μm and various fin widths (W_{fin}) ranging from 0.08 to 1μm, (a) un-normalized drain current , and (b) drain current normalized to the effective fin widths (W_{eff}).

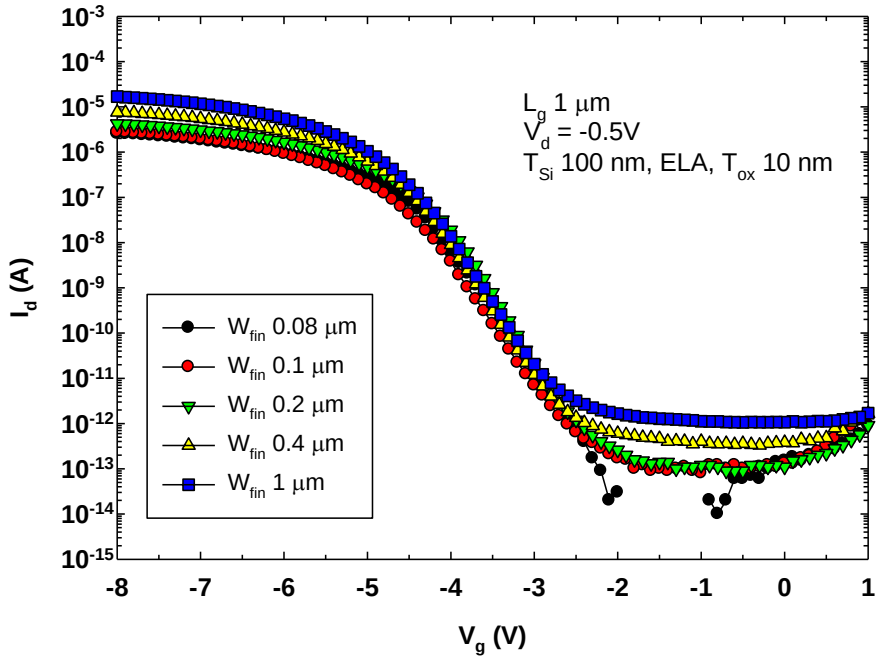


(a)

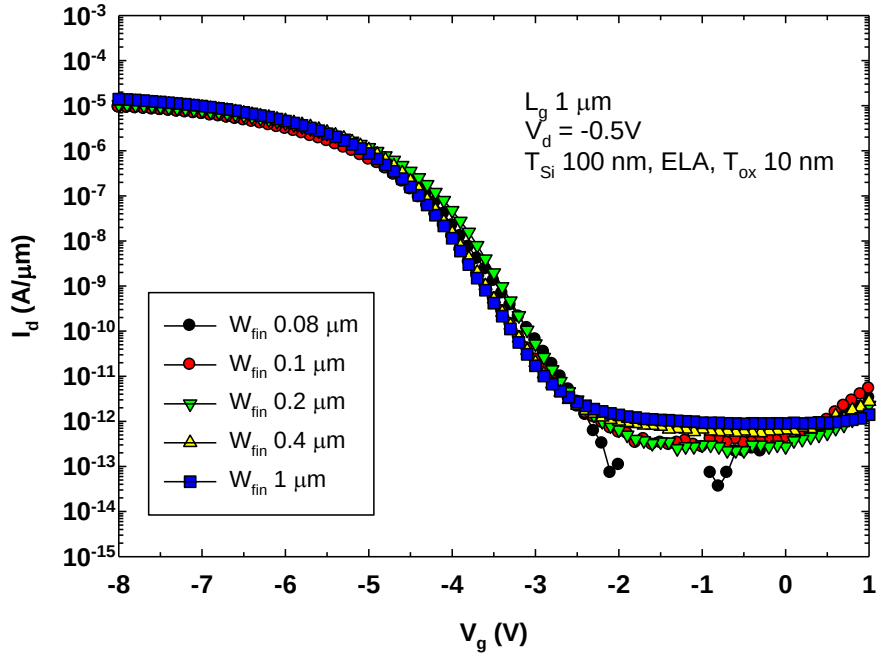


(b)

Fig. 3-4 Transfer characteristics of devices with gate length of 0.4μm and various fin widths (W_{fin}) ranging from 0.08 to 1μm, (a) un-normalized drain current , and (b) drain current normalized to the effective fin widths (W_{eff}).



(a)



(b)

Fig. 3-5 Transfer characteristics of devices with gate length of 1μm and various fin widths (W_{fin}) ranging from 0.08 to 1μm, (a) un-normalized drain current , and (b) drain current normalized to the effective widths (W_{eff}).

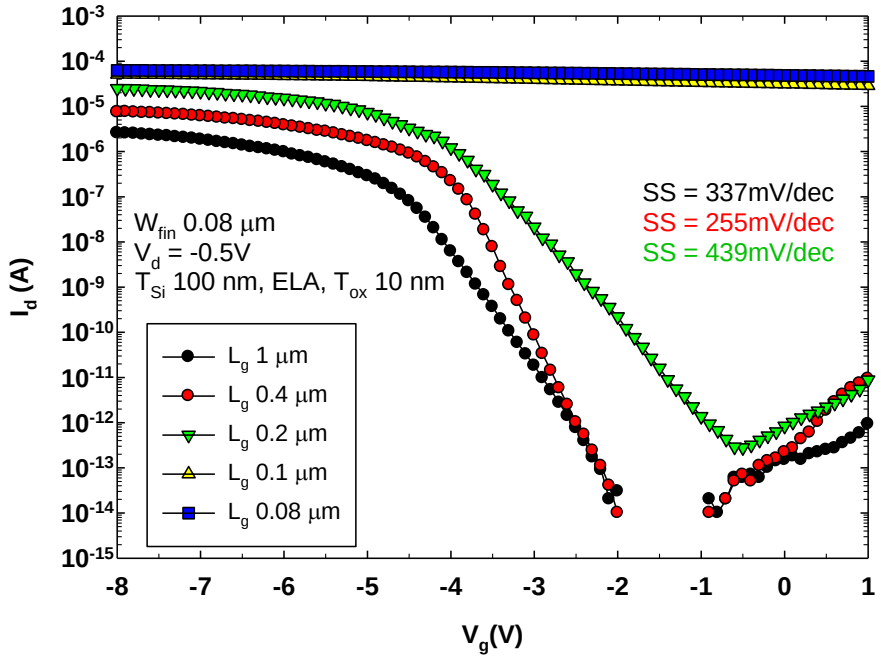


Fig. 3-6 Transfer characteristics of devices with same fin width of 0.08μm and various gate lengths ranging from 1 to 0.08μm.

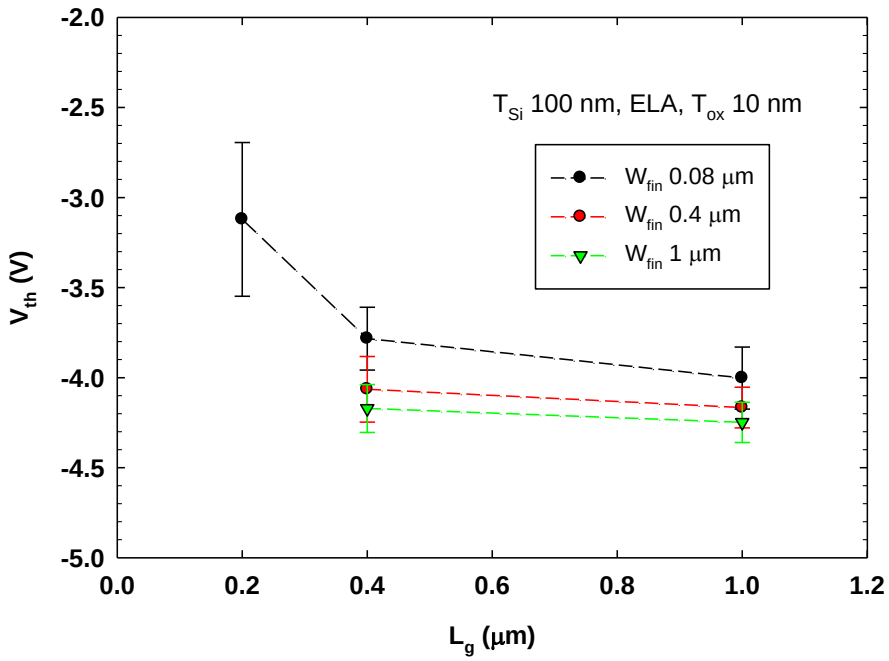


Fig. 3-7 Mean value and standard deviation of threshold voltage (V_{th}) as a function of the channel length for devices with various W_{fin}.

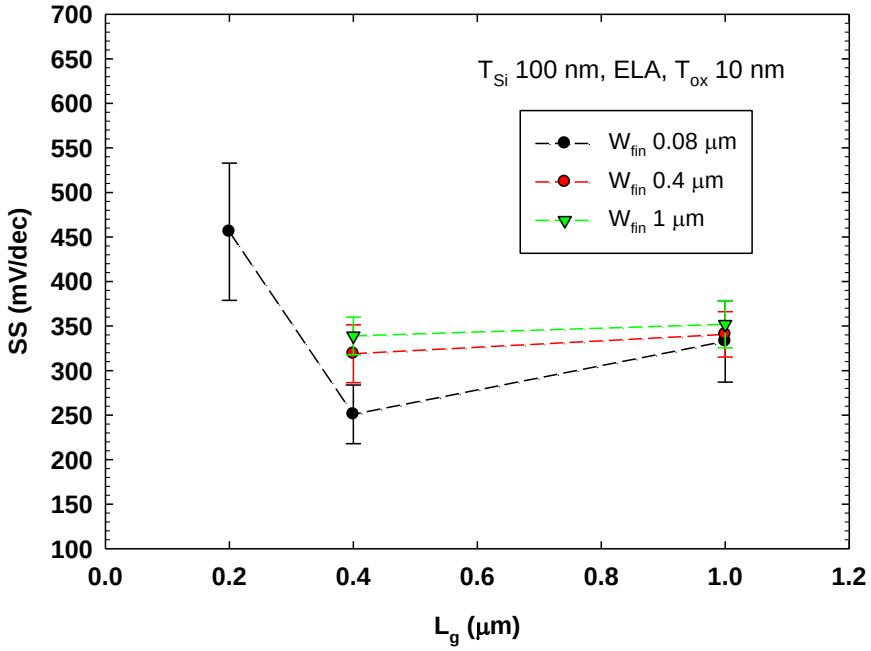


Fig. 3-8 Mean value and standard deviation of subthreshold swing (SS) as a function of channel length for p-FinFETs.

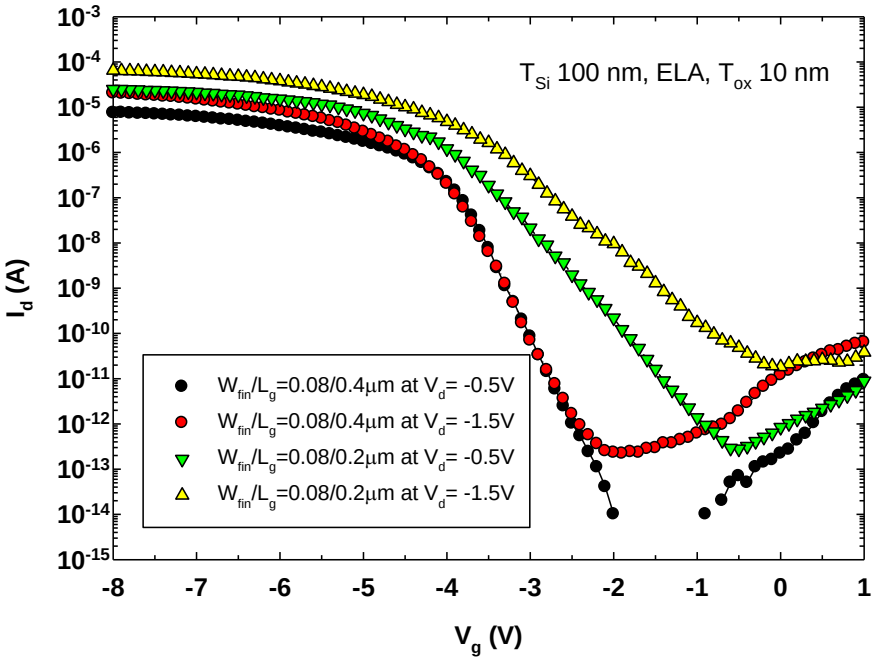


Fig. 3-9 Transfer characteristics for devices with channel lengths of 0.4 and 0.2μm.

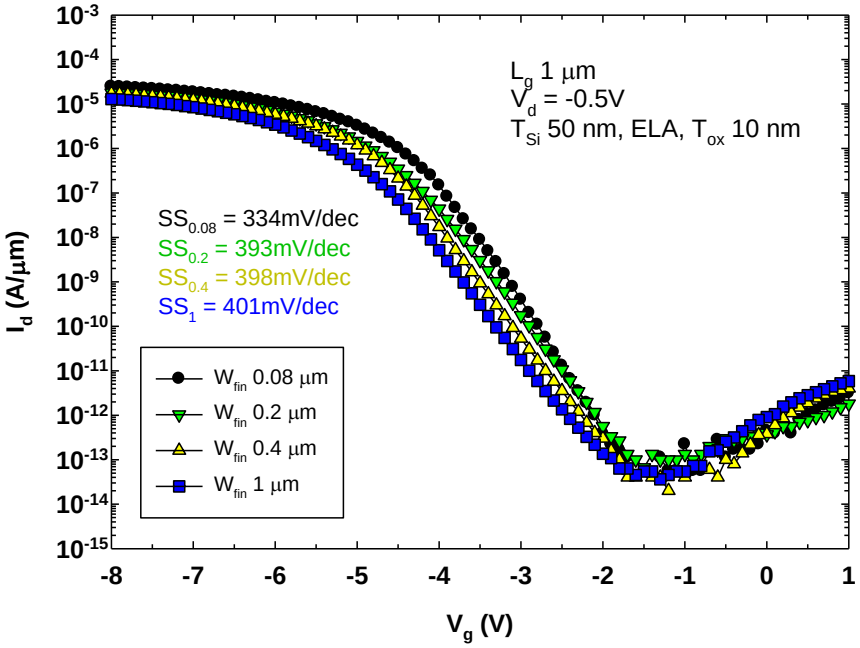


Fig. 3-10 Typical transfer characteristics of devices with gate length of 1μm and various fin widths (W_{fin}) ranging from 0.08 to 1μm. The drain current is normalized to the effective fin widths (W_{eff}).

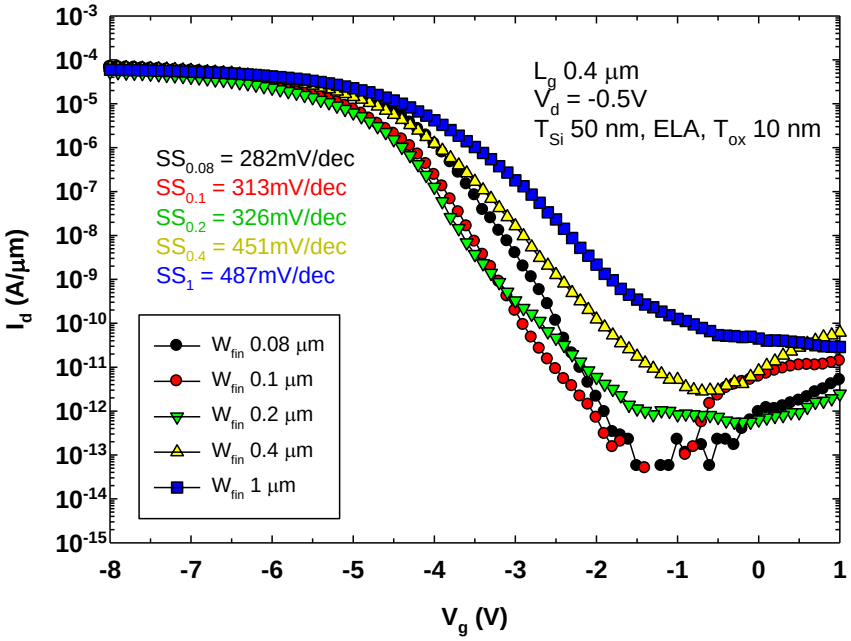


Fig. 3-11 Typical transfer characteristics of devices with gate length of 0.4μm and various fin widths (W_{fin}) ranging from 0.08 to 1μm. The drain current is normalized to the effective fin widths (W_{eff}).

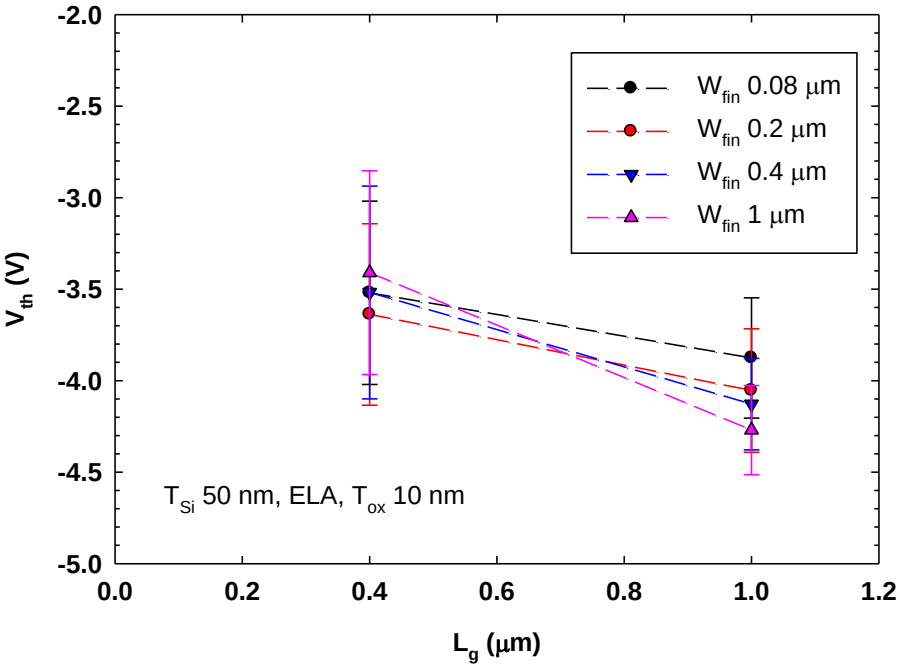


Fig. 3-12 Mean value and standard deviation of threshold voltage (V_{th}) as a function of the channel length for devices with various W_{fin}.

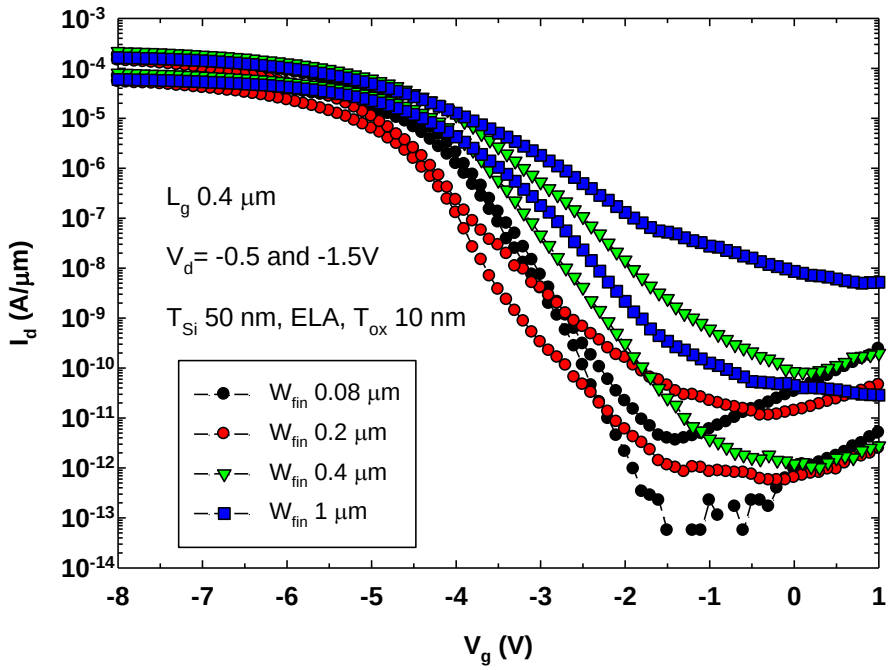


Fig. 3-13 Typical transfer characteristics of devices measured at V_d = -0.5 and -1.5 V with gate length of 0.4μm and fin widths (W_{fin}) ranging from 0.08 to 1μm.

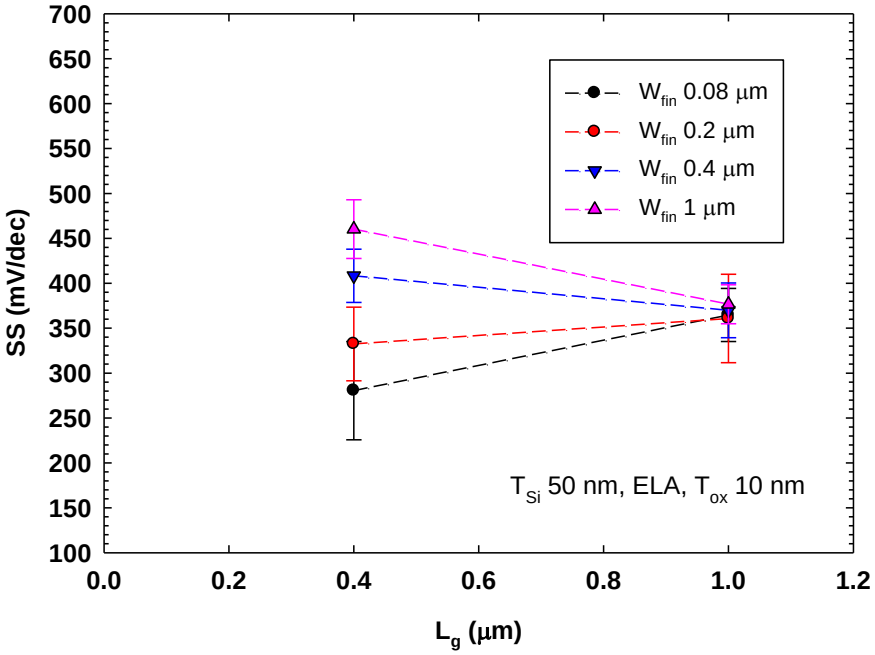
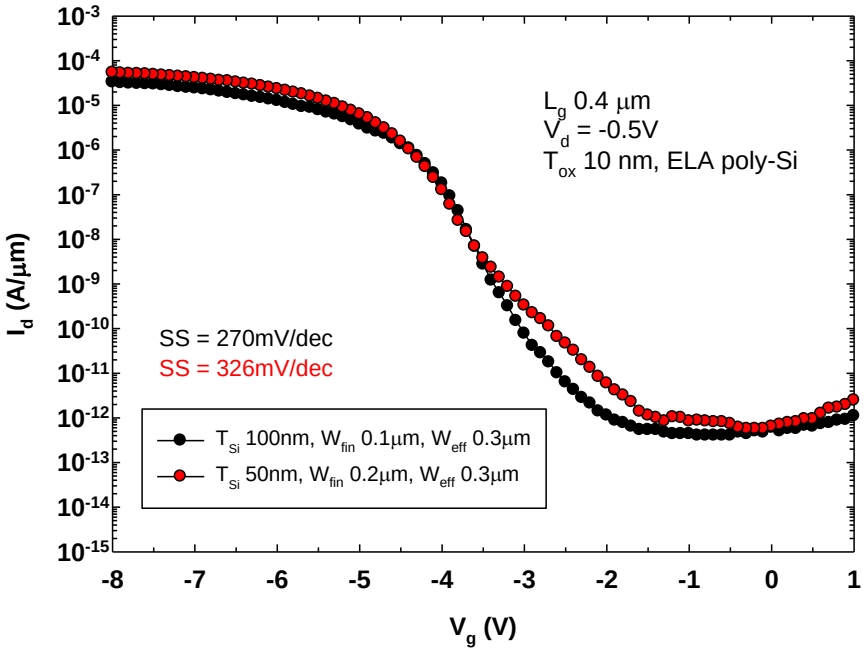
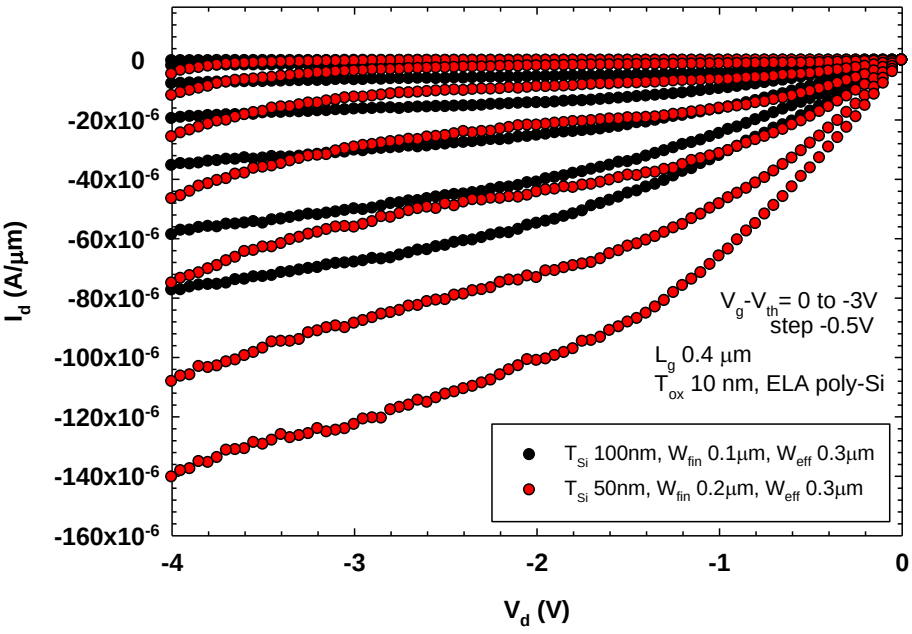


Fig. 3-14 Mean value and standard deviation of subthreshold swing (SS) as a function of channel length.



(a)



(b)

Fig. 3-15 Electrical characteristics of (a) I_d-V_g and (b) I_d-V_d for devices with the same effective fin width (W_{eff}) but different T_{Si} and W_{fin}.

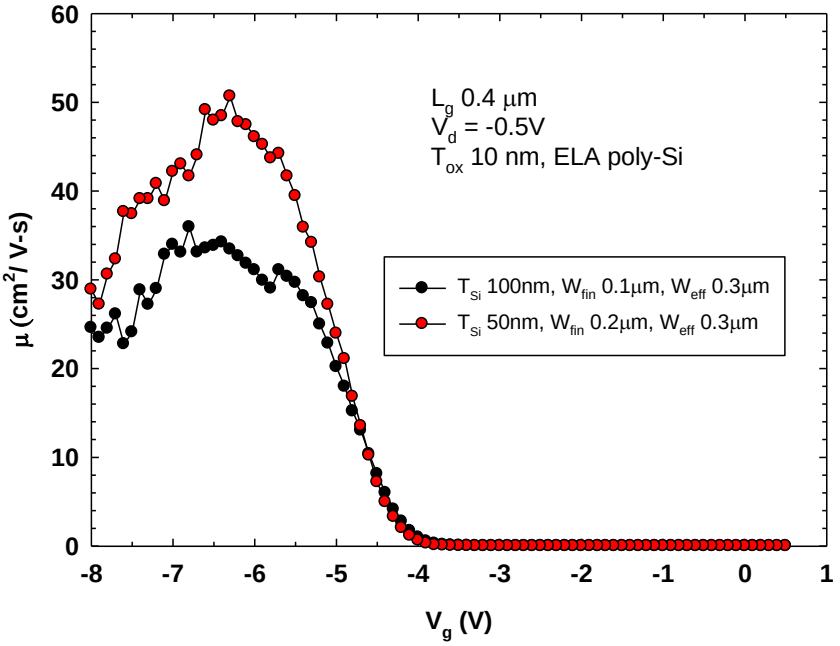


Fig. 3-16 Mobility of the devices characterized in Fig. 3-15.

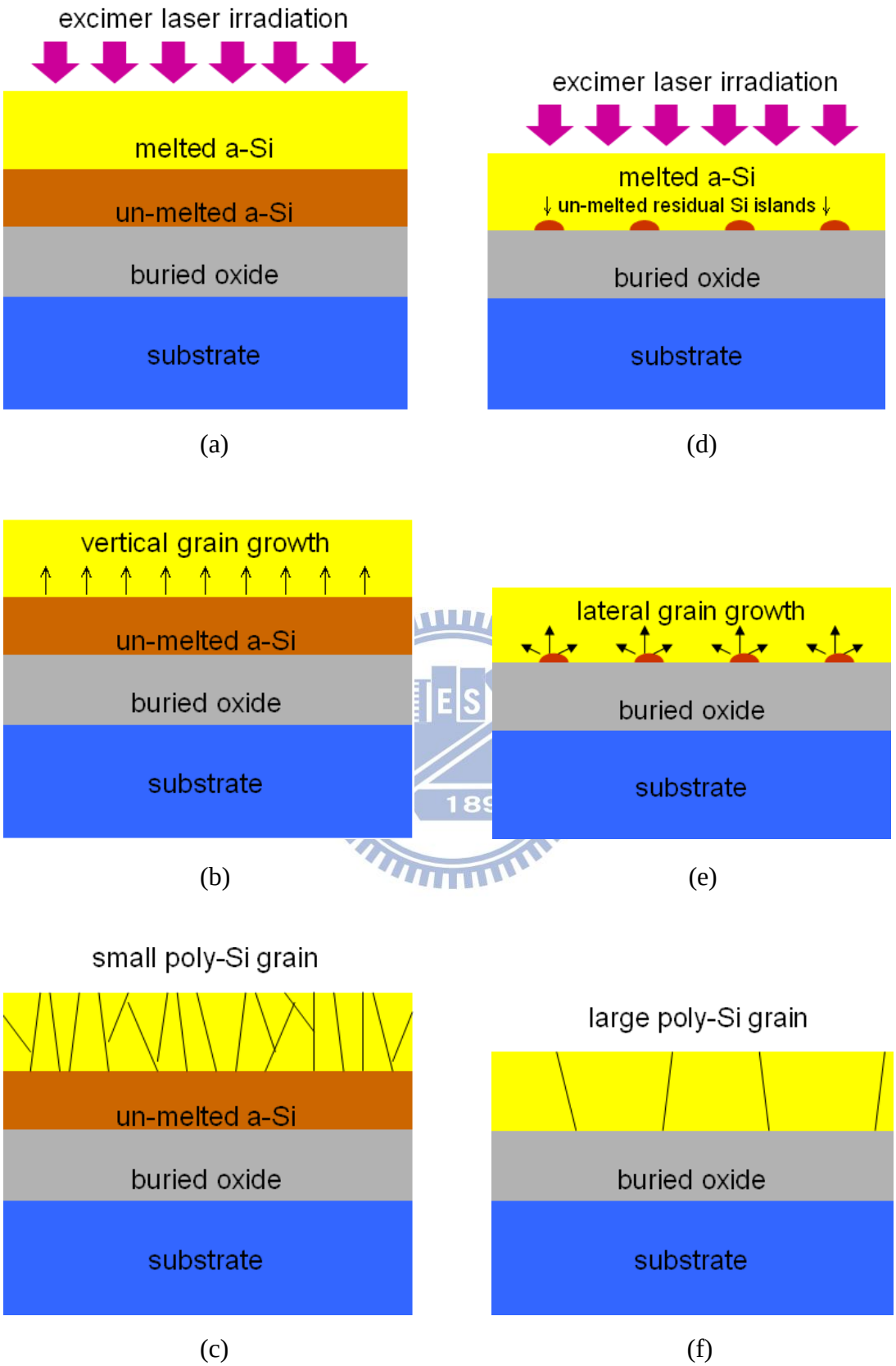
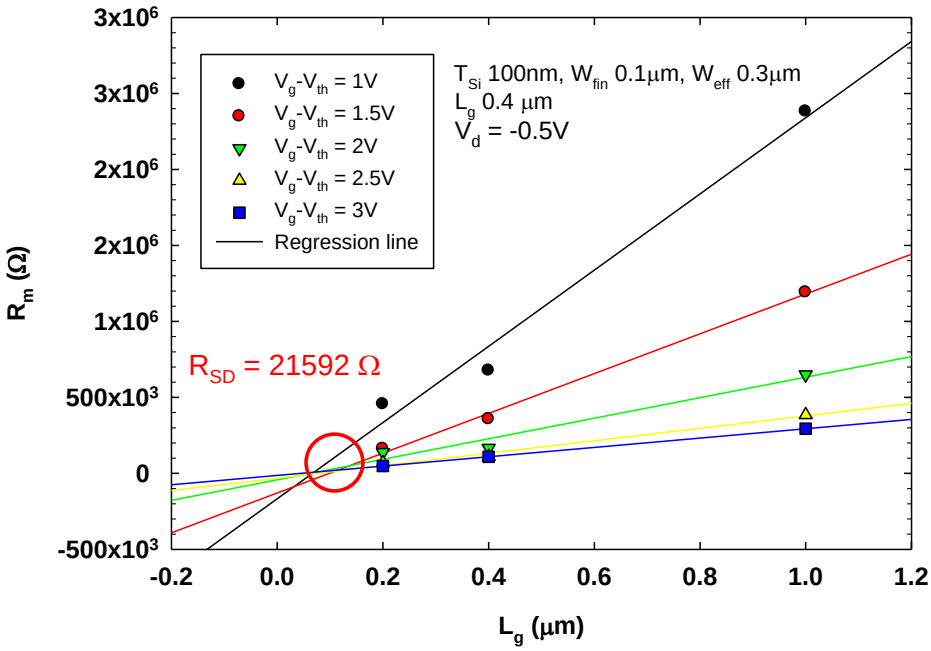
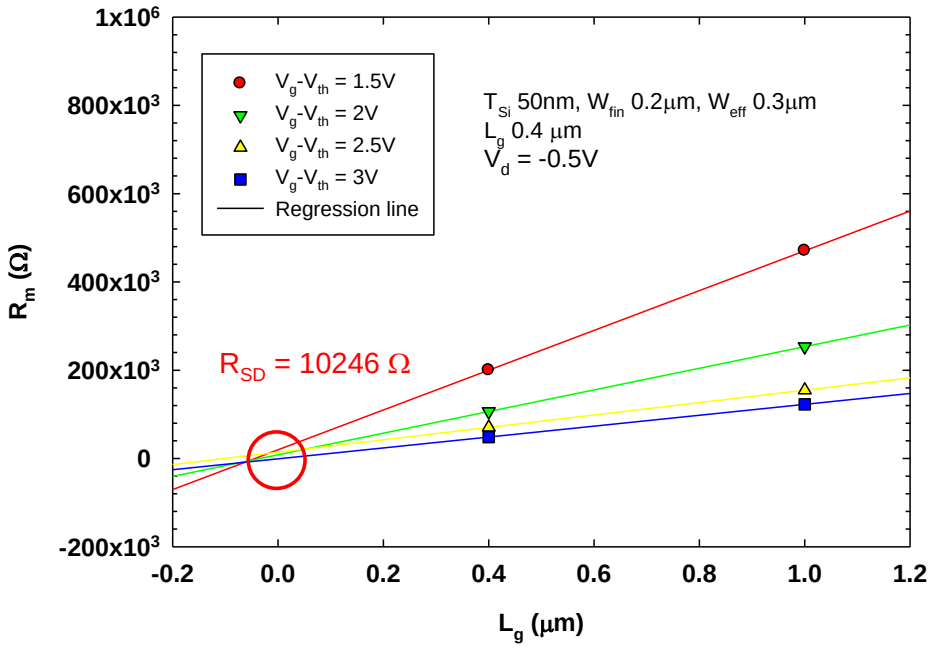


Fig. 3-17 Re-crystallization schemes as the a-Si film is irradiated with excimer laser irradiation. (a)-(c) are partial-melting process occurring in a thicker film, and (d)-(f) are near-complete-melting process occurring in a thinner film.



(a)



(b)

Fig. 3-18 Measured series resistance (R_m) and the extracted source/drain resistance (R_{SD}) of the devices with different channel thickness (T_{Si}) of (a) 100nm and (b) 50nm.

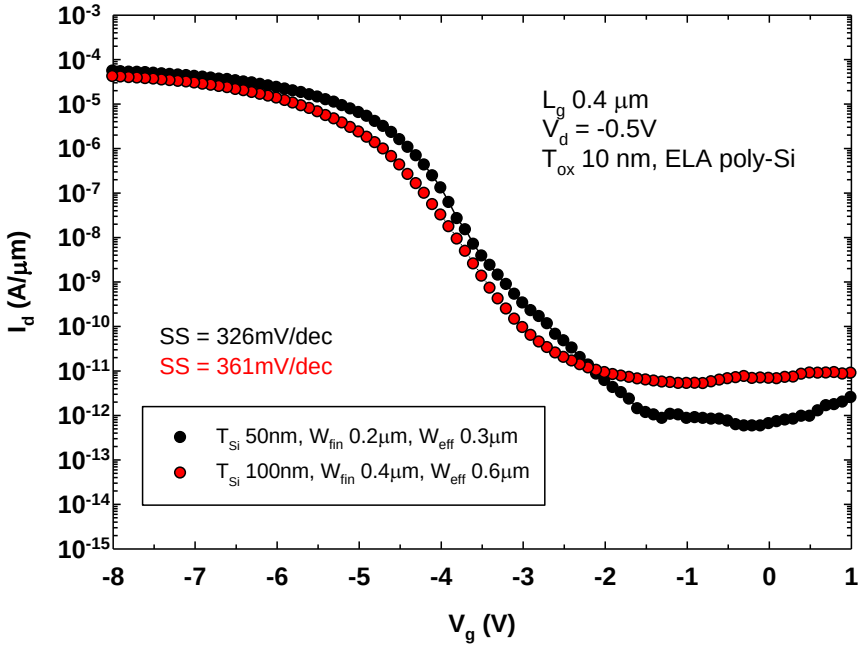
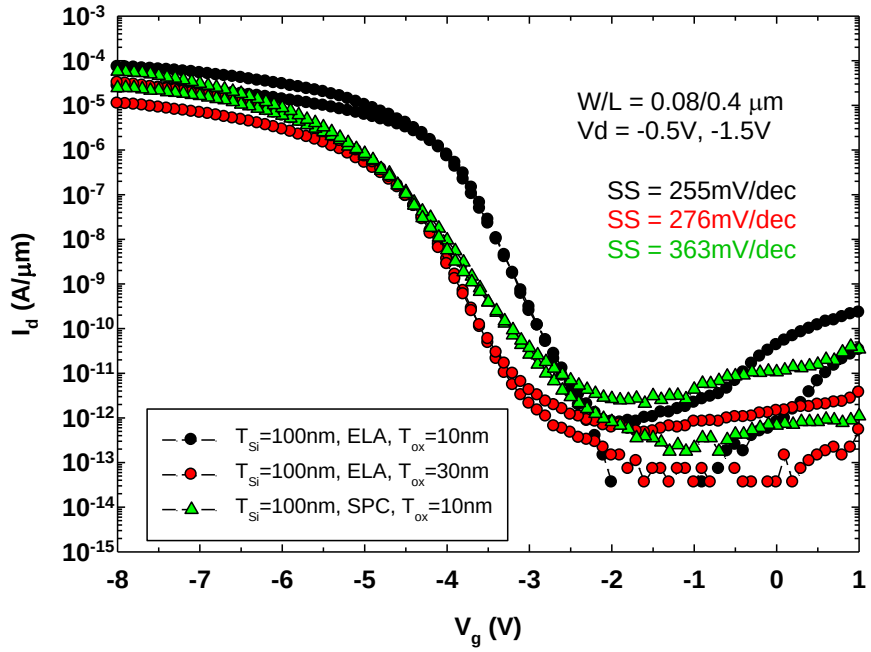
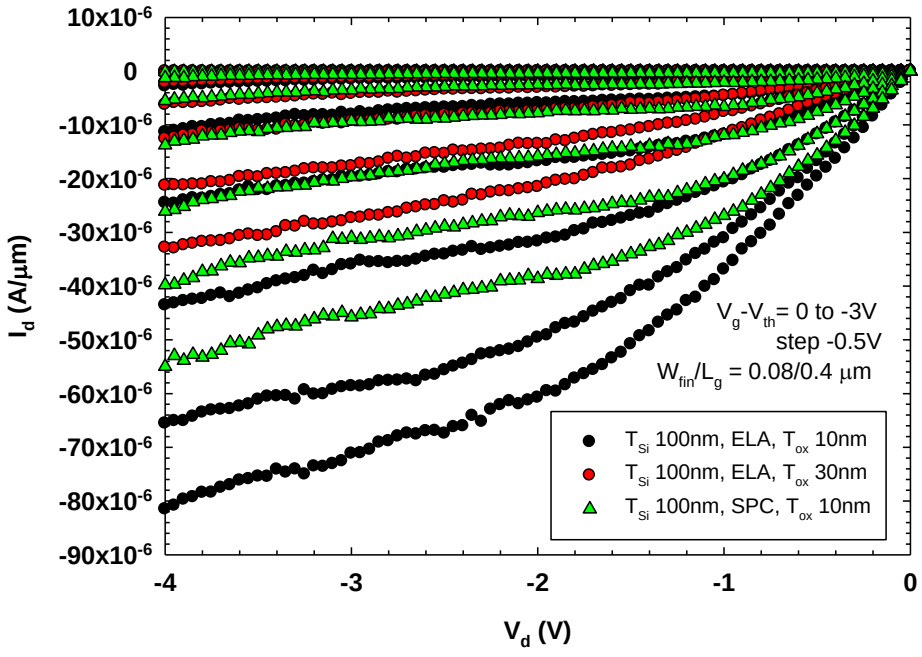


Fig. 3-19 Transfer characteristics for devices with W_{eff} of 0.3 and 0.6μm and L_g = 0.4μm.



(a)



(b)

Fig. 3-20 Electrical characteristics of (a) I_d-V_g and (b) I_d-V_d for SPC and ELA devices.

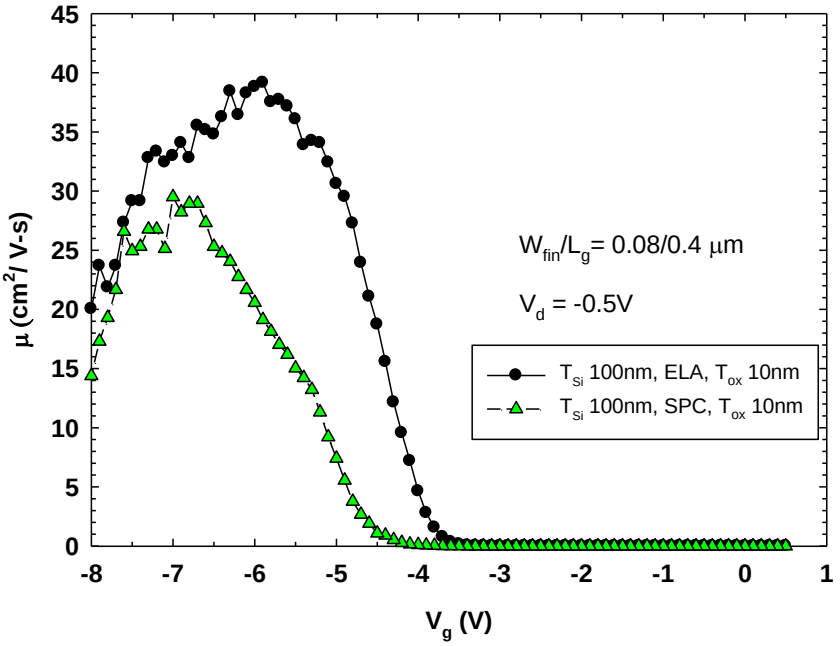


Fig. 3-21 Mobility of the SPC and ELA devices.

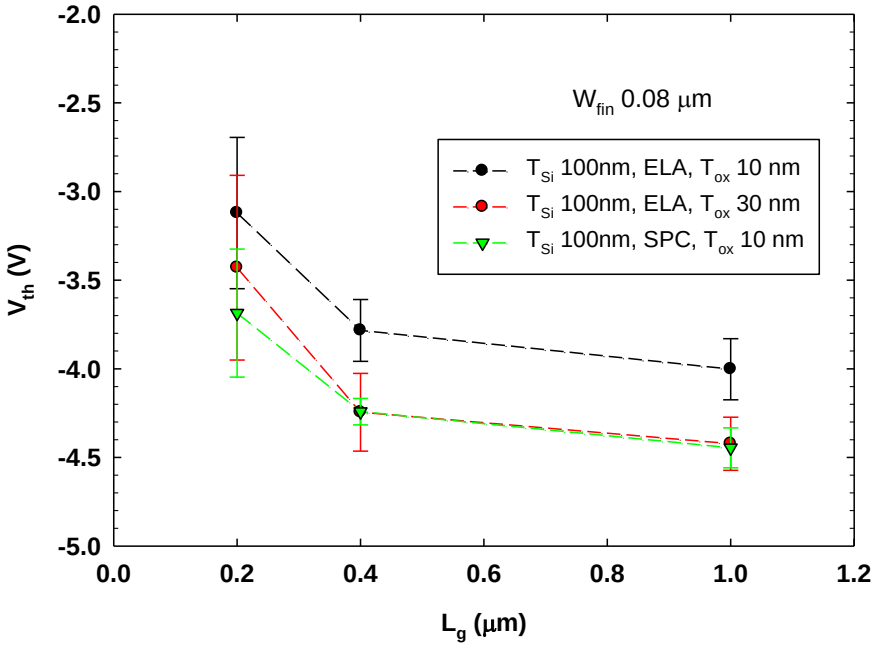


Fig. 3-22 Mean value and standard deviation of threshold voltage (V_{th}) as a function of the channel length for the SPC and ELA devices with W_{fin} of 80nm.

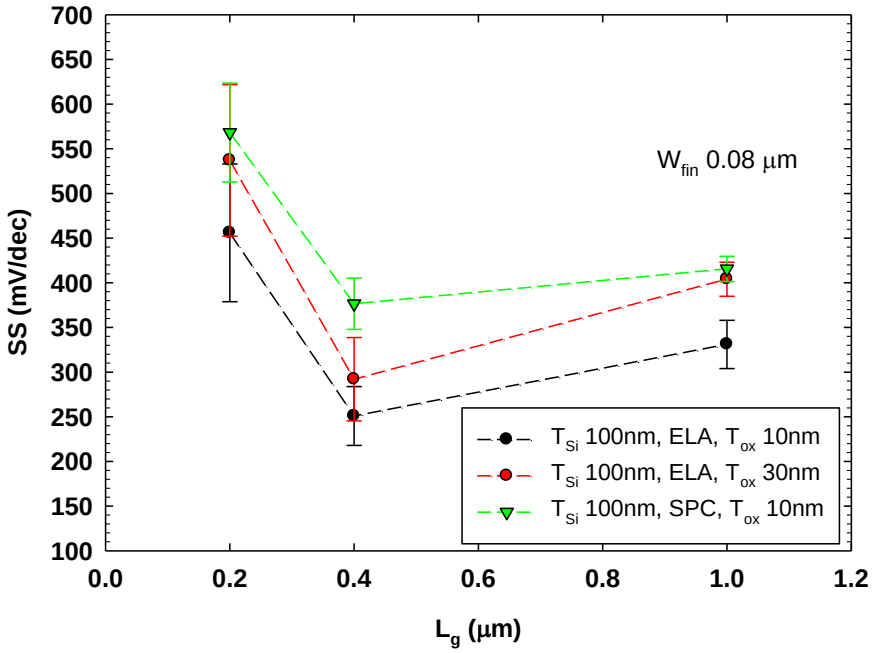


Fig. 3-23 Mean value and standard deviation of subthreshold swing (SS) as a function of channel length for the SPC and ELA devices with W_{fin} of 80nm.

Tables:

Table 2-1 Split conditions of channel thickness (T_{Si}) and oxide thickness (T_{ox}) for ELA and SPC FinFETs.

ELA	●	●	●	
SPC				●
T_{Si} 50nm	■			
T_{Si} 100nm		■	■	■
T_{ox} 10nm	▲	▲		▲
T_{ox} 30nm			▲	

Table 2-2 Dimensions of designed gate length (L_{mask}) and fin width (W_{mask}) with double patterning process.

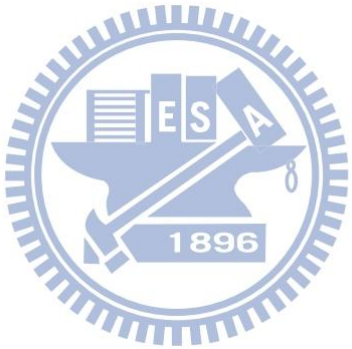
W_{mask} (μm) \ L_{mask} (μm)	0.08	0.1	0.2	0.4	1
0.08	●	●	●	●	●
0.1	●	●	●	●	●
0.2	●	●	●	●	●
0.4	●	●	●	●	●
1	●	●	●	●	●

Table 2-3 Specifications of the Canon FPA-3000i5+ Stepper.

Resolution	0.35 micron (dense lines)
NA	0.63-0.45 (automatically variable)
Reticle Size	5-inch
Reduction Ration	5:1
Field Size	20 mm x 20 mm
Overlay Accuracy	Mean + 3sigma ≦ 45 nm
Throughput	100 wph (200 mm)

Table 2-4 Measured gate lengths (L_{gate}) of various designed dimension on fin channel of various widths (W_{fin}). The data were measured from structures located in the same die with chan nel thickness of 100 nm.

W_{fin} (nm)	80	200	400	1000
L_{gate} (nm) of L_{mask} 80 nm	79	67	58	42
L_{gate} (nm) of L_{mask} 200 nm	182	180	163	149
L_{gate} (nm) of L_{mask} 400 nm	379	358	355	353



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論文題目：利用雙重微影成像法製作多晶矽鰭式場效電晶體元件之特性研究

A Study on the Device Characteristics of Polycrystalline Silicon FinFETs Fabricated with Double Patterning Technique

Publication List

[1] **H. Y. Chou**, C. I Lin, H. C. Lin, and T. Y. Huang, "Fabrication of Poly-Si FinFETs with I-line Double Patterning Technique," *Symp. on Nano Device Technology (SNDT)*, ND-22, pp.38, 2012. **(Excellence Award)**

[2] **H. Y. Chou**, C. I Lin, H. C. Lin, and T. Y. Huang, "Fabrication of Poly-Si FinFETs with I-line Double Patterning Technique (利用I-line雙重微影成像法製作多晶矽鰭式場效電晶體(FinFET))," *Nano Communication (奈米通訊)*, vol. 19, no. 2, pp.11-14, 2012.

[3] C. I Lin, **H. Y. Chou**, H. C. Lin, and T. Y. Huang, "Characteristics of P-Channel Polycrystalline Silicon FinFETs Fabricated with Double Patterning Technique," submitted to *Int. Electron Devices and Materials Symp.(IEDMS)*, 2012.