國立交通大學

電子工程學系 電子研究所碩士班

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利用低熱預算製程改善碳化矽電容介面能態密度

Improvement of 4H-SiC MIS Capacitor Interface State Density by Low Thermal Budget Processes

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摘要

碳化矽因為具有寬能隙以及高熱傳導係數，適合用來製作高功率元件。但是碳化矽的金氧半場效電晶體(MOSFET)的製作仍有很大的改善空間，如通道載子移動率的提升是個很重要的課題。氧化層與碳化矽基板之間的高介面能態密度(大於10^{12} cm^{-2})是造成低載子移動率的主因，且既有的閘極氧化層製程都需要1300以上的高溫氧化及退火，才能得到可接受的閘極氧化層。本論文研究利用低熱預算製程來降低介面能態密度，比較多種低熱預算製程對各項電性參數包含介面能態密度、介電層崩潰電場分布的影響，並探討不同的製程條件與介面能態密度的關係。

我們利用直接低溫(1050 ℃)濕氧氧化的條件當作本論文介面能態密度的參考上限，理論上氧化厚度越薄介面能態密度越小，研究發現濕氧30分鐘介面能態密度就達到飽和，原因是溫度不夠高使得一氧化碳(CO)不容易擴散到氧化層表面。高溫(1300 ℃)一氧化二氮直接氧化的條件做為本論文介面能態密度的參考目標。在距離導帶(conduction band) 0.4 eV的介面能態密度，低溫濕氧大約是$5x10^{11}$ $cm^{-2}eV^{-1}$，而高溫一氧化二氮為$4.67x10^{10}$ $cm^{-2}eV^{-1}$，有將近十倍的差距。。

一氧化二氮(N_2O)或阿摩尼亞(NH_3)低溫(1100 ℃)爐管退火可以些微改善介面能態密度，兩種製程的疊加可以更進一步改善介面能態密度，在距離導帶0.4 eV處的數值為2.92 $x10^{11}$ $cm^{-2}eV^{-1}$。在崩潰電場方面，一氧化二氮退火可以增加崩

潰電場但仍有較寬的電場分佈，可見一氧化二氮退火可以改善氧化層的品質，但是對於碳化矽基板不平整所造成的局部電場加強導致的提早崩潰，作用不大。增加一層低壓化學氣相沈積的氮化矽層可以明顯提高崩潰電場並改善崩潰電場分佈，推測是因為氮化矽和二氧化矽層的缺陷不容易疊對，故不易形成導通路徑。

氨氣電漿處理可以大幅改善介面能態密度，但是在電漿處理過後會產生0.5-1 V的平帶電壓的偏移，此負電荷的產生機制，尚不明瞭。電漿功率在150瓦跟200瓦有相同的改善趨勢，五分鐘比兩分鐘來的好，十分鐘即達到飽和。200瓦介面能態密度略高於150瓦，可能是主因是功率太高產生額外的缺陷，而100瓦功率不夠高即使時間加長到十五分鐘還是不如150瓦十分鐘的效果好。以化學氣相沈積製程製作介電層堆疊的方法有最低的熱預算，但是介面能態密度高於直接濕氧的條件，所以需要進一步退火處理。崩潰電場分佈很廣，推測原因是第一層的氧化層的品質不好，其中機制尚待探討。最後，我們以高溫量測萃取深能帶的介面能態密度，發現各種介面能態密度改善製程的有效範圍大約是在靠近導帶0.2-0.8 eV區間，對於1 eV以下的介面能態無明顯改善效果。

二次離子質譜儀縱深分析顯示高溫(1300 ℃)一氧化二氮直接氧化的試片，在二氧化矽/碳化矽介面有氮堆積現象，其它試片則無。推測氮在二氧化矽中不易擴散，如果先成長純二氧化矽，再進行氮處理，如果製程溫度不夠高，氮無法到達二氧化矽/碳化矽介面，故介面能態的改善效果不佳。

在所有低預算製程改善中，適當的氨氣電漿處理能達到較低的介面能態密度，其數值大約是1.37 x10^{11} $cm^{-2}eV^{-1}$，但是介面能態密度還是高出本論文最低參考值三倍(高溫一氧化二氮氧化)，且氨氣電漿處理的熱預算太低，只有氫可鈍化介面能態，推測氫鈍化只對淺能帶的介面能態有效，對0.5 eV以上的介面能態無效。如果要達到更低值，在新製程開發出來之前，高熱預算的製程還是的無法避免。

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Abstract

Silicon carbide (SiC) is suitable for fabricating high power semiconductor devices because of its wide band-gap and high thermal conductivity. Unfortunately, low channel mobility occurs on the 4H-SiC MOSFETs due to the high SiO_2/SiC interface state density. How to reduce interface state density is an important issue. In this thesis, several low thermal budget processes to reduce interface state density are evaluated. Electrical parameters including interface state density and breakdown field distribution are analyzed. The effect of process conditions on interface state density is also discussed.

The low temperature (1050 ℃) wet oxidation sample set provides the higher bound reference of the interface state density (D_{it}) in this thesis. It is expected that the shorter oxidation time would result in lower interface state density. However, it is observed that lots of carbon clusters saturate on the 0.5 hr wet oxidation sample. It is suspected that the oxidation temperature is not high enough for the diffusion of CO. The interface state density of the wet oxidation sample set is around $5x10^{11}$ $cm^{-2}eV^{-1}$

at E_c-E = 0.4 eV. High temperature (1300 ℃) N_2O oxidation sample sets the lower bound reference of $D_{it.}$ The D_{it} value of this sample is $4.67x10^{10}$ $cm^{-2}eV^{-1}$ and is 10 times lower than that of the wet oxidation samples.

Low temperature (1100 ℃) post-oxidation annealing, with the N_2O annealing or NH_3 annealing, can improve the interface quality separately. The N_2O annealing and NH_3 annealing have superimposed effect the D_{it} can be improved to 2.92 $x10^{11}$ $cm^{-2}eV^{-1}$ at E_c-E = 0.4 eV. N_2O annealing can improve breakdown field but the breakdown field variation is still large. These results indicate that N_2O annealing can improved oxide quality but the early breakdown due to the rough SiC surface cannot be changed. Samples with Si_3N_4 capping have tight breakdown field distribution because weak spots in the wet oxide do not coincide with the weak spot in the nitride layer so that early breakdown could be suppressed because current path is hard to form.

NH_3 plasma treatment can improve D_{it} effectively but a 0.5~1 V positive shift of flat-band voltage compared to wet oxidation sample is observed on all of the plasma treated samples. The trends of interface improvement by plasma treatment at 150 W and 200 W are similar. The interface state density decreases as the plasma treatment time increases from 2 minutes to 5 minutes and gradually saturates as the plasma treatment time increases to 10 minutes. At the same plasma treatment time, 200 W results in slightly higher interface state density than 150 W. It is suspected that higher plasma energy produces additional interface defects due to the stronger radiation. The 100 W 15 min sample has higher D_{it} than 150 W 10 min. It is thus concluded that 150 W 10 minutes is the optimized condition. Lower energy cannot passivate interface states effectively even if 15 min treatment.

Dielectric stacks sample has the lowest thermal budget. However, it has the highest interface state density among all samples. Post-deposition annealing is

required. Dielectric stacks sample exhibits wide breakdown field variation. It is suspected that the quality of the bottom PECVD oxide is too poor. Finally, to extract deep level interface states, high temperature measurement would be required. It is observed that the D_{it} improvement occurs only in the range of E_c-E = 0.2-0.8 eV. As E_c-E > 1 eV, there is no D_{it} improvement on all the samples.

Secondary ion mass spectroscopic analysis shows nitrogen pile-up at the SiO_2/SiC interface on the sample HT. This phenomenon is not observed on the other samples. It is suspected that the diffusion of nitrogen radicals in SiO_2 is slow. If nitrogen incorporation is processed after SiO_2 growth, there are not sufficient nitrogen radicals can reach the interface at low thermal budget processes.

Although suitable NH_3 plasma treatment achieves the lowest interface state density among these low thermal budget samples, $D_{it} = 1.37 \times 10^{11}$ $cm^{-2}eV^{-1}$, this value is still 3 times higher than the lowest bound reference. Furthermore, the thermal budget of the plasma treatment is too low. Only hydrogen can passivate the interface states. It is suspected that hydrogen can only passivate shallow level interface states and does not affect the interface states deeper than 0.5 eV. To achieve very low interface state density, novel low thermal budget processes must be developed. Otherwise high thermal budget process is still unavoidable.

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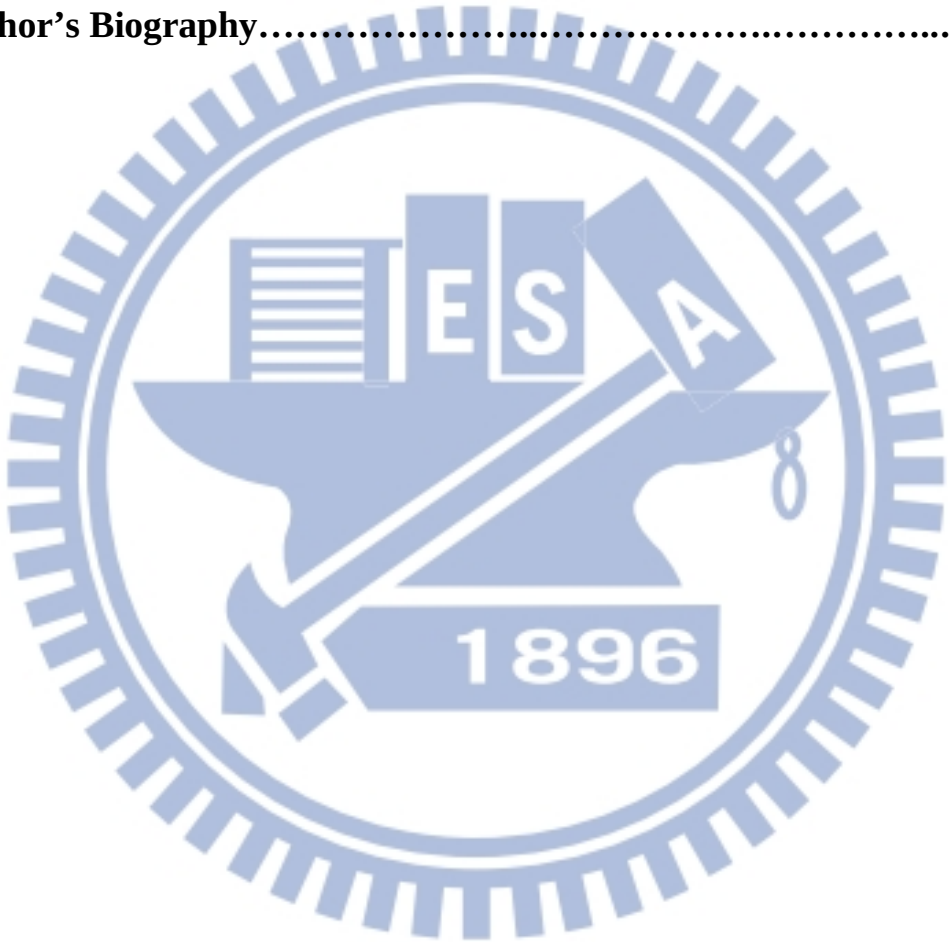
Contents



List of Tables

Chapter 1

Chapter 2

Chapter 3

List of Figures

Chapter 1

Chapter 2

Chapter 3

Chapter 1

Introduction

1-1 History of Semiconductor Power Devices

Power semiconductor devices have been developed for several decades. Although the fabrication of power device is on germanium substrate in the beginning, most of the common devices uses silicon as the main substrate currently. The power thyristor, also named silicon controlled rectifier (SCR), introduced in 1950s has high blocking voltage and good ability to handle high current, but the operation speed is low [1]. The other issue for thyristor is hard to turn off. Gate turn-off thyristor (GTO) can turn off device easily by the gate signal but still has low operation frequency and needs complex driving circuit.

Bipolar junction transistor (BJT) which appeared in 1960s provides a solution to the relative low switching speed in thyristor. However, there are several problems in BJT. First, it needs substantial base current to drive so the power dissipation increases in device. Second, when the base-collector junction becomes reverse-biased, BJT requires time to recombine minority carrier in the base and collector which limits the switching speed [2-3]. Third, the avalanche effect in BJT may destroy the device during turn-off operation. In the 1970s, power MOSFET which provides much faster switching speed with low application voltage was developed for power integrated circuits. In order to operate at high voltage, we must reduce the doping concentration to increase the length of the drift region. In this case, the on-resistance drastically increases and causes high power dissipation in the on-state [4.5]. In the 1980s, high performance insulated gate bipolar transistor (IGBT) was proposed. This device has high operation speed in MOSFET and high power in BJT. This advantage makes

IGBT a mainstream of power device since 1990s. Fig.1-1 shows the application region of power devices. IGBT and MOSFET are mainly used in automotive for high frequency application. SCR and GTO are mainly used in high power applications [6]. Fig.1-2 shows the history of semiconductor power devices [7].

The power semiconductor devices have broadened application in power supply automotive, aerospace electronics, TFT-LCD, and so on for several decades. The most common power devices are made of silicon, because silicon is low cost and has mature fabrication technology. But it is forecasted that silicon power devices would be replaced by the devices using wide band-gap substrates at very high power. There are several reasons for limiting the application of silicon power devices.

1. Low breakdown voltage

The impact ionization energy is proportional to the band-gap width, so avalanche breakdown occurs easily with low band-gap width.

2. The high on–resistance (R_{on})

For high voltage applications, we must reduce the doping concentration of the drift region to lower the electric field. As the doping concentration decreases and the drift region length increases, thus the series resistance also increases.

3. High reverse leakage current

P-N junction leakage current is proportional to the intrinsic carrier concentration (n_i). As shown in eq. (1-1), the band-gap increases and then n_i decreases. The off-state current can effectively reduce as shown in eq. (1-2) [8].

$$n_i = \sqrt{N_c N_V}\ e^{\frac{-E_G}{2kT}} \qquad \text{eq. (1-1)}$$

where n_i is the intrinsic carrier concentration (cm^{-3}), N_c is conduction band effective density (cm^{-3}) and N_v is valence band effective density (cm^{-3}), E_G is the band-gap, k is the Boltzmann constant, and T is the temperature in Kelvin.

$$J_L=\frac{qn_iW}{\tau_e}+q\left(\frac{D_h}{\tau_h}\right)^{1/2}\frac{{n_i}^2}{N_d} \quad \text{eq. (1-2)}$$

where n_i is the intrinsic carrier concentration (cm^{-3}), W is the width of the depletion region (cm), τ_e is the lifetime of electrons in the depletion region (s), N_d is the concentration of donor atoms (cm^{-3}), D_h is the diffusion constant of holes in the n-type region (cm^2/s), and τ_h is the lifetime of holes.

4. Low operation temperature

The band-gap of Si is 1.12 eV. This low value indicates that Si has much higher intrinsic carrier concentration at high temperature than wide band-gap materials. The operation temperature of Si power devices is limited to 150 ℃, because the large leakage current induced by the thermal-generation of electron-hole pairs. Si devices are not suitable for harsh environment.

1-2 Overview of Wide Band-gap Materials

As mention above, Si power devices reach their theoretical limits at high voltage and high temperature application. The wide band-gap materials, such as SiC and GaN, have attracted more and more attention in high power electronics. Fig.1-3 shows the theoretical limits of Si, SiC and GaN. Some important material parameters of wide band-gap semiconductors are listed in Table 1[9]. The band-gap of SiC and GaN is 3.26 eV and 3.39 eV, respectively. Such a wide band-gap allows operation at temperatures higher than 300 ℃. Since SiC has higher breakdown field than Si, SiC can achieve higher breakdown voltage with the same doping concentration. On the other hand, to sustain the same breakdown voltage, SiC devices allow thinner and higher doping drift region. Consequently, higher on-state current density can be conducted and the device area can be reduced. Although GaN has higher carrier mobility than SiC so that higher on current density and lower on resistance can be

achieved in GaN device, SiC has higher thermal conductivity than GaN so that SiC is more suitable at high power and high temperature environment. In addition, GaN usually grows by heteroepitaxy. The substrate such as Si and sapphire are usually used. The cost and quality of GaN crystal growth are issues. GaN is used for blue laser diode and high power microwave device [10-11]. Furthermore, the high defect density in GaN substrate is a big problem. The threading dislocation induces leakage current and limits the ability to produce high power density devices. As discussed above, the excellent electrical and material properties of SiC allow it to be fabricated as power devices.

1-3 Silicon carbide (SiC) Crystals

SiC is composed of silicon and carbon. SiC possesses more than 170 stack sequences known as polytypes. Each sheet of the SiC bi-layer is composed of one Si atom and one carbon atom [12]. Each C atom is bonded with 4 Si atoms. As shown in Fig.1-4 [13], The first carbon sheet defines a hexagonal plane which is labeled as A and The next bi-layer can be placed on the first sheet ‘valleys’ and is denoted as B or C. The packing sequence for HCP is ABAB and that for FCC is ABCABC. Figs.1-5 and 1-6 show the most common polytype stacking sequence in SiC [13]. The name of polytypes consists of number and letter. The number represents the periodicity of the stacking number. The letter represents the structure of polytypes (C=cubic, H= hexagonal, R= rhombohedral). For example, 3C-SiC represents stacking periodicity of ABC and cubic structure. There are four Miller indices (a_1 a_2 a_3 c) in the wurtzite structure (HCP) such as 4H-SiC (0 0 0 1) .The picture is shown in Fig.1-7. If we describe two symmetry atoms (A and B in Fig.1-8) with 3 Miller indices (a_1 a_2 c), the (2 -1 0) and (1 1 0) do not represent lattice symmetry. It is needed to add a 4^{th} Miller

index which can label the two atoms as (1 -1 0 0) and (1 0 -1 0) for lattice symmetry. The common used polytypes are 6H-, 4H-, and 3C-SiC. Different SiC polytypes have the same chemical and mechanical properties, but the band-gap and mobility are quite different. The band-gap values of SiC polytypes depend on percentage of hexagonality. The band-gap width of the 3C-SiC (0% hexagonal) is 2.39 eV which differs from the 3.33 eV of the 2H-SiC (100% hexagonal) [14]. We can see the Si-terminated face (0 0 0 1) and the C-terminated face (0 0 0 -1) in Fig.1-6. The two faces are different in oxidation rate and thus different MOS device properties. The 4H-SiC are more often used than the others because of its high breakdown field and high carrier mobility. The 3C-SiC has a smaller band-gap and lower breakdown field but higher mobility than the 6H-SiC. High quality 3C-SiC epi-layer can be grown on Si so that the wafer cost can be reduced.

Although SiC has good electrical properties such as high electron velocity, chemical inert, high breakdown field, and high carrier mobility, some MOSFET fabrication issues exist. First, dopant diffusion in SiC is very slow even at very high temperature so that ion implantation method must be employed. After ion implantation, very high temperature annealing (~1700 ℃) is required to activate dopants. Second, the oxidation rate of SiC is very low. Moreover, the poor SiO_2/SiC interface quality needs to be improved. The oxide reliability at high field and high temperature also needs more investigations.

1-4 Oxidation Issues of SiC

As mentioned above, SiC has superior electrical properties and can produce low on resistance and high blocking voltage power devices. SiC is the only one compound semiconductor that can be thermally oxidized directly, which is similar to the Si

technology. The power MOSFET is an important device for two reasons. First, it has higher switch speed and low power loss than BJT because MOSFET has no minority carrier storage effect. Second, it also has large safe operation area (SOA) for automotive application. The early SiC power MOSFET was reported in 1995 with UMOSFET structure [15]. The trench corner is easily to breakdown, so the breakdown voltage is only 260 V. In order to eliminate the corner breakdown, the DMOSFET structure was reported in 1997 [16]. The breakdown voltage was improved to 760 V. The LDMOSFET with a long lateral drift region can achieve a breakdown voltage of 2.6 kV [17]. Moreover, a RESURF technology combined with LDMOSFET structure to reduce surface field has been reported in literature [18]. In the present, there are several commercialized SiC devices such as Schottky Barrier Diode (SBD), Junction Barrier Schottky Diode (JBSD), and MOSFET. A 1200 V power MOSFET has been commercialized recently [19]. Unfortunately, the low channel mobility in the range of 5–40 cm/V-s occurs on the 4H-SiC MOSFET due to the higher SiO_2/SiC interface states density [20]. The large amount trapped charges at the SiO_2/SiC interface results in Coulomb scattering and degrades channel mobility. The usually measured SiO_2/SiC interface states density exceeds 10^{12} $1/cm^2/eV$, which is 100 times higher than the SiO_2/ Si interface.

The SiC oxidation mechanism obeys the following chemical reaction [21].

$$SiC + 1.5\ O_2 \rightarrow SiO_2 + CO$$

There are several steps for SiC oxidation. First, molecular oxygen transports to the SiO_2 surface and then diffuses toward SiO_2/SiC interface. Second, molecular oxygen reacts with SiC forming SiO_2 and the product (CO) diffuses out of the SiO_2. The unreacted carbon and undiffused CO residue at the SiO_2/SiC interface that cause the high interface state density (D_{it}). How to reduce D_{it} is a critical issue for SiC MOS device. The most commonly used method is employing a post-oxidation annealing

(POA) in NO or N_2O ambient at high temperature for a long time. During the POA process, N atoms incorporate to the SiO_2/SiC interface and form the Si-N and C-N bonds to passivate the interface states. NO annealing can be more effective in improving D_{it} than N_2O annealing. Because NO is a toxic gas, it is impractical to use NO [22-23]. Some researchers used high dielectric constant (high-κ) dielectrics to replace SiO_2 [24]. The electric field in high-κ dielectrics is lower than that in the low-κ SiO_2 at the same effective thickness. However, the conduction band offset between high-κ and SiC is lower than that between SiO_2 and SiC because of the higher dielectric constant the lower energy band-gap. The carrier tunneling barrier reduces and leakage current increases [25].

$POCl_3$ [26], NH_3 [27] and H_2 [28] annealing have also been reported in literature. Although $POCl_3$ annealing can achieve lower D_{it} than NO annealing, the increase of positive charges in oxide after annealing causes apparent flat-band voltage shift. H_2 annealing exhibits little improvement on D_{it} and the best result occurs at 800 ℃. Above 800 ℃, H_2 annealing does not further reduce $D_{it.}$ NH_3 and N_2O annealing do not reduce D_{it} to acceptable level [29]. In addition to these POA methods, the oxidation in sodium (Na) environment can reduce D_{it} and achieved channel mobility to above 150 cm^2/Vs. Unfortunately, there are many Na mobile ions in oxide [30].

High doping concentration (>>10^{15} cm^{-3}) n-type SiC substrate has been used to enhance oxidation rate [21]. This enhancement is due to the doping-induced lattice mismatch. However, the oxide quality degrades due to this mismatch. To enhance oxidation rate, preamorphization by ion implantation has been proposed [31]. The oxidation rate of amorphous SiC is comparable to that of Si so that the low temperature oxidation can be achieved. However, the wide carbon transition region occurs between the crystal SiC and SiO_2, as the temperature is not high enough to diffuse CO out and consume the amorphous region totally.

1-5 Motivation

The post-oxidation treatment methods in recently literatures are discussed in the previous section. Most of the methods need high temperature and very long annealing process. In this thesis we try to compare different types of low thermal budget processes (<1100 ℃) and the best process for the lowest interface state density is identified. The sample set of low temperature wet oxidation is the high bound reference of interface state density in this thesis since lots of carbon clusters during long time oxidation do not have enough time to diffuse out [32]. The current transport mechanisms of the wet oxide samples are also investigated The 1300 ℃ N_2O oxidation sample provides the lowest bound reference of interface states density in this thesis.

Three sets of samples are used to compare with reference samples. First, post-oxidation annealing (N) is performed. We want to understand if NH_3 and N_2O annealing have superposition effect or not. Second, the post-oxidation ammonia plasma treatment method has the lowest thermal budget but a few literatures used this method on SiC MIS capacitor [33]. We want to investigate the interface passivation effect with various times and powers of plasma. We also want to know the limitation of plasma treatment with high power and long treatment time. The optimum treatment condition would be found. Third, in order to avoid C transition layer at the SiO_2/SiC interface during thermal oxidation, we try to deposit plasma enhanced chemical vapor deposition (PECVD) oxide and High-κ material on SiC. We obtain large effective oxide thickness (EOT) with dielectric stacks.

High temperature measurement is performed because we want to extract deep level interface state density. We describe the details reasons for high temperature measurement in the next chapter. Mobile ion measurement is also performed in this

thesis.

1-6 Thesis Organization

The first chapter is the introduction including fundamental properties of power devices, wide band-gap materials, and SiC crystals. Then, the oxidation issues and known post-oxidation treatment methods are discussed. The second chapter shows the experimental procedure, electrical measurement conditions, and material analyses.

The third chapter is the experimental results and discussion. Various gate dielectrics are divided into 5 categories. They are wet oxidation (W), high temperature N_2O oxidation (HT), post-oxidation annealing (N, NH, and NOH), dielectric stack (ONO), and post-oxidation ammonia plasma treatment (P). Electrical properties such as interface state density and oxide breakdown field are discussed. The high temperature electrical characteristic and material analysis results are also discussed. Finally, the interface states density characteristic of the representable samples are summarized. The last chapter is the conclusions and future works of this thesis.

Table 1-1 Electrical properties parameters of wide band-gap semiconductors [9].

	Si	3C-SiC	6H-SiC	4H-SiC	GaN
E_g (eV)	1.12	2.3	2.9	3.2	3.39
E_c (MV/cm)	0.3	2	2.5	3	5
Vsat (10^7 cm/s)	1	2.5	2	2	2
μ_n (cm^2/V-sec)	1450	1000	415	950	1000
ε_r	11.7	9.6	9.7	10	8.9
λ (W/cmK)	1.3	5	5	5	1.3

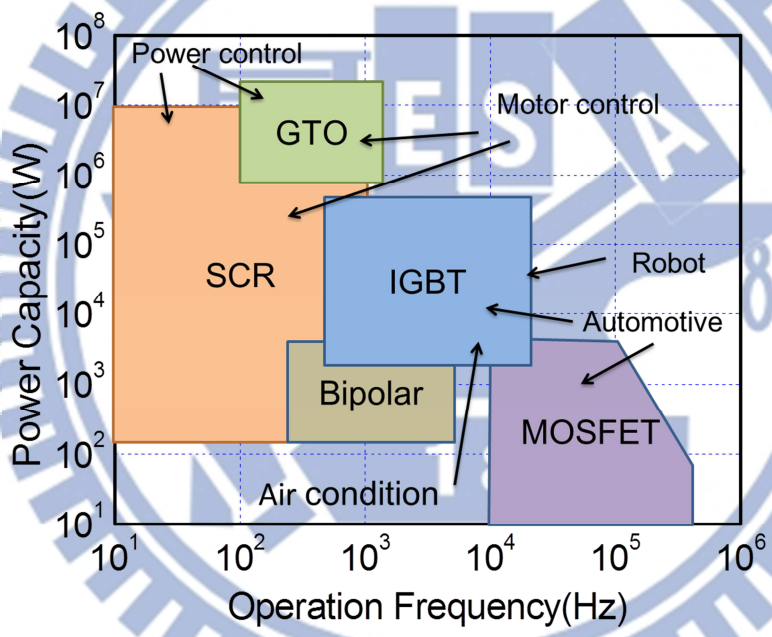


Fig.1-1 Application region apply in power devices. IGBT and MOSFET are mainly used in automotive for high frequency application. SCR and GTO are mainly used in high power applications [6].

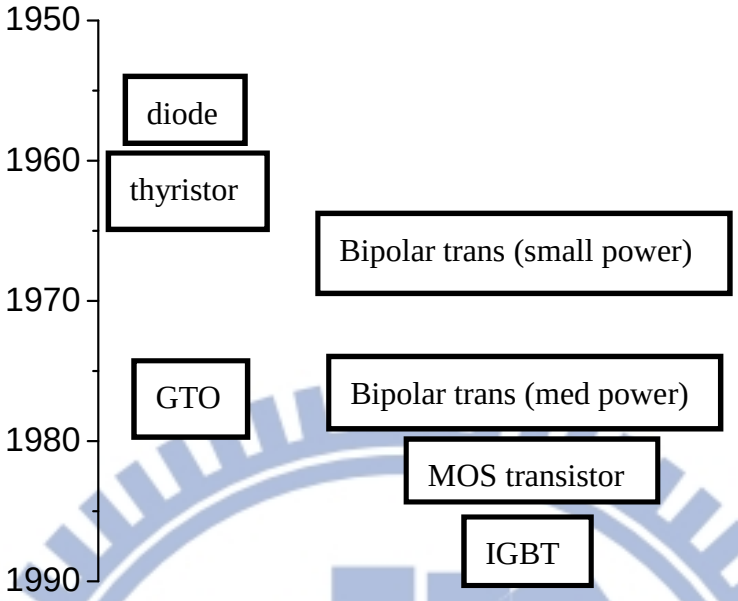


Fig.1-2 History trend of semiconductor power devices [7].

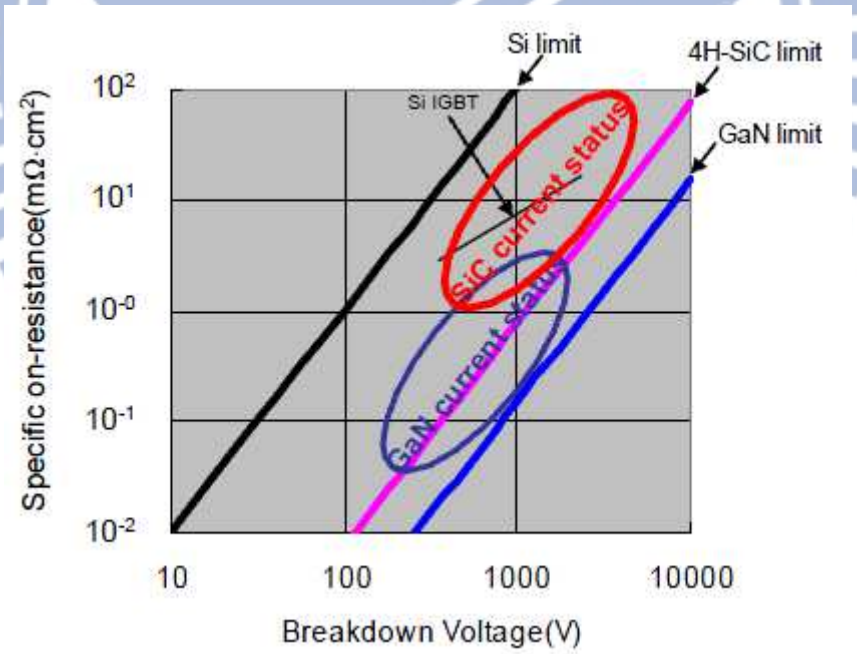


Fig.1-3 Theoretical limits of on resistance and breakdown voltage in Si, SiC, and GaN material [11]

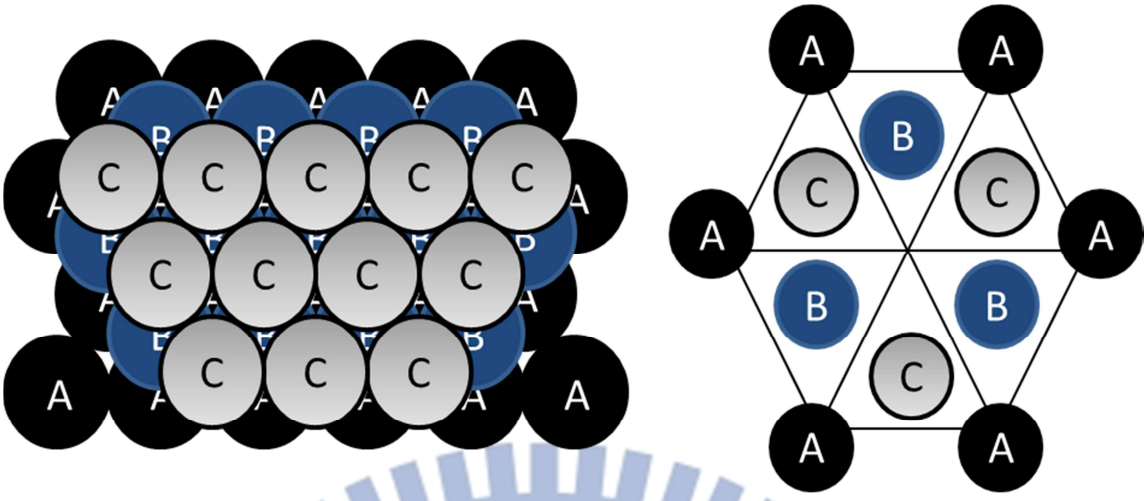


Fig.1-4 Close-packed sphere model shows three distinct layers (A, B, C) .The first carbon sheet defines a hexagonal plane which is labeled as A. The next bi-layer can be placed on the first sheet 'valleys' and is denoted as B or C. [13].

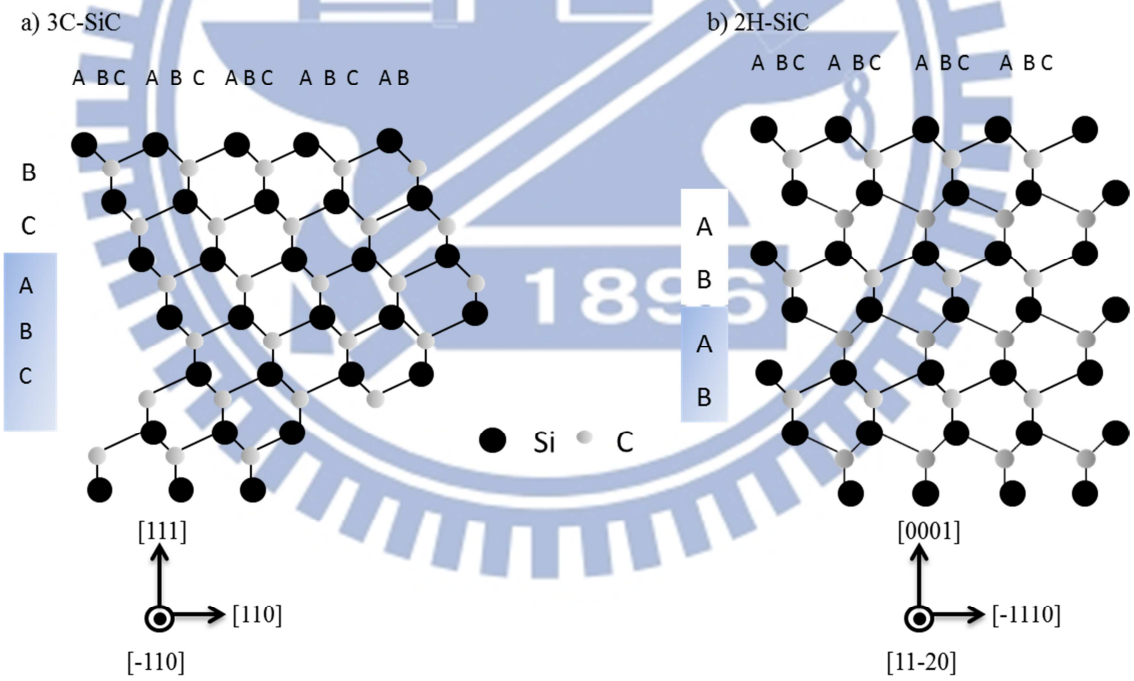


Fig.1-5 3C-SiC is the very only 100% cubic polytype exhibiting a strict zinc-blende-type structure while 2H-SiC represents the only 100% hexagonal polytype of silicon carbide structure (wurtzite-type structure) [13]

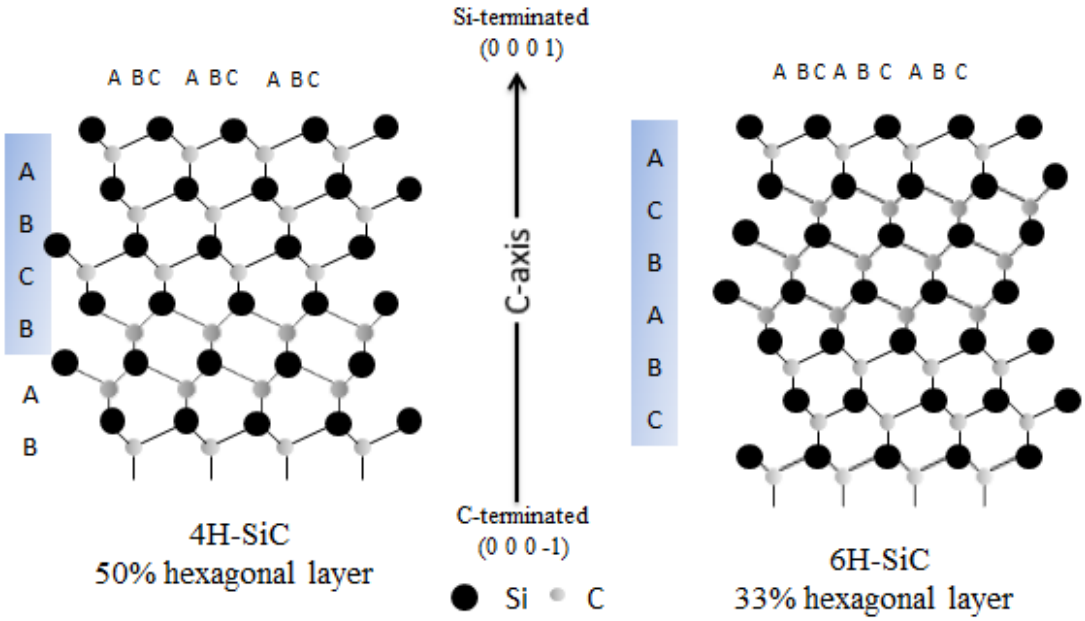


Fig.1-6 Crystal structures of the two most important SiC polytypes 4H- and 6H-SiC. We can see the Si-terminated face (0 0 0 1) and the C-terminated face (0 0 0 -1) [13].

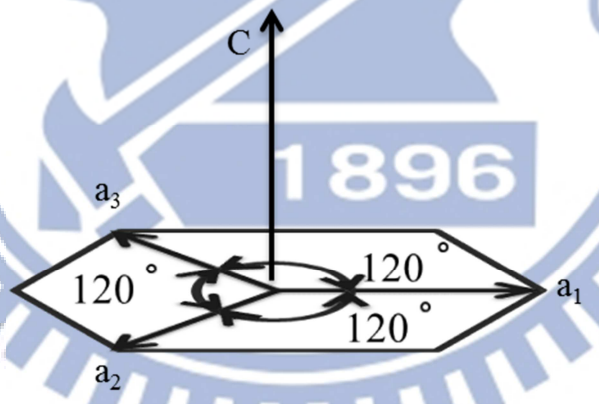


Fig.1-7 There are four Miller Indices (a_1 a_2 a_3 c) in hexagonal structure [13].

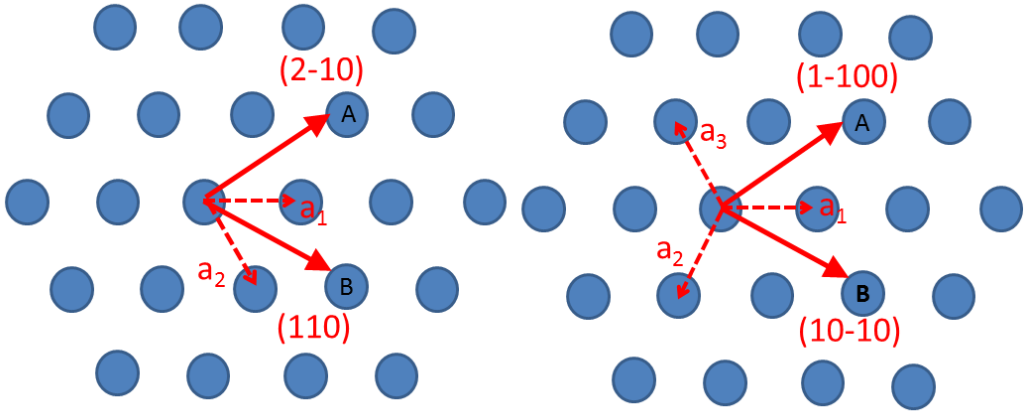


Fig.1-8 Two symmetry atoms (A and B) is described with 3 Miller indices (a_1 a_2 c), and 4th Miller Indices (a_1 a_2 a_3 c).

Chapter 2

Experiments

2.1 MIS Capacitor Fabrication

Simple metal-insulator-semiconductor (MIS) structure was fabricated. The substrate is an n-type (0 0 0 1)-oriented 4H-SiC epi-wafer. The lightly-doped n-type epi-layer is 11-μm-thick and is doped by N to a concentration of N_D = 3-6 x10^{15} cm^{-3}. First, a standard RCA clean was performed. Various gate dielectrics were formed by various processes as listed in Tables 2-1, 2-2, 2-3, and 2-4. Aluminum was deposited by thermal evaporation process and patterned by typical lithography process to be gate electrode. The gate area ranges from 1x10^{-3} cm^{-2} to 1x10^{-4} cm^{-2}. The dielectrics on the backside of the samples were wiped by wet processes followed by aluminum deposition to form contact. All samples were annealed at 400℃ for 30 min in N_2 ambient. The MIS structure is shown in Fig.2-1. The detailed processes of the various gate dielectrics are explained as follows. Gate dielectrics can be divided into 5 categories. They are wet oxidation (sample W), high temperature N_2O oxidation (sample HT), post-oxidation nitridation annealing (samples N, NH and NOH), dielectric stack (ONO), and post-oxidation ammonia plasma treatment (sample P).

1. Wet Oxidation

The gate dielectrics of sample W0.5, W1, W2, W3, and W5 were grown by wet oxidation process at 1050 ℃ for 0.5, 1, 2, 3, and 5 hr, respectively. The oxidation recipe is shown in Table 2-1. These samples are used to extract the parabolic rate constant (B) and the linear rate constant (B/A) of thermal oxidation of SiC according to the Deal-Grove model [21]. This sample set also provides the higher bound

reference of the interface state density (D_{it}) because low temperature thermal oxidation would result in a large amount of carbon clusters at the SiO_2/SiC interface [34].

2. High Temperature N_2O Oxidation

The gate dielectric was grown at 1300 ℃ in N_2O ambient. This sample provides the lower bound reference of D_{it} in this work and is labeled as sample HT. The process condition is listed in Table 2-1.

3. NH_3 and N_2O post-oxidation annealing

The gate dielectric of sample N was grown by wet oxidation at 1050 ℃ for 1 hr followed by an N_2O annealing at 1100 ℃ for 1 hr. Sample NH has the same wet oxide as sample N but the post-oxidation annealing was performed in NH_3 ambient at 1100 ℃ for 1.5 hr in a low-pressure chemical vapor deposition (LPCVD) system. After annealing, temperature went down to 800 ℃ and a 50-nm-thick Si_3N_4 layer was deposited for 5 minutes at 180 mTorr using SiH_2Cl_2 and NH_3 as precursors in the same LPCVD system. The expected nitride thickness is 50 nm. Sample NOH also has a wet oxide grown at 1050 ℃ for both N_2O and NH_3 annealing were performed in sequence after oxidation. After annealing, Si_3N_4 was deposited with the same condition for sample NH. This sample is mainly used to investigate whether the NH_3 and N_2O annealing has superimposed effect. The process conditions are listed in Table 2-2.

4. NH_3 plasma post-oxidation treatment

The NH_3 plasma treatment method is common used in Silicon process but only few literatures have been reported on SiC application [33]. The gate dielectric of this sample set was grown by wet oxidation at 1050 ℃ for 5 hr. After oxidation, samples were exposed to NH_3 plasma at different powers and periods at 300 ℃. The gas flow rate is 200 standard cubic centimeter per minute (sccm) and the chamber pressure was

250 Pa. The sample ID has the form of PA.B where A represents power in Watt and B represents period in minute. The process conditions are listed in Table 2-3.

5. Dielectric stack

We tried to deposit dielectric on SiC by CVD method in order to avoid C transition layer at SiO_2/SiC interface due to oxidation. The gate dielectric of sample ONO has an oxide/nitride/oxide structure. The sandwiched nitride layer has higher dielectric constant than oxide and thus can allow thicker physical thickness but remains the same effective oxide thickness. The first oxide layer was deposited at 350 ℃ using TEOS as precursor to a thickness of 10 nm in a plasma-enhanced chemical vapor deposition (PECVD) system. Then, a post-deposition annealing in pure O_2 ambient at 800 ℃ was performed for 30 min to densify the PECVD oxide. The Si_3N_4 layer was deposited in a LPCVD system to 57-nm-thick. The top oxide layer was deposited with the same deposition condition of the bottom oxide layer. The top layer acts as a barrier layer to block carrier injection from the metal gate due to the higher band-gap offset between metal/SiO_2 [35]. The expected effective oxide thickness is 50 nm. The process condition is listed in Table 2-4.

2.2 Electrical Characterization

Both capacitance-voltage (C-V) and current-voltage (I-V) characteristics of the MIS capacitors were measured. The high frequency C-V characteristics were measured by a precision impedance meter of model Agilent 4284A at 10 kHz with voltage swept from +5 to -4 V. The quasi-static C-V and I-V characteristics were measured by a semiconductor parameters analyzer of model Agilent 4156C. The voltage ramping rate for the quasi-static C-V measurement is 50 mV/sec.

The effective oxide thickness can be calculated from the accumulation

capacitance (C_{ox}). The Hi-Lo C-V method is common used to extract the interface state density. This method was proposed in 1970 [36]. The concept of the method is calculating the capacitance difference between high frequency (>1 kHz) C-V and low frequency C-V at each bias. The low frequency C-V includes the interface states capacitance (C_{it}) because the interface states are able to follow the low frequency signal. The interface states almost can't follow the high frequency C-V signal so that the C_{it} is not included in the measure capacitance. Fig.2-2 shows the typical Hi-Lo C-V curves on MOS capacitor. Since SiC is a wide band-gap material, it is hard to measure deep level traps due to their long respond time at room temperature. The time constant for hole emission from an interface states to valence band in a p-type semiconductor can be written as

$$\tau_p(E) = \frac{1}{\sigma_p v_T N_v} \, exp^{\frac{E-E_v}{kT}} , \qquad \text{eq. (2-1)}$$

where σ_p is the capture cross section for holes, v_T is the electron thermal velocity, N_v is the effective density of states in the valence band, k is Boltzmann's constant, T is the absolute temperature, and $E-E_v$ is the energy of the interface state relative to the valence band edge. Time constant for hole emission versus $E-E_v$ plot is shown in Fig.2-3 at different temperatures and different Hi-Lo frequency conditions [37]. The horizontal line in Fig.2-3 shows the cut-off frequency of D_{it} measurement. Those lines are used to define energy range of D_{it} measurement. The D_{it} value can be actually measure at room temperature using the Hi-Lo C-V method is about 0.2-0.6 eV away from the conduction band or valence band. If we want to measure deep level traps, rising temperature, bias at inversion, and illumination where interface response times are shorter are common methods used in literature. In this thesis, the measurement temperature is raised to 523 K. We can extract deep level D_{it} at 1.6 eV away from the conduction band or valence band. The relation between surface potential and the trap

energy is

$E_C - E_t = -\psi_S + E_g/2 + kT \ln(N_D/n_i)/q$, eq. (2-2)

where E_C is conduction band energy, E_t is trap energy, ϕ_S is the band-bending under gate bias, E_g is the energy gap of 4H-SiC, N_D is the doping concentration, n_i is the intrinsic carrier concentration of 4H-SiC, k is the Boltzmann constant and T is the absolute temperature.

The dielectric breakdown field is extracted from the I-V characteristics. The I-V curve is converted to current density-electric field (J-E) plot firstly using following equations:

$J = I/A_G$, eq. (2-3)

$E = (V_G - V_{FB})/EOT$, eq. (2-4)

where A_G, V_{FB}, J, E, and EOT are gate area, flat-band voltage, current density, electric field in oxide, and effective oxide thickness with respect to SiO_2, respectively. The breakdown field is defined as the electric field at which the current density equals to 10^{-2} A/cm^2.

The J-E plot is also used to identify the current transport mechanism. The Fowler-Nordheim (FN) tunneling, Schottky emission (SE), and Frenkel-Poole (FP) emission are been considered [38].

1. Fowler-Nordheim (FN) tunneling

The J-E equation is shown in eq. (2-5).

$$J = E^2 \exp\left[\frac{-4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar E}\right], \quad \text{eq. (2-5)}$$

where J is F-N tunneling current, E is electric field in oxide, m* is effective electron mass in oxide, $\varphi_{B,FN}$ is barrier height between semiconductor and oxide, and $\hbar$ is Planck's constant. The F-N tunneling barrier height ($\varphi_{B,FN}$) can be extracted from the

ln (J/E^2) versus 1/E plot. The slope gives barrier height ($\varphi_{B,FN}$). The current path is shown in Fig. 2-4(1).

2. Schottky emission (SE)

The J-E equation of Schottky emission is expressed as

$$J = A^* T^2 \exp\left[\frac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon_I}\right)}{kT}\right] \quad \text{eq. (2-6)}$$

and

$$A^* = \frac{4\pi q m^* k^2}{h^3} \ , \quad \text{eq. (2-7)}$$

where A^* is termed as the effective Richardson constant, J is current density governed by Schottky emission, m* is effective electron mass in oxide, E is electric field in oxide, φ_B, ε_I, k and h are Schottky barrier height, dielectric constant, Boltzmann's constant, and Planck's constant, respectively. The SE barrier height ($\varphi_{B,SE}$) can be extracted from the $\ln(J/AT^2)$ versus $E^{1/2}$ plot. The intercept gives the barrier height ($\varphi_{B,SE}$). The current path is shown in Fig. 2-4(2). The dielectric constant can be extracted from the plot. This value can be used to confirm if SE is the actual current transport mechanism.

3. Frenkel- Poole (FP)

The J-E equation of the FP emission is shown in eq. (2-8).

$$J = E \exp\left[\frac{-q\left(\phi_B - \sqrt{qE/\pi\varepsilon_I}\right)}{kT}\right], \quad \text{eq. (2-8)}$$

where J is the current density governed by Frenkel-Poole emission, E is electric field in oxide, $\varphi_{B,PF}$, ε_I, and k are barrier height, dielectric constant, and Boltzmann's constant, respectively. The barrier height ($\varphi_{B,PF}$) and dielectric constant (ε_I) can be extracted from the $\ln(J/E)$ versus $E^{1/2}$ plot. The intercept gives barrier height and the slope is related to dielectric constant. The current path is shown in Fig. 2-4(3).

Mobile ions in gate dielectric were measured in this thesis. First, the bias temperature stress (BTS) method was utilized. We elevated temperature to 473 K and applied around -1 MV/cm constant field for 30 min. Then, sample was cooling down to room temperature and high frequency C-V was measured to extract $V_{FB}(-)$. Second, sample was applied a +1 MV/cm electric field at 473 K for 30 min. After cooling down to room temperature, C-V was measured to extract $V_{FB}(+)$. The calculation formula for mobile ion density Q_m is shown in eq. (2-9).

$$Q_m = C_{acc} \times \left| V_{FB}(+) - V_{FB}(-) \right| \quad \text{eq. (2-9)}$$

Another measurement method is triangular voltage sweep (TVS). High frequency and quasistatic C-V characteristics were measured at 523 K. We integrated the area between high frequency and quasistatic C-V to obtain mobile ion value.

2-3 Material Analysis

Several material analysis techniques were used to understand the sample structure and dielectric composition. High resolution transmission electron microscope (TEM) was used to determine the accurate dielectric thickness and the interface roughness. The Energy-dispersive X-ray spectroscopy (EDS) was used to determine the atomic composition of each dielectric layer. Nitrogen may pile up at the SiO_2/SiC interface after various nitridation processes to passivate defects and reduce D_{it}. Carbon cluster at the SiO_2/SiC play important role on the interface quality. The depth profiles of N and C were measured by secondary ion mass spectrometry (SIMS) using Cs^+ as primary ion. The surface roughnesses on SiC surface and on gate dielectric surface were measured by atomic force microscopy (AFM)

Table 2-1 Main processes conditions of wet oxidation samples and high temperature N_2O.

Sample	W0.5	W1	W2	W3	W5	HT
Main Process	Wet O_2 1050 ℃ 0.5 hr	Wet O_2 1050 ℃ 1 hr	Wet O_2 1050 ℃ 2 hr	Wet O_2 1050 ℃ 3 hr	Wet O_2 1050 ℃ 5 hr	1300 ℃ N_2O grown

.

Table 2-2 Main processes conditions of NH_3 and N_2O post-oxidation annealing samples.

Sample	N	NH	NOH
Main Process	Wet O_2 1050℃ 1 hr		
	N_2O 1100 ℃ 1 hr	NH_3 1100 ℃ 1.5 hr	N_2O 1100 ℃ 1 hr+ NH_3 1100 ℃ 1.5 hr
		Si_3N_4 33 nm	Si_3N_4 33 nm

Table 2-3 Main processes conditions of NH_3 plasma treatment samples.

Sample	P100.10	P100.15	P150.2	P150.5
Main Process	Wet O_2 1050 ℃ 5 hr			
	100 W 10 min	100 W 15 min	150 W 2 min	150 W 5 min
Sample	P150.10	P200.2	P200.5	P200.10
Main Process	Wet O_2 1050 ℃ 5 hr			
	150 W 10 min	200 W 2 min	200 W 5 min	200 W 10 min

Table 2-4 Main process condition of dielectric stacks.

Sample	ONO
Main Process	TEOS PECVD 350 ℃ 10 nm
	800 ℃ O_2 30 min annealing
	LPCVD Si_3N_4 57 nm
	TEOS PECVD 300 ℃ 10nm

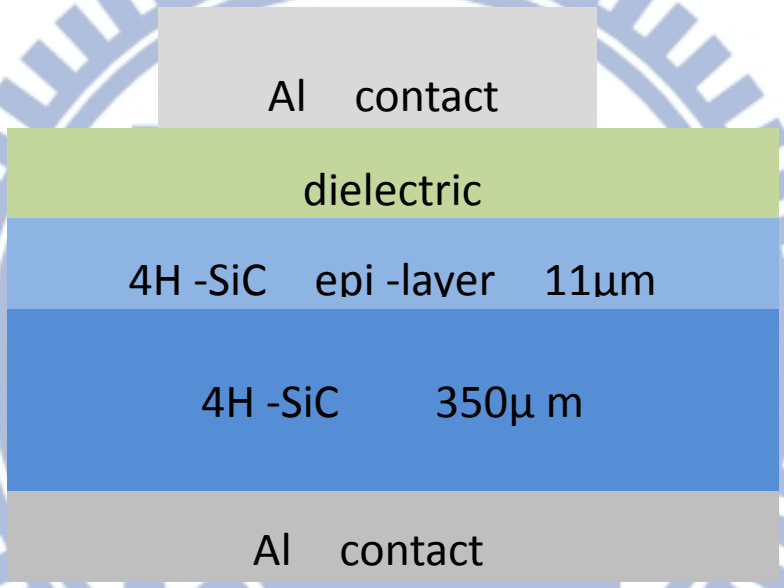


Fig.2-1 Schematic cross-sectional structures of the MIS capacitors

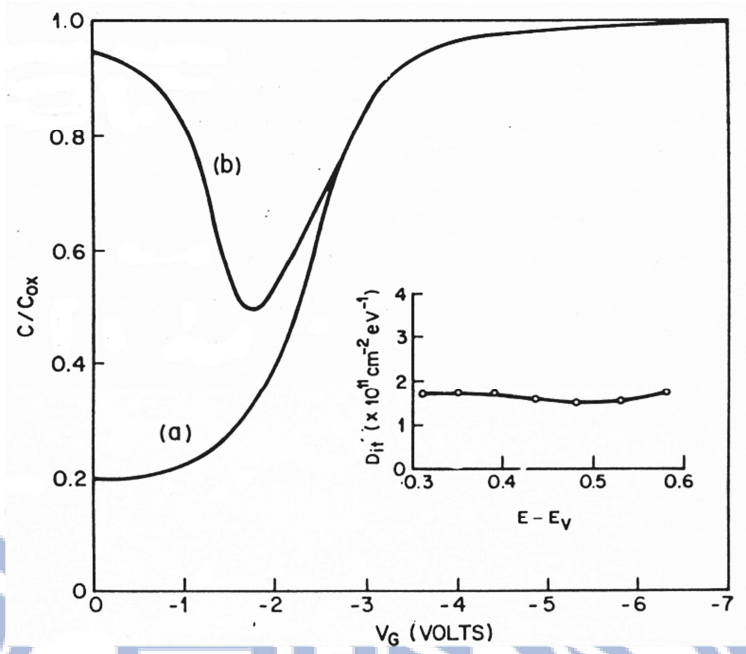


Fig.2-2 Hi-lo CV curve obtained from MOS capacitor

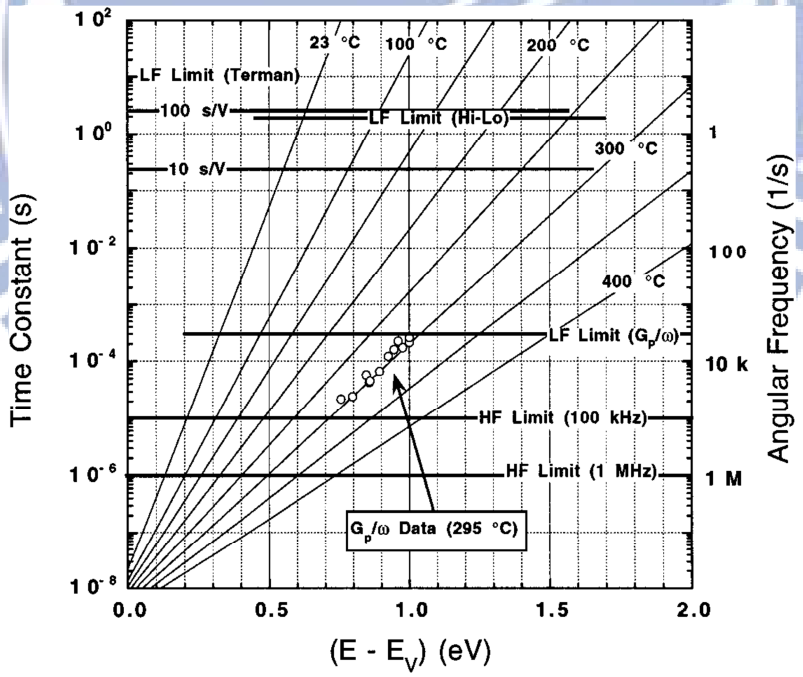


Fig.2-3 Time constants versus band-gap plot is at difference temperatures. Horizontal line is interface states extraction region with several methods [37].

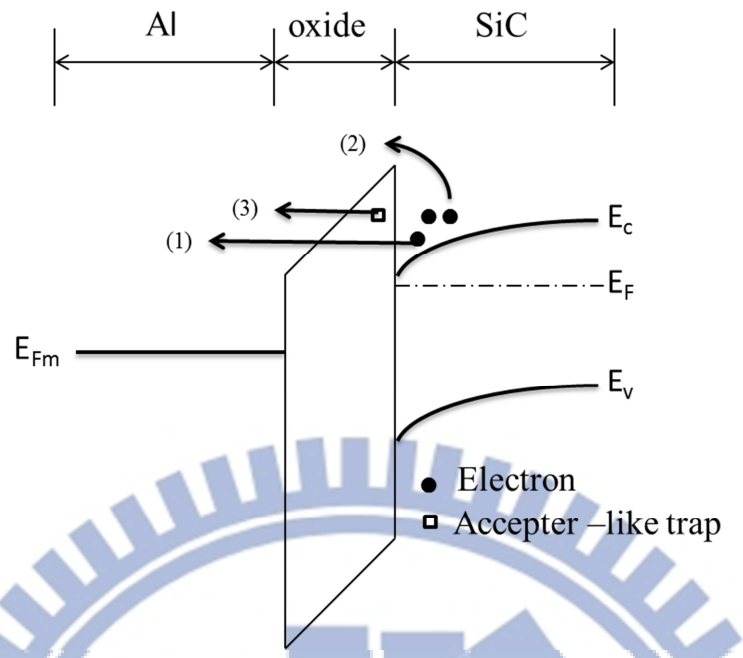


Fig.2-4 Schematic energy-band diagrams of current transport mechanism. The numbering (1)-(3) is related to current transport path. Where (1) is Fowler-Nordheim tunneling, (2) is Schottky emission, and (3) is Poole-Frenkel emission. E_C, E_F, E_V, and E_{FM} are the conduction band edge, Fermi level, valence band edge, and Fermi level of Al, respectively.

Chapter 3

Experimental Results and Discussion

3-1 1050 ℃ Wet Oxidation

The low temperature direct thermal oxidation is investigated in this thesis firstly. Samples W0.5, W1, W2, W3, W5 were wet oxidize at 1050 ℃ for 0.5 hr, 1 hr, 2 hr, 3 hr, and 5 hr, respectively. The thicknesses of the five samples are 9.5 nm, 14.6 nm, 20 nm, 26 nm and 32 nm in sequence. These thickness values are calculated from the accumulation capacitance (C_{ox}). Thickness as a function of oxidation time is shown in Fig.3-1. The oxide thickness saturates when the oxidation time becomes larger than five hours. Deal-Grove model is used to calculate the parabolic rate constant (B) and linear rate constant (B/A). The formula is shown in below.

$$t+\tau = \frac{X^2}{B}+\frac{X}{B/A}, \qquad \text{eq.(3-1)}$$

where X is the oxide thickness, τ is the time that consider native oxide, t is the oxidation time. In the initial oxide growth period, the X is very small. The linear term (B/A) dominates. The linear rate constant is related to the reaction between SiC and oxidants. If oxidants diffuse through grown oxide to oxidize the underlying SiC substrate and the product of CO molecules diffuse out of the sample for long term oxidation, the parabolic rate constant (B) dominates the oxidation rate. This constant is determined by the gas diffusivity at grown oxide. The calculation procedures are described in the next paragraph [21].

First, the thickness-oxidation time (t) plot is fitted by a second order polynomial. The τ value can be extracted by the second order polynomial fitting as shown in Fig.3-2. The extracted τ value is 0.43 hr. With the known τ value, we can plot the thickness (x) as a linear function of (t+τ)/x. The slope is parabolic rate constant (B)

and intercept is A as shown in Fig.3-3. The parabolic rate constant is around 0.000287 $\mu m^2/h$. The linear rate constant is around 0.019 $\mu m/h$. These two values are much lower than those of silicon oxidation, and the oxidation rate of SiC is quite slow.

The C-V characteristics of sample W5 is shown in Fig.3-4. It is observed that the C-V curves shift toward negative voltage axis with the decreasing of measurement frequency, and the shape of the C-V curves changes slightly at all frequencies. This phenomenon is related to the response of the interface states near conduction band. The deep level interface states can response the DC and AC signal at low frequency since the deep level states have longer trapping and detrapping time constant [39]. Significant separation of the high-low C-V curves indicates that high interface state density exists near conduction band edge.

It is expect that the shorter oxidation time sample has lower interface state density due to fewer carbon cluster formation. The interface state density extracted by the hi-lo C-V method is shown in Fig.3-5. There is no significant difference in interface state density between Sample W0.5, W1, W2, W3, W5. This result indicates that a large amount of carbon clusters have been formed in 0.5 hr at 1050 ℃. The interface state density is around $5x10^{11}$ $cm^{-2}eV^{-1}$ at E_c-E = 0.4 eV. It has been reported that the interface state density depends on wet oxidation thickness in literature but the oxidation temperature is 1110 ℃ which is higher than our experiment [40]. It is seems that lots of carbon clusters saturate on sample W0.5 because the oxidation temperature is possibly not high enough for the diffusion of CO.

The breakdown characteristic of 13-15 devices was measured on each sample. The breakdown voltage is defined at which the current density $J = 10^{-2}$ A/cm^2. Fig.3-6 shows the current density versus electric field (J-E) characteristics of the sample W1. The samples with thinner oxide, W0.5, W1, and W2, exhibit wide distribution of breakdown field while the samples W3 and W5 have tighter breakdown field

distribution as shown in Fig.3-7. The breakdown field of 8-9 MV/cm is achieved. The reasons for large variation of breakdown field of thinner oxide sample (< 20 nm) are possibly due to surface roughness. If the surface roughness of SiC is large, the electric field is partially enhanced at certain positions. The enhancement is more significant on samples with thinner oxide. The oxides of sample W0.5 and W5 were removed for AFM measurement. The AFM results are shown in Fig.3-8 (a) and Fig.3-8 (b). The root mean squire (RMS) roughness on SiC surface of the two samples are almost the same and the roughness does not depend on oxide thickness. The RMS value of sample W0.5 is 0.65 nm and that of sample W5 is 0.576 nm. Therefore, it is suspected that the surface roughness is the main reason for the early breakdown observed on the thin oxide samples. In summary, although wet oxidation results in high interface state density, the breakdown characteristic is reliable as the oxide is thicker than 26 nm.

The current transport mechanism is investigated by fitting the I-V characteristics with various transport models. The Fowler-Nordheim barrier height ($\Phi_{B,FN}$) is extracted by eq. 2-5. First, the $\ln(J/E^2)$ versus 1/E plot in the field of 6~10 MV/cm region is shown in Fig.3-9 (a). The slope gives the barrier height $\Phi_{B,FN}$. This value is related to the conduction band offset between SiO_2 and SiC. The theoretical value of Φ_B is 2.7 eV. The extracted $\Phi_{B,FN}$ values are shown in Fig.3-10. The $\Phi_{B,FN}$ decreases as the oxide thickness decreases. The possible reason is the surface roughness of the SiC substrate. The enhanced electric field causes the effective barrier height lowing. Sample W3 and W5 have barrier height larger than 2.7 eV. The reason is still unclear.

The Schottky-emission (SE) mechanism is examined according to eq. 2-6. The $\ln(J/AT^2)$ versus $E^{1/2}$ plot is shown in Fig.3-9 (b). The intercept of linear fitting of plot is related to the Schottky emission barrier height ($\Phi_{B,SE}$) and the slope of plot is

dielectric constant. The extracted $\Phi_{B,SE}$ value is shown in Fig.3-10. These values are slightly smaller than the theoretical value of 2.7 eV. Dielectric constant extracted by eq. 2-6 is shown in Fig.3-11. Those values are extremely lower than the theoretical dielectric constant of 3.9. Furthermore, the Frenkle-Poole (FP) emission barrier height ($\Phi_{B,FP}$) and dielectric constants are extracted by eq. 2-8. The ln (J/E) versus $E^{1/2}$ plot is shown in Fig.3-9 (c). The slope of the ln (J/E) versus $E^{1/2}$ plot is related to the dielectric constant and intercept of the plot is barrier height. The extracted $\Phi_{B,FP}$ value is shown in Fig.3-10. These values are about 1.8 eV. The extracted dielectric constant is shown in Fig.3-11. The values of sample W0.5 and W1 are close to the theoretical dielectric constant of 3.9 but the other samples have extremely lower dielectric constant.

In summary, FP emission is the main transport mechanism for samples W0.5 and W1 but the mechanisms for samples W2 W3 and W5 are still unclear. The electrical properties of all of the wet oxidation samples are summarized in Table 3-1.

3-2 High Temperature N_2O Oxidation

The gate dielectric of sample HT is grown by the directly oxidation at 1300 ℃ in N_2O ambient and is provided by the Industrial Technology Research Institute (ITRI). The effective oxide thickness is 104 nm. The high frequency and quasi-static C-V characteristics are shown in Fig.3-12. These two C-V curves are very close which implies that the interface state density is very low at conduction band edge. Fig.3-13 compares the extracted interface state density of sample HT with the sample W5. It is clear that the interface state density of sample HT is much lower than that of the wet oxidation sample. The interface state density at E_c-E = 0.4 eV is about 4.67×10^{10} $cm^{-2}eV^{-1}$ on sample HT.

The breakdown field distributions of sample HT and sample W5 are shown in Fig.3-14. The breakdown field of sample HT is lower than the sample W5. It is suspect that the lower breakdown field is due to the thick oxide. As the oxide thickness increases, the process induced defects may increase. These defects may percolate to a leakage path so that the breakdown is reduced. The extracted electrical properties of sample HT are summarized in Table 3-2.

3-3 N_2O and NH_3 Post-Oxidation Annealing

The gate dielectric of sample N was grown by wet oxidation at 1050 ℃ for one hour followed by N_2O annealing for 1 hr at 1100 ℃. This sample is designed to investigate the low temperature N_2O annealing effect. The wet oxide thickness is around 14.6 nm and the final gate dielectric thickness increases slightly to 15 nm after N_2O annealing. The gate dielectric of sample NH was grown by wet oxidation at 1050 ℃ for one hour followed by a 1.5 hr NH_3 post-oxidation annealing. After that, a 50-nm-thick nitride was deposited. The nitride deposition is used to increase the EOT to around 50 nm without high temperature oxidation. Sample NOH experienced sequential N_2O and NH_3 post-oxidation annealing. After that, nitride layer was deposited. The cross-sectional TEM micrograph of sample NOH is shown in Fig.3-15. The actual silicon dioxide layer is around 12.8-nm-thick. A 2~3-nm-thick interfacial layer is formed between the Si_3N_4 layer and the SiO_2 layer. This interfacial layer is identified as SiON by EDS analysis. The thickness of the Si_3N_4 layer is around 33 nm. The high frequency C-V characteristics of sample W1, N, NH, NOH and HT are compared in Fig.3-16. Samples W1 and N exhibit almost identical C-V curves and flat-band voltage. The flat-band voltage does not shift significantly after N_2O annealing. This phenomenon indicates that no more effective charges occur after N_2O

post-oxidation annealing. The C-V curves of samples NH and NOH are slightly "stretched-out" compared to that of sample W1. The reason will be discussed later.

The interface state density extracted by hi-lo C-V method is shown in Fig.3-17. Either N_2O annealing or NH_3 annealing can improve the interface quality separately. Among them, sample NOH has the lowest interface state density except the sample HT. This result indicates that the N_2O and NH_3 treatment has superposition property. The values of the interface state density of samples N, NH, and NOH are 3.87 $x10^{11}$, 3.67 $x10^{11}$, and 2.92 $x10^{11}$ $cm^{-2}eV^{-1}$, respectively, at E_c-E = 0.4 eV. The mechanism of interface state passivation is related to nitrogen pile up at SiO_2/SiC. Possible chemical reaction of N_2O annealing has been proposed in ref [41]. N_2O decompose to N_2 and O_2 at high temperature.O_2 reacts with N_2O to form NO. The NO diffusion in SiO_2 causes the nitrogen piling up.

The I-V characteristics of samples N, NH, and NOH are shown in Fig.3-18 (a), (b), and (c), respectively, and the breakdown field distribution is shown in Fig.3-19. Although sample N has higher Median breakdown field than sample W1, the breakdown field variation of sample N is similar to that of sample W1. The higher Median breakdown field implies that the oxide quality in bulk is improved by N_2O annealing. The large variation implies that N_2O annealing does not smooth the SiC surface roughness. The Median breakdown field is around 10 MV/cm on sample NH and sample NOH and the distribution is quite tight.

Early breakdown phenomenon occurs on samples W0.5, W1, W2, and N. These samples have thin wet oxide as gate dielectric. No early breakdown is observed on sample NH and NOH. The main difference between these two groups is the nitride deposition. The early breakdown is attributed to some weak spots in the dielectric. If the weak spots in the wet oxide do not coincide with the weak spot in the nitride layer, early breakdown could be suppressed because current path is hard to form. Using gate

dielectric stack to improve dielectric yield has been studied in 1990s [42] and can be used on SiC MOS devices. The extracted electrical properties of samples W1, N, NH, and NOH are summarized in Table 3-3.

3-4 NH_3 Plasma Treatment

In this catalog, SiC substrate was wet oxidized at 1050 ℃ for 5 hour followed by NH_3 plasma treatment. The plasma treatment was performed at only 300 ℃. This is the lowest thermal budget in this thesis.

The C-V characteristics of sample P150.10 is shown in Fig.3-20. We can see the quasi-static C-V and high frequency C-V curves are very close, which indicates that the interface state density is reduced by NH_3 plasma treatment. It is supposed that the nitrogen provided by NH_3 could passivate the C-cluster-like defects. However, a 0.5~1 V positive shift of flat-band voltage is observed on all of the plasma treated samples as shown in Fig.3-21. The shift and variation of flat-band voltage depends on neither the plasma power nor the treatment period. Furthermore, the variation of flat-band voltage after plasma treatment is larger than that before plasma treatment. The origin of the negative charges is not clear at this moment.

The interface state densities at E_c-E = 0.4 eV of the plasma treated samples E_c-E = 0.4 eV are compared in Fig.3-22. All of the samples experienced plasma treatment has apparently lower interface state density than the reference sample W5. The trends of interface improvement by plasma treatment at 150 W and 200 W are similar. The interface state density decreases as the plasma treatment time increases from 2 minutes to 5 minutes and gradually saturates as the plasma treatment time increases to 10 minutes. At the same plasma treatment time, 200 W results in slightly higher interface state density than 150 W. It is suspected that higher plasma energy produces

additional interface defects due to the stronger radiation. As the plasma energy decreases to 100 W, the interface state density saturates at around $2x10^{11}$ $cm^{-2}eV^{-1}$ even if the treatment time extends to 15 minutes. It is thus concluded that 150 W 10 minutes is the optimized condition. Lower energy cannot passivate interface states effectively. Higher energy would generate additional defects. The improvement saturate after 10 minutes. Longer treatment time is not necessary.

The breakdown field distributions of the plasma treatment sample are shown in Fig.3-23. Except few early breakdown devices, the distribution of each sample is very tight and the breakdown field is within 8-9 MV/cm. This value is almost equal to the 5 hours wet oxidation sample W5, which means the plasma treatment process does not damage the bulk quality of the thermal oxide. The extracted electrical properties of the plasma treatment samples are summarized in Table 3-4.

3-5 Dielectric Stacks

In previous sub-sections, a wet oxidation at 1050 ℃ was performed and it is observed that the C-cluster-like defects has been saturated at this process. In this section, we evaluate the interface quality by direct depositing a plasma vapor chemical vapor deposition (PECVD) oxide on SiC substrate. No oxidation of the SiC substrate is performed so that the C clusters produced during wet oxidation process is avoided.

Sample ONO has an oxide/nitride/oxide sandwiched gate dielectric. The top and bottom oxide layers are PECVD oxide. The middle layer is a LPCVD nitride. The C-V characteristic is shown in Fig.3-24. We can see apparent C-V distortion and large separation between quasi-static C-V and high frequency C-V curves. This indicates that very high interface state density exists near the conduction band edge. The

flat-band voltage of sample ONO is 5.64 V which indicates a large effective oxide charge of $-1.65 \times 10^{12}/cm^2$. These negative charges may exist at the oxide/nitride interfaces or the traps in the nitride layer.

The interface state density extracted by hi-lo C-V method is shown in Fig.3-25. The interface state density of sample ONO is much higher than that of the wet oxide sample W5. This result indicates that suitable oxidation or post deposition oxidation/annealing must be performed. The breakdown field distribution of sample ONO is shown in Fig.3-26. A wide distribution is observed. In sub-section 3-3, it is observed that the nitride/oxide stack can reduce the breakdown field variation effectively, however, sample ONO still exhibits wide breakdown field variation. It is suspected that the quality of the bottom PECVD oxide is too poor. It should be noted that as the bottom oxide is leaky, electron can tunnel into the nitride layer easily. This may explain the large amount negative charges calculated from the high flat-band voltage. The extracted electrical properties of sample ONO is summarized in Table 3-5.

3-6 High Temperature Measurement

As has been mentioned in chapter-2, the interface states can be measured is in the range of E_c-E = 0.2~0.6 eV at room temperature. To extract deep level interface states, high temperature measurement would be required. The deep level interface states can respond measurement signal at high temperature. Deep level interface states up to E_c-E = 1.6 eV can be detected at 523 K as shown in Fig.2-3. In this sub-section, deep level interface states of samples NOH, HT, and P150.10 are measured because these samples have the lowest interface state density in each category.

The high frequency C-V characteristics of sample NOH at various temperatures

are shown in Fig.3-27. The flat-band voltage decreases from 0.5 V to 0.24 V as the temperature increases from 298 K to 523 K. The flat-band shift is almost equal to the change of work function difference between Al and 4H-SiC when temperature increases. When sample is cooled down to room temperature, the C-V curves return to its original position. The quasi-static C-V characteristics of sample NOH at 298 K and 523 K are shown in Fig.3-28. No significant C-V shift is observed when temperature goes high but a visible distortion at high temperature is observed. This distortion implies that more deep level interface states are measured at 523 K.

Interface state density measured at various temperatures of samples NOH, HT, and P150.10 are shown in Fig.3-29, Fig.3-30, and Fig.3-31, respectively. The full range interface state densities of these three samples are compared in Fig.3-32. The highest value of the interface state density measured at different temperatures is selected to plot this figure. Sample HT has the lowest interface state density in the range of E_c-E = 0.2-0.8 eV. As E_c-E > 1 eV, the three samples have the same interface state densities. These results indicate that all of the interface state passivation techniques can reduces the shallow level interface states only. Sample P150.10 has higher interface states in the range of 0.6-0.8 eV compared to other samples. The plasma treatment does not passivate the interface states in this range and additional interface states were produced. The states near conduction band are usually regarded as accepter-like traps. Those traps usually capture electrons. The trapped electrons cause the C-V positive flat-band shift.

To understand if the interface state passivation is attributed to nitrogen or not, depth profiles of N, H, O, C, and Si were analyzed by secondary ion mass spectroscope (SIMS). Fig.3-33(a) shows the SIMS profiles of the HT sample. Nitrogen pile-up at the SiO_2/SiC interface is observed. However, the nitrogen pile-up phenomenon is not observed on the samples NOH and P150.10 as shown in

Figs.3-33(b) and (c), respectively. A peak of hydrogen signal at the SiO_2/SiC interface is observed on each samples. It is not clear if this peak is due to hydrogen pile-up or due to the matrix effect of the SIMS analysis.

We speculate that nitrogen radicals diffuse through oxide slowly. The oxide layer on SiC is thicker than 13 nm. If the process temperature is not high enough, the amount of nitrogen radicals reaching the SiO_2/SiC interface is not large enough. Sample HT is directly oxidized at high temperature in N_2O ambience so that nitrogen obviously piles up at the interface. These would explain the reason why the interface state density is not effectively improved by low temperature processes. Plasma treatment has the lowest thermal budget. Only hydrogen can reach the SiO_2/SiC interface. It is suspect the hydrogen can passivate shallow traps but not deep traps so that the interface state in the region of 0.5-0.8 eV is not improved on the plasma treated sample P150.10.

Fig.3-34 shows the quasi-static C-V of sample P150.10. An abnormal peak occurs as the measurement temperature is higher than 473 K. The large peak occurs at around V_G = 1 V, under which the SiC surface changes from weak inversion to depletion state. The I-V characteristic of sample P150.10 at various temperatures is shown in Fig.3-35. We can see a current peak at around V_G = 1 V as the temperature is higher than 473 K. The peak position is the same as that of the quasi-static C-V peak. Those abnormal phenomena are explained as follow.

The quasi-static C-V is obtained by measuring current and then convert current to capacitance by C = I/(dV/dt). As the gate voltage ramped down from positive voltage toward negative voltage, mobile ions in gate dielectric will be drifted from SiC substrate toward gate electrode. The mobile ion induced current adds on the capacitance displacement current, therefore, a capacitance peak is recorded. This phenomenon is identical to that observed on the measurement of mobile ion by the

triangular voltage sweep (TVS) method. Fig.3-36(a) shows the quasi-static C-V characteristic and the high frequency C-V measured at 523 K. The mobile ion density is estimated to be $3.97x10^{11}$ cm^{-2}. Mobile ion density is also extracted by the bias temperature stress (BTS) method. The temperature is 473 K and the bias is ±1.33 MV/cm. The stress time is 30 minutes. The high frequency C-V characteristics are measured at room temperature after negative and positive bias stress as shown in Fig.3-36(b). The Mobile ion is calculated from the flat-band voltage shift and the result is $1.65x10^{11}$ cm^{-2}. This value is consistent with that extracted by the TVS method. Thus, we conclude that the peak of the quasi-static C-V curve is attributes to mobile ions and the peak does not occur in the high frequency C-V curve because mobile ions can't respond the stepping of the gate bias even at 523 K.

The quasi-static C-V curve of sample NOH has no the abnormal peak. Fig.3-37 shows the high frequency C-V curves after negative bias stress and positive bias stress at 523K for 30 minutes. The electric field is 1 MV/cm. The mobile ions of this sample are lower than the detection limit of this BTS condition. This result implies that the mobile ions observed in sample P150.10 is closely related to the wet oxidation process because abnormal quasi-static C-V peak also occurs at sample W5. The quasi-static C-V curve of sampleW5 is shown in Fig.3-38.

3-7 Summary of Interface State Density Characteristic

Interface state densities of representative samples in this thesis are shown in Fig. 3-39. Sample ONO has the lowest thermal budget. However, it has the highest interface state density among all samples. It is also suspected that the PECVD oxide on SiC exhibits poor quality. Further analysis is required. Various nitridation processes such as N_2O oxidation, N_2O post-oxidation annealing, NH_3 post-oxidation

annealing, and NH_3 plasma post-oxidation treatment can reduce the interface state density. The N_2O post-oxidation annealing and NH_3 post-oxidation annealing have superimposed effect (sample NOH). However, suitable NH_3 plasma treatment achieves the lowest interface state density among these low thermal budget samples. The interface state density at E_c-E = 0.4 eV of sample P150.10 is 1.37×10^{11} $cm^{-2}eV^{-1}$. It should be noted that the interface state density of the high temperature N_2O oxidation (sample HT) is 3 times lower than that of sample P150.10. To achieve very low interface state, novel low thermal budget processes must be developed. Otherwise high thermal budget process is still unavoidable.

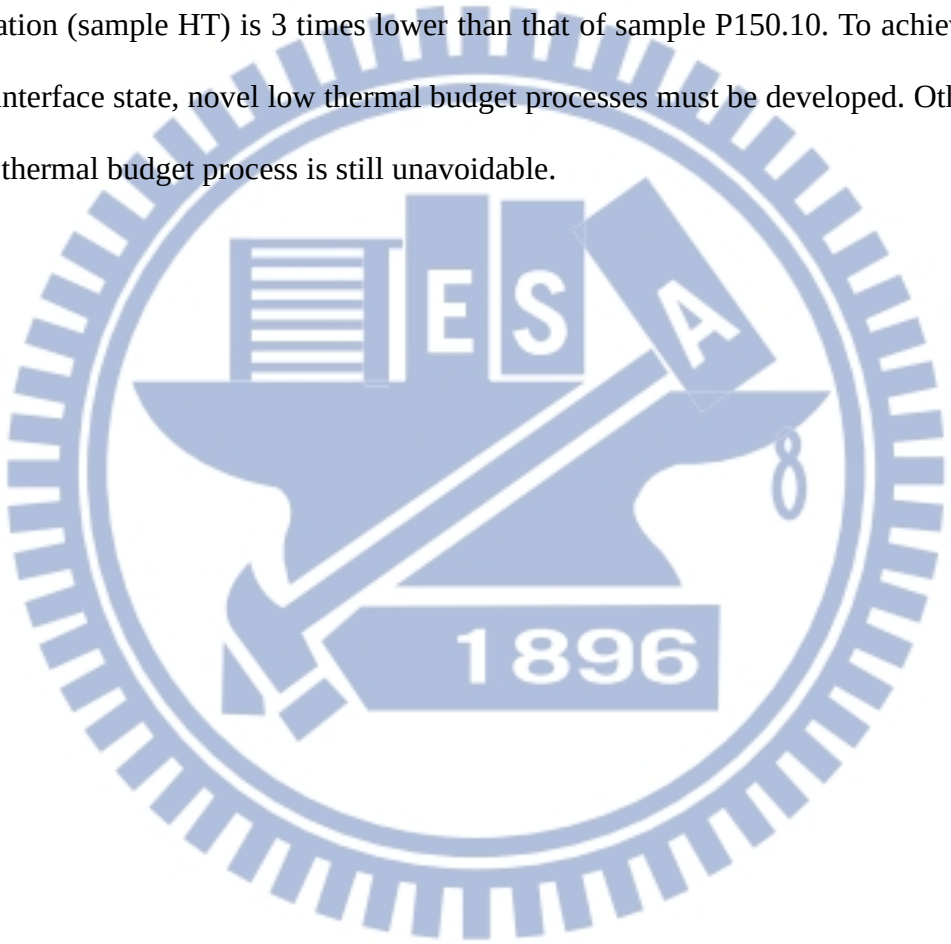


Table 3-1 The electrical properties of all of the wet oxidation samples are summarized.

Sample	**W0.5**	**W1**	**W2**	**W3**	**W5**
Effective Thickness (nm)	**9.5**	**14.6**	**20**	**26**	**32**
Average V_{FB} (V)	**0.29**	**0.25**	**0.252**	**0.28**	**0.563**
D_{it} ($cm^{-2}eV^{-1}$) at E_c-E = 0.4 eV	**$5.91x10^{11}$**	**$5.75 x10^{11}$**	**$5.02x10^{11}$**	**$4.8x10^{11}$**	**$5.47x10^{11}$**
Median value of Breakdown Field (MV/cm)	**7.54**	**6.7**	**8.93**	**8.83**	**9**
Standard Deviation	**1.24**	**2.1**	**1.54**	**0.2**	**0.75**

Table 3-2 The electrical properties of high temperature N_2O sample is summarized.

Sample	**HT**
Effective Thickness (nm)	**104**
Average V_{FB} (V)	**0.12**
D_{it} ($cm^{-2}eV^{-1}$) at E_c-E = 0.4 eV	**$4.67x10^{10}$**
Median value of Breakdown Field (MV/cm)	**6.11**
Standard Deviation	**1.41**

Table 3-3 The electrical properties of all of N_2O and NH_3 post-oxidation annealing are summarized.

Sample	W1	N	NH	NOH
Effective Thickness (nm)	14.6	15	37.9	39.36
Average V_{FB} (V)	0.25	0.31	0.56	0.52
D_{it} ($cm^{-2}eV^{-1}$) at E_c-E = 0.4eV	$5.75x10^{11}$	$3.87x10^{11}$	$3.67x10^{11}$	$2.92x10^{11}$
Median value of Breakdown Field (MV/cm)	6.7	9.88	10.5	9.69
Standard Deviation	2.1	3.21	0.76	0.82

Table 3-4 The electrical properties of all of NH_3 post oxidation plasma treatment are summarized.

Sample	W5	P100.10	P100.15	P150.2	P150.5
Average V_{FB} (V)	0.563	1.04	0.936	1.048	0.955
D_{it} ($cm^{-2}eV^{-1}$) at E_c-E = 0.4eV	$5.47 x10^{11}$	$2.23x10^{11}$	$2.23x10^{11}$	$3.15x10^{11}$	$1.44x10^{11}$
Median value of Breakdown Field (MV/cm)	9	8.07	9	9.02	9.05
Standard Deviation	0.75	0.23	1.85	0.88	1.05
Sample	P150.10	P200.2	P200.5	P200.10	
Average V_{FB} (V)	1.04	1.11	1.19	1.07	
D_{it} ($cm^{-2}eV^{-1}$) of E_c-E = 0.4eV	$1.37x10^{11}$	$2.79x10^{11}$	$1.99x10^{11}$	$1.84x10^{11}$	
Median value of Breakdown Field (MV/cm)	8.94	8.51	9.07	9.23	
Standard Deviation	1.87	0.64	0.36	0.19	

Table 3-5 The electrical properties of dielectric stacks sample is summarized.

Sample	**ONO**
Effective Thickness (nm)	**67.8**
Average V_{FB} (V)	**5.64**
D_{it} ($cm^{-2}eV^{-1}$) of E_c-E = 0.4eV	**$1.67x10^{12}$**
Median value of Breakdown Field (MV/cm)	**8.56**
Standard Deviation	**2.97**

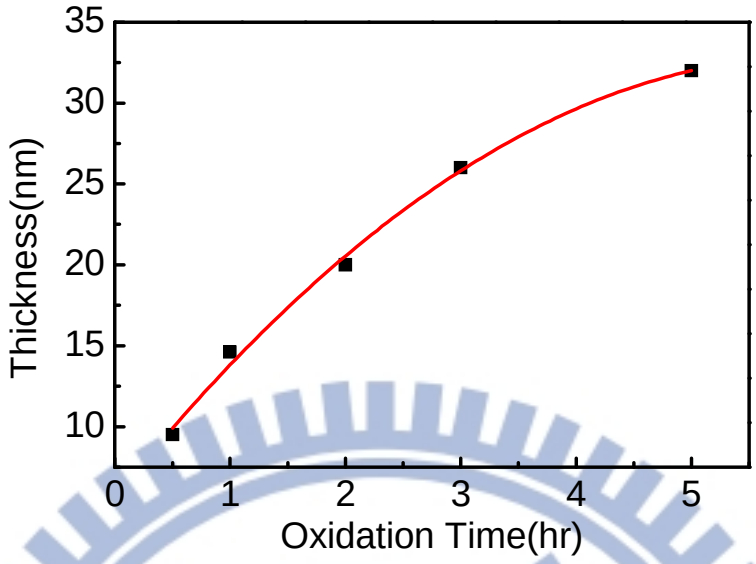


Fig.3-1 Thickness of wet O_2 1050 ℃ as a function of oxidation time. Thickness is determined by accumulation capacitance (C_{ox}).

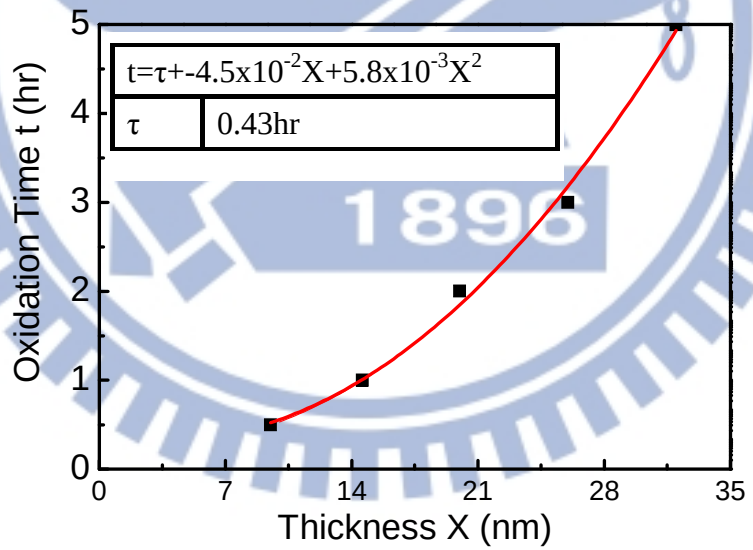


Fig.3-2 Thickness (X)-oxidation time (t) plot is fitted by a second order polynomial. The τ value can be extracted by the second order polynomial fitting.

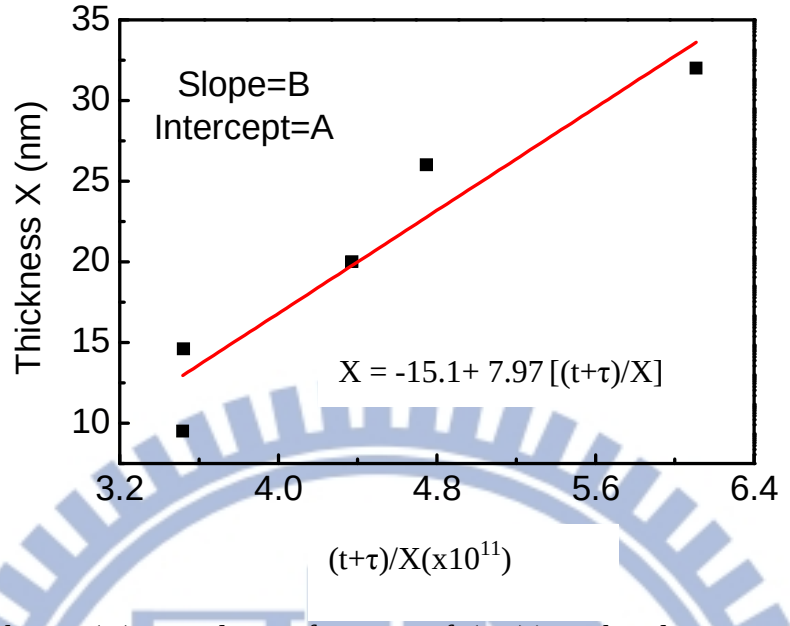


Fig.3-3 Thickness (X) as a linear function of (t+τ)/X. The slope is parabolic rate constant (B) and intercept is (A).

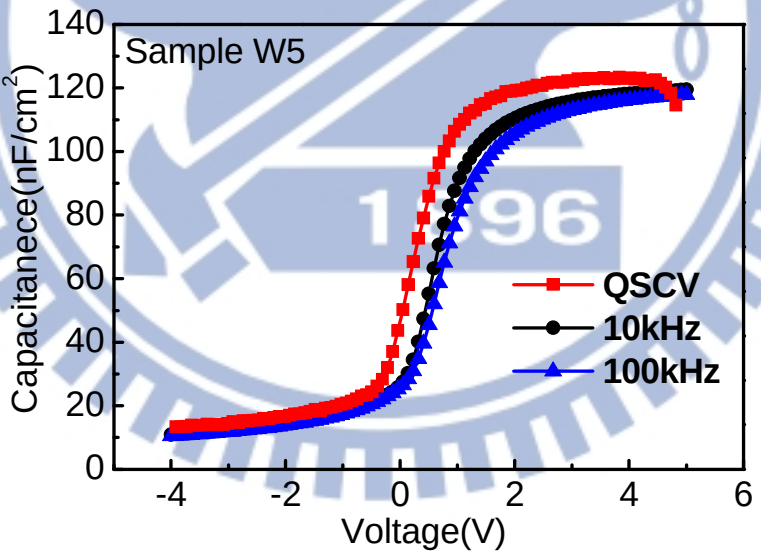


Fig.3-4 C-V characteristics of sample W5. It is observed that the C-V curves shift toward negative voltage axis with the decreasing of measurement frequency.

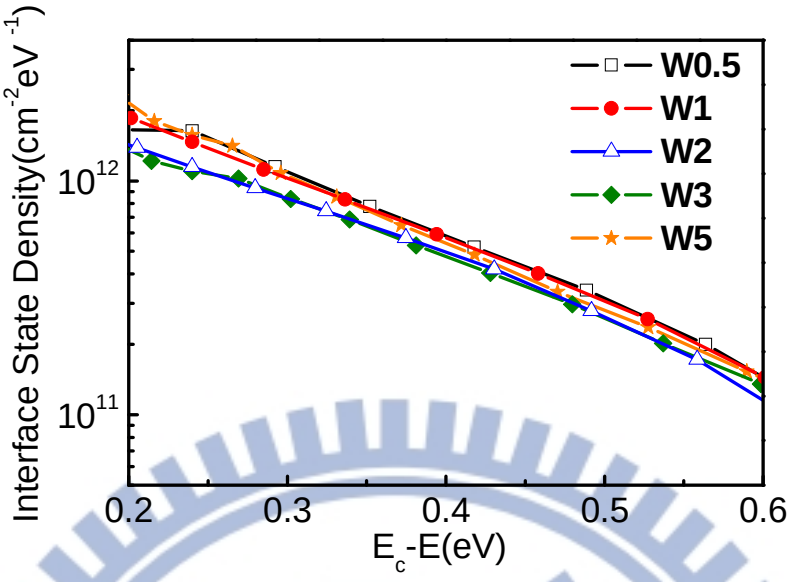


Fig.3-5 Interface state density characteristic of wet oxidation samples are summarized.

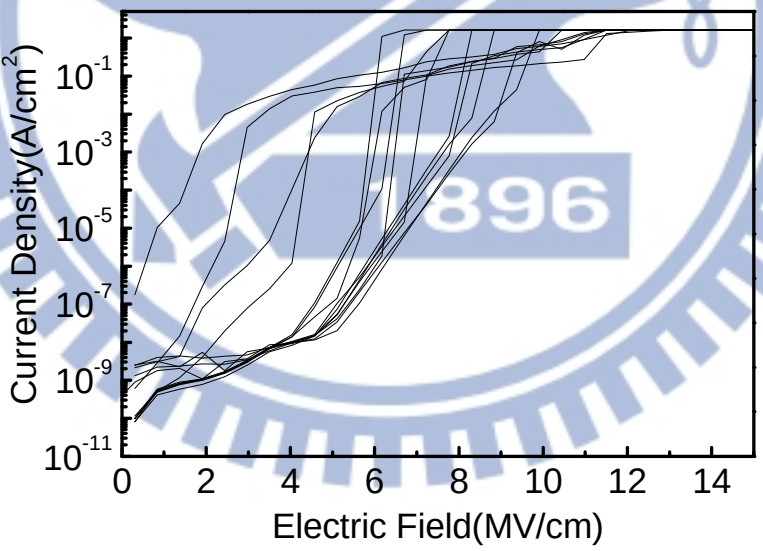


Fig.3-6 Current density versus electric field (J-E) characteristics of the sample W1.

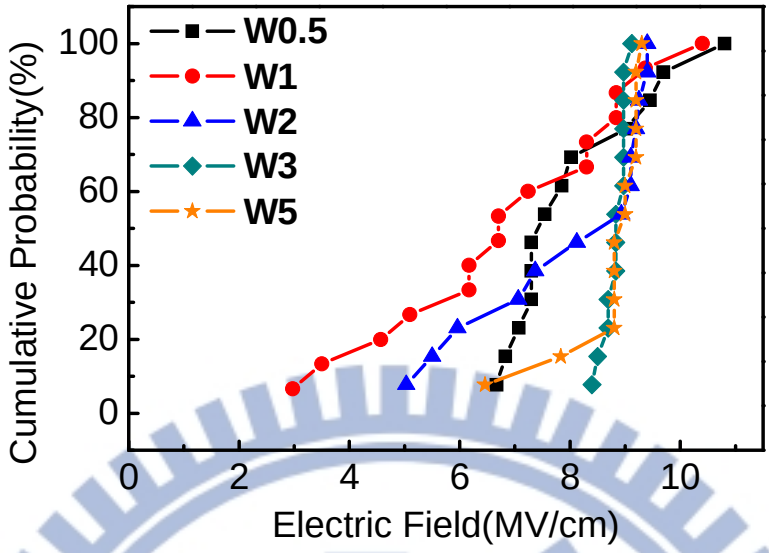
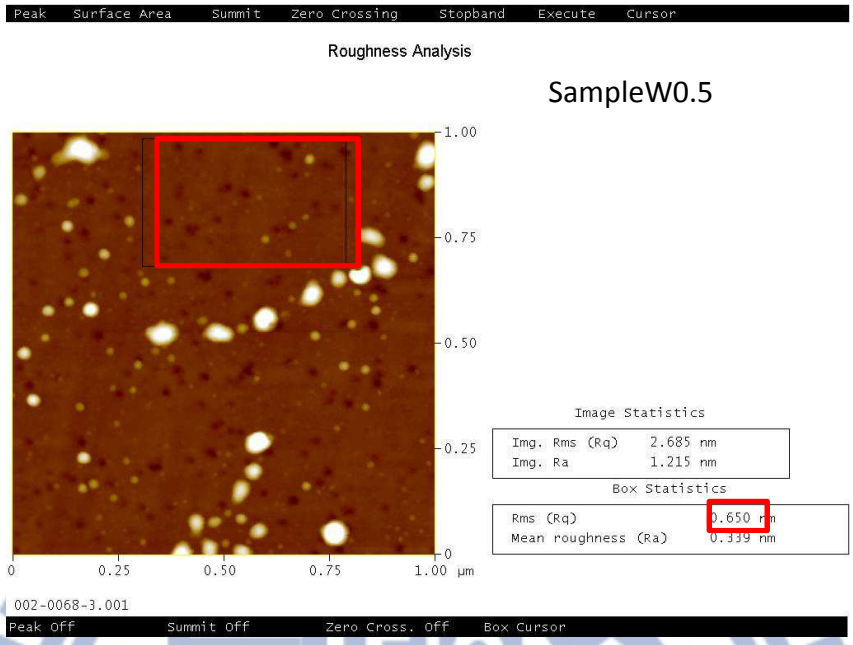


Fig.3-7 Breakdown field distributions of only wet oxidation samples. The samples with thinner oxide, W0.5, W1, and W2, exhibit wide distribution of breakdown field while the samples W3 and W5 have tighter breakdown field distribution.

(a)



(b)

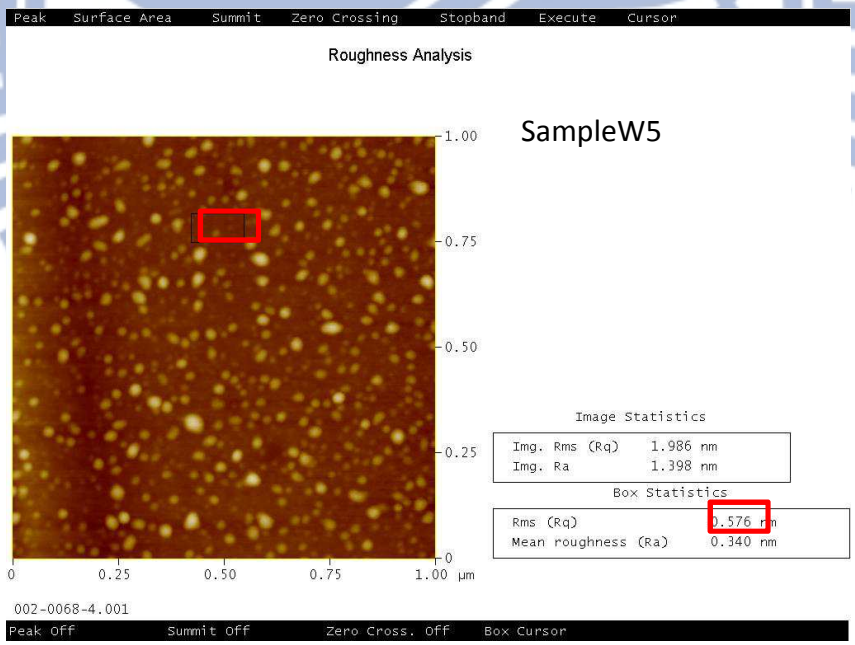
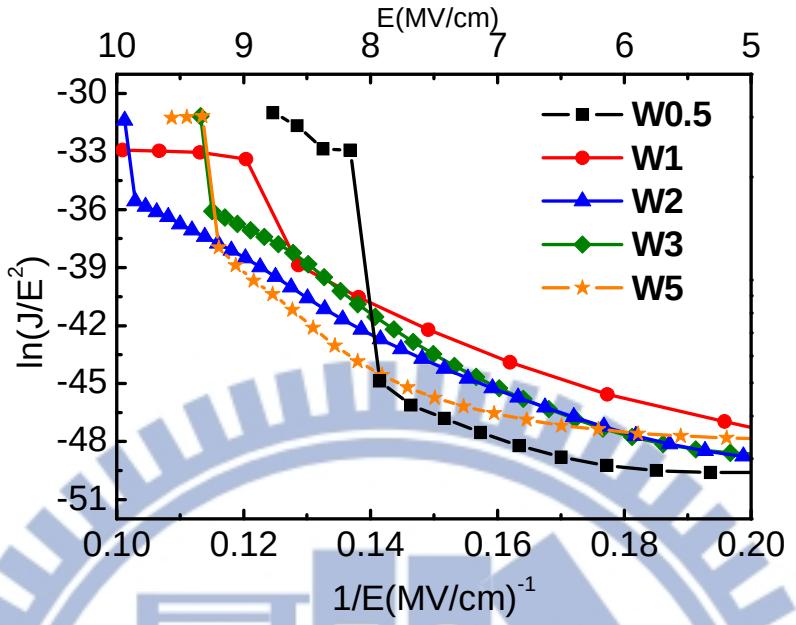
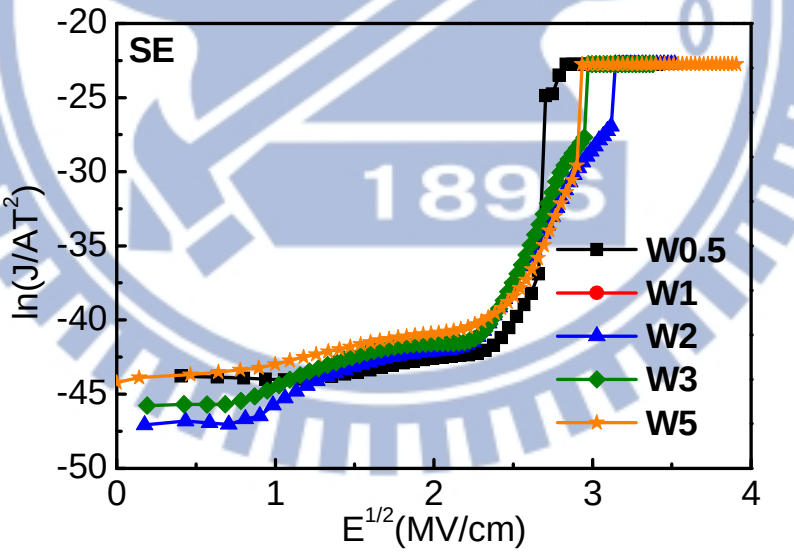


Fig.3-8 (a) SiC surface roughness root mean squire (RMS) value of sample W0.5. The value of sample W0.5 is 0.65 nm. (b) SiC surface roughness root mean squire (RMS) value of sample W5. The value of sample W5 is 0.576 nm.

(a)


E(MV/cm)
10
9
8
7
6
5
-30
-33
-36
-39
-42
-45
-48
-51
ln(J/E²)
0.10
0.12
0.14
0.16
0.18
0.20
1/E(MV/cm)⁻¹
W0.5
W1
W2
W3
W5

(b)


SE
-20
-25
-30
-35
-40
-45
-50
ln(J/AT²)
0
1
2
3
4
E^1/2(MV/cm)
W0.5
W1
W2
W3
W5

(c)

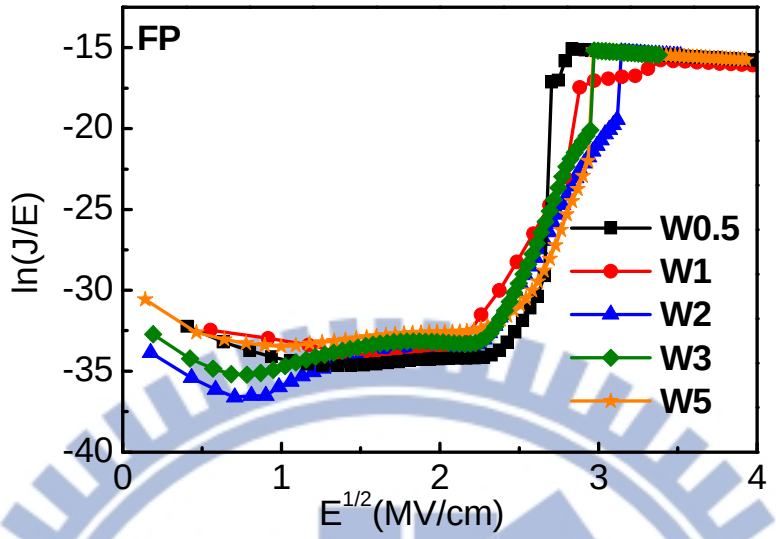


Fig.3-9 (a) The ln (J/E^2) against 1/E plot of Fowler-Nordheim linear fit with varying oxidation time. (b) The ln (J/AT^2) against $E^{1/2}$ plot of Schottky-Emission (SE) linear fit with varying oxidation time. (c) The ln (J/E) against $E^{1/2}$ plot of Frenkle-Poole (FP) linear fit with varying oxidation time.

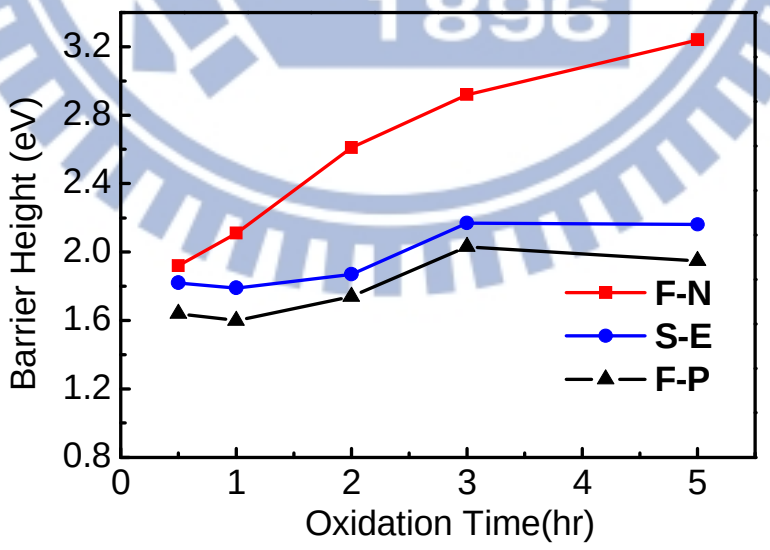


Fig.3-10 Barrier heights extract from Fowler-Nordheim tunneling (FN), Schottky Emission (SE), and Frenkle-Poole (FP) as the function of wet oxidation time. The

theoretical barrier height is 2.7eV for FN and SE.

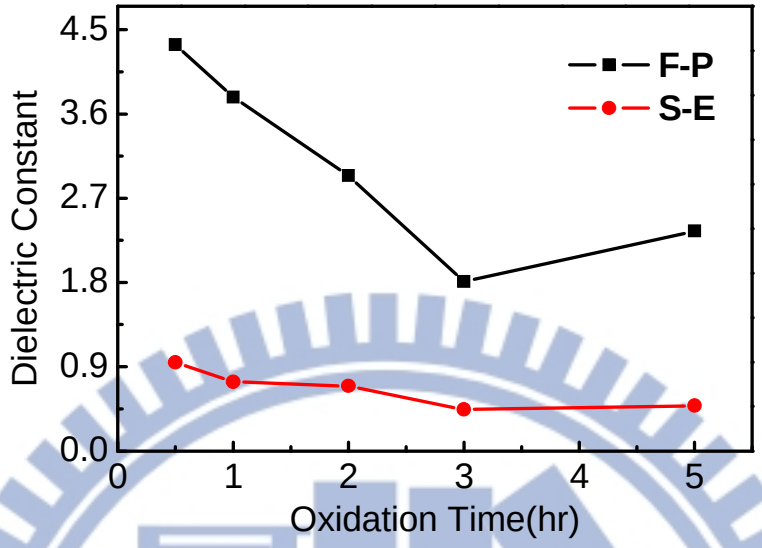


Fig.3-11 Dielectric constants extract from Frenkel-Poole (FP) and Schottky emission (SE) as the function of wet oxidation time. The theoretical dielectric constant is 3.9.

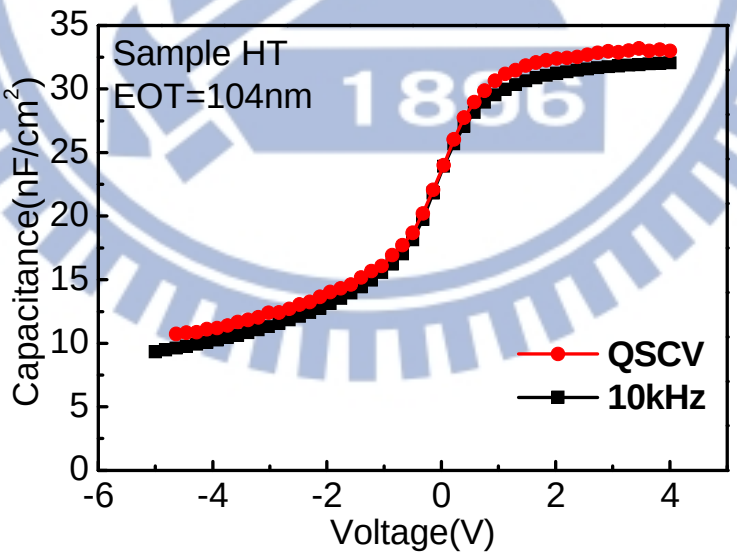


Fig.3-12 High-low CV characteristic of sample HT.

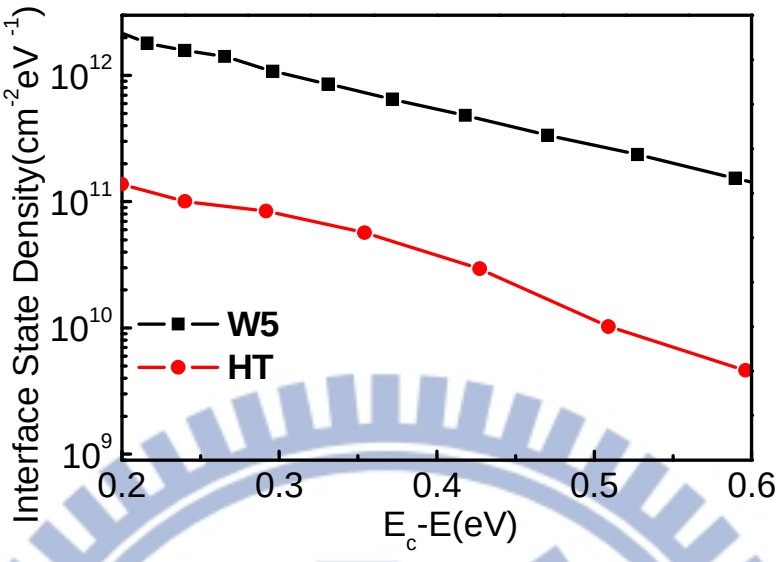


Fig.3-13 The extracted interface state density of sample HT and the sample W5.

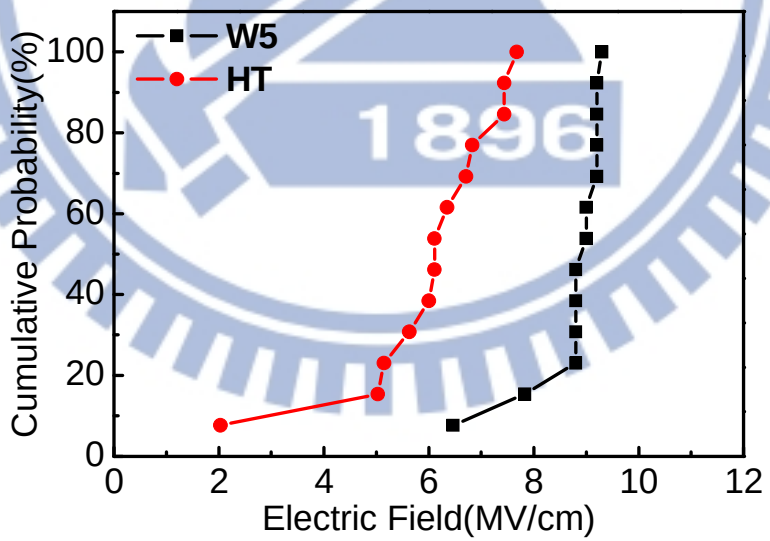


Fig.3-14 Breakdown field distributions of sample HT and sample W5

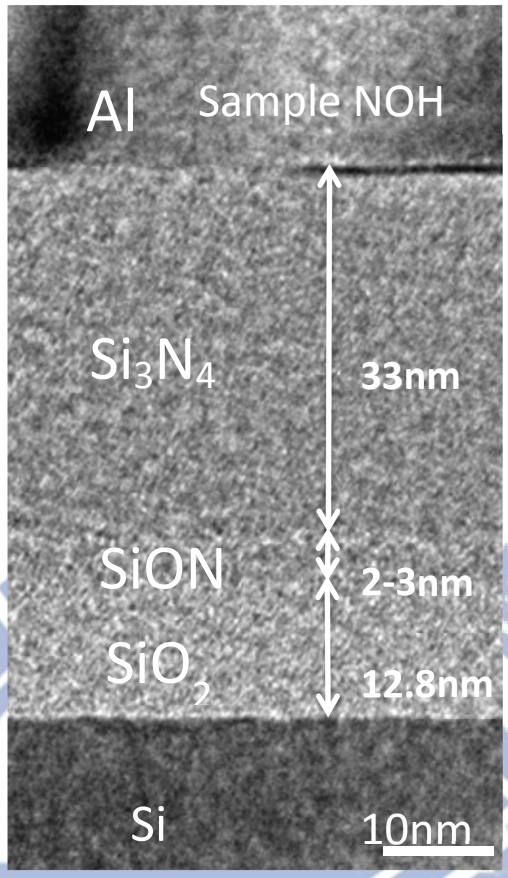


Fig.3-15 Cross sectional TEM micrograph of sample NOH (W1+ N_2O + NH_3 + Si_3N_4).

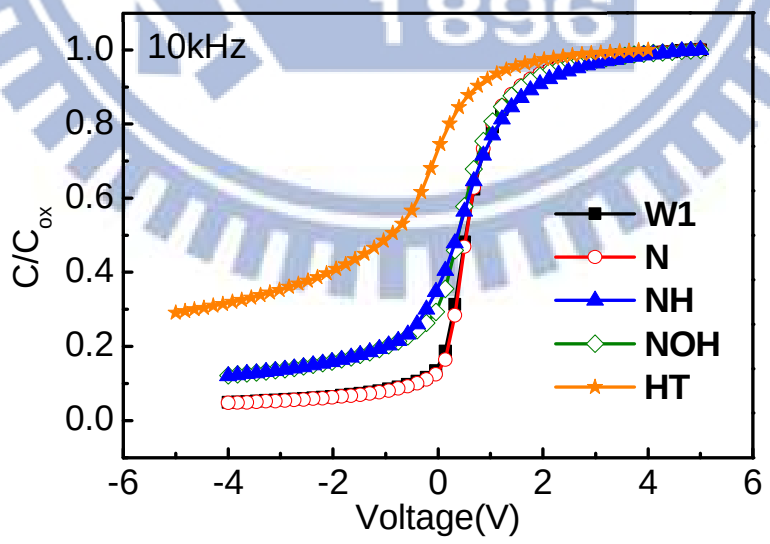


Fig.3-16 The high frequency C-V characteristics of sample W1, N (W1 + N_2O), NH (W1 + NH_3 + Si_3N_4), NOH (W1 + N_2O + NH_3 + Si_3N_4) and HT are compared.

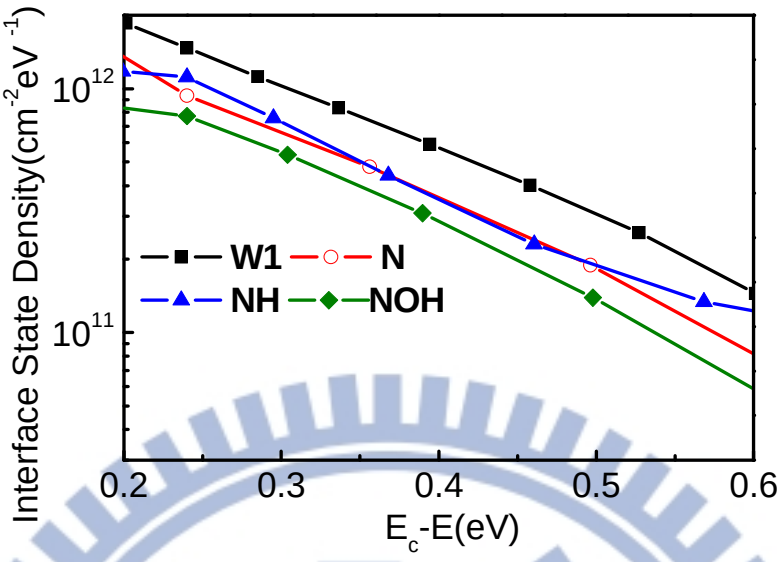
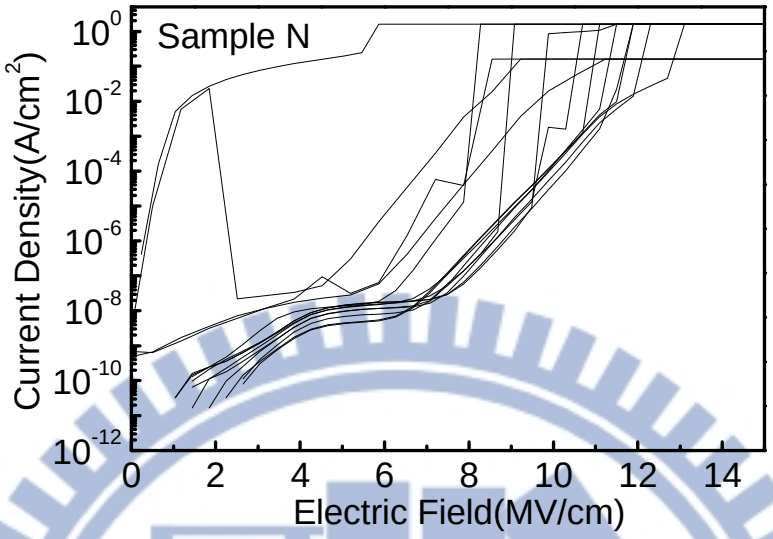
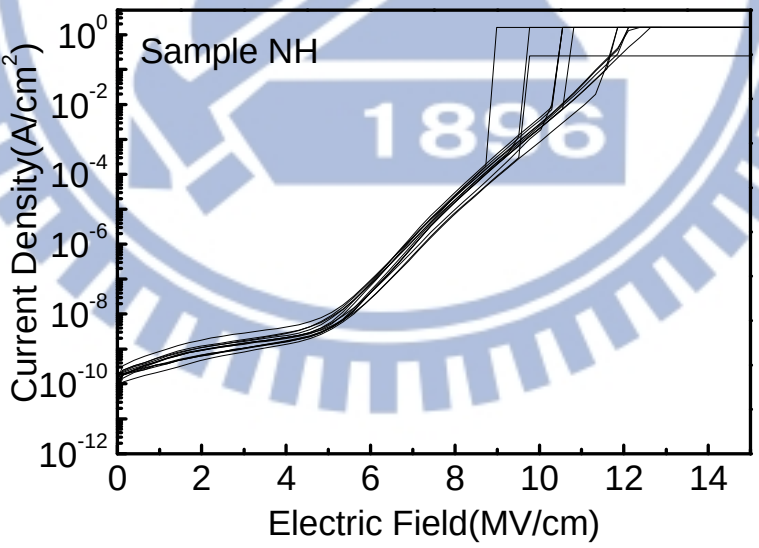


Fig.3-17 The interface state density of sample W1, N (W1 + N_2O), NH (W1 + NH_3 + Si_3N_4), NOH (W1 + N_2O + NH_3 + Si_3N_4) and HT are extracted by hi-lo C-V method.

(a)


Sample N
Current Density(A/cm2)
Electric Field(MV/cm)

(b)


Sample NH
Current Density(A/cm2)
Electric Field(MV/cm)

(c)

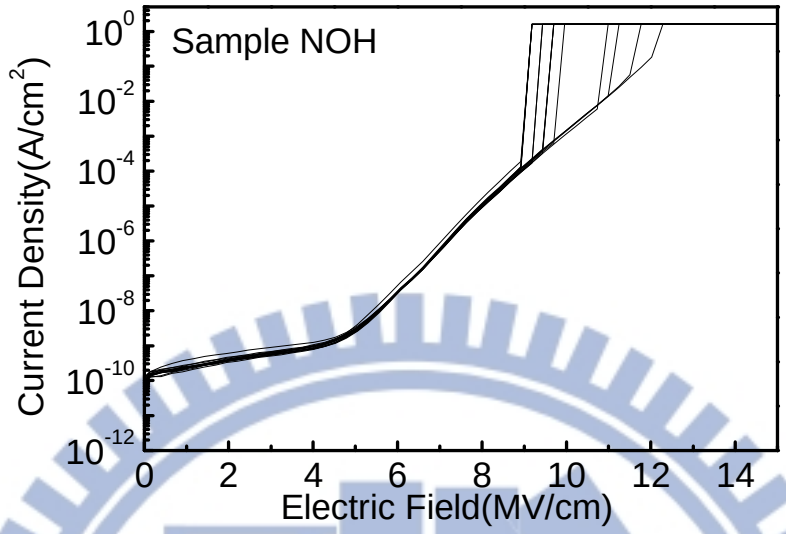


Fig.3-18 The Current density versus electric field (J-E) characteristic of sample (a) N (W1 + N_2O), (b) NH (W1 + NH_3 + Si_3N_4), (c) NOH (W1 + N_2O + NH_3 + Si_3N_4)

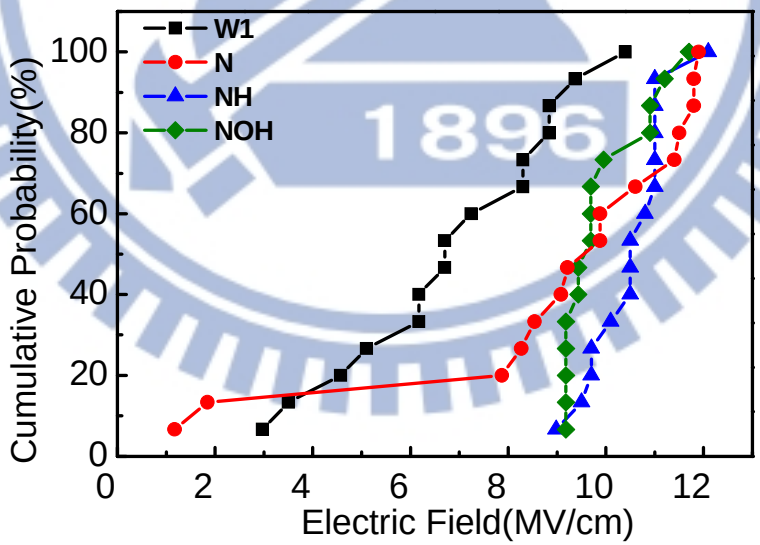


Fig.3-19 Breakdown field distributions of sample W1, N (W1 + N_2O), NH (W1 + NH_3 + Si_3N_4), NOH (W1 + N_2O + NH_3 + Si_3N_4)

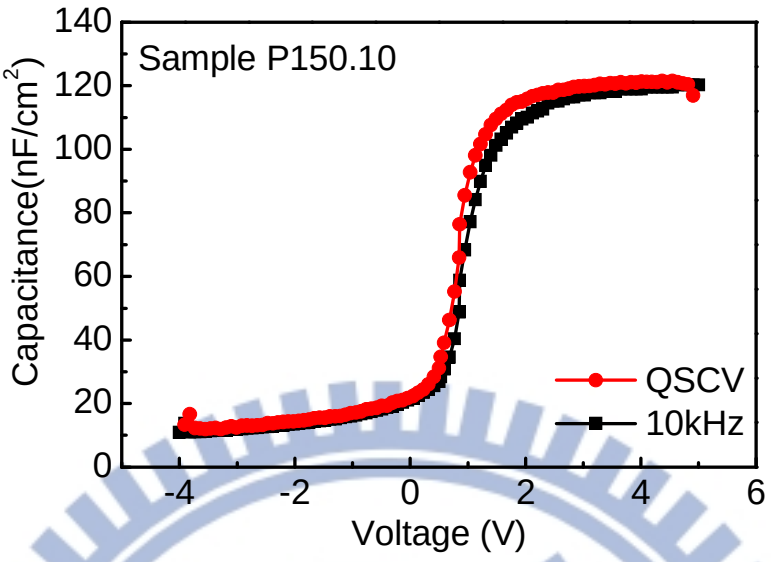


Fig.3-20 High-low CV characteristic of sample P150.10.

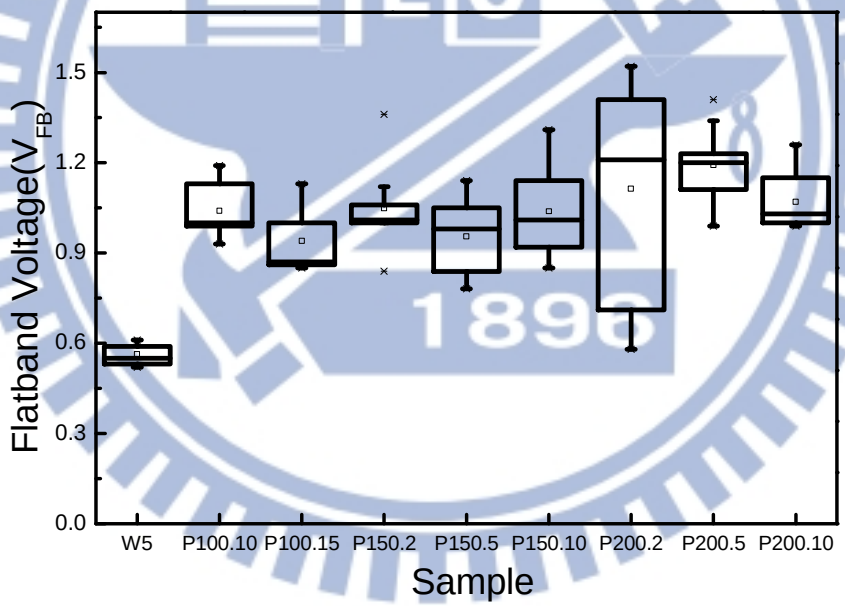


Fig.3-21 Flat-band voltage distribution of high frequency CV of NH_3 plasma treatment samples.

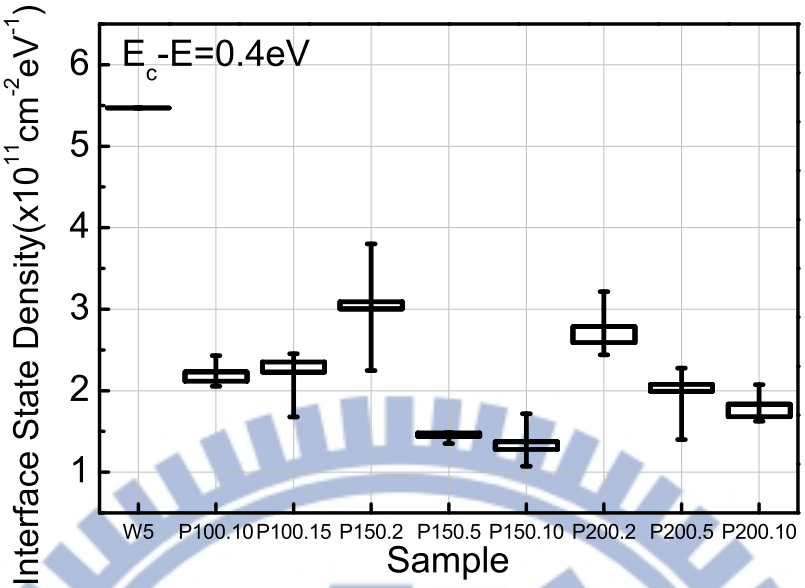


Fig.3-22 Interface state density at E_c-E= 0.4 eV characteristic of sample W5, P100.10, P100.15, P150.2, P150.5, P150.10, P200.2, P200.5, and P200.10 are compared.

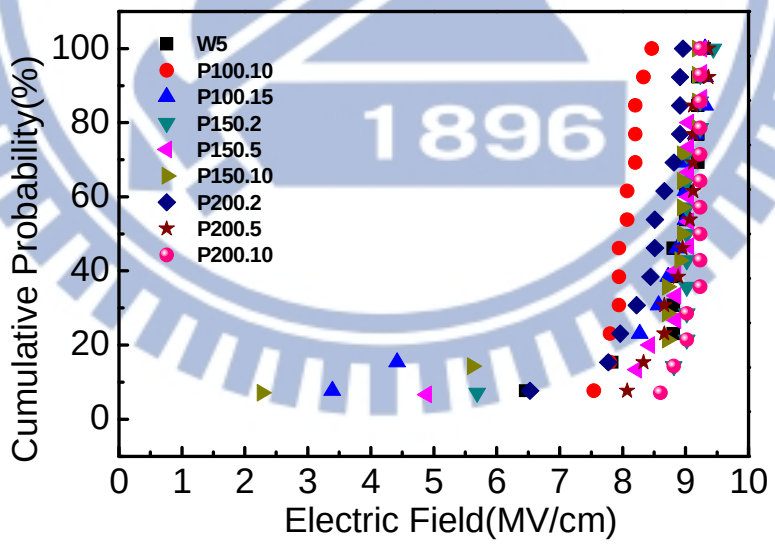


Fig.3-23 Breakdown field distributions of W5 and all NH_3 plasma treatment samples.

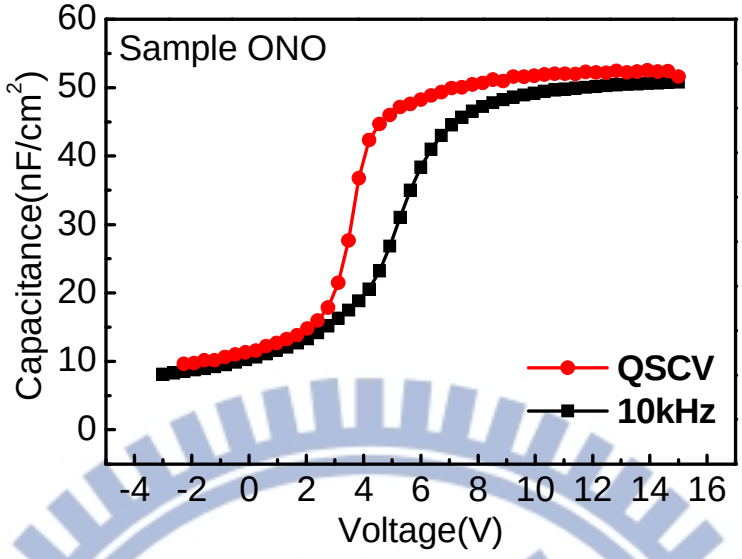


Fig.3-24 High-low CV characteristic of sample ONO.

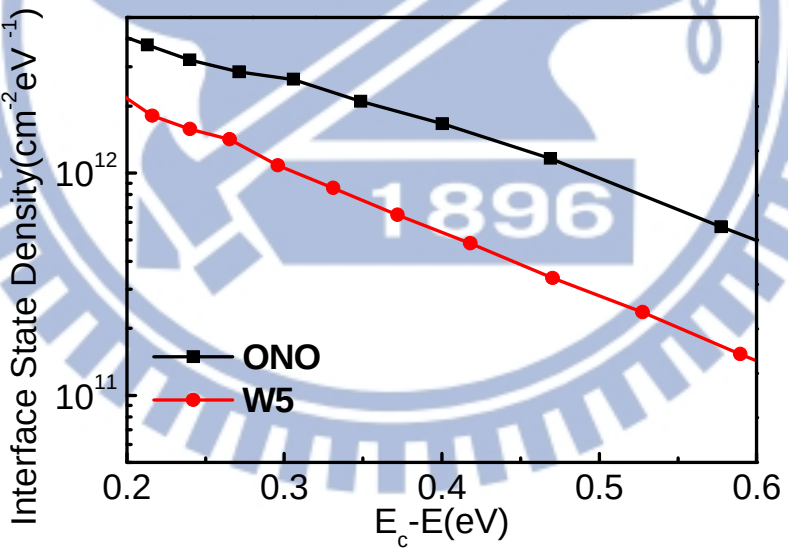


Fig.3-25 Interface state density characteristic of sample ONO and W5.

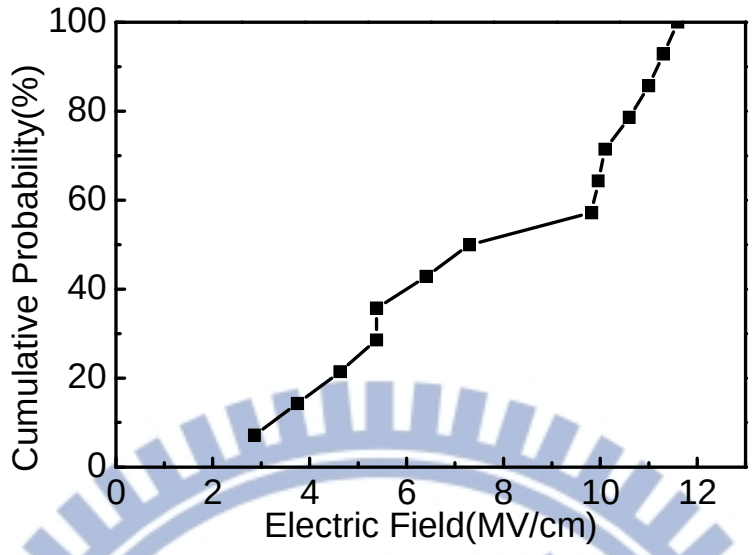


Fig.3-26 Breakdown field distribution of sample ONO.

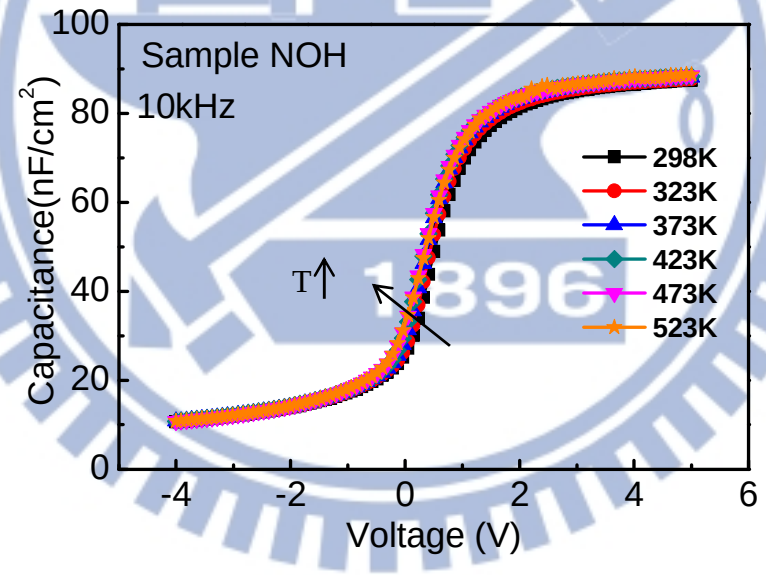


Fig.3-27 The high frequency C-V characteristics of sample NOH (W1 + N_2O + NH_3 + Si_3N_4) at various temperatures. CV negative shift because the work function difference of Al and 4H-SiC is decreased with temperature up.

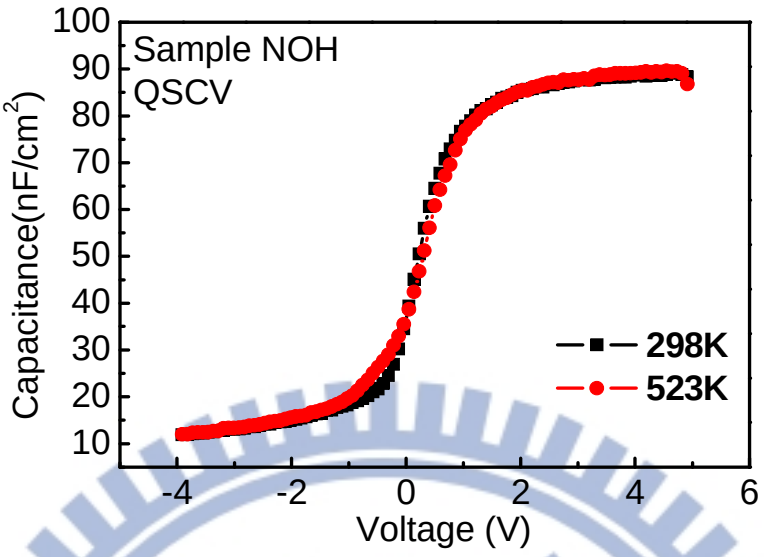


Fig.3-28 Quasi-static frequency CV characteristic of sample NOH (W1 + N_2O + NH_3 + Si_3N_4) measured at 298 K and 523 K.

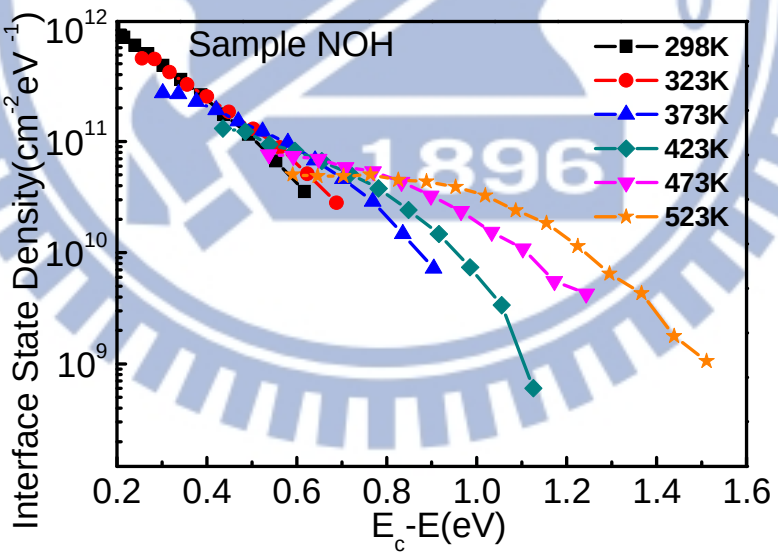


Fig.3-29 Interface state density of sample NOH (W1 + N_2O + NH_3 + Si_3N_4) measured at various temperatures.

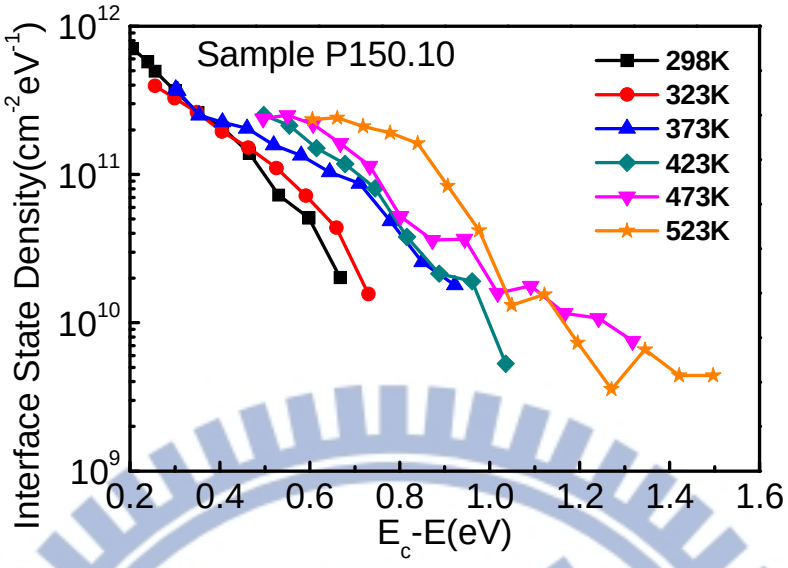


Fig.3-30 Interface state density of sample P150.10 measured at various temperatures.

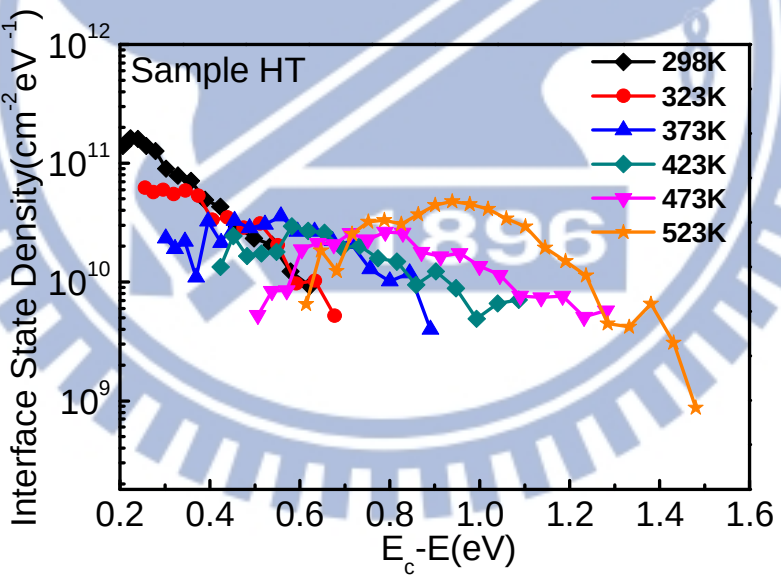


Fig.3-31 Interface state density of sample HT measured at various temperatures.

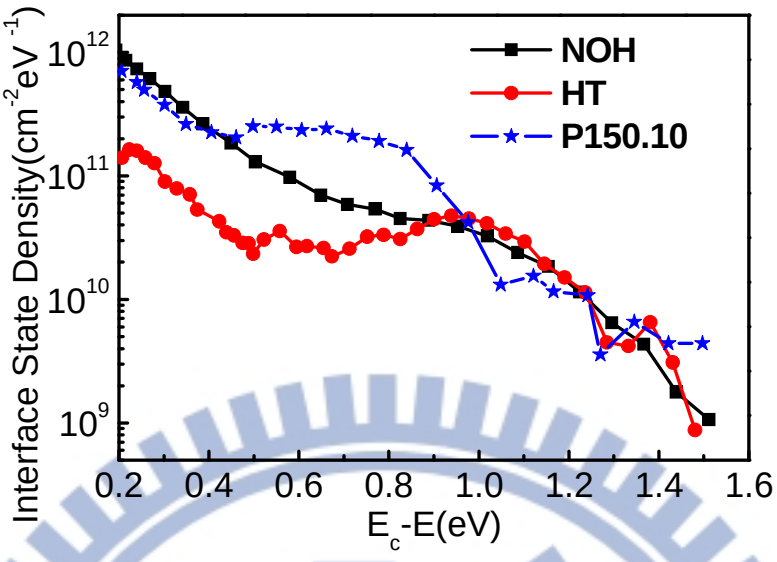
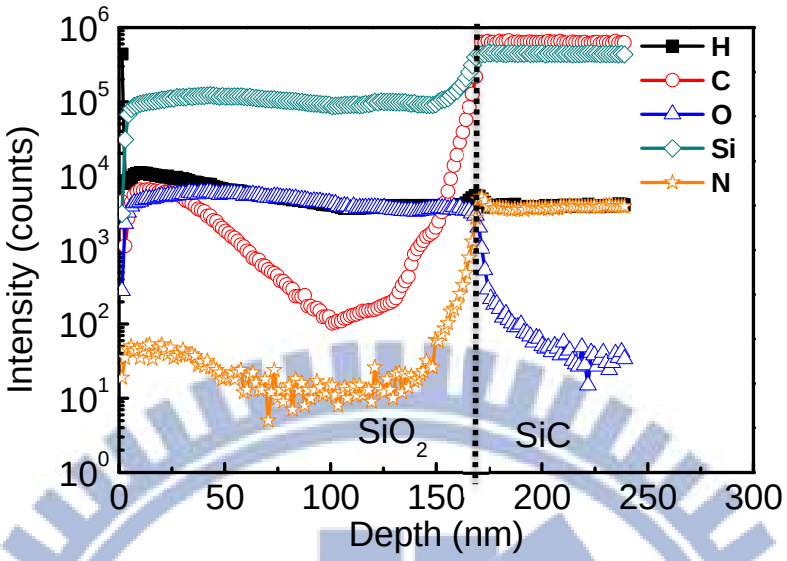
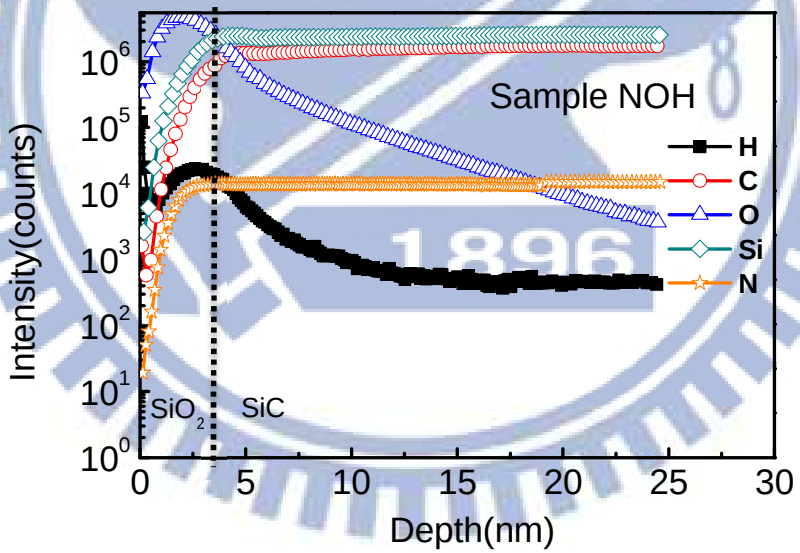


Fig.3-32 The full range interface state density of sample NOH, P150.10 and HT are compared

(a)


Intensity (counts)
Depth (nm)
H
C
O
Si
N
SiO2
SiC

(b)


Intensity(counts)
Depth(nm)
Sample NOH
H
C
O
Si
N
SiO2
SiC

(c)

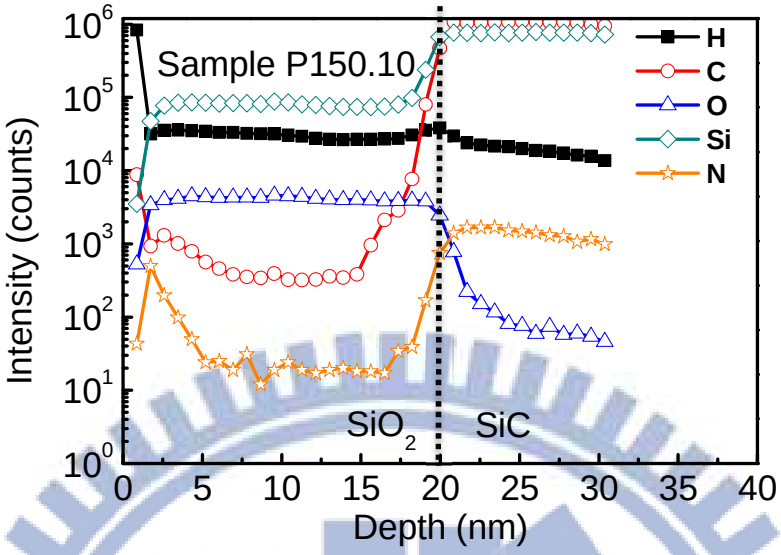


Fig.3-33 (a) The SIMS profile of the HT sample was obtained from instrumentation center at NTHU. (b) The SIMS profile of the NOH sample was obtained from MA-TEK. Nitride was removed before SIMS analyze. (c) The SIMS profile of the P150.10 sample was obtained from instrumentation center at NTHU.

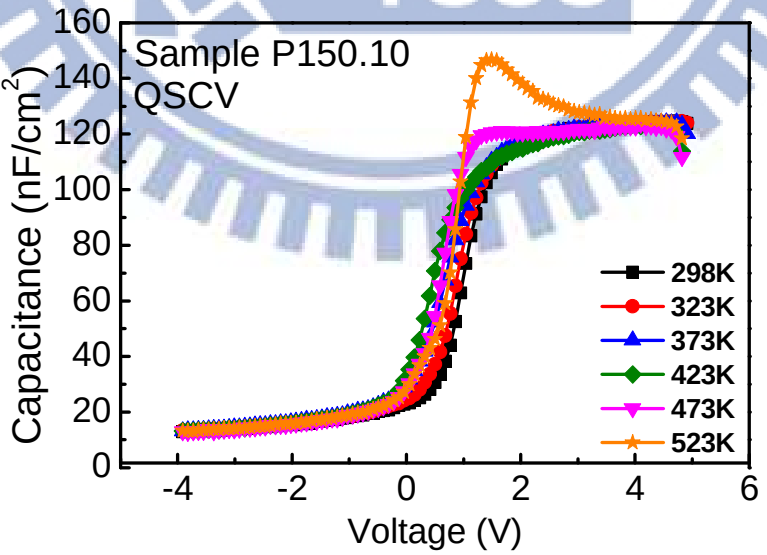


Fig.3-34 Quasi-static frequency CV characteristic of sample P150.10 measured at different temperatures.

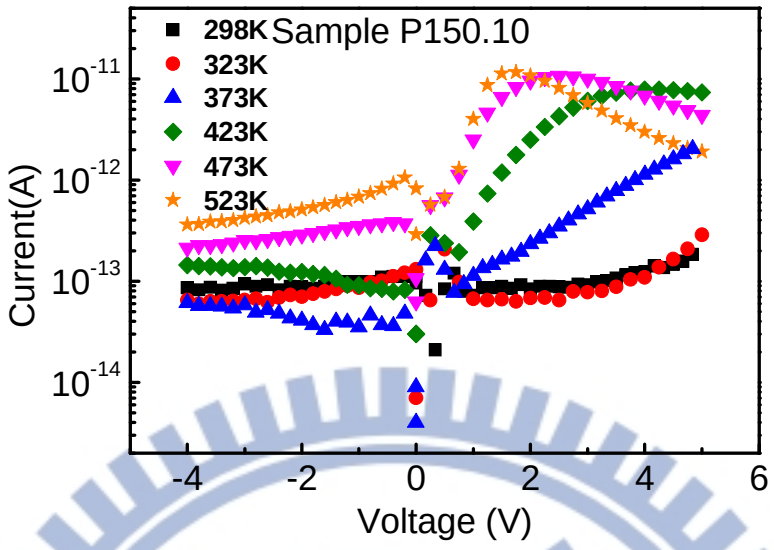
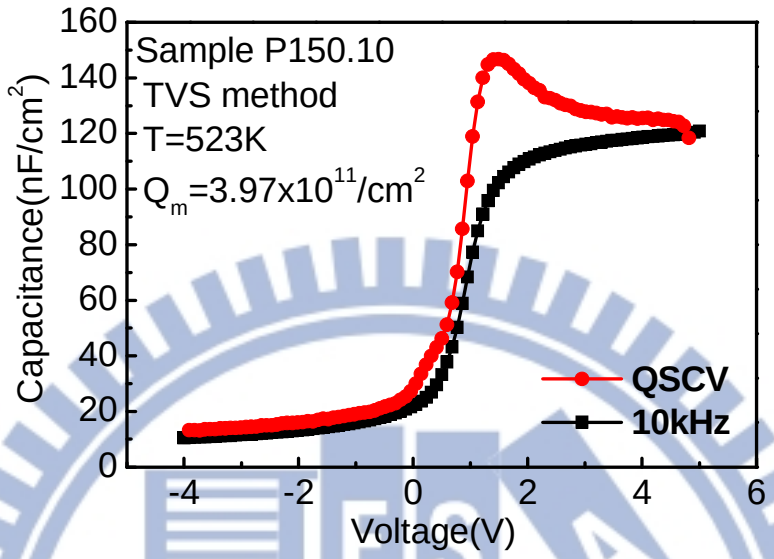


Fig. 3-35 Leakage current characteristic of sample P150.10.

(a)



(b)

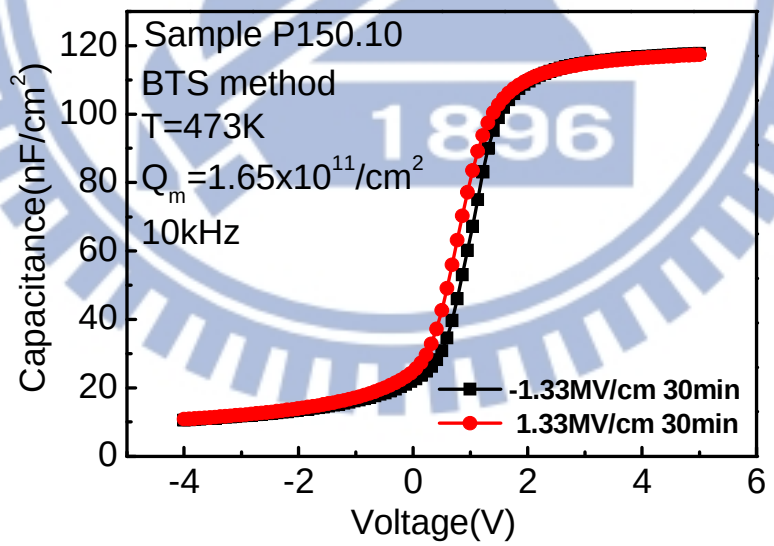


Fig.3-36 (a) High low CV of sample P150.10 at 523 K and mobile ion is calculated by TVS method (b) Sample P150.10 is bias and temperature stress. Temperature is 473 K and bias is ±1.33 MV/cm. The stress time is 30 minutes.

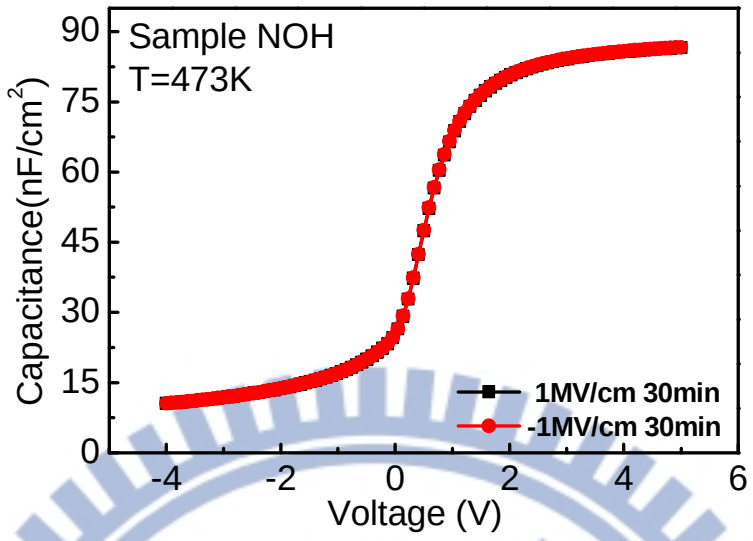


Fig.3-37 Sample NOH is bias and temperature stress. Temperature is 473 K and bias is ±1 MV/cm. The stress time is 30 minutes.

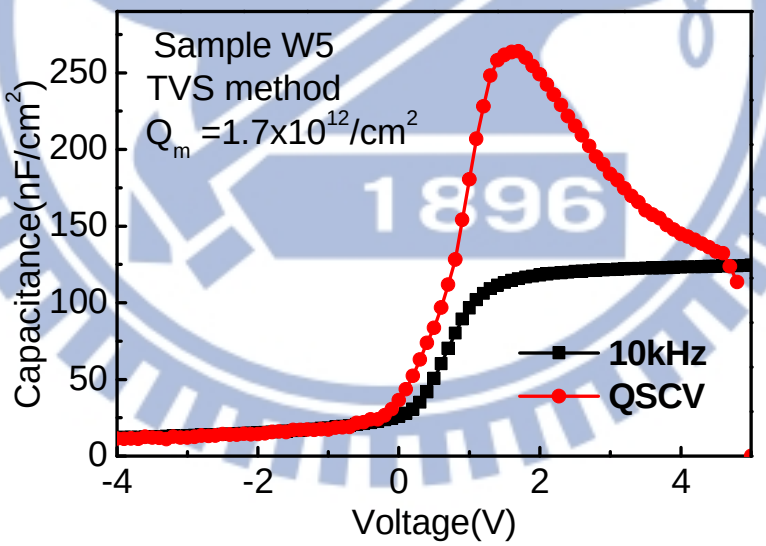


Fig.3-38 High low CV of sample W5 at 523k and mobile ion is calculated by TVS method

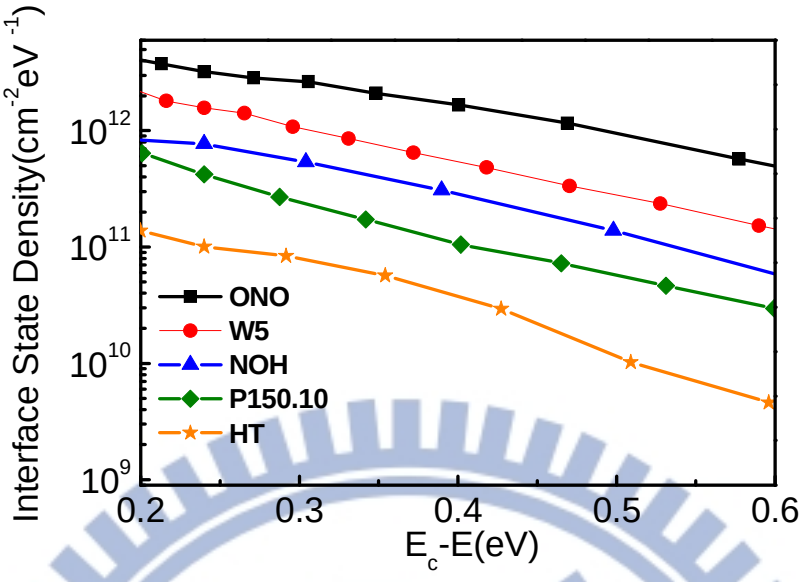


Fig.3-39 Interface state densities of representative samples in this thesis are summarized.

Chapter 4

Conclusions and Future works

4-1 Conclusions

In this thesis, the effect of low thermal budget processes on the improvement of the interface state density for the SiO_2/SiC interface is studied. In the beginning the wet oxide characteristics were evaluated. The very low oxidation rate of SiC is modeled by Deal-Grove model. It is observed that wet oxidation samples have higher D_{it} at the SiO_2/SiC interface and the C-V shift at different measurement frequency is due to difference response time of interface states. Different wet oxidation times result in almost the same $D_{it.}$ The value is around $5x10^{11}$ $cm^{-2}eV^{-1}$ at E_c-E = 0.4 eV. This result indicates that C clusters saturate after wet oxidation for 30 min because the temperature is not high enough for CO out-diffusion. The wide distribution of breakdown field occurs at thinner oxide sample (< 20nm) because of surface roughness

Sample HT has the lowest D_{it} in this study. The value is $4.67x10^{10}$ $cm^{-2}eV^{-1}$ at E_c-E = 0.4 eV. The relatively low breakdown field is due to large amount of defects in the thicker oxide. These defects may percolate to a current path easily.

Both N_2O and NH_3 post-oxidation annealing can slightly improve D_{it} because nitrogen may pile up at interface. It is also observed that the N_2O post-oxidation annealing and NH_3 post-oxidation annealing have superimposed effect. The D_{it} of sample NOH can be lowered to $2.92\ x10^{11}$ $cm^{-2}eV^{-1}$ at E_c-E = 0.4 eV. Sample N has lager breakdown field than sample W1. This result suggests that N_2O annealing can improve breakdown field but the variation is still large. Samples NH and NOH, with

nitride capping, have high and uniform breakdown field because the defects in oxide and nitride would not coincide to form leakage path.

The NH_3 plasma treatment method has the lowest thermal budget in this study. Significant large Flat-band voltage shift is due to negative charge generation during plasma treatment. The degree of D_{it} improvement does not depend on plasma power but depend on plasma treatment time. The reason is the diffusion of radicals through oxide into interface is related to treatment time. The improvement saturates at 10 min. The D_{it} of sample P150.10 is as low as $1.37x10^{11}$ $cm^{-2}eV^{-1}$ at E_c-E = 0.4 eV. The plasma treatment is a better process than the post-oxide nitridation because of lower thermal budget and lower D_{it}. Breakdown field of plasma treatment sample is same as sample W5. The ONO stack formed by CVD process can avoid C transition layer at interface but the D_{it} value is even larger than that of the wet oxidation samples and is not practical.

High temperature measurement was performed to extract the deep level D_{it}. It is found that all of the D_{it} improvement methods have the almost identical deep level traps. It is thus concluded that all of the D_{it} improvement methods evaluated in this thesis can passivate shallow level interface states and is not effective for deep level interface states.

Secondary ion mass spectroscopic analysis shows nitrogen pile-up at the SiO_2/SiC interface on the sample HT. This phenomenon is not observed on the other samples. It is suspected that the diffusion of nitrogen radicals in SiO_2 is slow. If nitrogen incorporation is processed after SiO_2 growth, there are not sufficient nitrogen radicals can reach the interface at low thermal budget processes.

The lowest interface state density achieved in this thesis is sample P150.10. However, the interface state density of this sample is still higher than the interface state density of the sample with high temperature N_2O oxidation (sample HT) by 3

times. Furthermore, the thermal budget of the plasma treatment is too low. Only hydrogen can passivate the interface states. It is suspected that hydrogen can only passivate shallow level interface states and does not affect the interface states deeper than 0.5 eV. Although the current result is acceptable for MISFET application, to achieve very low interface state, novel low thermal budget process must be developed otherwise high thermal budget process is still unavoidable.

4-2 Future works

In this study, some important results have been summarized in previous section. However, many works are worthy for further investigation. They are listed here.

1. The source of the negative charges after plasma treatment is not clear at this moment. Further material analysis will be performed in the future. Those negative charges may degrade the channel mobility due to Coulomb scattering. How to reduce negative charges is an important issue.
2. The sample HT has low breakdown field due to thick oxide. We try to repeat the process of 1300 ℃ N_2O-grown oxide and reduce oxide thickness to improve breakdown characteristic in the future.
3. Except the samples W0.5 and W1, the current transport mechanisms for other samples are still unclear. The further investigation at various temperatures would help on clarifing the transport mechanism.
4. The thinner (10 nm) PECVD oxide deposition on SiC has large leakage current and poor interface quality. The reason is not clear in this stage. We doubt the stoichiometric ratio of PECVD oxide is not theoretical at initial deposition stage. The stoichiometric ratio of PECVD oxide will be detected by SIMS and XPS analysis.

5. In order to operate at high voltage and high temperature for a long time, the reliability of the gate dielectric must be investigated. Poor SiC MOS lifetimes below 1000 s at 6 MV/cm and 350 ◦C has been reported in literature [43]. Bias-stress-induced threshold-voltage instability due to electron tunneling from the oxide traps is observed [44]. Therefore, reliability of the MIS structure fabricated by the low thermal budget processes proposed in this thesis should be evaluated carefully. Time dependent dielectric breakdown (TDDB) and bias temperature instability (BTI) will be measured in the future.
6. The hydrogen and nitrogen can passivate C-cluster–like defects during NH_3 plasma treatment but the thermal stability is an issue for high temperature MISFET processes application. Hydrogen may escape from interface during high temperature processes. If NH_3 plasma treatment will want to be embedded in MISFET processes, the thermal stability of NH_3 plasma treatment–MIS-capacitor will be further investigated.
7. The deep level (E_c-E > 1 eV) D_{it} is not passivated for all samples as mentioned in previous cheaper. How to reduce deep level D_{it} is worthy to investigate.
8. In addition to nitrogen passivation, it has been reported that fluorine passivation can reduce interface state density at the SiO_2/Si interface [45]. It is worthy to evaluate the effect of fluorine passivation on SiC substrate. Several processes can be considered. They are CF_4 plasma treatment, NF_3 annealing, fluorine ion implantation, and so on.
9. If we want obtain lowest D_{it}, the high temperature N_2O is needed in recently stage. We will try to fabricate planar SiC MISFET in next year. NH_3–plasma-treatment and 1300℃ N_2O will be embedded in SiC MISFET. The source and drain dopant activation issues need further investigation.

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碩士論文題目：

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Improvement of 4H-SiC MIS Capacitor Interface State Density by Low Thermal Budget Processes