國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

使用新的量測方法探討三面閘極金氧半電晶體氧化層隨機陷阱造成之擾動效應

The Random Trap Induced Fluctuations of Bulk Tri-gate Devices by a New Trap Profiling Technique

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中華民國 一○一 年 八 月

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碩士論文

A Thesis

Submitted to Department of Electronics Engineering and Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

In Partial Fulfillment of the Requirements

for the Degree of

Master of Science

in

Electronics Engineering

August 2012

Hsinchu, Taiwan, Republic of China

中華民國 一Ｏ一 年 八 月

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摘要

CMOS 元件快速微縮的情況下，元件進入奈米世代以後，有相當多的挑戰必須克服，諸如短通道、效能的提升、閘極氧化層漏電流。截至目前，大部份挑戰皆是可以被克服的，諸如：使用極淺接面(ultra-thin junction)來克服短通道效應、strained Silicon 來提昇元件性能。除此之外，通道中的載子濃度以及陷阱所在位置其結果會反映在元件特性的擾動上，例如驅動電流以及元件的臨界電壓上會產生擾動，導致元件特性不一致(mismatch)。

在此篇論文中，我們引用了一個新的機制，稱作隨機陷阱造成的擾動效應 Random Trap Fluctuation (RTF)，由於元件在長時間的操作下會產生相當多的隨機陷阱在通道表面，例如：閘級和汲極偏壓在汲極端所產生的熱載子(Hot Carrier stress)或利用加溫度產生熱載子(NBTI)對氧化層產生的缺陷，因此，該效應對於元件可靠度而言相當的重要，因為當元件被 stress 之後的陷阱是造成元件擾動的主要來源，但是以現在的量測技術而言，無法清楚的了解氧化層或是通道表面上的陷阱對是如何對電晶體的臨界電壓產生影響。在這篇論文中，我們提出一個新的量測方法稱為 **Random Trap Profiling (RTP)** ，此方法可以找出通道中陷阱的分佈位置，利用本篇論文所提出的

方法成功的解決電荷幫浦法在面積太小的元件中無法量測的問題，因為元件尺寸在未來的元件趨勢中一定是越來越小，因此利用此方法即使元件面積很小也可以找出氧化層內缺陷的位置。

本文中，我們成功的使用新的方法來探討一批28奈米製程的三閘極電晶體，並成功的找出通道中陷阱的分佈位置，並且獲得幾項結論: (1) 我們成功的將通道中因為受到摻雜載子影響以及元件經過長時間操作後產生的陷阱對造成的影響分開。(2) 兩種不同的操作機制 (HC以及NBTI)分別操作在兩種不同類型的電晶體中，對於N通道來說，因為受到HC stress的影響，因此會在汲極端產生大量的陷阱，反觀P通道元件，因為受到NBTI的影響，其產生的陷阱分佈是在通道中間。(3) 最重要的一點，我們利用此方法發現到無論是 HC stress 或者是 NBTI stress都會因為通道表面的不均勻(surface roughness effect)，或是因為上表面與側壁之間的角落效應(corner effect)而產生許多的陷阱，這是影響三維元件可靠性的重要原因。

本文利用改良式萃取缺陷水平位置的方法，可以深入了解小尺寸元件缺陷位置，對於未來在研究新的CMOS元件可靠性以及性能上的優越表現可提供重要的設計參考指標。

The Random Trap Induced Fluctuations of Bulk Tri-gate Devices by a New Trap Profiling Technique

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ABSTRACT

As device channel length continues to scale beyond 100nm, we need to overcome many problems such as short channel effect, performance enhancement, and leakage current. So far, the major challenges have been overcome by difference technologies. For example, the short channel effect is solved by ultrathin junction depth and strained silicon device is used to enhance the electrical performance. While the variation properties induced by the discrete dopants and traps induce the fluctuation of electronics properties significantly in the channel which lead to the mismatches of threshold voltage (V_{th}) and driving current.

In this thesis, we proposed a new mechanism, called Random Trap Fluctuation (RTF), which was considered to be another important issue for the device after the long term stress. It varies with the device after the stress, e.g., Hot Carrier Stress (HC) or Negative Bias Temperature Instability (NBTI). Also, it was observed that RTF is the major fluctuation source after the stress. But, the understanding of the actual mechanisms and phenomena of oxide (or interface) traps induced V_{th} fluctuation has been very difficult and rare has been reported so far. In this thesis, we developed a newly technique, called **Random Trap Profiling (RTP)**, to profile the stress-induced traps. Compared to the conventional lateral

profiling technique, Charge-pumping Profiling, RTP shows its advantages for applications to single and very small devices and very suitable for ultra-scaled 3D devices, such as FinFET or Trigate.

In this thesis, we used this new random trap profiling technique to identify the oxide trap position after the stress for a 28nm single-fin bulk trigate device and examine the physical mechanisms. As a consequence, several salient results can be drawn: (1) we successfully separated the fluctuation source from the discrete dopant and the source from the random traps after the stress. (2) Two stress schemes, HC and NBTI, have been utilized to examine the trigate nMOS devices and trigate pMOS devices respectively. For trigate nMOS devices, the oxide traps are generated near the drain side after hot carrier (HC) stress; but for triage pMOS devices, they are generated more in the middle of the channel after the NBTI stress. More importantly, (3) it has been found the reliability killer of advanced trigate devices should be the surface roughness on the side-wall and corner effect induced random traps either under the HC or NBTI stress, and the latter dominates the degradation of bulk trigate devices. These results will be helpful and valuable for the design of the next generation bulk trigate CMOS devices beyond 20nm generation.

誌　謝

兩年的時間很快就過去，非常感謝在這些日子以來不斷幫助我的貴人，首先感謝莊紹勳老師在兩年前收我為研究生，帶領我走過研究所這個階段，老師給予的課業上的指導與建議，讓我在學業與研究上獲益良多並學習到對事物應有的嚴謹態度，在未來的日子中想必也是受用無窮。除此之外，老師總是授權讓學生在研究上可以盡情發揮，並給予適當的建議，有了這些建議才讓我可以順利做出其實驗結果，我必須在此表達感謝之意。

謝謝實驗室的其他同仁，包含了謝易睿學長，感謝你的指導，在我剛進研究所時，總是不斷的給予我教導與協助，使我能在研究上可以很快上手，每當我遇到瓶頸時，總是給我相當好的建議，這兩年也謝謝你帶我做了這麼多的實驗，還有同屆的侑璉、英傑、政達，謝謝你們在這兩年的陪伴，讓我在實驗室中除了實驗之外還可以充滿歡笑聲，謝謝學弟們，包含了宗慶、敬翰、尚墩、邦齊、漢樽，謝謝你們幫助學長處理一些瑣碎的雜事，讓學長在實驗上可以無後顧之憂，另外也謝謝汪大暉老師的學長與同學們，包含了邱榮標學長，鍾岳庭學長，以及同屆的泓達和定樺，謝謝你們兩年來的相伴，總歸一句，感念所有的夥伴，因為你們的陪伴，使我兩年研究生活豐富，即使艱辛，仍充滿歡笑。

最後要感謝是我的家人，總是在我失落的時候給我最大的鼓勵是我精神上最大的支柱，由於你們默默的支持和關愛，我才能堅持完成學業。

謹將這份榮耀獻給培養我多年的父母親

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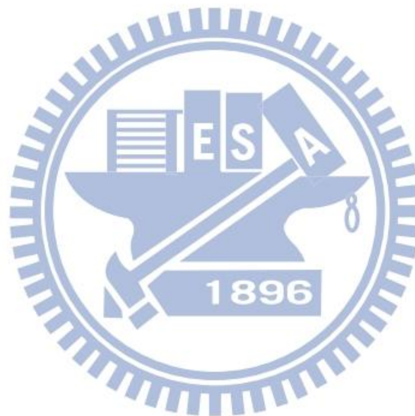

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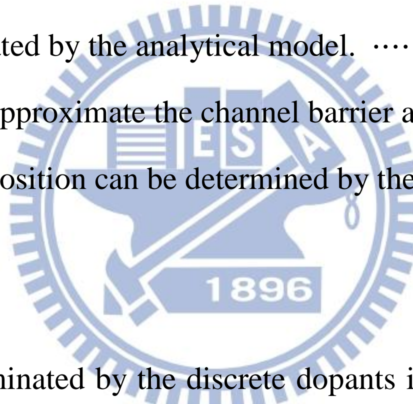

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Chapter 1
Introduction

1.1 Background

As the scaling of bulk CMOS devices reaches the physical limit, multi-gate device, or FinFET-like transistor structures, emerges as a promising candidate to extend its further scaling owing to its superior integration, higher subthreshold slope, reduced leakage, and immunity to the RDF (Random-Dopant Fluctuation) [1.1] by using the lightly-doped or undoped silicon fin. For ultra-low-power applications such as portable devices, implanted medical instruments, and wireless body sensing networks, operating at below threshold voltage is an effective solution [1.2] to reduce both static and dynamic power consumptions. Moreover, FinFET devices present the following advantages: (1) shallow trench isolation is not needed and (2) the device DIBL or short channel effect can be effectively improved as a result of the increasing gate controllability upon the channel region in the ultra-thin silicon body of Si-fin.

In reported studies, several reliability issues for FinFET have been identified, e.g., threshold voltage instability [1.3], stress induced film degradation [1.4], and corner effects [1.5]. Among them, threshold voltage instability is due to the dynamics of carriers charging/discharging in oxide traps such as negative bias temperature instability (NBTI) in pMOS devices or hot carrier effect (HCE) in nMOS devices.

1.2 The Motivation of This Work

Since CMOS technology has reached 20 nm node at this time, further scaling to below 20 nm and even beyond has been widely acknowledged as encountering many new challenges and in particular with regard to V_{th} variation issues. Recent study [1.6] revealed that random

dopant fluctuation (RDF) is the major source of V_{th} variation in scaled bulk CMOS. To improve the RDF, FDSOI or FinFET with undoped (lighter) channel [1.7-1.9], has been proposed subsequently to reduce the variability effectively.

Also, recent developments [1.10] in CMOS technology have highlighted the need in using the 3D technique as a method to extend the scaling of CMOS device for high speed and low power logic applications. Several approaches among them, such as tri-gate devices, double-gate devices, and FinFETs, along with lightly-doped or undoped silicon fin technology, have been utilized to improve the device performance. However, so far, the sources and the mechanisms of V_{th} variation have not been experimentally clarified on trigate devices. As a consequence, we are interested in understanding the variability of trigate devices.

For the first time, in this thesis, we apply a new measurement method to observe the Vth variation in various n-MOS devices and p-MOS devices employing different channel area bulk trigate devices. The impact of the 3D device on the device reliability and variability will be investigated and compared.

1.3 Organization of the Thesis

There are five parts in this thesis. Chapter 1 is the introduction. In Chapter 2, we describe the experimental setup and the method of Methodology of Random Trap Profiling Technique (RTP). In Chapter 3, the variability study based on the V_{th} variation and the stress-induced interface traps on n-MOS devices will be examined. On the other hand, using similar analysis, we will discuss the variability of trigate p-MOS devices. In Chapter 4, we will discuss the corner effect and sidewall surface roughness effect. Finally, the summary and conclusion will be given in Chapter 5.

Chapter 2

Experimental Setup and V_{th} Variation

2.1 Introduction

As devices are scaled to the nanoscale dimension, it is important to understand random fluctuations. Since there are many possible microscopic causes, it is desirable to understand the mechanism of variability. Therefore, electrical measurement of random fluctuations is a useful technique to observe such microscopic effects. It is necessary to collect a lot of data of standard deviation values for various kinds of transistors fabricated by different process conditions. If such data is properly compared and analyzed, it may become possible to extract quantitative information about random fluctuations. Based on this consideration, a simple normalization method for comparing standard deviation values of random threshold voltage fluctuations was proposed. The method was used to compare devices with various origins and to analyze the causes of random fluctuations [2.1].

This chapter is divided into two sections. First, we will illustrate the fundamental experimental setup to characterize CMOS devices. Second, the method of Random Trap Profiling Technique (RTP) used in this thesis will be introduced, and its fundamental theory will be described in detail.

2.2 Experimental Setup

The experimental setup for the current-voltage measurement of devices is illustrated in Fig. 2.1. Based on the PC controlled instrument environment by HP-IB (GP-IB, IEEE-488 Standard) interface, the complicated and long-term characterization procedures during analyzing the behaviors in MOS devices can be easily achieved. As shown in Fig. 2.1, the equipment, including the semiconductor parameter analyzer (HP 4156C), low leakage switch mainframe (HP E5250A), dual channel pulse generator (HP 8110A), cascade guarded thermal probe station and a thermal controller, provides an adequate capability for measuring the device characteristics. In addition, programs written by HT-Basic were used to execute the measurement via HP-IB interface.

2.3 Methodology of Random Trap Profiling Technique (RTP)

First of all, the amount of increased traps (ΔN_{it}) can be extracted by standard deviation of V_{th}, we know that the interface trap is the principal cause of the V_{th} shift if traps are distributed discretely in the oxide,

$$V_{th,stress} = V_{th,fresh} + V_{th,shift} = V_{th,fresh} + \frac{q}{C_{ox}} D_{trap} \quad (1)$$

where $V_{th,stress}$ is the threshold voltage after the stress by hot carrier or negative bias temperature instability test. $V_{th,fresh}$ and $V_{th,shift}$ are the virgin threshold voltage and the shift threshold voltage, respectively. D_{trap} is the interface trap density. Also,

$$\sigma V_{th,shift} = \sqrt{\sigma V^2{}_{th,stress} - \sigma V^2{}_{th,fresh}} \quad (2)$$

the standard deviation of V_{th} shift is obtained by the standard deviation of $V_{th,stress}$ ($\sigma V_{th,stress}$) ,

and the result can be presented as the summation of the delta function of the trap density from the surface to the depletion region by a delta function, i.e.,

$$\sigma V_{th,shift} = \sigma(\frac{q}{C_{ox}} D_{trap}) = \frac{q}{C_{ox}} \sqrt{\frac{\int_0^{W_{dep}} N_{trap}(x)dx}{LW}} \quad (3)$$

$$= \frac{q}{C_{ox}} \sqrt{\frac{\int_0^{W_{dep}} \Delta N_{trap}(x)\delta(x - x_{trap})dx}{LW}} \quad (4)$$

$$= \frac{q}{C_{ox}} \sqrt{\frac{\Sigma \Delta N_{trap}(x_{trap})}{L_{eff} W}} \quad (5)$$

$$= \frac{q}{C_{ox}} \sqrt{\frac{\Delta N_{trap}}{L_{eff}}} \quad . \quad (6)$$

From the above equations, we can obtain the interface trap density,

$$\Delta N_{trap} = L_{eff} (\frac{C_{OX}}{q} \sigma V_{th,shift})^2 (\#/cm^2). \quad (7)$$

Since RTF above the channel barrier peak dominates V_{th} variation after stress, the delta trap density can be profiled along the channel as the peak shifted by varying the source-to-drain bias, V_{sd}. The principle of the measurement method is to locate the channel barrier peak position by varying the drain bias based on a quasi-2D V_{th} model (Fig. 2.2). Because DIBL is proportional to the peak position which can be calculated by an analytic form [2.2] (Fig. 2.3), the peak position can be determine ed by the measured DIBL while the channel barrier was approximated as the second degree curve (Fig. 2.4), i.e.,

$$\frac{Y_0 - Y_{Peak}}{(L_{eff} - \Delta L)/2} = \frac{DIBL}{(V_{bi} - V_{s,max})} . \quad (8)$$

Here, L is the effective channel length, $V_{s,max}$ is the barrier height of long channel, and V_{bi} is

the junction barrier of the source and channel. The subthreshold swing can be expressed as

$$S.S. = (1+\frac{C_{dm}}{C_{OX}})\times 60mV \text{ [2.3]} \tag{9}$$

where C_{ox} is the oxide capacitance, and C_{dm} is the depletion-layer capacitance given by

$$C_{dm} = \frac{Q_{dep}}{V} \tag{10}$$

the depletion capacitance is proportional to the channel length, because $Q_{dep}=qnLW$. *Then, we can derive the following:*

$$\frac{L_{eff}-\Delta L}{L_{eff}} = \frac{C_{dm}}{C_{dm,0}} = \frac{S.S.-60mV}{S.S._{0}-60mV}, \tag{11}$$

from which the horizontal position along the channel is given by:

$$Y_{peak} = [\frac{1}{2} - \frac{1}{2}\frac{DIBL}{(V_{bi} - V_{s,max})}\times\frac{S.S. - 60mV}{S.S._{0} - 60mV}]\times L_{eff}. \tag{12}$$

In the measurement method, the parameters were extracted experimentally. L_{eff} can be extracted by the charge pumping technique that our group developed in [2.4]. By applying continuous incremental pulses at the gate, the charge pumping current (I_{cp}) is induced, then the I_{cp} will be proportional to the shape of the local V_{th}. Thus, the channel barrier height, $V_{s,max}$, can be found. V_{bi} can be determined from V_{th} by varying V_{bs}, and the extrapolated value as the gate length vanishes will determine the value of V_{bi}.

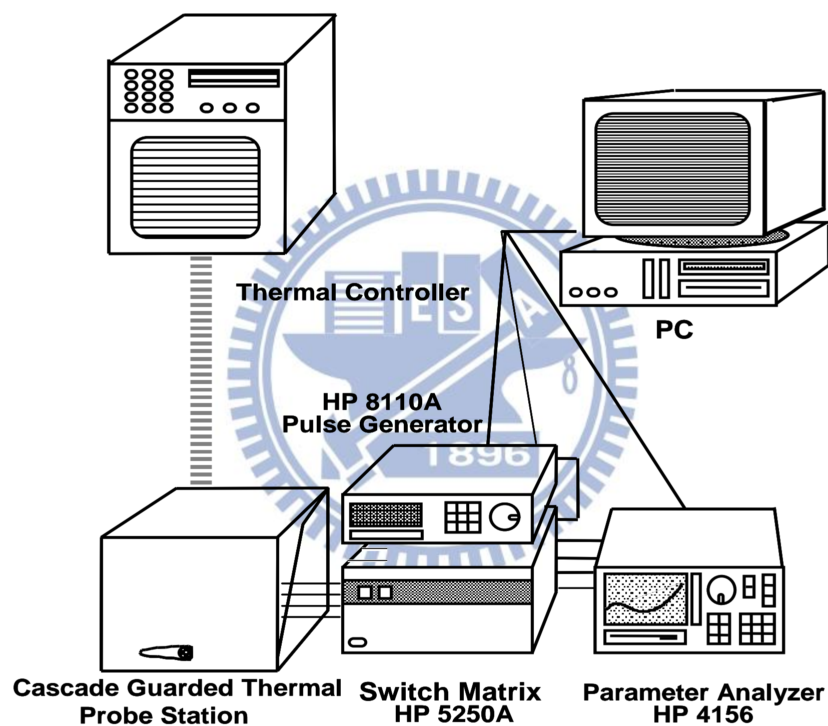


Fig. 2.1 The experimental setup for the current-voltage measurement of MOS devices. Automatic controlled characterizations system is setup based on the PC controlled instrument environment. The energy band diagram of the Si-SiO_2 interface in the channel at the trap location.

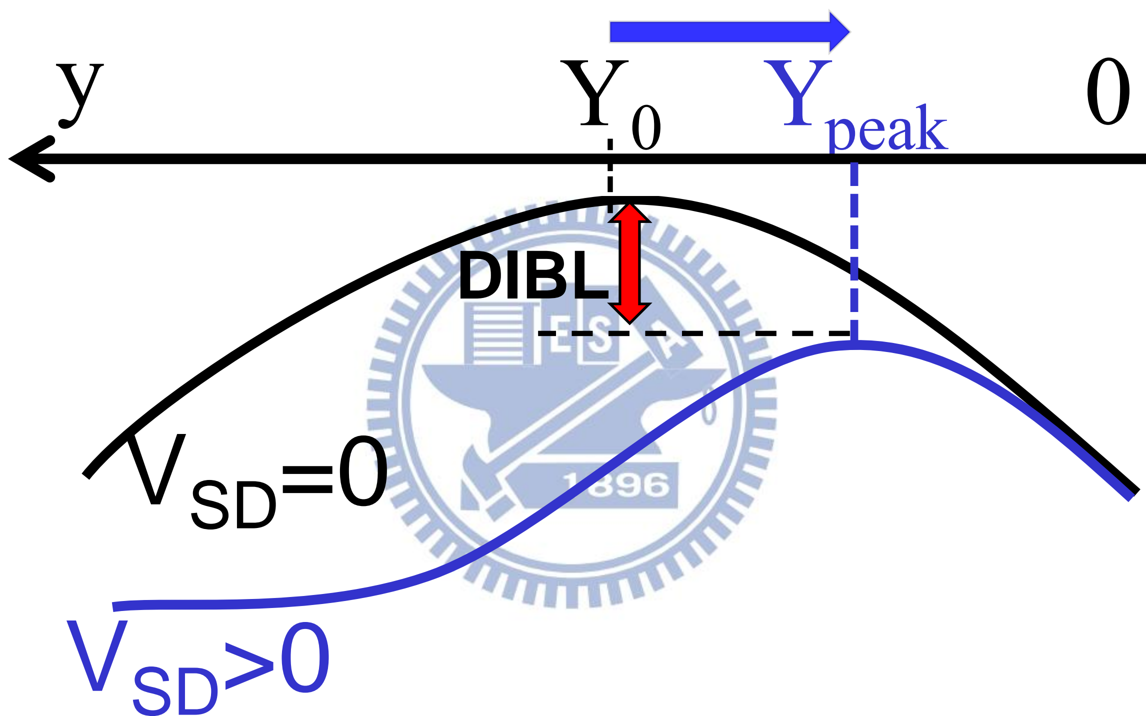


Fig. 2.2 By varying the V_{SD}, the barrier peak can be found from the DIBL since as V_{SD} increases, the barrier peak will be shifted toward the drain such that the delta trap density can be profiled along the channel.

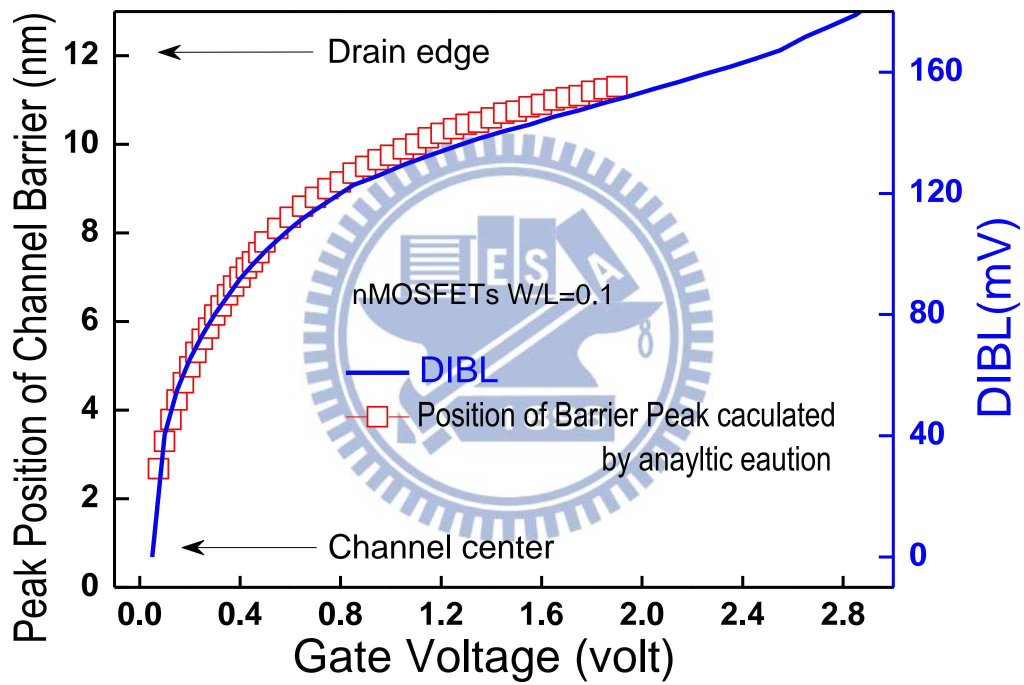


Fig. 2.3 It was found that the DIBL shift is well matched with the position of channel barrier peak calculated by the analytical model.

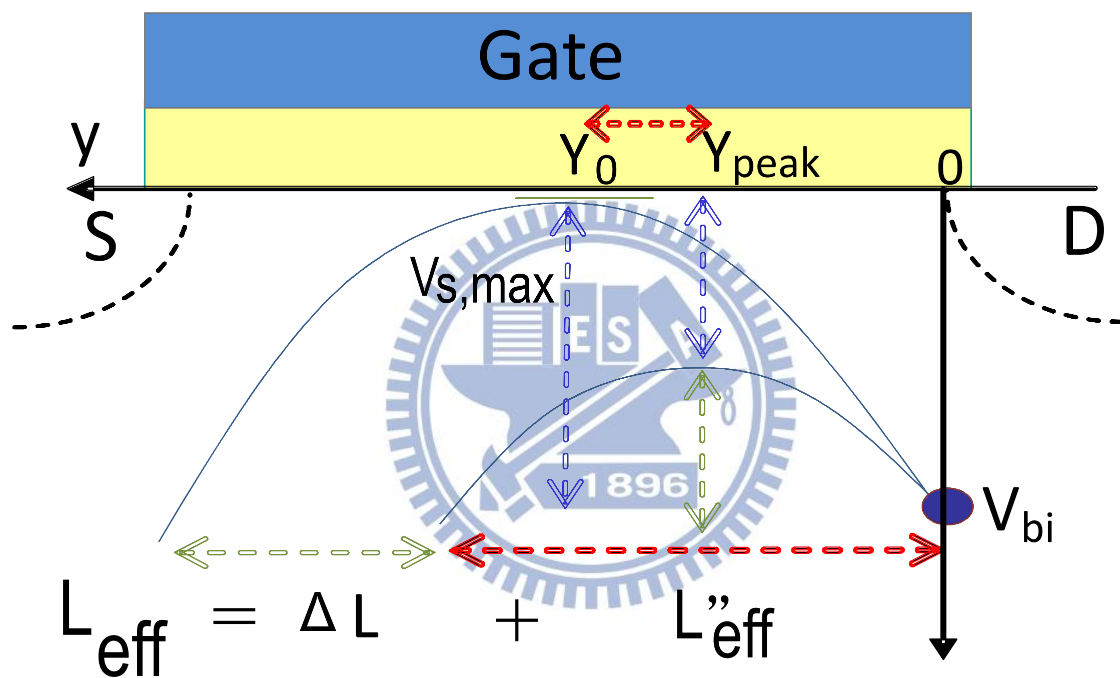


Fig. 2.4 A new model is to approximate the channel barrier as a second degree curve, in which the peak position can be determined by the DIBL.

Chapter 3

Spatial Distribution of Traps in Bulk Trigate Devices After Long Term Stress

3.1 Introduction

Bulk trigate devices might be the mainstream CMOS architecture beyond 20nm owing to good short channel effect and low V_{th} variation [3.1]. But, the reliabilities are rarely discussed, and the discussion on the mechanism of degradation of such devices after the stress was very few. Doping and trap induce significant characteristic fluctuations [3.2] randomly in nanometer scale metal-oxide-semiconductor field effect transistors (MOS devices). The oxide trap spatial spectrum is the key to understand the mechanisms of degradation. Due to the ultra-scaled active region and multi-fin layout for trigate devices, we face the challenges to identify the oxide trap positions after the stress by the matured techniques, such as charge pumping technique [3.3], which is limited by small area devices. Since the order of the measured Icp is close to the background leakage, a new method should be urgently required. From reported results, it was found that V_{th} variation is dominated by discrete dopants at the channel barrier peak, known as random dopant fluctuation (RDF). Furthermore, if oxide traps are present above the channel barrier peak, another effect, called random trap fluctuation (RTF) [3.4], will be involved in the V_{th} variation Fig. 3.1. Therefore, the main idea of random trap profiling technique is to measure V_{th} variation after the stress to identify the amount and position of traps in bulk tri-gate devices which will then be extended to understand the physical mechanism associated with the fin-height.

3.2 Device Preparation

Advanced poly-Si gate bulk planar and trigate CMOS devices, with SiON insulator, were

fabricated [3.5]. The bulk CMOS process, using the front-end-of-line steps outlined in Fig. 3.2. After the conventional STI process, good formation, and V_T-adjust ion implantation, the STI oxide was slightly recessed by various amounts on selected wafers prior to gate-stack formation. The schematic cross section diagram of a trigate MOS device is shown in Fig. 3.3. The width of trigate is 30nm and the height is different by recessed depth. L_{eff}= 25nm. Both control and splits are made on the same wafer. To exclude and avoid the parasitic effects, single-fin devices were prepared, Fig. 3.4. Devices with different areas were used to calculate the V_{th} variations.

3.3 Parameters of the Measurement Method

In the measurement method, the parameters were extracted experimentally (Fig. 3.5- 3.7), L_{eff} can be extracted by the charge pumping technique on the control devices simultaneously made on the same wafer. When the continuous increment pulses reached over the local threshold voltage (V_{th}) and local flat band voltage (V_{fb}), the charge pumping current (I_{cp}) begins conduction, then the I_{cp} will be proportional to the shape of local V_{th}. Thus, the channel barrier height can be found. V_{bi} can be determined from V_{th} by varying V_{bs}, and the extrapolated value at the gate length vanishes will be a function of V_{bi}.

3.4 Variability of Trigate MOS Devices

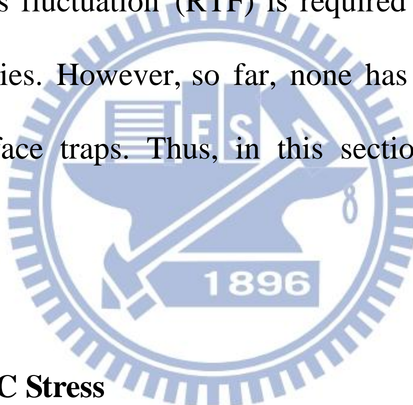
First of all, bulk trigate devices improve Vth variation because stronger gate electrostatic suppresses RDF, the factor A_{vt} [3.6] has a linear relation with channel area, which can help us to understand the fluctuation of electrical characterizing in different channel areas, as shown in Fig. 3.8. Here, the trigate devices shows obvious smaller slopes of A_{vt} than the control ones because the stronger gate electrostatic for such devices to suppress the discrete dopant

induced RDF. But, after the stress, V_{th} degradation of trigate devices was much worse than that of control due to RTF (Fig. 3.9).

3.5 Impact of Stress-induced Random traps

3.5.1 Introduction

A large number of variation effects have been reported, examples include: random dopant fluctuation (RDF) [3.7], line-edge roughness (LER) [3.8-3.9], and local oxide thickness variations [3.10]. In addition to these effects, recent study [3.11] has proved that process-induced random traps fluctuation (RTF) is required for proper interpretation of V_{th} variation in CMOS technologies. However, so far, none has been reported on the effect of stress-induced random interface traps. Thus, in this section, we will discuss the device variability after the HC stress.



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3.5.2 Variability After the HC Stress

Since the positions and number of charges trapped at the SiO_2/Si interface are randomly distributed, it is possible for this variation to affect the V_{th} variation [3.12]. Fig. 3.10 shows the measured V_{th} for studying the stress effect using the HC stress (V_{GS}= V_{DS}= V_{dd}+V_{fb}= 2V for 100 and 200sec) on planar n-MOS device. It is observed that standard deviation of the devie after the stress is larger than that of the fresh device, because the standard deviation of stressed device contains Random Dopant Fluctuation (RDF) and Random Trap Fluctuation (RTF) and the fresh device has RDF only.

The local σV_{th} profiling results by RTP of planar devices is shown in Fig. 3.10. It was

found that the peaks are near the drain edge of the devices after the HC stress, but for the local σV_{th} profiling results of trigate devices, it was found that the peaks are not only near the drain edge but also in the channel region after the HC stress. Fig. 3.11

This result indicates that stress-induced interface traps are the dominant source of the enhanced V_{th} variation after the HC stress, and the planar and trigate device contains different factors inducing σV_{th}.

3.5.3 Variability After the NBTI Stress

By applying a similar analysis, we apply the NBTI stress (V_{GS} -V_{th}= -2V at 125℃) to generated the interface traps of the pMOS device which would show more degraded V_{th} variation. To study the stress-induced degradation, Fig. 3.13 shows the measured the standard deviation after the NBTI stress (V_{GS} -V_{th}= -2V for 100 and 200sec, at 125℃). The standard deviation of trigate device is larger than that of the planar device. The result indicates that trigate generates more interface traps at the SiO_2/Si interface in comparison to the planar device. Fig. 3.14 shows the local σV_{th} profiling results by RTP for trigate devices. It was found that many peaks are observed after NBTI stress in the channel region, originating from the sidewall roughness. (Fig. 3.15) The trap densities of trigate devices are much larger than those of the control.

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The result is similar to that of n-MOS devices, in which we observed a higher standard deviation in trigate device after the NBTI stress that is attributed to the more interface traps generation.

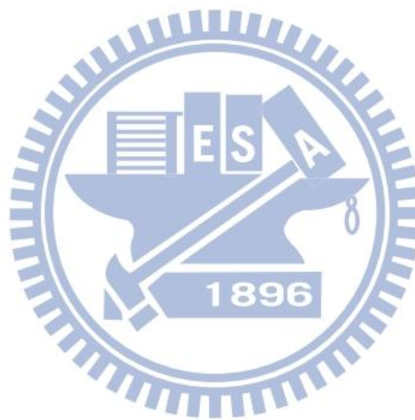
3.5.4 Discussion

To characterize the oxide trap spatial spectrum, random trap profiling was performed after the hot carrier (HC) stress on the planar and trigate nMOS devices respectively. (Fig. 3.10~12) It was found that the local Vth variation fluctuated heavily near the drain edge after the HC stress, showing where the traps were generated due to a high electric field. (Fig. 3.10) But, for trigate devices after the HC stress(Fig. 3.11), not only the local Vth variation was observed near drain edge but also on the sidewall, meaning that the sidewall is a critical region in terms of trigate reliability. We suspect that the sidewall corner effect induced a high electric field, consequently generating the traps. As a result, in trigate nMOS device, the trap density calculated from V_{th} was much higher than that of the planar after the HC stress. (Fig. 3.12)

NBTI stress was also applied to examine the degradations of the planar and bulk trigate pMOS devices. (Fig. 3.13~Fig. 3.15) In planar devices, local V_{th} variation occurred around the channel center. (Fig. 3.13) But, for trigate devices, unusual peaks of local V_{th} variation (blue lines) were observed in the channel region. (Fig. 3.14) We assume that these peaks came from the traps caused by the surface roughness and corner effect of the sidewall. Because, during NBTI stress, the profile of electric field intensity distributed across the sidewall, and the closer to corner the field is, the stronger the intensity becomes. This high intensity field led to the generation of traps. So the trap densities of trigate devices were much larger than those of the control. (Fig. 3.15)

We conclude that NBTI stress dominates the degradation of trigate devices due to the surface roughness and corner effects. (Table 1) However, by taking good care of the sidewall process, the reliability of trigate devices might be improved. These results provide us a

direction on a good control of the reliability in future 3D FinFET devices.



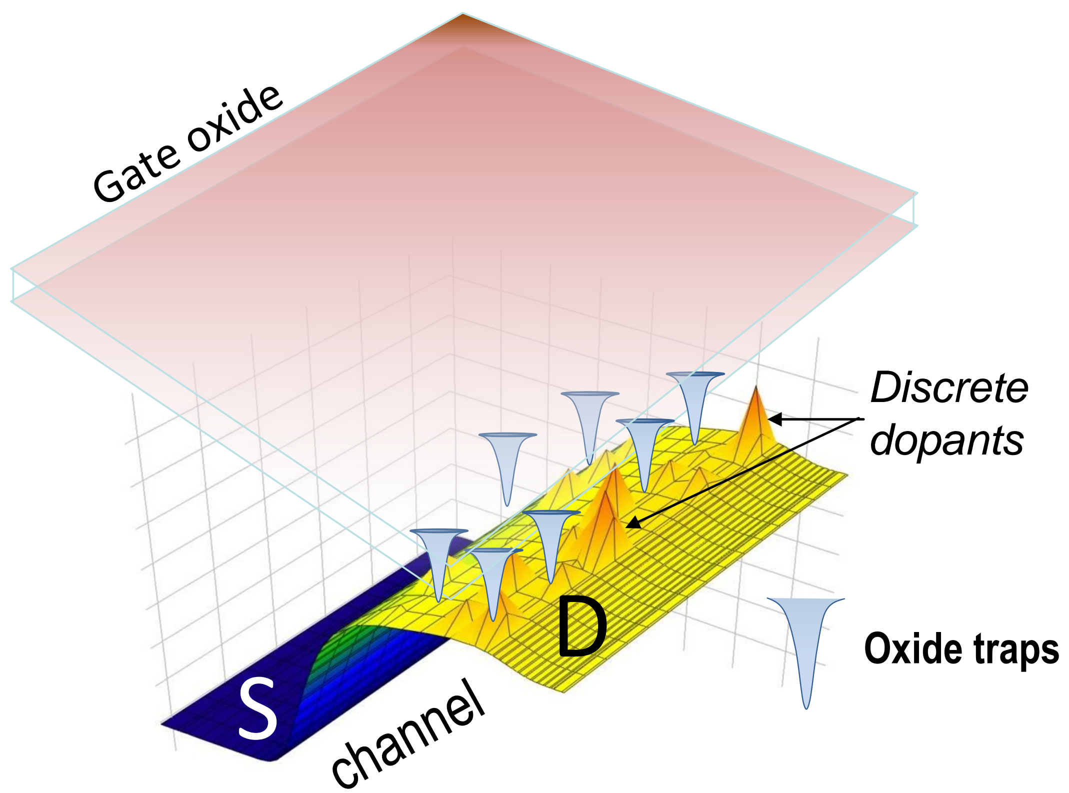


Fig. 3.1 V_{th} variation is dominated by the discrete dopants in the channel, known as RDF; however, after the stress, another effect, RTF caused by the traps, will also lead to V_{th} variation.

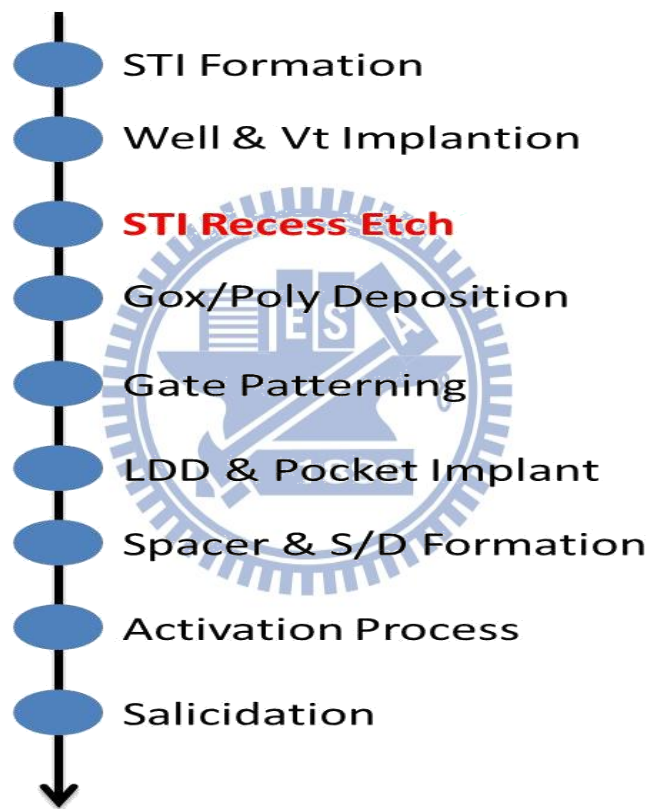


Fig. 3.2 Key process steps used to fabricate tri-gate bulk MOS devices in this work.

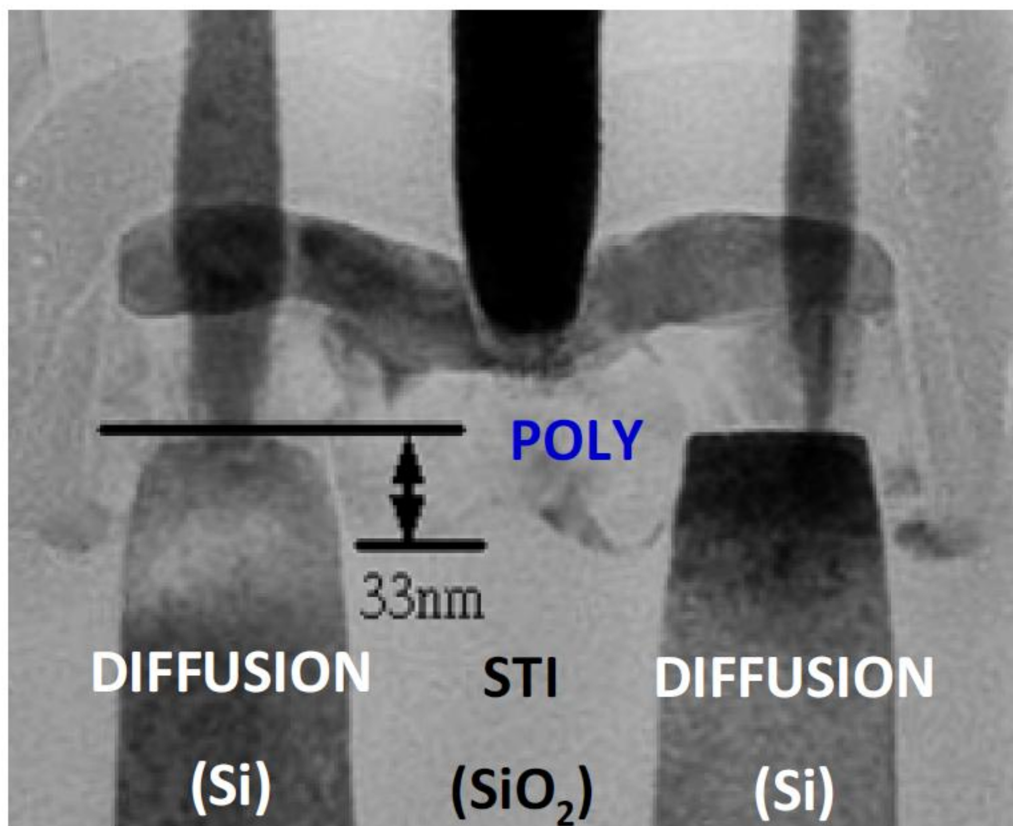


Fig. 3.3 Transmission electron microscopy cross-section taken along a poly-Si gate for 30nm nominal STI-oxide recess depths.

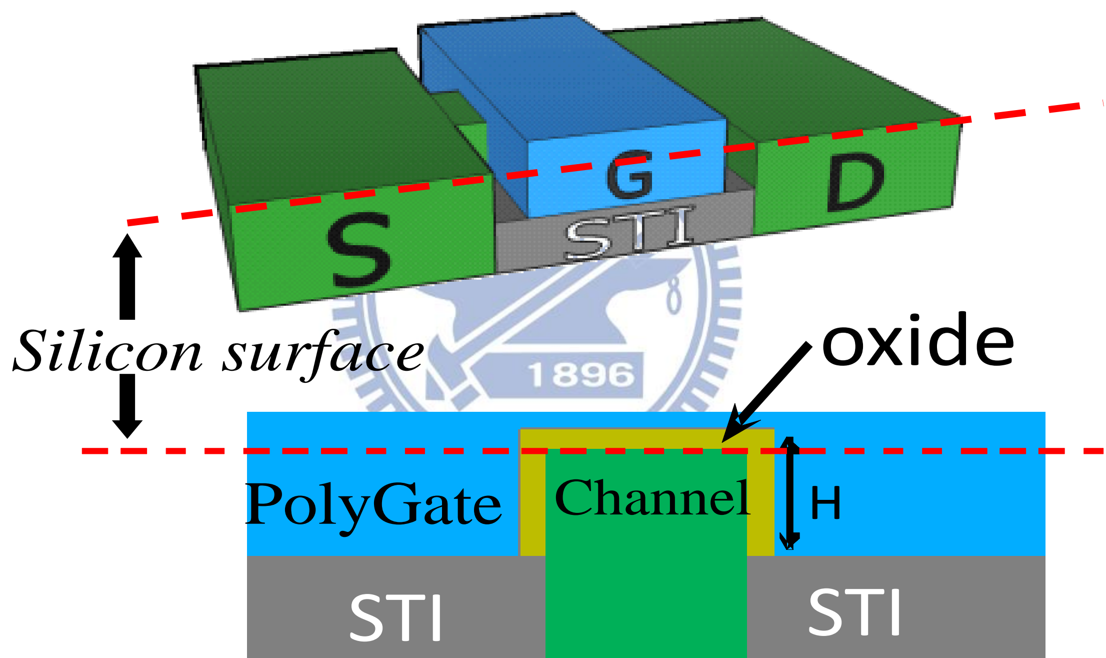


Fig. 3.4 (top) The 3D structure of bulk trigate formed by STI etching into the silicon surface, to form the Fin-channel; (bottom) the cross sectional view with fin height H. Drain current is perpendicular to this plane.

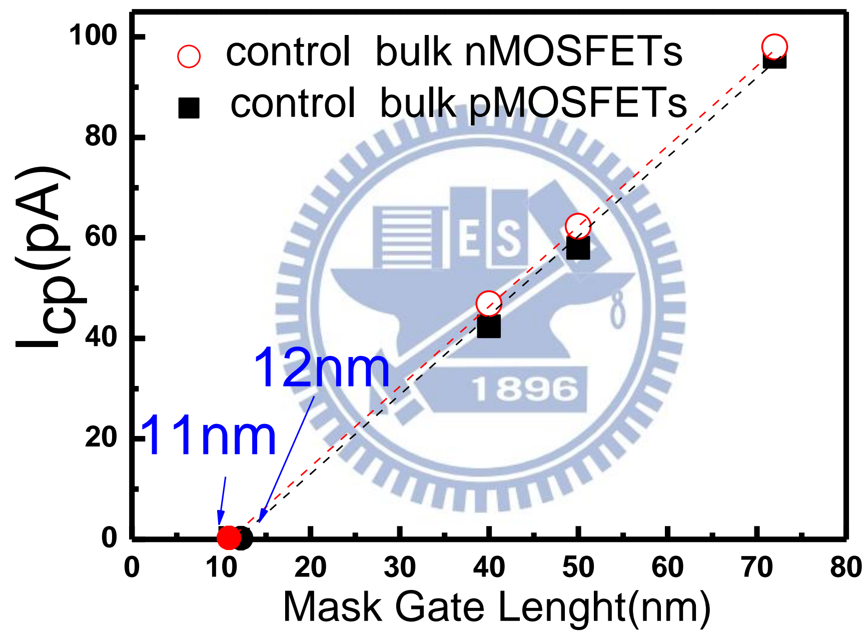


Fig. 3.5 The L_{eff} in Table 2 can be extracted by the charge pumping measurement. L_{eff}= L_{mask}- ΔL, ΔL= 12nm (nMOS), 11nm (pMOS).

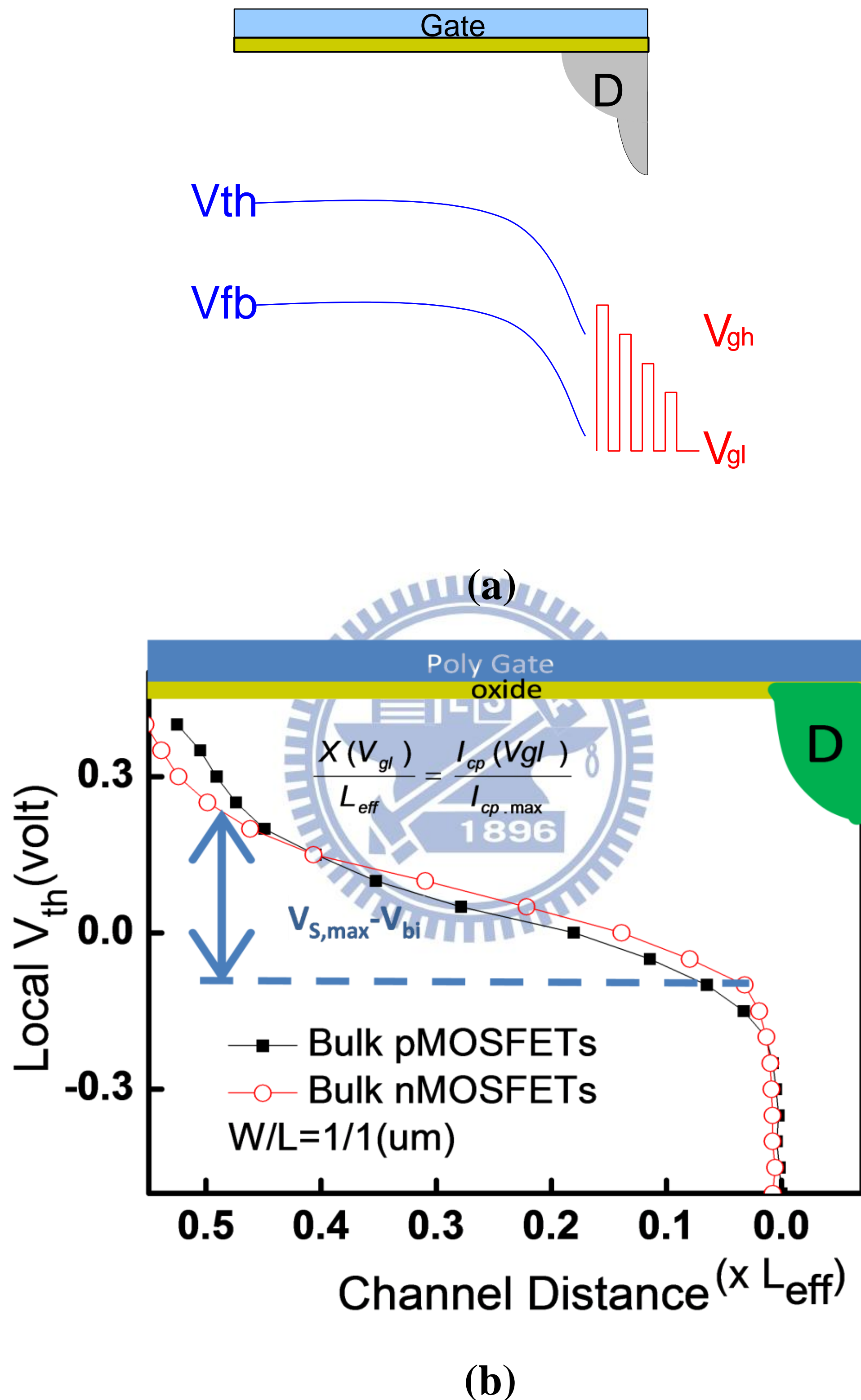


Fig. 3.6 (a) Illustration of the flat-band and local threshold voltages, (b) Using charge pumping measurement, the local threshold voltage can be profiled, where at the center ($0.5L_{eff}$), the local threshold voltage reaches the maximum.

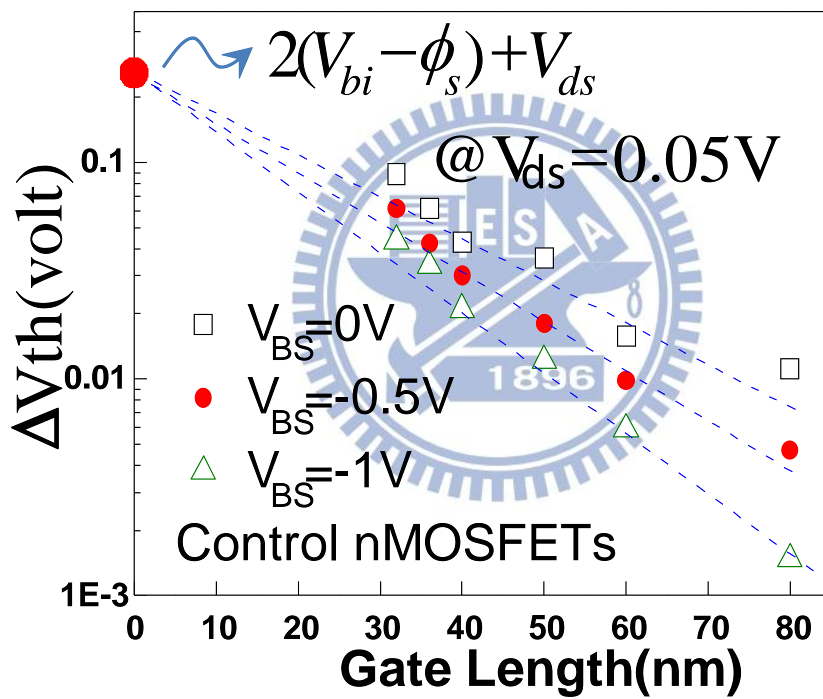


Fig. 3.7 V_{bi} can be determined from V_{th} by varying V_{bs}, and the extrapolated value at zero gate length yields to $2(V_{bi}-\phi_S) + V_{ds}$ such that V_{bi} can be found.

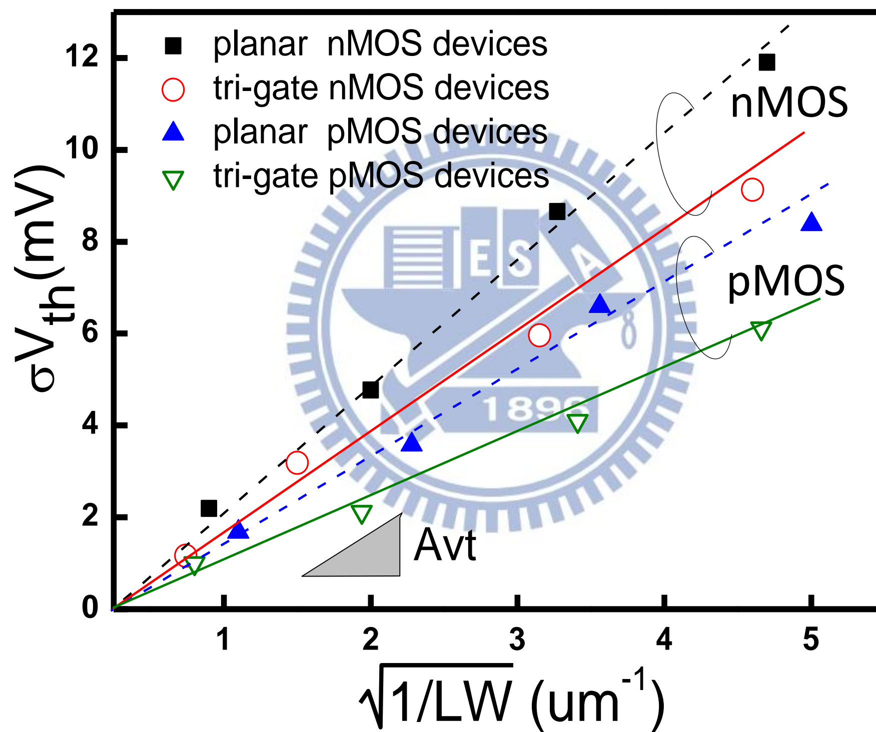


Fig. 3.8 The trigate devices shows obvious lower slopes of Avt than the planar ones (control) because a stronger gate field in trigate tends to inhibit the discrete dopant induced RDF.

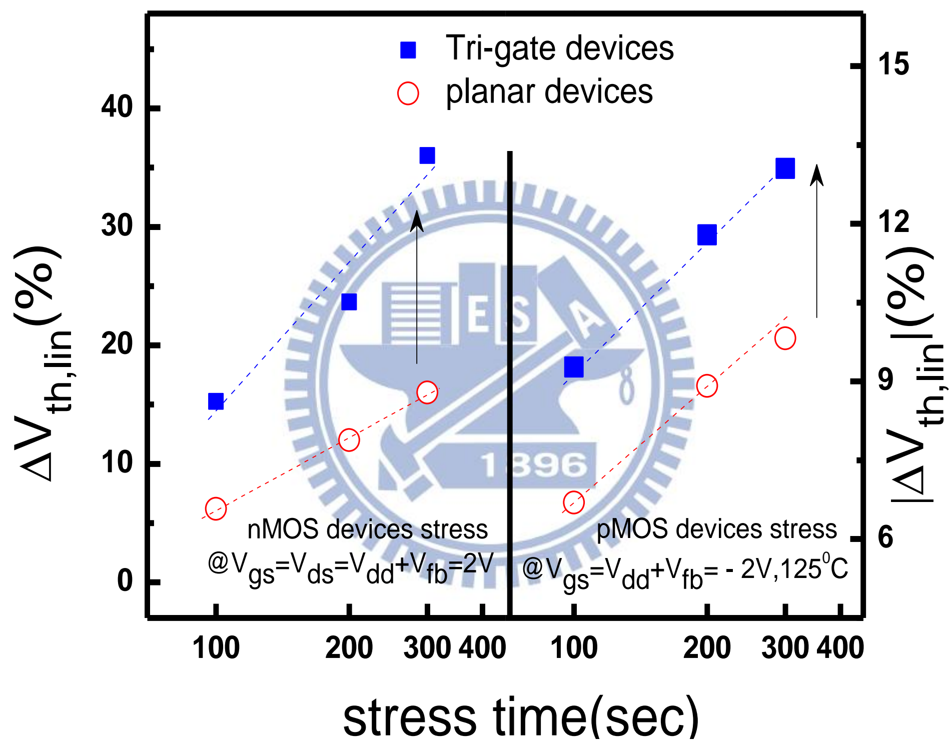


Fig. 3.9 Although trigate devices show good variability, they show much worse Vth degradation after the stress than that of the control, resulting in an increase of Vth variation.

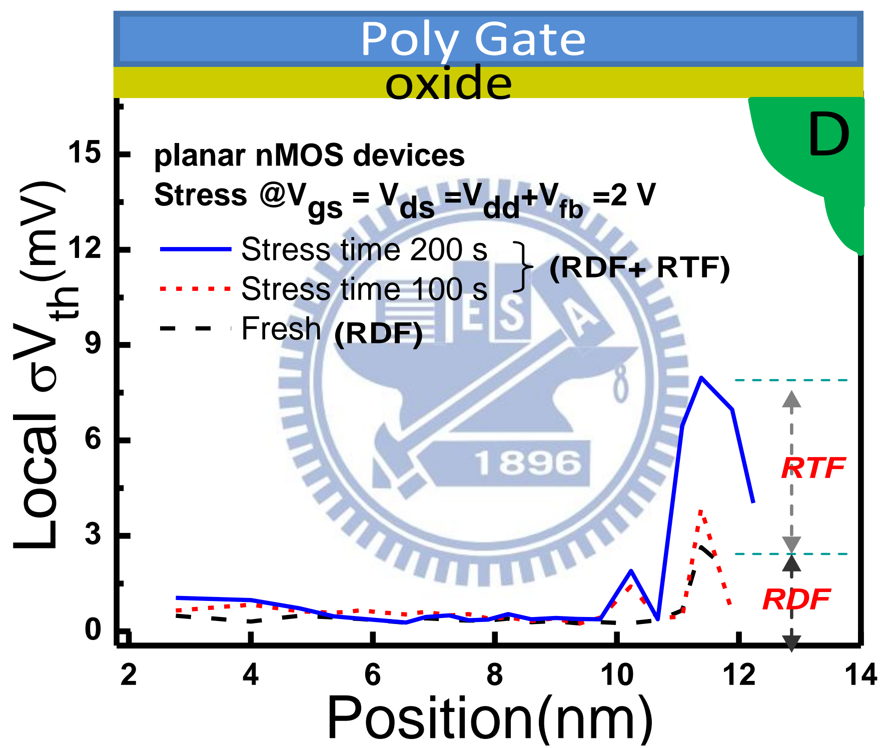


Fig. 3.10 The local σVth profiling results by RTP for planar devices. It was found that the peaks are near the drain edge of the devices after the HC stress.

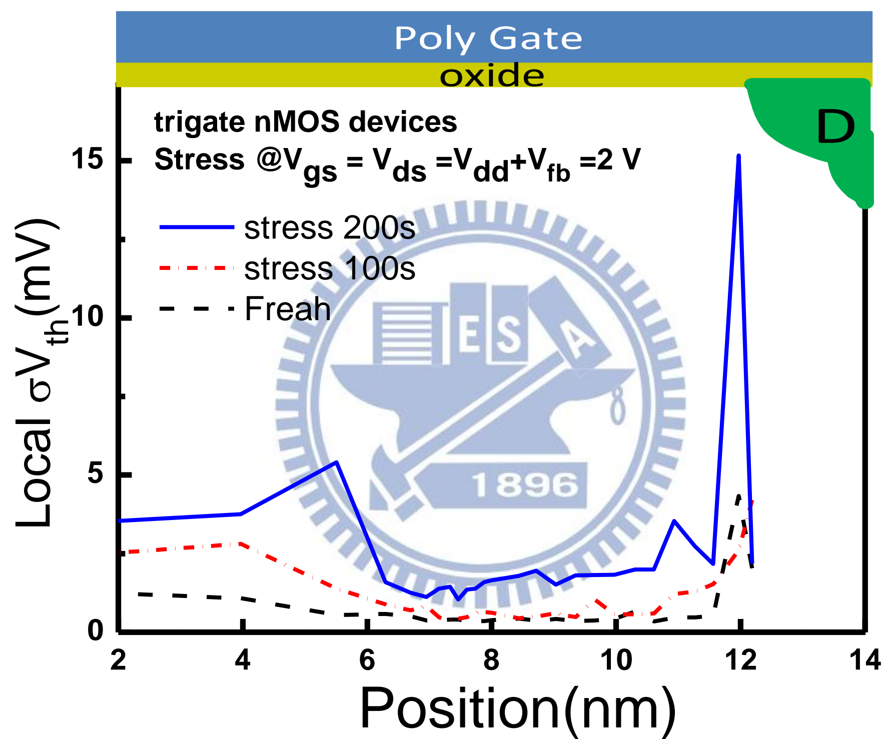


Fig. 3.11 The local σVth profiling results by RTP for trigate devices. It was found that the peaks are not only near the drain edge but also in the channel region after the HC stress.

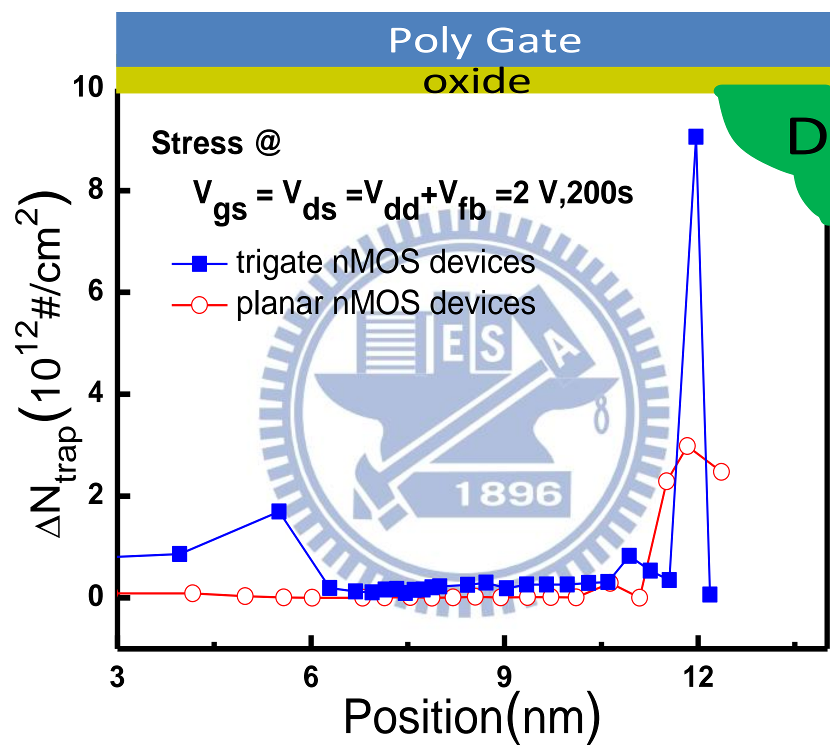


Fig. 3.12 The comparison of Δtrap densities for planar and trigate devices after the HC stress, showing that the traps of trigate device are much larger than those of planar device.

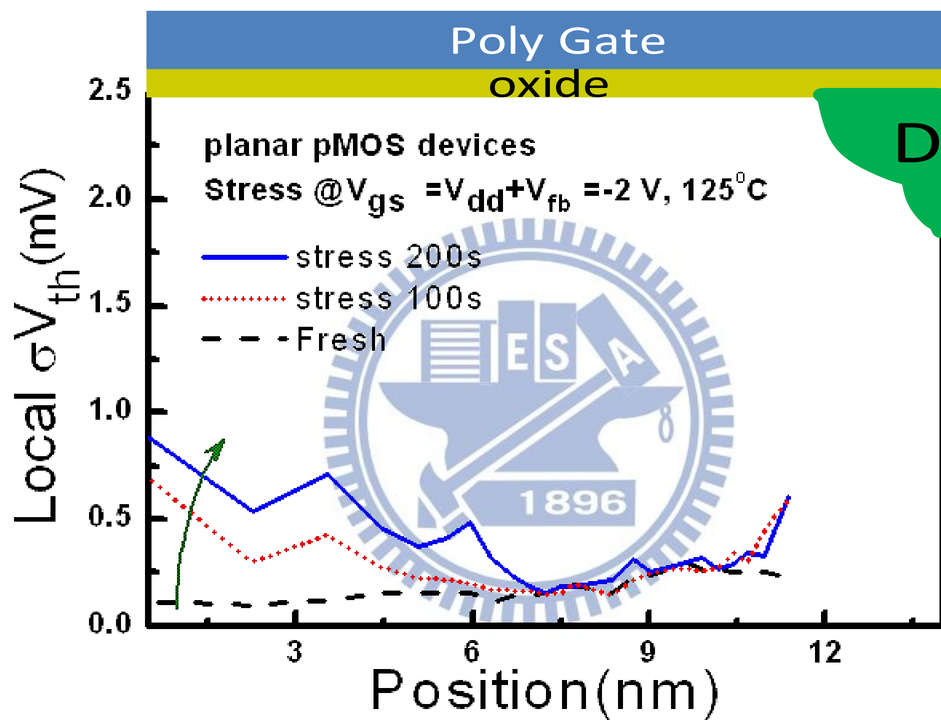


Fig. 3.13 The local σVth profiling results by RTP for planar devices. It was found that a larger amount of traps was generated in the channel center and drain edge after NBTI stress.

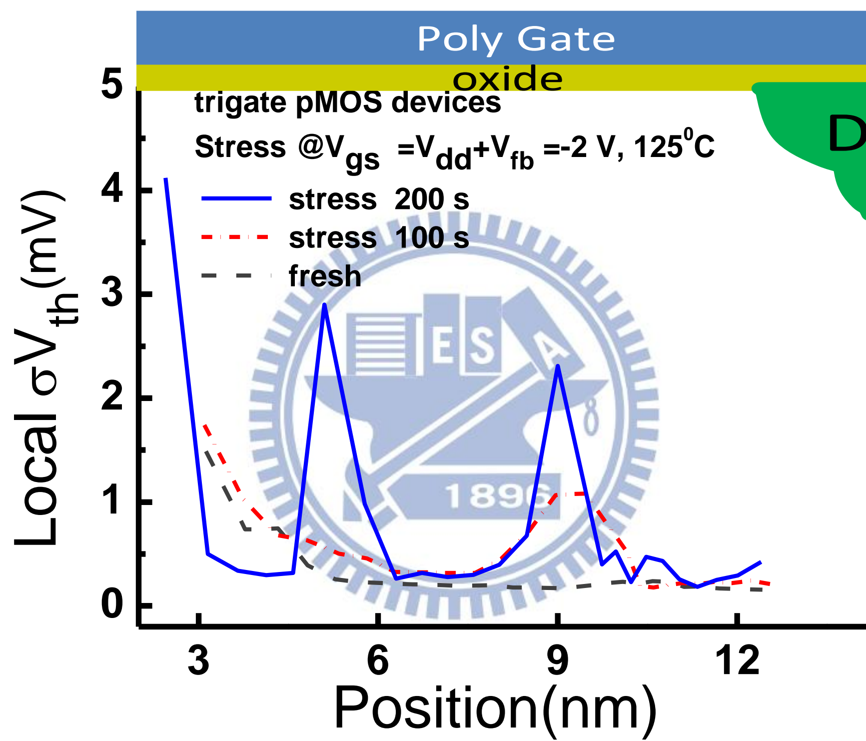


Fig. 3.14 The local σVth profiling results by RTP for trigate devices. It was found that many peaks are observed after NBTI stress in the channel region, coming from the sidewall roughness.

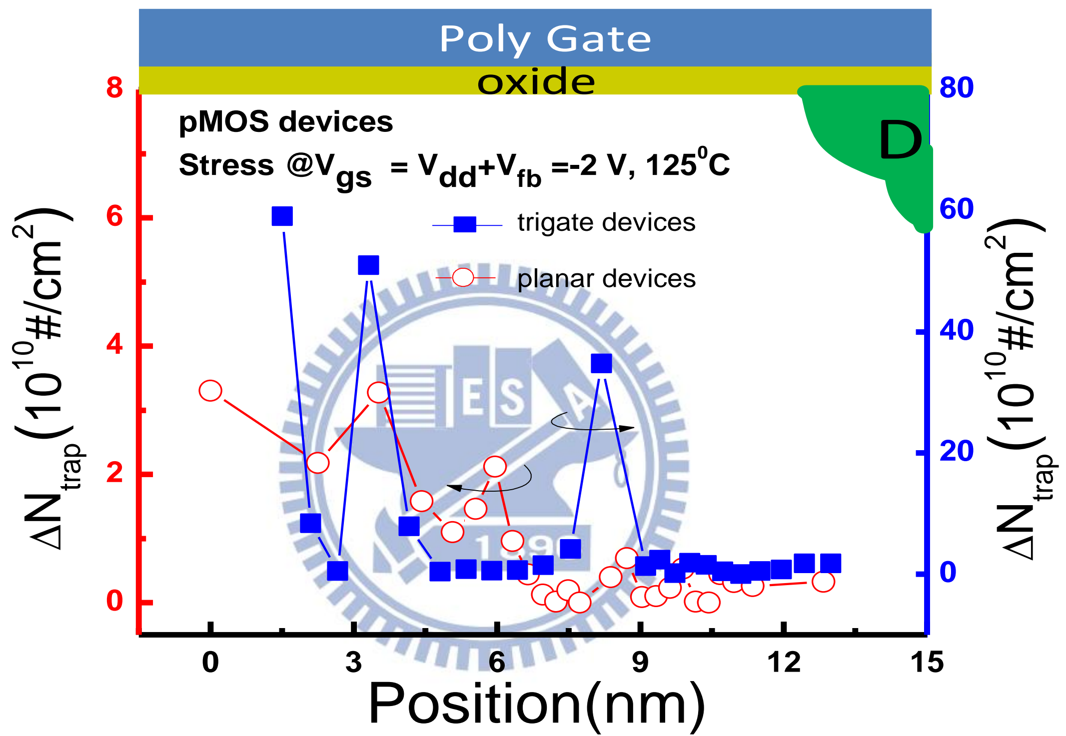


Fig. 3.15 The Δtrap densities of trigate devices are much larger than those of the control.

Stress Condition \ Splits	Average Increased Trap Density(cm^{-2})	
	Bulk Planar Devices	Bulk Trigate Devices
HC stress@ $V_{gs}=V_{ds}=V_{dd}+V_{fb}$, 25^0C, 200sec	1×10^{12}	1.8×10^{12} ($\times$ 1.8)
NBTI stress@ $V_{gs}=V_{dd}+V_{fb}$,125^0C,200sec	1.3×10^{10}	1.8×10^{11} ($\times$ 13.8)

Table 3.1 The comparison of the generated trap densities for trigate and planar devices after HC or NBTI stress, showing that NBTI stress dominates the reliability of trigate devices due to the surface roughness and corner effect of sidewall.

Chapter 4

Experimental Observation on the Trap Fluctuation of Small Scale Trigate CMOS Devices

4.1 Introduction

Trigate is a promising structure for MOS transistors with gate lengths of 20 nm and smaller. Several variants of the gate design in trigate device have been suggested [4.1]. In the trigate case, the gate wraps around the rectangular silicon fin from three sides. The Trigate device has a large effective channel width: $W_{eff}= 2*T_{fin} + W_{fin}$. So, the use of the gate wrap around design is attractive since a significantly higher drive current can be achieved for the same minimum feature size.

In this chapter, we will demonstrate that V_{th} variation can be suppressed by advanced 3D technology meanwhile the performance of devices keeps improved for MOS devices. Extensive comparisons between trigate and segmented trigate devices will be justified on examining the effects of electrical field and sidewall height [4.2]. In addition, the impact of corner effects on the device variability will also be verified [4.3]. The comer effect which is known to make worse the electrical performance of the shallow trench isolated (STI) MOS transistors [4.4-5]. In this chapter, we will examine the comer effect on the electrical performance of trigate transistors with minimum feature size of 36 nm.

For trigate devices after the HC stress, not only the local V_{th} variation was observed near the drain edge but also on the sidewall, meaning that the sidewall is a critical region in terms of trigate reliability. We suspect that the sidewall corner effect induced a high electric field, consequently generating the traps [4.6]. For the trigate devices, not only the electric field and

impact-ionization at the corner of the sidewall but also the surface roughness at the sidewall need to be taken care of. Therefore, this study will investigate the effect of varying sidewall height in the trigate devices.

4.2 Device Preparation

Advanced poly-Si gate bulk trigate devices, with SiON insulator, were fabricated. After the conventional STI process, well formation, and V_T-adjust ion implantation, the STI oxide was slightly recessed by various amounts (10nm, 15nm, or 30nm) on selected wafers just prior to gate-stack formation. The schematic cross section diagram of trigate MOS device splits are shown in Figs. 4.1-4.2. Also, the electrical characteristics are given in Fig. 4.3, where the driving current of low S/D resistance trigate device is larger than the low R_{sd} ones. The width of trigate is 45nm and the height is different by recessed depth. The effective channel length, L_{eff}= 25nm for n type and L_{eff}= 24nm for p type devices. Both control and split are made on the same wafer. To exclude and avoid the parasitic effects, single-fin devices were prepared. Devices with different areas were used to calculate the V_{th} variations.

4.3 Factors Affecting the Reliability in Trigate nMOSFET

4.3.1 Stress voltage bias dependence

To characterize the oxide trap spatial distribution, random trap profiling was performed after hot carrier (HC) stressing the trigate nMOS devices. (Figs. 4.4-4.5) By changing the vertical electric field, it was found that the density of trap becomes larger near the drain edge after the stress, and the position of the most serious damage was not changed by the vertical

electric field. On the other hand, by changing the lateral electric field, it was found that the region of the distribution of trap, and the density of trap was not increased more heavily by the stress. We suspect that the electric field was controlled by the bias voltage.

4.3.2 S/D Resistance dependence

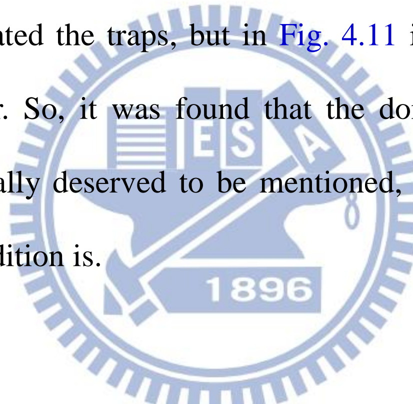
In this part, we will investigate the threshold voltage degradation characteristics of the fabricated high and low S/D resistances, Fig. 4.2, respectively. Gate length (L_g) for device is 36 nm, and effective channel length (L_{eff}) is 25 nm. Owing to the surrounding-gate structures, healthy switching characteristics are obtained even at low S/D resistance device [4.7-8]. An increment of S/D series resistance gives rise to a decrease in the effective drain voltage ($V'_D = V_D - 2*I_D*(R_{S/D} + R_{ext})$ as well as the lateral channel field for a given external drain bias (Fig. 4.6). Under the hot carrier stress, the degradation of V_{th} is largely increased for low resistance device, because the device contain larger electric field; on the other hand, the electric field of high resistance device was smaller, because there is a voltage drop across the source/drain series resistance. Therefore, the surface roughness effect for low S/D resistance device is much worse than the high S/D resistance device. The results are shown in Fig. 4.7 and Fig. 4.8.

4.3.3 Corner effect

In general, the corner effect is good for the device performance [4.3], because the stronger electric field will increase an additional edge current, but the higher electric field is harmful to the device seriously. The local V_{th} variation was observed near the drain edge but also on the sidewall, meaning that the sidewall creates another effect. The illustration (Fig. 4.9)

of the high electric field at the trigate corner in Fig. 4.9 will induce the RTF for devices after the HC stress. It can be seen that the current flow is pushed toward the corners in the case of trigate MOS device (2-corner effect). The issue causes slightly higher local standard deviation of threshold voltage which is produced by interface traps.

First, we measured hot carrier degradation in bulk trigate devices under the bias condition of V_{GS}= V_{DS}= 1.7 volt and 2.2 volt, because the worst stress condition at operating voltage is V_{GS}= V_{DS}. In low electric field case, it shows that the degradation is dominated by corner effect, Fig. 4.10, because the local V_{th} variations near the drain edge and middle of channel are similar. On the other hand, we suspect that the sidewall corner effect induced a high electric field and generated the traps, but in Fig. 4.11 it shows that the degradation is dominated by the hot carrier. So, it was found that the dominated effect was different in varying electric field, especially deserved to be mentioned, the corner effect was found no matter whether the stress condition is.



4.3.4 Fin Height dependence under HC stress

As the stress bias is increased, the degradation of V_{th} is accelerated due to the incremental change in the electric field. Larger degradation is observed at the shorter fin height rather than at the higher fin height under the same stress condition [4.9]. Due to the low fin height device, it will induce a higher electric field for devices after the HC stress, Fig. 4.12. The ΔN_{trap} profiling for different Fin-height trigate devices after HC stress is show in Fig. 4.13. More traps are observed for lower Fin-height device as a result of larger electric field.

4.4 Factors Affecting the Reliability in Trigate pMOSFET

4.4.1 Surface roughness

To enhance the driving current of the trigate MOS devices, the higher sidewall was evaluated. Fig. 4.14 is the change of driving current of the same trigate devices (equivalent effective length and gate width) when the sidewall depth increases up to 30 nm. To examine the sidewall effects, devices with three different sidewall heights have been compared, Fig. 4.15, in which the higher the sidewall is, the more device degradation becomes as a result of the sidewall roughness and a high electric field on the sidewall corner. As expected, the drive current of devices increase as the recess depth increases from 10 nm, 15 nm, and to 30 nm. Unfortunately, the variation of the trigate devices is larger when the height of the sidewall increased by process (Fig. 4.16). And, the threshold voltage was degraded in higher sidewall device. This means that the trigate MOS devices will suffer from serious variability problem without tight control of sidewall height. One way to handle this problem will be to use more controllable process.

4.4.2 The Shallow Trench Isolation effect

NBTI stress was also applied to examine the degradations of the trigate pMOS devices. To further identify the local V_{th} variation caused by the STI effect, we measured the fresh devices for three different fin spacing devices as shown in Fig. 4.17. According to the results of the distributions of dopant densities (DDP) measurement in this figure, obviously, the variation of the local V_{th} is larger for narrow fin spacing devices. In addition to DDP measurement, the distribution of traps was observed by RTP measurement, too, Fig. 4.18. The

region of FET near the STI beak has been suffered from the stress of the beak and induced the traps in the region. For narrow fin spacing devices that exhibit a sharp beak, Fig. 4.19, it induces higher electric field under the stress.

4.5 Discussion

As a result, in bulk trigate nMOS devices, the trap density was much higher than that of the convention trigate after the HC stress. Because the high electric field was induced by corner structure, so the damage becomes more serious for trigate devices. In addition, the influence of corner effect under varying electric field is summarized in Table 2. According to the measured data, we know that the average increased trap density near the drain edge was 2.18 times as large as the average increased trap density in the middle channel for low electric field case. On the other hand, the average increased trap density near the drain edge was 3.35 times as large as the average increased trap density in the middle channel for high electric field case, so the corner effect will dominate the reliability of segmented trigate devices for low voltage operation.

To examine the sidewall effects, devices with three different sidewall heights have been compared, Table 3, in which the higher the sidewall is, the more device degradation becomes as a result of the sidewall roughness and a high electric field at the sidewall corner.

In Fig. 4.20, the interface state density of Fin structure was measured by fabricating trigate devices with RTP method, from Fin height dependency, ΔNtrap of 3.1×10^{10} (# • cm^{-2}) of top surface was obtained, meaning that NBTI stress dominates the reliability of trigate devices due to the sidewall surface roughness, and the 10-year lifetime prediction for trigate

pMOS devices after the NBTI stress. It shows that the higher the fin is, the device shows poorer lifetime, Fig. 4.21.

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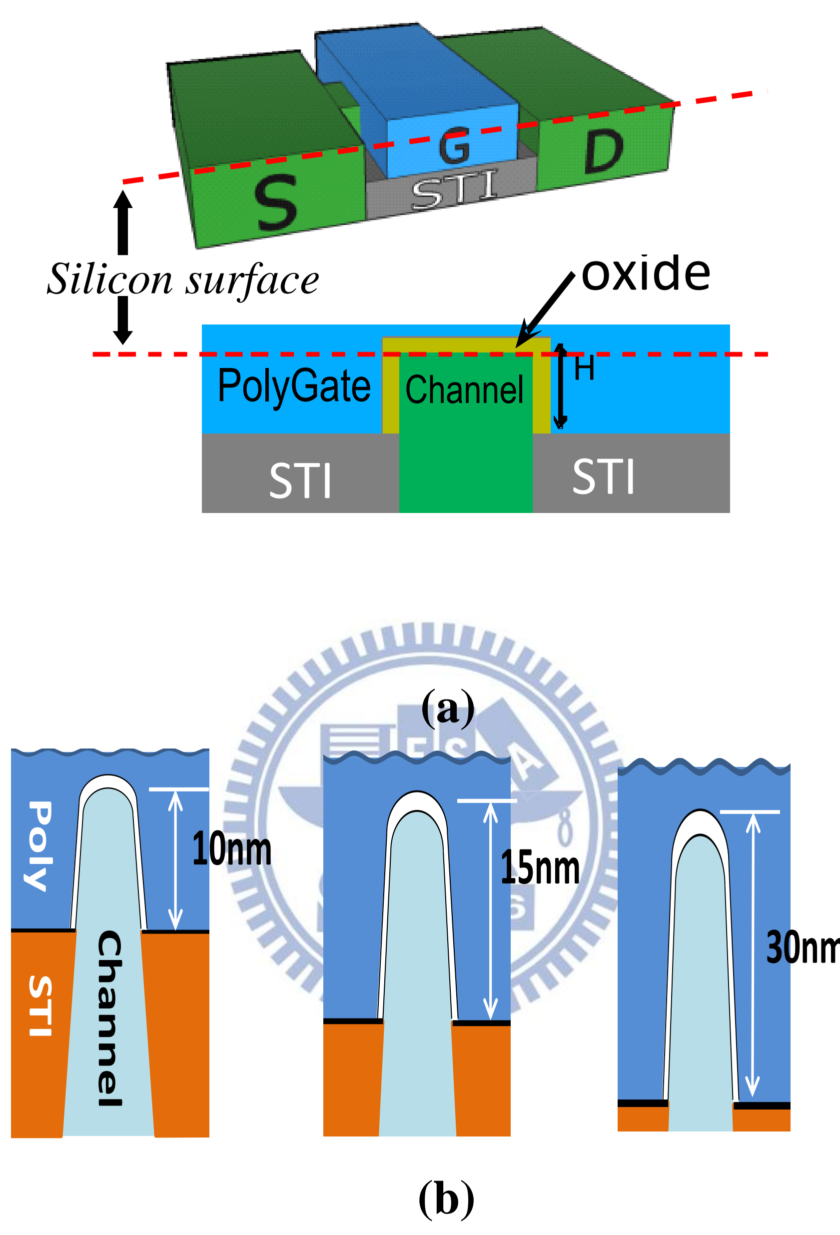


Fig. 4.1 The 3D structure of bulk Trigate (a) and split of Fin height (b), to form the Fin-channel the cross sectional view with fin height H. Drain current is perpendicular to this plane.

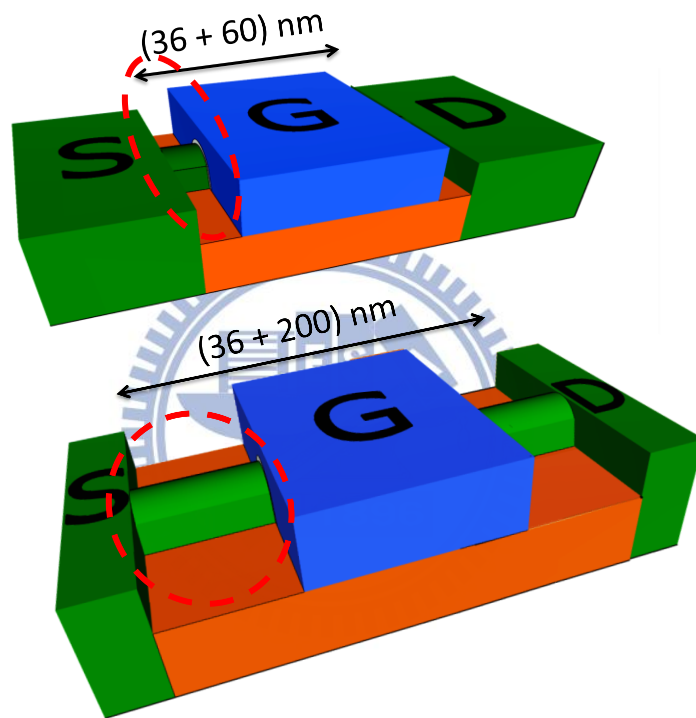


Fig. 4.2 Illustration of the comparison between (a) high R_{sd} (b) low R_{sd}, the total length of the high device is 36nm (gate length) + 200nm (S/D); on the other hand, the total length of the low device is 36nm (gate length) + 60nm (S/D).

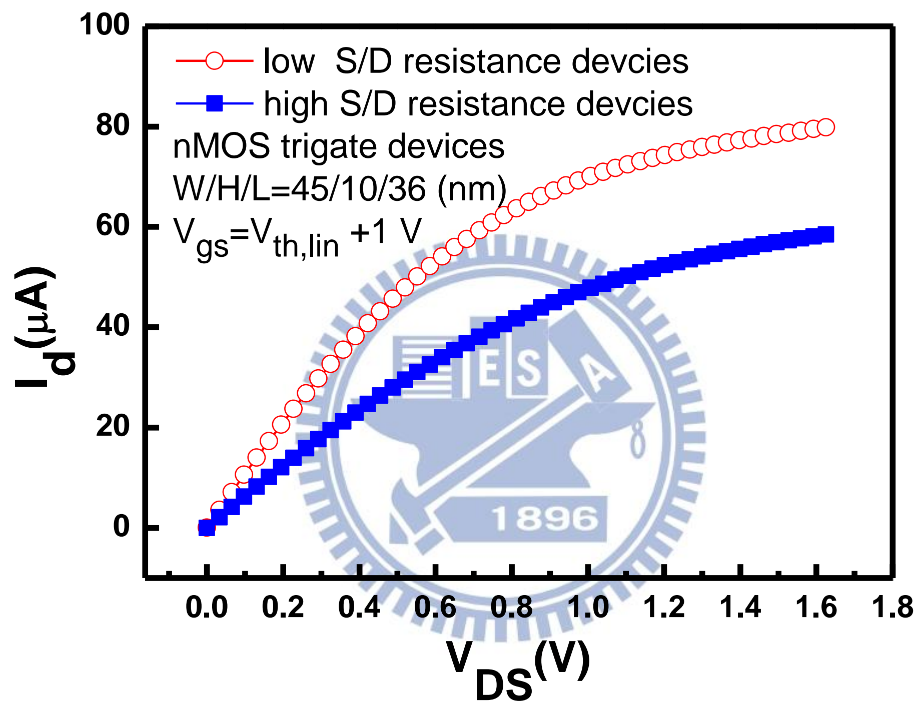


Fig. 4.3 Comparisons of measured output characteristics for low Rsd vs. high Rsd bulk trigate MOS devices, I_D-V_D curve.

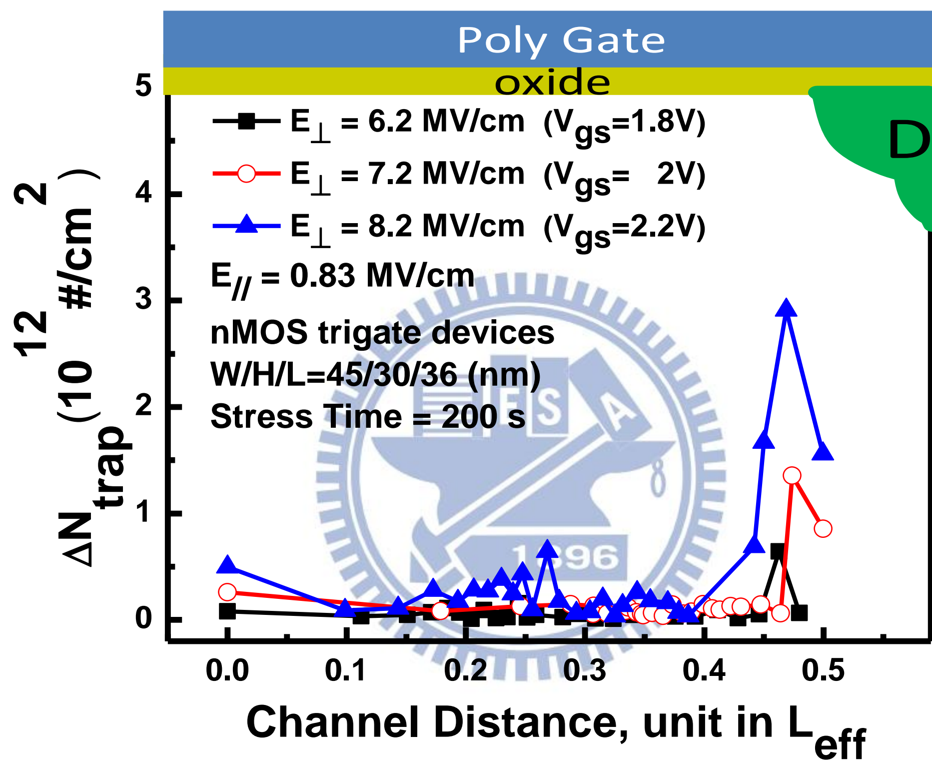


Fig. 4.4 ΔN_{trap} profiling by different stress condition, different gate voltage bias, showing that the trap distribution is affected by the stress bias.

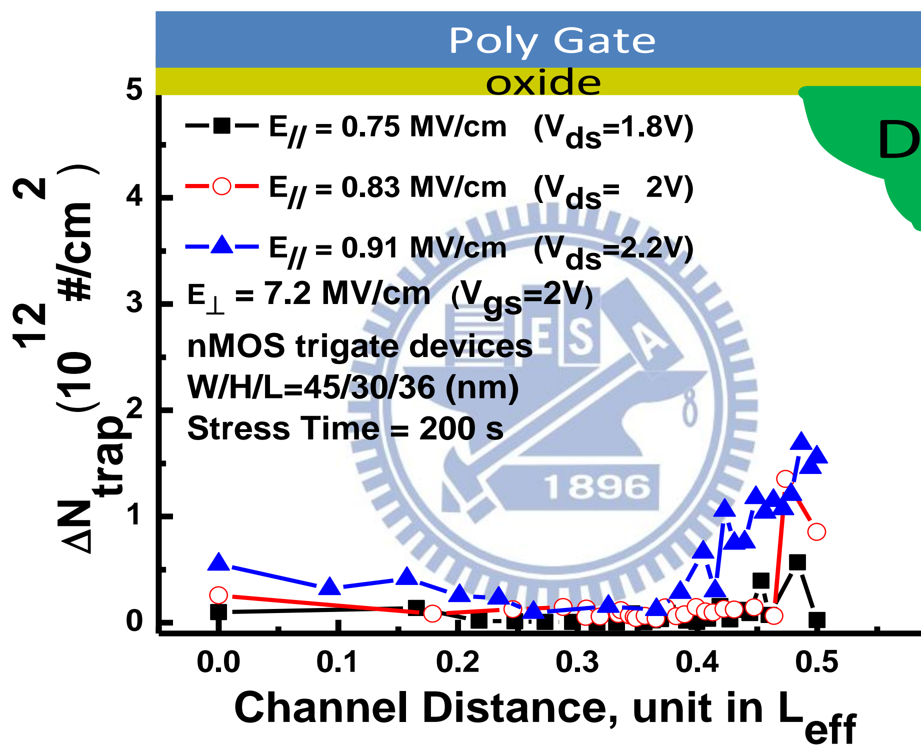


Fig. 4.5 ΔN_{trap} profiling by different stress condition, different drain voltage bias, showing that the trap distribution is affected by the stress bias.

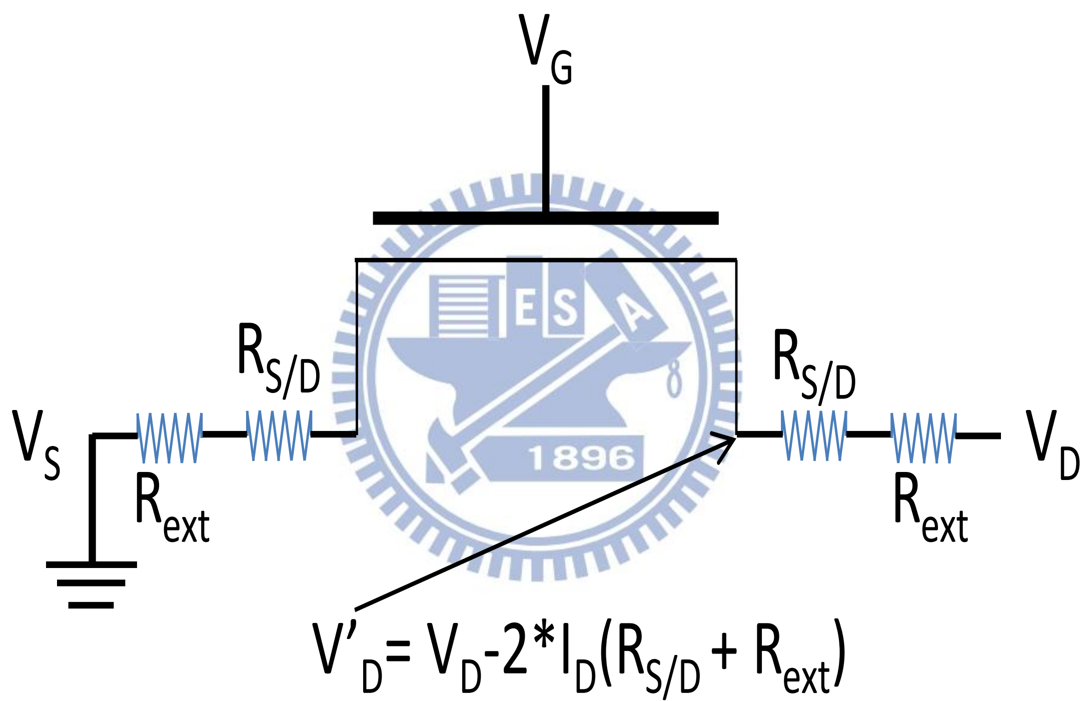
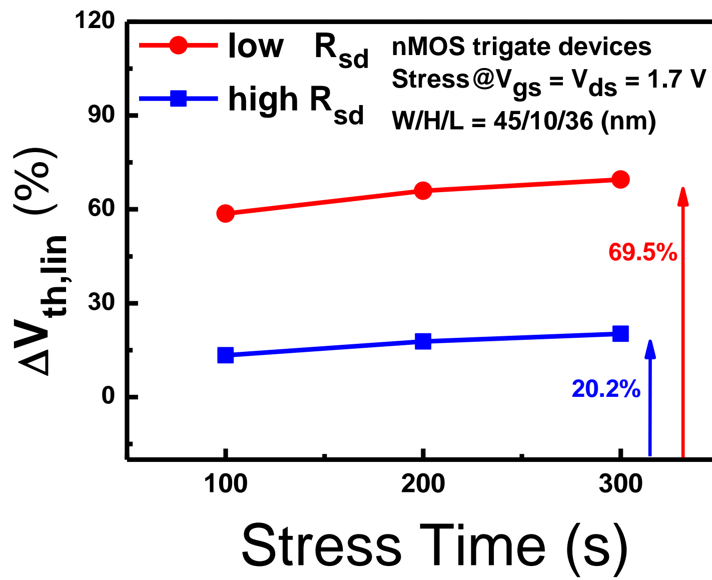
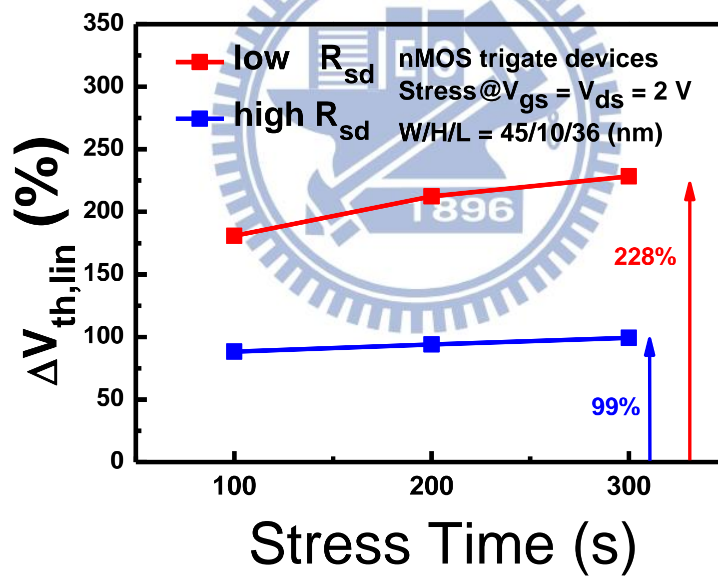


Fig. 4.6 Illustration of S/D series resistance giving rise to a decrease in the effective drain voltage as well as the lateral channel field for a given external drains bias.



(a)



(b)

Fig. 4.7 The threshold voltage degradation in (a) low electrical field and (b) high electrical field, which show obvious serious V_{th} degradation in Trigate devices.

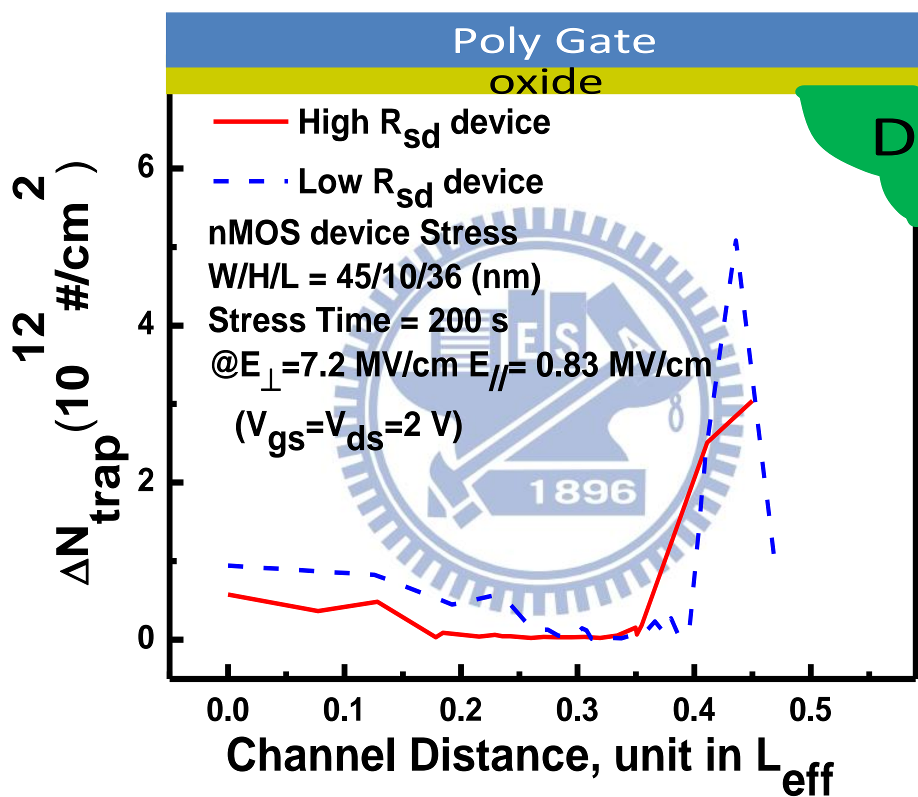


Fig. 4.8 ΔN_{trap} profiling for different R_{sd} trigate devices after NBTI stress. By increasing the resistance, the reliability was enhanced by high R_{sd}.

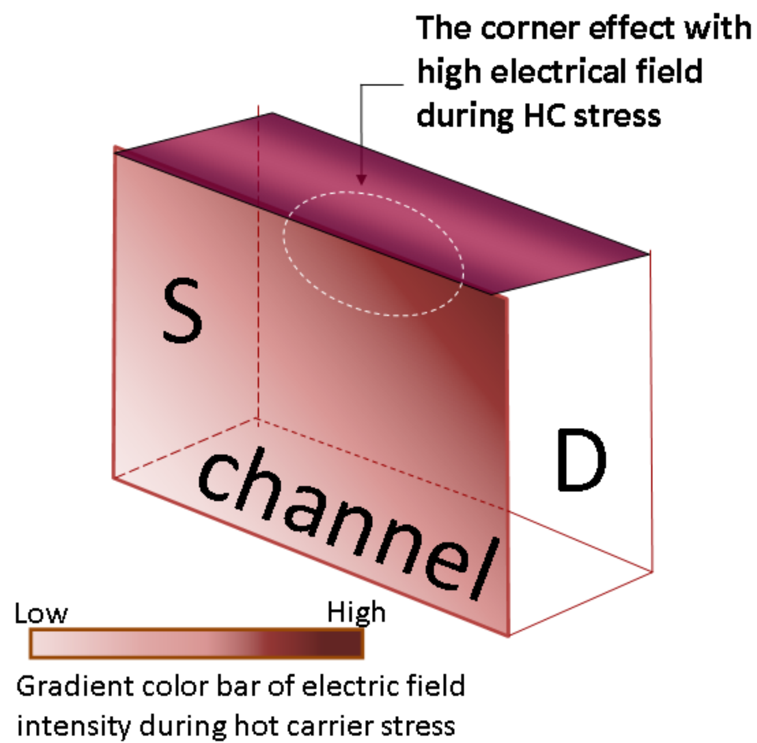


Fig. 4.9 Illustration of the high electric field distribution at the corner and drain edge for trigate which will induce the RTF for devices after the HC stress.

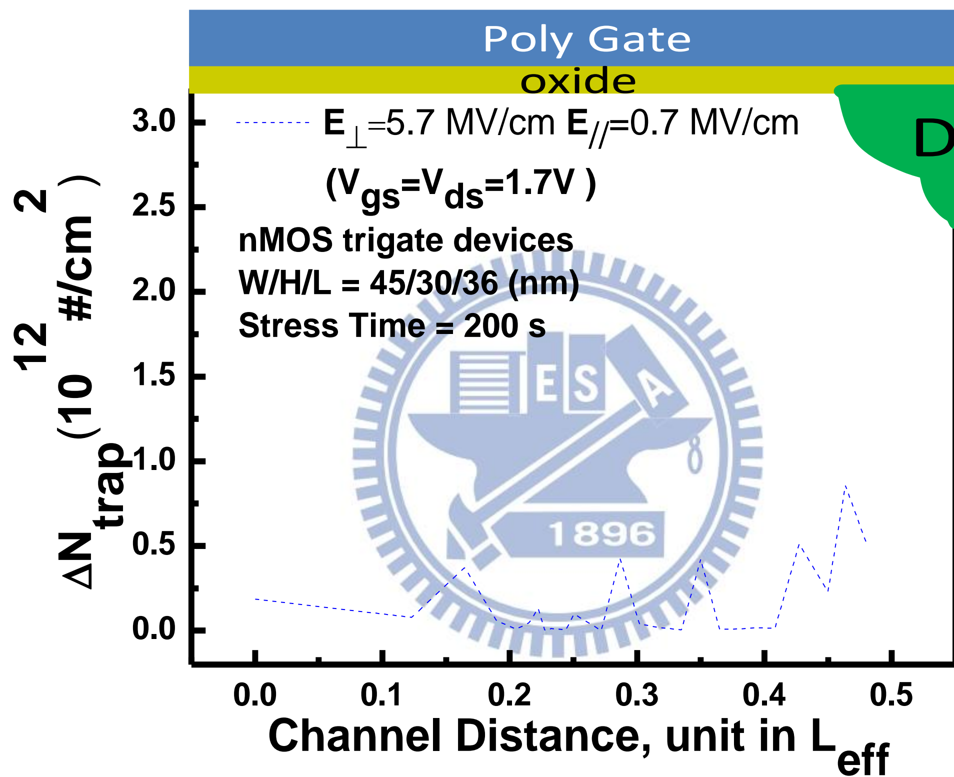


Fig. 4.10 ΔN_{trap} profiling results by RTP for low electric field condition. It was found that the peaks are not only near the drain edge but also in the channel region after the HC stress.

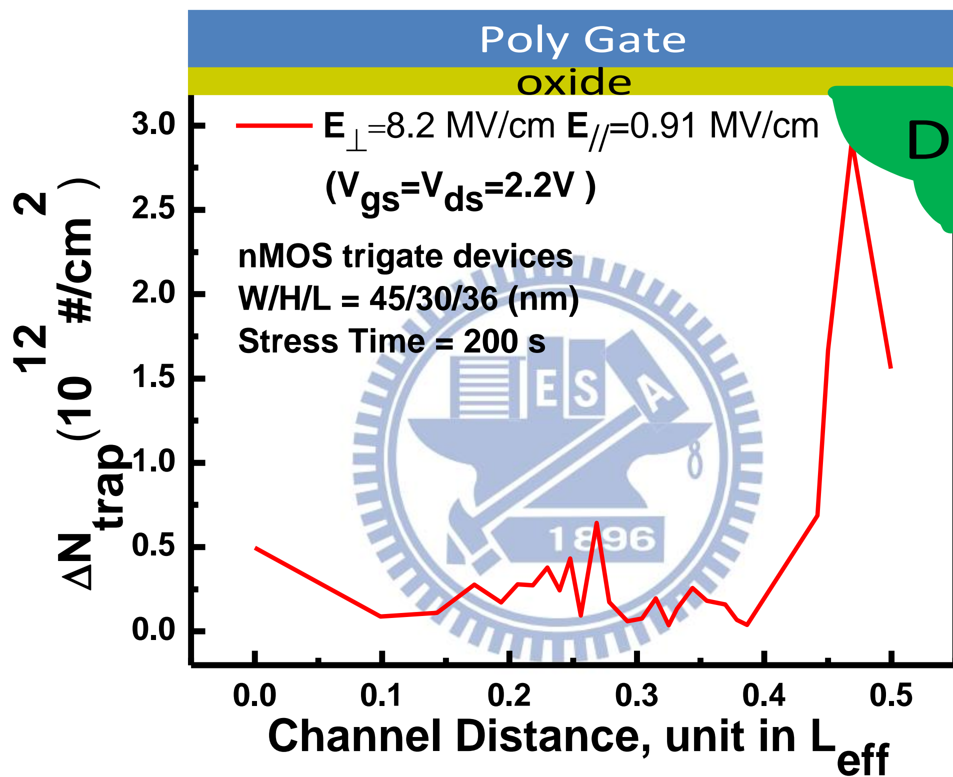


Fig. 4.11 ΔN_{trap} profiling results by RTP for high electric field condition. It was found that the peaks are not only near the drain edge but also in the channel region after the HC stress.

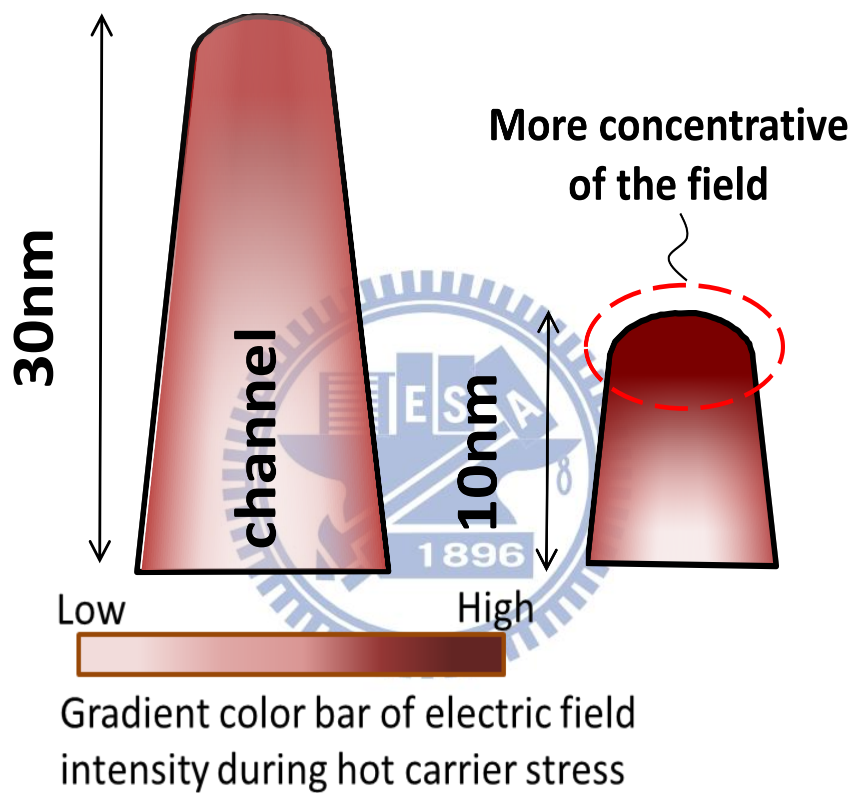


Fig. 4.12 Illustration of the high electric field at the low fin height device which will induce the higher electric field for devices by the HC stress.

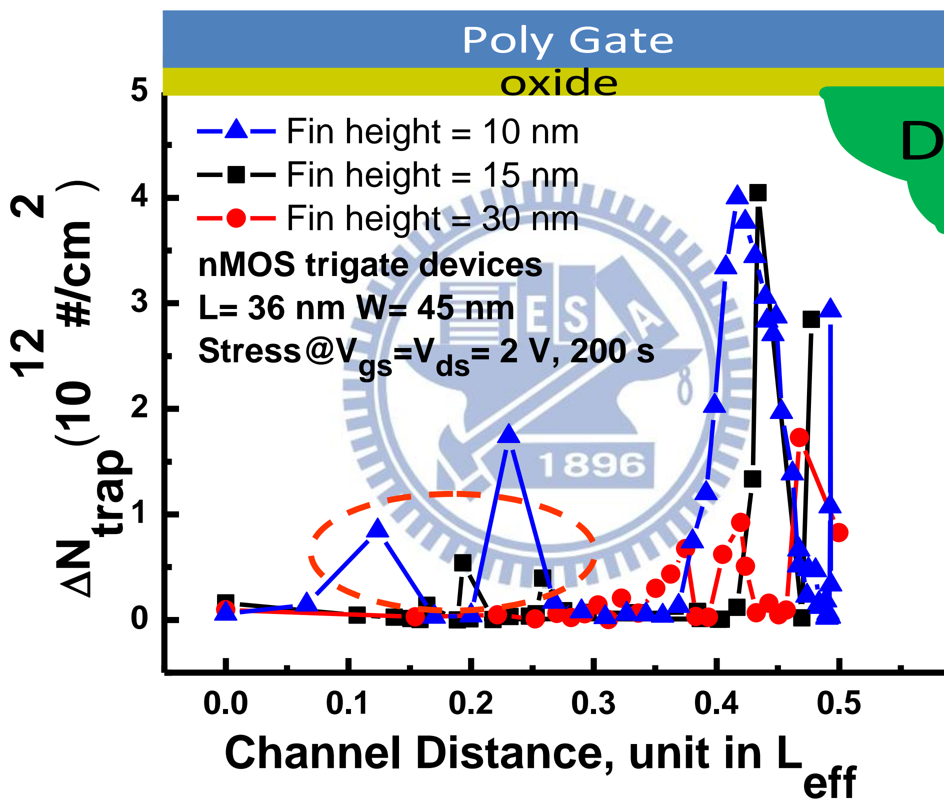


Fig. 4.13 ΔN_{trap} profiling for different Fin-height trigate devices after the HC stress. More traps are observed for lower Fin-height device as a result of larger electric field.

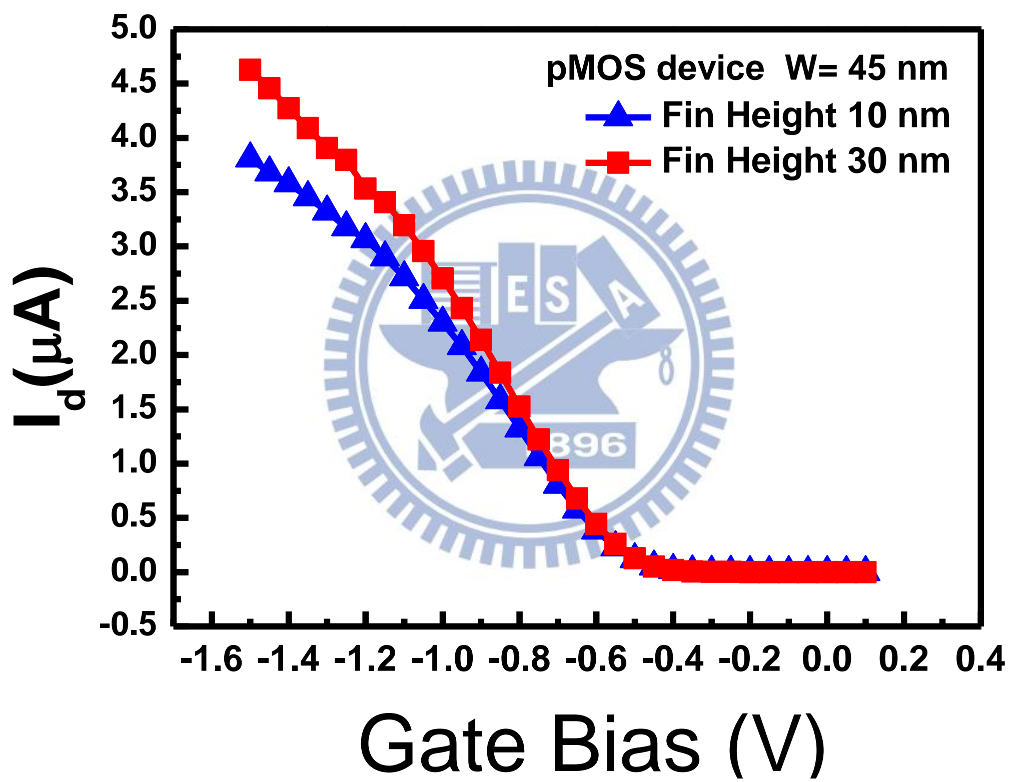


Fig. 4.14 Comparisons of transfer characteristics of P-channel trigate devices for two different fin height values.

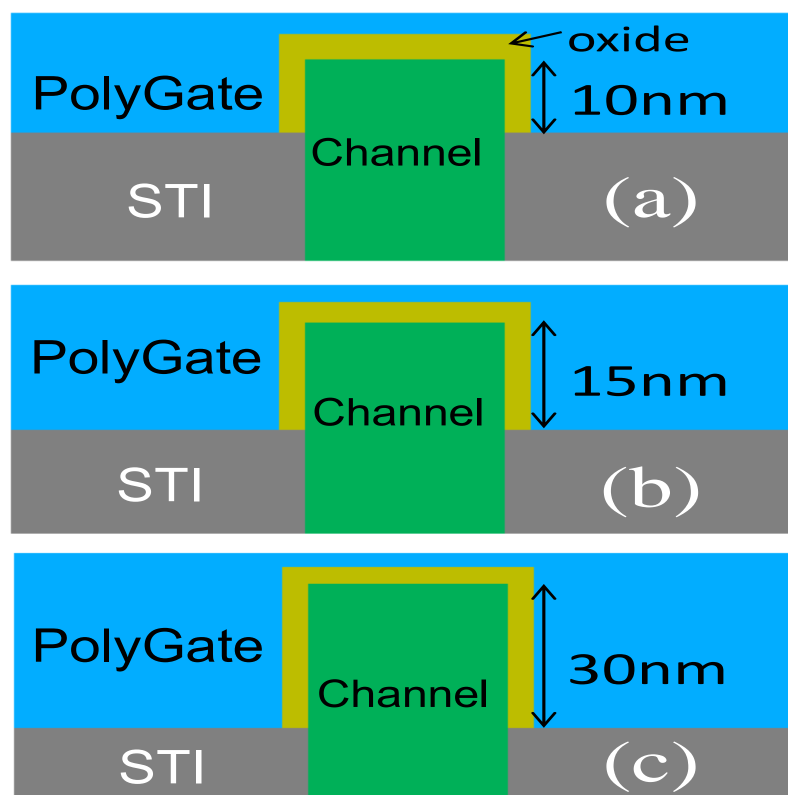


Fig. 4.15 To study the sidewall effects on the degradation of stressed trigate devices, three different sidewall devices were measured.

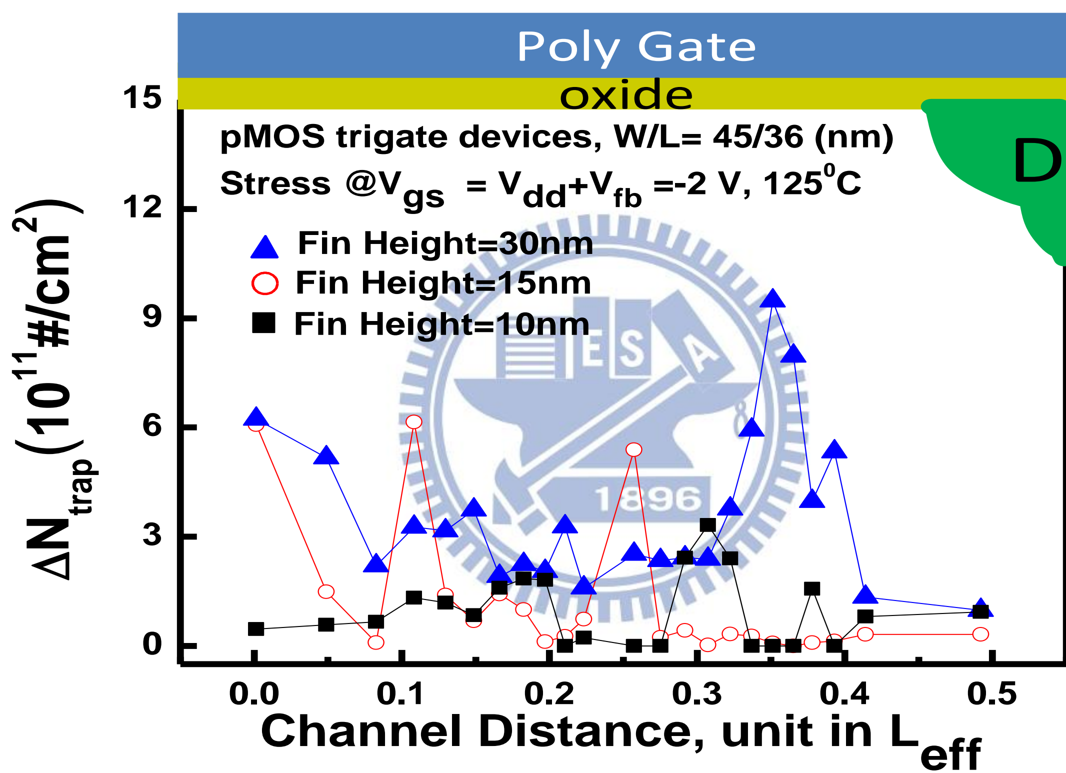


Fig. 4.16 ΔN_{trap} profiling for different Fin-height Trigate devices after the NBTI stress. More traps are observed for larger Fin-height device as a result of sidewall roughness effect.

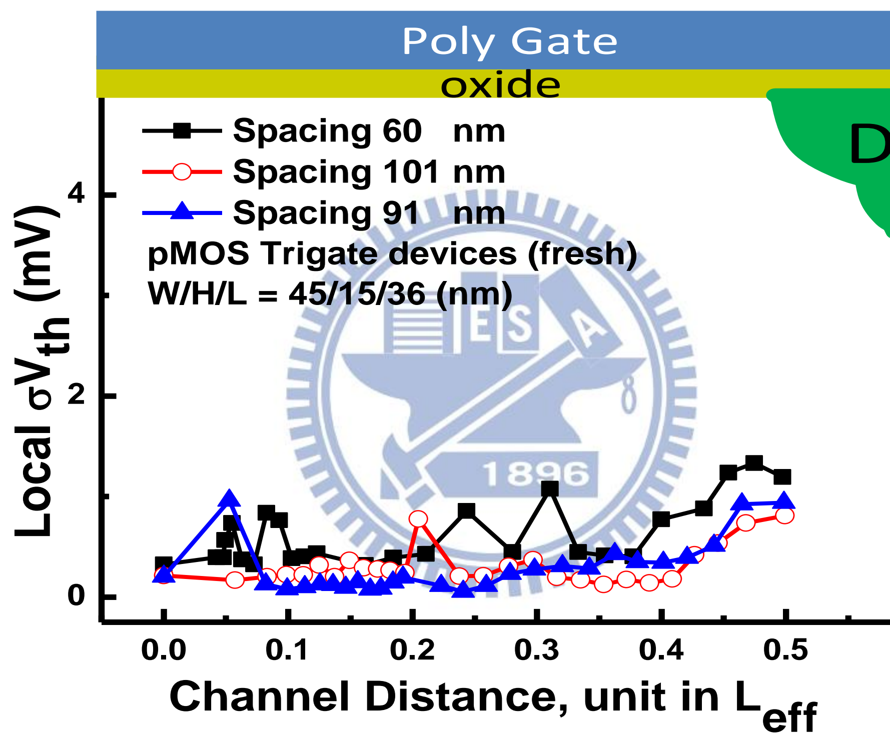


Fig. 4.17 Different fin spacing affects the variation of fresh devices.

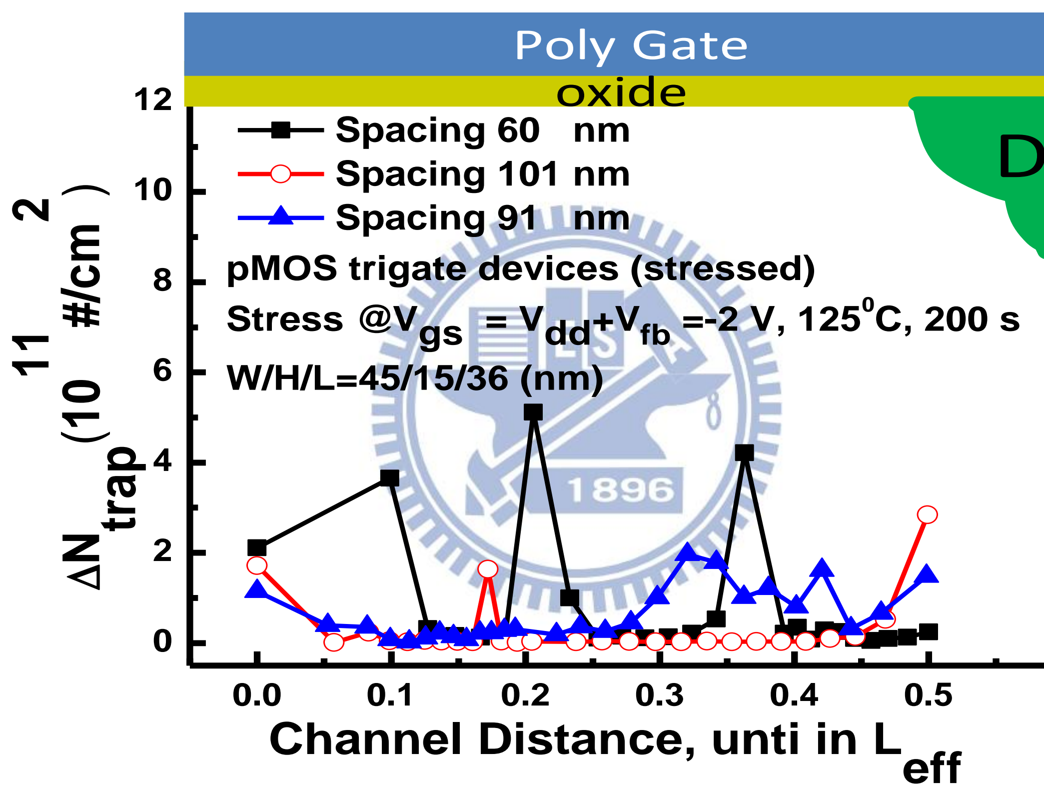


Fig. 4.18 To study the Fin spacing effect on the degradation of stressed trigate devices, three different spacing devices were measured.

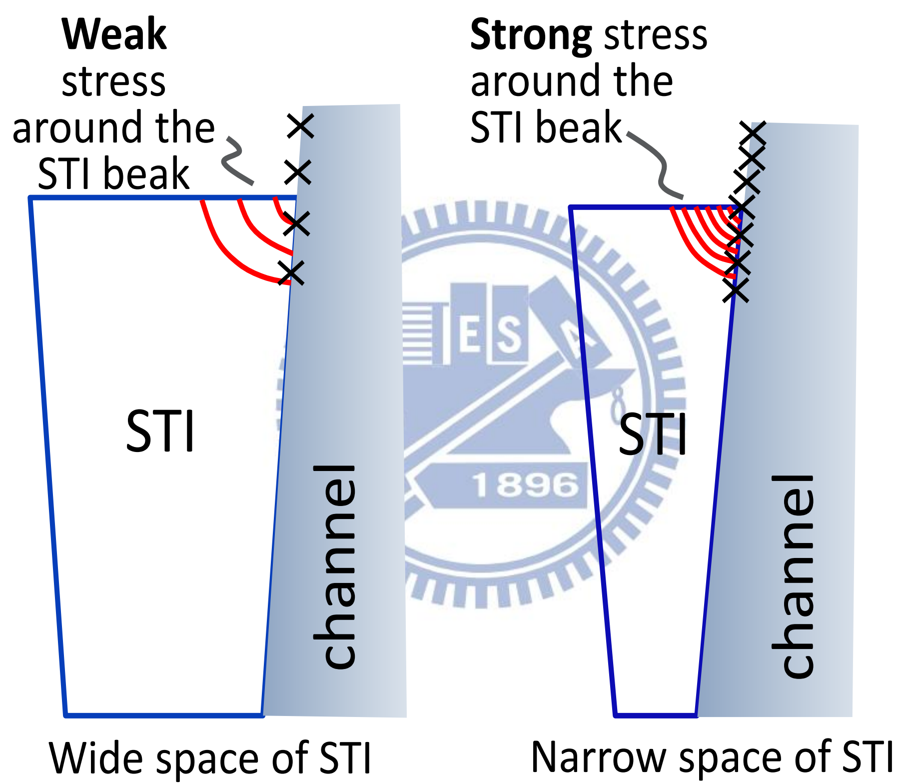


Fig. 4.19 Illustration of the STI spacing induced the sharper corner, such that higher electric field at the corner was induced.

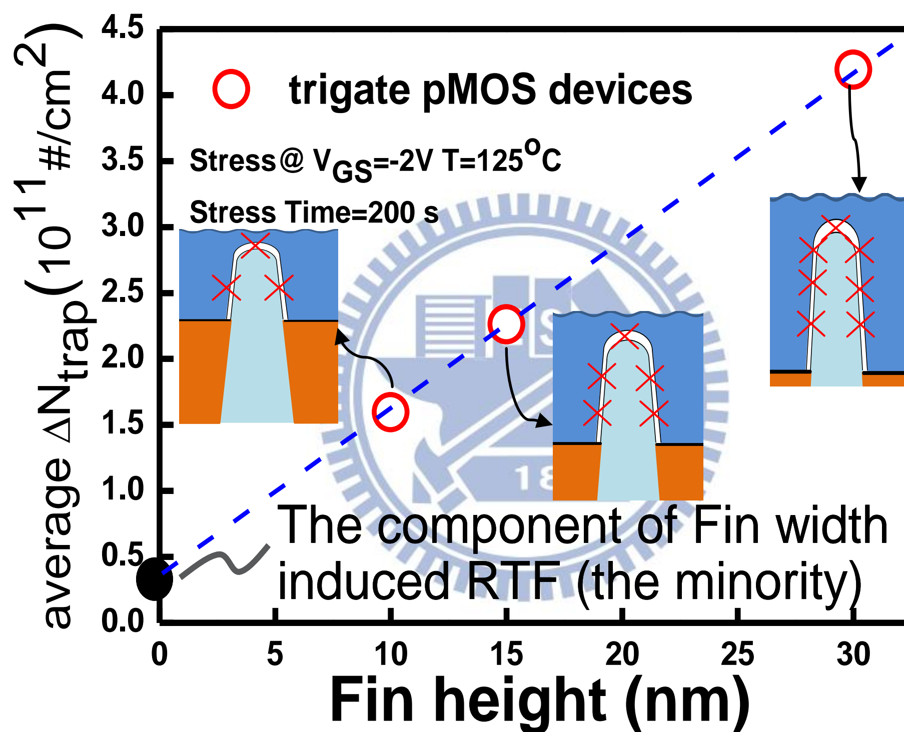


Fig. 4.20 Interface state density of Fin structure was measured by fabricating trigate devices with RTP method, from Fin height dependency, ΔNtrap of 3.1×10^{10} ($\#/cm^2$) for top surface were extracted.

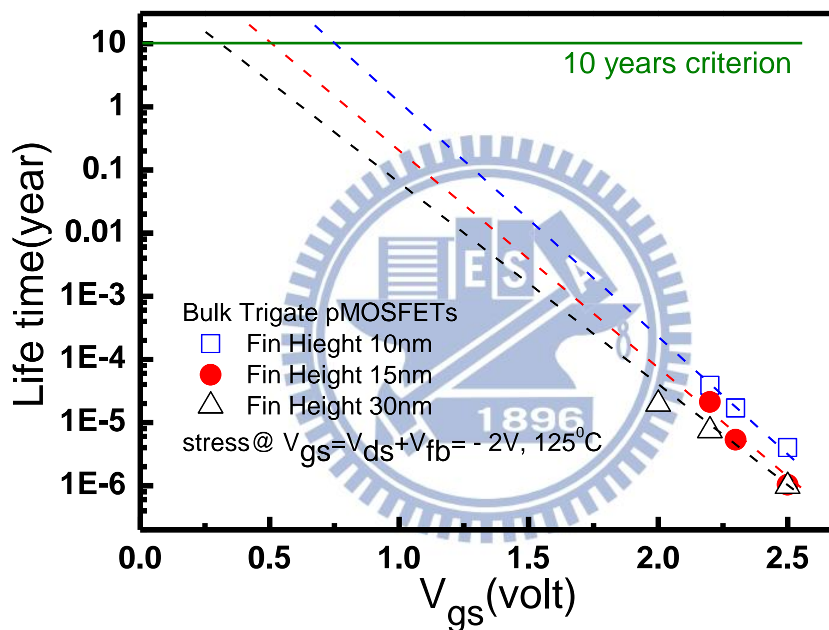


Fig. 4.21 10-year lifetime predictions of trigate pMOS devices after the NBTI stress, showing the higher fin device shows poorer lifetime.

The average trap density@ Stress Time = 200 s	Average increased trap density (cm^{-2})		
	Channel middle	Drain Edge	Channel middle / Drain Edge(%)
E = 5.7 MV/cm (V_{GS}=V_{DS}=1.7V)	$1.62x10^{11}$	$3.53x10^{11}$	46%
E = 8.2 MV/cm (V_{GS}=V_{DS}=2.2V)	$3.13x10^{11}$	$1.05x10^{11}$	30%

Table 4.1 The comparison of the generated trap densities for middle of channel and near drain edge after HC stress, showing that the damages near drain edge dominates the reliability of trigate devices in high electric field.

The average trap density@ Stress Time = 200 s	Average increased trap density (cm^{-2})		
	Fin Height 10 nm	Fin Height 15 nm	Fin Height 30 nm
trigate devices	$1.6x10^{11}$	$2.3x10^{11}$	$4.2x10^{11}$

Table 4.2 The comparison of the generated trap densities for different Fin height devices after NBTI stress, showing that Fin height dominates the reliability of trigate devices due to the surface roughness.

Chapter 5
Summary and Conclusion

In order to find the positions of oxide traps in the channel under the stress experimentally, the random trap profiling technique (RTP) has been proposed to characterize the distributions of random trap densities in the channel of a small dimensional bulk-trigate device. Trigate devices show better RDF variability but poorer reliability than the conventional planar devices. The HC stress and NBTI stress have been also conducted to study the mechanisms of random-traps-fluctuation (RTF) which induced the V_{th} aggravation for both trigate nMOS and pMOS devices. We conclude that NBTI stress dominates the degradation of trigate pMOS devices due to the surface roughness on the sidewall with reference to the HC stress on trigate nMOS devices. However, by taking good care of the sidewall process, the reliability of trigate devices might be improved. These results provide us a direction on a good control of the reliability for future 3D trigate devices.

Moreover, the variability of different Fin-height trigate devices with high and low series resistances are investigated in this thesis. Several salient features can be drawn: (1) For HC stress with low electric-field, since the corner effect plays a more important role in the degradation of trigate devices, an alternative approach is provided to alleviate the corner effect by increasing the S/D resistance of trigate devices to achieve an acceptable reliability. (2) For nMOS devices, devices with shorter fin-height shows more serious V_{th} degradation after the HC stress than those with taller ones; on the contrary, for pMOS devices, devices with taller fin-height exhibit more serious V_{th} degradation after NBTI stress than those with shorter ones. (3) We have found that the major source of reliability degradation for pMOS devices after NBTI stress is the sidewall roughness of fin-height not the surface roughness of

the fin-width.

These results provide us a good understanding of the random traps fluctuation (RTF) of trigate devices and a guideline to achieve a high performance and good reliability of bulk trigate CMOS devices beyond 28nm generation.

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