國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

運用隨機電報訊號方法分析

三閘極電晶體的多層級氧化層陷阱

The Multi-trap Analysis of Trigate MOSFETs Using the Random Telegraph Noise Measurement

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中華民國 一O一 年 十一 月

二氧化鉿電阻式記憶體多位元操作之隨機電報雜訊分析

The Random Telegraph Noise (RTN) Analysis of Multi-Level Operation Methods in HfO_2-based Resistive Random Access Memory

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摘要

隨著互補式金氧半電晶體(CMOS)的微縮，隨機電報訊號對元件產生劇烈的汲極電流波動所造成的影響是極為重要的可靠度議題之一。 隨機電報訊號的產生是由於單一載子從基板穿隧至閘極氧化層而被捕捉的物理現象。在本篇論文中，我們可以觀察此種缺陷的物理特性，且利用改良的萃取方法去準確得知缺陷的能階以及深度。

隨著超大型積體電路微縮至22奈米，漏電問題以及大幅的變異(variation)擾動問題，使得傳統的平面電晶體將不敷未來微縮用途，因此，在1999年所提出的三閘極電晶體(trigate) 結構在近幾年受到進一步的重視。然而在這樣的新型結構中依然存在著許多問題尚待解決，根據我們的觀察隨機電報訊號就是其中一項導致變異的重要來源。本文中，我們發表的一種簡單的實驗方法來萃取隨機電報訊號缺陷在互補式金氧半電晶體通道方向和氧化層中深度的分佈位置。為了研究隨機電報訊號對三閘極電晶體的影響，我們採用平面電晶體來和三閘極電晶體做比較。由實驗結果得知，在製流中產生的隨機電報雜訊缺陷在不同結構的元件中分佈特性並不相同，亦即在三閘極電晶體中缺陷分佈位置較靠近多晶矽閘極，而在平面電晶體中缺陷位置卻較為靠近基板。此外我們發現造成多層級隨機電報訊號的原因，這是由於氧化層中兩個缺陷的位置過於接近，以至於缺陷能帶的分佈互相重疊所導致。

根據上述單一元件中多層級隨機電報雜訊的研究，我們將它運用於對於靜態隨機記憶體(SRAM, Static Random Access Memory)的影響。利用隨機電報雜訊造成門檻電壓的擾動原理，我們可以成功的解釋靜態隨機儲存器在蝴蝶圖轉換的過程中發生錯誤的機制。此外，我們由蝴蝶圖中萃取出讀取靜態雜訊邊際，並比較隨機電報訊號的產生對讀取靜態雜訊邊際的影響，在此情況下此我們觀察到隨機電報訊號將會造成讀取靜態雜訊邊際擾動，擾動範圍可由2mV至23mV。在量測中我們明顯發現蝴蝶圖受到隨機電報訊號的影響而分裂，分裂開來的層級數正好相當於多層級隨機電報訊號的層級數。此一現象將是未來使用三閘極電晶體來設計SRAM時，必需謹慎考量的一項重要微縮因素。

The Multi-trap Analysis of Trigate MOSFETs Using the Random Telegraph Noise Measurement

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Abstract

As CMOS devices are continuously scaled, the influence of Random Telegraph Noise (RTN) in CMOS devices is one of the most important reliability issues. The RTN phenomena are resulted from the single carrier trapped and de-trapped between the channel and the trap in the gate dielectrics. In this thesis, we have observed the physical properties of single trapped carriers through a novel RTN profiling technique. This technique enables the extraction of the lateral location and vertical depth of a single trap or multiple traps in an advanced trigate nMOSFET device.

As VLSI technology scaled toward 22nm node, the short channel effect and variability are intolerant in the planar architecture. So, even FINFET structure has been proposed since 1999 which received much more attention more recently. However, there are several problems which need to be solved in such a device. According to our observation, RTN is one of the most important variation sources. In this thesis we develop a simple experiment method to extract the two dimensional distribution of RTN traps. To study the influence on trigate MOSFETs, we compare

trigate devices with conventional planar devices. From the profiling results, we have found that the process-induced RTN traps are generated near poly gate in trigate devices but generated near the channel of the planar devices. In addition, we have found the origins of multi-level RTN generation, which came from the cross-section of overlap traps.

Based on the results of our research of RTN at the device-level, we further investigate the impact of multiple RTN on SRAM and find a newly RTN-induced failure mechanism of SRAM successfully. Besides, we extract the RSNM from butterfly curves. Comparing the RSNM (read static noise margin) of the cell with RTN and without RTN respectively, the RSNM has been degraded from 2mV to 23mV in this work because of multi-RTN. From the measurement, butterfly curves are split into multiple levels, which is corresponding to the multiple levels of RTN in a pull-down or pull-up device directly. These phenomena are first reported and will be significant for consideration in the future design of trigate SRAM.

致　　謝

兩年的研究生生涯一轉眼就過去了，還記得剛考上研究所，來到人生地不熟的新竹，面對課業上新的挑戰，心中滿是不安，因此我要特別感謝在這兩年之中，不論是研究上、課業上、生活上給予我幫助的每一個人。首先要向我的指導教授莊紹勳老師表達深摯的謝意。老師在課業和研究中給予我們寶貴的指導與建議，讓我在學業與研究上獲益良多，更讓我們學習到對事物應有的嚴謹態度。

此外我要感謝實驗室所有一起努力的學長和夥伴，感謝周承翰、謝易叡學長，在我對實驗一無所知的時候是你們將那寶貴的知識傳承了下來，謝易叡學長謝謝你耐心地帶領我做實驗，讓我能快速地進入狀況，以及一起努力的同學蔡漢旻、黃英傑、蔡政達、謝泓達、房定樺，和你們一起討論，讓我在遇到瓶頸的時候能夠有新的靈感，遇到挫折的時候有堅持下去的力量，有你們的陪伴讓黯淡的實驗室更加添了一抹色彩，另外還有汪大暉老師實驗室的學長們，邱榮標、鍾岳庭、周佑亮學長，感謝你們在我實驗遭遇困難而停擺的時候，向你們請教時不吝給我意見，真的助益量多。最後還有實驗室的學弟，伍邦齊、林尚墩、陳敬翰、王漢樽、林宗慶，衷心的期盼你們

在將來的日子裡都能夠互相扶持，在困境中彼此幫忙，也預祝你們學業、實驗盡都順利，也祝你們都能如期畢業。

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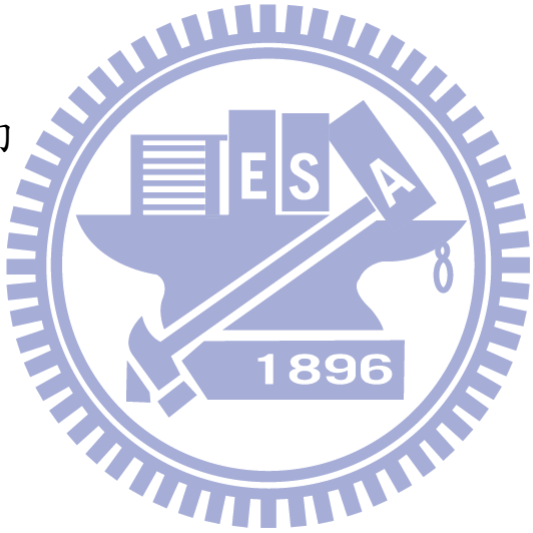
2012 年 11 月下旬



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Chapter 1

Introduction

1.1 Background

Silicon CMOS has been the main stream IC fabrication technology for three decades. In the last few years, the industry has witnessed a striking progress in downsizing the planar CMOS. Despite many fabrication challenges, 15nm physical gate length bulk MOSFETs have been demonstrated. However, scaling planar CMOS to 10nm-and-below would be exceptionally difficult, if not completely impossible, due to electrostatics, excessive leakages, mobility degradation, and many realistic fabrication issues. Particularly, the control of leakage (hence power) in a nanoscale transistor would be critical to high-performance chips such as microprocessors. Non-planar MOSFETs provide potential advantages in packing density, carrier transport, and device scalability. FinFET structure MOSFETs have been researched for a decade [1.1], they were not seriously considered by the industry due to their complicated fabrication process. These structures have regained attentions in deep-sub-100nm CMOS due to many scaling limits associated with the planar CMOS.

FinFET devices are suitable in sub-32 nm technology owing to their superior short channel control, steep subthreshold swing, and immunity to Random Dopant Fluctuation

(RDF) [1.2] with lightly-doped or undoped silicon fins. However, in extremely scaled devices, the impacts of RTN [1.3-1.4] resulting from trapping/detrapping of a single carrier charge in defect state at the interface have become serious concerns in deca-nanometer MOSFETs. Furthermore, the RTN amplitude exhibits long-tailed distribution and inverse area dependency. Thus, RTN has created a serious variation source in BULK MOSFETs as well as thin silicon film based multi-gate devices. In this work, we evaluate the effect of multi-charged trap induced RTN on the analog properties of FinFET and Bulk-planar devices by 2-D profiling method.

On the other hand, the soft error susceptibility of SRAMs has significantly increased in the nanometer regime. In recent years, the variations of devices have induced circuit failed, and it is an important issue that should be solved immediately [1.5-1.7]. RTN is one of the most important variation issues, especially multiple RTN.

In this thesis, the generation mechanism of RTN traps has been found. Instead of charge pumping method [1.8], we proposed a new method to profile the distribution of multi-RTN traps, because the charge-pumping current may be too small to be reliably measured in small-size devices at a lower frequency required. Using the method we proposed in this thesis a newly RTN-induced failure mechanism of trigate SRAM was found, and it will be very valuable in the future reliability and technology of SRAM cell.

1.2 The Motivation of this Work

Recently, random telegraph noise has been regarded as a serious concern for CMOS device scaling. It is caused by the capture and emission of charge carriers in the gate oxide traps and results in severe I_d fluctuation as shown in Fig. 1.1 (a), and threshold voltage shift as shown in Fig. 1.1 (b). Due to its strong dependence on device dimension, it is predicted that RTN amplitude will grow with device scaling more rapidly than that the V_{th} variation caused by random dopant fluctuation. Therefore, new methods for measuring and modeling RTN are necessary to gain more understanding of the statistics of RTN as a function of bias and device size. Moreover, the impact of RTN on the reliability of circuit operation such as SRAM read/write stability is not negligible even for the 40 nm generation. Because the multi-level RTN will increase the switching amplitude, it is more likely to cause system failure [1.9] as shown in Fig. 1.2. However, due to the complex switching mechanisms of multi-level RTN, it is difficult to analyze this phenomenon. For the purpose of analyzing this phenomenon, we develop a simple and useful method which enables the multi-level RTN reduces to two-level RTN, as shown in Fig. 1.3. Additionally, stress-induced RTN [1.10] is another big issue in this study. In this work, we compare the traps distribution between planar devices and trigate devices as shown in Fig. 1.4 (a) and Fig. 1.4 (b). Besides, we compare the fresh devices and stressed devices. Finally, we are

interested in the impact of RTN on trigate SRAM. In order to enhance the SRAM operation speed, the larger supply voltage is used often. However, the larger supply voltage might cause the device stressed and induce the RTN signals. It will reduce the RSNM and even induce failure of the transition in butterfly curves.

1.3 Organization of the Thesis

In this thesis, we will focus on the device variation which is caused by RTN-traps, because RTN-traps induce threshold voltage shifted severely. To discuss the correlation between trap position and I_D variation, we develop a new method to profile traps distribution. Then we measured the SRAM circuits to analyze the impact of RTN traps on the circuits. Moreover, we use different stress methods to control the generated traps. Through the different stress method, the trap positions can be controlled successfully.

In Chapter 2, we introduce the profiling methods and the extracting method of the RTN-trap positions. Besides, we describe the basic properties of RTN, the process flow, and the operation principle. Afterwards, we introduce the CMOS devices used in our study.

In Chapter 3, we compare the bulk planar devices with the bulk trigate devices in both fresh condition and stressed condition to identify the effect of process-induced RTN traps and stress-induced RTN traps. In Chapter 4, we demonstrate the applications of the result

we reported in chapter 3. The applications include the influence of multi-level RTN on SRAM cell with the trigate devices and the planar devices by the manipulation of RTN-trap positions. Finally, the summary and conclusions are given in Chapter 5.

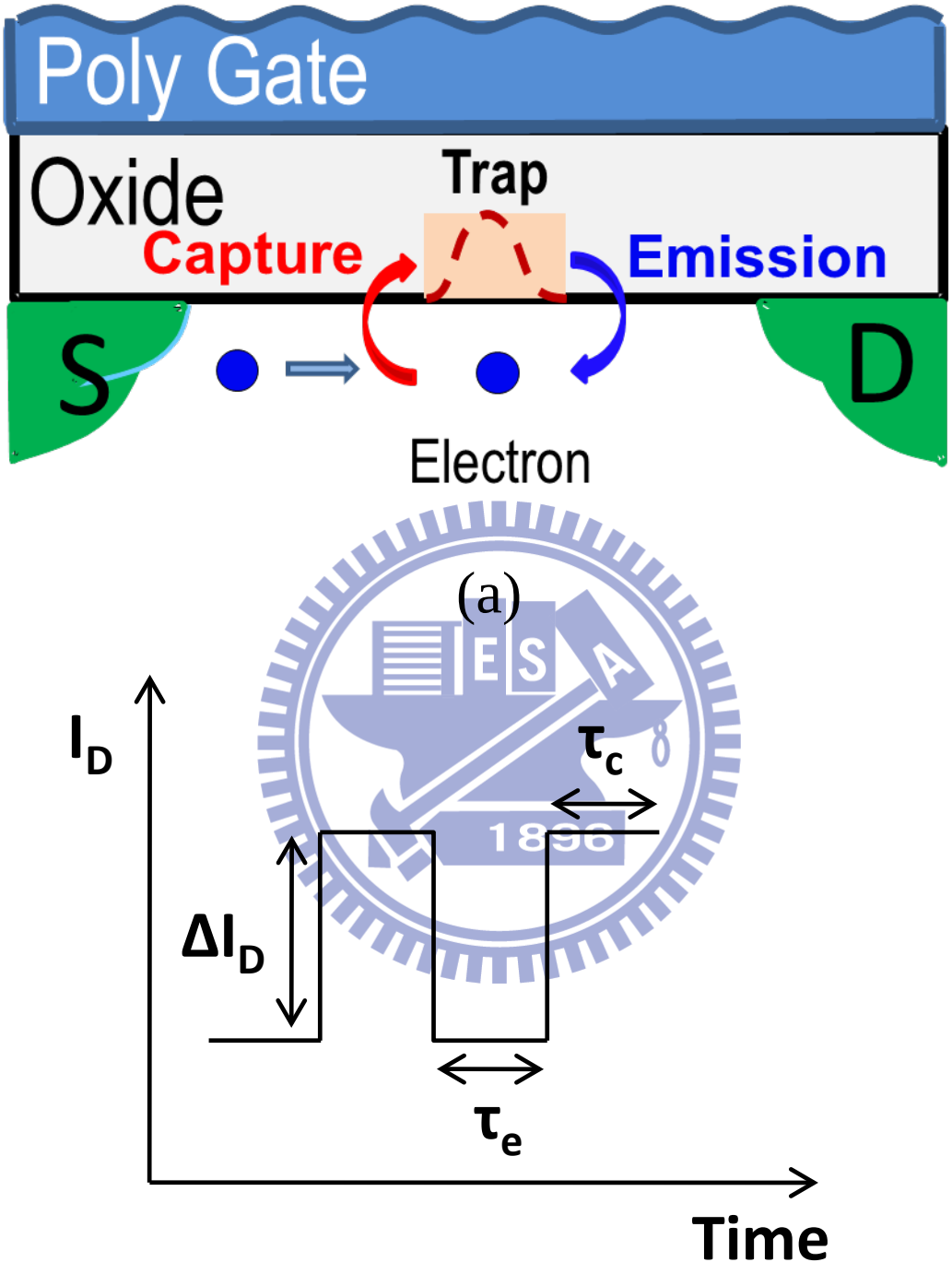


Fig. 1.1 (a) Carrier trapping and detrapping by the slow trap near the drain side. (b) Illustration of the three parameter of the RTN noise: capture time τ_c, emission time τ_e, and current amplitude ΔI_D.

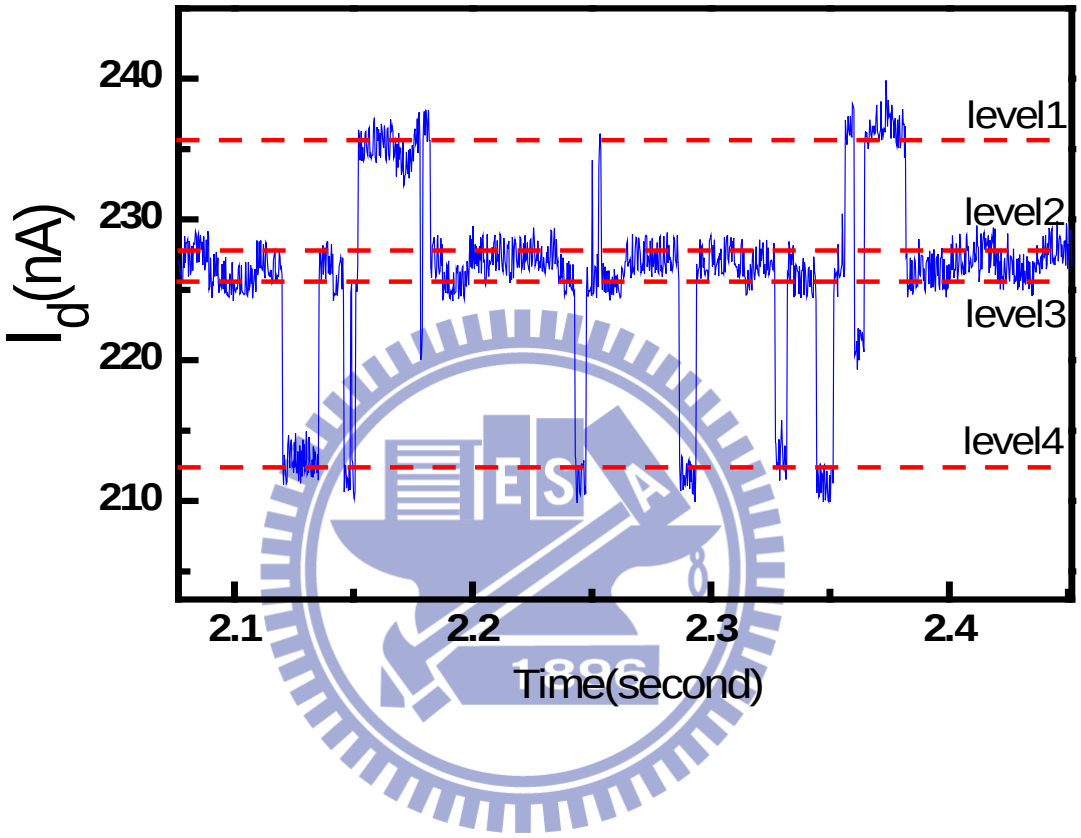


Fig. 1.2 The schematic diagram of Multi-level RTN.

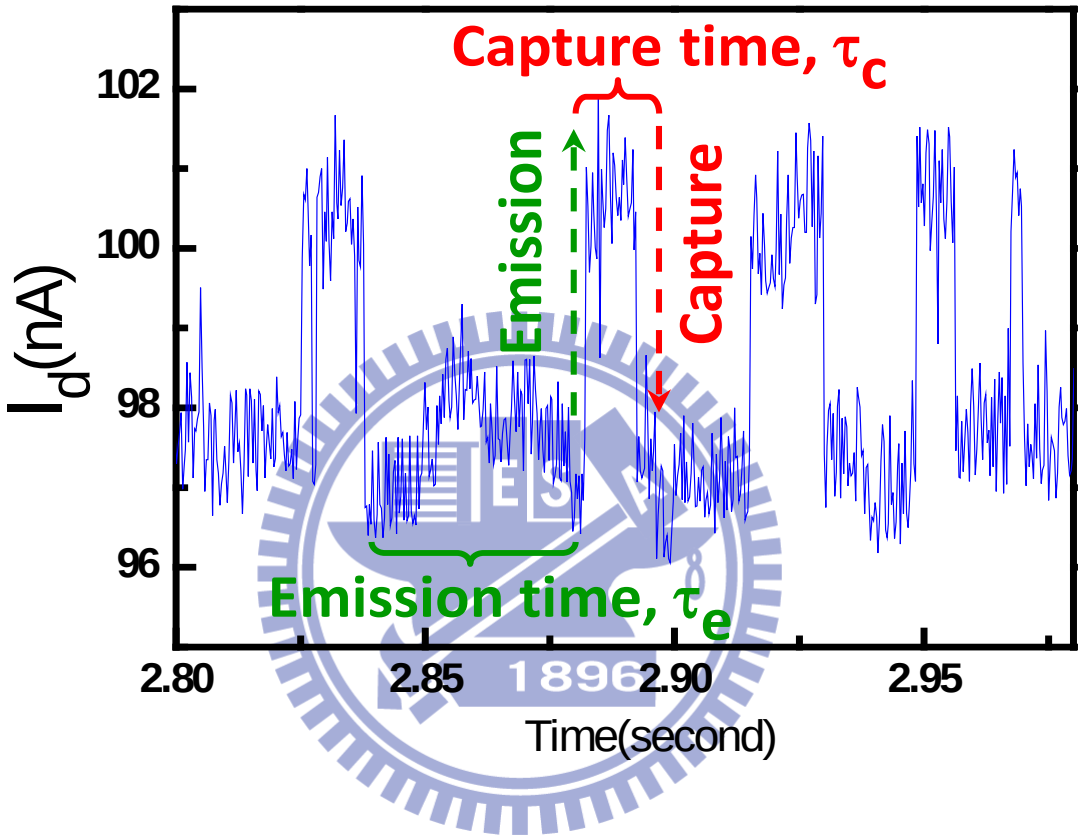
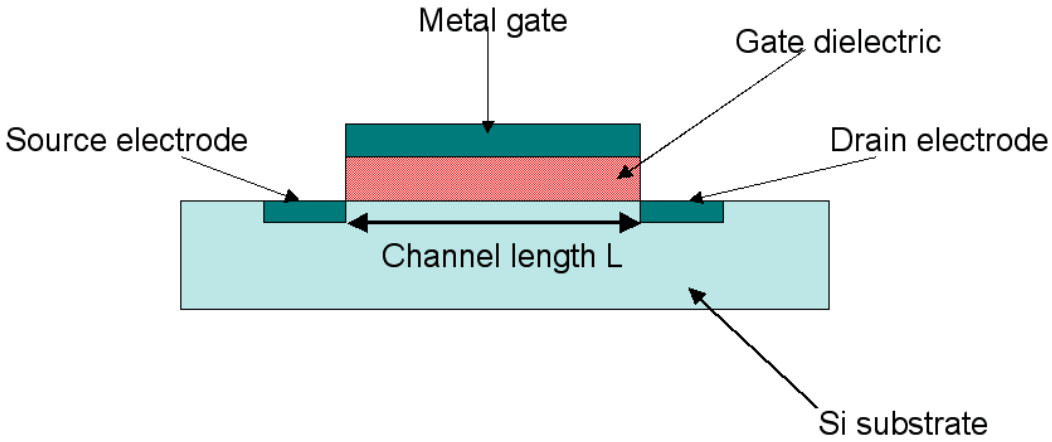
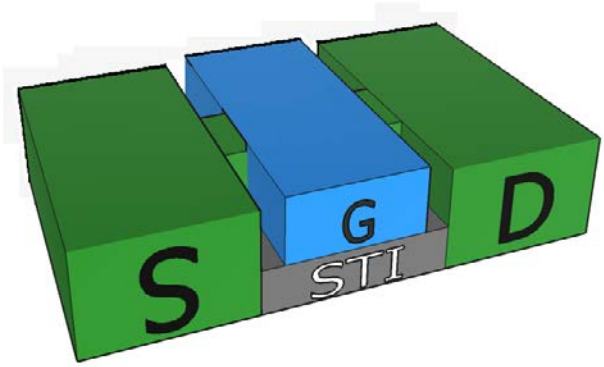


Fig. 1.3 A Two-level RTN schematic diagram.



(a)



(b)

Fig. 1.4 (a) Convention planar MOSFET. (b) Trigate structure MOSFET.

Chapter 2

Profiling Method- Theory and Experiment Setup

2.1 Introduction

Recently, random telegraph noise has been regarded as a serious concern for scaling of CMOS devices. Due to its strong dependence on device dimensions, it is predicted that RTN amplitude will grow with device scaling more rapidly than the V_{th} variation caused by random dopant fluctuation. RTN is believed to be originated from the traps at the Si/SiO_2 interface through the process of capture and emission of charge carriers in the channel, leading to switch current between two or multiple levels [2.1]. Based on the temperature and voltage dependence of single charge effect, an analytical model for tunneling mechanism is developed and traps parameters are extracted [2.2], including the trap depth and the trap energy.

Recently, the charge pumping measurements has been utilized to characterize trap properties. However, the charge-pumping current may be too small to be reliably measured in small-size devices at a lower frequency required. Besides, the charge-pumping current may contain gate leakage as devices are stressed or heavily destroyed even when wear out or soft breakdown happens. In this chapter, we demonstrate a new method of extracting the

trap positions with 2-D distribution in the oxide layer. This method includes the lateral profiling and the longitudinal profiling. To extract the trap depth, the mechanism of RTN should be understood. Because the trap depth is relate to time constant, capture time (τ_c) and the emission time (τ_e). Through the slope of $\ln(\tau_c/\tau_e)$ versus V_G, the trap depth could be extracted. Besides, we utilize the barrier peak in the channel direction to probe the trap position. RTN signals are the most sensitive at the barrier peak. By increasing source-to-drain voltage, V_{SD}, the barrier peak will be shifted from the middle of channel to the drain side, and the correct position can be extracted. Therefore, the position of RTN signals can be extracted in channel direction.

2.2 Profiling Method in Two Dimension

2.2.1 General Equation of the Trap Depth

Figure 2.1 (a) shows the schematic diagram of RTN (random telegraph noise) noise with drain current fluctuation. The probability of a transition from the high current state to the low current state is given by $1/\tau_e$. Similarly, the probability of a transition from the low current state to the high current state is $1/\tau_c$. E_T in thesis is the energy of the trap, and the E_F is Fermi energy for electrons. Based on the principle of detailed balance, the average emission time is given by [2.3]:

$$\frac{\bar{\tau}_c}{\bar{\tau}_e} = g \exp\left(\frac{E_T - E_F}{kT}\right). \qquad (2.1)$$

Here, k is the Boltzmann constant, T is the temperature, τ_c and τ_e are average capture time and emission time, respectively, and g is the degeneracy factor. Therefore, let g = 1;

$$\ln\frac{\bar{\tau}_c}{\bar{\tau}_e} = -\frac{1}{kT}[\left(E_{C,ox} - E_T\right) - \left(E_C - E_{Fn}\right) - \phi_0 + q\psi_s + q\frac{Z_T}{T_{ox}}(V_{gs} - V_{FB} - \psi_s - \psi_p)]. \qquad (2.2)$$

where E_{Cox} is the conduction band edge of the oxide, E_C is the conduction band edge of silicon, φ_o is the difference between the electron affinities of Si and SiO_2, V_{FB} is the flat-band voltage, φ_s is the amount of band-bending, Z_T is the position of the trap in the oxide measured with respect to Si-SiO_2 interface, T_{ox} is the oxide thickness, V_{GS} is the gate-source voltage, and q is electronic charge. The right-hand side of Eq. (2.2) represents the difference between trap energy level and electron's Fermi level. We can easily recognize the energy difference from Fig. 2.2.

By differentiating (2.2) with respect to V_{GS}, the position of the trap in the oxide Z_T can be obtained by the following equation:

$$z_T = -T_{ox}\frac{kT}{q}\frac{d(\ln(\bar{\tau}_c/\bar{\tau}_e))}{dV_{gs}} \quad . \qquad (2.3)$$

2.2.2 Lateral Profiling Method

Because the RTN signals are more sensitive to the peak of the channel potential barrier, and the barrier peak is dependent on the source-to-drain voltage; the trap position in the channel direction can be defined. Fig. 2.3 shows the barrier peaks fluctuated by oxide traps. The emission/capture charge on the local trap causes barrier peaks raised/suppressed directly, and the drain current would suffer from the barrier scattering seriously. By increasing source-to-drain voltage, the barrier peak will be shifted from the middle of the channel to the drain side. The relation between source-to-drain voltage and the position of barrier peak cane be derived as below:

$$\begin{cases} \dfrac{Y_{peak} - Y_0}{L_{eff} - \Delta L} = \dfrac{(V_{bi} - V_{c,\max}) - DIBL}{(V_{bi} - V_{c,\max})} & (2.4) \\ \dfrac{L_{eff} - \Delta L}{L_{eff}} = \dfrac{C_{dm}}{C_{dm,0}} = \dfrac{S.S. - 60mV}{S.S._0 - 60mV} . & (2.5) \end{cases}$$

where Y_{peak} is the position of barrier peak at given V_{DS}, Y_0 is the barrier peak at V_{DS} = 0.05V, L_{eff} is the effective channel length, ΔL is depletion region length at given V_{DS}; which used to adjust the channel length, $S.S._0$ is the subthreshold I_d swing at V_{DS} = 0.05V, S.S. is the subthreshold I_d swing at given $V_{DS,}$ V_{bi} is junction barrier between source and channel, $V_{c,max}$ is barrier heigh of long channel, as shown in Fig. 2.4.

To extract the trap position, we extract V_{bi} , $V_{c,max}$, and ΔL experimentally.

2.3 Device Preparation and Experimental Setup

2.3.1 Device preparation

The 28nm technology node of the bulk trigate CMOS devices with poly-Si gate made on a pilot foundry platform, with EOT(SiO_2)= 20Å were prepared as shown in Figs. 2.5. Also bulk-planar devices on the same technology node were made for comparisons as shown in Figs. 2.6.

2.3.2 Experimental Setup

The experimental setup for the current-voltage measurement of devices is illustrated in Fig. 2.7 and Fig. 2.9, respectively. Each of the analyzers is connected by the co-axial or tri-axial cable including the semiconductor parameter analyzer (HP 4156C) as shown in Fig. 2.7. In order to suppress the noise of transport, we connect the parameter analyzers directly without switch mainframe, while the RTN signal is measured, as shown in Fig. 2.8. The Cascade guarded thermal probe station, and a thermal controller. This facility provides an adequate capability for measuring the low leakage devices MOSFET characteristic. Therefore, our group developed a control system in HT-Basic language. Through

IEEE-488 (GPIB) cable, we can directly give the order to each analyzer. From the above system, the I-V and C-V characteristics of the MOSFET devices can be precisely performed.

While measuring the RTN signal, we set the interval time and the total measure points in the beginning. Then, to calculate both the high level state time and the low level state time of I_d, we can get the average τ_c and τ_e. In this experiment the gate voltage is biased at V_{th} versus different V_{DS}. Through the I_D-V_G curve the V_{th} can be extracted.

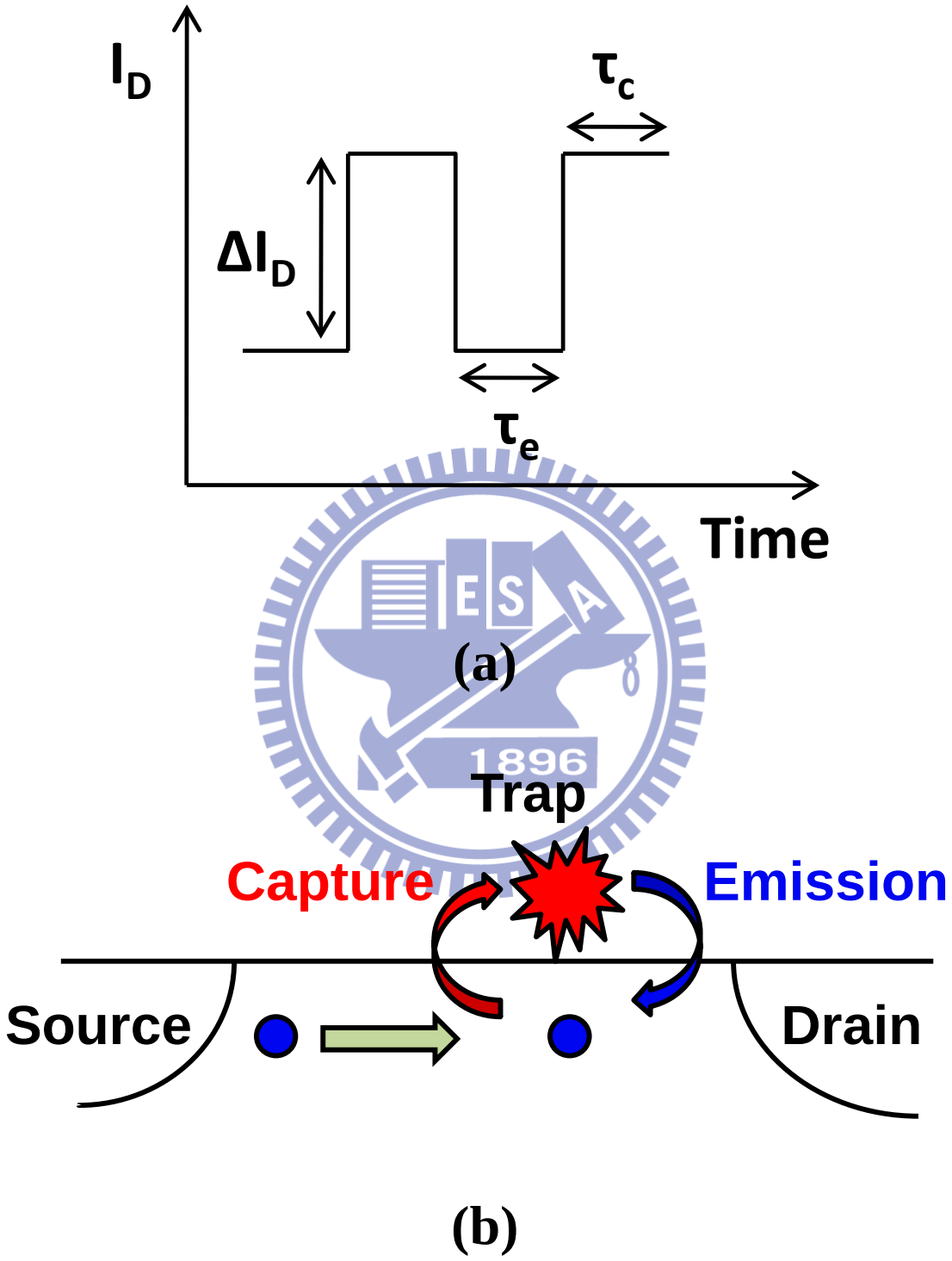


Fig. 2.1 (a) Illustration of the three parameter of the RTN noise: capture time τ_c, emission time τ_e, and current amplitude ΔI_D. (b) Carrier trapping and detrapping by the slow trap near the drain side.

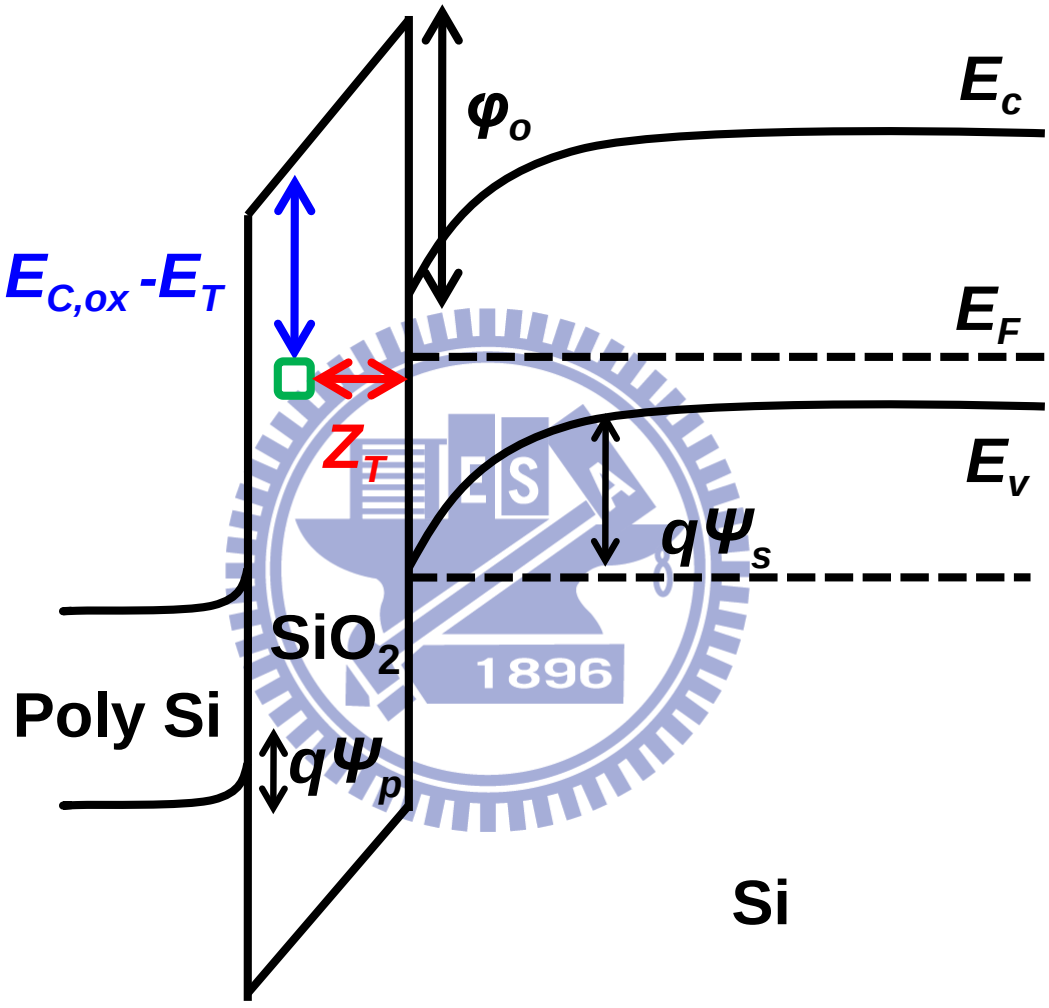


Fig. 2.2 The energy band diagram of the Si-SiO_2 interface in the channel at the trap location.

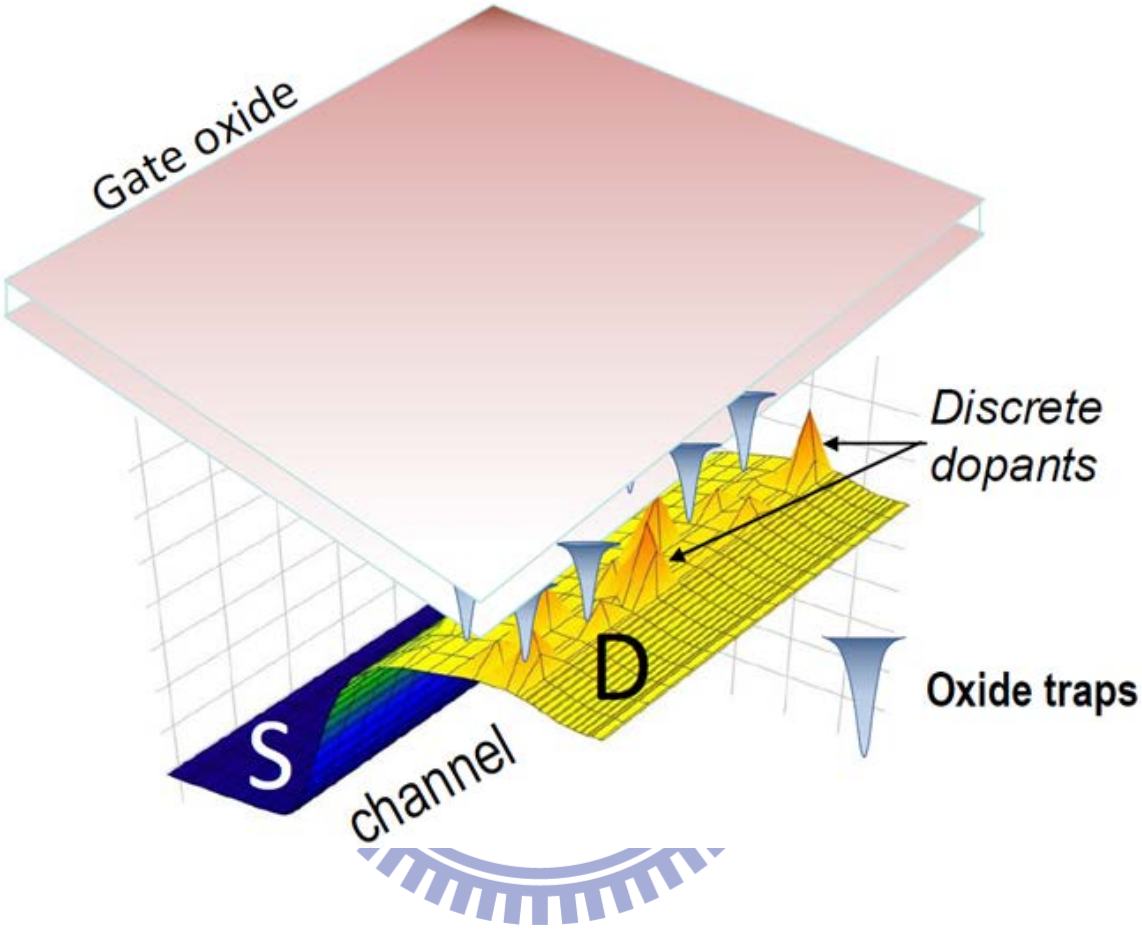


Fig. 2.3 Oxide trap RTN induce barrier peak fluctuate: V_{th} variation is dominated by the trapping or de-trapping in the oxide layer trap.

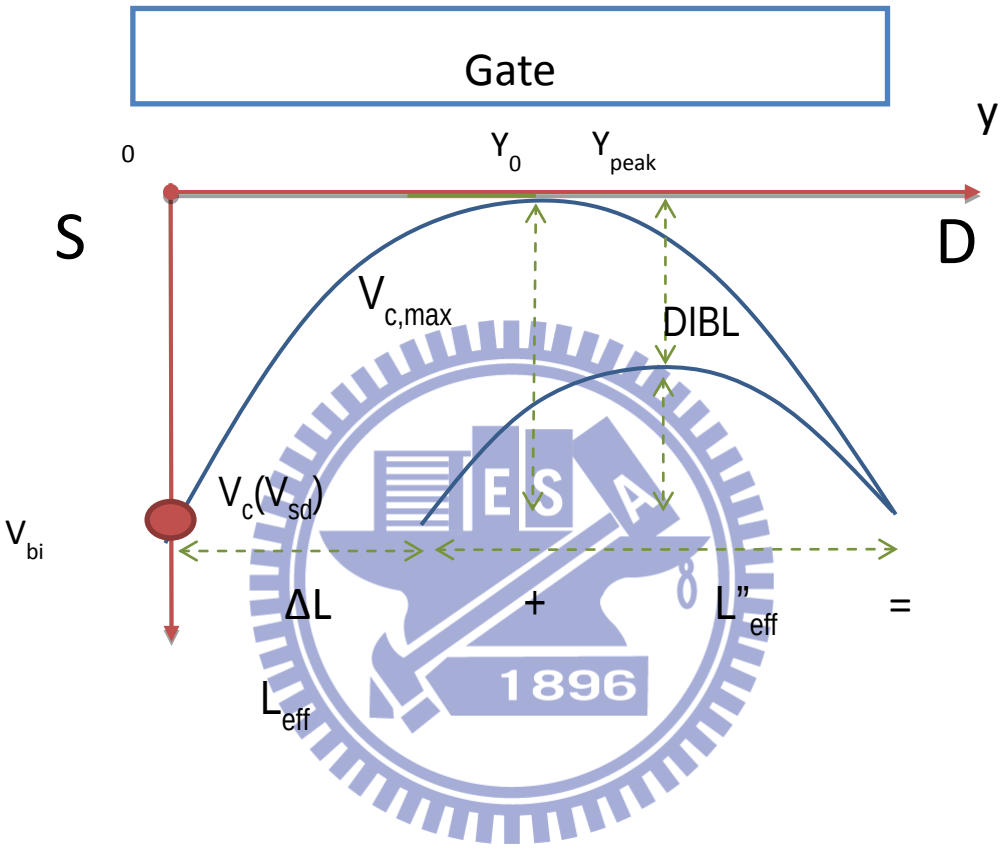


Fig. 2.4 A new model is to approximate the carrier peak in the channel as a second degree curve, in which the peak position can be determined by the DIBL.

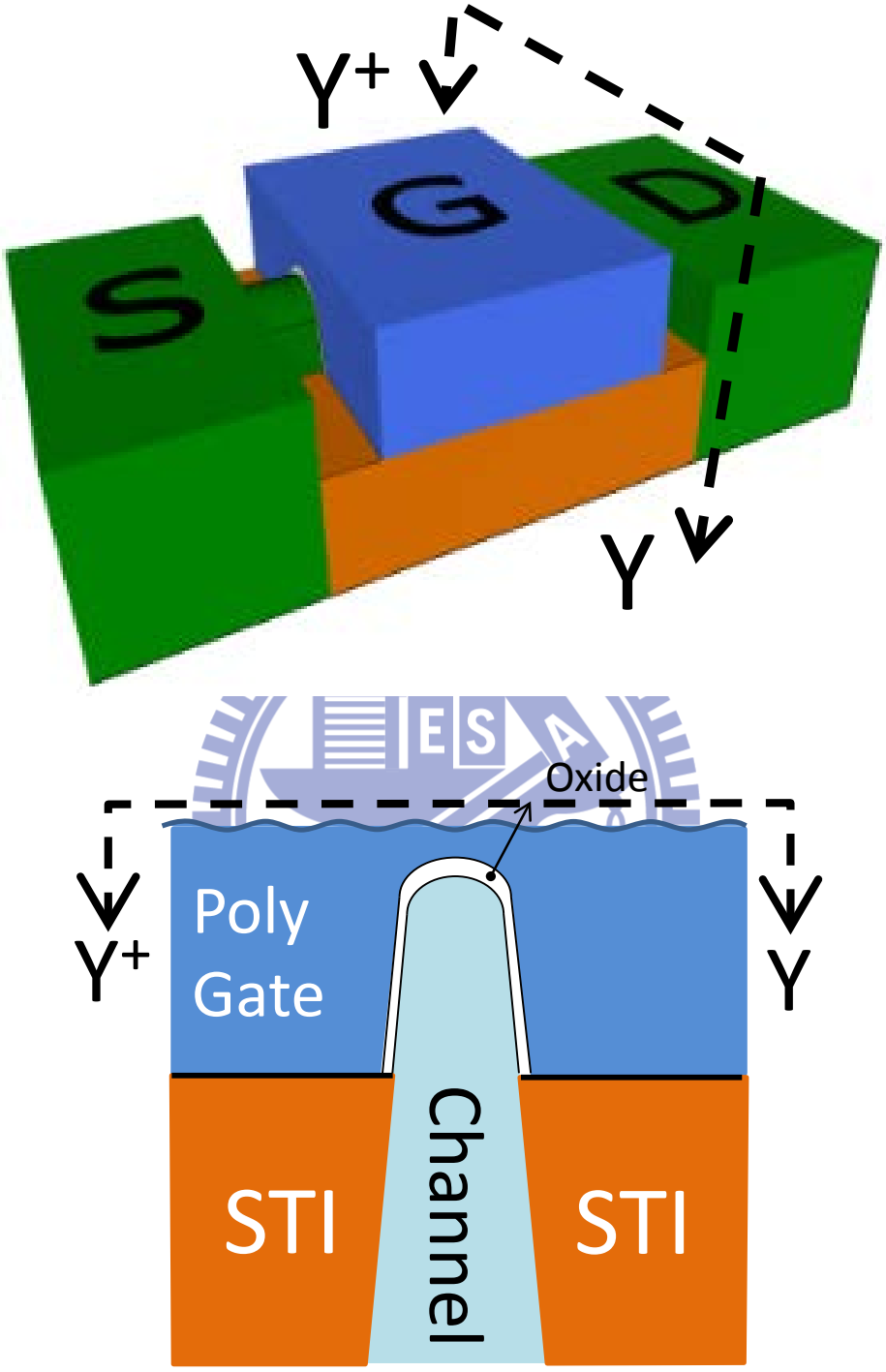


Fig. 2.5 (a) The 3D schematic of bulk trigate device used in this work. (b) The cross-section from Y to Y^+ of trigate device.

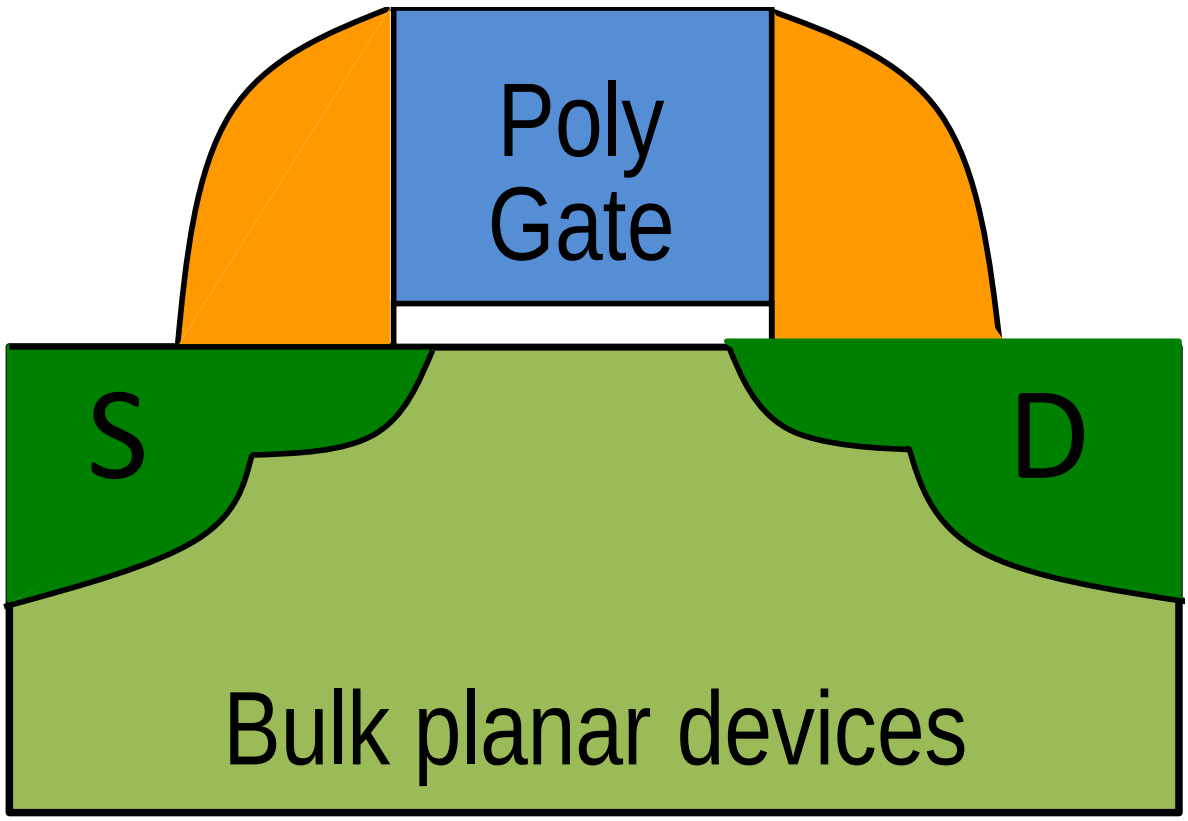


Fig. 2.6 The bulk planar MOSFET devices made for comparisons.

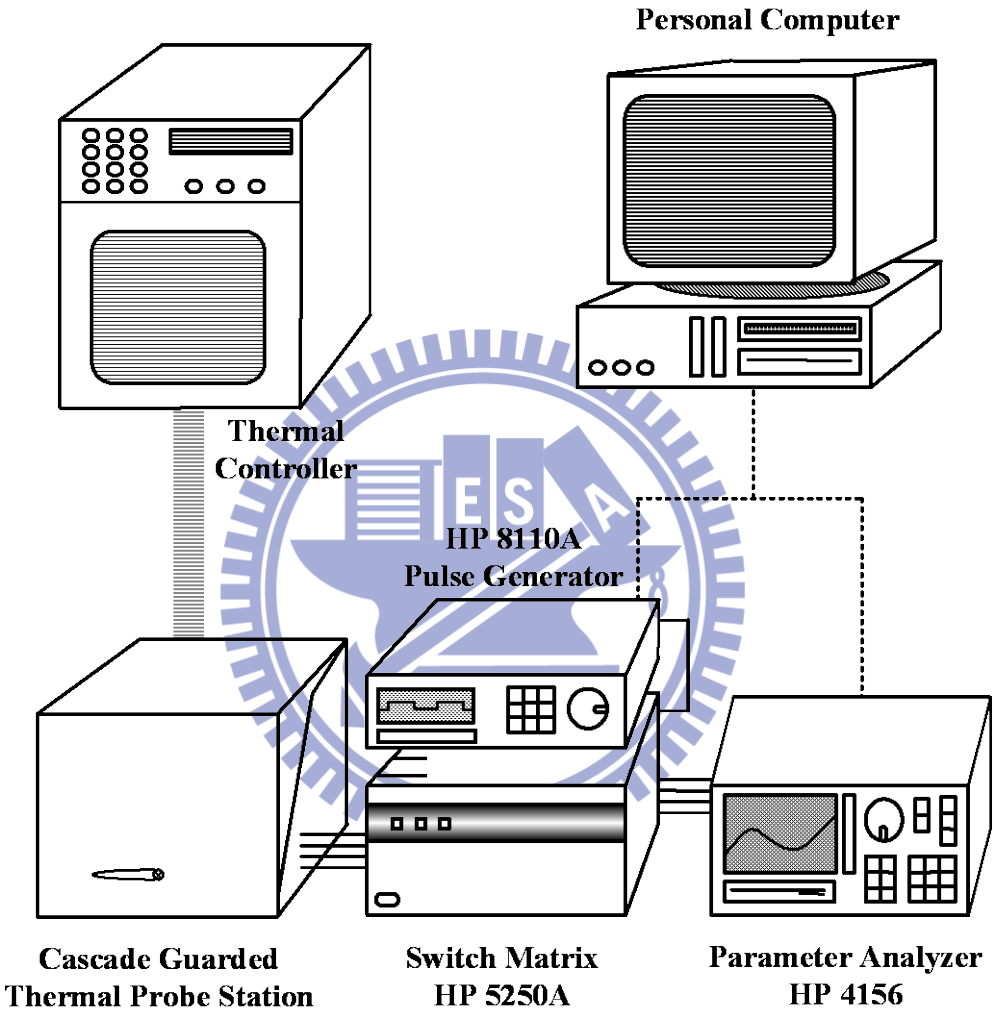


Fig. 2.7 The experimental system of current-voltage (I-V) for both n-type or p-type MOSFET.

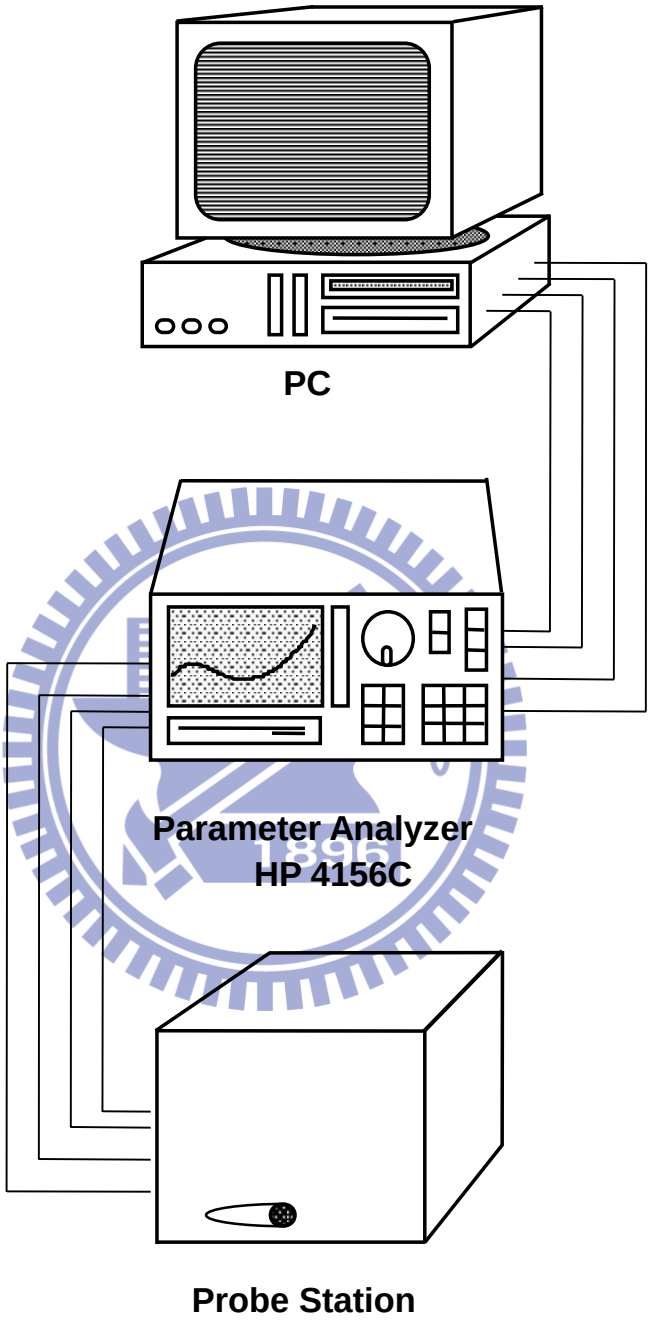


Fig. 2.8 The measurement setup using Analyzer HP 4156C to do the sampling of RTN signals.

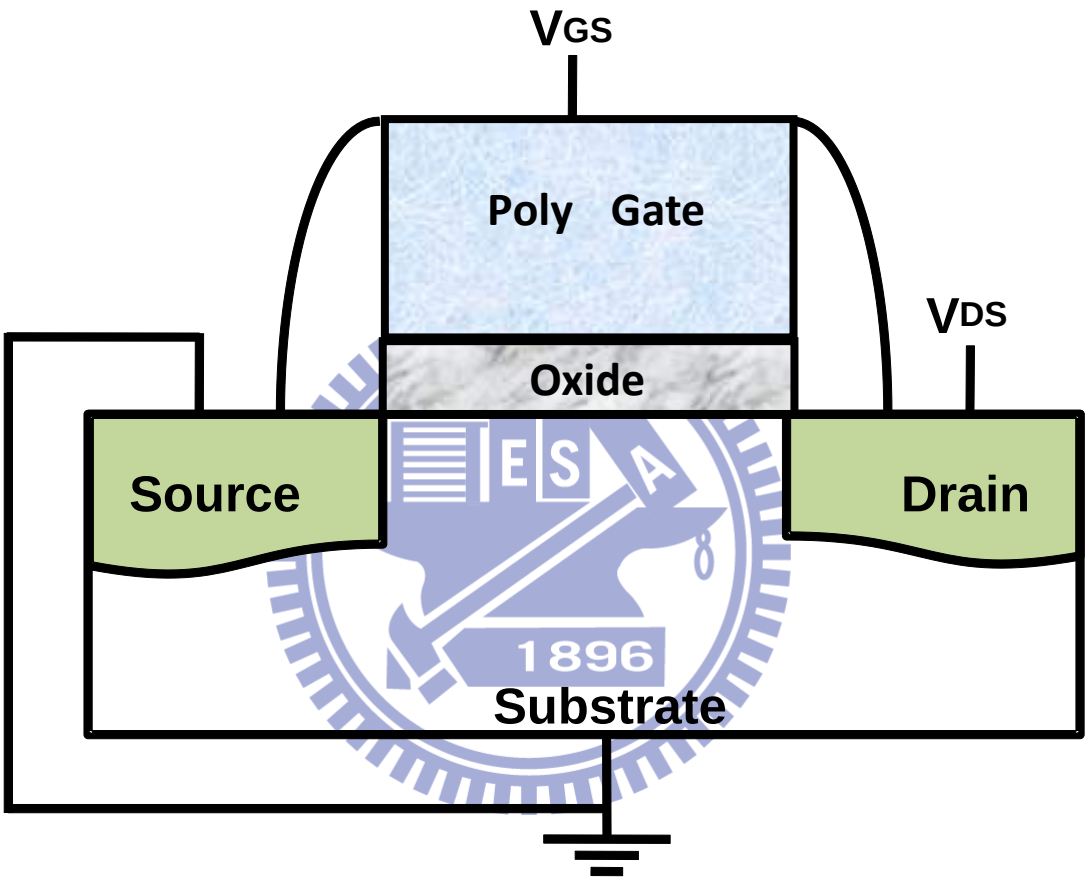


Fig. 2.9 The terminals setup for the sampling using HP4156C Analyzer.

Chapter 3

Influence of Multi-level RTN in Trigate MOSFET And the Distribution of Oxide Trap Through 2-D Profiling

3.1 Introduction

As Intel co-founder Gordon Moore’s bold prediction, popularly known as Moore's Law, states that the number of transistors on a chip will double approximately every two years. Electrical engineer which has maintained this pace for decades, this golden rule as both a guiding principle and a springboard for technological advancement, driving the expansion of functions on a chip at a lower cost per function and lower power per transistor by introducing and using new materials and transistor structures. As VLSI scales toward 22nm node, the leakage and variation are intolerant in the planar devices. Therefore, finFET structure had been proposed since 1999 and been mass produced recently. However, there are several problems not solved in FINFET device, and RTN is one of the most important variation sources.

In this chapter we dedicated to profile the distribution of RTN traps to explain the influence of trap positions. In order to understand the difference between the planar

devices and the trigate devices, we used two kinds of devices in this experiment separately. On the other hand, we took the devices under stressed condition and fresh condition while measurement, to understand the difference between processing induced RTN and stress induced RTN. Since finFET devices just began to be used on mass product recently, the device quality was not very stable. Devices with defect might induce circuit failed and power consumption. Through this study, we can realize the drawbacks of produce process and improve the procedure.

3.2 Experimental

3.2.1 Process Induce RTN Trap

Figure 3.1 shows the result of a RTN trap in the planar pMOS device. According to our experiment, the trap distribution is a Gaussian-like shape. To understand the reason of Gaussian-like distribution, we examine Eq. 3.1 and Eq. 3.2 below.

$$\frac{\bar{\tau}_c}{\bar{\tau}_e} = g \exp\left(\frac{E_T - E_F}{kT}\right), \tag{3.1}$$

$$Z_T = -T_{OX}\frac{K_B T}{q}\frac{d(\ln(\tau_c/\tau_e))}{dV_g}. \tag{3.2}$$

The depth of RTN traps can be extracted from Eq. 3.2, and the trap depth is related to

the trap energy, E_T. However, the trap energy is a distribution rather than a constant. The trap distribution is dependent on the channel position.

The difference between oxide trap energy level and Fermi level is changed by gate voltage and determines the ratio of capture time and emission time. Through physical methodology, we can find the relationship between time constants and trap energy and Fermi level with trap depth.

Fig. 3.2 is the result of RTN traps in the planar nMOS devices. The figure demonstrates that there are two traps in the planar nMOS device. From the profiling result, the different depths of two traps can be observed easily in this profiling method. We also observed that the two traps interact in the middle of them. To discuss the profiling result, we can examine the $\Delta I_D / I_D$ curve as shown in Fig. 3.3. Depending on the trap location, 3 cases of RTN signal can be observed in the $\Delta I_D / I_D$ curve, from which the case 1 and the case 3 are two-level signals, but the case 2 is four-levels in the interaction region because the barrier peak is affected by the two overlapping traps.

Figure 3.4 shows the profile of single RTN trap in a trigate pMOS device, and Fig. 3.5 shows the profile of a bulk-trigate nMOS device. By comparing the trap profiling results of bulk-trigate devices with the planar devices, the broader distributions can be observed in both nMOS devices and pMOS trigate devices. From the result, we make an assumption that the deeper RTN trap might induce boarder distribution. Fig. 3.4 shows the single trap

profile, and Fig. 3.5 shows the profile of two RTN traps without overlapping. Comparing Fig. 3.2 and Fig. 3.5, we realize that if the two traps separate far enough, the signals are always two-levels. Because both traps are not overlapped, no 4-level RTN is observed. On the other hand, if the two traps are so close that the trap energy overlapped thus it will induce four-level RTN signals in the overlapped region.

By differentiating equation 3.1 with V_{GS}, the position of the trap in the oxide is conventionally obtained. Fig. 3.6 shows positive dependency of $\ln(\tau_c/\tau_e)$ on V_{GS} for planar devices and negative dependency for trigate devices. The RTN-traps in the trigate devices tend to exchange with gate, but the RTN-traps in the planar devices tend to exchange with channel. Because the trap depths in the trigate devices are deeper than that in the planar devices as shown in Fig. 3.7. As a result, Fig.13 outlines the information of process induced RTN traps.

We also got the cross-sections of RTN traps by examining the profiling result. Fig. 3.9 compares the cross-sections of RTN traps with reported data [3.1], [3.2], and theory value, showing good consistency.

3.2.2 Stress Induce RTN Trap

Since SRAM is highly vulnerable to mismatch, and the devices might be stressed while operating; to understand the stressed devices impact on circuits is important. To understand the behavior of post-stressed SRAM, we utilize different stress mechanisms, hot carrier (HC) stress and NBTI stress for the nMOS devices and the pMOS devices respectively. HC means carriers gain enough energy to enter the conduction band. We used drain avalanche to get the hot carrier. This occurs when a high drain voltage is applied under non-saturated conditions, and results in the very high electric fields near the drain, which accelerates channel carriers into the drain's depletion region. Studies have shown that the worst effects occur when $V_D = 2V_G$. Instead of HC stress, we utilize NBTI stress for pMOS devices. In the sub-micrometer devices nitrogen is incorporated into the silicon gate oxide to reduce the gate leakage current density and prevent the boron penetration. However, incorporating nitrogen enhances NBTI. It is possible that the interfacial layer composed of nitride silicon dioxide is responsible for those instabilities. This interfacial layer results from the spontaneous oxidation of the silicon substrate. To limit this oxidation, the silicon interface is saturated with nitrogen resulting in a very thin and nitride oxide layer. In the case of NBTI, it is believed that the electric field is able to break Si-H bonds located at the Silicon-oxide interface. H is released in the substrate where it migrates. The remaining

dangling-bond contributes to the threshold voltage degradation.

Figure 3.10 shows the result of HC-induced two traps in the planar nMOS devices. As people know, the carrier energy is usually raised on the high field region. The depletion region is the region of the highest electric field. Therefore, HC-induced traps tend to cluster in near drain region closely. From our research before, we got a conclusion that different RTN traps might interact with each other, if the energy band overlaps. Therefore, the profile of RTN traps after HC stressed is three regions separately, including the left-trap region, the right-trap region, and the overlapped region. Because these two RTN signals are quite different, it is beneficial to analyze. Otherwise, the RTN signal would become mess and hard to be analyzed. Fig. 3.11 shows the I_D RTN signals of these separate regions. In the overlap region, the I_D RTN signal is raised to a 4-level RTN obviously.

Figure 3.12 shows the result of NBTI-induced RTN traps in the planar pMOS devices. The RTN traps tend to be generated in the middle of channel, because NBTI-stress bias on V_G=-2V only, and without V_D bias.

After the experiment upon, the stress condition the trigate devices we used on is similar to that we used on the planar devices. Fig. 3.13 shows HC stress in trigate nMOS devices. The similar trap distribution can be observed on Fig. 3.11 and Fig. 3.13. Although the bulk-trigate structure and the bulk-planar structure are different, HC-induced RTN traps are usually generated in the vicinity of drain region. It is because the contribution of the

highest field is there. Likewise, we use NBTI stress in the trigate pMOS devices. Fig. 3.14 shows the profiling result of NBTI-induced RTN traps, and the two fully-overlapped traps are observed. It is because these two traps located in the same position in channel direction, but the vertical positions are different. Besides, we find that these two traps exclude each other to induce three-level RTN. Fig. 3.15 (a) shows the schematic, these two traps are barely aligned together. When one trap is occupied, it will repulse the other to capture the carrier as shown in Fig. 3.15 (a) & (b).

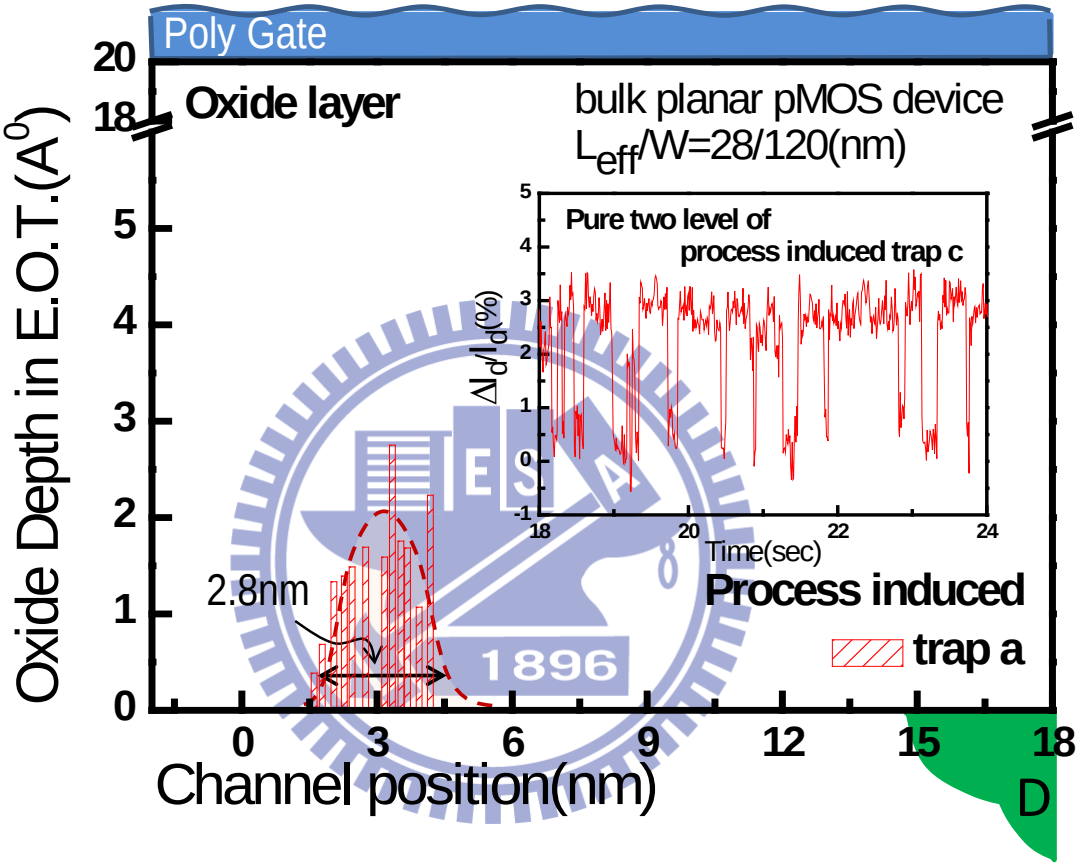


Fig. 3.1 The profiling result of the process-induced single RTN in the bulk planar pMOS devices, showing a Gaussian-like profile. The insert is the $\Delta I_d/I_d$ data of this RTN, confirming that there is only single RTN trap.

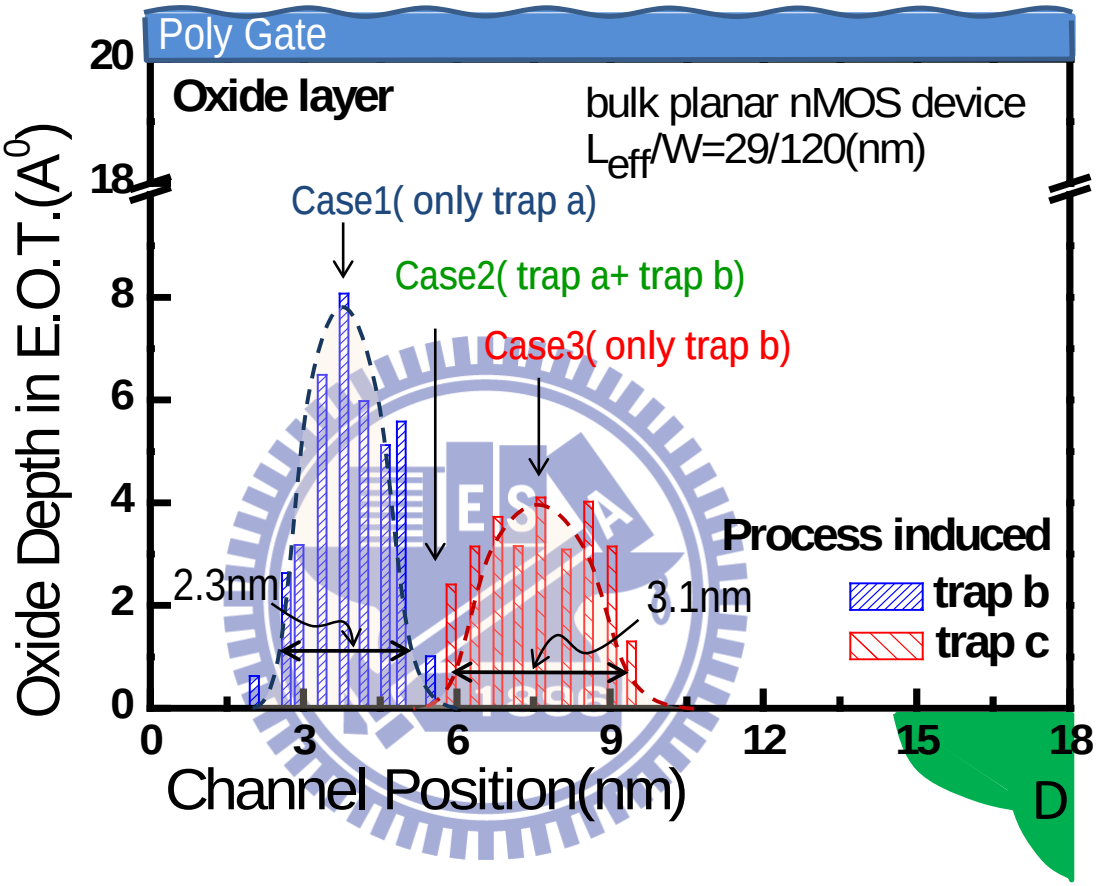


Fig. 3.2 The profiling result of process-induced multi-RTN in the bulk planar nMOS devices, showing 2 Gaussian-like packets, traps b & c. Note that we categorize this result into the Case 1, 2, and 3. For the Case 2, two packets are overlapped in tails.

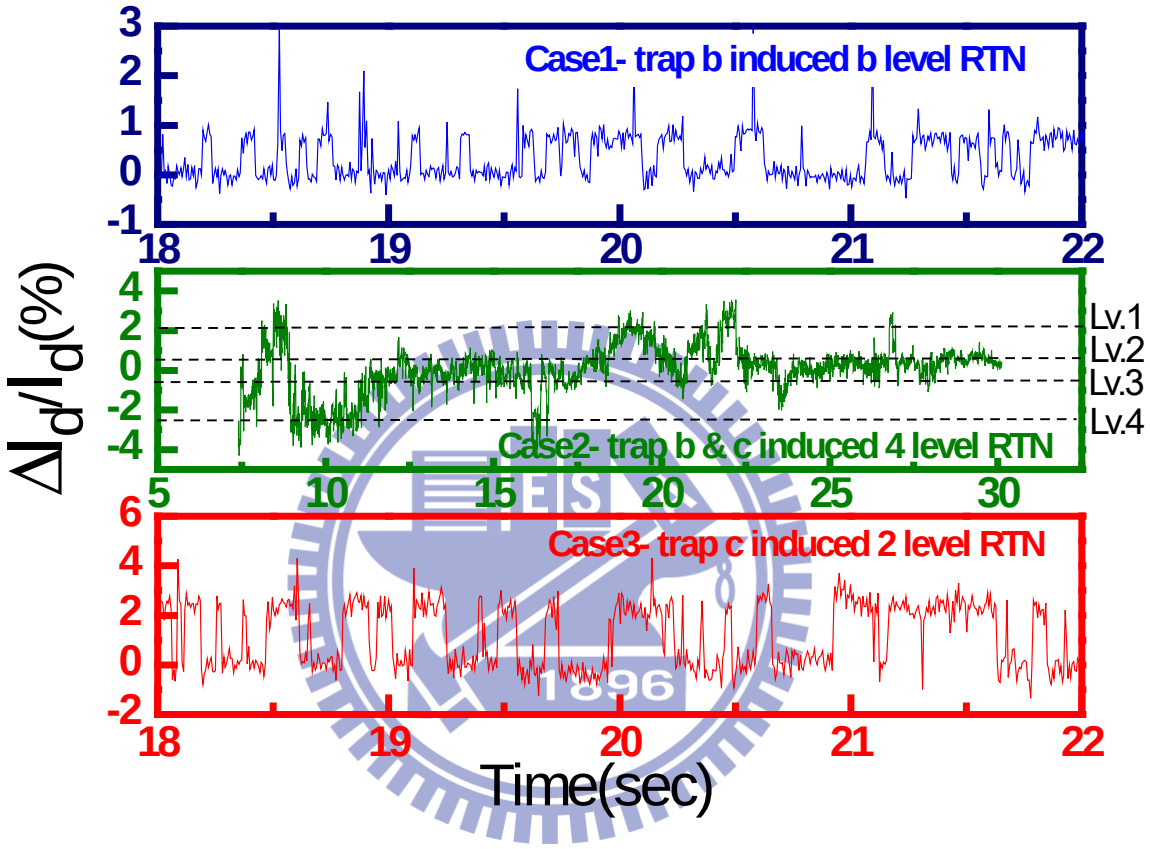


Fig. 3.3 The result of the profiling of the process-induced two-RTN traps in the bulk trigate nMOS devices, showing 2 Gaussian-like waveforms, but both waveforms are not overlapped because of a large distance between them.

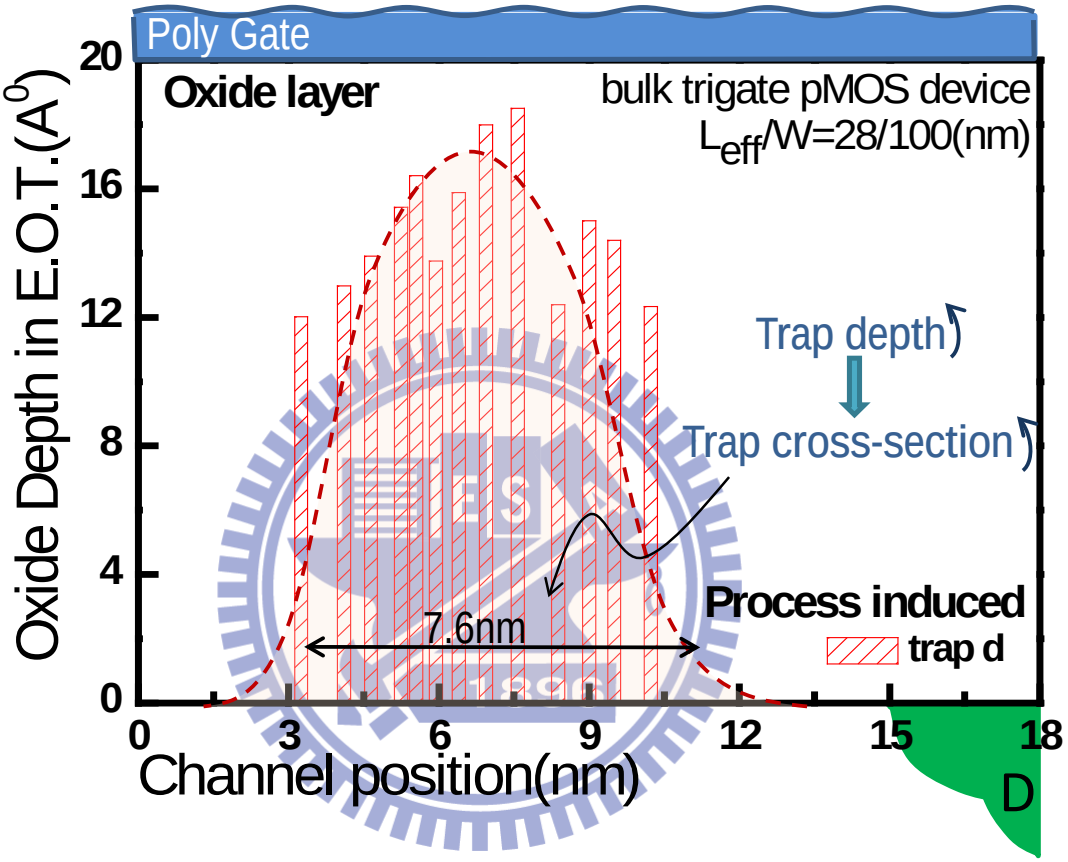


Fig. 3.4 The result of the profiling of the process-induced single-RTN in the bulk trigate pMOS devices, showing a Gaussian-like distribution.

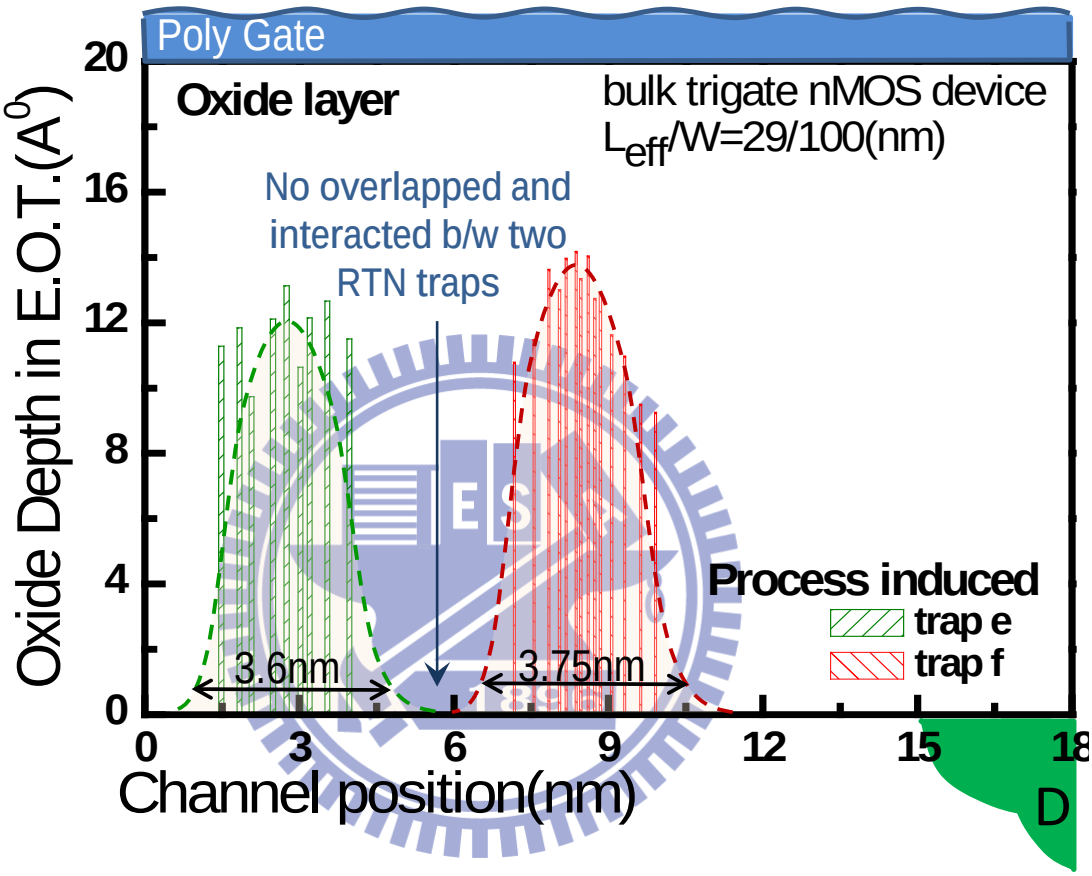


Fig. 3.5 The result of the profiling of the process-induced two-RTN traps in the bulk trigate nMOS devices, showing 2 Gaussian-like waveforms, but both waveforms are not overlapped because of a large distance between them.

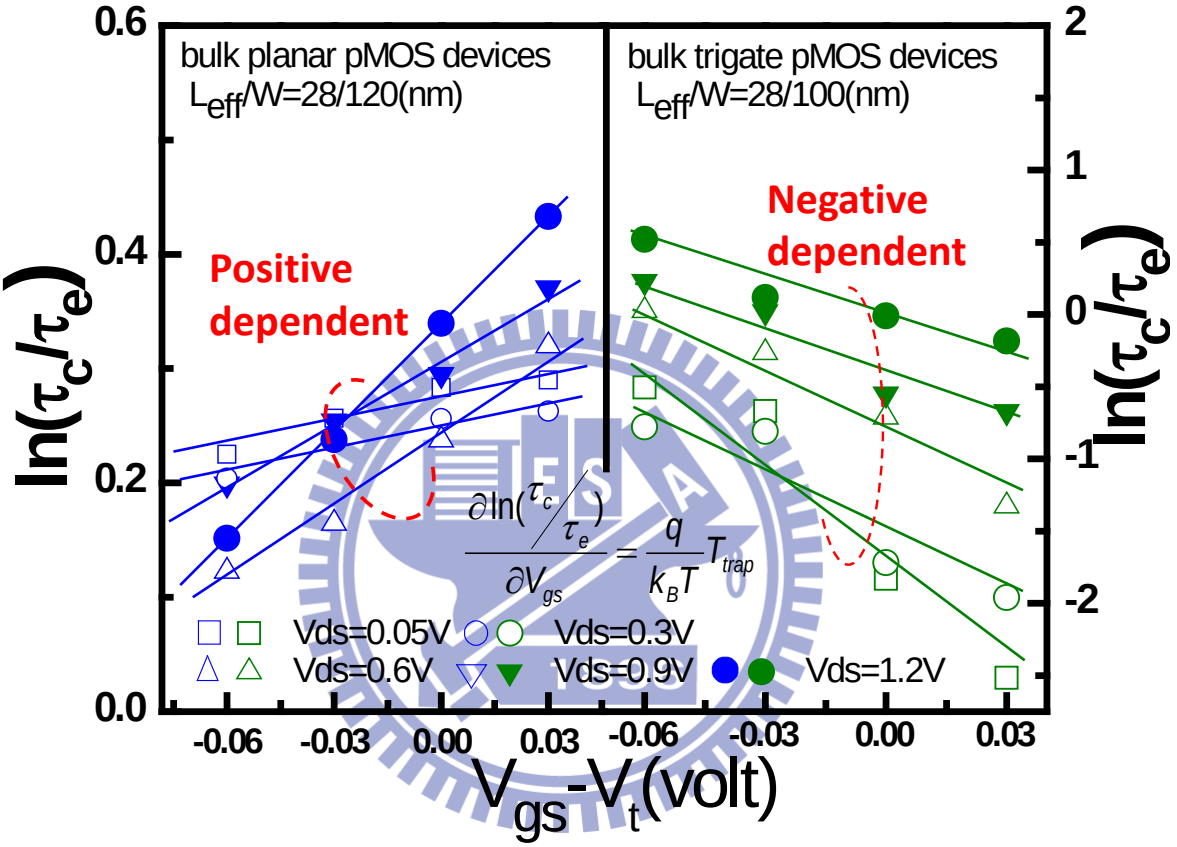


Fig. 3.6 **(left)** the $\ln(\tau_c/\tau_\varepsilon)$ dependency of the bulk planar pMOS devices, showing the positive dependency, but **(right)** the bulk trigate devices shows the negative dependency.

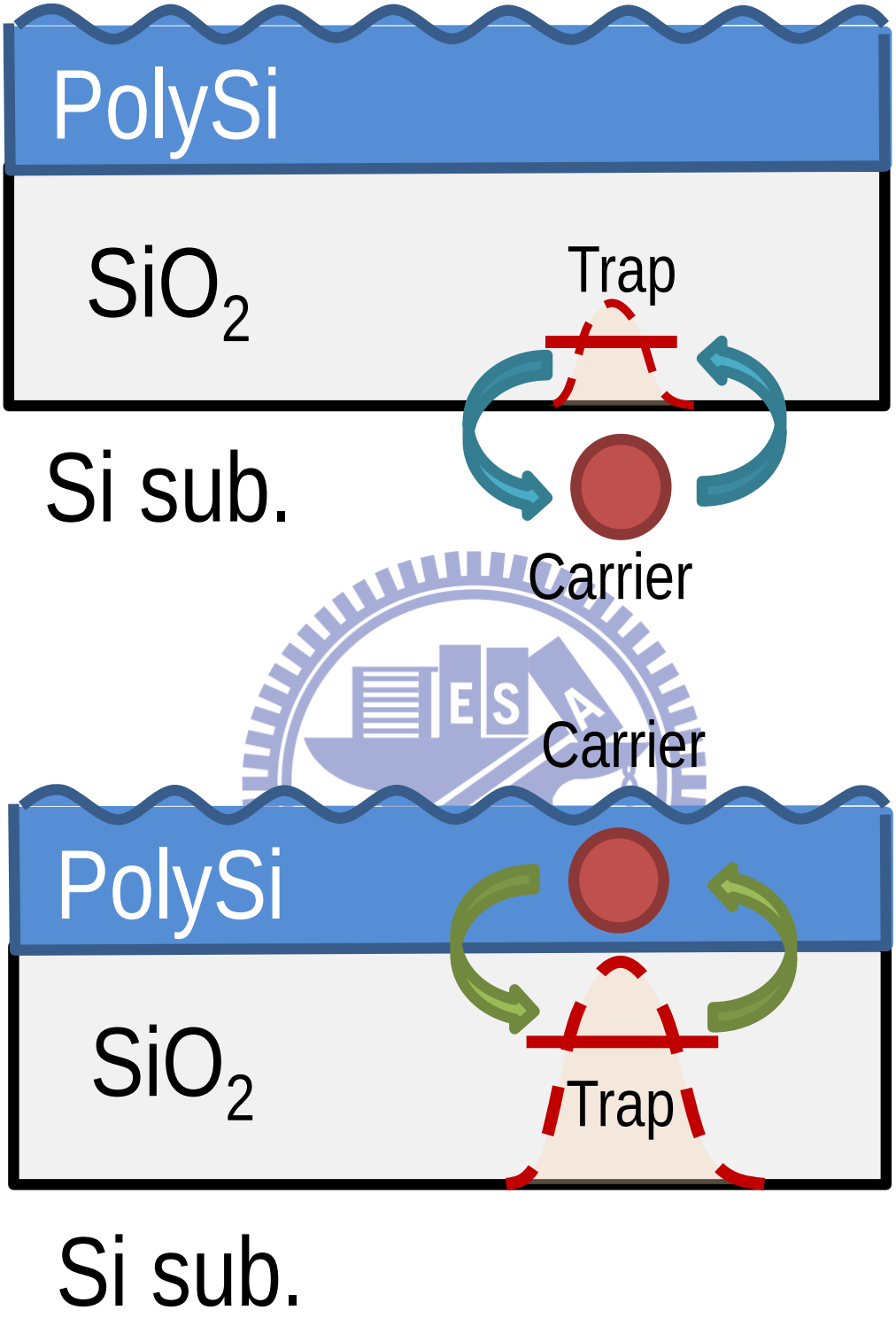


Fig. 3.7 From judging the RTN proofing data and $\ln(\tau_c/\tau_e)$ dependency, we conclude that ***(up)*** RTN of planar devices are near the interface between the oxide and Si; ***(down)*** RTN of trigate devices are near the interface between the oxide and poly-Si.

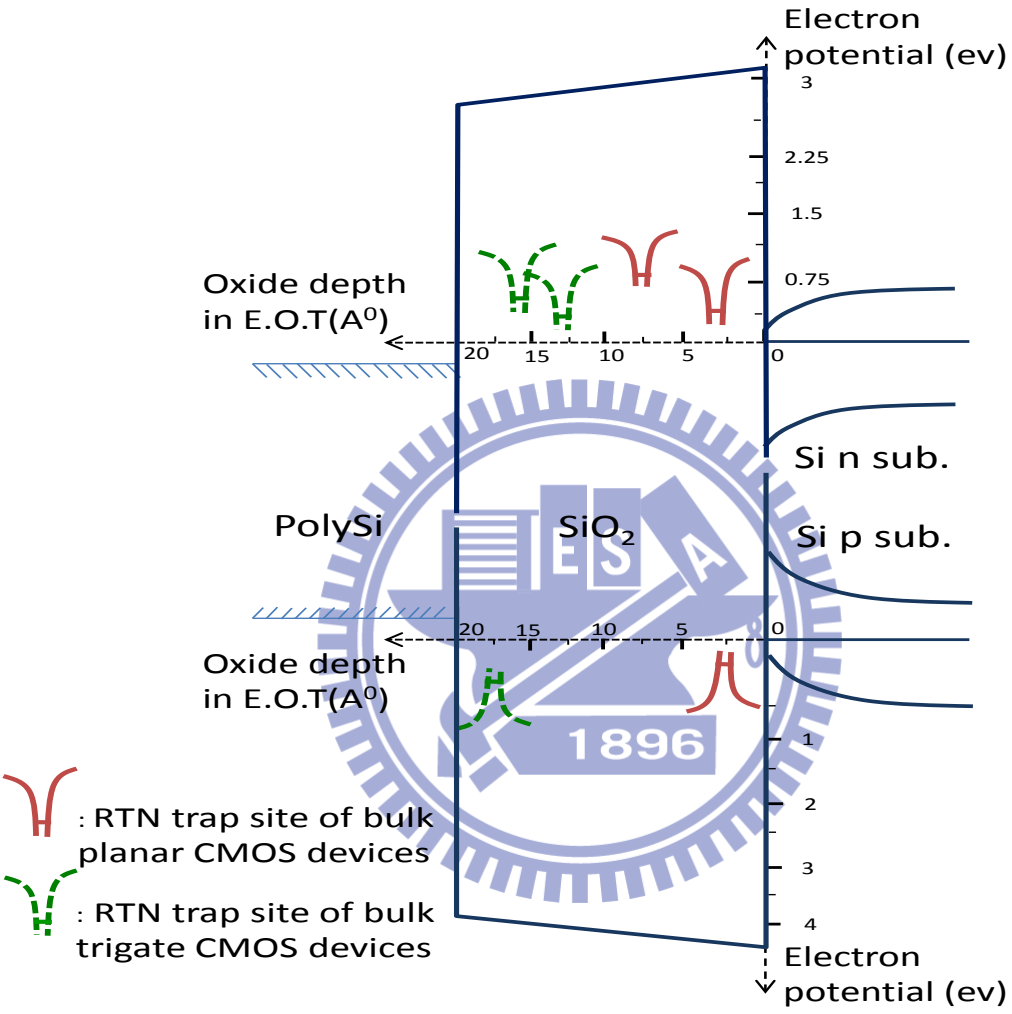


Fig. 3.8 Summarizes the information of process induced RTN in this work.

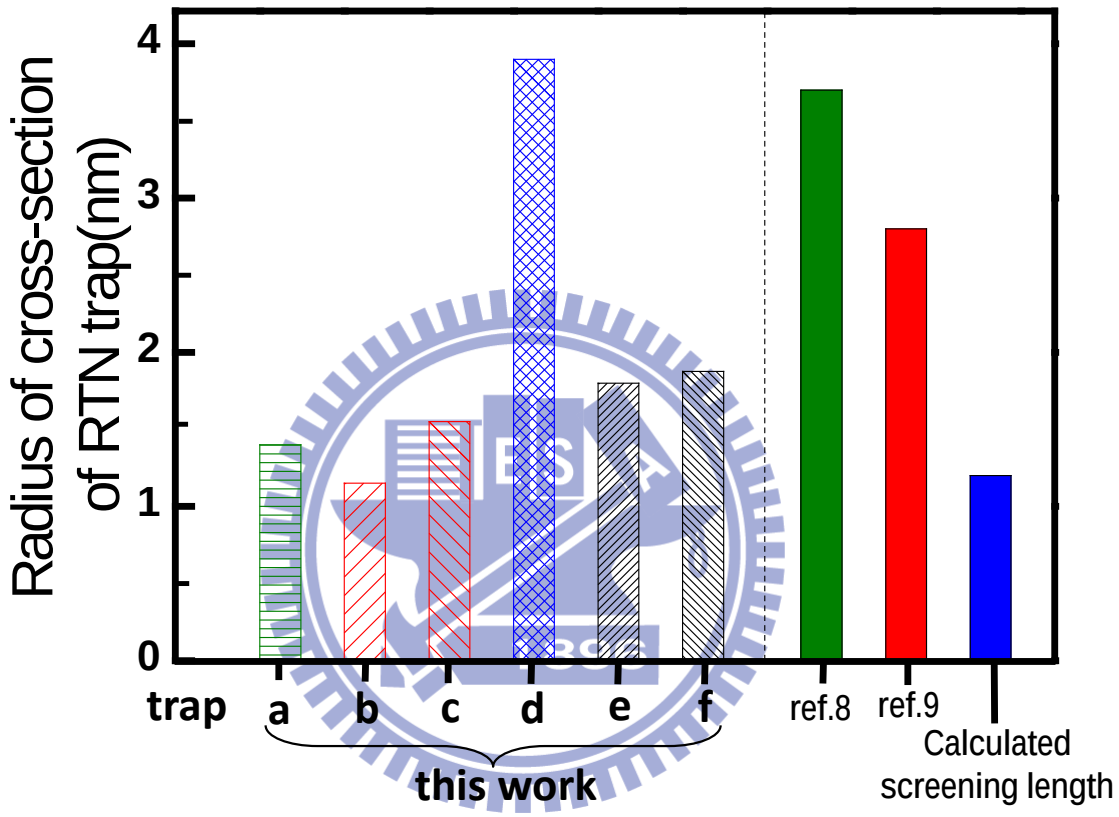


Fig. 3.9 The comparisons of the cross-section of the process-induced RTNs in this work. The reported data and the theoretical value show good consistency.

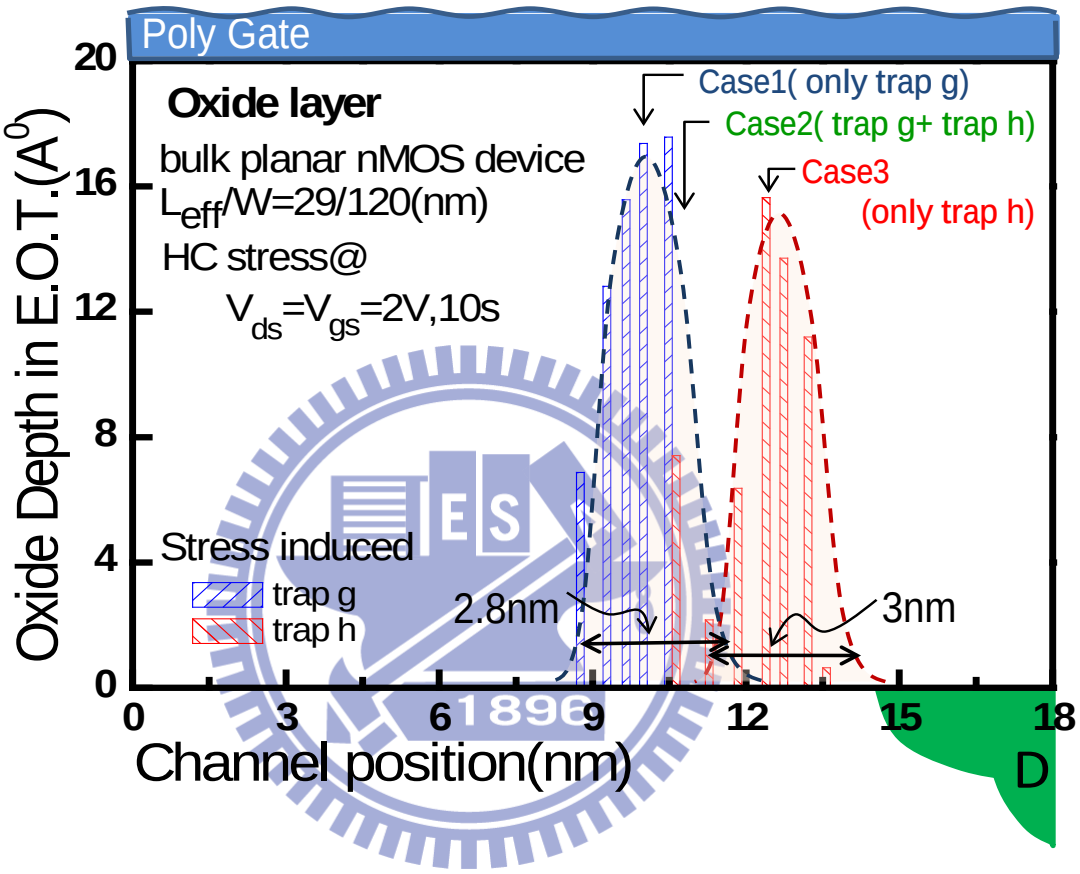


Fig. 3.10 The result of the HC stresss-induced multi-RTN in bulk planar nMOS devices, showing 2 Gaussian-like packets, traps g & h with strong interference. We categorize this result into the Case 1, 2, and 3. For the Case 2, two packets are overlapped in tails.

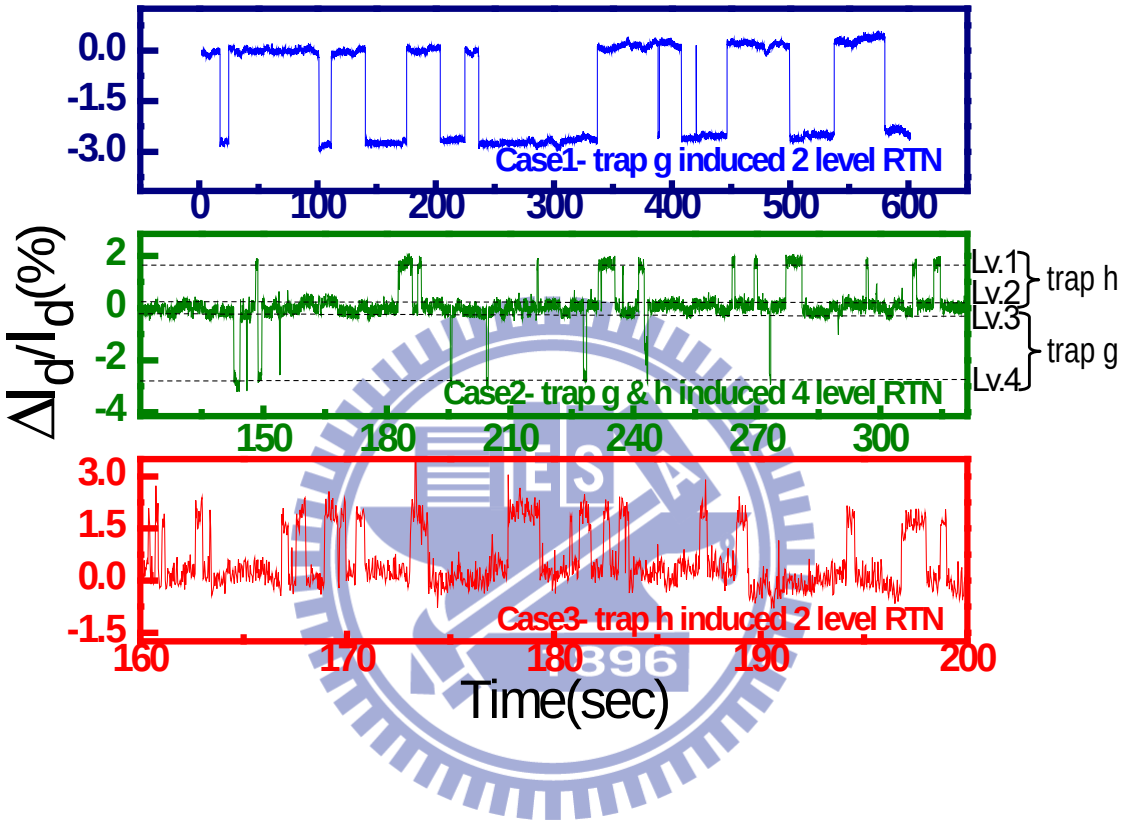


Fig. 3.11 Cases 1, 2, & 3 addressed in Fig. 3.10. Case 1 shows clear 2 level of $\Delta I_d/I_d$ for trap-g induced RTN, and the Case 3 is the same for trap-h. But the Case 2 shows 4-level behavior composed by the trap-g & trap-h. Lvs.1 &2 are contributed from the trap-h, the others are from the trap-g.

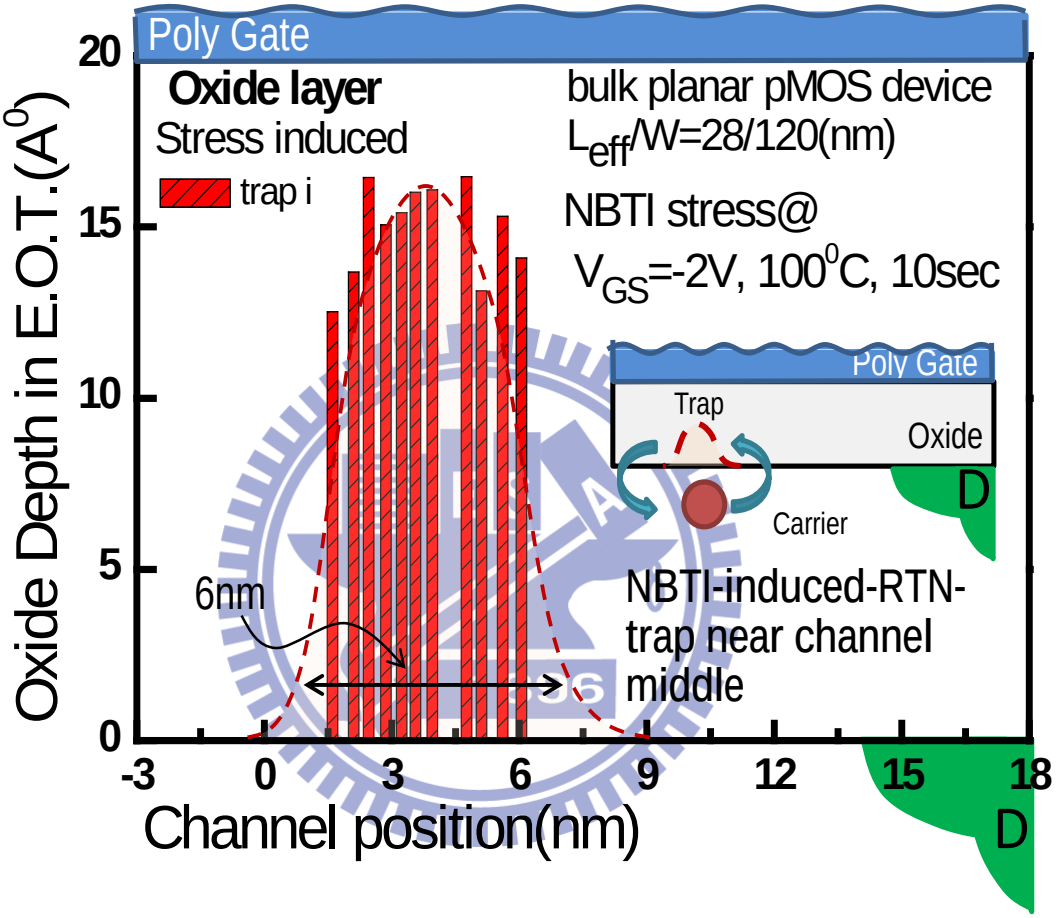


Fig. 3.12 The result of the NBTI stress-induced single-RTN in the bulk planar pMOS devices, showing a Gaussian-like shape. Note that this shape distributes near the middle of the channel region.

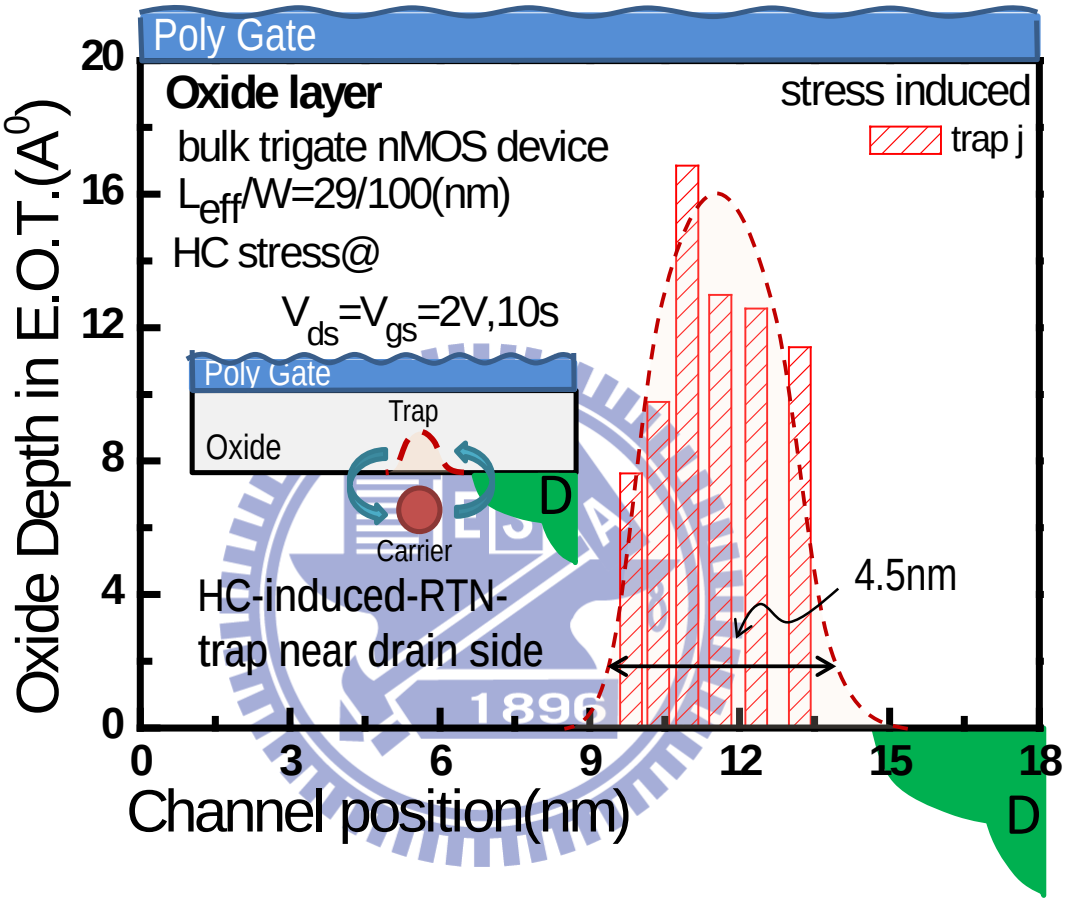


Fig. 3.13 The result of the HC stress-induced single-RTN trap in bulk trigate nMOS devices, showing a bell shape. Note that this shape distributes near the region of drain side.

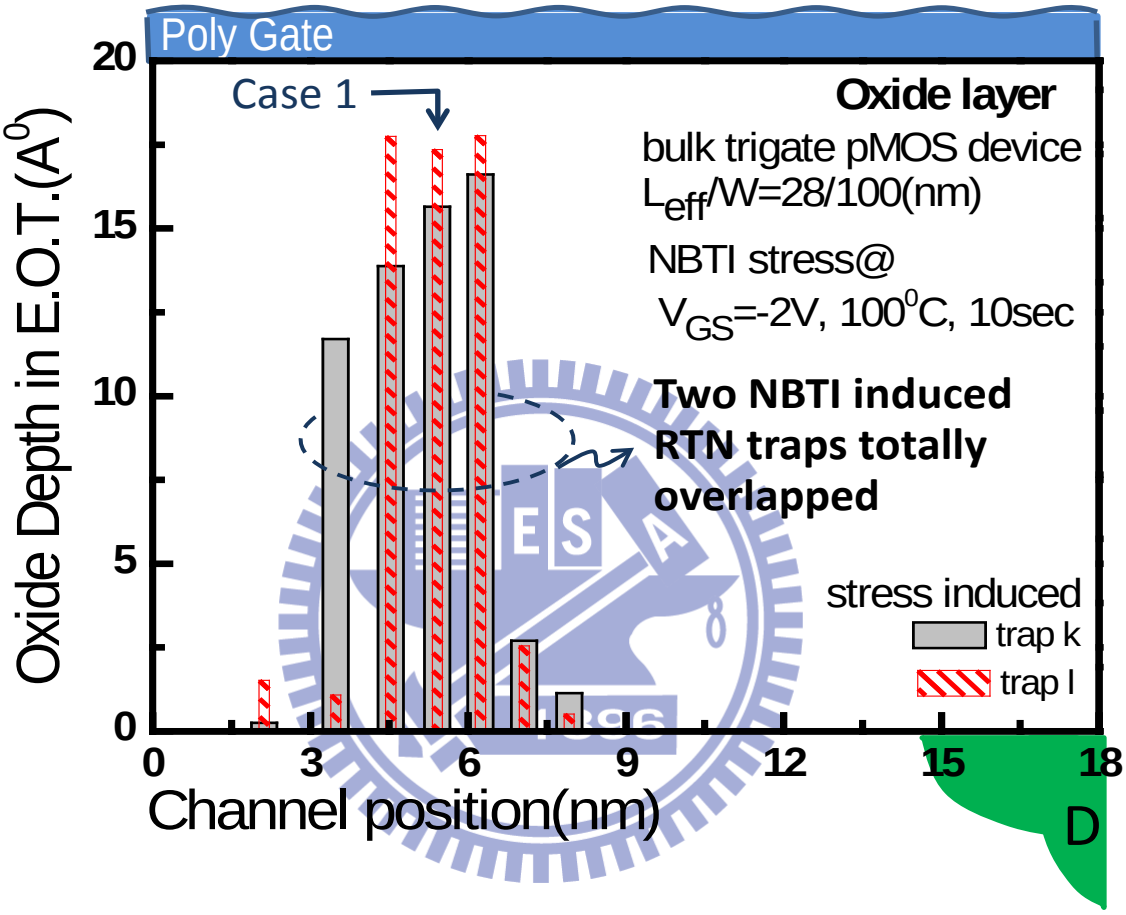


Fig. 3.14 The result of the NBTI stress-induced 2-RTN traps in bulk trigate nMOS devices. These two traps are totally overlapped in the shape and aligned on the same channel position with very close trap depths.

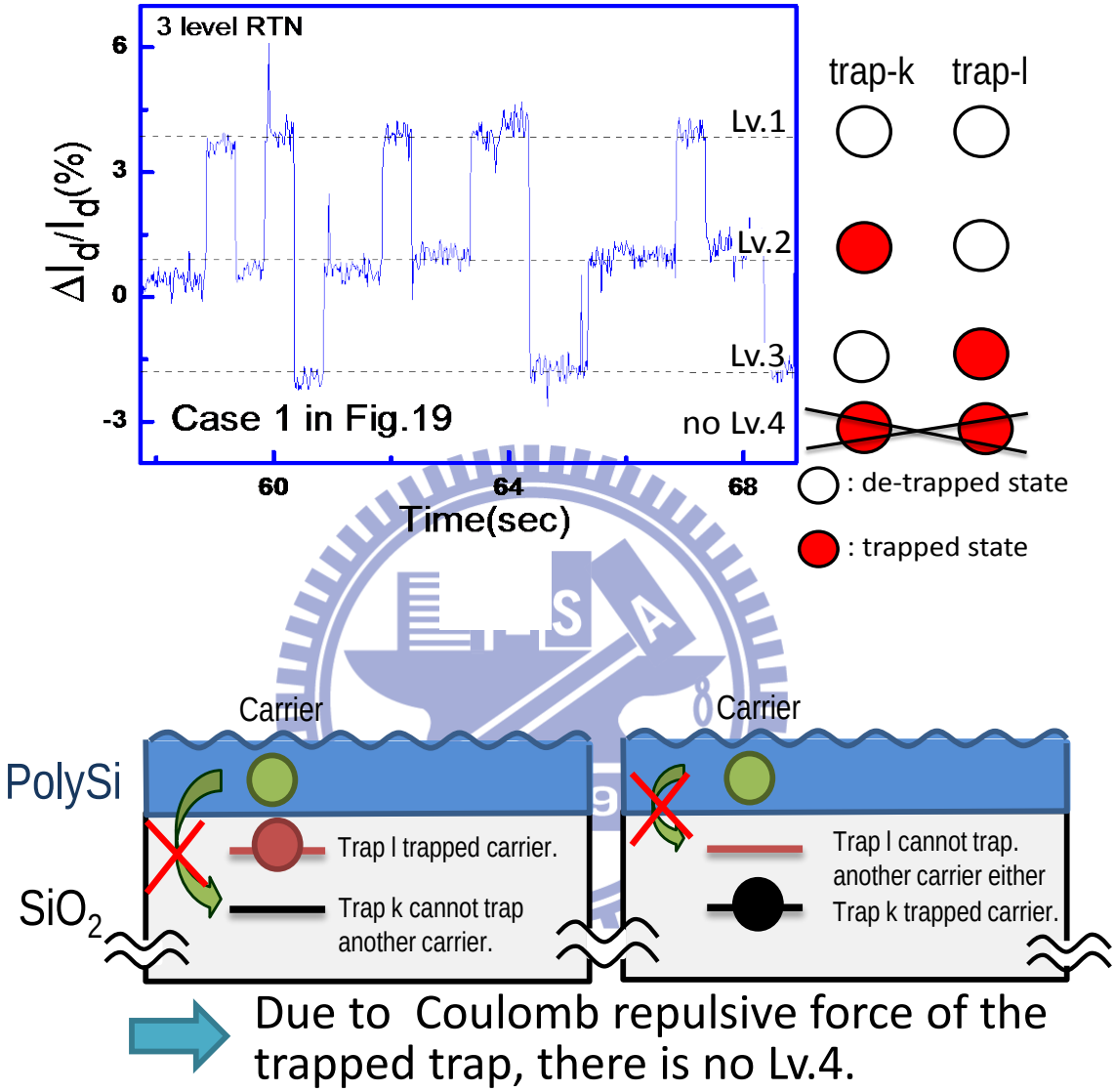


Fig. 3.15 **(a)** The **3** level RTN was observed in the Case 1 addressed in Fig. 3.14. There is no Lv.4, which two traps are overlapped. This is due to the fact that Coulomb repulsive force of a trapped trap rejects the trapping process of empty trap, (b) & (c).

Chapter 4

The Applications of Multi-RTN: The Impact on SRAM Operation & The Manipulation of RTN-trap Positions

4.1 Introduction

In this chapter, we will be focused on the influence of device variation on circuits, especially for SRAM. As microprocessors and other electronic applications get faster and faster, the need for large quantities of data at very high speeds increases, while providing the data at such high speeds get more difficult to accomplish. Besides, the manipulation of RTN-trap positions has been demonstrated by utilizing different stress methods. It will reveal a new scenario of the discrete-bit storage on SONOS or nano-crystal memory cells in the future.

As microprocessor speed increases from 25 MHz to 1GHz and beyond, system designers have become more creative in their use of cache memory, interleaving, burst mode, and other high-speed methods for accessing memory. The old system sporting just an on-chip instruction cache, a moderate amount of DRAM and a hard drive have given way to sophisticated designs using multi-level memory architectures. One of the primary building blocks of the multi-level memory architecture is the data cache.

According to our previous research, RTN traps induced by excessive mechanical stress are correlated to leakage current in very high-density SRAM devices, especially multi-RTN, and it will degrade the RSNM severely.

Finally, we are interested in the manipulation of RTN-trap positions. In the previous study, we found that the RTN-trap position is dependent on the stress methods, and therefore, we may control the trap positions by the HC stress or the FN stress.

Hot-carrier emission is expected to be accelerated in the depletion region. Electrons gain energy through channel potential. While electrons get 3.2eV, it will be injected from the conducting band in the silicon substrate to the gate dielectric, and it is probable to break either a covalent or a Si-H bond randomly. Because the HC-stress will induce electron-hole pairs, by monitoring the substrate current, we can distinguish the extent of hot carriers. A high substrate current means a large number of created electron-hole pairs and therefore an efficient Si-H bond breakage mechanism. When interface states are created by HC stress, the threshold voltage is modified, and the subthreshold slope is degraded.

According to the principle of HC stress, it can be used to control the RTN traps generated at the drain edge. Moreover, the maximum electric field will be shifted toward the center of the channel by modifying the drain voltage, and the traps will be generated there. Through the profiling result, we found that the traps are generated at the region

between the channel middle and the drain edge actually. In the final part, we utilize the FN stress to generate RTN-traps in the center of channel. In the previous measurement result, we found that the RTN traps are located in the center of the channel through NBTI stress. Hence, we consider that the electric field distribution of NBTI stress is similar to that of FN stress in nMOS devices. After the measurement, the manipulation of RTN-traps in the channel which is generated by different stress conditions has been observed.

4.2 The Basics of SRAM

4.2.1 SRAM Operations

The SRAM cell consists of a bi-stable flip-flop connected to the internal circuitry by two access transistors as shown in Fig. 4.1. When the cell is not addressed, the two access transistors are closed, and the data is kept to a stable state, latched within the flip-flop. The flip-flop needs the power supply to keep the information. The data in an SRAM cell is volatile. However, the data does not “leak away” like in a DRAM, so the SRAM does not require a refresh cycle.

Figure 4.2 shows the read/write operations of an SRAM. To select a cell, the two access transistors must be “on” so the elementary cell (the flip-flop) can be connected to

the internal SRAM circuitry. These two access transistors of a cell are connected to the word line (also called row or X address). The selected row will be set at V_{CC}. The two flip-flop sides are therefore connected to a pair of lines, B and $\bar{B}$. The bit lines are (also called columns or Y addresses). During a read operation, these two bit lines are connected to the sense amplifier that recognizes if a logic data “1” or “0” is stored in the selected elementary cell. This sense amplifier then transfers the logic state to the output buffer which is connected to the output pad. There are as many sense amplifiers as the output pads. During a write operation, data come from the input pad. It then moves to the write circuitry. Since the write circuitry drivers are stronger than the cell flip-flop transistors, the data will be forced onto the cell. When the read/write operation is completed, the word line (row) is set to 0V, the cell (flip-flop) either keeps its original data for a read cycle or stores the new data which was loaded during the write cycle.

4.2.2 Steady Noise Margin

The SRAM cell immunity to static noise is measured in terms of SNM that quantifies the maximum amount of voltage noise that can be tolerated at the cross-inverters output nodes without flipping the cell. The graphical method to determine the SNM uses the static voltage transfer characteristics of the SRAM cell inverters.

4.2.3 Impact of Multi-level RTN on SRAM

Figure 4.3 is a 6T SRAM and TEM picture. To study RTN impact on SRAM carefully, we defined two cases of multi-RTN traps generated in different transistors. The two cases including RTN traps are generated on the pull up transistor only, and RTN traps generated on both pull-up transistor and pull-down transistor, as shown in Fig. 4.4. Because the RTN signals induce the V_t disturbance, the V_t of device with RTN will become multi-level.

Figure 4.5 shows the butterfly curve of planar SRAM under the case 1, pull-up transistor with multi-RTN signals. It has been observed that the butterfly curves split into 4-levels (the insert). Fig. 4.6 shows the RTN signals measured in pull-up transistor, and 4-levels can be pointed out demonstratively. It is the reason for the butterfly curves split into 4-levels. The similar phenomena can be observed in the trigate SRAM. Fig. 4.7 shows the butterfly curves of the trigate SRAM also split into clear 4-level transition under the same case. Fig. 4.8 shows the I_D RTN signals measured in the pull-up transistor, and 4-levels can be demonstrated. Comparing the butterfly curves of the planar SRAM with the trigate SRAM, the butterfly curves of trigate SRAM separate widely. It is because the RTN amplitude of the trigate devices is larger than that of the planar devices. Fig. 4.9 shows the comparison of σRSNM between the planar devices and the trigate devices under the case 1. From the figure, we realize that the σRSNM increases severely, due to the RTN generation

under the case 1. Besides, the σRSNM for trigate SRAM is much larger than the planar SRAM under this case. From the result of our research, we also found that σRSNM depends on the amplitude of RTN signals.

Figure 4.10 shows the butterfly curves of the planar SRAM under the case 2, M2 and M3 with multi-RTN. It has been observed that the butterfly curves translate fail because of RTN signals. Note that the insert shows a noticeable component of transition failure. Fig. 4.11 shows the results of multi-RTN induced trigate SRAM failure on transition, which is due to a wide V_t-shift of M3 raised by the trapping and de-trapping of multi-RTN traps. When V_t is shifted by RTN process upon the trigger voltage of SRAM, the transition will be immediately failed, Fig. 4.12 The larger multi-RTN induced V_t shift is, the higher the probability of transition failure raises.

4.3 The Manipulation of RTN-trap Positions

Figure 4.13 shows the schematic of hot-carrier stress under V_G= V_D= 2V bias condition and indicates that the impact ionization region is close to the drain edge while the drain voltage is increased. Fig. 4.14 shows the measurement result of the hot carrier stress under this condition, and the traps profile is approached to the drain side actually.

Figure 4.15 shows the schematic of hot-carrier stress under V_G= 2V and V_D= 1.5V

condition and indicates that the impact ionization region is far from the drain edge while drain voltage decreased. Fig.4.16 shows the measurement result of hot carrier stress under this condition. It has been observed that the traps profile is located in the region between the channel middle and the drain edge. Fig. 4.17 shows the I_B-V_G curve. The hot carrier stress is caused by that electric field which accelerates electrons and induces electron-hole pairs, so monitoring the I_B curve is an indispensable way to identify the mechanism of stress induced RTN-trap. I_B/ I_D ratio shows the efficiency of hot carrier stress rate, and the largest the hot carrier stress rate has been observed at V_D= 2.5V.

According to the profiling result of NBTI stress, we utilize FN-stress to inject charge to the center of the channel. Fig. 4.18 shows the schematic of the FN stress. Fig. 4.19 shows the result of RTN-traps profiling under FN-stress. Because the electric field of FN-stress is broader than that of the hot carrier stress, the wider distribution is observed. Besides, two distinct traps are found. Fig. 4.20 shows the slopes of the $\ln(\tau_c/\tau_e)$ versus V_G curve. The totally distinct slopes have been observed that the positive dependency of $\ln(\tau_c/\tau_e)$ versus V_G for trap A and negative dependency for trap B. Therefore, we consider that there are two traps.

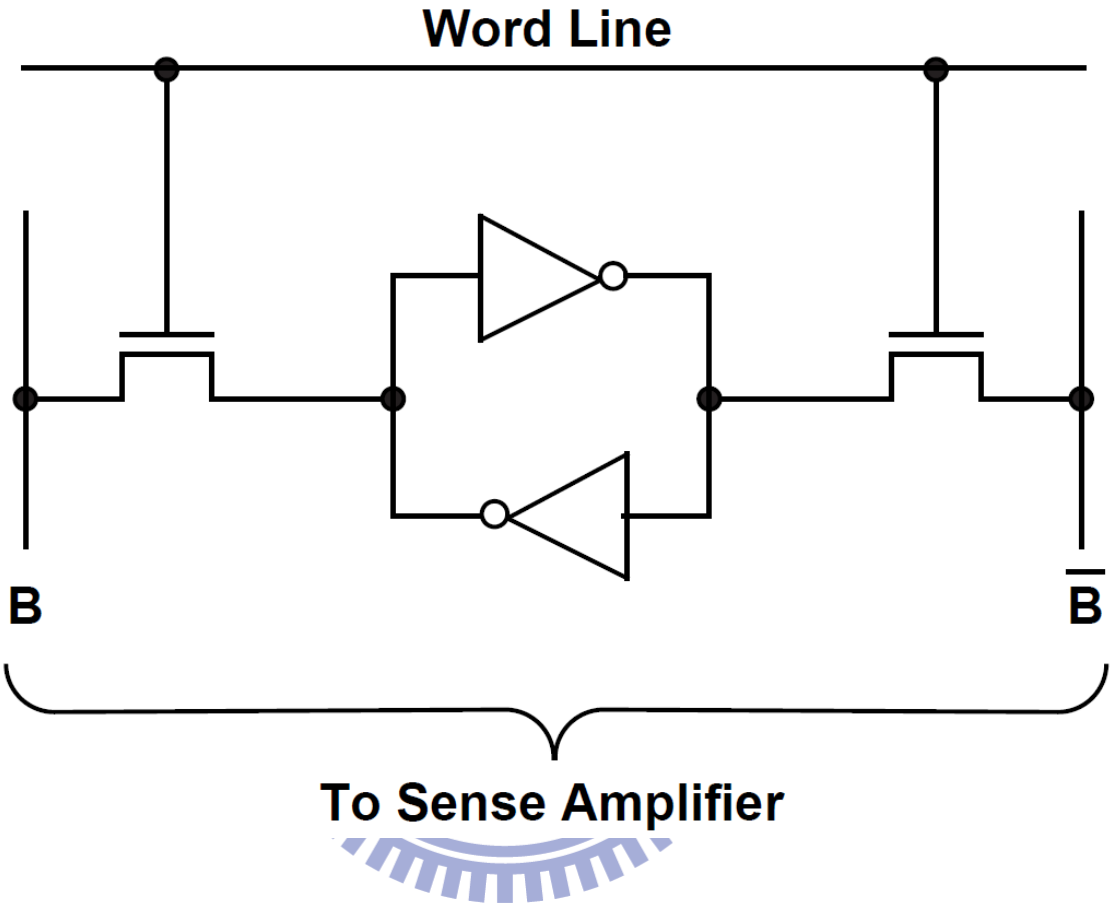


Fig. 4.1 The schematic of SRAM cell. The SRAM cell consists of a bistable flip-flop connected to the internal circuitry by two access transistors.

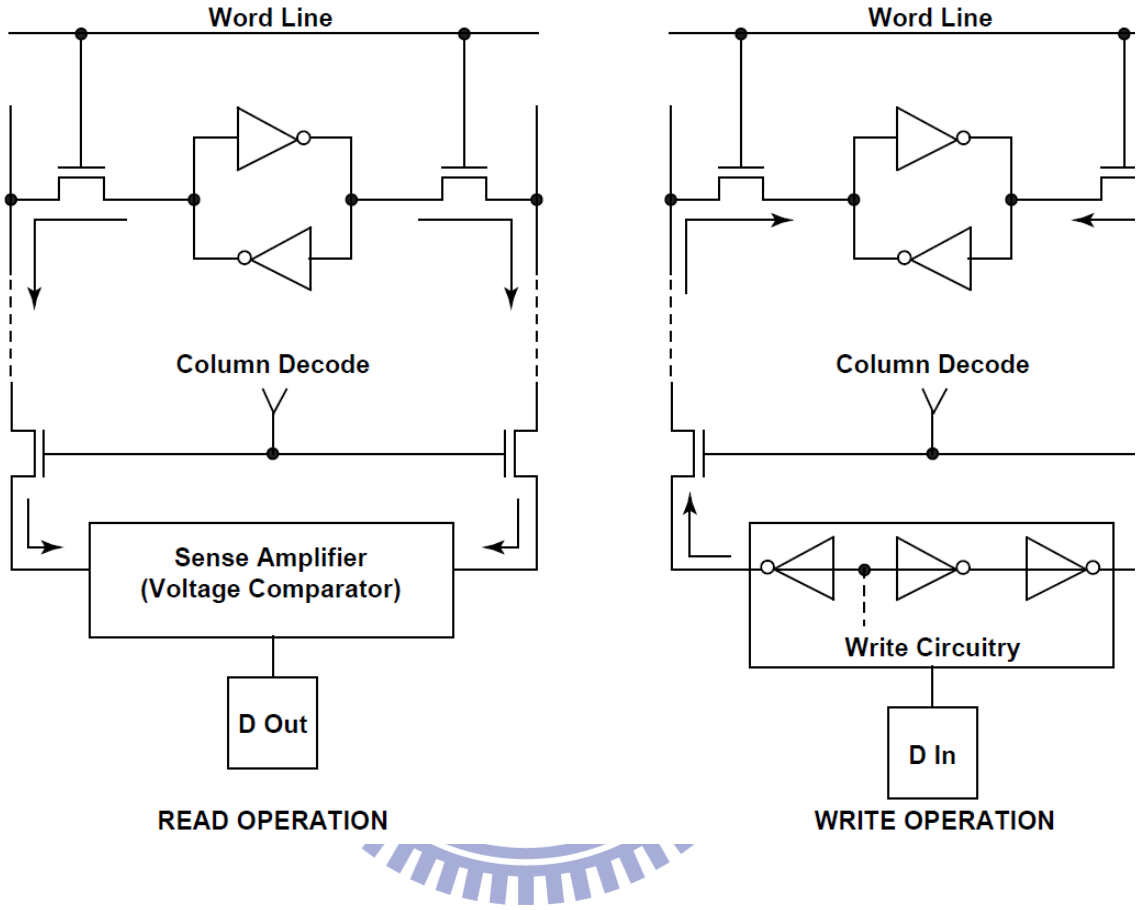


Fig. 4.2 Read/write operations.

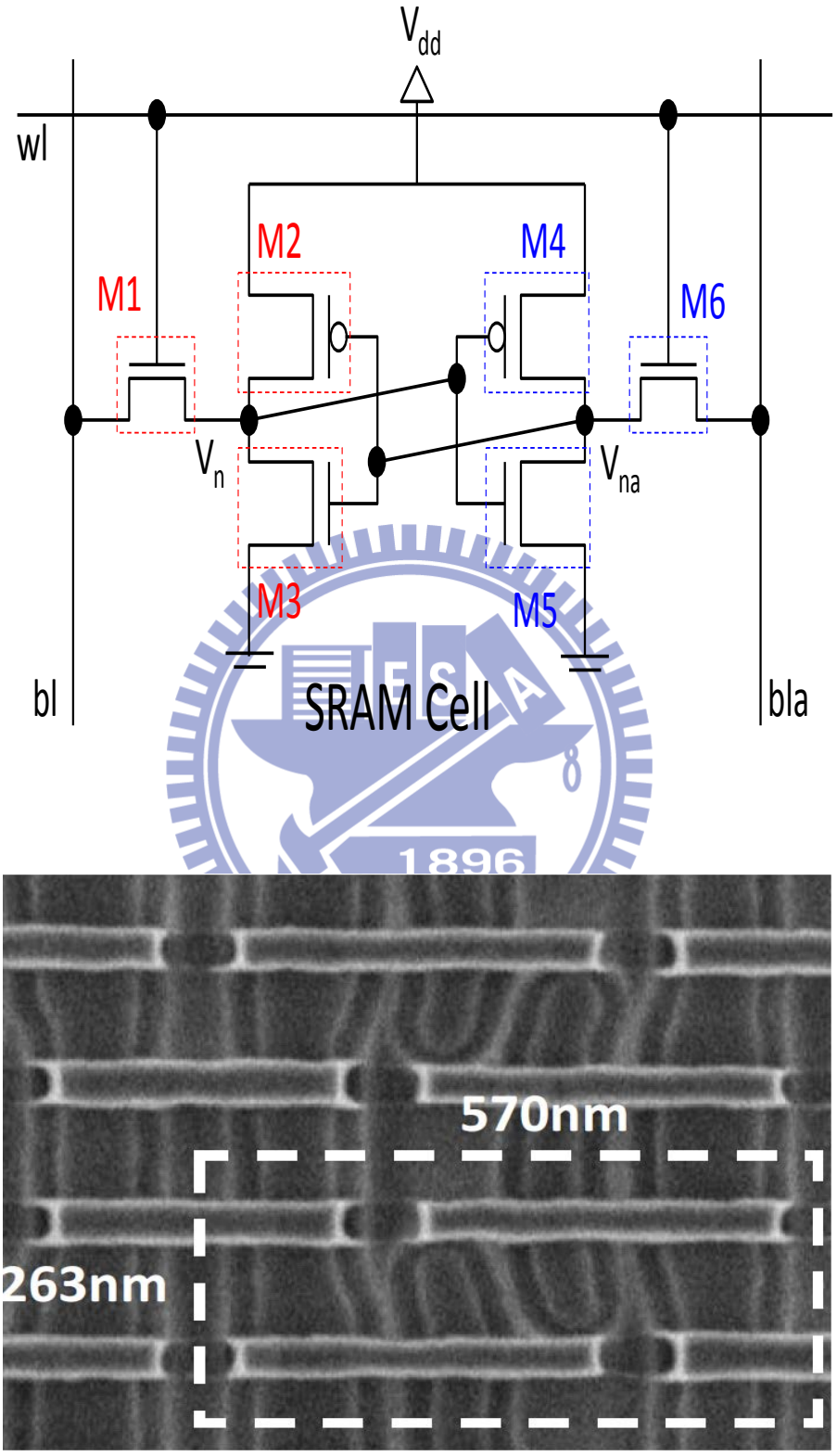


Fig. 4.3 ***(Top)*** The schematic of the SRAM circuit. (Bottom) The TEM view of SRAM.

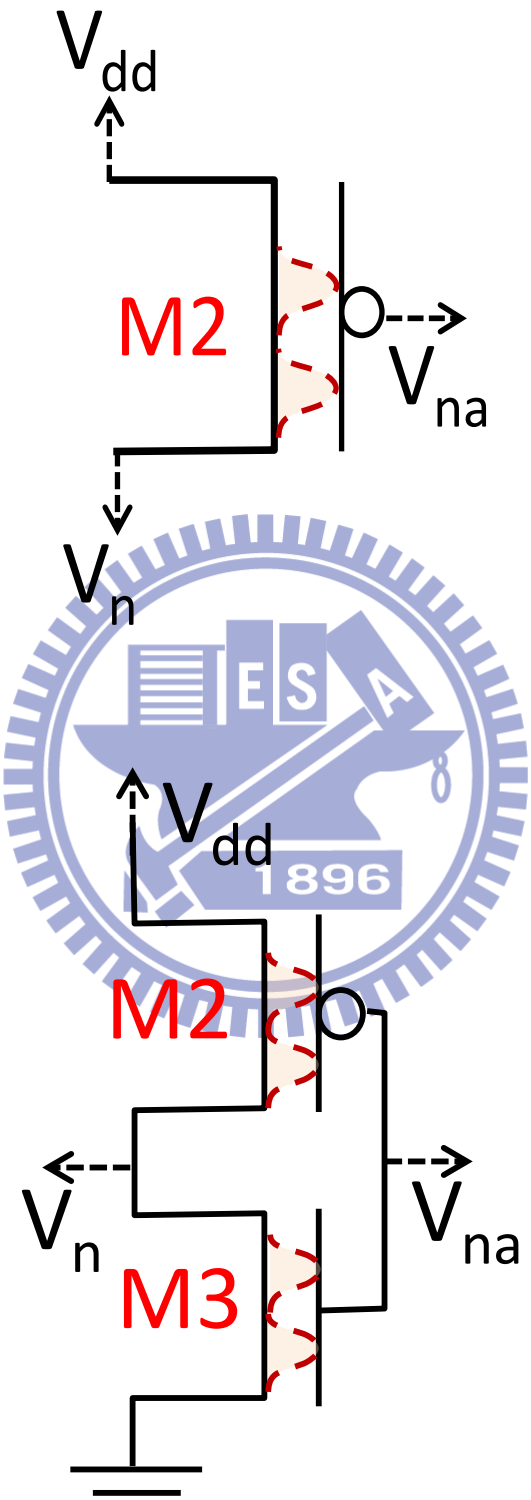


Fig. 4.4 Two multi-RTN cases utilized to study the impact of multi RTN on SRAM.

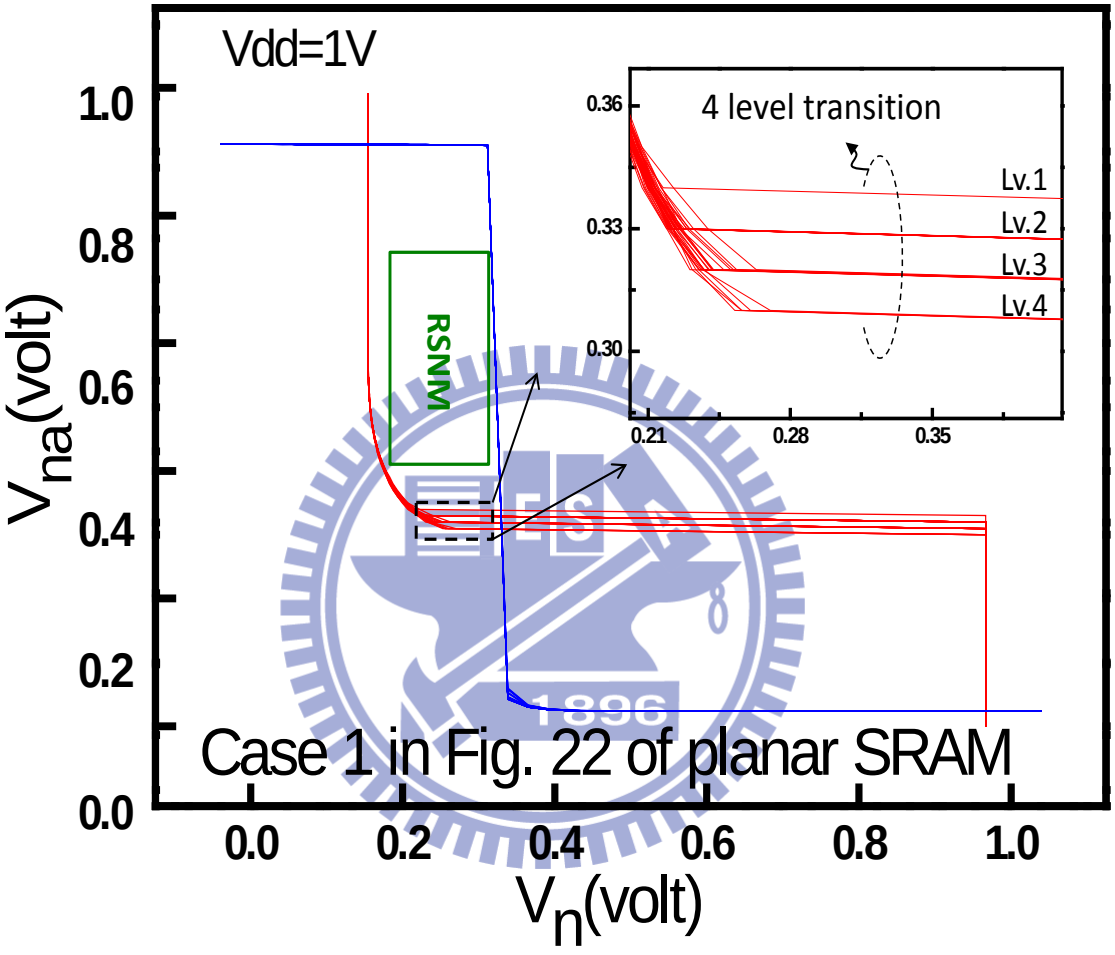


Fig. 4.5 The butterfly curves of planar SRAM with multi-RTN in M2 device. Note that the branch (red) with RTN traps has more fluctuated than that without RTN trap (blue) one. **The insert** is the zooming up, in which clear 4 level characteristic is observed, corresponding to 4 level I_d RTN of M2 devices.

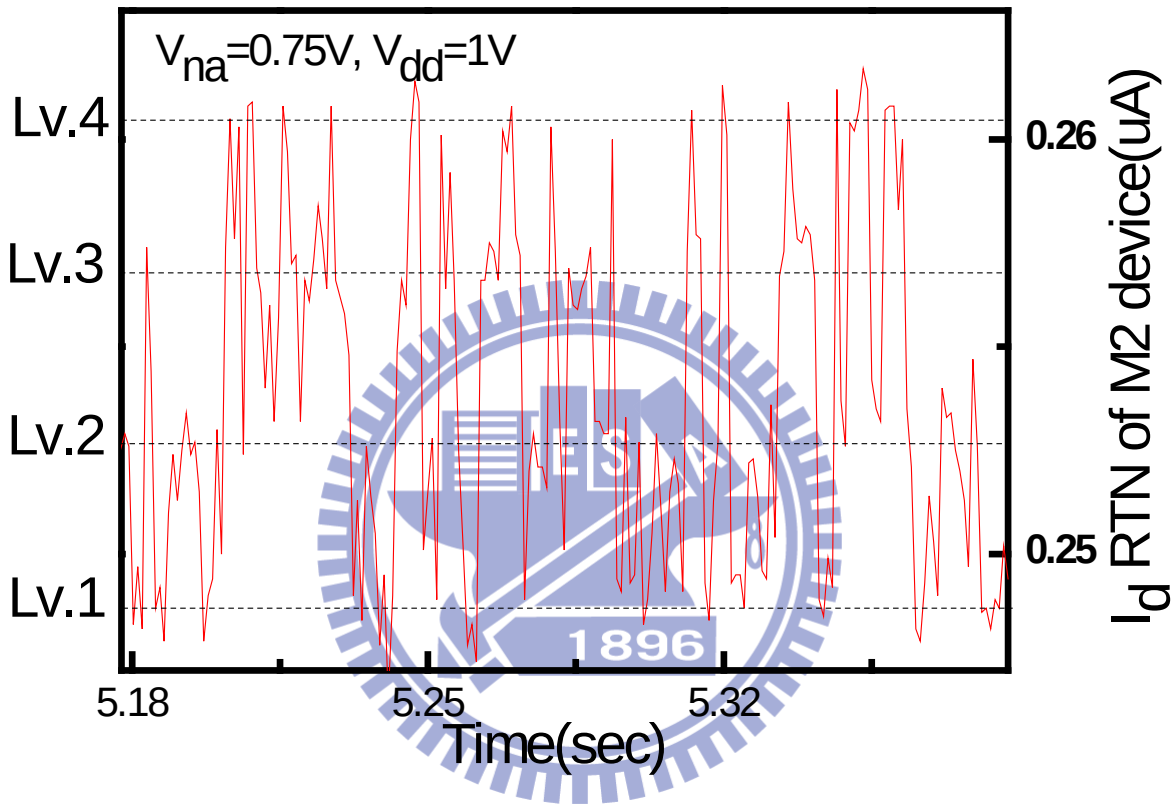


Fig. 4.6 As a result, RTN fluctuation degrades the RSNM of SRAM.

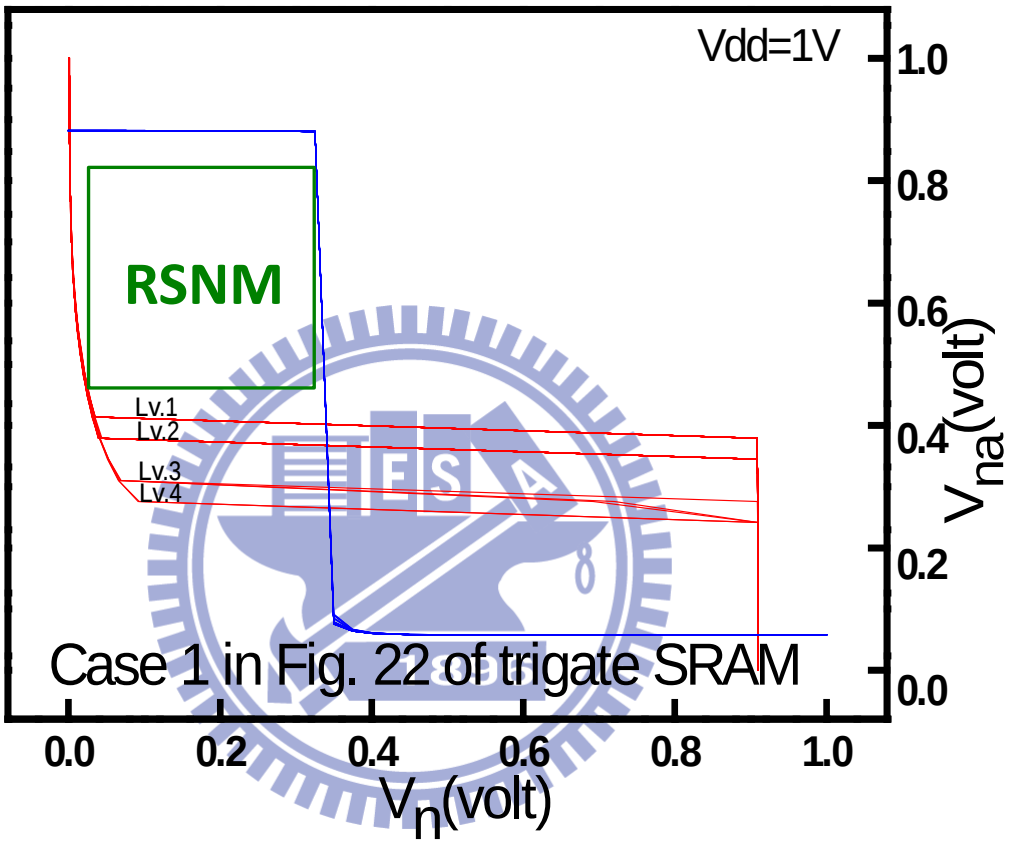


Fig. 4.7 The butterfly curves of trigate SRAM with multi-RTN in M2 device. Note that the branch (red) with RTN traps has more fluctuation than that without RTN trap(blue) one.

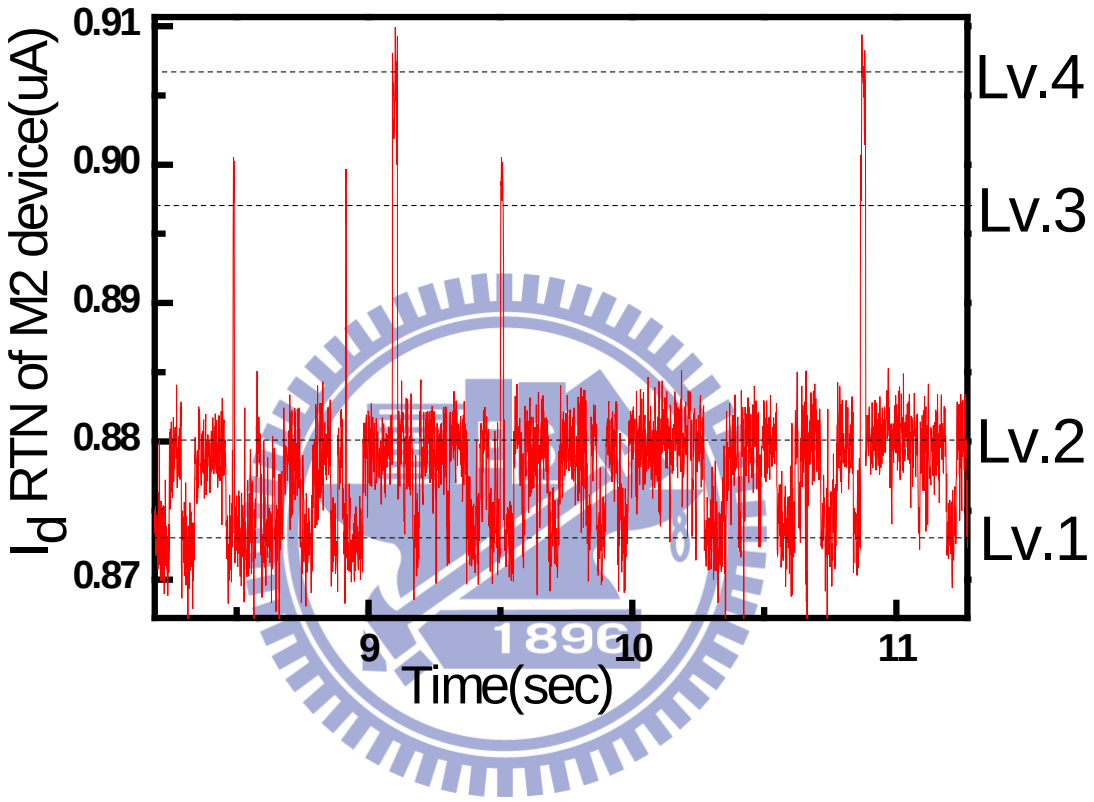


Fig. 4.8 Clear 4 level characteristic is observed, corresponding to 4 level I_d RTN of M2 devices.

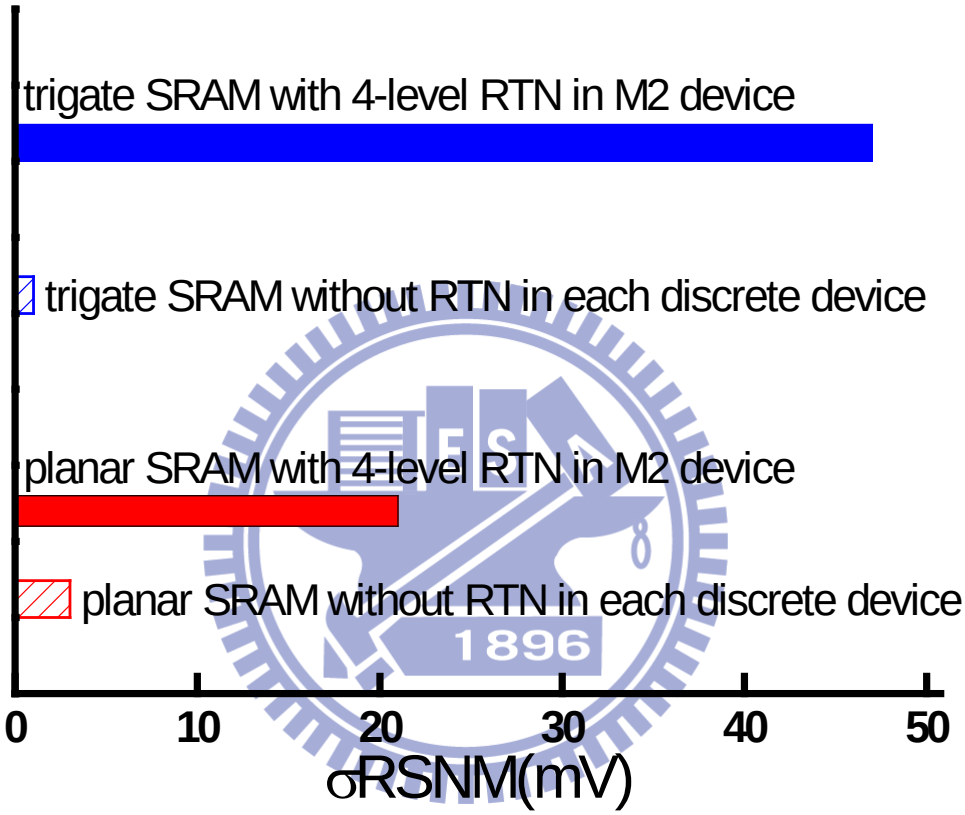


Fig. 4.9 As a result of multi-RTN in the oxide of M2 devices, the variation of RSNM will increase astonishingly. Note that the variation of RSNM increases much larger in trigate devices than that of planar devices.

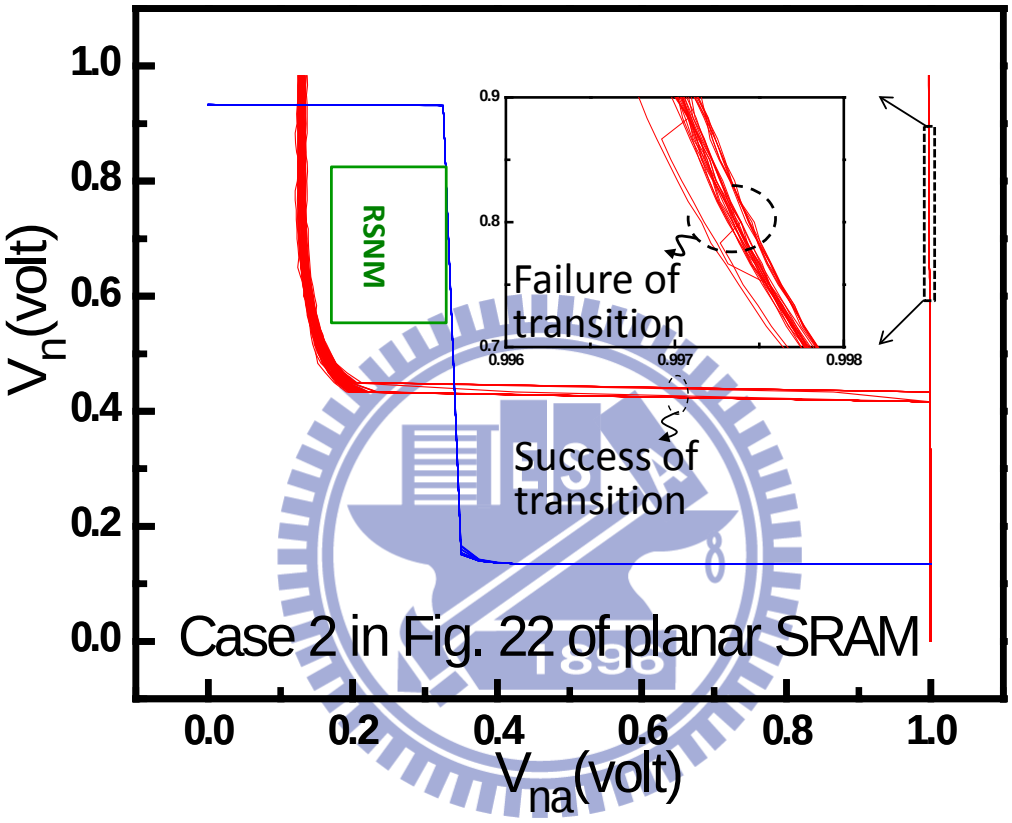


Fig. 4.10 The butterfly curves of planar SRAM with multi-RTN in M2 & M3 device. Note that the red branch shows transition failure component (the insert) due to multi-RTN in M3&M2 device. This is a newly RTN induced SRAM failure mechanism.

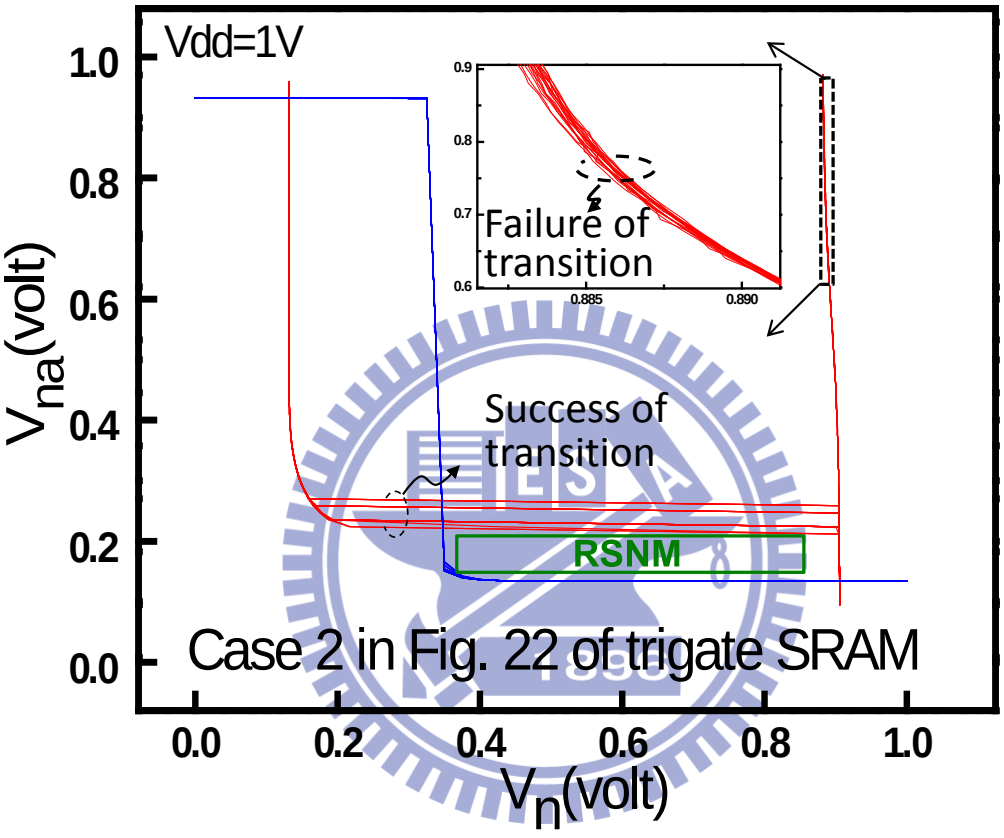


Fig. 4.11 The butterfly curves of trigate SRAM with multi-RTN in M2 & M3 devices. Note that the red branch shows transition failure component (**the insert**) due to multi-RTN in M3&M2 devices. This is a newly RTN induced SRAM failure mechanism.

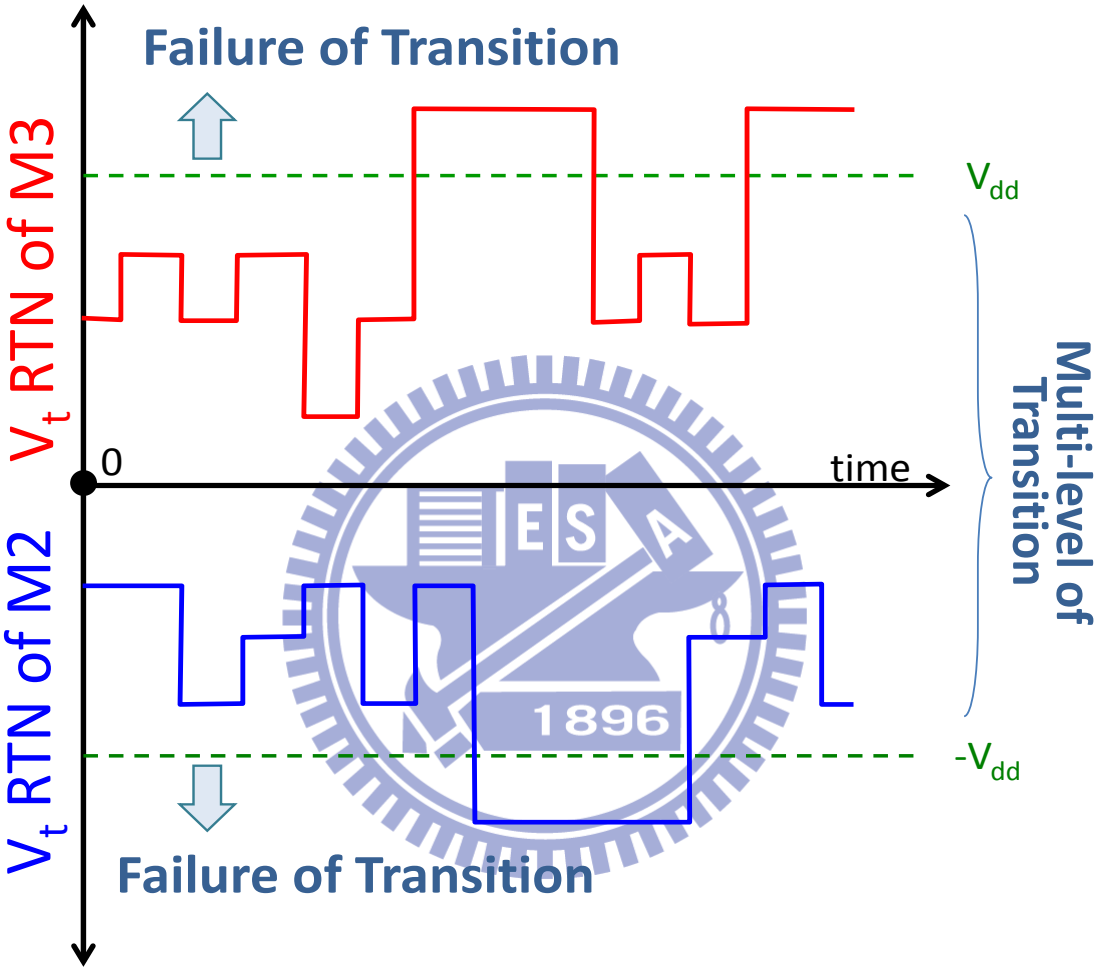


Fig. 4.12 The schematic to explain why multi-level transition and failure of transition in butterfly curves of SRAM. The RTN-induced Vt shift in M2 or M3 causes these abnormal transitions of curves.

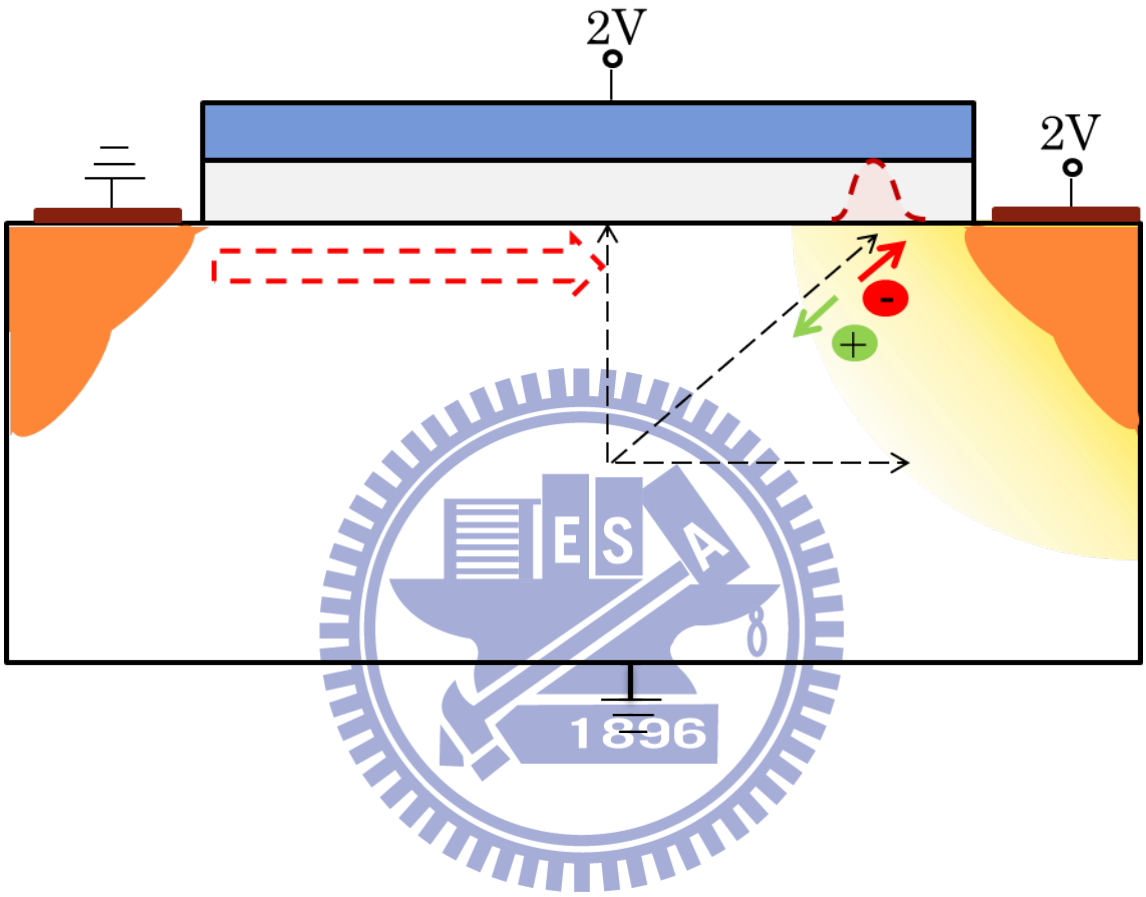


Fig. 4.13 The schematic to indicate that vertical electric field is approach to horizontal electric field, therefore RTN-traps in this stress condition is near the drain side.

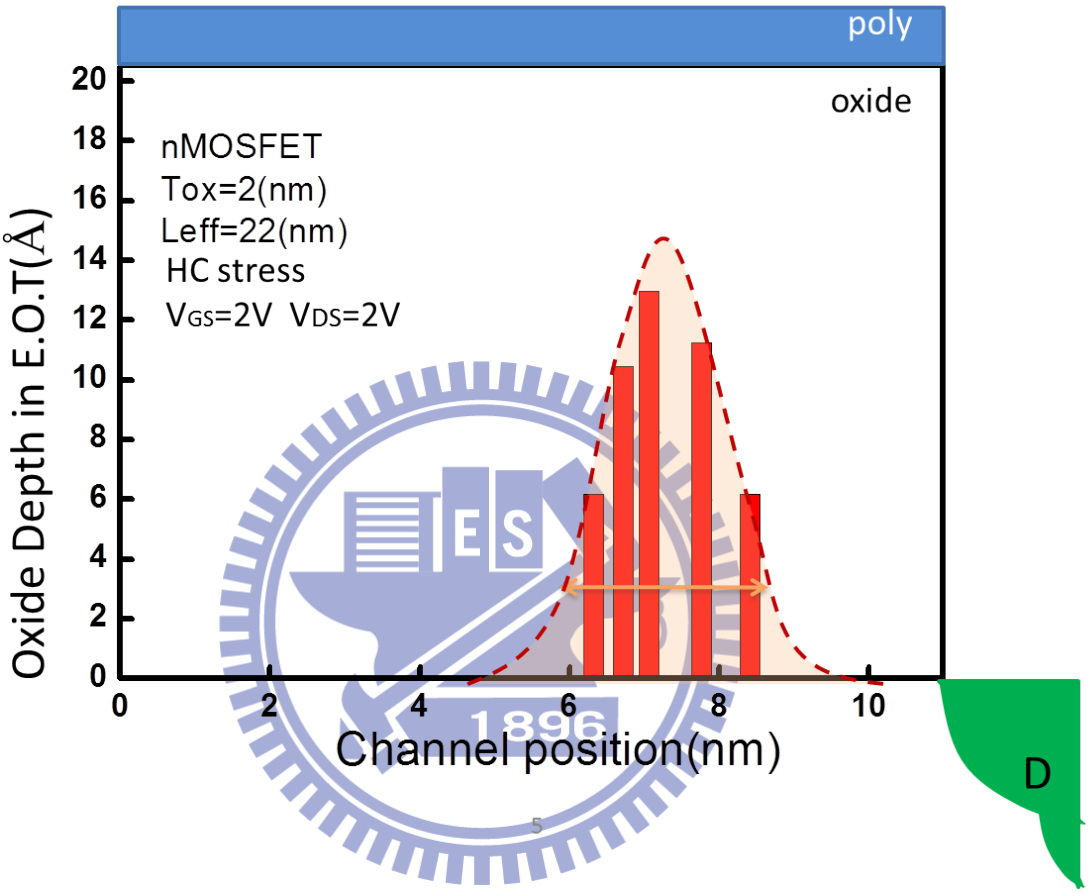


Fig. 4.14 The result of the HC stress-induced single-RTN trap in bulk planar nMOS devices, showing a bell shape. Note that this shape distributes near the drain side.

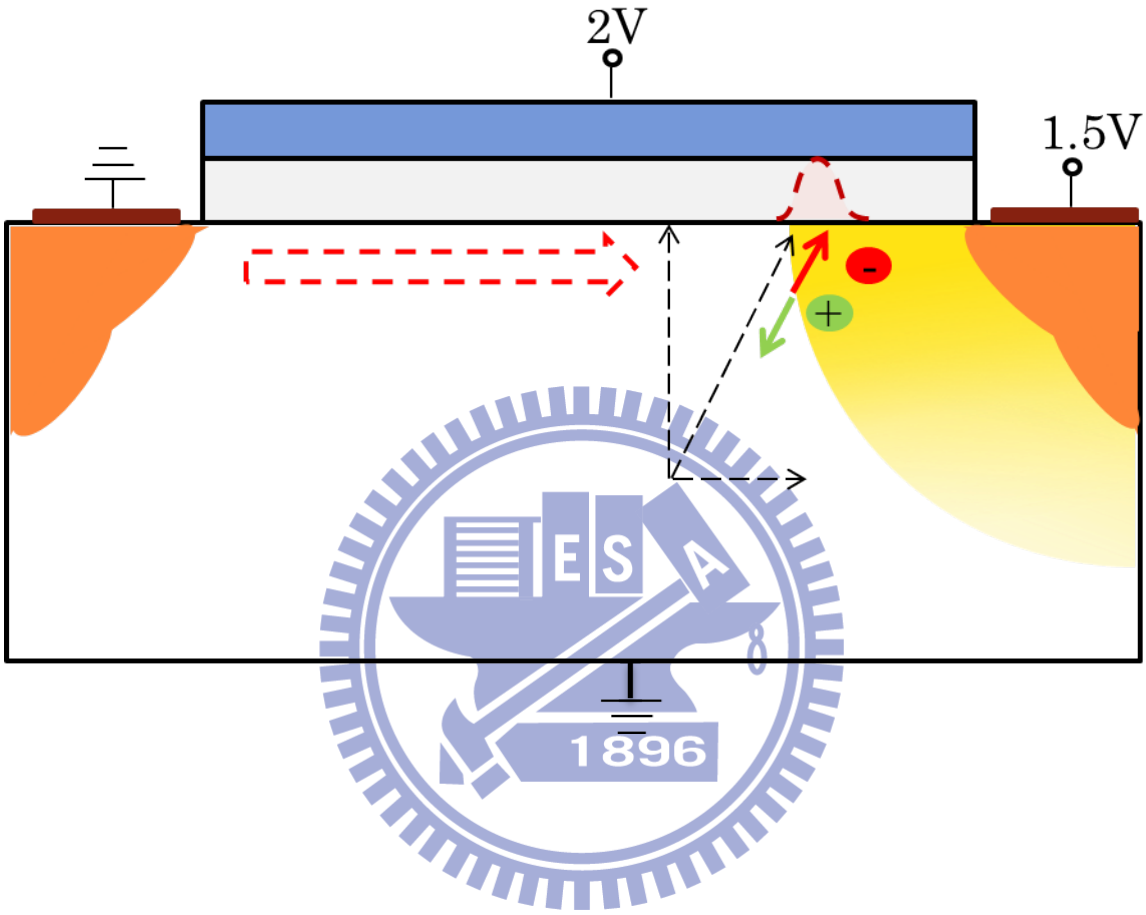


Fig. 4.15 The schematic to indicate that vertical electric field is approach to the horizontal electric field, therefore RTN-traps in this stress condition is near the drain side.

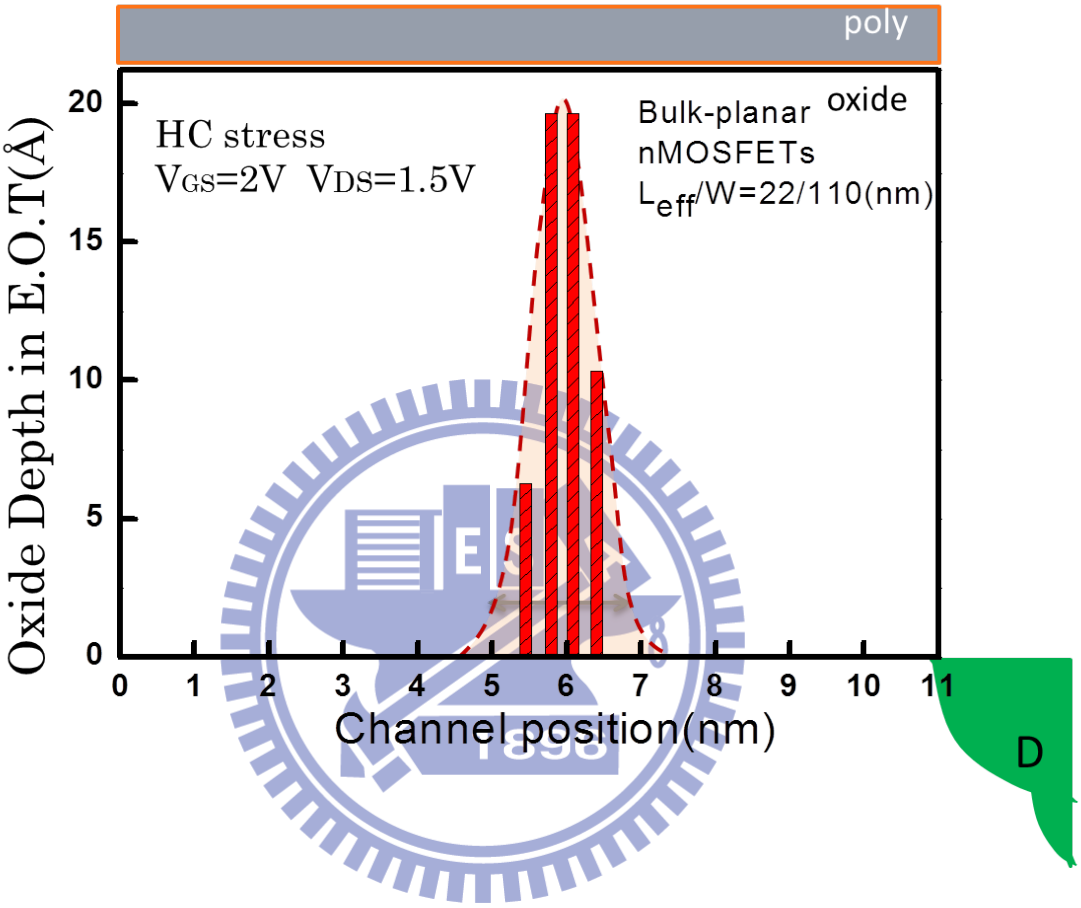


Fig. 4.16 The result of the HC stress-induced single-RTN trap in bulk planar nMOS devices, showing a bell shape. Note that this shape distributes more far from the drain side region.

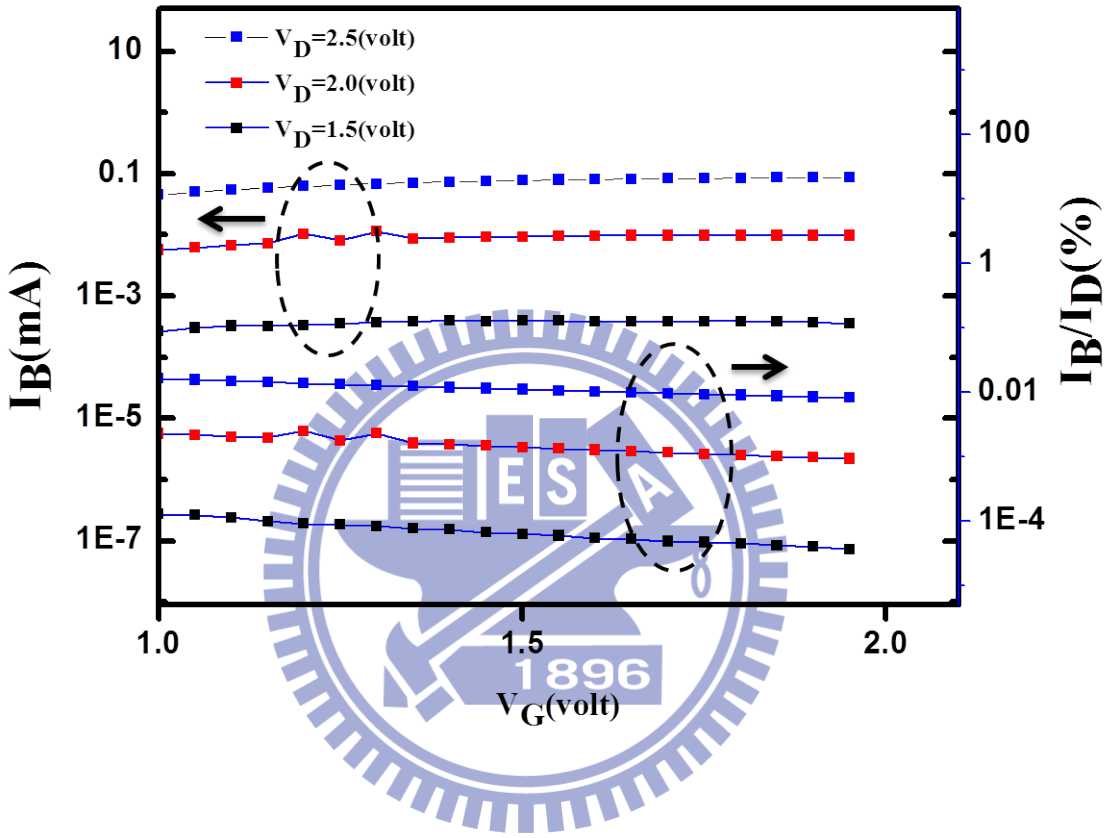


Fig. 4.17 The result of I_B and I_B/I_D versus V_G curve at different V_D for the hot carrier stress condition.

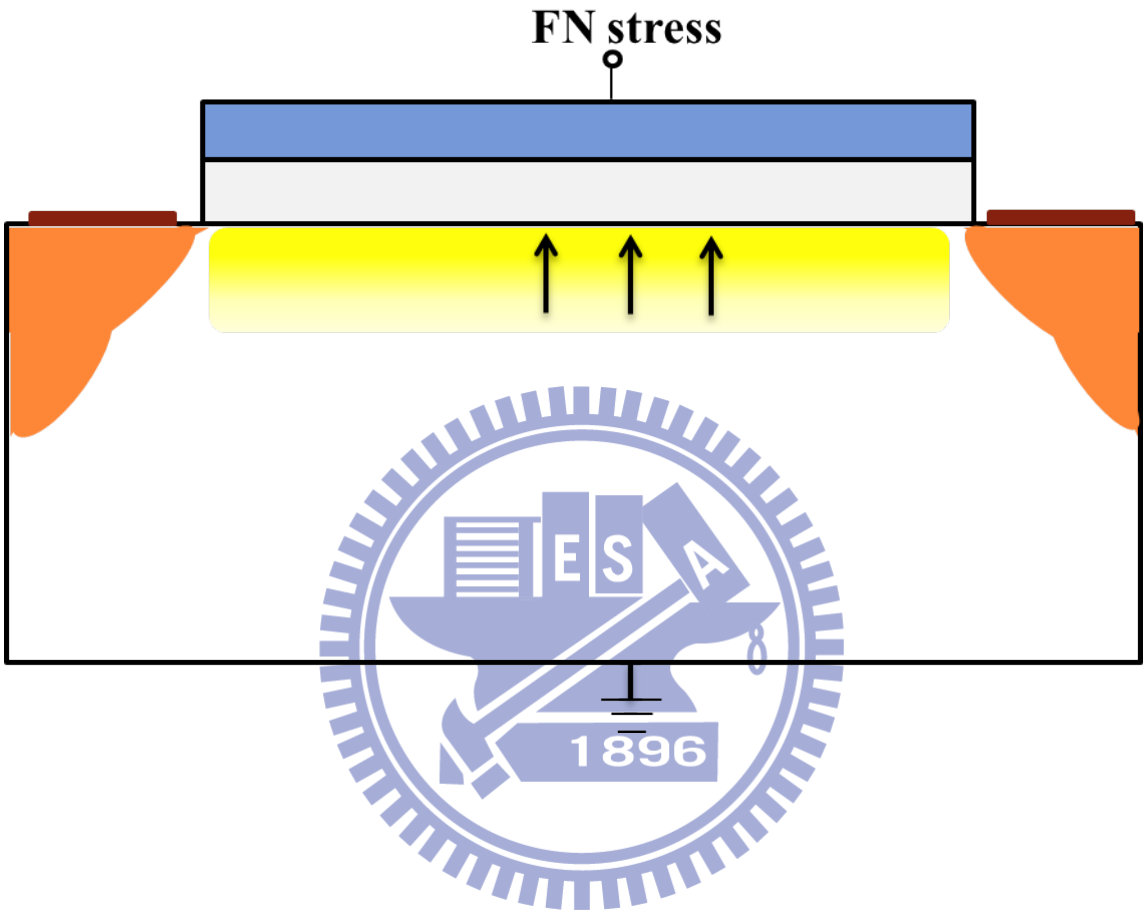


Fig. 4.18 The schematic to indicate the uniform distribution of electric field, therefore RTN-traps in this stress condition distribute uniformly in the channel.

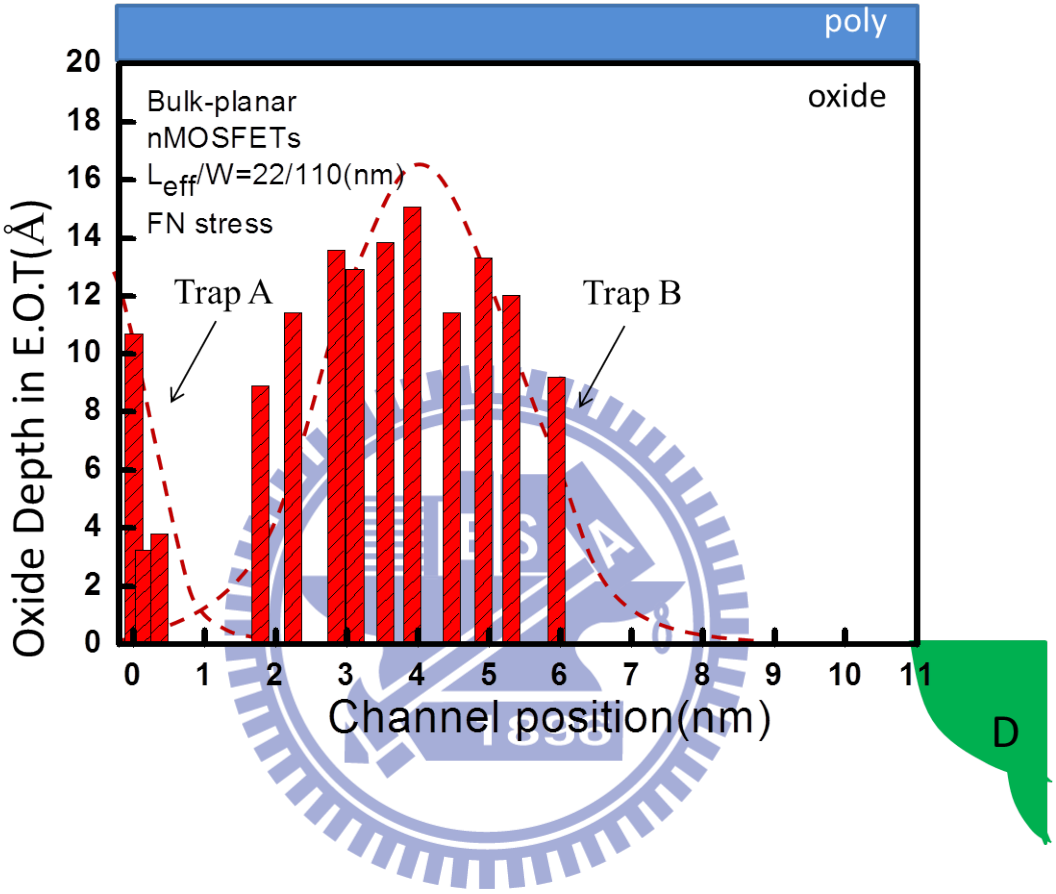


Fig. 4.19 The result of the FN stress-induced double-RTN traps in bulk planar nMOS devices, showing a bell shape. Note that this shape distributes more in the central of drain side.

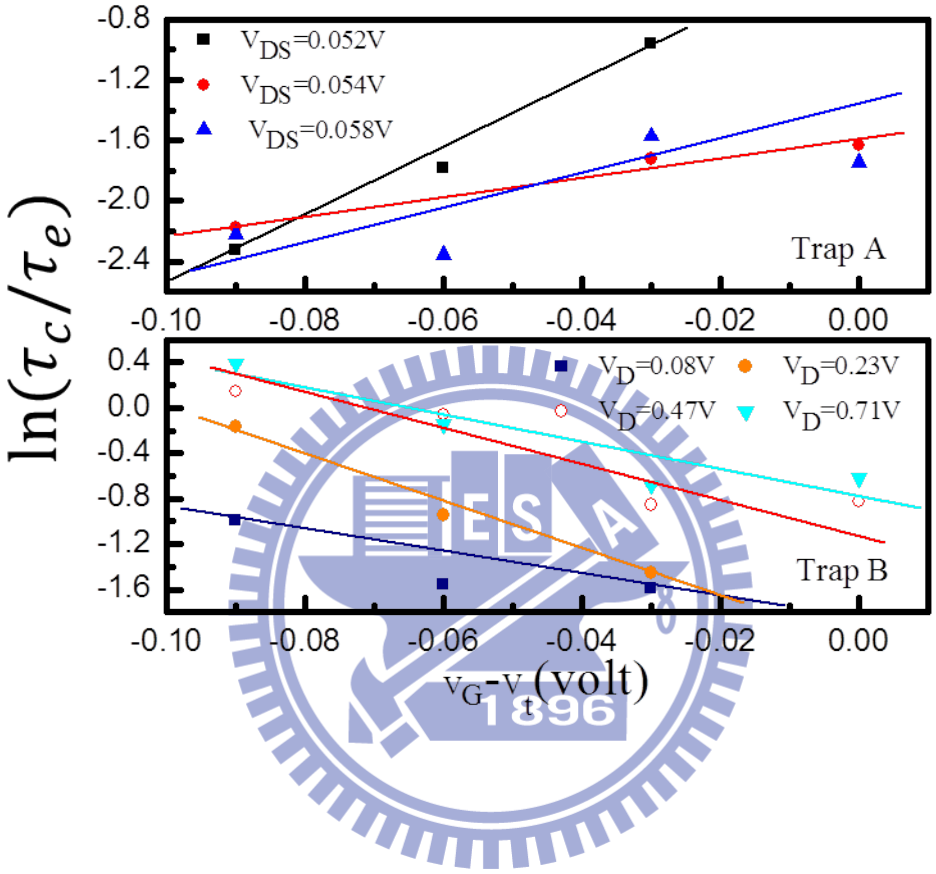


Fig. 4.20 The $\ln(\tau_c/\tau_e)$ dependency of the profiling result, ***(Top)*** showing the positive dependency for left traps, but ***(Bottom)*** the right traps shows the negative dependency.

Chapter 5

Summary and Conclusions

Recently, random telegraph noise has been regarded as a serious concern for CMOS device scaling. Due to its strong dependence on the device dimension, it is predicted that RTN amplitude will grow with device scaling more rapidly than the V_t variation caused by random dopant fluctuation. From the reported research we have already been able to extract the trap depth, and the relations between trap depth and RTN amplitude are understood. However, the lateral profile is hard to be extracted due to the severe leakage current of the small-size devices. Besides, multi-level RTN is difficult to be analyzed too.

In this thesis, a new method has been developed, and the multiple-RTN signals of the bulk trigate devices have been decoupled successfully. It was found that the process-induced RTN are generated near the poly gate for the trigate devices but near Si substrate for the planar devices, which can be explained by the fact that the interface of the poly gate and oxide layer for the trigate devices is damaged during the implantation of poly impurities. We have also extracted the cross-sections of RTN-traps and profiled the shape of traps in two dimensional directions. Gauss-like distributions were observed. Moreover, the radii of extracted RTN traps are around 1nm~3nm, consistent with the reported data.

This technique has been also utilized to investigate the impact of multi-RTN on the trigate SRAM cell and the manipulation of positions of RTN traps. In this study, stress-induced RTN traps is observed indeed while SRAM switching, and we also have found that the multiple levels of RTN will cause multiple-level transitions of butterfly curves for SRAM, which suppresses RSNM window severely. Moreover, multi-RTN will induce V_t-shift and may directly fail the transition of SRAM. This is a newly RTN-induced failure mechanism of the trigate SRAM. In addition, we applied this profiling method to manipulate the different trap positions under different stress conditions. By utilizing different stress methods, we have controlled the RTN-traps position successfully near the drain edge, in the middle of the channel, and in the region between the middle of the channel and the drain edge. These results will also be able to explore a new scenario of the discrete-bit storage of SONOS memory with various kinds of traps which are important to the understanding of the memory reliability.

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