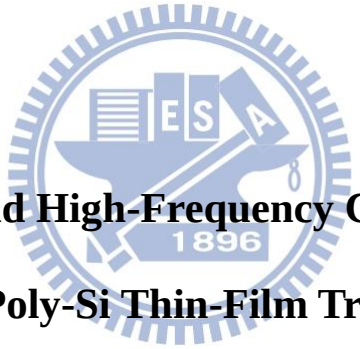
國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

N 型多晶矽薄膜電晶體元件製作與高頻特性分析



Fabrication and High-Frequency Characterization of N-type Poly-Si Thin-Film Transistors

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黃調元 博士

中 華 民 國 一 〇 一 年 九 月

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摘要

本篇論文中，吾人製作N 型薄膜電晶體元件並研究其高頻特性。高頻特性容易受到寄生效應的影響，因此降低寄生效應為特性好壞的主要關鍵。此薄膜電晶體使用了矽化鎳來降低源極、汲極和閘極的接觸電阻，另外也利用了過度曝光與光阻微調技術微縮了閘極的長度來改善高頻特性。我們還發現在多指型閘極結構中，雙重微影成像技術容易造成閘極長度的誤差，使得在關閉狀態時電流會傾向從較短的閘極長度處漏走。

此外，我們成功的藉由小訊號模型萃取出小訊號參數，由 S 參數比較模擬與量測結果，證實了小訊號模型的正確性。與單一閘極結構的小訊號參數相比，我們可以發現在多指型閘極結構中的寄生電阻會變小，寄生電容會增加，但整體來說對改善截止頻率與最大震盪頻率還是有利的。雖然外部阻抗很大而且可能會影響到實際的交流性能，但是由模擬結果證實是可信的。歸一化量測值與模擬結果做比較，可明顯發現兩者趨勢是相符的。

Fabrication and High-Frequency Characterization of N-type Poly-Si Thin-Film Transistors

Student: **Ting-Yao Lin** **Advisors:** **Dr. Horng-Chih Lin**
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Abstract(English)

In this thesis, we have fabricated n-type poly-Si thin-film transistors (TFTs) and studied their high frequency characteristics. High frequency characteristics are affected easily by the parasitic components, hence reduction of these components is essential. Resistances of source, drain, and gate are reduced with the aid of Ni silicidation technique in this work. To effectively shrink the gate length, we used both over-exposure and photoresist-trimming techniques to shrink the dimension of the PR patterns. These actions are helpful in improving the high frequency characteristics. However, we found the fluctuation in the dimensions of the interdigital poly-Si gate patterns fabricated by double-pattering process is significant. The anomalously

shortened gate lengths in the interdigital gate structures tend to increase the off-state current.

We've also successfully extracted the small-signal parameters by using a small-signal model. The simulation results of S parameters agree well with the measured data, confirming the accuracy of the small-signal model. As compared with the device with single-gate pattern, the values of parasitic resistances become smaller and the values of parasitic capacitances increase in the interdigital gate structure. But it is still beneficial for improving cut-off frequency and maximum oscillation frequency with the interdigital gate structure. Although the extrinsic resistances are large and may affect the practical ac performance, the analysis is confirmed with the simulation results and proved to be reliable. From both the normalized data and the comparison of the experimental results with the simulation, it is observed that the trends of calculation agree well with the measurements.

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這個致謝我遲遲拖到了口試結束的今天才下筆，這是因為到了今天，碩士生涯才算是完整的結束，我的文筆不好，或許沒有辦法完整傳達我所有的想法，卻有著我最深的感動與不捨，這兩年來要感謝的人很多，絕對不能只謝天就好。

我最感謝的莫過於指導我碩士生涯的兩位指導教授 林鴻志 教授及 黃調元教授，包容我在研究上的不成熟。林老師不只給我在論文上面的指導，給我正確的研究方向，也常常提醒我，不管是現在身為研究生或是之後身為研究人員，在做研究時面對困難應有的態度。黃老師除了在半導體領域上有著專業及寬廣的知識，最讓我印象深刻的就是黃老師的深不見底的中文造詣和陽光般的笑容，看到老師的笑容，彷彿心情都好了起來。

能夠完成此論文還要感謝口試委員楊文祿教授與陳坤明博士的指教，讓我更清楚研究上的缺點以及疏失，對本論文有更深的了解，當然林老師和黃老師對於此論文內容以及英文文法十分嚴謹，幫忙缺乏英文論文寫作經驗的我能夠交出一份漂亮的碩士論文。

在 ADTL 這個實驗室，認識了很多人，不管是在研究上、生活上，都給我莫大的幫助。蔡老大總是很用心的帶我做研究，不厭其煩的回答我一些蠢問題，在製程上的經驗非常老到，幫我避開了很多會在製程上遇到的問題，省了很多時間，雖然隨著我們越來越熟，你充滿色彩的笑話也常讓我無法接話，不過衷心覺得有你真好，另外撇開幽默感不說，你真的是個蠻不錯的男人。阿民雖然早我們一步畢業，無法陪我們到最後，但感謝你在模擬和電性上的指導，聽說你好像有看好我，不過我好像讓你失望了。阿毛和馬腳總是在實驗室裡唱雙簧，見識到你們獨特的幽默，也在我研究遇到困難時，給了我很多不同的想法與意見，也感謝你們為了實驗室的大家切了很多 FIB，那真的是一個費神又費時的苦工，你們的付出，大家都有目共睹。剛到實驗室時，發現嘉文學長是我大學同校的學長，讓我有點受寵若驚而且額外親切，嘉文學長對於研究與英文的堅持，是我應該要去學習的，另外嘉文學長的冷幽默也是一絕。克慧學姊也常給我一些在實驗與量測上的意見，還有傳授一些小撇步。委屈阿莫常常跟這我們這屆小碩班一起瘋一起鬧，不過也因為這樣我們的感情很 close 啦(自以為)!看著你常在開口第一句就說好餓喔!好脹喔!也漸漸習以為常，但是實驗要做，身體也要顧啊!阿哲哥真的身藏不露，除了桌球打得好外，有幸看到你帶學弟做實驗能在暑假就有成果，實在是神人等級。管金儀學長，ADTL 是個不錯的實驗室，歡迎你加入，請好好享用。

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包交通實在是太令人感動了。乾媽一號彭彭無理頭的搞笑，為實驗室帶來了不少歡笑，以及乾媽二號曉惠正妹常常帶好吃的給實驗室的大夥兒吃，兩位合體後的 hp 連線，行動力讓我很畏懼，砲火更是不同凡響，讓人無力招架。坐在乾媽三號仙女姐姐旁邊兩年，都覺得我受到仙氣的影響，再加上你的鼓勵，讓我有了很多做實驗的動力和正面的想法。

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謹以此論文獻給關心我、愛我的每個人。

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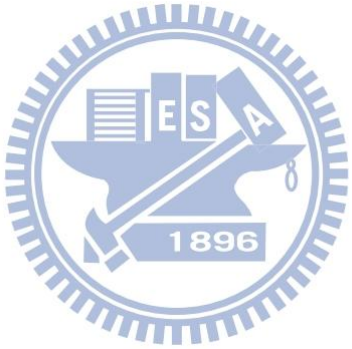

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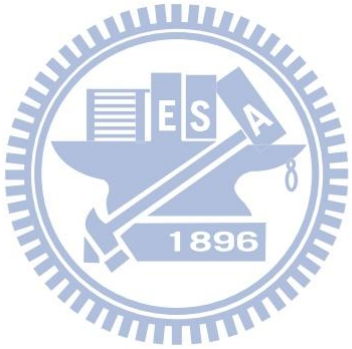


Chapter 1

Introduction

1-1 Overview of Thin-Film Transistor Technology

Dr. Paul K. Weimer invented and contributed to the development of thin-film transistors (TFTs) as he was employed at Radio Corporation of America in Princeton in 1962 [1.1]. In this work cadmium sulfide was used as the active channel, while source, drain, and gate were made of metals [1.1]. Since then several alternative materials have been explored and used as the channel layer, such as hydrogenated amorphous silicon (α-Si:H) [1.2], and polycrystalline silicon (poly-Si) [1.3] [1.4].

The α-Si TFTs were developed much earlier than the poly-Si counterparts because the α-Si:H material can be deposited on glass substrates at a low temperature with plasma-enhanced chemical vapor deposition (PECVD). However, α-Si TFTs are not feasible for high-performance circuits because of the low carrier mobility which is typically less than $1cm^2/V \cdot s$. Until Fa and Jew developed the first poly-Si TFT [1.2], the demerits of α-Si TFTs were not appropriately addressed. Electron mobility of poly-Si TFTs can reach as high as $260cm^2/V \cdot s$ [1.3] [1.4]. However, high-temperature

processes are incompatible with the manufacturing of the liquid-crystal displays (LCD) with low-cost glass substrates, hence, low-temperature polycrystalline silicon (LTPS) techniques are developed. LTPS TFTs not only cost less, but also make the resolution of active-matrix liquid-crystal displays (AMLCDs) higher [1.5]. However, the occurrence of the kink effect may limit the application to analog circuits [1.6].

The grain size of poly-Si is one of the major factors influences the carrier mobility. The effective mobility increases as the grain size is expanded. The grain size of as-deposited poly-Si is smaller than that with the poly-Si re-crystallized from α-Si. There are 3 popular methods for re-crystallization, including solid phase crystallization (SPC), excimer laser crystallization (ELC) and metal-induced lateral crystallization (MILC). However, properties of the re-crystallized materials are strongly dependent on the technique employed and the conditions used in the process. Firstly, the SPC process usually takes longer time, roughly 24-48 hours if processed under 600℃. This requirement certainly affects the throughput and thermal budget. Secondly, the ELC process takes much less time to fabricate, and the substrate does not have to be subjected to high temperature environment. However, the surface of the re-crystallized film is not smooth at all and protruding regions appear near the grain boundaries [1.7]. Lastly, the MILC process which adds a little metal into α-Si is also able to maintain the processing temperature below 600℃ and thus reduces thermal

budget [1.8]. Usually poly-Si films produced with ELC or MILC schemes are with much larger grains as compared with those produced with SPC.

Nowadays, LTPS TFT has the potential to become a widely applied technique for related applications. For instance, AMLCD [1.6][1.9], metal-oxide-nitride-oxide-polysilicon (MONOS) [1.10], and fingerprint scanning array [1.11].

1-2 Overview of Radio Frequency Techniques

With the thriving in technology development, wireless transmission among electronics gears doubtlessly prevails throughout our daily life. In early days the transmission was mostly limited to the audio communication. Nowadays, accessing data of other formats like texts or video images and a much larger capacity of data transmission has been greatly demanded. Thus, speeding the speed of transmission is a paramount issue to put focus on.

Over past decades, transistors have been widely used and continually developed due to its mature technique. Moreover, operation frequency of the circuits continuously improves thanks to the scaling down of devices. Many kinds of high-performance circuits constructed by transistors are available, such as filter, mixer,

divider, phase-locked loop (PLL), voltage-controlled oscillator (VCO), and low-noise amplifier (LNA). Among them, the PLL is used for precisely controlling and automatically modulating frequency [1.12]. VCO is another kind of oscillation circuits which controls the oscillation frequency with voltage [1.13]. The purpose of a LNA is to receive signal by antenna with high gain and sensitivity. In order to reduce loss, LNA is usually put in the front of antenna [1.14].

Major factors for improving the electrical performance of transistors applied for radio frequency (RF) circuits include high electron mobility, high transconductance, high current drive, low parasitic resistance, low parasitic capacitance, and high frequency response characteristics. By achieving those mentioned above, we could improve cut-off frequency (f_t) and maximum oscillation frequency (f_{max}). By properly shrinking the dimensions of TFTs, the devices' RF performance is expected to improve significantly and becomes feasible for RF IC application. Additionally, the Si TFTs fabricated on a flexible polymer substrate for construction of large-area RF systems for applications in aerospace, such as phased array antennas for communication, remote sensing, and surveillance [1.15]. The system-on-panel (SoP) can be used to upgrade the displays and advance the function of many products. For example, it could be integrated into a cell phone which is capable of doing transaction by electric wallet or RF identification (RFID) [1.16].

1-3 Overview of Silicide Technology

The major metal silicides adopted today are developed from titanium (Ti), cobalt (Co), and nickel (Ni), in that order. There materials offer a few advantages, such as low resistivity, low contact resistance, good process compatibility, and can be formed in a self-aligned manner. However, there also exist a few issues which have been studied in numerous publications, like bridging, stress, thin film agglomeration, etc.

Ti-salicide was developed as the first salicide material. The early issue is the severe bridging occurring over spacers due to lateral diffusion of Si atoms which react with Ti on the spacers. The formed silicide forms conduction bridges connecting the gate and source/drain regions. Applying a two-step annealing in N_2 is capable of overcoming the problem [1.17]. Specifically, the first step is performed at a relative low temperature (650-700℃) to form C49 $TiSi_2$ with higher resistivity. In this stage bridging would not occur due to the low temperature. Then a wet etching is employed to selectively remove the un-reacted Ti film on the wafer surface, including that on the spacers. The second anneal is then done at a higher temperature (> 800℃) to transfer the C49 $TiSi_2$ into C54 $TiSi_2$ [1.18]. But the problem of a large thermal budget still exists. Besides, the sheet resistance of silicide increases anomalously when the devices are scaled down (< 0.25μm). This phenomenon is called the narrow-line-width effect [1.19] and limits the Ti salicide from being implemented in

sub 0.25 micron-node.

Co-silicide succeeded Ti-silicide at 0.18um technology node and beyond. To avoid bridging, a two-step anneal procedure is still used to form low-resistivity $CoSi_2$ at a high temperature (> 700℃) from high-resistivity CoSi of the first annealing done below 500℃ [1.20]. Before the aforementioned process, a TiN capping layer is usually deposited onto the Co layer and serves as a barrier to avoid oxidation during the following annealing in N_2, because Co-salicide process is sensitive to contamination of the ambient, especially oxygen [1.21]. The major disadvantages of Co-salicide are the narrow-line-width effect (occurring as line width smaller than 100nm) and a mass of Si consumption.

The Ni-salicide technology was proposed in 1991. The NiSi salicide for 0.4μm-CMOS exhibited nice characteristics [1.22]. The advantages of Ni-silicide include less narrow-line-width effect, lower resistivity, lower contact resistance, lower thermal budget, and less Si consumption [1.23][1.24]. Ni-salicide usually demands only one step of anneal at a temperature ranging between 350℃ and 700℃ to form low-resistivity NiSi. At such a temperature, Ni-salicide can be free from the bridging issue. Besides, doping with 5% Pt-incorporation was found to increase the phase transformation temperature [1.25]. From the application point of view, Ni-salicide process developed in the early 1990s has been introduced in nano-scale technology

nodes owing to the fact that several properties mentioned above are superior to those of Ti- and Co-salicide technologies.

1-4 Motivation

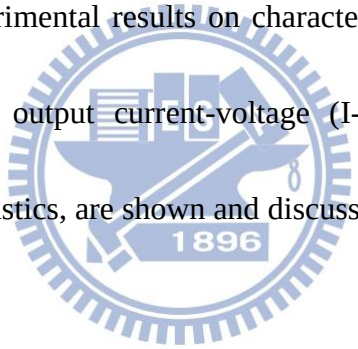
Displays have been widely-used in our daily life and it wouldn't surprise us that the hot products recently discussed and focused are the flat-panel types. Looking inside them, TFTs are usually used as the switch of pixels in the AMLCDs. Besides, the performance of TFTs has greatly improved in recent years and should be capable of serving as the basic building blocks on ICs manufactured on the panel of displays. For SoP purpose, ICs of different functions, like central processing unit (CPU), memory, and RF, are demanded to be integrated on the same panel. Nonetheless, few works are reported on studying the RF characteristics of poly-Si TFTs, owing to their relatively low mobility as compared with the bulk Si counterparts, as well as the rather large device size in modern manufacturing (e.g., channel length > 3μm). However, considering the low-temperature processing and the capability of being manufactured on glass or flexible substrates, this subject is worthy of exploration. Several ways can be adopted to improve the RF performance of poly-Si TFTs. One is to scale down the channel length which can readily increase the on current and the transconductance. Reduction of parasitic source/drain series resistance is another key

work. In this work we adopt these approaches in the device fabrication and study the RF characteristics of the fabricated devices.

1-5 Organization of Thesis

In Chapter 2, the process for an n-type poly-Si TFT is described and evaluated. Utilization of photoresist-trimming techniques for device fabrication is stated. The characterization scheme and measurement setup are also introduced

In Chapter 3, the experimental results on characterizing the fabricated devices, including the transfer and output current-voltage (I-V), small-signal parameters extraction, and RF characteristics, are shown and discussed.



Chapter 2

Device Fabrication and Measurements

2-1 Device structure and Process Flow

The process scheme is shown in Fig. 2.1. First of all, a wet oxide with thickness of 1000 nm was formed on a six-inch silicon substrate as the buried oxide. An amorphous silicon (α-Si) layer was then deposited with low pressure chemical vapor deposition (LPCVD) to serve as the channel layer as shown in Fig. 2.1 (a). The channel thickness was either 50 or 100nm. Solid phase crystallization (SPC) method, which was performed at 600℃ in N_2 ambient for 24 hours, was then used to transform the film from α-Si into poly-Si in order to promote the electron mobility. The poly-Si layer was then defined to form active regions by an I-line lithographic and subsequent anisotropic etching steps, as depicted in Fig. 2.1 (b). LPCVD tetraethylorthosilicate (TEOS) oxide with thickness of 10nm was deposited as the gate oxide. Next, a 100nm *in-situ* phosphorus doped poly-Si was deposited by LPCVD. Subsequently a 25nm TEOS oxide was deposited to serve as the hard mask material by LPCVD as shown in Fig. 2.1 (c). Afterwards, the gate was defined by a photolithographic step and etched by reactive ion etching (RIE) as shown in Fig. 2.1 (d). A 20nm TEOS oxide layer and

a 15nm nitride layer were deposited, and then etched by RIE for forming sidewall spacers as shown in Fig. 2.1 (e). A 15nm-thick nickel layer was deposited and then thermally processed at 450℃ by rapid thermal anneal (RTA) in N_2 ambient to form Ni-silicide on source, drain, and gate regions. Afterwards source/drain regions were doped by a self-aligned implant with P_{31}^{+} ions with energy of 10keV and dose of $5\times10^{15}cm^{-2}$ as shown in Fig. 2.1 (f). A 500nm-thick PECVD oxide layer was deposited to act as the passivation layer in order to prevent the penetration of humidity and impurity. Finally, a metallization process was performed to form metal pads.

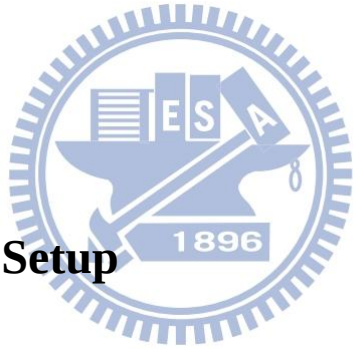
To effectively shrink the gate length, we used over exposure and photoresist-trimming techniques to scale down the dimension of the PR patterns. The difference of patterned PR lines with L_{mask} of 0.25μm located at different dies distributed on a wafer before and after trimming was inspected with the In-line scanning electron microscope (SEM) and the results are shown in Figs. 2.2 and 2.3, respectively. In this thesis, L_{mask} is the designed length of the structures on the mask, and L_{gate} is the practical value measured with an In-line SEM. The results of poly-Si line patterns with trimmed PR with L_{mask} of 0.25μm measured from five dies at different location of a wafer are shown in Fig. 2.4. The measured L_{gate} ranges from 0.185 to 0.238μm.

But the trimming method was found to have feet of clay, and the trimmed PR would collapse when L_{gate} is further shortened. In this work we thus focus on devices with channel length equals to or larger than 0.2μm. Cross-sectional transmission electron microscopy (TEM) image of a n-type TFT is shown in Fig. 2.5. The unexpected voids seen in the picture were formed during the preparation of the TEM sample by focus ion beam.

In order to promote f_t, we hope hope that the fabricated devices provide high transconductance. The feasible methods to increase transconductance include the decrease in gate length, increase in gate width, and implementation of self-aligned silicidation procedure to reduce the parasitic resistance. Interdigital gate-finger design shown in Fig. 2.6 is adopted to avoid the current crowding phenomenon in the device.

In this work, in addition to the single patterning (SP) method mentioned above to form the poly-Si gates, an additional split of samples with the poly-Si gates patterned with a double patterning (DP) technique [2.1] was also fabricated and characterized. However, because of the issues resulted from the overlay capability of the I-line stepper and the dimension control of patterns during the manufacturing of the two reticles used for the DP process, severe fluctuation in the dimensions of the final poly-Si gate patterns in the interdigital gate structures is observed. In-line SEM images of the gate patterns formed with the DP and SP techniques are individually

shown in Figs. 2.7 (a) and (b). Severe gate pattern fluctuation can be identified in Fig. 2.7 (a), while the situation shown in Fig. 2.7 (b) is much better. The cumulative data of the measured L_{gate} extracted from the two splits of devices with nominal gate length of 0.22μm are shown in Fig. 2.8. In this picture, the measured data range from 0.21 to 0.238μm for the SP split, while the distribution for the DP split is widened from 0.171 to 0.328μm. The different outcome would draw impacts on the device characteristics that are addressed in the next chapter. In this work the RF characterization focuses on the fabricated devices with SP technique for the sake of superior and more uniform device characteristics.



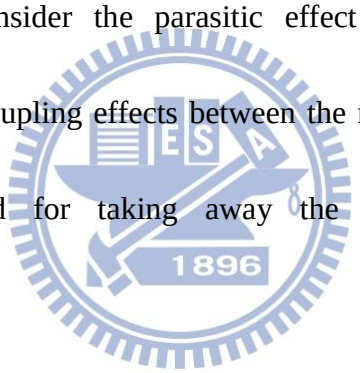
2-2 Measurement Setup

The electrical characteristics of poly-Si TFTs were characterized by an HP4156 semiconductor parameter analyzer. From the I-V curves measured, the characteristics of poly-Si TFTs, such as subthreshold swing (SS), threshold voltage (V_{th}), leakage current, on/off current ratio, driving current, etc., can be extracted.

The S parameters of poly-Si TFTs were characterized by an HP8510C network analyzer. The measured S parameters were then used to acquire additional properties such as f_t, f_{max}, Y parameters and Z parameters, etc.

2-3 De-embedded Process

In order to precisely measure the electrical parameters from devices, two steps for correction procedure must be followed. First step is to calibrate the measurement system. It is made by referring to the ideal condition and real outcome. The calibration techniques, such as short-open-load-through (SOLT), through-reflect-line (TRL), line-reflect-match (LRM), are usually employed to define S parameters on the reference plane at the probe tip and promote the accuracy of the measurements [2.2]. Secondly, we have to consider the parasitic effect of the bonding pads and interconnect, because the coupling effects between the metals are significant at high frequency. The step used for taking away the parasitic effects is called "de-embedding".



In this work, we use the SOLT method to calibrate and a two-step de-embedding procedure to remove the parasitic effects via open test fixture and short test fixture. The SOLT calibration models include short circuit inductance, open circuit capacitance, matching load, and length of the through line [2.3]. The equivalent circuit diagram shown in Fig. 2.9 includes the parallel parasitic capacitances ($Y_{p,1}$, $Y_{p,2}$, $Y_{p,3}$) and series parasitic impedances ($Z_{p,1}$, $Z_{p,2}$, $Z_{p,3}$) surrounding the transistor. The open test fixture and the diagram of the equivalent circuit equipped with parallel parasitic capacitances are shown in Figs. 2.10 (a) and (b), respectively. The short test

fixture and the diagram of the equivalent circuit equipped with serial parasitic impedances and parallel parasitic capacitances are shown in Figs. 2.11 (a) and (b), respectively. Firstly, the matrix of parallel parasitic capacitances and serial parasitic impedances is respectively calculated by a simple mathematics presented in Eqs. 2.1 and 2.2,

Y_{open}: Y-parameter matrix is measured from the open test fixture.

Y_{short}: Y-parameter matrix is measured from the open test fixture.

$Y_{transistor}$: Y-parameter matrix is measured from the transistor.

Y_{DUT}: Y-parameter matrix is measured from the transistor with parasitic effect.

$$Y_{open} = \begin{bmatrix} Y_{p,1} + Y_{p,3} & -Y_{p,3} \\ -Y_{p,3} & Y_{p,1} + Y_{p,3} \end{bmatrix}, \tag{2.1}$$

$$\left(Y_{short} - Y_{open}\right)^{-1} = \begin{bmatrix} Z_{p,1} + Z_{p,3} & Z_{p,3} \\ Z_{p,3} & Z_{p,1} + Z_{p,3} \end{bmatrix}, \tag{2.2}$$

Then, the actual transistor's Y-parameter matrix without parasitic effects could be obtained using Eq. 2.3:

$$Y_{trans} = \left(\left(Y_{DUT} - Y_{open}\right)^{-1} - \left(Y_{short} - Y_{open}\right)^{-1}\right)^{-1}, \tag{2.3}$$

Using this two-step procedure the influence of parasitic effects can be lifted and therefore the accuracy of the measurements is assured [2.4].

Chapter 3

Results and Discussion

3-1 Basic Electrical Characteristics

In this work, we have fabricated symmetric n-type TFTs with various channel thicknesses and widths. Figures 3.1 and 3.2 show the transfer and output characteristics of n-type TFTs with nominal gate length of 0.22μm and various gate widths of 8 and 64μm, respectively. The devices were patterned with the SP method mentioned in last chapter. The former device contains only one gate stripe, while the latter is of interdigital type with eight gate stripes connected together. The on-to-off current ratio (I_{on}/I_{off}) at V_d = 0.1V is about 10^7, and the maximum transconductance (g_m) is about 0.68mS at gate voltage of 3V in saturation region for the device with gate width of 8 μm as shown in Fig. 3.1 (a). Figure 3.2 (a) shows that the I_{on}/I_{off} is about 10^7 at V_d = 0.1V and the maximum g_m is around 6 mS at gate voltage of 2.6V with gate width of 64 μm. The output characteristics with different gate widths are shown in Fig. 3.1 (b) and 3.2 (b). Certainly, the more the gate width increases, the more I_{on} and I_{off} gain. However, the currents in Fig. 3.2 (b) are not exactly 8 times higher than that shown in Fig. 3.1 (b), indicating the effect of fluctuation of the gate

dimensions. Nonetheless, the deviation from the dependency of the number of gates is not huge as compared with the case with DP technique which will be shown in the next paragraph.

Table 3.1 summarizes the current drive and g_m of n-type TFTs with various channel thicknesses and widths. Compared with channel thickness of 500Å , the value of I_d and g_m become larger, in channel thickness of 1000Å structure, owing to the effect of grain size of the channel thickness. The grain size is difference at different channel thickness. The grain size is larger with channel thickness of 1000Å .

Figure 3.3 shows the transfer characteristics of devices fabricated with SP and DP techniques at V_d = 0.1V. The SEM images of the two devices are shown in Fig. 2.7 and as mentioned in last chapter that the patterned gates show larger fluctuation with the SP method. Summary of the measured gate length of the eight gate fingers of the two devices with nominal gate length of 0.22μm is listed and compared in Table 3.2. As can be seen in the Table that the finer gate patterns of the DP device can be even shorter than 0.22μm. These “short” gates tend to increase the off-state current owing to short channel effects, therefore the DP device exhibits an I_{off} three orders of magnitude higher than that of the SP one at V_d = 0.1V. Other major impact resulted by the fluctuation in gate length is the degradation in the g_m value, as shown in the figure. Consequently the RF characteristics would be seriously affected.

3-2 Small-Signal Modeling

3-2-1 Modeling Setup Flowchart

The flowchart of complete small-signal model setup strategy [3.1] is shown in Fig. 3.4. Following the flowchart, a complete small-signal model is established successfully for our n-type poly-Si TFTs. In the next section, we will extract extrinsic and intrinsic parameters step by step and compare them with the results of simulation.

3-2-2 Extrinsic Parameter Extraction

The small-signal equivalent circuit of an n-type TFT is shown in Fig. 3.5. First, the parasitic resistances (R_g, R_d, R_s) were extracted through the cold model [3.2]-[3.5]. The small-signal equivalent circuit was transformed into the cold model when V_{gs} = V_{ds} = 0V. This bias condition causes the voltage-dependent current generator to become zero and the output resistance (r_o) to become infinite. Different from the bulk MOSFET without substrate loss, partial depletion in the channel of the device necessitates the consideration of the non-quasi-state effect [3.6]. The coupling path formed between the source and drain through the quasi-neutral body region causes the resistances expression to become frequency dependent. Cross-sectional view of an n-type TFT with partial depletion under the zero condition and the equivalent circuit model are shown in Figs. 3.6 (a) and (b), respectively. The neutral-body coupling path

is constituted by the source-side and drain-side junction capacitances ($C_{j,bs}$ and $C_{j,bd}$), and body conductances (G_{bs} and G_{bd}) [3.4][3.5]. Based on the equivalent circuit, the parasitic resistances of the cold model can be measured by the real component of Z parameters, which can be written as

$$\mathrm{Re}(Z_{11} - Z_{12}) = R_g + \frac{A_g}{\omega^2 + B}, \tag{3.1}$$

$$\mathrm{Re}(Z_{12}) = \mathrm{Re}(Z_{21}) = R_s + \frac{A_s}{\omega^2 + B}, \tag{3.2}$$

$$\mathrm{Re}(Z_{22} - Z_{12}) = R_d + \frac{A_d}{\omega^2 + B}, \tag{3.3}$$

where A_g, A_s, A_d, and B are constant values at fixed bias. The existence of neutral body may cause the parasitic resistances to become frequency dependent. It can explain why the resistance-vs.-frequency curves are not the same as those for conventional MOSFETs. When the frequency approaches infinity, the parasitic resistance components can be extracted. After the extraction of extrinsic parameters, this can be carried out using the following procedure as shown in Fig. 3.7 [3.3]. First, the S parameters of the device are measured as shown in Fig 3.7 (a). The S parameters are then transferred to Z parameters by subtracting R_g, R_d and R_s which are in series, as shown in Fig 3.7 (b). The Z parameters are further transferred to Y parameters and the matrix of the intrinsic admittance can be determined.

3-2-3 Intrinsic Parameter Extraction

The small-signal model of intrinsic Y parameters is shown in Fig. 3.8. The analysis is based on the definition of Y parameters and it can be described as below:

$$Y_{11}^{i} = j\omega\left(C_{gs} + C_{gd}\right), \tag{3.4}$$

$$Y_{12}^{i} = -j\omega C_{gd}, \tag{3.5}$$

$$Y_{21}^{i} = g_m - j\omega\left(C_{gd} + g_m\tau\right), \tag{3.6}$$

$$Y_{22}^{i} = \frac{1}{r_o} + j\omega\left(C_{ds} + C_{gd}\right). \tag{3.7}$$

The intrinsic parameters of small-signal model as a function of their Y parameter, Y^{i}, are shown below:

$$C_{gd} = -\frac{\mathrm{Im}\left(Y_{12}^{i}\right)}{\omega}, \tag{3.8}$$

$$C_{gs} = \frac{\mathrm{Im}\left(Y_{11}^{i}\right)+\mathrm{Im}\left(Y_{12}^{i}\right)}{\omega}, \tag{3.9}$$

$$C_{ds} = \frac{\mathrm{Im}\left(Y_{12}^{i}\right)+\mathrm{Im}\left(Y_{22}^{i}\right)}{\omega}, \tag{3.10}$$

$$r_o = \frac{1}{\mathrm{Re}\left(Y_{22}^{i}\right)}, \tag{3.11}$$

$$g_m = \mathrm{Re}\left(Y_{21}^{i}\right), \tag{3.12}$$

$$\tau = \frac{\mathrm{Im}\left(Y_{12}^{i}\right)-\mathrm{Im}\left(Y_{21}^{i}\right)}{g_m\times\omega}. \tag{3.13}$$

The r_o and g_m can be extracted directly for real part of Y parameters. The τ is the slope

of the imaginary part of Y parameters versus frequency multiplied by g_m. The cross section of an n-type TFT with the corresponding parasitic parameters of small-signal equivalent circuit is shown in Fig. 3.9.

3-3 Experiment and Simulation Analyses

Theoretically extrinsic elements are bias-independent. When V_{ds} = 0V and V_{gs} < V_{th}, the TFT is in the cut-off state. In the cut-off state, as shown in Fig. 3.10, the real parts of Z parameters for a device with channel thickness of 100 nm (L = 0.22μm, W = 8μm) operated at V_{ds}/V_{gs} = 0/0V and V_{ds}/V_{gs} = 0/-1V are shown as a function of frequency. The results decrease with increasing frequency and approach constant values (i.e., R_d, R_s, and R_g), as predicted by Eqs. (3.1)-(3.3). Given the condition of cut-off state, the values of extrinsic resistances gradually become stable as the frequency increases. We also use this scheme to determine the extrinsic resistances for a device with channel thickness of 50 nm (L = 0.22μm, W = 8μm) at V_{ds} = V_{gs} = 0V and the results are shown in Fig. 3.11. It is found that the extrinsic parameters are R_g = 120.33Ω, R_d = 129.41Ω, and R_s = 8.182Ω.

After subtracting extrinsic parameters, the intrinsic Y parameters can be calculated. Intrinsic elements are theoretically bias-dependent and frequency-independent. The extraction of the intrinsic capacitances is based on Eqs.

(3.8)-(3.10). The imaginary part of the experimentally measured Y parameters linearly increases with angular frequency as shown in Fig. 3.12 The imaginary part of Y parameters increases with increasing frequency and the slopes of the curves approach constant values (i.e., C_{gs}, C_{ds}, and C_{gd}), as predicted by Eqs. (3.8)-(3.10). The g_m and r_o as a function of angular frequency are shown in Fig. 3.13. Since the variation of g_m with angular frequency is small, we can determine it as the mean value in low frequency range, e.g., < 10GHz. From Eq. (3-11), the r_o is inversely proportional to $\mathrm{Re}(Y_{22}^i)$ and $\mathrm{Re}(Y_{22}^i)$ usually is very small. Thus, a small variation in $\mathrm{Re}(Y_{22}^i)$ will cause a dramatic change in r_o. The following item determined from the imaginary part of the experimentally measured Y parameters, $\mathrm{Im}(Y_{12}^i) - \mathrm{Im}(Y_{21}^i)$, is divided by g_m (or $\mathrm{Re}(Y_{21}^i)$) and shown in Fig. 3.14 as a function of the angular frequency. From Eq. (3-12), the slope of the curve is τ, which indicates the mean delay time when gate bias and g_m change asynchronously. According to the above procedure we obtain the results of intrinsic parameters of the n-type poly-Si TFT (channel thickness = 500Å , L = 0.22μm, W = 8μm) including C_{gs} = 6.668fF, C_{gd} = 2.479fF, C_{ds} = 2.105fF, g_m = 0.489mS, r_o = 3663Ω, and τ = 1.314psec. Moreover, f_t is 8.074GHz and f_{max} is 11.69GHz, obtained from the measurement of S parameters as shown in Fig. 3.15.

In order to verify the accuracy of the small-signal model, we use the software "Advanced Design System (ADS)" (Agilent Technologies) to simulate and compare

with the experimental results. The frequency range is set to be from 0.2GHz to 40GHz at V_d = 2V and V_g = 4V. We apply the extracted parameters in the small-signal model to simulate and compare the outcome with measured results of S parameters in Fig. 3.16. As can be seen in the figure that the simulation results correspond well with the measured data, confirming that the small-signal model is accurate.

One thing should be noted in the above results is that R_d is obviously larger than R_s. Considering the fact that the device is symmetrical in structure, R_s and R_d should be identical. This weird trend is attributed to the layout of the test structure and the measurement scheme. The layout of the test device is asymmetrical after the de-embedding process as shown in Fig. 2.6. The error arisen during the de-embedding process is also an issue. Additionally, the grain boundary of poly-Si should also affect the resistance.

The above procedure is also applied to a device with channel thickness = 1000Å (L = 0.22μm, W = 8μm) and the results are shown in Figs. 3.17-3.20. Similar trends are observed for this device and the results are R_g = 107.93Ω, R_d = 119.932Ω, and R_s = 7.879Ω for extrinsic parameters, and C_{gs} = 7.264fF, C_{gd} = 2.26fF, C_{ds} = 2.413fF, g_m = 0.705mS, r_o = 2207Ω, and τ = 1.189psec for intrinsic parameters. The f_t is 11.159GHz and f_{max} is 15.856GHz from the measurement of S parameters at V_d = 2V and V_g = 2V, as shown in Fig. 3.21. A comparison between simulated and measured S

parameters is shown in Fig. 3.22.

Table 3.3 summarizes the small-signal parameters of the n-type poly-Si TFTs with various channel thickness and width. Broadening the gate width is expected to improve the ac characteristics. Although g_m has been improved, the values of parasitic resistance become smaller but the values of parasitic capacitance increase. The gain in resistance components is balanced but the net effect is beneficial for improving f_t and f_{max}.

Both f_t and f_{max} are bias-dependent. An example for f_t is shown in Fig. 3.23. The g_m increases with increasing V_d, leading to an improved f_t as V_d increases. Moreover, as compared with V_g, V_d is much more influential to f_t. As the extrinsic parameters (R_g, R_d, and R_s) are ignored, f_t and f_{max} can be respectively expressed as

$$f_t \propto \frac{g_m}{C_{gs}+C_{gd}}, \tag{3.14}$$

$$f_{max} \propto f_t\sqrt{r_o}. \tag{3.15}$$

Although the extrinsic resistances are large and may affect the practical ac performance, the above analysis is confirmed with the simulation results and proved to be reliable. Major small-signal parameters extracted at V_d = 2V and various V_g are shown in Fig. 3.24. The corresponding f_t and f_{max} were also measured and shown in Fig. 3.25. Figure 3.26 modifies Fig. 3.25 by normalizing the data to that measured at

V_g = 1V and compares the experimental results with the theoretical predictions made by Eqs. (3.14) and (3.15). It is observed that the trends of calculation agree well with the measurements.

Table 3.1 Summary of basic electrical characteristics of n-type TFTs with various channel thicknesses and widths.

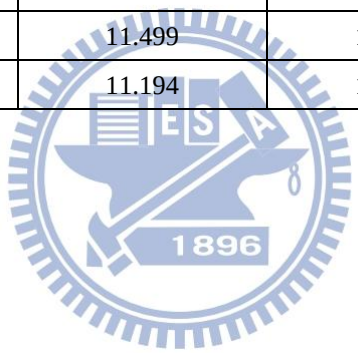
	Channel thickness = 500Å		Channel thickness = 1000Å	
	L/W = 0.22μm/8μm	L/W = 0.22μm/64μm	L/W = 0.22μm/8μm	L/W = 0.22μm/64μm
I_d,sat(mA)	2.3	23.9	3.7	33.2
g_m,sat(μS)	683	5921	843	6261
g_m,sat per width (μS/μm)	85.38	92.52	105.38	97.83

Table. 3.2 Measured dimensions of poly-Si gates patterned with SP or DP method with nominal gate length of 0.22μm.

The order of the gate in the interdigital structure from left side	DP	SP
Number 1 gate	0.185μm	0.210μm
Number 2 gate	0.260μm	0.233μm
Number 3 gate	0.182μm	0.222μm
Number 4 gate	0.253μm	0.234μm
Number 5 gate	0.174μm	0.229μm
Number 6 gate	0.259μm	0.215μm
Number 7 gate	0.178μm	0.229μm
Number 8 gate	0.260μm	0.231μm

Table 3.3 Summary of the small-signal parameters of n-type poly-Si TFTs with various channel thickness and width.

	V_d = 2V, V_g = 4V		V_d = 2V, V_g = 2V	
	Channel thickness = 500Å L/W=0.22μm/8μm	Channel thickness = 500Å L/W=0.22μm/64μm	Channel thickness = 1000Å L/W=0.22μm/8μm	Channel thickness = 1000Å L/W=0.22μm/64μm
$R_g(\Omega)$	120.33	18.25	107.93	19.68
$R_{d(}\Omega)$	129.41	13.92	119.932	15.02
$R_{s(}\Omega)$	8.182	1.092	7.879	1
C_{gs}(fF)	6.668	42.708	7.264	41.338
C_{gd}(fF)	2.479	17.777	2.26	17.756
C_{ds}(fF)	2.105	8.1	2.413	10.576
g_m(mS)	0.489	4.356	0.705	6.771
$r_{o(}\Omega)$	3663	171.891	2207	335
τ(psec)	1.314	1.043	1.189	0.893
f_t(GHz)	8.074	11.499	11.159	17.123
f_{max}(GHz)	11.69	11.194	15.856	21.515



Chapter 4

Conclusion and Future Work

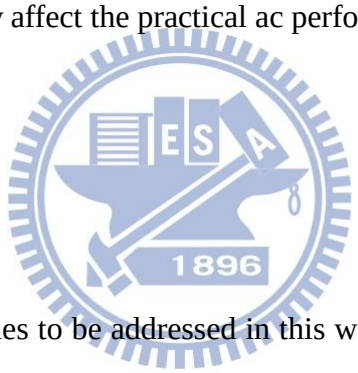
4-1 Summary and Conclusion

In this thesis, we have successfully fabricated and studied the RF characteristics of n-type poly-Si TFTs. An I-line-based DP process was developed and used in the fabrication of the devices. Resistances of source, drain, and gate were reduced with the aid of Ni silicidation technique and implant-to-silicide scheme. RF characteristics of the fabricated devices were characterized and a small-signal model was developed to extract and analyze major parameters.

The characterized devices are with either single or interdigital gate pattern. For devices with identical nominal gate length and various gate width, I_{on} and I_{off} increase reasonably with increasing gate width. However, the drain currents are not strictly proportional to the gate width, owing to the effect of fluctuation of the gate dimensions. The issue is postulated to be resulted from the poor dimension control of the patterns on the two reticles used for the DP process. Severe fluctuation in the dimensions of the final poly-Si gate patterns in the interdigital gate structures is observed. The anomalously shortened gate lengths tend to increase the off-state

current owing to the short channel effects.

We've also successfully extract small-signal parameters by small-signal model. The simulation results of S parameters agree well with the measured data, confirming that the small-signal model is accurate. We have also studied the variation of parameters at different condition. As compared with the device with single-gate pattern, the values of parasitic resistance become smaller but the values of parasitic capacitance increase in the interdigital gate structure. In addition, the extrinsic resistances are large and may affect the practical ac performance.

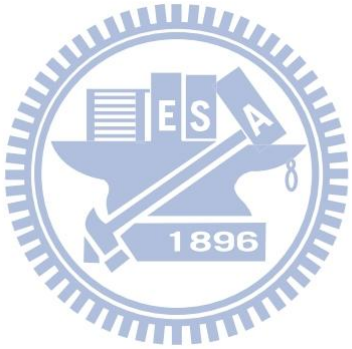


4-2 Future Work

There remain some issues to be addressed in this work. It has been demonstrated that the parasitic components would affect RF characteristics and thus it is essential to reduce these parasitic components. Further optimization of the silicidation process can help. Adoption of low-resistance metallic gate materials or novel gate structures is useful to reduce the gate resistance. Refining the re-crystallization to increase grain size of the poly-Si films represents another useful approach for device performance improvement.

The error arisen during the de-embedding process is an issue when we extract

parasitic parameters. The layout of the through test-structure is needed for de-embedding procedure. The through test-structure can improve the accuracy of de-embedding procedure. On the other hand, tighter CD control during the manufacturing of the reticles for the DP process can help reduce the fluctuation in the dimensions of the final poly-Si gate patterns in the interdigital gate structures. The DP technique is also feasible for producing asymmetric S/D structure in the fabricated n-type poly-Si TFTs. Extra freedoms offered by the asymmetric scheme in the optimization of device structure should be a viable way for further boosting the RF performance of the devices.



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Chapter 2

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Chapter 3

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Figures

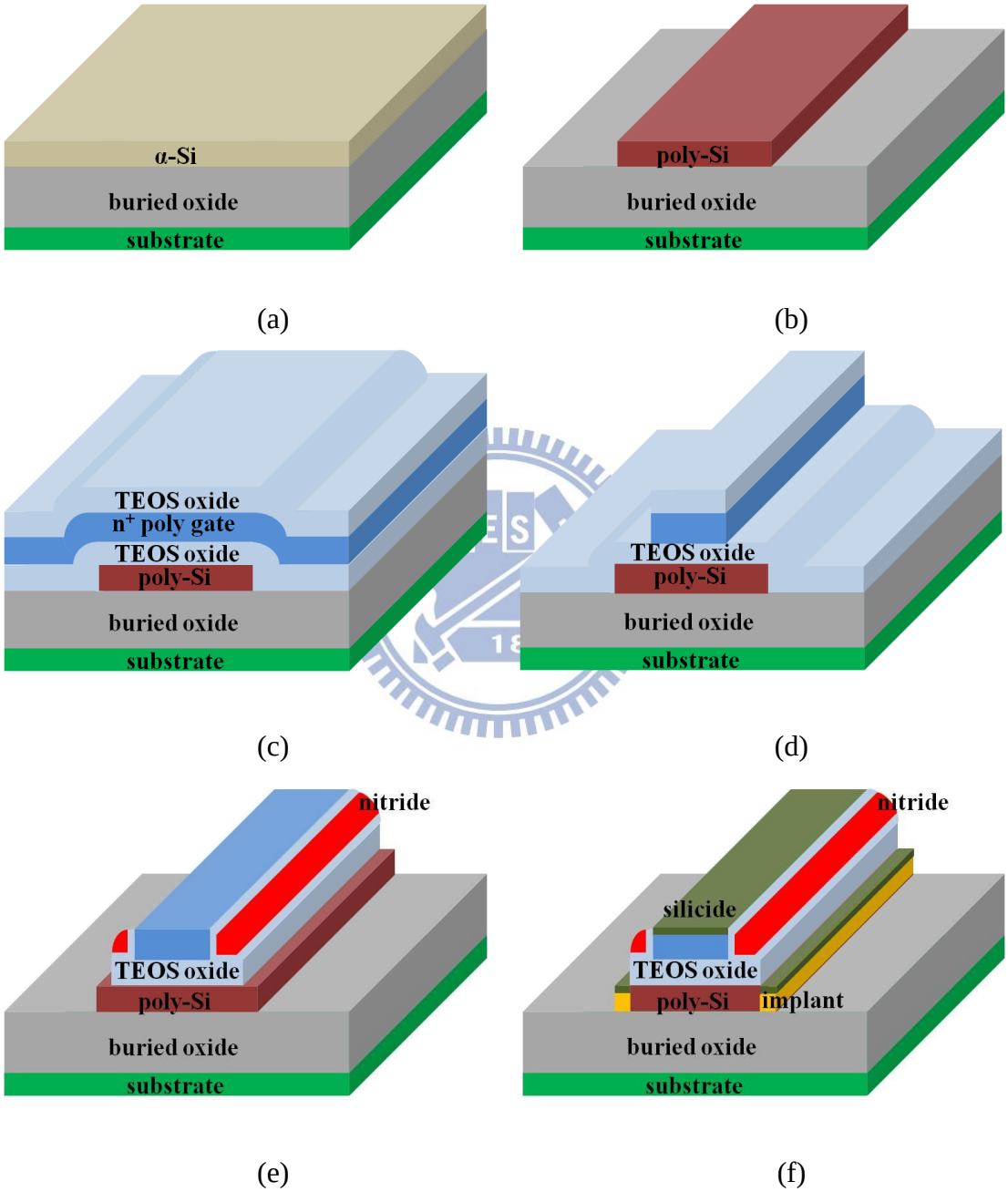


Fig. 2.1 Process flow of the poly-Si TFT fabrication.

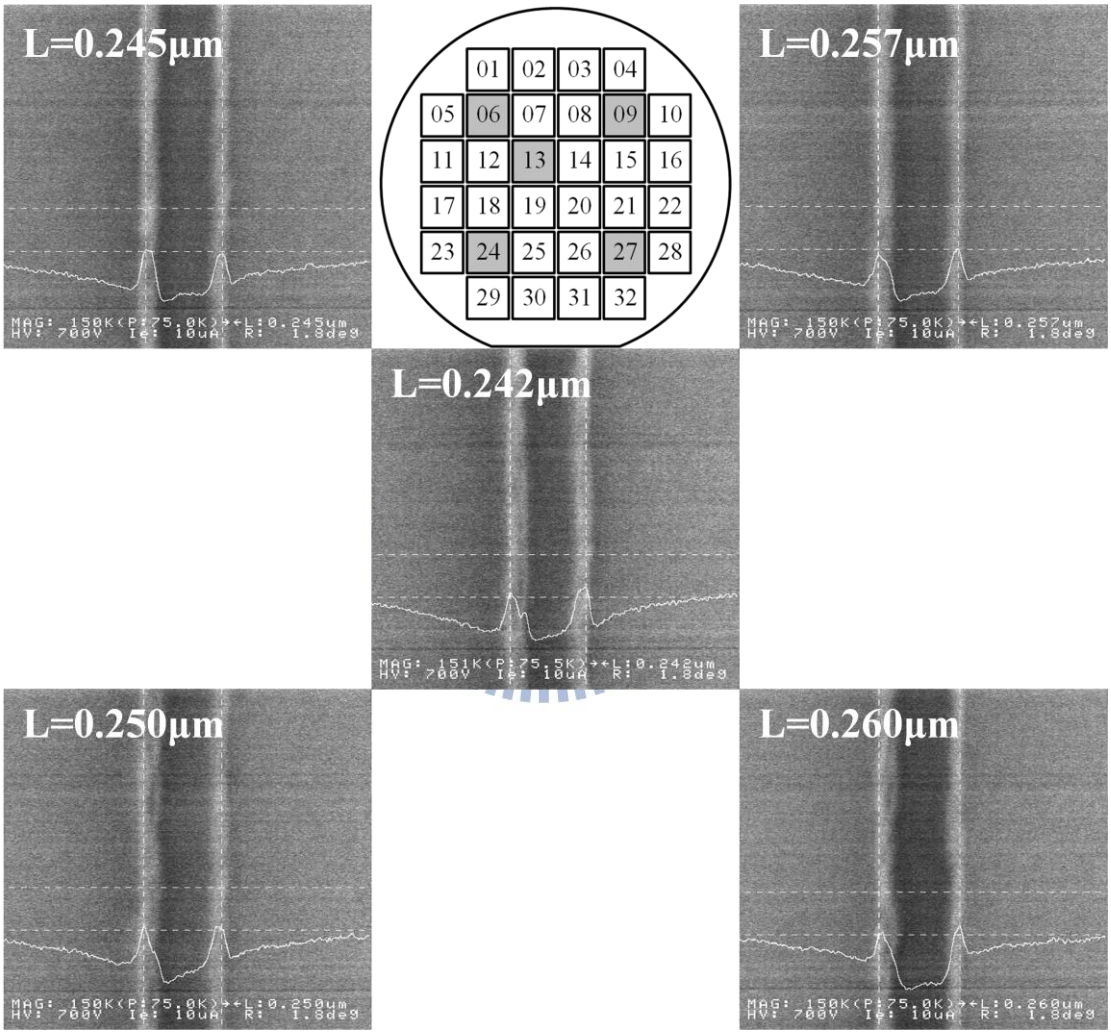


Fig. 2.2 In-line SEM image of patterned PR lines with L_{mask} of 0.25µm located at different dies of a wafer before trimming.

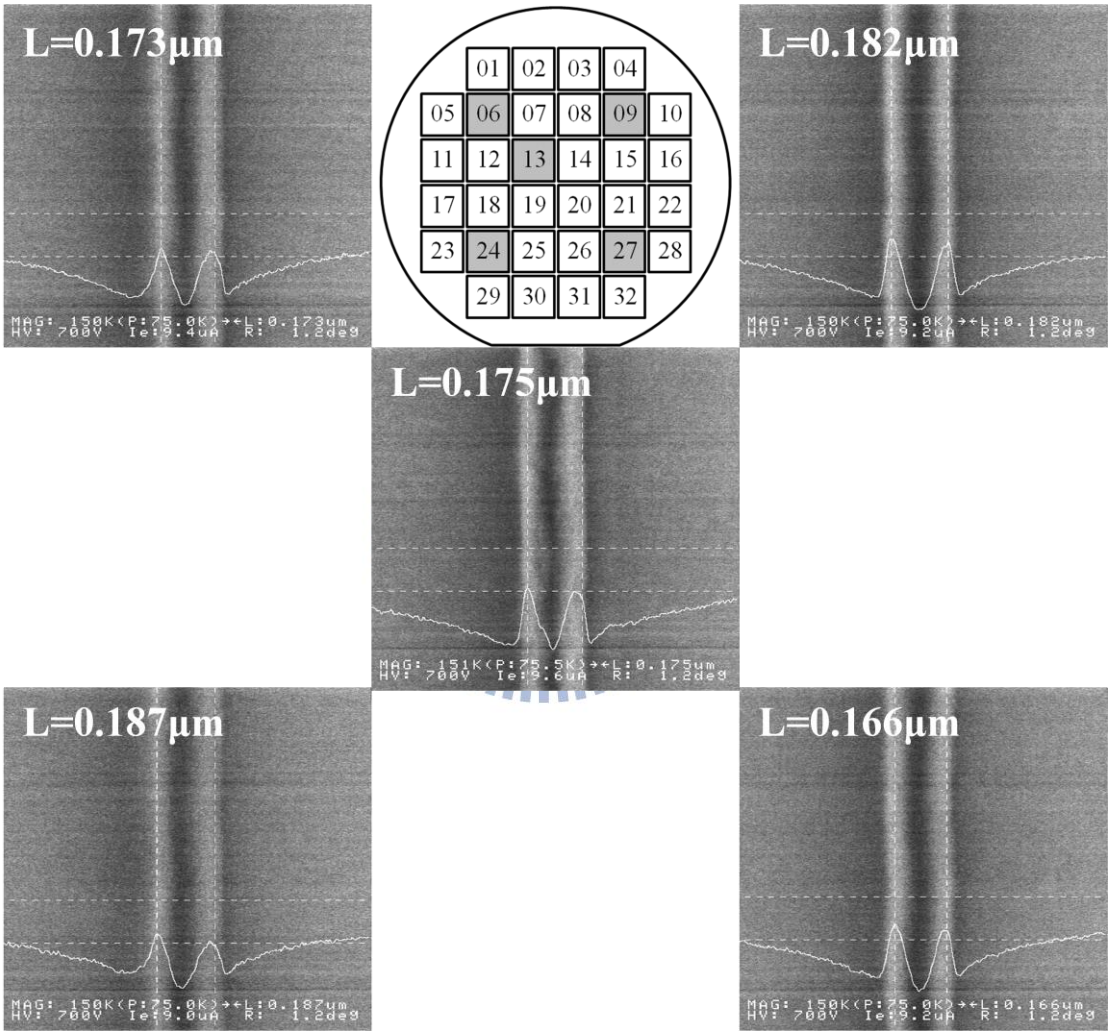


Fig. 2.3 In-line SEM image of patterned PR lines with L_{mask} of 0.25µm located at different dies of a wafer after trimming.

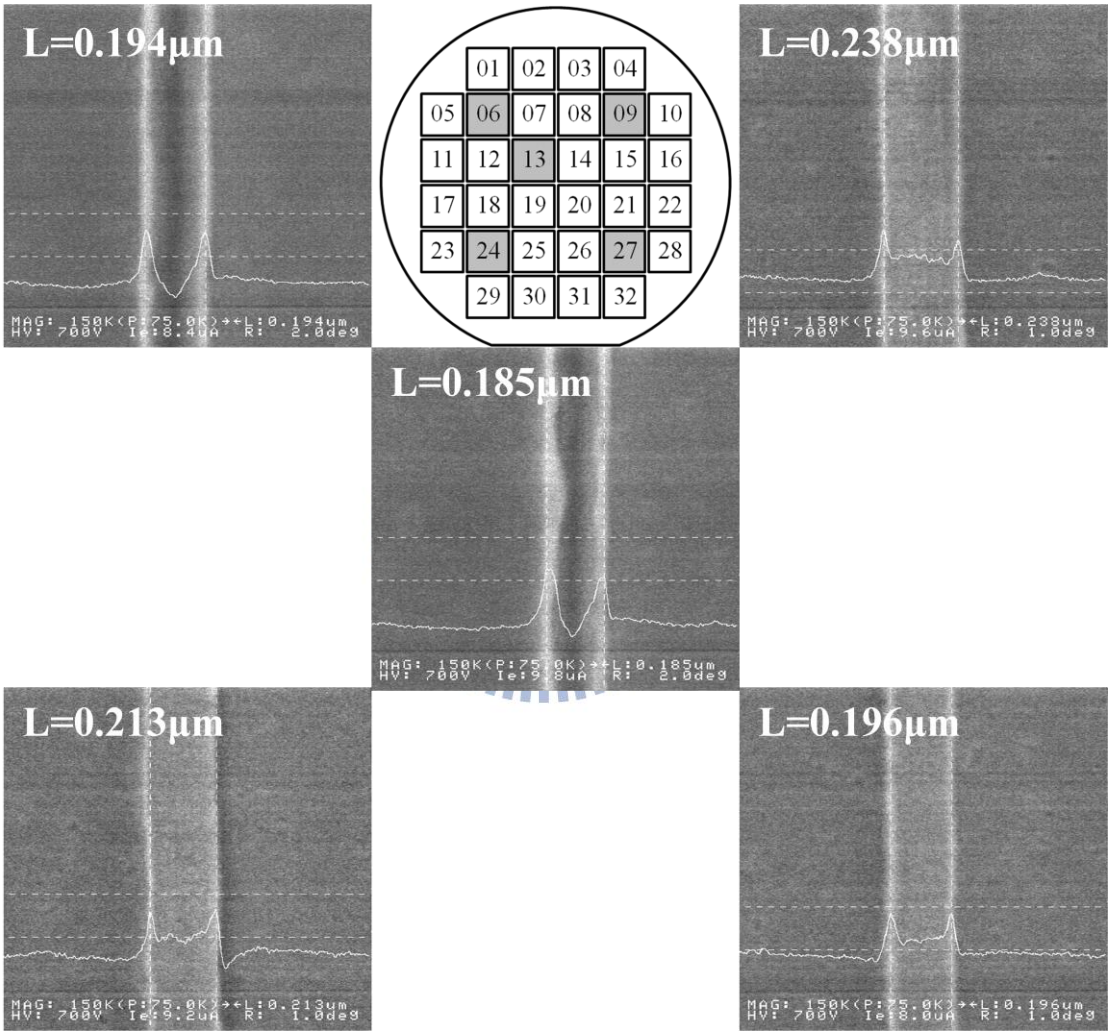


Fig. 2.4 In-line SEM image of patterned poly-Si lines located at different dies of a wafer after stripping off the trimmed PR.

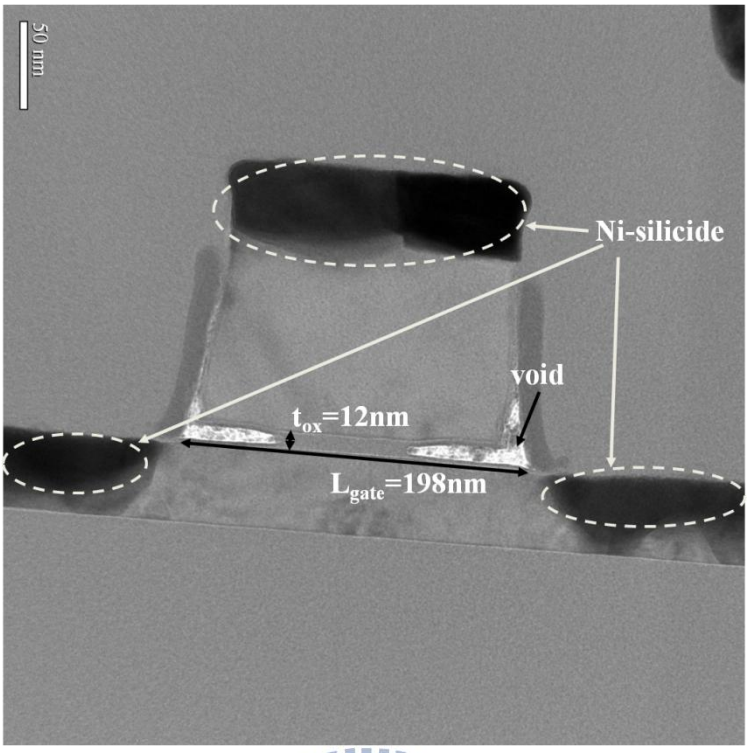


Fig. 2.5 Cross-sectional TEM image of a n-type TFT device.

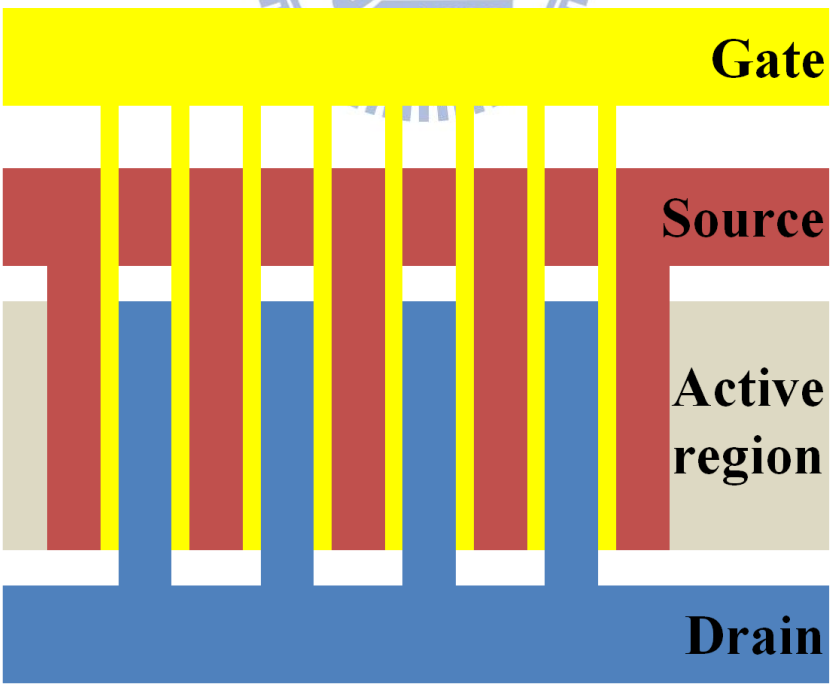
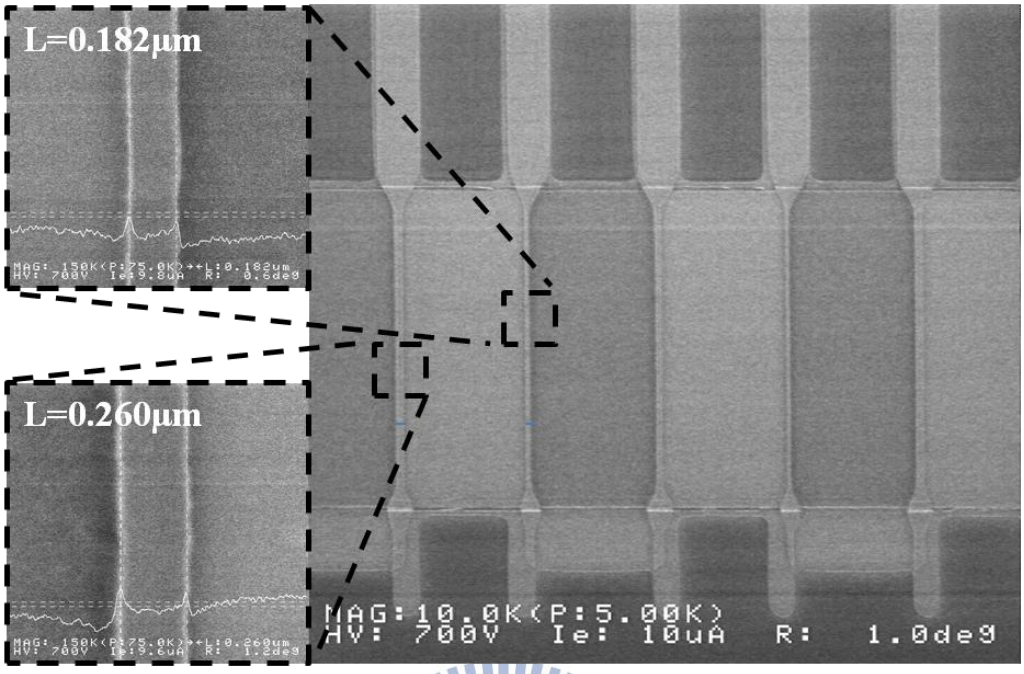
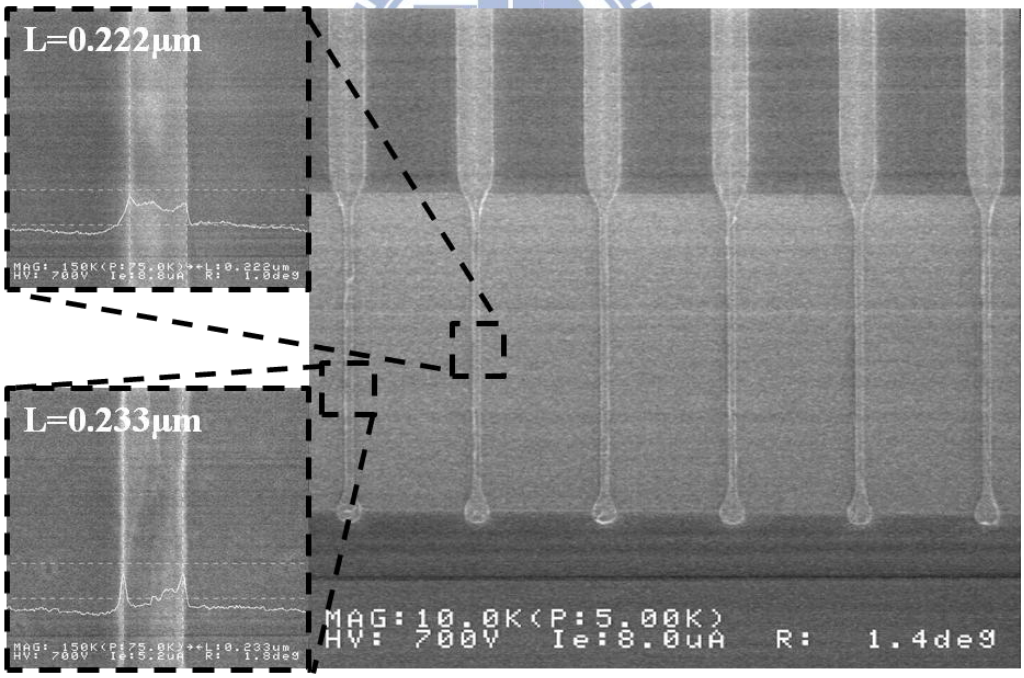


Fig. 2.6 The device design with interdigital gate structure.



(a)



(b)

Fig. 2.7 In-line SEM images of poly-Si gates patterned with (a) DR techniques with severe fluctuation and (b) SP techniques with greatly reduced fluctuation.

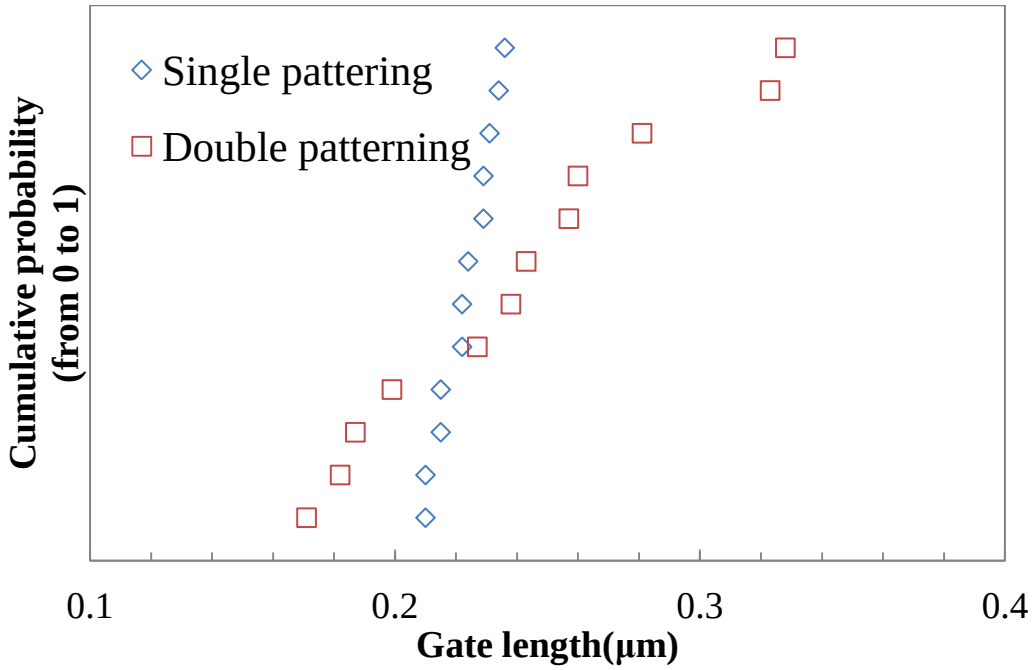


Fig. 2.8 Cumulative plots of measured dimensions of poly-Si gates patterned at different dies of a wafer with SP or DP methods with nominal gate length of 0.23μm.

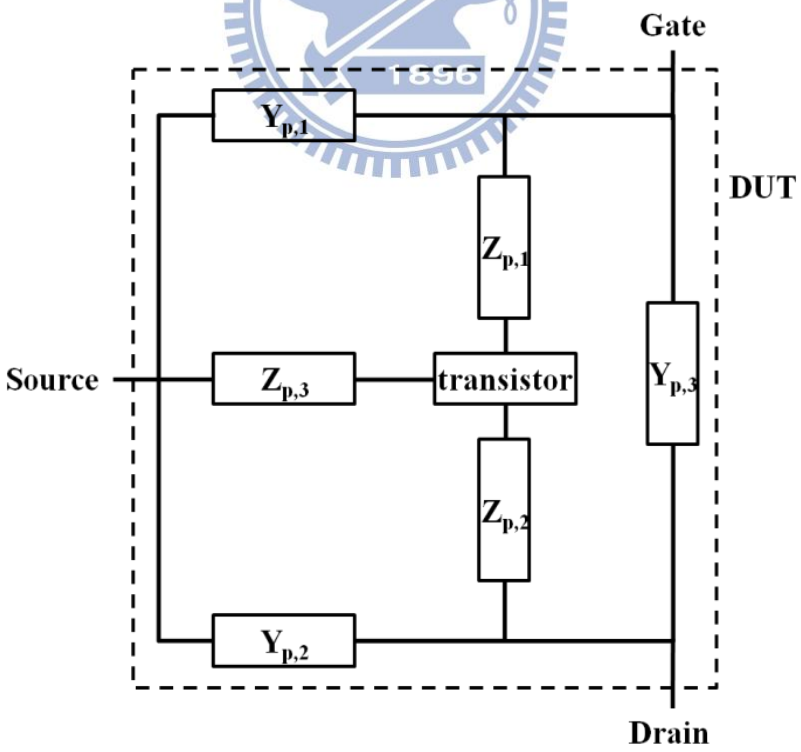
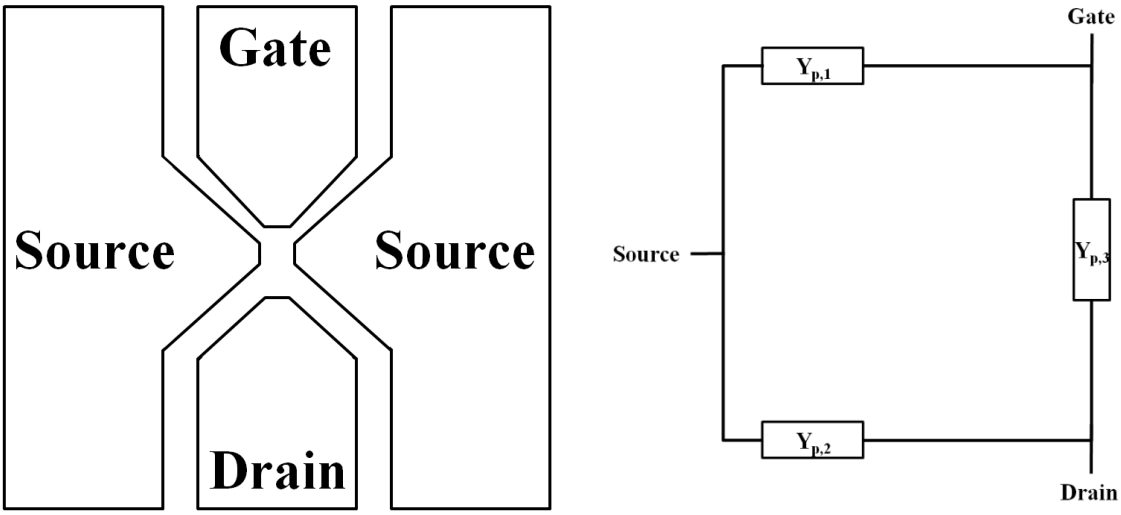
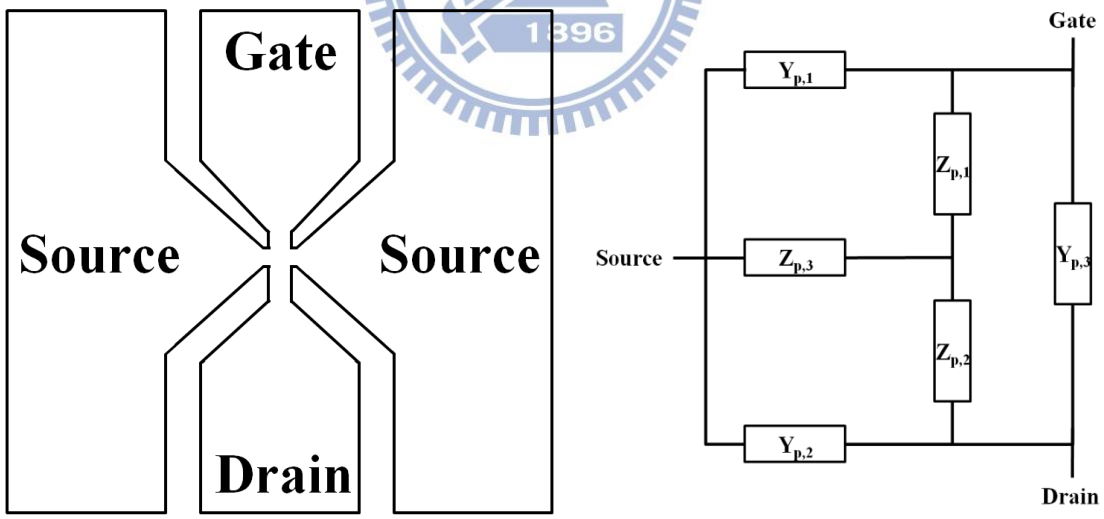


Fig. 2.9 Equivalent circuit diagram used for the two-step correction including parasitic effect [2.2].



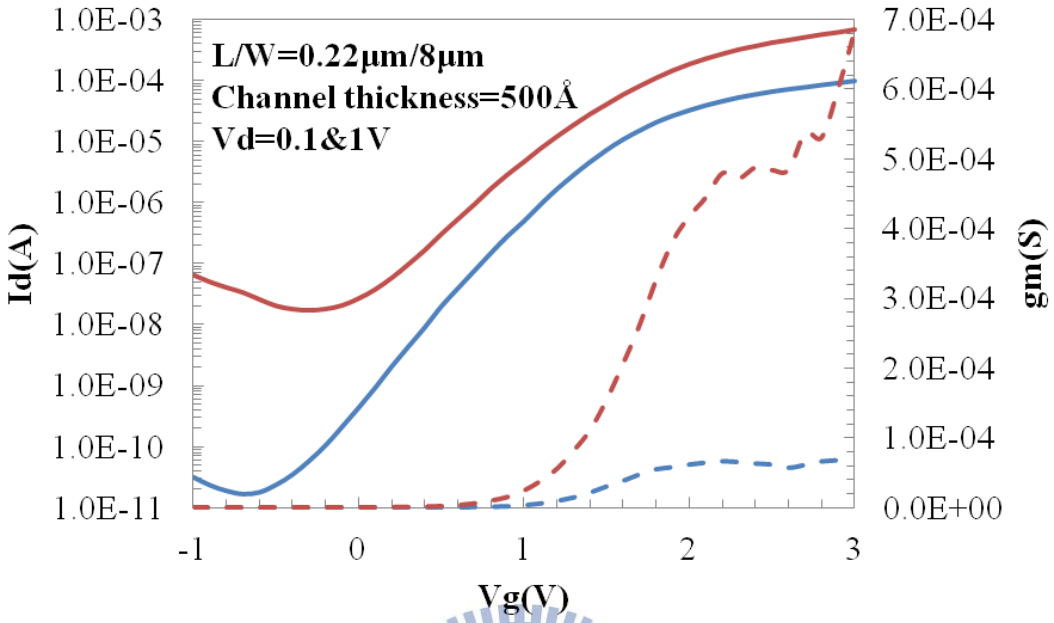
(a) (b)

Fig. 2.10 (a)The open test fixture and (b) the diagram of equivalent circuit.

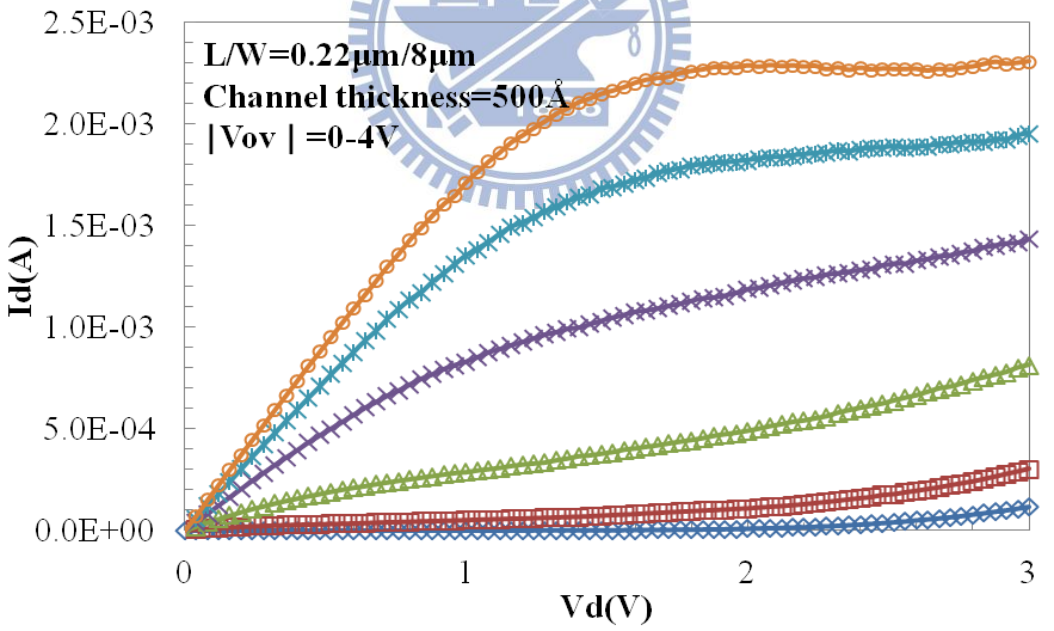


(a) (b)

Fig. 2.11 (a) The short test fixture and (b) the diagram of equivalent circuit.

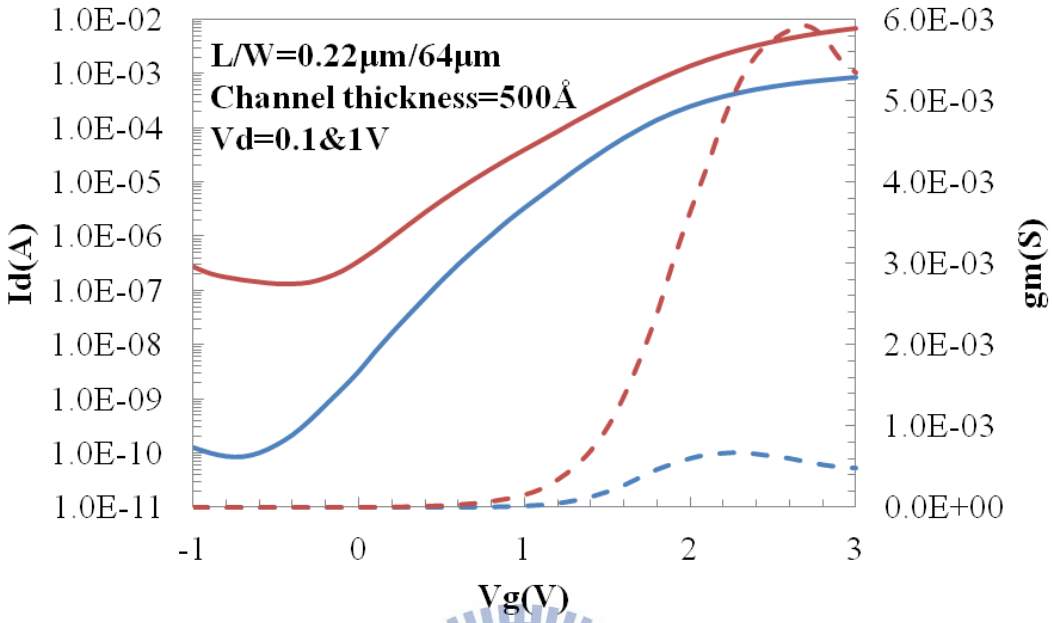


(a)

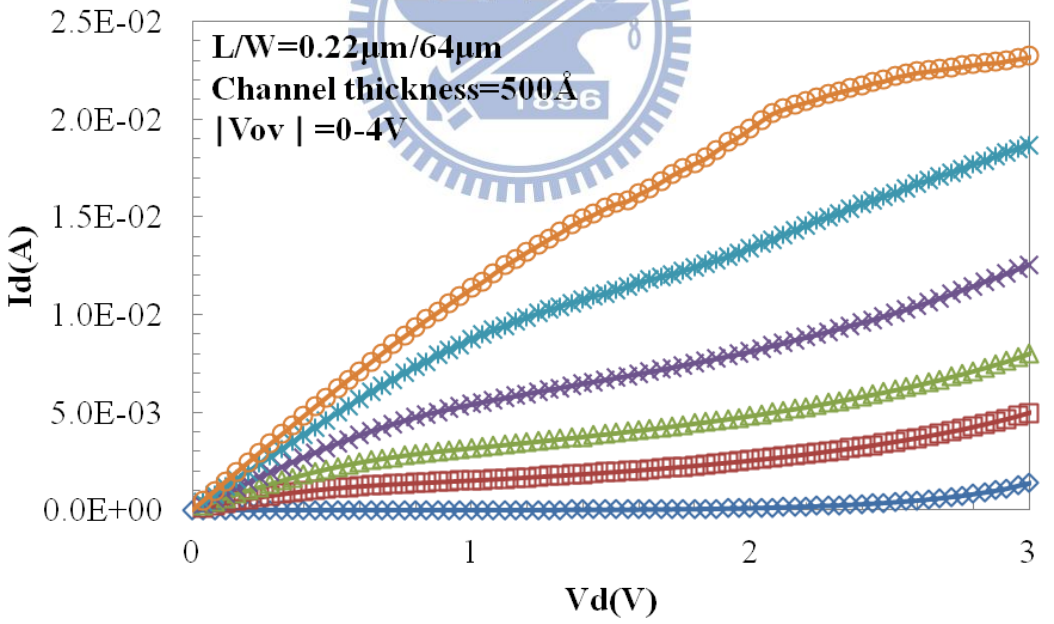


(b)

Fig. 3.1 (a) Transfer and (b) output characteristics of n-type TFT with L/W = 0.2μm/8μm.



(a)



(b)

Fig. 3.2 (a) Transfer and (b) output characteristics of an SP n-type TFT with L/W = 0.2μm/64μm.

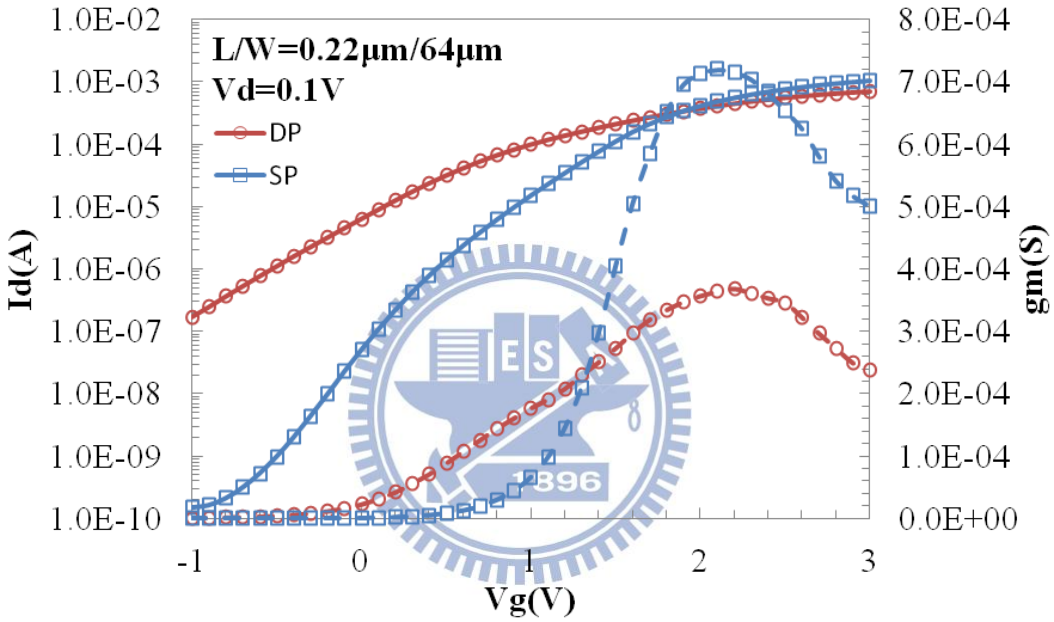


Fig. 3.3 Transfer characteristics of n-type TFTs at V_d = 0.1V patterned with SP and DP techniques. Nominal gate length and width are equal to 0.22µm and 64µm, respectively.

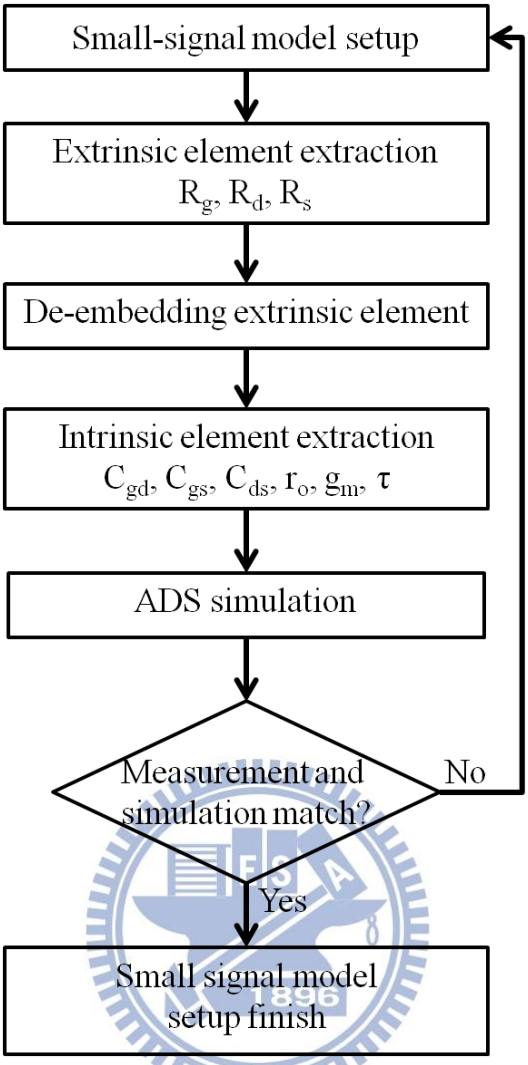


Fig. 3.4 The flowchart of small-signal model setup.

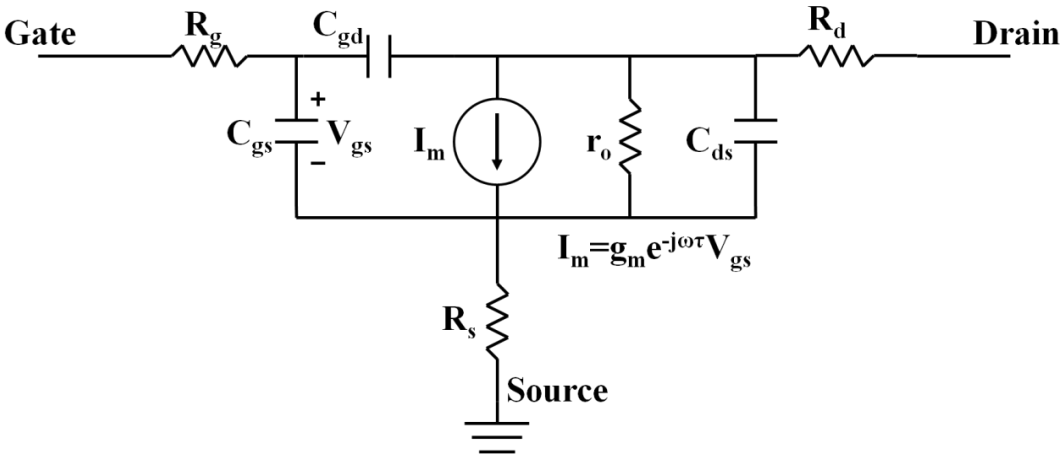
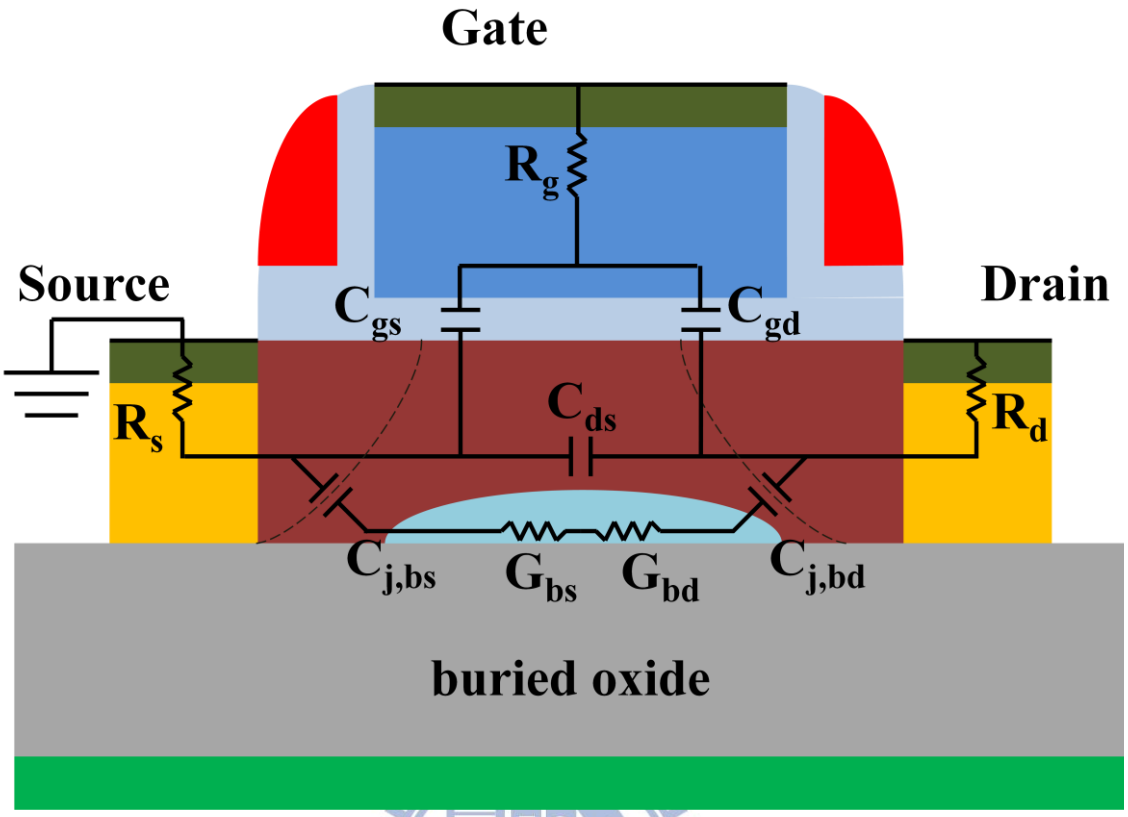
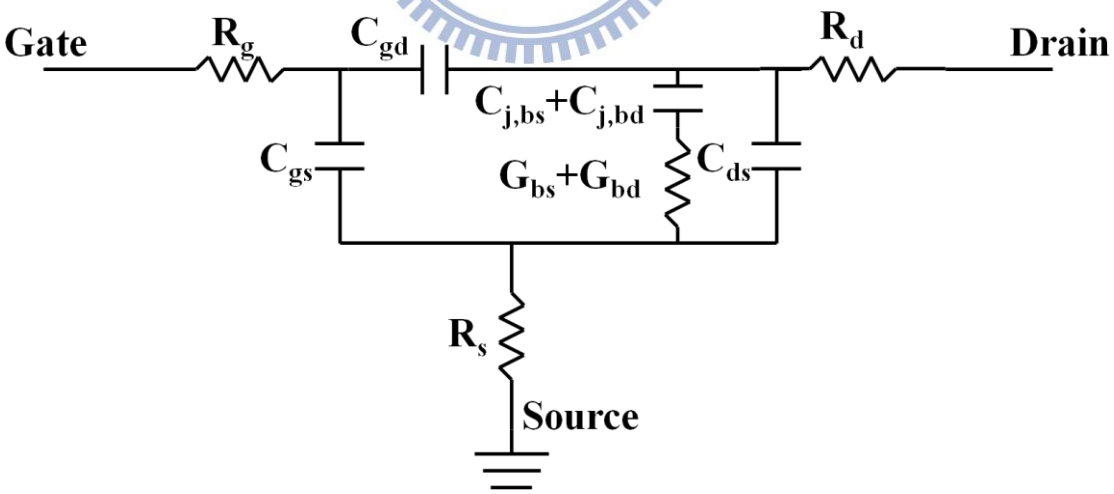


Fig. 3.5 Small-signal equivalent circuit of an n-type TFT.



(a)



(b)

Fig. 3.6 (a) Cross-sectional view of n-type TFTs with a partially depleted channel under the zero condition and (b) the equivalent circuit model.

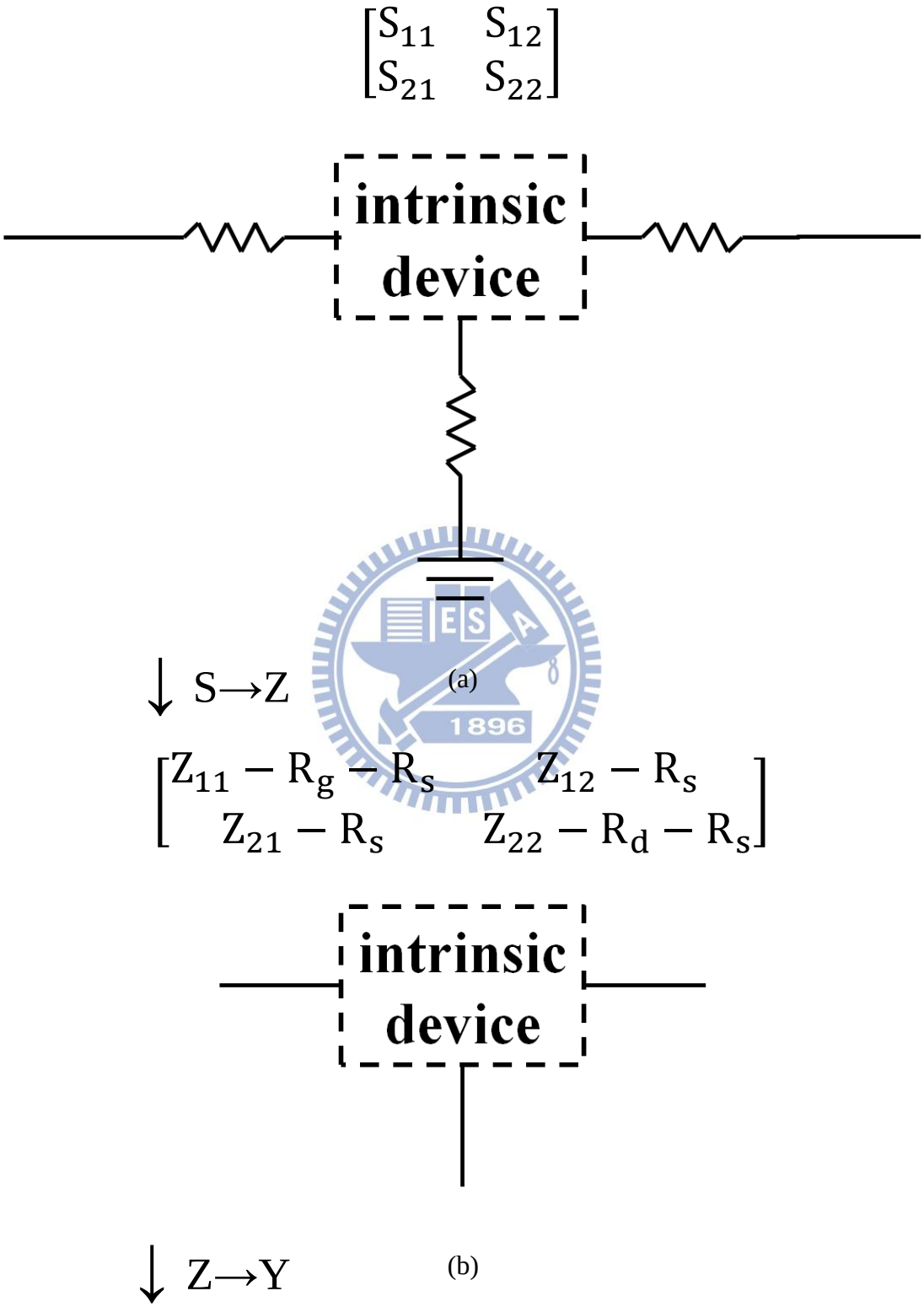


Fig. 3.7 Method of extracting intrinsic Y-parameter matrix of the device.

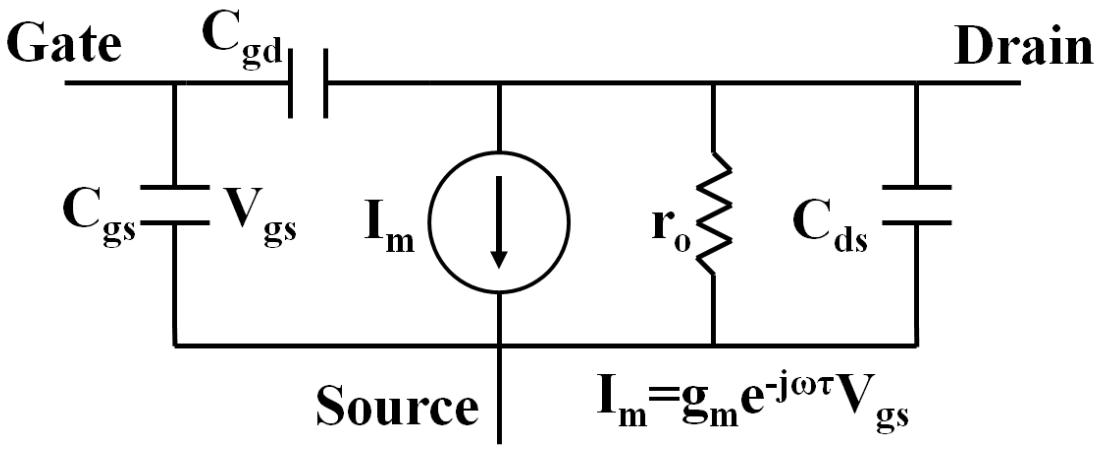


Fig. 3.8 Intrinsic part of an n-type TFT.

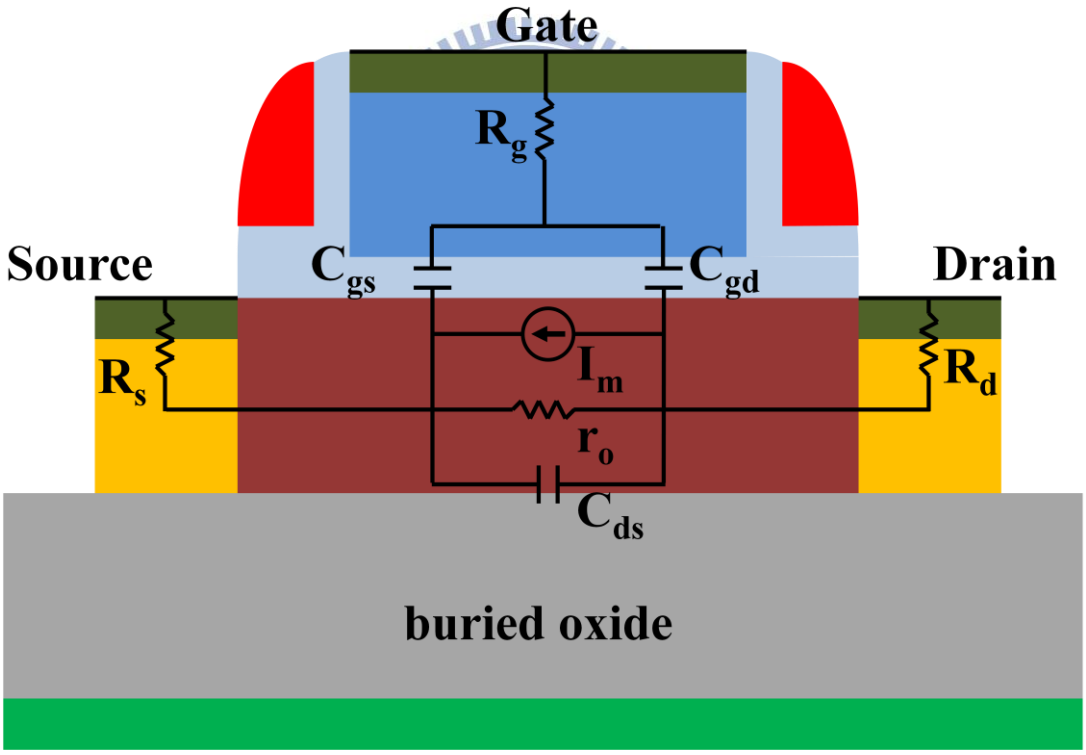


Fig. 3.9 The cross section of an n-type TFT with corresponding small-signal equivalent circuit.

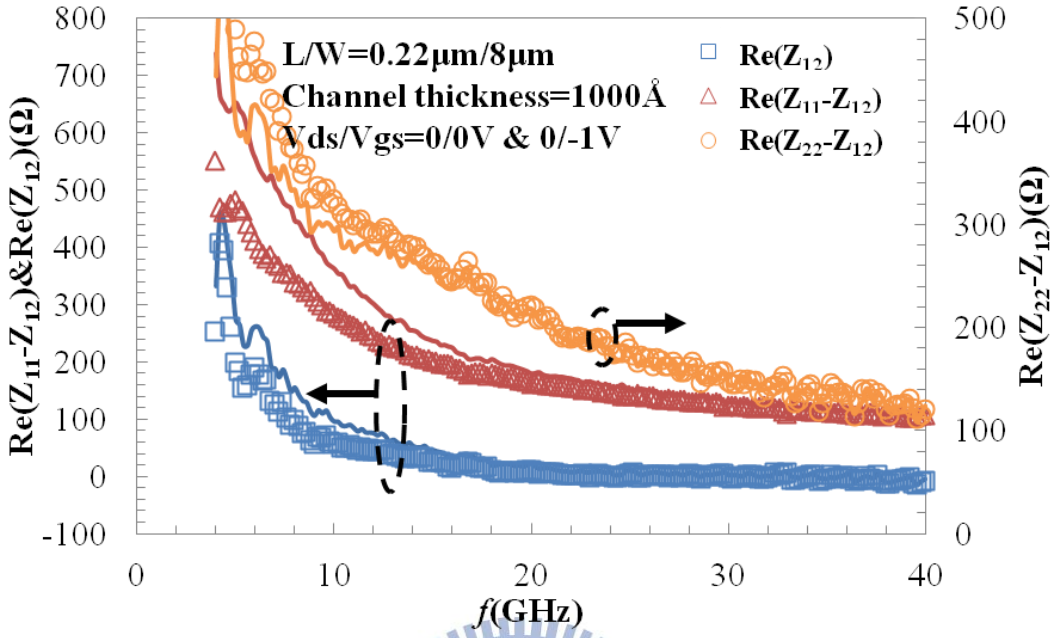


Fig. 3.10 Modeling results for extrinsic resistance extraction considering the neutral-body effect at cut-off condition for a device with channel thickness of 1000Å . (lines: V_d = 0V and V_g = -1V. symbols: V_d = V_g = 0V)

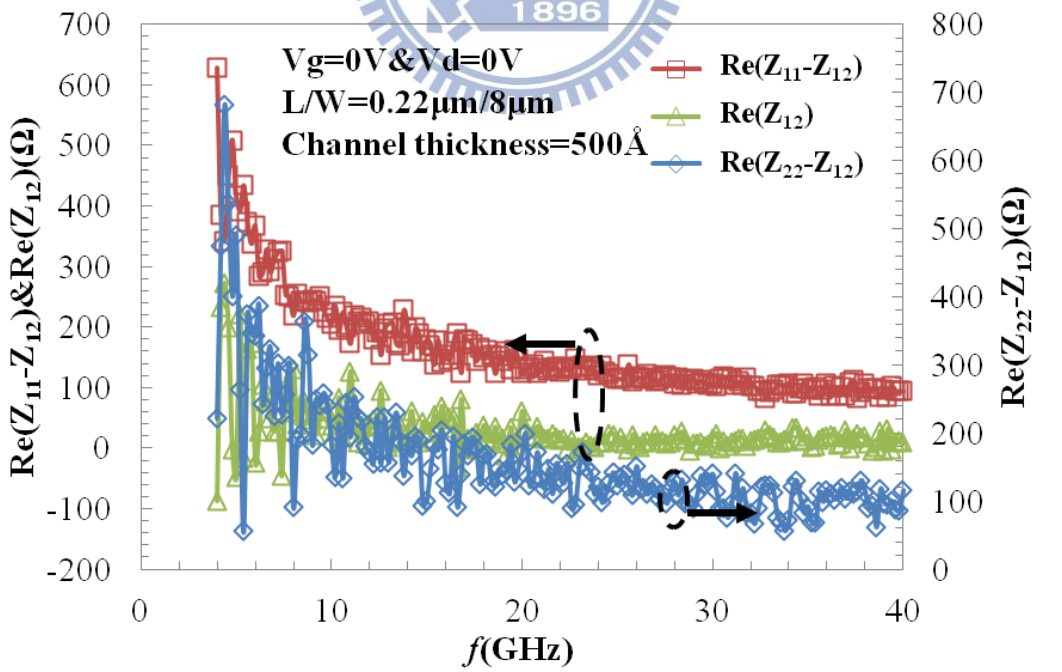


Fig. 3.11 Modeling results for extrinsic resistance extraction considering the neutral-body effect at cut-off condition for a device with channel thickness of 500Å .

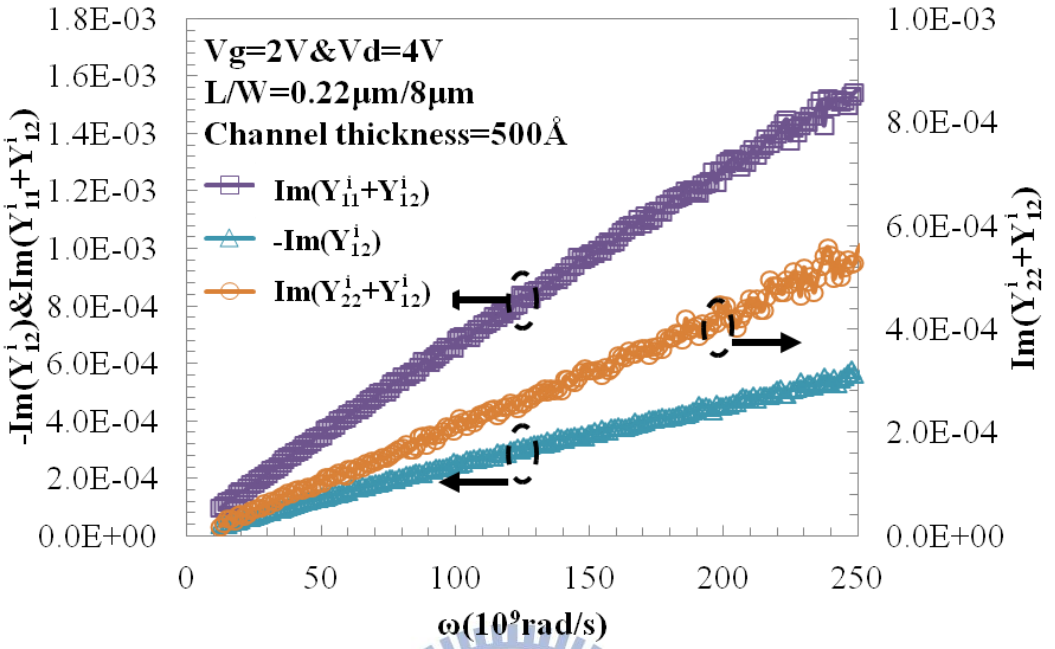


Fig. 3.12 Modeling results for $Im(Y_{11}+Y_{12})$, $-Im(Y_{12})$, and $Im(Y_{22}+Y_{12})$ for a device with channel thickness of 500Å .

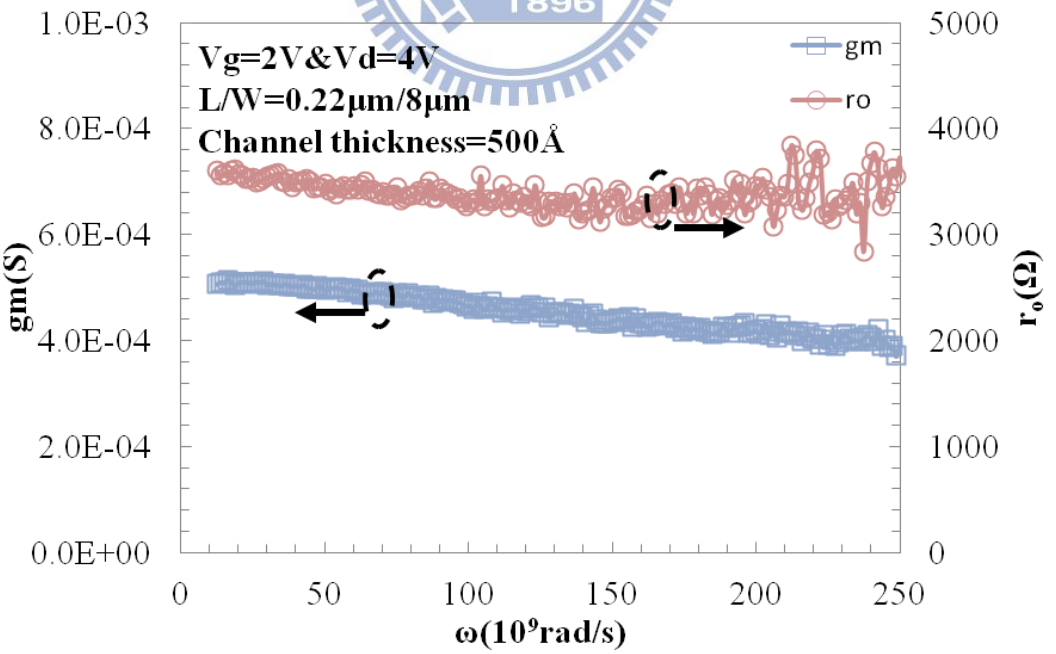


Fig. 3.13 Modeling results for g_m, and r_o for a device with channel thickness of 500Å .

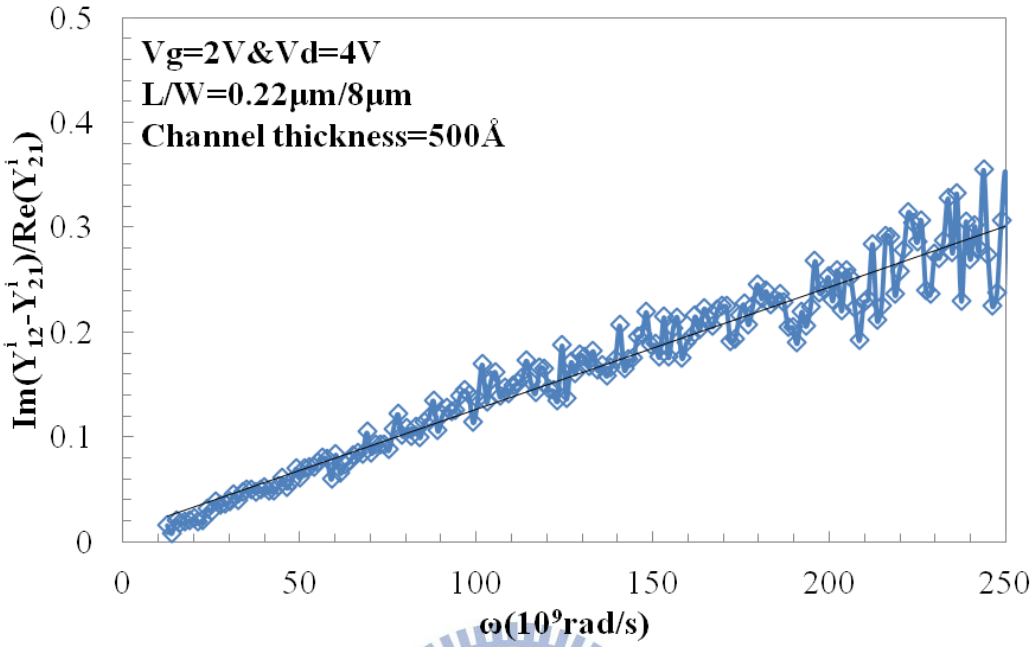


Fig. 3.14 Modeling results for τ for a device with channel thickness of 500Å .

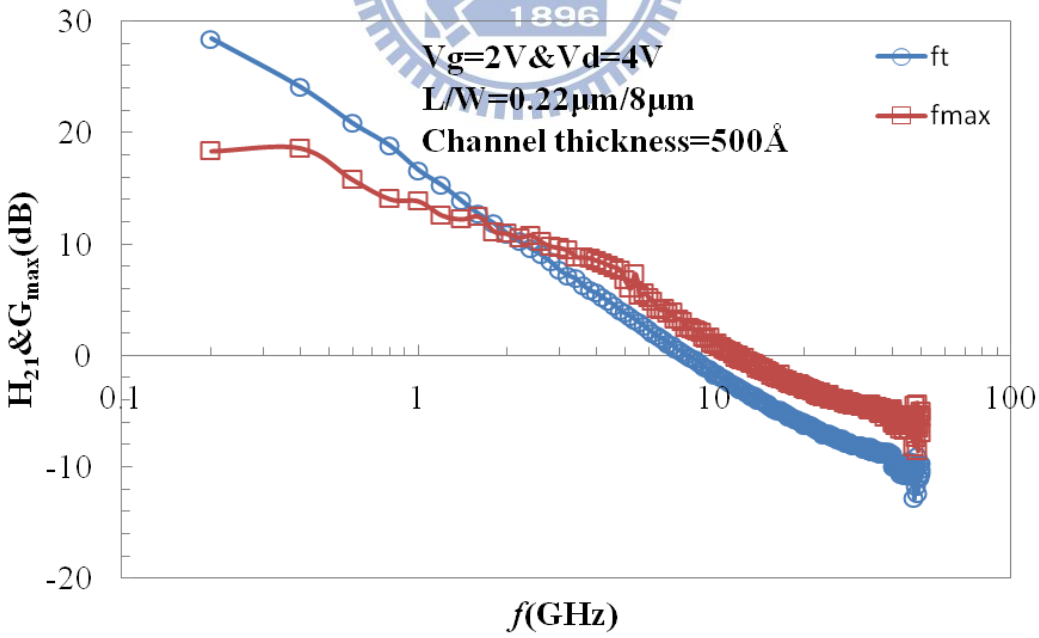
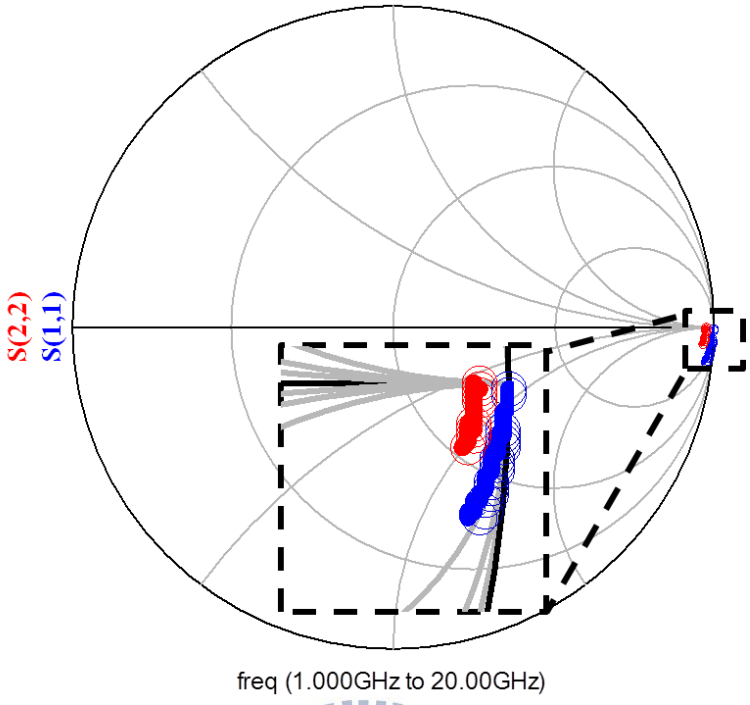
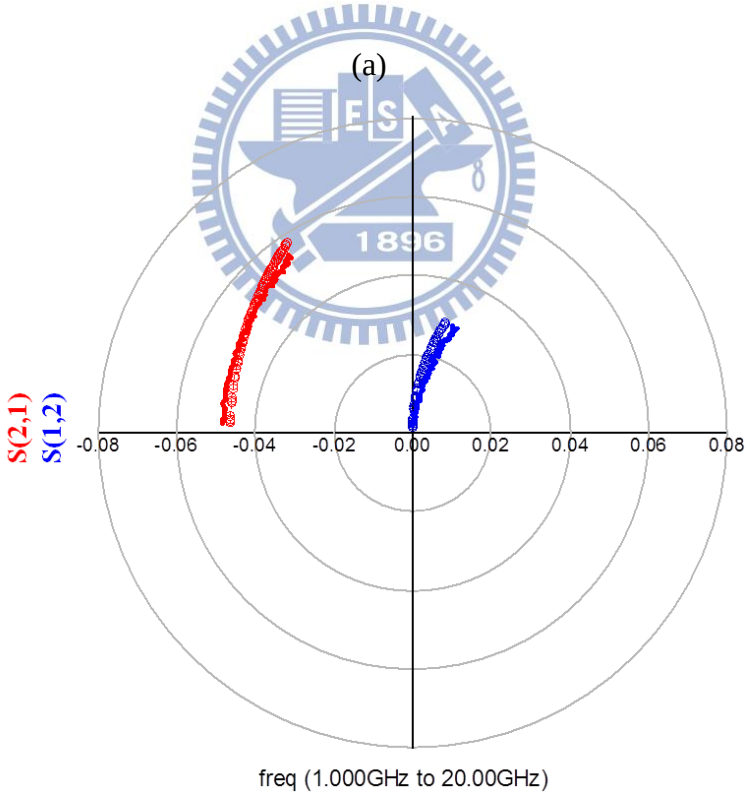


Fig. 3.15 Measured results of f_t and f_{max} for a device with channel thickness of 500Å .



(a)



(b)

Fig. 3.16 Modeling results of (a) S_{11} and S_{22} and (b) S_{12} and S_{21} at V_d = 2V and V_g = 4V. (lines for measurements, symbols for models, channel thickness = 500Å ,and L/W = 0.22μm/8μm)

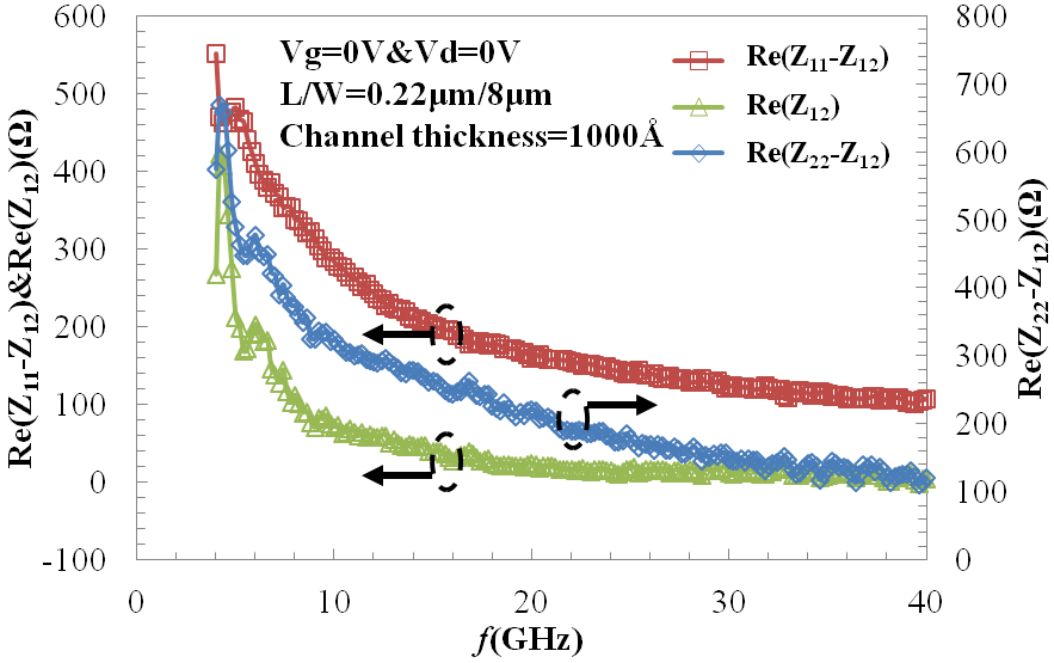


Fig. 3.17 Modeling results for extrinsic resistance extraction considering the neutral-body effect at cut-off condition for a device with channel thickness = 1000Å

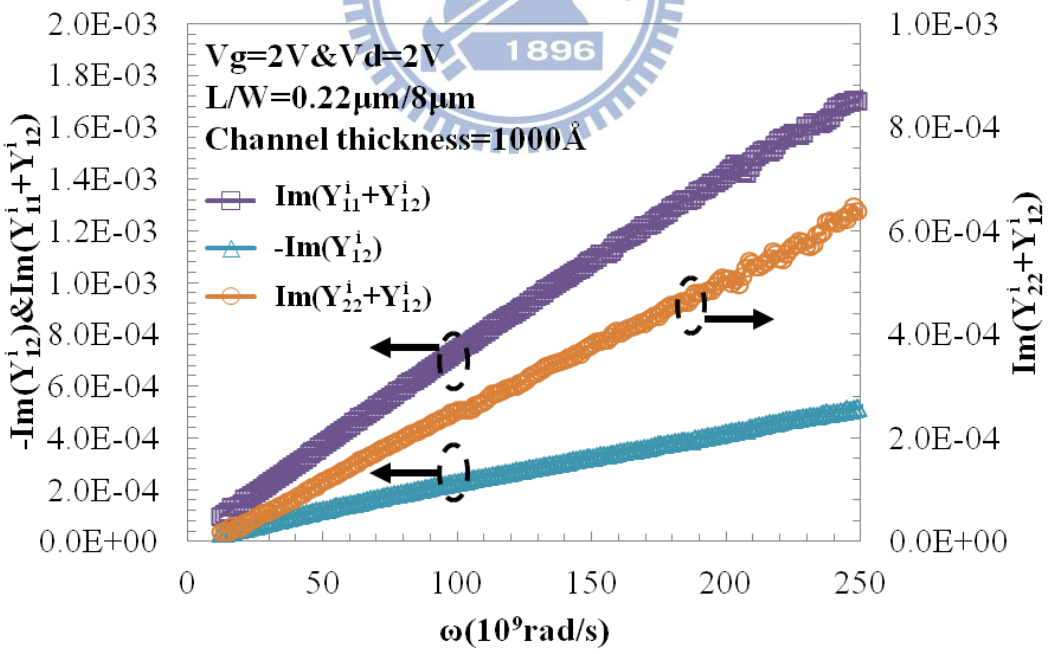


Fig. 3.18 Modeling results of $Im(Y_{11}+Y_{12})$, $-Im(Y_{12})$, and $Im(Y_{22}+Y_{12})$ for a device with channel thickness = 1000Å

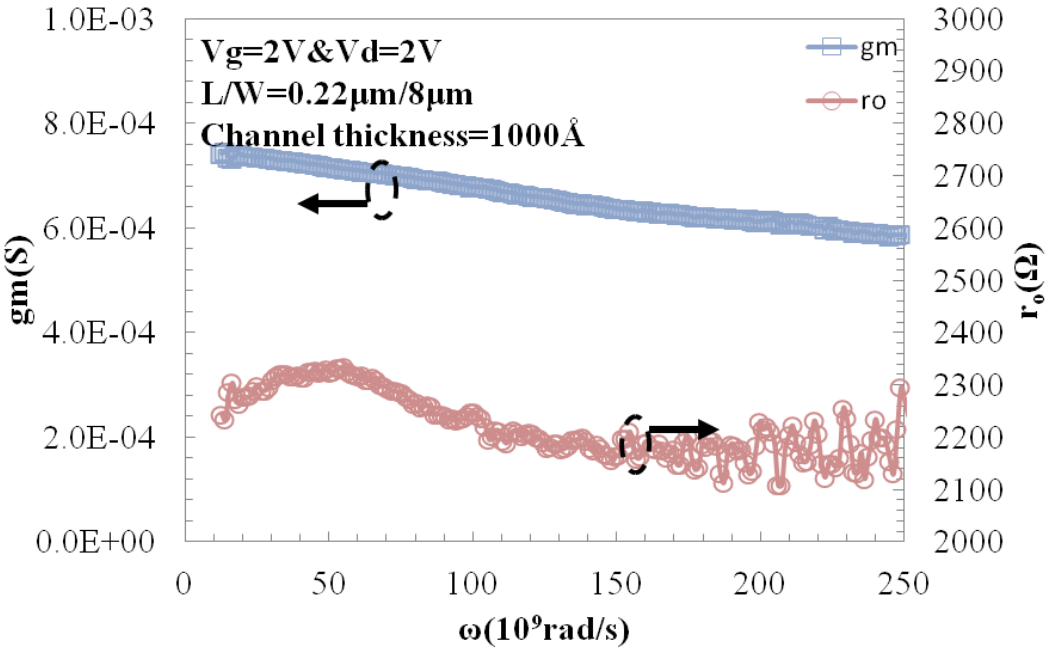


Fig. 3.19 Modeling results of g_m, and r_o for a device with channel thickness = 1000Å

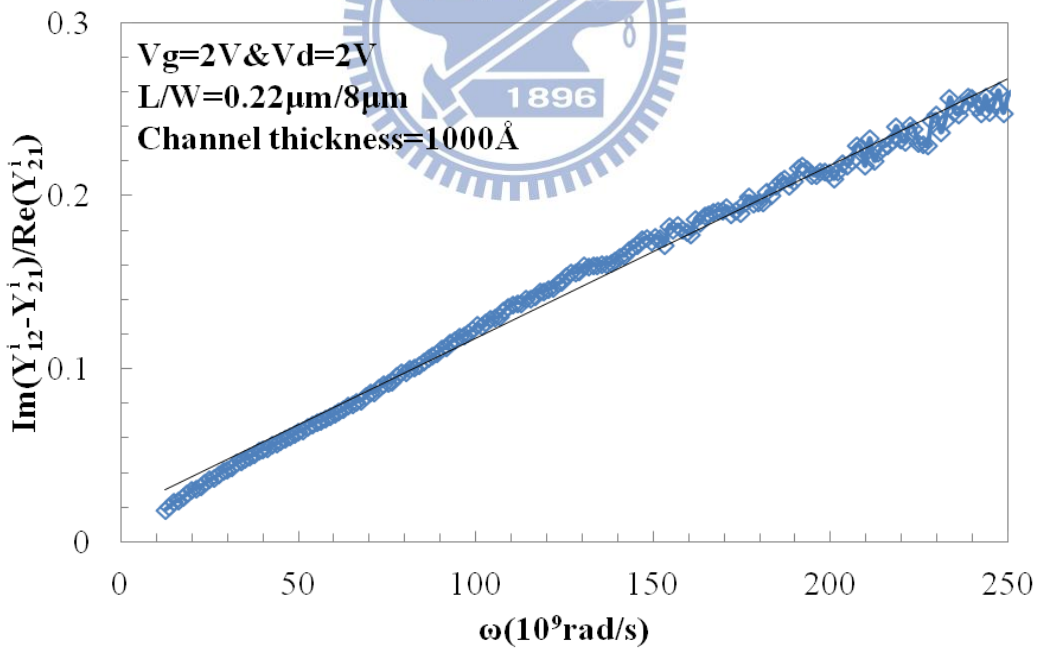


Fig. 3.20 Modeling results of τ for a device with channel thickness = 1000Å

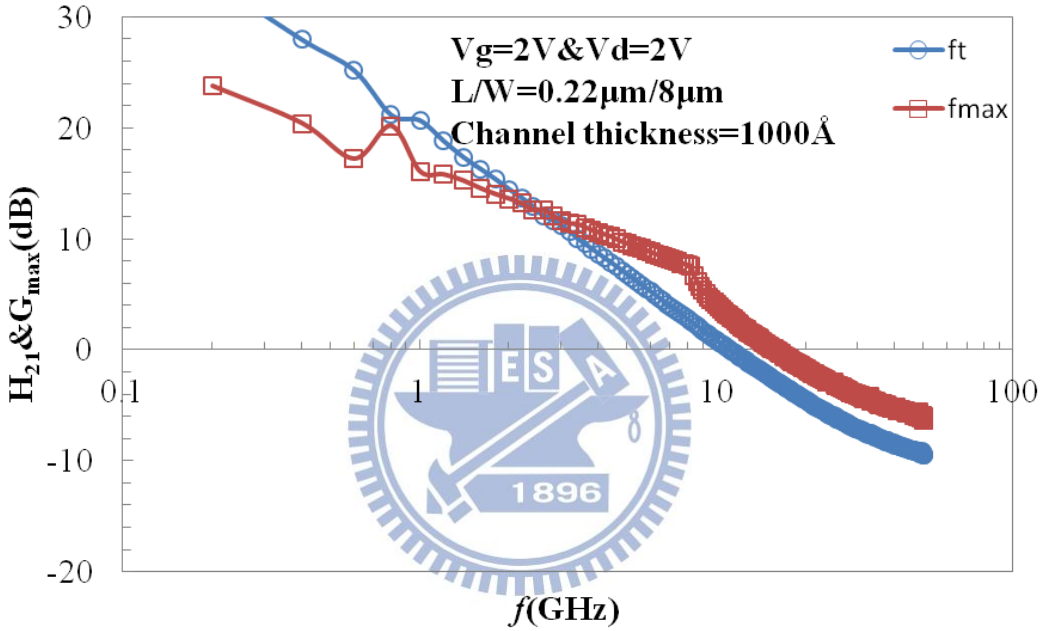
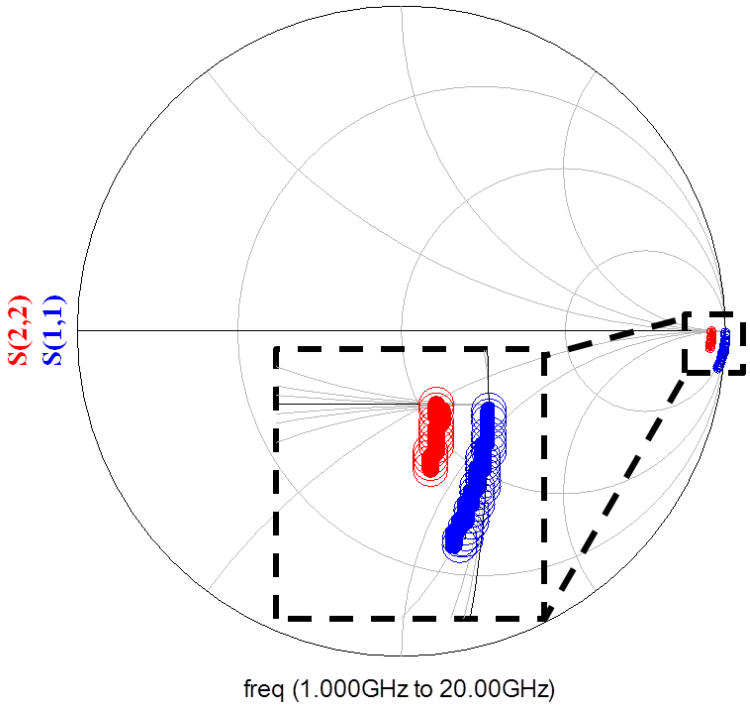
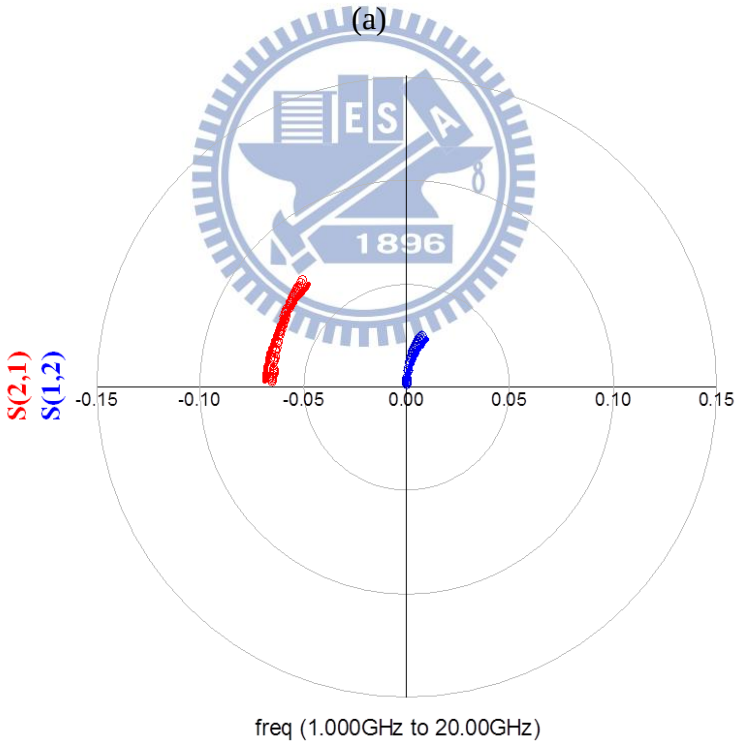


Fig. 3.21 Measured results of f_t and f_{max} for a device with channel thickness = 1000Å



(a)



(b)

Fig. 3.22 Modeling results of (a) S_{11} and S_{22} and (b) S_{12} and S_{21} at V_d = 2V and V_g = 2V. (lines for measurements, symbols for models, channel = 1000Å ,and L/W = 0.22μm/8μm)

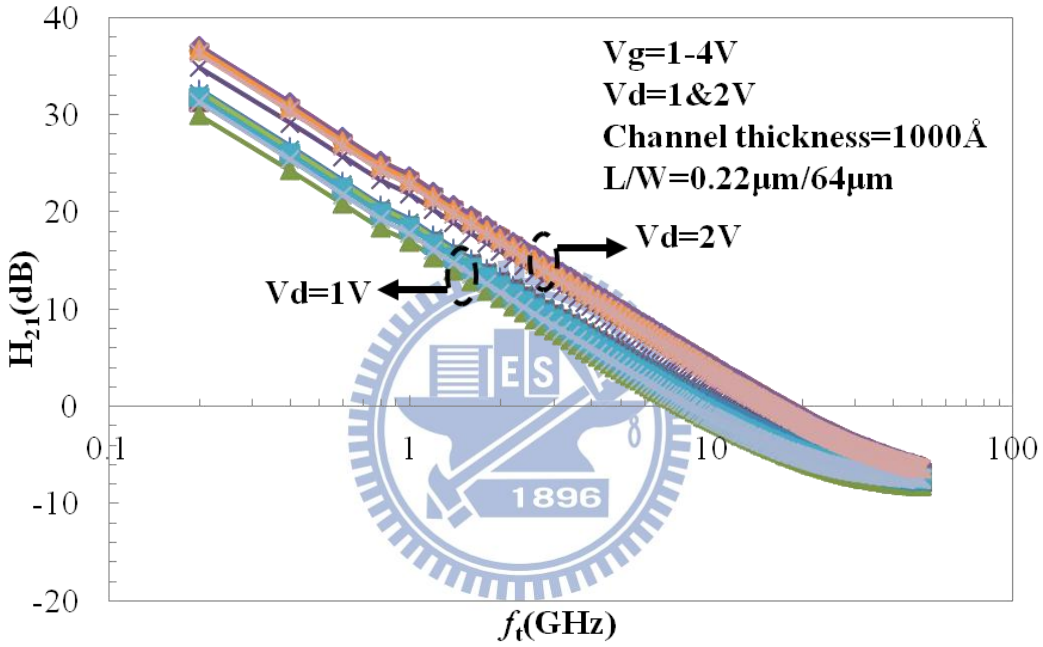


Fig. 3.23 f_t measured at V_d = 1V and 2V for a device with channel thickness of 1000Å .

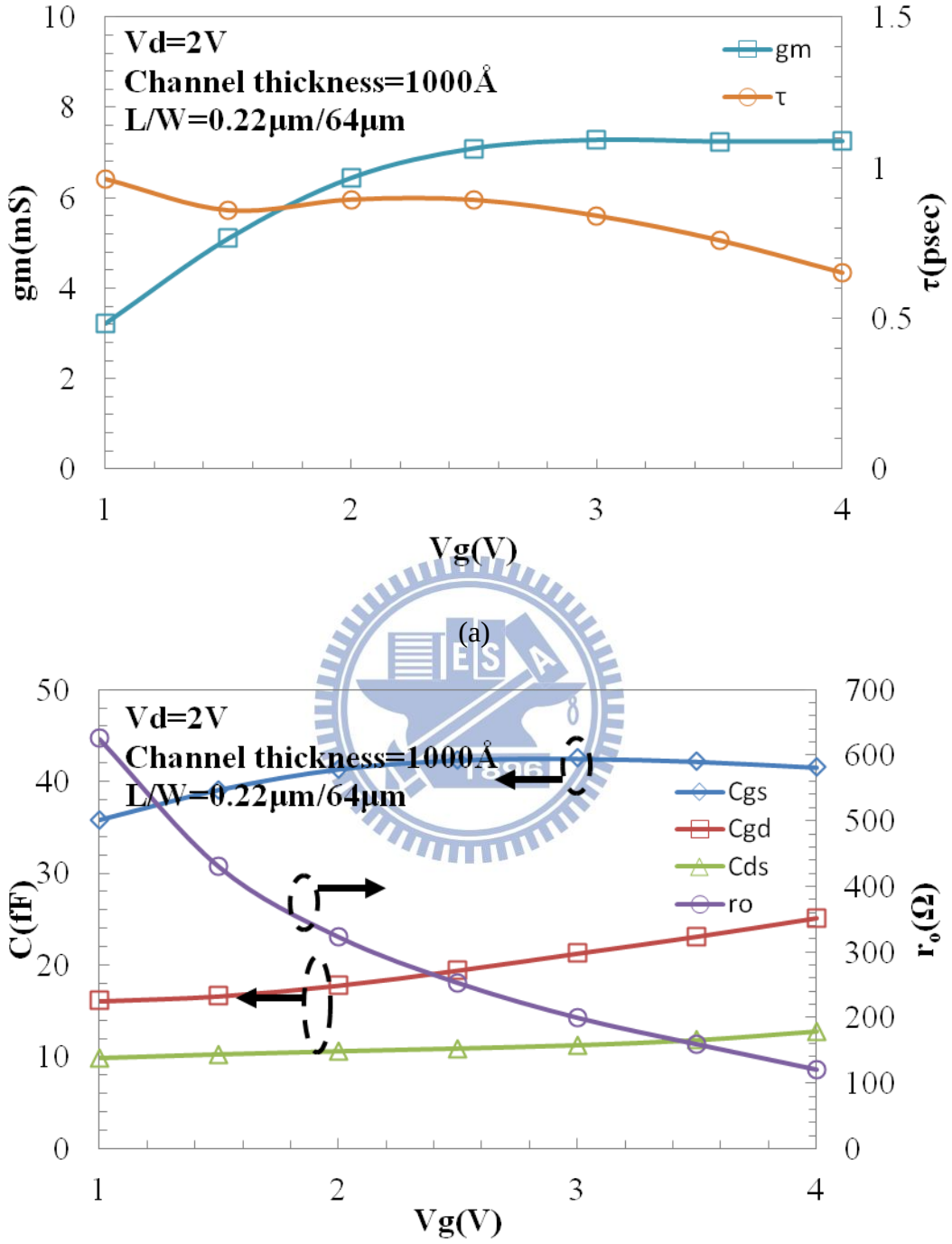


Fig. 3.24 Small-signal parameters extracted at V_d = 2V and various V_g for a device with channel thickness of 1000Å .

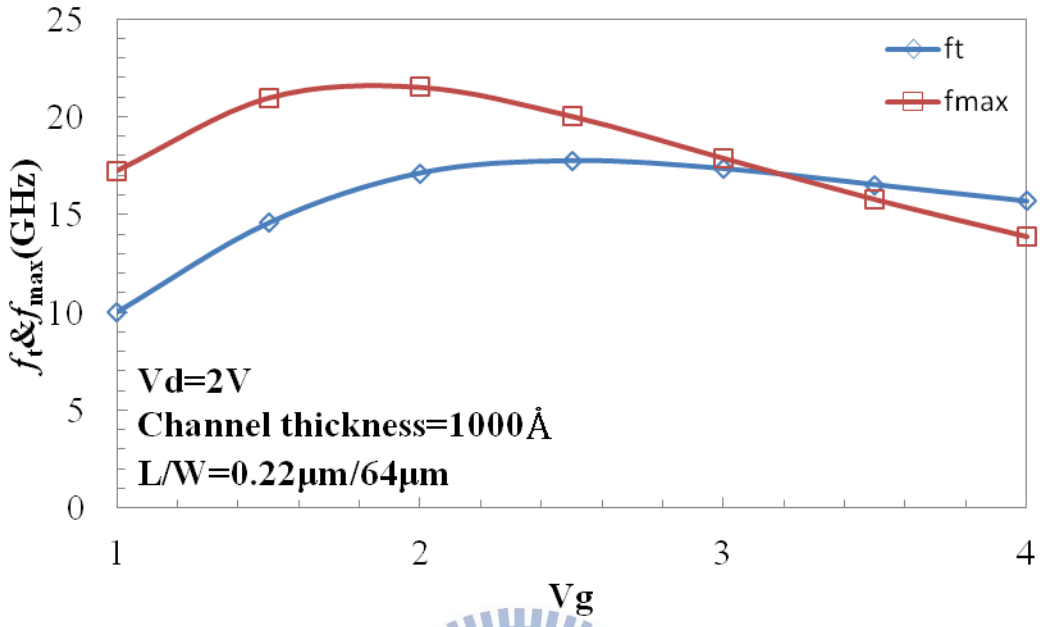


Fig. 3.25 The f_t and f_{max} measured at V_d = 2V and various V_g for a device with channel thickness of 1000Å .

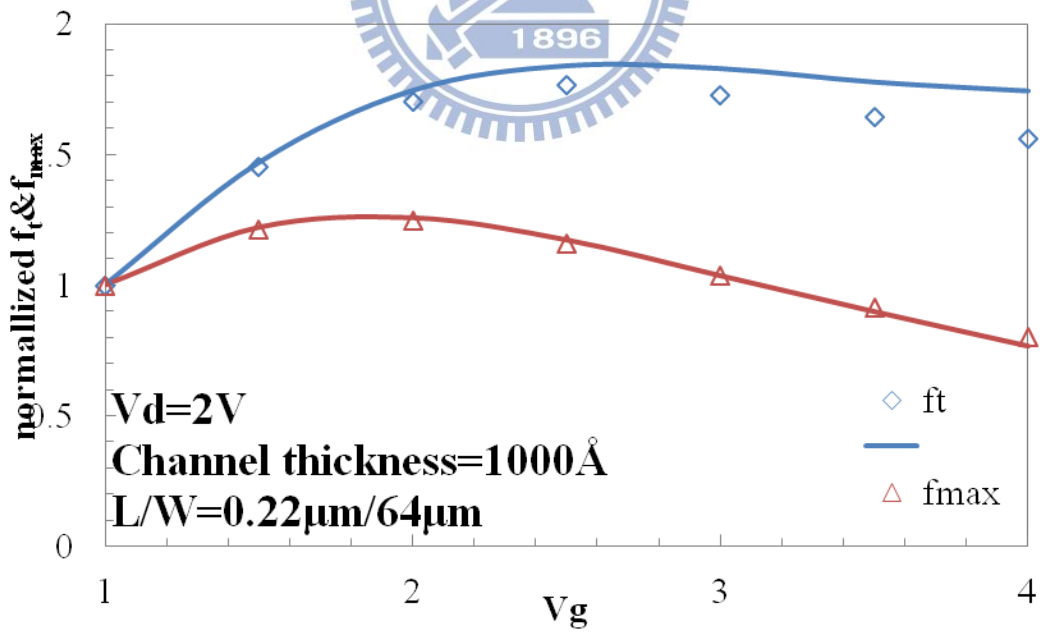


Fig. 3.26 Comparisons between analytical calculation (lines) and measured f_t and f_{max} (symbols) versus gate voltage for a device with channel thickness of 1000Å .

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