A New Internal Overvoltage Protection Structure for the Bipolar Power Transistor

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Abstract—A new integrated structure for the internal overvoltage protection of a bipolar power transistor is presented which consists of the simultaneous integration of an interdigitated n-p-n (p-n-p) bipolar power transistor and a merged n-(p) channel enhancement MOSFET. The magnitude of the overvoltage protection for the bipolar power transistor is determined by the threshold voltage of the merged MOSFET, which can be controlled by the thickness of the gate oxide and the substrate doping of the merged MOSFET. A simple analytic model for the overvoltage protection has been developed. The fabrication techniques and design considerations of this integrated structure are discussed, and the applicability of the proposed structure is demonstrated experimentally.

I. Introduction

POWER integrated circuits have been recognized to be of great importance in system applications, as well as a challenging task for linear integrated-circuit designers and technologists. In the past ten years, there has been rapid progress in the fabrication technologies leading to higher current, higher voltage, and higher power semiconductor devices [1], especially in the development of package technologies capable of handling the heat-transfer requirements of more and more powerful chips. On the other hand, tremendous steps have also been taken in circuit design aimed at increasing the safety of power devices under the various types of overloaded conditions.

Among the protection circuits of a bipolar power transistor in a linear integrated circuit is a threshold circuit for a bipolar power transistor [2], which is shown in Fig. 1 where several Zener diodes, three resistors, and one bipolar transistor are used. In the above circuit, the magnitude of overvoltage protection is determined by Zener voltage and Zener diodes in series. When the collector-to-emitter voltage of the bipolar power transistor Q_1 is larger than V_z, the switch transistor Q_2 will operate in the saturation region, the base of the bipolar power transistor Q_1 will be approximately short circuited to the emitter, and then the bipolar power transistor Q_1 will be off. Obviously, the resistors and Zener diodes used need more isolation islands. Moreover, the minimum current gain is required to ensure the switch transistor Q_2 operated in the saturation region.

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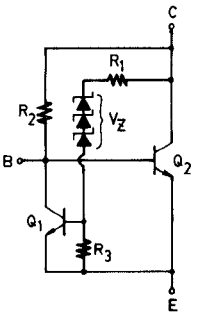

Fig. 1. Circuit diagram of a bipolar power transistor using Zener diodes, resistors, and a bipolar transistor for overvoltage protection.

In this paper, a simple integrated structure using an enhancement MOSFET for the internal overvoltage protection of a bipolar power transistor is presented and studied experimentally. Since the threshold circuit of the proposed structure consists of only one enhancement MOSFET, no additional isolation island is required for simultaneous integration, so less area occupation and simple design considerations are needed. The basic operational principle of the proposed structure for the overvoltage protection will be described in Section II where the expressions for the overvoltage detection and transition voltage are derived in terms of the basic device parameters. In Section III, design considerations and fabrication techniques of a bipolar power transistor with internal overvoltage protection are discussed. Moreover, the characteristics of the experimentally fabricated devices are compared to the results of the developed model in the section. In the last section, concluding remarks are given.

II. Basic Integrated Structure and Operational Principle

A schematic cross-section view of an n-p-n bipolar power transistor with an n-channel enhancement MOSFET as an internal overvoltage protection device is shown in Fig. 2(a) where only a single isolation island is used. Aside from the n^+-buried layer and deep collector diffusions, it is clearly seen from Fig. 2(a) that an interdigitated n-p-n bipolar power transistor and an n-channel enhancement MOSFET are fabricated simultaneously. The source and substrate of the n-MOSFET are internally connected together and then connected to the emitter of the interdigitated n-p-n bipolar

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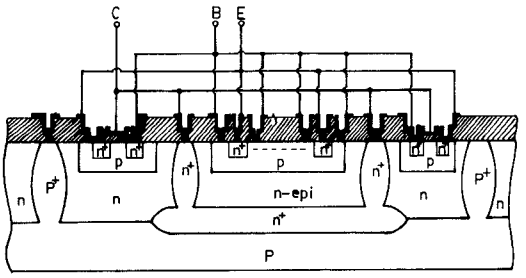


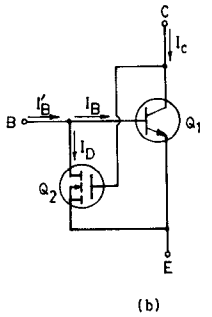


Fig. 2. Schematic diagram of a bipolar power transistor using one MOSFET for overvoltage protection. (a) Cross-section view of the integrated circuit. (b) Circuit representation.

power transistor by metallization, while the base and drain, the gate, and the collector are separately connected by using integrated-circuit metallization. With the connection in such a manner, the bipolar power transistor still maintains three terminals; however, the n-MOSFET behaves as a threshold detector. The equivalent circuit of this connection is shown in Fig. 2(b). This connecting configuration is slightly different from that of the LAMBDA bipolar transistor proposed previously [3]. The main difference is that the substrate of the n-MOSFET is connected to the base of the bipolar transistor in a LAMBDA bipolar transistor, while the substrate of the n-MOSFET is connected to the emitter of the bipolar transistor for protection application. Another difference is that the n-MOSFET as a protection device is fabricated in another p-well, while both the bipolar transistor and the MOSFET are fabricated in a single p-well for the LAMBDA bipolar transistor. These two different connections will produce a different current–voltage characteristic which will be discussed later.

From Fig. 2(b), it is clearly visualized that when an applied collector–emitter voltage V_{cE} is smaller than the threshold voltage of the n-MOSFET, the n-MOSFET is off; then the current–voltage characteristic is the same as that of an n-p-n bipolar transistor. Once V_{cE} exceeds the threshold voltage V_T of the n-MOSFET, the n-MOSFET is on; then the base current I'_B is partially taken out by the I_D of the n-MOSFET. Consequently, the actual base current of the n-p-n bipolar transistor is decreased; the collector current I_c is also decreased. When the base current I_B is wholly taken out by the I_D of the n-MOSFET, the n-p-n bipolar transistor is now operated in the cutoff region, and

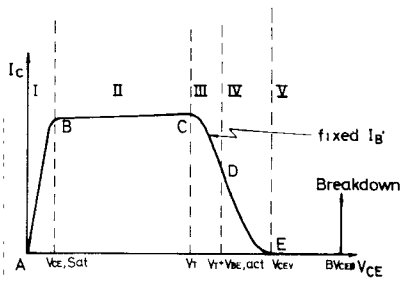


Fig. 3. The $I-V$ characteristic of the proposed overvoltage protection structure for a bipolar power transistor.

TABLE I
OPERATING REGION OF BIPOLAR POWER TRANSISTOR AND MOSFET IN AN INTEGRATED STRUCTURE FOR PROTECTION PURPOSE

Operating Region / Transistor	Region I	Region II	Region III	Region IV	Region V
Q_1	Sat	Act	Act	Act	Off
Q_2	Off	Off	Sat	Lin	Lin

the collector current of the bipolar transistor is equal to the collector reverse saturation current I_{cEo}. If the threshold voltage V_T of the n-MOSFET is much larger than the emitter–collector saturation voltage $V_{cE,\text{sat}}$ of the n-p-n bipolar transistor, then the general $I_c - V_{cE}$ characteristic of the n-p-n bipolar transistor with a fixed external base current drive I'_B is shown in Fig. (3) where the characteristic curve can be divided into five regions according to the operating points of the individual bipolar transistor and MOSFET as shown in Table I. However, the most interesting regions concerned with protection purposes are the transition region and the cutoff region.

The threshold voltage of the n-channel enhancement MOSFET may be expressed by [4]

$$V_T = \phi_{Ms} + 2\phi_{fp} - \frac{Q_{ss}}{C_0} + \frac{\sqrt{2K_s\epsilon_0 qN_{As}(2|\phi_{fp}|)}}{C_0} \qquad (1)$$

where ϕ_{Ms} is the work function difference of the gate metal with respect to the silicon substrate (p-type), ϕ_{fp} is the potential difference between the Fermi level and the intrinsic energy level in the substrate, C_0 is the gate oxide capacitance per unit area of the n-MOSFET, Q_{ss} is the surface fixed charge density of the Si–SiO_2 interface, N_{As} is the surface concentration of the base diffusion, K_s is the dielectric constant of silicon, and ϵ_0 is the permittivity of the free space.

It is clearly seen that higher surface doping concentration N_{As}, thicker gate oxide thickness, and lower interface fixed charge density will give a larger threshold voltage for an n-channel enhancement MOSFET, which tends to give larger overvoltage protection for the bipolar transistor. Note that although higher surface doping concentration may reduce the breakdown voltage of the drain junction, the emitter–base voltage of the bipolar transistor operated in the active region is always smaller than 1 V; hence, lower breakdown voltage in the drain junction does not

limit the normal operation for protection purposes. This is one of merits of the proposed structure. If the substrate of the n-MOSFET is connected to the base of the bipolar transistor, the substrate–bias effect will seriously reduce the threshold voltage of the n-MOSFET; then the $I-V$ characteristic will be the same as that of the LAMBDA bipolar transistor as described previously [3].

When the base current I_B of the n-p-n bipolar transistor is zero, the bipolar transistor will be operated in the cutoff region; the external base current drive I_B' will be equal to the drain current I_D of the n-MOSFET operated in the linear region. In this case, we may obtain

$$I_B' = I_D = \frac{Z\mu_n C_0}{L}(V_{cEv} - V_T)V_{BE,\text{cut in}} \tag{2}$$

where L is the channel length of the n-MOSFET, Z is the channel width of the n-MOSFET, μ_n is the electron mobility in the inversion layer, V_{cEv} is the collector–emitter cutoff voltage of the bipolar transistor, and $V_{BE,\text{cut in}}$ is the emitter–base voltage of the bipolar transistor operated in the cut-in condition.

From (2), the collector–emitter cutoff voltage of the bipolar transistor V_{cEv} may be written as

$$V_{cEv} = \frac{I_B' L}{Z\mu_n C_0 V_{BE,\text{cut in}}} + V_T. \tag{3}$$

The electron mobility in the inversion layer may be written as the following empirical form [5]:

$$\mu_n = KT^{-\alpha}(V_{Gs} - V_T)^{-\gamma} = KT^{-\alpha}(V_{cE} - V_T)^{-\gamma} \tag{4}$$

where α, K, and γ are the empirical constants which can be obtained by comparing (4) to that of experimental measurements. Note that α and β are always positive for higher applied gate voltage.

The transition voltage ΔV_t is defined as the voltage range of the differential negative resistance region, which may be easily obtained from (3) and (4). The result is

$$\Delta V_t = V_{cEv} - V_t = \left[\frac{I_B' L T^{\alpha}}{ZKC_0 V_{BE,\text{cut in}}}\right]^{1/1-\gamma}. \tag{5}$$

For protection applications, the transition voltage must be designed to be small. From (5), it is clearly visualized that a higher aspect ratio (Z/L), higher inversion layer mobility, and thinner gate oxide will give smaller transition voltage. However, thinner gate oxide thickness will give lower protection voltage as discussed previously; hence, a suitable compromise between the protection voltage and the transition voltage must be made. Nevertheless, a higher aspect ratio and higher surface doping concentration in the substrate of the n-MOSFET are needed for smaller transition voltage and larger protection voltage for a bipolar power transistor.

III. Experimental Results and Discussions

In order to show the capability of the proposed protection structure for the bipolar power transistor, three testing patterns are designed. Fig. 4 shows the metallization patterns of the designed mask in which the n-channel MOSFET is designed to surround the interdigited bipolar power transistor in order to obtain a higher aspect ratio for the n-channel MOSFET's. The specifications of these testing patterns are listed in Table II where the aspect ratios of the MOSFET's are 400, 300, and 100 for patterns 1, 2, and 3, respectively. For simplicity, the $\langle 100\rangle$ n/n^+ wafers with an epilayer resistivity of 8.7 $\Omega\cdot$cm and an epithickness of 17 μm are used as the substrate wafers throughout the experiments. The fabrication sequences are the same as those of the bipolar transistor. However, an additional mask is designed to regrow the gate oxide of the MOSFET, which can be used to obtain a different gate oxide thickness and to check the developed model described in the previous section. For practical applications, this additional mask is not necessary so that the diffusion profiles of the bipolar transistor will not be changed by simultaneously fabricating the MOSFET. Two typical $I-V$ characteristics of the fabricated bipolar power transistors with the MOSFET as the threshold detector are shown in Fig. 5 where Fig. 5(a) shows the overvoltage protection of 20 V and Fig. 5(b) shows the overvoltage protection of 80 V. Since the $I-V$ characteristic of Fig. 5 is measured by a Tektronix 576 in a probe station, the power dissipation of the fabricated devices is intentionally limited in order to prevent the devices from destruction; thus, a higher current characteristic does not appear in the presented photographs.

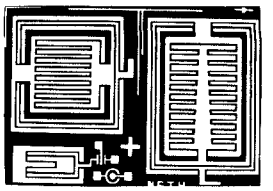
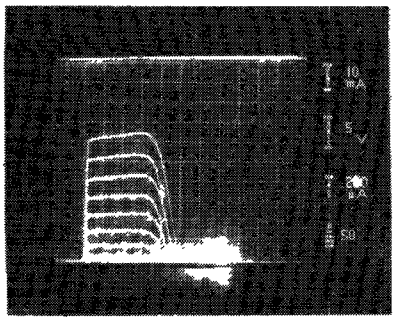


Fig. 4. Photograph of the metallization pattern in the designed mask.

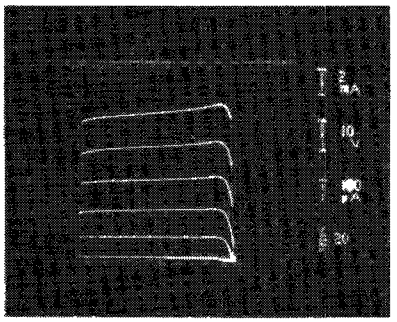
TABLE II
Specifications of the Designed Mask

Pattern Number	1	2	3
Channel length (μm)	15	15	
Channel width (μm)	6000	4500	1520
Base area (cm^2)	1.5×10^{-2}	1×10^{-2}	4.5×10^{-3}
Emitter area (cm^2)	9.5×10^{-2}	3.78×10^{-3}	1.32×10^{-3}
Emitter periphery (μm)	15400	13200	1540
Base corner radius (μm)	50	50	50
Emitter finger width (μm)	70	60	85
Emitter finger length (μm)	350	700	380
Number of fingers	22	8	2

In order to compare the fabricated characteristics to the design equations developed in the previous section, a different gate oxide thickness and surface doping concentration for the MOSFET's are fabricated. The flatband voltage of the fabricated MOSFET was measured from the controlled samples by using $C-V$ measurements, and the surface doping concentration of the MOSFET was



(a)



(b)

Fig. 5. Photographs of the $I-V$ characteristic of the fabricated devices. (a) Low protection voltage (LBT-423). (b) High protection voltage (LBT-613).

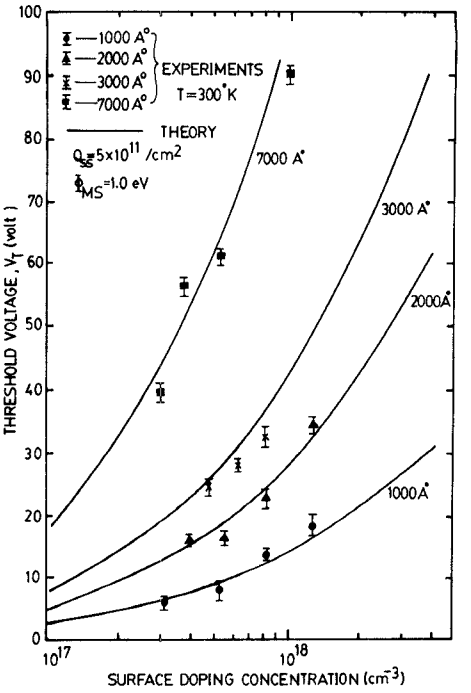


Fig. 6. Threshold voltage as a function of surface doping concentration in the substrate of the n-channel MOSFET for different gate oxide thicknesses.

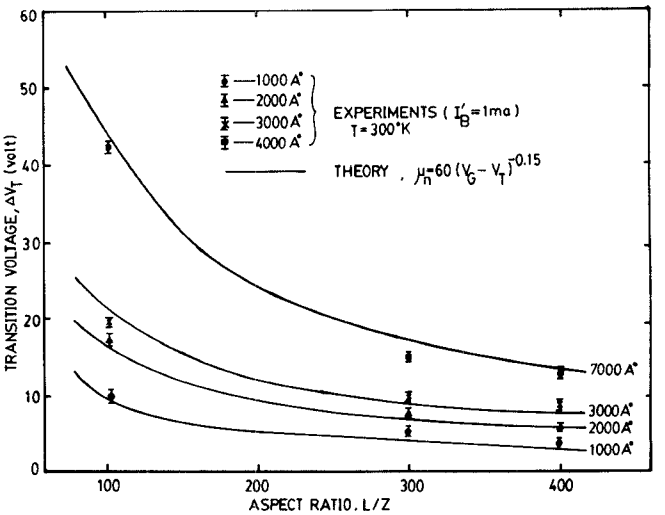


Fig. 7. Transistion voltage as a function of the aspect ratio of the n-channel MOSFET for different gate oxide thicknesses.

measured by using spreading resistance probe (Mazur 100). Fig. 6 shows the threshold voltage measured from the fabricated devices as a function of surface doping concentration for different gate oxide thickness, in which the solid curves represent the theoretical calculations using (1) and the parameters used are also cited. It is clearly seen that fairly good agreement between the measured data and theoretical prediction is obtained. Moreover, it is shown that the maximum protection voltage of about 90 V can be obtained from the proposed structure. Fig. 6 shows the transition voltage of the fabricated devices as a function of the aspect ratio of the MOSFET's for different gate oxide thicknesses, in which the solid curves represent the theoretical calculations using (5) and the empirical constants for mobility are also cited. It is clearly visualized that the presented simple model can fairly predict the experimental observations.

It should be noted that the final thickness of the gate oxide will be the same as that of the protection oxide on the active base region after finishing the emitter diffusion process if the additional mask is not used. Hence, the thickness of the gate oxide still can be controlled as desired if the ambient dopant drive-in processes can be properly chosen. For example, the steam ambient in a conventional drive-in process can be changed by using both steam ambient and dry O_2 ambient with different drive-in time. If an additional mask is used to regrow the gate oxide in low-temperature plasma oxidation, then ion implantation can be used to adjust the surface doping concentration of the n-MOSFET. These give another flexibility to obtain the desired protection voltage for the bipolar power transistor. Similarly, the proposed protection structure can be easily applied to the case of the p-n-p bipolar power transistor. It is worth noting that a higher protection voltage needs a thicker gate oxide in order to prevent the gate oxide from breakdown, as indicated in Fig. 6. This consideration has been a common practice in designing high-voltage MOSFET's. With regard to the transient behavior of the present structure, the on–off switching time is much less than 1 μs, as demonstrated in a recent publication [6]. In order to improve the transient behavior, the self-aligned silicon-gate technology must be used for the threshold detector (MOS device), which reduces not only the gate–source capacitance, but also increases the transconductance of the MOS device.

IV. Conclusion

In this paper, a new overvoltage protection structure for a bipolar power transistor has been proposed and studied. This protection structure consists of only one merged MOSFET, which can be simultaneously fabricated by using existing bipolar integrated-circuit technologies. The major advantage of the presented protection structure is that the protection device can be simultaneously integrated without additional isolation islands, which may reduce the chip area when compared to the protection circuit using a resistor, Zener diodes, and bipolar transistor. Since the protection device is only a MOSFET and the magnitude of overvoltage protection is the threshold voltage of the MOSFET, the magnitude of overvoltage protection can be controlled by existing technologies. However, in the protection circuit using Zener diodes, the magnitude of overvoltage protection is equal to the total Zener voltage of Zener diodes in series, which produces quantum jumps depending on the number of Zener diodes in series. Moreover, in this paper, a very simple model for designing the protection device has also been developed. It has been shown that the developed model is in fairly good agreement with the results of the fabricated devices.

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References

[1] S. K. Ghandhi, *Semiconductor Power Devices*. New York: Wiley, 1977.
[2] B. Murari, "Power integrated circuits: Tradeoffs and solutions," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 307–319, June 1978.
[3] C.-Y. Wu and C.-Y. Wu, "An analysis and the fabrication technology of the LAMBDA bipolar transistor," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 414–419, Feb. 1980.
[4] A. S. Grove, *Physics and Technology of Semiconductors*. New York: Wiley, 1969, pp. 218–220.
[5] F. F. Fang and A. B. Fowler, "Transport properties of electrons in inverted silicon surfaces," *Phys. Rev.*, vol. 169, pp. 613–631, May 1968.
[6] C.-Y. Wu and C.-S. Lee, "A new high power voltage-controlled differential negative resistance device—The LAMBDA bipolar power transistor." *IEEE Electron Device Lett.*, vol. EDL-4, Apr. 1983.

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